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The state of state machines

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APPLICATIONS
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The PC82 Universal Programmer and Tester is a PC-based development tool designed to program and test more than 1500 ICs. The latest version of the PC82 is based on the experience gained after a 7 year production run of over 100,000 units.

The PC82 is the US version of the Sunshine Expro 60, and therefore can be offered at a very competitive price for a product of such high quality. The PC82 has undergone extensive testing and inspection by various major IC manufacturers and has won their professional approval and support. Many do in fact use the PC82 for their own use!

The PC82 can program E/EPROM, Serial PROM, BPROM, MPU, DSP, PLD, PEEL, GAL, FPL, MACH, MAX, and many more. It comes with a 40 pin DIP socket capable of programming devices with 8 to 40 pins. Adding special adaptors, the PC82 can program devices up to 84 pins in DIP, PLCC, LCC, QFP, SOP and PGA packages.

The unit can also test digital ICs such as the TTL 74/54 series, CMOS 40/45 series, DRAM (even SIMM/SIP modules) and SRAM. The PC82 can even check and identify unmarked devices. Customers can write their own test vectors to program non standard devices. Furthermore it can perform functional vector testing of PLDs using the JEDEC standard test vectors created by PLD compilers such as PALASM, OPALjr, ABLE, CUPL etc. or by the user.

The PC82’s hardware circuits are composed of 40 set pin-driver circuits each with TTL I/O control, D/A voltage output control, ground control, noise filter circuit control, and OSC crystal frequency control. The PC82 shares all the PC’s resources such as CPU, memory, I/O hard disk, keyboard, display and power supply.

A dedicated plug in card with rugged connecting cable ensures fast transfer of data to the programmer without tying up a standard parallel or serial port. Will work in all PC compatibles from PC XT to 486.

The pull-down menus of the software makes the PC82 one of the easiest and most user-friendly programmers available. A full library of file conversion utilities is supplied as standard.

The frequent software updates provided by Sunshine enables the customer to immediately program newly released ICs. It even supports EPROMs to 16Mbit.

Over 20 engineers are employed by Sunshine to develop new software and hardware for the PC82. Not many competitors can boast of similar support!

Citadel, a 32 year old company are the UK agents and service centre for the Sunshine range of programmers, testers and in circuit emulators and have a team of engineers trained to give local support in Europe.
FEATURES

ADD ON A SPECTRUM ANALYSER ............................................ 982
Spectrum analysers are invaluable in R\textsuperscript{2} design but are expensive. Ian Hickman presents a modular analyser design which delivers useful performance at an affordable price. This oscilloscope add-on can display a 0 to 400 MHz sweep with a true logarithmic input amplitude response.

PC ON A CHIP ................................................................. 1003
One chip now runs software eight times as fast as the original XT computer system. David Guest investigates the single chip PC's features and compromises.

DISTORTION IN POWER AMPLIFIERS ............................ 1009
Is class AB better than Class B? Doug Self analyses audio power stage configurations and draws some interesting conclusions.

WORKING WITH PROGRAMMABLE LOGIC .................. 1017
Sequential logic - Registered functions, and state machines in particular, can fit into registered PALs or field programmable logic sequencers. As with combinatorial logic, each needs to be decided on its merits. Geoff Bostock explains the ground rules.

THE FACTS AND FIGURES OF RECEIVER PERFORMANCE .......... 1026
In receiver specifications, static performance figures are useful, but nowhere near as much as dynamic parameters. Jon Dyer cuts through the haze of misunderstanding surrounding HF receiver design.

USING RF TRANSISTORS ............................................... 1049
A key criterion in RF circuit design is choosing the right transistor. Motorola applications engineers Norm Dye and Helge Granberg consider the important parameters for both power and small-signal devices in bipolar and power mosfet form.

REGULARS

COMMENT ................................................................. 971
New challenge for amateur radio.

UPDATE ................................................................. 972
ISDN does it now, Mirror, mirror on the chip, Video disc recorder may rival tape, Dodge chips beat gold and drugs, Antenna boost for cellular phones, Joint development sees 64Mbit dram samples, Esprit to go more commercial, Philips to make monitor tubes in Austria.

RESEARCH NOTES ................................................................. 976
Can noise improve your hearing? Fermat's ghost laid to rest? Laser/sound will declog your tubes … or simply steam them, Superconducting barrier starts to melt.

CIRCUIT IDEAS ................................................................. 993
Variable-inductance, low-frequency VCO, DS1233 replaces monostable, PC uses parallel printer port, Under-frequency inverter protection, Single-diode full-wave rectifier.

LETTERS ................................................................. 996
Dirty Windows: out in the cold, kids playing, too slow, Relay breakdown, Spectrum space, Absolute test not needed, Neural emissions, Give Workbench a chance, CFA: the last word? Respect the giants.

NEW PRODUCTS ................................................................. 1039
EW + WW's pick of new offerings in electronics and production engineering technology.

APPLICATIONS ................................................................. 1034
Power factor control, switching power, PABX on a chip, better LCD backlighting.

In next month's issue: Designing a microprocessor controlled power supply. Matthew Rahman details a fully keypad-programmable, multi-rail laboratory instrument. His article provides detailed circuits and documented source code for the Z80 processor at the heart of the design. This code will be made available to readers on disk.

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New challenge for amateur radio

When was the last time that you read or heard something positive about amateur radio? I can’t remember either. Everyone recalls and enjoys the Hancock sketch where the man himself played a pompous, petty and technically incompetent ham communicating with a world where everybody wanted to talk and nobody wanted to listen. We remember Tony Hancock’s radio amateur because it encapsulates truth about the hobby more accurately than any words that we might write about it. Amateur radio desperately needs a new reason for its continued existence.

Radio communications was the principal driving force behind electronics development from its beginnings until the end of the second World War. It was used to tie empires to their mother countries, and then as an instrument of war itself when empires disintegrated. Radio hams found themselves involved in research and development especially in the early days of radio, and then as a source of specialised skills in the war years. There was a post-war surge of interest fuelled by the availability of surplus equipment, most of which required technical competence to adapt for amateur use. But when this was gone, radio amateurs became simple consumers and mostly bought their equipment off the shelf losing much of their technical independence and usefulness. Garton and Simpson were now able to document Hancock’s radio ham.

Somewhat paradoxically, the intellectual decline in amateur radio reached a trough when the numbers engaged in the hobby peaked in the early Eighties. Two factors combined and contributed in this. Firstly, the multiple choice entrance examination was an order of magnitude easier to pass than its written predecessor; secondly, radioamateurs as a hobby was massively popularised by the CB boom. Most of the new influx could contribute nothing except self-conscious and inane chatter using equipment which owed more to credit card companies than the owners’ technical competence. We are now seeing a decline in the number of radio amateurs as the novelty wears off.

Naturally, this jaundiced view does not tell the whole story. One only has to look to the work of Amateur satellite groups and the activities of Surrey University to appreciate that some aspects of the hobby remain challenging, educational and useful. A few enlightened souls still manage to push the bounds of RF design engineering, usually by combining the demands of their jobs with the pursuit of their hobby. But if amateur radio is to command any respect – and retain its frequency allocations and privileges – it must take up new challenges.

The market requirement for cordless communications once again casts RF engineering as a driving technology. While it seems unlikely that amateur radio could contribute directly at chip level development, it has a role to play in enthusing and educating the next generation of RF engineers. As editor of this magazine, I hope to hear from radio amateurs prepared to experiment with direct digital synthesis, IF band DSP, spread spectrum communications, high performance small signal and large signal RF systems, broadband design techniques and packet transmission, etc.

If amateur radio finds itself incapable of, or indifferent to accepting a new challenge, then it does not deserve to survive.

Frank Ogden G4JST.
Virtual application or virtual reality? ISDN promises telepresence by allowing the direct transmission of digitised, compressed video images over the public switched network. Real applications, such as remote data gathering, are only just starting to appear.

Mirror, mirror on the chip

The possibility of aluminium mirrors projecting TV images from conventional cameras takes a step closer this month as scientists from Texas Instruments explain that they have improved the contrast ratio of their micromirror device to a level that can compete with standard CRTs. This picture was reconstituted by video codec at Reuters’ west London studio.

More mundanely, ISDN is transmitting high-quality artwork between studios and clients, and letting users access and search photo libraries – and receive the images – by phone. House hunters can view properties without leaving estate agents’ offices, and car buyers specify the options they would like, build the model on screen and view it from various angles, outside and in. Hairdressers can show customers how they would look with various styles, called up from a centralised databank and framed around their own faces.

In France the FNAC record store chain already has in-store multimedia music sampling terminals updated by ISDN.

The technical and human possibilities of ISDN, however, far exceed the replacement of motorcycle couriers or provision of a telephone jukebox. Peter Cochrane, research manager at BT’s Marlsham Heath laboratories, described them as “virtual teleporting”.

“Of necessity,” he said, “we are going to have to replace physical travel with telecommunications and telepresence.” He looks forward to “being able to communicate with other human beings on the basis of eye-contact, gaze awareness – right size, right colour, looking real.” As an end-to-end digital link with bandwidth in excess of 50 kbit/s, conveying sound, video, text and data in broadcast quality, virtually error free, ISDN will soon provide that facility. Already, via endoscopy, a surgeon can hold a case conference, in effect inside a patient who is many miles away, with colleagues also at distant locations.

At Southampton, BT introduced a surrogate head, using 3D wideband ISDN technology. A user on-site wearing lightweight cameras on spectacle frames, transmits virtual reality images back to, for example, a technical expert or a surgeon, who can conduct the repair, examination or operation without leaving his or her base.

“Virtual reality may take out multimedia,” predicted Cochrane. “It’s much more natural and versatile.”

The other advantage of ISDN is its economy of telecommunications capacity. Cochrane predicts that the local call area will grow quickly at national and continental level to become global. Even now, NatWest Securities can send closing prices from the Paris Bourse to Edinburgh in 25s. A fashion retailer has reduced overnight polling (data-gathering) from 15min to 35s per store.

Although ISDN is at its best on fibre optics, it can be carried on existing paired copper cables – usefuly increasing their capacity – in a service called ISDN 2.

A package for retailers proposes to put all their voice links, epos data polling, credit card authorisation, and security video monitoring, each of which has its own dedicated line, onto one ISDN 2 line. As the Whitbread sailors are being pounded around the world on the ocean wave they can reflect on the irony that the technology they are helping to test will one day mean that no-one need leave home again.

Peter Willis
Engineers at Samsung's Advanced Institute of Technology are close to developing a digital video recorder using discs instead of tape.

Scheduled for launch in 1995, the machine will use magneto-optical readable discs. But the Korean company can expect fierce competition from Japanese competitors such as Matsushita and Sony.

Both are working on digital video disc and tape recorders. Samsung hopes that the key laser component, developed with Russian engineers, will put it ahead of the Japanese by several years.

Korean electronics companies Samsung, Goldstar and Daewoo have the reputation of being efficient, low cost makers of technology developed elsewhere. Samsung, though wants to start setting new standards.

When broadcast tv pictures are converted into digital code, the data stream runs at more than 200Mbit/s. Data compression according the MPEG-2 standard can reduce this by about 30:1 to 8Mbit/s, while still delivering quality that matches the Super-VHS tape system. But at this data rate a delivery time of 110min on a single disc. The first step will employ new technology developed elsewhere. Samsung thinks the help it got from Russian engineers to Korea for two years to work the D-VDR.

The technique is known as second harmonic generation. The source light is infrared pumps the yag in a lasing action that emits coherent light of a wavelength around 1µm. This light is then beamed into a second crystal of KTP (potassium titanyl phosphate) that has a non-linear optical characteristic and generates a second harmonic of the input frequency at 0.5µm. Thus the system emits coherent green light at a power of 20mW, strong enough to record onto the disc.

The US military has been working on the same technique to communicate with submarines, because see water has an optical window at this wavelength. Very probably the work done in Russia was originally commissioned by the military. The practical difficulties, for instance keeping the infra-red laser cool enough to avoid self-destruction, have deterred electronics companies from trying to use the system for consumer products. US researchers used Peltier junctions. Samsung thinks the help it got from Russia makes the system affordable.

Said Insik Park: "Russian engineers are a lot cheaper than Japanese, and Japanese are reluctant to transfer technology. So it is much easier to hire Russian engineers.

There is no high power solid state green laser yet but in 1991 SAIT engineer Insik Park went to Russia and saw how the IOFFE Technical Institute in St Petersburg was getting green light from infra-red lasers. Samsung signed a deal which brought Russian engineers to Korea for two years to work the D-VDR.

Said Insik Park: "Russian engineers are a lot cheaper than Japanese, and Japanese are reluctant to transfer technology. So it is much easier to hire Russian engineers.”

Samsung's storage target is a feature film DVD-recorder spread out over a laboratory bench. This makes the 1995 target for a consumer launch seem optimistic but Samsung has a good track record of delivering promises on time.

Barry Fox

**Video disc recorder may rival tape**

**Dodgy chips beat gold and drugs**

Stolen chips are worth more than gold or drugs, according to police fighting a growing microprocessor crimewave in Silicon Valley.

But some firms are fighting back. Intel is giving its microprocessors serial numbers following robberies that have led to a thriving grey market in 486 chips.

Intel will stamp serial numbers on its microprocessors and possibly extend the numbering system to other products. Other US semiconductors makers are also expected to announce that higher priced chips will have serial numbers.

In the most recent armed robbery, TEG Micro Technology in Fremont, California had more than $500,000 worth of chips stolen, mostly i486 microprocessors valued at more than $400 each. Two other armed robberies of Fremont businesses netted more than $300,000 worth of chips just weeks before the latest robbery.

Police say robbers can easily unload the chips in the grey market. Once they reach the grey market they are untraceable.

The serial number scheme is also intended to prevent the growing number of thefts by chip company staff who can easily smuggle out a handful of chips and earn hundreds of dollars.

Police say more chips are lost through staff theft than armed robberies.
Antenna boost for cellular phones

A redesigned antenna looks set to save costs and give better coverage for cellular telephone services.

Called SmartAntenna and developed by Northern Telecom, the device uses four flat antenna panels mounted on a mast. Each panel can send out five overlapping beams that can be individually adjusted for strength.

This means the coverage area can be tailored to requirements with higher strength beams hitting up areas, for example.

It also gives more flexibility in the positioning of the antenna; the base station no longer needs to be at the centre of the cell.

The mast is connected to a control module and radio base station in a cabinet at the foot of the tower. Active electronics in the masthead and cabinet comprises five functional blocks. The first is the antenna array itself along with beamformers and duplexers. Secondly, there is the switch matrix for transmit and receive that switches multiple transceivers into a single beam.

Dual redundant low noise amplifiers for each receive beam are fitted in the masthead equipment.

The control module in the cabinet is responsible for switching the best transmit and receive beams to each of the transceivers on a timeslot by timeslot basis. Selection of the best beam is made according to received signal amplitude.

Finally, transmit power amplifiers, hybrid combiners and duplexers are fitted at the masthead. Test and alarm functions are distributed throughout the system.

Each plate antenna covers a 90° arc with its five beams. Each beam covers a fixed 18° arc and is controlled by changing the gain. Because of the higher gain, the antenna has about twice the range of a standard omni cell in rural areas, which can cut the number of base stations by up to 75% compared with omni cell sites and 50% compared with tri-sectored cell sites.

Improved carrier to interference ratio allows greater frequency re-use. Each time slot of each transceiver can be allocated to any mobile on any radial beam. Shadowing caused by buildings is also cut, reducing the number of dropped calls from mobile users.

Increases in receive sensitivity let mobiles transmit at lower power, increasing battery life and talk time.

Nortel Matra’s cellular PCS system for providing DCS1800 networks in Europe will be the first to use the antennas.

Joint development sees 64Mbit dram samples

Siemens and IBM are sampling the 64Mbit dram they co-developed, but have yet to decide whether they will combine forces to make it.

Asked if sampling the chip to potential customers meant Siemens intended to supply it as a product, a representative replied: “If we are sampling I understand that someone might be interested to supply it as a product, a representative. “We’ll decide later next year.”

But he added: “Our development agreement with IBM does not include joint manufacturing.”

Siemens’ options on making the chip are “completely open” he said. “Both parties are negotiating the question what to do now."

IBM and Siemens reckon the decision is not urgent because first production of the 64Mbit will not be required until late 1995, ramping up to volume production in 1996.

“We are not in a hurry,” said the Siemens representative. “We’ll decide later next year.”

Since it takes 18 months to build a wafer fab and bring it into production, the building works would have to be started in June 1994 for there to be any chance of making first silicon by late 1995.

As well as the 64Mbit deal, Siemens and IBM jointly make 16Mbit drams and share with Toshiba a joint research and development effort on the 256Mbit dram.

Esprit to go more commercial

The vice-chair of the European Commission, Martin Bangemann, has challenged critics of EC funded research saying future Esprit programmes will be tailored to produce more commercial results and products.

The fourth framework of projects to be awarded under the Esprit programme will, he said: “not only focus on technical challenges, but will ensure that the special activity will be noticed by the general public.”

Bangemann, who is also commissioner in charge of information technology, said the previous policy of Esprit projects concentrating on “precompetitive development” led to accusations that the commission was spending money on nothing.

He rejected such charges saying: “It is not true that our programmes have no results, but the wider public is often unaware of them.”

Bangemann was speaking at the launch of Goldrush, a computer from ICL that uses parallel processing technology. It was developed as part of an Esprit project called EDS.

Goldrush is a database server that can have up to 127 hypersparc rise microprocessors.

Bangemann said: “Our future depends on quick acceptance of developments. We must see to it that European enterprises gain advantage through early access to products offered.”

Philips to make monitor tubes in Austria

Philips is to start producing colour monitor tubes at its factory in Lebring, Austria.

About 29 million Dutch guilders are being invested to add 0.4 million monitor tubes to the 2 million cathode ray tubes already produced.

European demand for monitor tubes is expected to double from 2.5 million pieces a year to 5 million by 1997.

Monitor tube production will start late next year ending the monopoly of imports from the Far East. First off the line will be 15in tubes followed soon by 17in models.

Around 40 jobs will be created and some existing staff will be retrained to work on the new line. Philips already produces 2.5 million monitor tubes a year at its Taiwanese factory.
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RESEARCH NOTES

Can noise improve your hearing?

Traditional engineering wisdom takes for granted the assumption that you can hear better in a quiet environment. But workers in the US have been questioning that fact by using increased background noise to improve s/n ratios – with a little help from a crayfish.

In electronics design, great emphasis has always been placed on low-noise circuitry, whether for domestic audio or in rf front-ends listening for errant Martian spacecraft.

According to conventional linear information theory, random noise is detrimental to the transmission of data: end of argument... well, not quite.

Frank Moss and colleagues from the University of Missouri at St Louis have shown that a small amount of random noise may enhance, rather than obscure weak signals. Experiments to confirm this speculation (Nature, Vol 365, No 6444) were conducted, not with conventional electronic components, but with pick-up devices unlikely to be found in the average engineer’s toolbox. Moss and his team used specialised biological cells called mechanoreceptors, taken from crayfish tails.

As the name suggests, the normal function of these cells is to detect tiny water movements that might signal the presence of some larger and hungrier species. Because they are always working at (or beyond) the limits of conventional information theory in a permanently noisy environment, they were regarded as a good starting point to investigate the possibility of enhanced signal-to-noise performance.

The rather counter-intuitive notion that noise might actually improve performance derives from some research conducted over a decade ago into periodicities in climate. This work, together with later theoretical studies, showed that, in certain non-linear systems, the information content of a weak signal can be enhanced by noise through “stochastic resonance” in which the output coherence relative to the input noise passes through a maximum at an optimal value of the input noise. In other words a little noise does you good.

At the University of Missouri, Moss and his colleagues wired up the crayfish cells and stimulated them by moving water back and forth. The cells are so naturally sensitive that the equipment had to be isolated from everyday building vibrations at 10Hz and lower. What the team were trying to assess was the extent to which randomly introduced water fluctuation affected the cells’ ability to respond to regular periodic fluctuations.

When the effective signal-to-noise ratio of the system was computed from the measured electrical activity of the cells, Moss found very clear evidence of a certain noise intensity at which the s/n is a maximum. This improvement is about 4.5dB compared with the figure in the absence of noise.

Whether this enhancement is something that Nature has evolved to make the best of a noisy environment is a question as yet unanswered. But it does seem that the crayfish is by no means unique. Moss and his colleagues draw attention in their paper to various psycho-physical studies that have hinted at the existence of this effect in human visual perception. People, it seems, are much better at perceiving ambiguous shapes when they are presented in the context of visual “noise”. Stochastic resonance is clearly not something which will improve the performance of conventional linear transducers. But in any artificial intelligence system or information processing context where non-linearity plays a part, we might well learn a lesson or two from the humble crayfish.

Fermat’s ghost laid to rest?

For close on 400 years mathematicians have puzzled over one of the most intriguing numerical mysteries, the so-called last theorem of Pierre de Fermat. Fermat was a 17th century Frenchman who asserted that, for any whole number n greater than 2, the equation \( x^n + y^n = z^n \) has no solution for which x, y and z are whole numbers greater than zero. What makes this assertion so intriguing is Fermat’s tantalising hint that he knew a wonderful proof. But Fermat claimed he had no space in his notebook to write it down. The search for it has been a challenge to mathematicians ever since.

Over the years, the “theorem” has been verified in different ways for a variety of specific values of n. Number-crunching computer studies in the USA have recently validated Fermat’s assertion for values of n up to 4 million. But a general proof has remained elusive... until a surprise announcement by Andrew Wiles, a British mathematician working at Princeton University.

Wiles’ breakthrough follows some ground-laying by other workers who have progressively established links between Fermat’s assertion and the properties of elliptic curves. Key to this is the so-called Taniyama conjecture, named after the Japanese mathematician Yutaka Taniyama. Proof of the Taniyama conjecture is generally agreed to amount to proof of Fermat’s theorem.

Andrew Wiles has now presented a 200 page proof of the Taniyama conjecture, causing excitement for mathematicians all over the world – those who can understand it!

Some experts are saying that Wiles proof might take as long as a year to check over thoroughly, though it is said to look good. Establishing Fermat’s assertion as a true theorem – something that can be proved as a general statement – will be far more than just a tour de force of number crunching. Mathematicians who have studied Wiles’ work say that it will provide a valuable new tool to open up whole areas of number theory. One wonders if that’s what Pierre de Fermat had in mind all those years ago.
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CIRCLE NO. 104 ON REPLY CARD
Laser/sound probe will declog your tubes...

Development by a UK team of a miniaturised probe that makes use of a laser's ability to cut as well as its ultrasonic characteristics could transform laser surgery of clogged arteries from the possible – into the practical.

Clogged arteries (atherosclerosis) are among the main causes of strokes and heart attacks. What happens is that a lining of cholesterol and similar fatty materials builds up in the form of plaques on the arterial walls until the blood supply is blocked or dangerously restricted. Doctors have long been trying to treat such blockages with drugs, by mechanically scraping away the cholesterol, by balloon angioplasty (stretching the artery walls) and by bypass surgery. More recently it has been shown that atherosclerotic plaques can be blasted away with pulses of powerful laser light.

But though enough laser energy can be fed along a fibre-optic catheter into some of the bigger blood vessels, laser ablation is not an easy technique. It is made particularly difficult by the fact that, while X-rays can be used to guide a catheter, they will not show up the soft walls of the vessels.

Most therapeutic systems incorporate a second catheter, carrying an ultrasound probe to provide pictures on a screen for the surgeon to study. The only problem is that not many blood vessels are big enough to take two catheters at once, especially if they are already half blocked.

A new approach to this problem has been described (Electronics Letters. Vol 29. No 18) by a team of researchers at Umist and the Killingworth Hospital in Leeds. They have developed an experimental system that should eventually make it possible, using a single catheter, to image the body tissue at the same time as treating it with laser ablation.

The single-catheter probe makes use of the fact that laser light can induce its own ultrasonic vibrations when it hits a target. The team showed that usable ultrasonic signals could be generated in an experimental human finger using laser pulses with an energy of around 3mJ. This (thankfully for the volunteer) is enough to produce good images, but not enough to do any damage. In the experimental set-up, the energy was delivered along exactly the same 600μm core fibre that is used at higher powers for ablation treatment.

In their experiments, the team successfully picked up ultrasound echoes using a 3mm diameter polymer transducer fitted around the tip of the optical fibre. They say that further miniaturisation should lead to a whole range of medical applications apart from combining intra-arterial imaging with laser ablative therapy.

...or simply steam clean them

Researchers at Sandia National Laboratories in Albuquerque, New Mexico, have developed a steam engine smaller than a pinhead. The special motor is designed to power the growing number of micromechanical devices found in everything from weapons to medical equipment. Engineers have been able to machine tiny gear wheels, axles and ratchets no bigger than a few microns across, for some time. Manufacturing techniques are borrowed from the world of chip fabrication, where etching of components this size is routine. But the main problem with micromechanical devices has been to find a suitable micro-motor to power them. You can scale down a gear wheel to micron dimensions, but not a diesel engine or even a conventional electric motor or actuator; there are simply too many parts.

Micro-mechanical engineers machines have been forced to make do with experimental human finger using laser pulses with an energy of around 3mJ. This (thankfully for the volunteer) is enough to produce good images, but not enough to do any damage. In the experimental set-up, the energy was delivered along exactly the same 600μm core fibre that is used at higher powers for ablation treatment. In their experiments, the team successfully picked up ultrasound echoes using a 3mm diameter polymer transducer fitted around the tip of the optical fibre. They say that further miniaturisation should lead to a whole range of medical applications apart from combining intra-arterial imaging with laser ablative therapy.
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Superconducting barrier starts to melt

High temperature superconductivity is back in the news with an announcement that scientists may be on the brink of ambient pressure superconducting at over 150K.

The excitement has been created by Paul Chu and associates at the University of Houston in Nature, Vol 365, No 6444. If their results are anything to go by, it looks as if we are set for another sharp rise in $T_c$, the critical temperature at which any material has yet to become superconducting at 135 degrees above absolute zero. These layer compounds contained mercury in addition to barium, copper and oxygen and were a triumph of laboratory cookery.

Theory, for the most part, lagged behind patient empiricism. Paul Chu’s latest step forward (or upward) is the result both of meticulous experimental technique and also a critical analysis of progress so far.

“We found that the structure of the mercury-containing compound is rather different from others. That gave us the hint that the application of pressure would raise the temperature substantially,” he says.

Using a ceramic based on mercury, barium, calcium, copper and oxygen, Chu found that a $T_c$ of 153K could be achieved at a pressure of 150kbar. This is the highest temperature at which any material has yet exhibited superconducting properties — though the theoretical underpinning is still rather sketchy. “Two things happen,” says Chu. “One is that we reduce the interatomic distances. As a result, some of the electrical charges move through the copper/oxygen layer, the active component of the material, more easily. Therefore the critical temperature goes higher.

“In addition to that we’ve now found another factor. But the details of that are still unknown. We’re still trying to find out.”

That modest assessment of this pioneering work belies the real progress that has been made. Paul Chu and his colleagues have now assembled enough theoretical understanding to be able to predict the next step with confidence. Instead of using high pressures, they aim to make use of clever chemistry. As Chu observes: “High pressure brings atoms closer together, and there are chemical ways of doing the same thing. So by using chemical substitution, we hope to retain a high critical temperature at atmospheric pressure.”

Early substitution attempts have so far not proved successful, mainly because attempts to tinker with the chemistry have disturbed the structure of the molecular lattice. But the team confidently expect to make a material that will become superconducting at 150K before very long.

Practical room-temperature superconductors are of course still a long way off, and even the existing high $T_c$ ceramics are not without considerable manufacturing and operating problems. Physical brittleness and the loss of superconducting properties in the presence of strong magnetic fields are but two major obstacles. But if the history of this fascinating subject is anything to go by, there is bound to be more unexpected progress just when everyone is becoming complacent. Such is the nature of scientific discovery.

Research Notes is written by John Wilson of the BBC World Service.
Encounters with RF are much easier if a spectrum analyser is to hand. Although based on a commercial TV tuning head, Ian Hickman's design delivers linear, useful performance in its basic form and may be adapted to a much higher degree of sophistication including continuous coverage and wider frequency span.

A n oscilloscope is undoubtedly the basic tool of the trade in general electronic design and development work. For investigating RF equipment, an instrument of sufficient bandwidth is a help and certainly much better than nothing.

A standard spectrum analyser is expensive; even a second hand model will cost the best part of £2000. An add-on box to the ubiquitous oscilloscope provides a much cheaper alternative. The design shown here is capable of further development in several directions, so this article should be regarded as a starting point.

As it stands, it has its limitations so I think of it more as a spectrum monitor rather than a spectrum analyser. Nevertheless, it has already proved itself useful and would be even more so with suggested further development.

The spectrum monitor is built around a TV tuner, the particular one used here is a beautifully crafted all surface-mount example, the Toshiba EG522F. Possible suppliers of this unit are given in Ref. 1.

The EG522F provides continuous coverage from the bottom of Band I to the top of Band III in two ranges, a third range covering Bands IV/V. There is a gap between the top of Band III and the bottom of Band IV; the continuous coverage tuner mentioned in Ref. 2 is apparently no longer available. The design of this spectrum monitor is generally applicable to most types of TV tuner and any necessary circuit modifications should be straightforward.

It was desired to give the finished unit as much as possible of the feel of a classic spectrum analyser rather than the current generation of push-button controlled instruments. The design challenge was to leave the way open for further development if required. To
this end, within its case the monitor was constructed as three separate units—PSUs, sweep generator, RF/IF unit—interconnected by ribbon cables.

Power rails are ±15V for general analog circuitry, +12V for the tuner and +30V for its tuning varactor supply. Fig. 1, terminating in a 7-pin plug accepting a mating ribbon-cable-mounted socket (RS “inter PCB crimp” style).

Sweep circuitry

The sweep circuitry to drive the tuner's varactor tuning input is shown in basic form in Fig. 2a. This produces a sawtooth waveform of adjustable amplitude and fixed duration symmetrically disposed about ground. This means that as the span (the tuning range covered by the monitor) is increased or decreased (the dispersion is decreased or increased), a signal at or near the centre of the display becomes contracted or expanded width-wise but remains on-screen. This is a great convenience in use.

Operation is as follows. On negative excursions of the clock drive, Tr1 is off and Tr3 clamps the capacitor C1 and the NI input of A1 to the voltage at the output of A1, Vclamp: the output therefore sits at l/ciamp, the voltage at the wiper of R5. A1 forms a Howland current pump, so that when Tr1 is turned on, removing the clamp, a negative charging current Vcinw/R5 is applied to the capacitor. As A1 must act to maintain voltage equality between its inputs, a linear negative going ramp results. If C1 is selected correctly relative to the clock frequency, the voltage across it will just reach -1/ciamp during each positive excursion of the clock, Fig. 2b.

For convenience, the clock frequency is derived from the mains, giving a choice of sweep durations. The sweep amplitude can be set to any value from zero to maximum, the sweep remaining ground centred as illustrated in Fig. 2c, where R2 was used to advance Vcinw steadily from ground to its maximum value, over a number of sweeps.

Fig. 3 shows the full circuit of the sweep circuitry which operates as follows. The 15V ac from the psu is sliced by Tr1 (Fig. 3a) and fed to a hex inverter to sharpen up the edges. R5 and R6 around the first two inverters provide some hysteresis—without this, noise on the mains waveform will simply be squared up and fed to the counters as glitches causing miscounting. The output of the inverters is a clean 50Hz squarewave and appears at position I of switch S1b. The half period is 10ms, this setting the shortest sweep duration. A string of four 74LS90 decade counters provide alternative sweep durations up to 100 seconds.

The selected squarewave from S1B is level shifted by Tr2 and Tr3 to give a control waveform swinging (potentially) over ±15V, although the positive excursion only reaches Vclamp. This waveform is routed to control the fet in the sweep circuit, line 1. A3 and A1 provide currents via R6 and R5 which are fed to a summing amplifier to provide the main and fine tuning controls, line 2. R4 is adjusted to make the full range of the centre frequency set control R3 just cover the required 30V varactor tuning range of the TV tuner.

Lines 1 and 2 are connected as shown in Fig. 3b, line 1 operating the clamp transistor Tr3. Being a jfet, the gate turns on at 0.6V above Vclamp, so line 1 never in fact reaches ±15V. The sweep generator operates as in Fig. 2a, with one or two additions. S1b selects a size of capacitor appropriate to the sweep duration, two of the capacitors being re-used by altering the charging current by a factor of 100 via S1c. (Note that for a linear sweep, it is sufficient to ensure that the ratio of R1 to R2 is the same as the ratio of the two resistors connected to the non-inverting input of A3, the actual values can be whatever is convenient.) R17 is adjusted so that the ramp output from A3 swings equally positive and negative about earth. S2 selects the span from full span for the selected band of operation of the TV tuner, via decade steps down to zero span, where the...
**Fig. 3a.** Sweep duration generator and centre frequency setting circuits.

**Fig. 3b.** Sweep generator, sweep/centre-frequency summer and sweep shaping circuits.
tuner operates unswept at the spot frequency selected with centre frequency controls $R_1$ and $R_{2}$; $R_{41}$ provides a continuously variable control between the settings given by $S_2$. $R_{41}$ enables the full span, with var at max, to be set just to swing over the 0 to 30V tuning range of the tuner when centre frequency $R_1$ is set appropriately. If centre frequency is set to minimum or maximum, only the upper or lower half of the span will be displayed, at the left or right side of the oscilloscope trace respectively.

Inverting amplifier $A_S$ sums the negative-going sweep waveform and the negative tuning input from $R_1$ and $R_{2}$, to provide a positive-going voltage between 0 and +30V. It also provides waveform shaping, the reason for which is discussed later. The shaped sweep output from $A_S$ is level shifted by $T_{tr}$ and $D_1$ before passing to the TV tuner varactor tuning input since it is important that the sweep should start right from zero volts if the bottom few MHz of Band I are to be covered.

All of the front panel controls shown in Fig. 3 (except the reset control, of which more later) were mounted on a sub-panel behind the main panel and connected to the sweep circuit board - mounted on the same sub-panel - via ribbon cable, making a self contained sub-unit.

**RF section**

Fig. 4 shows the RF/IF unit, which is powered via a ribbon cable from the sweep circuit board. The gain of the TV tuner $K_T$ can be varied by means of $R_{41}$, which thus substitutes for the input attenuator of a conventional spectrum analyser. Compared to the latter, this spectrum monitor has the advantage of a tuned front end, as against a wideband direct-to-mixer architecture.

The front end tuning helps to minimize spurious responses - always a problem with any receiver, including spectrum analysers. The IF output of the tuner, covering approximately 34 - 40MHz, is applied via a fet buffer to grounded base amplifier $T_{tr}$. This provides IF gain and some selectivity, its output being buffered by emitter follower $T_{tr}$ and applied to the main IF filter $F_1$, of which more will be said later. The output of the filter is applied to a true successive detection logarithmic IF amplifier.

The required well decoupled +5V supply is produced locally by $K_{u}$. The log amp output $V_{log}$ is applied to an output buffer op-amp $K_{c2}$ via a simple single-pole switchable video (post detection) filter, which is useful in reducing grass on the baseline when using a high dispersion channel and a suitably slow sweep speed.

Filter time-constants up to one second were fitted in the instrument illustrated, but such large values will only be useful with wide dispersions at the slowest sweep speeds. The buffered $V_{log}$ is applied to the Y input of the display used, typically an oscilloscope. $R_{52}$ permits the scaling of the output to be adjusted to give a 10dB/division display.

**Special considerations**

The frequency vs tuning voltage law of the TV tuner is not linear, being simply whatever the L.O. varactor characteristic produces. Just how non-linear is clearly shown in Fig. 5a which shows both the linear tuning ramp and the output $V_{log}$ from the IF strip, showing harmonics of a 10MHz pulse generator at 50, 60 through to 110MHz plus a 115MHz marker (span range switch $S_{24}$ being at full span and span variable control $R_{16}$ fully clockwise). Also visible are the responses to the signals during the retrace, these being telescoped and delayed.

The frequency coverage is squeezed up in the middle and unduly spread out towards the end with a yawning gap between 110 and 115MHz. The result of some simple linearisation is shown in Fig. 5b. As the ramp reaches about 10V, $T_{tr}$ turns on, adding a second feedback resistor $R_{53}$ in parallel with $R_{41}$, halving the gain of $A_S$ and slowing the ramp down so as decompress the frequency coverage in the region of 70 to 100MHz, maintaining a 10MHz/division display.

Just before 100MHz, $D_{1}$ turns on, shunting some of the feedback current via $R_{53}$ away from the input and thus speeding the ramp up again, whilst another more vicious breakpoint, due to $D_{1}$ at around 110MHz, speeds the ramp on its way to 30V, correctly locating the 115MHz marker just half a division away from the 110MHz harmonic.

The linearisation has been optimised for operation on Band A (bands I and II) and holds quite well on Band B (band III) with the particular tuner used. Ideally other shaping stages similar to $A_S$ would be employed for Band III and Band IV/V.

Note that whilst the linearisation shown in Figs 4 and 5 has produced an approximately constant 10MHz/division display on full span.

---

**Fig. 4. Circuit diagram of the RF/IF unit. This is built around a Toshiba EG522F TV tuner. Though almost any other model covering Bands I to V inclusive could be used.**
for reduced spans $S_1$ attenuates the sawtooth before it is conveyed to the shaping stage. Consequently, for reduced spans the actual span/div depends upon the setting of the centre frequency control, although the portion of the full band displayed will be approximately linear, except where it happens to lie across one of the break points.

The filter used in the spectrum monitor illustrated is a 35.4MHz 6-pole crystal unit designed for 20kHz channel spacing applications. This was used as it was to hand just waiting for a suitable application. However it is not ideal, having a basically square-passband shape approximating the proverbial brick wall filter.

This is not a great inconvenience in practice: it simply means that a slower sweep speed than would suffice with an optimum Gaussian filter must be used. Even with a Gaussian filter, the combination of large span and fast sweep speed used in Fig. 5a and 5b would have been quite excessive - it was used as the stretching of the responses makes the effect of linearising circuitry more easily visible.

Fig. 5c shows the same Band A (43 to 118MHz) display using the nominal 100ms sweep. FM stations in the range 88 to 104MHz are clearly visible, no longer being lost in the tails of other responses.

Although the particular crystal filter used is no longer available, a number of alternatives present themselves. A not too dissimilar filter with a centre frequency of 33.368MHz is available from Ref. 4. Its 20kHz 3dB bandwidth (compared with 9.5kHz for the filter used in the prototype) would permit faster sweep speeds or wider spans to be used but, being only a 4-pole type, its ultimate attenuation is rather less and the one-off price may make it unattractive.

A choice of no less than five crystal filters in the range 35.0 to 35.9MHz is available from Ref. 5. With bandwidths ranging from 8kHz at -6dB (type XF-354S02) to 125kHz at -3dB (type XF-355S02, a linear phase type). A simple alternative would be to use synchronously tuned LC filters though at least twice as many tuned stages should be employed in order to take advantage of the greatly increased on-screen dynamic range offered by the log-amp in the design featured here, compared to the linear scale used in Ref. 2.

The excellent dynamic range of the spectrum monitor is illustrated in the multiple exposure photo. Fig. 5d, which shows an 80MHz CW signal applied to the monitor via a 0 to 99dB step attenuator. The signal generator output frequency and level were left constant and a minimum of 20dB attenuation was employed, to buffer the monitor input from the signal generator output. The attenuation was increased by 60dB in 10dB steps and then by two further steps of 5dB, the display of the signal being offset to the right using the centre frequency controls at each step. Fig. 5d shows the excellent log-conformity of the display over a 65dB range, the error increasing to 3dB at -70dB relative to top-of-screen reference level. It also shows the inadequate 63dB ultimate attenuation of the crystal filter used, with the much wider LC stage taking over below that level.

An alternative to crystal or LC filters is to use saw filters, a suitable type being Murata SAF39.2M50P. This is a low impedance 39.2MHz type designed for TV/VCR sound IF, some additional gain being necessary to allow for its 17dB typical insertion loss. Two of these filters would provide an ultimate attenuation of around 80dB, enabling full use to be made of the subsequent log-amp’s dynamic range. The 60kHz 6dB bandwidth of each filter would limit the discrimination of fine detail, but allow full span operation at the fastest sweep speed. They could then be backed up by switching in a narrower band filter as and when necessary.

Further development

A number of refinements which will occur to the reader could be incorporated in this spectrum monitor, to increase its capabilities and usefulness. One simple measure concerns the method of display. As our oscilloscope has sweep speed ranges in 1 - 2 - 5 sequence plus a variable control, the output from $S_{rg}$ was simply used as a 'scope trigger. However, if $S_{trig}$ is set permanently at $L_{coup}$ and a further buffer op-amp added between $A_3$ and $A_4$ to implement the span/var function, the fixed amplitude output from $A_3$ (suitably scaled and buffered) can be fed out to the display oscilloscope, set to dc coupled external X input, providing a sweep speed automatically coupled to the sweep speed control $S_4$.

At the slower sweep speeds, eg 1 or 10 seconds per sweep, a long persistence 'scope provides better viewing, whilst for the 100s sweep a digital storage 'scope or a simple storage adapter is very useful. However the slower sweep speeds are only necessary when using a narrow filter with a wide span, if one of the slowest sweep speeds is in use, it can be very frustrating to realise just after the signal of interest appears on the screen, that one needed a different setting of this or that control, since there will be a long wait while the scan completes and then restarts. Pressing the reset button $S_5$ will reset the tuner sweep voltage to $L_{coup}$ to give another chance to see the signal, but without resetting either the sweep period selected by $S_3$ or the oscilloscope trace.

If one of the sections of the 3069 IC is
Using the instrument

This spectrum monitor is rather like the least-facile spectrum analysers, i.e. it is entirely up to the user to ensure that an appropriate IF bandwidth, video filter setting and sweep speed are used, suitable for the selected span. Failure to do so means that as the spectrum analyser sweeps past a signal the latter will not remain within the filter bandwidth long enough for its full amplitude to be registered. This is important in a full-blown analyser, where the reference level (usually top of screen) is calibrated in absolute terms, e.g. OX1Bm.

Fig. 6a. Oscilloscope display of the 100MHz output at maximum level from an inexpensive signal generator, with the fixed level internal 1kHz AM applied. Oscilloscope set to 100mV/div, vertical, 500ns/div, horizontal.

Fig. 6b. Display using the spectrum monitor of the same output but using 50kHz external modulation, set for the same modulation depth. SPAN 100kHz/div, vertical, 100ms/div, horizontal.

Fig. 6c. As 6b, but external modulation input reduced by 30dB, displayed 100ms SWEEP.

Fig. 6d. SWEEP speed.

Fig. 6e. As bb, but external modulation Input absolute terms, e.g. OX1Bm.

Fig. 6f. As 6c, but external modulation Input.

Fig. 6g. As bb, but external modulation Input.

Fig. 6h. As 6f, but external modulation Input.

Fig. 6i. As bb, but external modulation Input.

Fig. 6j. As 6g, but external modulation Input.

Fig. 6k. As bb, but external modulation Input.

Fig. 6l. As 6h, but external modulation Input.

Fig. 6m. As bb, but external modulation Input.

Fig. 6n. As 6i, but external modulation Input.

Fig. 6o. As bb, but external modulation Input.

Fig. 6p. As 6j, but external modulation Input.

Fig. 6q. As bb, but external modulation Input.

Fig. 6r. As 6k, but external modulation Input.

Fig. 6s. As bb, but external modulation Input.

Fig. 6t. As 6l, but external modulation Input.

Fig. 6u. As bb, but external modulation Input.

Fig. 6v. As 6m, but external modulation Input.

Fig. 6w. As bb, but external modulation Input.

Fig. 6x. As 6n, but external modulation Input.

Fig. 6y. As bb, but external modulation Input.

Fig. 6z. As 6o, but external modulation Input.

Fig. 6aa. As bb, but external modulation Input.

Fig. 6ab. As 6x, but external modulation Input.

Fig. 6ac. As bb, but external modulation Input.

Fig. 6ad. As 6y, but external modulation Input.

Fig. 6ae. As bb, but external modulation Input.

Fig. 6af. As 6z, but external modulation Input.

Fig. 6ag. As bb, but external modulation Input.

Fig. 6ah. As 6aa, but external modulation Input.

Fig. 6ai. As bb, but external modulation Input.

Fig. 6aj. As 6ad, but external modulation Input.

Fig. 6ak. As bb, but external modulation Input.

Fig. 6al. As 6af, but external modulation Input.

Fig. 6am. As bb, but external modulation Input.

Fig. 6an. As 6ai, but external modulation Input.

Fig. 6ao. As bb, but external modulation Input.

Fig. 6ap. As 6aj, but external modulation Input.

Fig. 6aq. As bb, but external modulation Input.

Fig. 6ar. As 6ak, but external modulation Input.

Fig. 6as. As bb, but external modulation Input.

Fig. 6at. As 6al, but external modulation Input.

Fig. 6au. As bb, but external modulation Input.

Fig. 6av. As 6am, but external modulation Input.

Fig. 6aw. As bb, but external modulation Input.

Fig. 6ax. As 6ao, but external modulation Input.

Fig. 6ay. As bb, but external modulation Input.

Fig. 6az. As 6ap, but external modulation Input.

Fig. 6ba. As bb, but external modulation Input.

Fig. 6bb. As 6av, but external modulation Input.

Fig. 6bc. As bb, but external modulation Input.

Fig. 6bd. As 6aw, but external modulation Input.

Fig. 6be. As bb, but external modulation Input.

Fig. 6bf. As 6az, but external modulation Input.

Fig. 6bg. As bb, but external modulation Input.

Fig. 6bh. As 6ba, but external modulation Input.

Fig. 6bi. As bb, but external modulation Input.

Fig. 6bj. As 6bd, but external modulation Input.

Fig. 6bk. As bb, but external modulation Input.

Fig. 6bl. As 6be, but external modulation Input.

Fig. 6bm. As bb, but external modulation Input.

Fig. 6bn. As 6bh, but external modulation Input.

Fig. 6bo. As bb, but external modulation Input.

Fig. 6bp. As 6bi, but external modulation Input.

Fig. 6bq. As bb, but external modulation Input.

Fig. 6br. As 6bj, but external modulation Input.

Fig. 6bs. As bb, but external modulation Input.

Fig. 6bt. As 6bo, but external modulation Input.

Fig. 6bu. As bb, but external modulation Input.

Fig. 6bv. As 6bp, but external modulation Input.

Fig. 6bw. As bb, but external modulation Input.

Fig. 6bx. As 6bq, but external modulation Input.

Fig. 6by. As bb, but external modulation Input.

Fig. 6bz. As 6br, but external modulation Input.

Fig. 7a. A band IV TV signal, showing (left to right) the vision carrier, colour sub-carrier, sound subcarrier and Nicam digital stereo signal.

Fig. 7b. 4.8kb/s data FSK modulated onto a VHF carrier; 10dB/div vertical, 40kHz/div, horizontal.

Fig. 7c. High modulation index FM produced by a triangular modulating waveform has a near rectangular envelope with a flat top and steep sides. Individual spectral lines are not visible in this 20s exposure as there was no relation between the modulating frequency and the sweep repetition period. The wavy lines are due to ringing on the tails of the filtered response.
DESIGN

To provide different signal paths for the different bandwidths rather than select the bandwidth by switching in one or other of several filters all operating at the same IF frequency.

Working with a single IF bandwidth has its drawbacks. Switching filters is a messy business - assuming the display 'scope is in the non working mode for the first IF permitting full span on each band to be examined without resort to very slow sweep speeds. A second conversion to 4.5MHz enables stock 5kHz filters to be used as an intermediate bandwidth, while a third conversion to 455kHz provides a choice of filters with bandwidths of 5kHz or less.

As Fig. 8 indicates, no filter switching is involved: the desired output is simply selected and fed to the log IF strip, which can operate quite happily at each of these frequencies. The net gain of the second and third IFs is fixed at unity, so that switching bandwidths does not alter the height of the displayed response - provided of course that the span and sweep speed are not excessive. Another improvement would be better linearisation of the frequency axis avoiding sharp breakpoints, with the provision of shaping appropriate to each band. The easiest way to achieve this is probably to store \( n \) values in prom, \( n \) being a power of two, and read these out successively to DAC. The \( n \) values would correspond to equal increments along the frequency axis, each value being what was required to provide the appropriate tuning voltage from the DAC. The use of multiplying DACs will provide linear interpolation between points, giving in effect a shaped varactor drive voltage waveform with \( n \) breakpoints per scan. With many breakpoints available, the change of slope at each will be very small, avoiding the harsh breaks visible in Fig. 5b. The two msbs of the prom could be used as select lines to call up a different law for each of the three bands.

Frequency readout

A true digital readout can be provided by counting the frequency of the LO output from the TV tuner, prescaled by a divide-by-100 circuit to a more convenient frequency. Using the positive half cycle of the 5.0MHz squarewave at pin 12 of IC2 provides a 100ms gate time which, in conjunction with the divide-by-100 prescaler, gives a 1kHz resolution. The positive-going edge can be used to jam a count equal to the IF frequency into a string of reversible counters, set to count down, the appearance of the borrow output switching a flip-flop to set the counters to UP count for the rest of the gate period.

The negative-going edge can reset the flip-flop and latch the count: for economy the negative half period could simply enable a seven segment decoder/display driven direct from the counters if you don't mind a flashing display.

If span is set to zero, the tuned frequency is indicated exactly. If span is set to one thousandth or even one hundredth of full span, the frequency will correspond to the centre of the average frequency over the duration of the scan. In principle, the same applies up to full span, if the linearisation is good.

A simpler scheme for frequency readout uses a digital voltmeter. The output of \( A_2 \), besides feeding \( A_3 \), is also fed to a summing amplifier with pre-settable gain which combines it with a pre-settable offset. This is arranged (for example, on band A) so that with \( R_1 \) at zero, its output is 530mV and with

redeployed to a position between \( S_{1B} \) and \( R_{1B} \), the sweep will occur during the negative half of the squarewave selected by \( S_{1B} \) (see Fig. 2b). A second pole of \( S_4 \) can then be used to reset \( IC_{8 - 1} \) to all logic zeros, avoiding a long wait during the unused 50% of the selected squarewave output from \( S_{1B} \) before the trace restarts - assuming the display 'scope is in the external X input mode, rather than using triggered internal timebase.

Working with a single IF bandwidth has its drawbacks. Switching filters is a messy business however it is achieved. Fig. 8 shows an economical scheme using inexpensive stock filters.

Wide bandwidth LC or saw filters operating somewhere in the range 35 to 39MHz are used for the first IF permitting full span on each band to be examined without resort to very slow sweep speeds. A second conversion to 10.7MHz enables stock 50kHz filters to be

![Fig. 8. Block diagram showing modified architecture, giving a choice of IF bandwidths. It is simpler to provide different signal paths for the different bandwidths rather than select the bandwidth by switching in one or other of several filters all operating at the same IF frequency.](image)

![Fig. 9a. The LO. output of the EG522F tuner at 400MHz, showing also the 2nd and 3rd harmonics. Span 100MHz/div, vertical 10dB/div, ref. level (top of screen) 0dBm.](image)

![Fig. 9b. Block diagram of a spectrum monitor based on TV tuners, providing continuous coverage from below 1MHz up to approx. 400MHz.](image)
R1 at maximum its output is 0.18V. This is fed to the DVM on the 2.000V range, providing a readout of 100kHz/2nV. Similar scaling arrangements can be employed for the other bands, the accuracy of the resulting readout depending upon the accuracy of the linearisation employed.

This arrangement ignores the effect of centre frequency fine control R2 which can, if desired, be taken into account as follows. The outputs of A1 and A2 are combined in a unity gain non-inverting summing amplifier, the output of which is fed via a 47K resistor to A3 as now, and also to the scaling-sum-offset amplifier.

However, the simplest frequency calibration scheme of all, unlike the counters and displays, requires no additional kit whatever and unlike the DVM scheme, is totally independent of the exactness of linearisation. It is simply to calibrate, for each of the three bands, the centre screen frequency against the reading of the digital dial of the ten turn pot R. Calibration charts are as effective as they are cheap, and in the present application they can also be very accurate, since all of the instrument’s supplies are stabilised.

Continuous coverage

My final word concerns the missing coverage between the top of band III and the bottom of band IV, whilst also adding coverage from zero Hz up to the bottom of band 1.

Many tuners now available will probably, like the Toshiba EG522F, have an LO output available from the tuner when tuned near the bottom of Band IV. The level of the 490MHz fundamental is -18dBm and the second and third harmonics are both well over 25dB down. The output over the rest of the band is well in excess of -14dBm. Using broadband amplifiers to boost the tuner’s LO output to say +7dBm, it can then be applied as the mixer drive to a commercial double-balanced mixer, the signal input being applied to the mixer’s signal port via a 400kHz low pass filter.

This tuner is used purely as a local oscillator, with the mixer’s output being applied to the signal input of a second IF-tuner fixed tuned to 870MHz. Fig. 9b. The second tuner thus becomes the first IF of an up-converting 0.4MHz spectrum analyser; its output being fed to a 35MHz second IF strip as in Fig. 4. This arrangement provides continuous coverage from 0Hz almost up to the top end of the 225 - 400MHz aviation band in one sweep, so only one set of sweep linearisation is necessary.

A most useful feature in a spectrum analyser, not always found even in professional models, is a tracking generator. This provides a constant amplitude CW test signal to which the analyser is always on tune. Fig. 9b also shows how for the patently cost of yet another tuner and mixer, such a facility can be engineered. Used in conjunction with a reflection coefficient bridge, it turns a spectrum analyser into a rudimentary scalar network analyser.

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"Smart power" is generally taken to mean the inclusion of control and protection facilities into a discrete power transistor package. Most devices with this tag offer only limited protection through their integral thermal and overvoltage protection circuitry. International Rectifier has produced a mosfet which is so smart as to be virtually unburstable, yet cheap enough to replace standard mosfets in most applications. By Frank Ogden.

Smart enough to avoid destruction?

The ideal power mosfet would include decisive thermal shutdown with excess junction temperature, an overcurrent sensing mechanism which doesn’t adversely affect on-resistance and a fast overvoltage clamp which dissipates spike energy in the main transistor channel. If device protection can be provided in a standard three-terminal package, so much the better. There are transistors on the market which have some these characteristics. The IRSF3010 has all of them – plus full ESD protection.

The device behaves like the n-channel 11A, 50V power mosfet which it is until a critical parameter is exceeded. From then on, internal protection circuitry takes over.

Referring to the functional diagram, the zener diode between the input and source provides ESD protection for the input and also limits the applicable voltage at the input to 10V. This mechanism will withstand the full 4000V body model discharge through the input pin of the device removing the need for any special handling precautions.

The internal RS bistable memorises the occurrence of an error condition and controls the state of the output transistor through Q2 and Q3. The flip-flop may be cleared by holding the input to the device low for a specified minimum period, typically around 7μs.

The comparator pair senses overcurrent and over-temperature signals against an internally generated reference. Either comparator can reset the fault flip-flop and turn the power transistor off. During fault condition, Q2 disconnects the gate of Q1 from the input while Q3 shorts this to ground ensuring rapid power device turnoff.

The zener diode between the gate and
drain of the main power transistor causes channel conduction when the drain-source voltage of the device exceeds a predefined limit.

**Device operation**

The control logic and protection circuits are powered from the signal on the input pin of the IRSF3010. When positive voltage appears at the input to the device, the flip-flop turns Q2 on and connects the gate of the main device to the input. The turn-on speed is limited by the channel resistance of Q2 and the gate charge requirements of Q1. Using a higher input voltage will improve the turn-on time but it does not affect the turn-off switching speed. The control circuitry draws around 300µA from the device input terminal enabling compatibility with most drive circuitry.

When the drain current exceeds the preset limit, the protection circuit resets the internal flip-flop and turns Q1 off. Holding the device input below 1.3V for a minimum of 10µs will restore normal operation. Unlike schemes which monitor the total current through the power transistor channel, current measurement in the IR device is made by examining the current flowing in just a few cells out of the several hundred thousand which make up the power transistor. This avoids an increase in device saturation voltage to accommodate the sensing circuitry.

The device overvoltage circuitry also differs from the conventional. When the drain to source voltage exceeds 55V, the zener diode between gate and drain turns the device on before the breakdown voltage of the drain-source diode is reached. This greatly enhances the energy the device can dissipate during turn-off of inductive loads compared to the avalanche breakdown mode. Thus the transistor can be used for fast de-energisation of inductive loads. The absorbed energy is limited only by the maximum junction temperature.

**Typical waveforms at overcurrent shutdown.** After turn-on, the current in the inductor at the drain starts ramping up. At about 15A, the overcurrent protection shuts down the device.

**Switching waveforms from clamped inductive load using 5V input voltage.** In typical switching applications below 40kHz, the difference in switching losses between the IRSF3010 and a similar current rated standard mosfet is negligible.

**Over-temperature protection.** The graphs show an IRSF3010 switching a 1Ω resistive load connected to a 12V power supply. When thermal balance is established, the junction temperature is limited on a pulse by pulse basis.

**Reader Services Offer**

To obtain your free sample of the International Rectifier IRSF3010 protected power transistor, fill in and send off the special reply card located between pages 1024 and 1025 of this issue. This reader services offer is being handled directly by International Rectifier. Our editorial office is unable to assist in any queries relating to it. This offer is restricted to the first 500 replies.
This Hewlett-Packard oscilloscope combines the feel and display of a top line analogue instrument with the precision and programmability of digital electronics. This DSO is easy to use because it was designed by electronics engineers for electronics engineers.

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Variable-inductance, low-frequency VCO

Variable-frequency oscillators using the then principle of varying inductance of a coil by varying mutual inductance in a transformer were first described by K C Johnson in WW April and May 1949. My adaptation is shown in the diagram.

If L is the inductance of a coil through which flows an alternating current and some part of the same current flows in a mutually coupled coil, the effective inductance of the first coil Lı is L₂ = M, since the second coil may or may not be wound in the same sense. M is the mutual inductance.

A differential voltage-controlled amplifier can be used to vary the proportion of the oscillatory current flowing through the second coil, the total oscillatory emitter current being shared in a varying proportion between the two halves of the amplifier.

Transistor Tr3 is an emitter follower feeding the common-base amplifier made up of Tr1 and Tr2, the differential pair, whose output goes to Tr3 and completes the loop. Loop gain is set by R662.

Voltage control varies series inductance and therefore frequency in this LF oscillator.

DS1233 replaces monostable

Dallas's DS1233 EconoReset, described in the March 1992 issue (p910) normally resets a microprocessor after detecting upsets on its supply, but has other possibilities, being effectively a monostable in a TO-92 package which maintains a low on the output for 350ms after power is applied. Here, it delays and produces an inverted pulse with a fixed width. Its frugal power needs can be supplied by a cmos gate.

Figure 1 shows the former, in which it delays a rising edge by 350ms, replacing a monostable and an and-gate. When the cmos gate output rises, the DS1233 output remains low for 350ms, going high after that period and returning low when power is removed.

In Fig. 2, a negative-going pulse wider than 350ms at the gate output produces a 350ms pulse from the DS1233. When the gate output goes low it applies power to the DS1233, the output going low for the time-out period and then returning high, unless the gate output is shorter than 350ms, in which case the output will correspond to the input.

Squegging at 600kHz occurred at zero crossing points, which was eliminated by the addition of C2; a more suitable transformer may be designed to avoid the problem.

Mike Button
TDR Ltd,
Malmesbury
Wiltshire

Fig. 1. Dallas's Econoreset microprocessor reset device used to delay a pulse rising edge by a fixed 350ms. Used in such a way, the DS1233 replaces a monostable and an And gate is contained in a small package. Power comes from the cmos gate.

Fig. 2. The DS1233 produces a fixed 350ms negative-going pulse.
PC counter uses parallel printer port

Needing to use a PC as a counter/timer without tying up the input/output bus, it seemed that the printer port would serve the purpose, but that the counter would need a separate power supply. In the event, this was unnecessary, since power at 8mA is derived from the serial port. The circuit allows measurement of frequency and period of a TTL input under software control from the PC.

Figure 1 shows clock signals coming from the 4060 32.768kHz crystal oscillator, which delivers the basic crystal frequency for period counting. In this mode, one cycle of input signal gates the clock to the counter. In frequency measurement the gate is open for 1s, during which the input goes to the counter. Four quad tri-state switches pass the counter output, a nibble at a time, to the status port.

Operating procedure is first to select the frequency or period mode; to reset flip-flop 1 and the counter, FF1 being set by the rising edge of the input or the 1Hz reference in period mode; counting begins and when FF1 output goes to 1, counting stops. The PC then reads the 16 bits, four bits at a time.

The 5-bit input status port reads the count and monitors measurement cycle status, the data port to enable tri-state switches and for mode selection and the control port to reset FF1, the address of the printer adaptor in use (LPT 1, 2 or 3) being found in the dos data area.

In period mode, the count must be multiplied by 1/32768 to obtain a sensible reading.

Dhananjay V Gadre
Inter-University Centre for Astronomy and Astrophysics
Pune India

Using a PC's printer adaptor, this circuit converts the computer into a frequency/period counter needing no other power supply than the serial port.
Under-frequency inverter protection

If a 50Hz inverter's output frequency falls below that required by the equipment it powers, this circuit disconnects the output. Input comes from the inverter's driver stage, any asymmetry being eliminated by the first D-type flip-flop. At each low-to-high transition of Q1, C1 discharges through the transistor Tr1 and begins to charge again through R2 and P1. As this voltage reaches the threshold voltage of Clock 2 input, the Q1 output latches into the second flip-flop. As shown in the timing diagram, the Q2 output, which drives the output transistor and therefore the relay, is either 0 or 1, depending on the input frequency. Resistor Rf inserts a little hysteresis to prevent relay chatter.

Adjust P1 to make TTH = Tu (=1/fc, the frequency at which the relay disconnects the load). This trip frequency can lie in the 48-62Hz range with the components shown.

M S Nagaraj
Isro Satellite Centre
Bangalore
India

Single-diode full-wave rectifier

This single-diode, single op-amp rectifier is used for LF rectification in an RTTY FSK demodulator. During a positive input half wave, D1 conducts and the circuit becomes a non-inverting amplifier, so that

\[ V_{out} = \frac{V_{in}}{R_1 + R_2} R_1 \]

for positive inputs. On negative half cycles, D1 is virtually an open circuit and on negative inputs.

\[ V_{out} = \frac{V_{in}}{R_1 + R_2} \left(1 - \frac{R_3}{R_1} \right) \]

Making R3 = R1 and R1 = 2R2 reduces this to

\[ V_{out} = \frac{-V_{in}}{R_1 + R_2} \]

which is the inverse of that for positive inputs and both half cycles are amplified. Diode imperfections can cause an imbalance between the halves; in such cases, increase R1 to 200-220kΩ.

Francois Guillet
France
Dirty Windows

What an interesting coincidence that Barry Fox's guest editorial (EW + WW, September) querying whether innovators and fancy features actually satisfy users needs, was in the same issue as some wag was telling us that Microsoft had spent the last ten years perfecting Windows (Update).

I was most interested to read Andy Wright's article on cold fusion (EW + WW, October). The emphasis is more on the radiation emitted and products formed, rather than on heat production. Even so, some important points were omitted, presumably for brevity. The original authors (Pons and Fleischmann) have withdrawn their claim for radiation emission and tritium formation. They concentrated on heat production. They generate enough heat to bring the electrolyte to the boil, but the heat is much more easily explained in straight chemical terms on the assumption that there is no cold fusion.

I have seen a video of the F & P equipment in action and was surprised to see that no effort had been made to keep oxygen away from the palladium. The fact that hydrogen saturated palladium gets hot in the presence of oxygen has been known for a very long time. Palladium acts as a catalyst in the conversion of hydrogen (or heavy hydrogen) and oxygen to form water and heat.

During normal running the palladium is surrounded by oxygen in solution in the electrolyte, by oxygen bubbles coming off the platinum anode, and by oxygen in the gas above the liquid. Heavy hydrogen bubbles coming off the palladium effectively purge the oxygen from solution in the immediate vicinity of the cathode. If this equilibrium is disturbed, so that some oxygen reaches the palladium, then a hot spot is created, this sets up a convection current, bringing more oxygen down from the anode round the bottom of the tube and up past the central palladium electrode, producing even more heat. In the video, the electrolyte came to the boil, allowing oxygen from the gas phase to reach the palladium.

The total heat generated in the experiments of F & P was always less than the electrical energy put into the system. The electrical energy input was applied over several days or weeks. During this time it was accumulating a store of chemical energy in the form of hydrogen in the palladium. If for any reason, oxygen reached the palladium then this accumulated energy was released in a few minutes.

If I am right then you would also expect an experiment using ordinary light water to generate heat. Well, according to Pons himself, "It does". See Nature Vol 338 page 691.

David Dewey
Hayes Ridge, Herts

Andy Wright's timely reminder (EW + WW, October) that there is life in cold fusion after the lynch mob has run amok is to do a simple thing like copy a file? Of course, all these things will be sorted out in Windows NT, won't they? Or did I hear there was something called Cairo beyond that?

A less charitable view is that for the past 12 years Microsoft's operating systems have been crippled by some very poor decisions made in the eagerness to rush out something for the IBM PC, and the various versions of Windows followed a similar pattern because of eagerness to compete with the MacOS gui.

Anyone who strays into their local school is likely to see quite young children opening windows, resizing them, launching applications by double clicking with a mouse, selecting files created by one application and dropping them into another. In other words using Acorn Rise Os they can do all the things a Windows user wants to do, and a good deal more easily.

Isn't it time that someone asked why it is that a small British company can produce a wimp based operating system which runs comfortably on a 1 Mbyte machine with a single floppy disk, while multi-million dollar Microsoft is still
promising to sort things out with Windows NT? The last thing I read about Windows NT said that it would expect to find 8Mbyte of ram, but really needed 12Mbyte!

Apparently not! Month after month the computer press is full of reviews with headlines like “Chile compiler shout out”, “468 wars” or “Word-processor head to head”. Magazines get fatter, worthwhile articles get fewer, but the advertising revenue rolls in.

Sadly I’m beginning to see the first signs of this trend in EW + WW. Almost every month there is an article described as “PCs Engineering.” It isn’t, it’s just a program review by a fancy name. I cannot remember when I last saw an article that mentioned any other computer than an IBM.

The assumption seems to be that the PC is the industry standard and that any other computer must be a toy. Unfortunately joining two or three pieces of standard and supposedly compatible equipment, then persuading them to talk to each other, can still take a very long time.

I find it very hard to believe that people are not finding worthwhile and commercially viable uses for computers like the Amiga, Atari or the various Acorn Risc machines, which could find a mention in your pages. Looking back over 20 odd years of your magazine in its various guises, one thing that stands out is the number of oddballs finding a voice in your pages. So why the present obsession with helping Bill Gates’ bid for world domination?

Les May

Rochdale

I agree with every word the correspondent says. Intel architecture is slow and stunted while Microsoft operating systems have always been cumbersome and inefficient. How IBM ever allowed Bill Gates to become the world’s highest paid executive, and Intel the world’s most profitable semiconductor is beyond me.

The truth is that the two companies have more of their products in use than all their competitors combined — by a factor of several times. To ignore this in our reviews would be to do a disservice to our readers.

Personally I use a Macintosh.

Editor

Kids playing with Windows

John Carrey raises some very valid points about the dreadful Windows (EW + WW, October). To my understanding Windows was conceived as an aid for children to use PCs without the need to comprehend DOS. That the adult world embraced the product is hardly in accordance with the original quotation: “When I became a man I put away childish things”. Apart from this large useless package taking up a useful chunk of my hard disk, I can do anything quicker under dos.

I resent the loss of some 9Mbyte of disk space for a program that I am forced to use to run software because there is no dos alternative. But how much worse it is for schools with their low budgets and old machines, where a 40Mbyte hard disk is a luxury; more than 25% of disk space taken up with operating systems!

Professionally, I am involved in satellite remote sensing analysis, where the operational software is dos based. I am happy to report that I don’t know of any Windows products in this field.

Recently I completed a low cost satellite image analysis package for schools, which includes 20Mbyte of high resolution satellite images, which for low capacity hard disk users can be loaded individually (250Kbyte each) from floppy. The analysis software requires 1Mbyte and no it does not run under Windows nor ever will!

DJ Standen

Slower using Windows

John Carrey’s letter (EW + WW, October) criticises several aspects of Windows. The writer, as do other Windows critics, overlooks a basic fault inherent in Windows software.

Much commercial use of Windows type software involves continuous interaction with the keyboard user. The typical slow reaction time of the user partly conceals the extreme slowness of Windows basic execution.

Our work uses PC programs that need minimal user interaction and emphasise any slowness in execution. Two pairs of sample runs — each using identical input data and a 66MHz 486 system — demonstrate the inefficiency of graphics based text screens. These programs allow a run-time choice between text only and EGA graphics based screens.

For data requiring limited calculation the text only screen took 3s. An identical calculation using the EGA alternative took 283s — more than 30 times as long.

With data needing extended calculation the graphics screen had less effect but still took twice as long — 5 and 10 hours.

These were short test calculations. Practical use implies single runs lasting from a few minutes up to several months continuous calculation — with pro rata time increases for EGA. Apologists for Windows state that faster processors will solve this kind of problem — forgetting that many basic calculations are still far too slow.

Windows NT appears to offer even worse possibilities. A recent review emphasised its need for the fastest processors — presumably not to improve the speed of basic calculation.

When will someone produce a 32bit operating system that combines all essential basic facilities with maximum processor utilisation and excludes complex gimmicks?

RG Silson

Tring, Herts

Relay breakdown

After reading A. Millar’s letter (Clunky versus Cost, EW + WW, October), I feel that several points raised in the letter are in need of clarification.

Mr Millar says that you cannot dismiss the mechanical switch or the relay too lightly. I wasn’t aware, from what was written, that I had.

The manuscript, as originally submitted, went into some depth about the pros and cons of said devices, but the editorial knife removed these references, probably because the article was primarily about solid state switching.

As far as lab tests on a new board are concerned, I too, wholeheartedly concur that a quality relay does present itself as a perfect switch — no semiconductors to distort the signal or cause noise when new. However, Mr Millar seems to have missed the fact that all relays do age, the cheaper types faster than others. Once contacts become oxidised, the resultant high resistance, if not corrected by modulated by signal level, will cause all manner of intermittency, noise and distortion problems.

Cost was mentioned briefly by Mr Millar but not properly pursued. Yes, the Focusrise console dispenses unilaterally with any solid state switching, and its sonic performance, in all respects, is widely acclaimed by the pro-audio industry, and rightly so. However, it does cost hundreds of thousands of pounds; transparent audio performance is not achieved without some considerable cost. The real challenge is to engineer an audio switch which is fairly transparent and is economic enough to be fitted hundreds of times over in a budget/mid-priced console.

Furthermore, the cost of relay switching isn’t related purely to the cost of the devices used, but more to the careful design of the environment surrounding the component. The inductive nature of the relay means that audio and switching ground return paths have to be isolated if spurs are to be avoided. This philosophy can be extended as far as providing completely separate switching and audio supply rails, mechanical isolation of the relays (separate PCB’s) and hefty

Spectrum space

The article “FM stations may close in spectrum shake-up” (EW + WW, September) about finding room in the spectrum for T-DAB makes me wonder whatever happened to bands 1 and 11P? These useful frequencies, once the home of 405-line tv in the UK, are still used for tv in the rest of the world.

I well remember the introduction of 625-line tv on uhf. We were told that, in about 20 years time, the vhf bands would carry two 625-line networks, in addition to the four planned on uhf.

Joseph B Fox

Redhill, Surrey

December 1993 ELECTRONICS WORLD + WIRELESS WORLD
trackwork/extendive ground planes. Furthermore, mutual-inductance coupling, poor regulation of supply rails, even microphonic pickups, all have to be considered if a design is to be a success. The extra time this requires at the design stage, the cost of larger or separate PCBs, drive and protection circuitry, isolation using opto-isolators etc. all add insidiously to the overall cost.

As far as the SSM2142 solid state switch package is concerned it is somewhat attractive but costly around £8 per IC, with the switching function made “split-free” using internal complementary ramp generators and comparators. Again, performance is achieved with cost.

Where commercial mixer switch designs are concerned, manufacturers are understandably reticent to publish circuit diagrams, so comparison with those shown in the article is somewhat difficult. What I had intended from the paper was an appraisal of the basic techniques employed in audio switching, rather than to provide the last word on commercial, cost-no-object, topologies which have little relevance to most budget or mid-priced applications.

Mike Meechan
Reading
Berks

Absolute test not needed

I refer to the letter from Greg M Ball (EW + WW, August) about my articles a year earlier (EW + WW, July 1992). He notes that the simple THD test circuit (my Fig. 1a reproduced from the Burr Brown data sheet) results in a common mode input to the op amp as large as the signal output, which I did not specifically point out as it will have been appreciated by most readers.

Additional distortion in the non-inverting connection compared with the inverting circuit (often described as being due to common-mode failure) is a well known phenomenon and is the reason the inverting connection is usually preferred where lowest possible distortion is the design criterion. Equally the non-inverting circuit is usually preferred where lowest possible noise is the design criterion. Even so, there is no reason why an op amp should not be designed adequately to have common-mode rejection and to provide a sufficient output signal.

Additional distortion in the NI connection due to common-mode failure is, as Ball notes, often even the largest possible dynamic range is leaving one with a problem where possible noise is the design criterion, whereas distortion is the design criterion. In the inverting connection compared with the non-inverting connection (my Fig. 1a) one can use a technique similar to one often used in evaluating an op amp’s settling time. A side chain consisting of an input and a feedback resistor equal in value to those defining the op amp’s gain is used, the voltage at their junction then being measured at the op amp’s inverting input, of that the drive signal is largely cancelled out at this point.

Slight adjustment of one of the sidechain resistors, plus maybe a whisper of quadrature trim, let the input signal be entirely outphased at this point. It can then be connected to the virtual earth of another op amp, which will provide an amplified version of any signal at the output of the DUT for which there is no common mode input signal, viz the DUT’s distortion.

While cancellation of the input signal can never in practice be absolutely complete, up to 60dB of input signal rejection is certainly feasible, permitting the use of a modest THD meter to complete the measurement.

Ian Hickman
Waterlooville, Hampshire

Neural omissions

With reference to my article “Neural networks hit the jackpot!” (EW + WW, August), an important part of the original article appears to be missing.

The missing section should be added at the end of the box “Back propagation algorithm”, where it states: “Contribution to the network error of the weights located between the input and hidden nodes can be found from calculating the derivative as follows.”

Unfortunately the calculations are not shown. Here is the missing part:

$$\delta_k = \sum_i \delta_i y_i (1 - y_i) \beta_k$$

where $\beta_k$ is the error at the output of a hidden node, and is defined as:

$$\beta_k = \sum_j e_j y_j (1 - y_j) \beta_k$$

We have derived it for each layer of the network, all that remains is to adjust the weights in the network to reduce the error. The change required in value for a weight between the input and hidden nodes is given by:

$$\Delta w_{x_i y_j} = -\delta_i y_j (1 - y_j) \beta_k$$

and likewise for a weight between the hidden and output nodes:

$$\Delta w_{y_i z_k} = -\delta_k y_k (1 - y_k) \beta_i$$

where $\delta$ represents the step size used in weight adjustment.

A typical value for $\delta$ used in other optimisation methods is 0.5. This is confirmed by Drew van Camp (a computer programmer and researcher at the University of Toronto). Also, there is a small but important printing error on page 652 in the text below the first equation: $e_i$ is not squared as stated. The second equation is correct since this involves taking the sum of the square of the errors.

George Overton
Kelmscott, Leicestershire

Give Workbench a chance

It is to be regretted that your reviewer of Electronic Workbench Pro (EW + WW, September) gave it a somewhat cool reception. It is obvious to me that insufficient time was spent with what is after all a unique example of CAD software. And it is unfortunate that the simple circuits that come with the software were the only ones that were tried.

The generally negative tenor of the review might well deter younger computer users and educational establishments from investigating it: where else can you find a program that has all the features it offers and at the price?

Sure enough, having used it for a number of months, it has idiosyncrasies and the odd bug or two (which were clearly not discovered, either). But then, what CAD software hasn’t? If I wanted more accurate quantitative measurements, I would go for Spice or Analyser III.

But for a designer, the sheer pleasure of knocking together a sample circuit in a few minutes and seeing how it behaves is extraordinarily valuable and time saving. Yes, it is memory greedy and not a little tardy, but with greater familiarity, ways round all these become apparent.

Also, version 3.0 is due any time and will address all the criticisms I have of it. But has your reviewer ever waited for a student to construct and then fathom out the workings of a simple circuit on a laboratory bench? This takes 2min 25s using a 386 plus coprocessor for handy, which was the longest simulation I have recorded — about the same time for the soldering iron to heat.

Reg Williamson
Kidsgrove, Staffs

CFA: the last word?

FM Kabbary’s letter (EW + WW, September) seeks to continue the debate on the crossed-field amplifier but maybe it is time this dead horse was spared further flogging. The claim to have found corrections to Maxwell’s equations quoted by Martin Spencer (EW + WW, May) cannot be confirmed by Drew van Camp (a computer programmer and researcher at the University of Toronto). Also, there is a small but important printing error on page 652 in the text below the first equation: $e_i$ is not squared as stated. The second equation is correct since this involves taking the sum of the square of the errors.

George Overton
Kelmscott, Leicestershire

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The generally negative tenor of the review might well deter younger computer users and educational establishments from investigating it: where else can you find a program that has all the features it offers and at the price?

Sure enough, having used it for a number of months, it has idiosyncrasies and the odd bug or two (which were clearly not discovered, either). But then, what CAD software hasn’t? If I wanted more accurate quantitative measurements, I would go for Spice or Analyser III.

But for a designer, the sheer pleasure of knocking together a sample circuit in a few minutes and seeing how it behaves is extraordinarily valuable and time saving. Yes, it is memory greedy and not a little tardy, but with greater familiarity, ways round all these become apparent.

Also, version 3.0 is due any time and will address all the criticisms I have of it. But has your reviewer ever waited for a student to construct and then fathom out the workings of a simple circuit on a laboratory bench? This takes 2min 25s using a 386 plus coprocessor for handy, which was the longest simulation I have recorded — about the same time for the soldering iron to heat.

Reg Williamson
Kidsgrove, Staffs

Respect the giants

For many years space has been found in EW + WW for entertaining controversy about the validity of experiments on the effect of movement on the propagation of light. I want to suggest that it is unfair to readers without specialist knowledge of the issues to continue to imply that the observations are open to simple dispute. If you continue to publish letters perhaps they should come with some sort of health warning.

For those unfamiliar with the correspondence a brief explanation is appropriate. In the 19th century a number of experiments were carried out to discover the effects of moving the apparatus used to measure the speed of light. Those which Michelson and Morley performed in 1887 are the most famous.

It was strongly believed that light propagated at the speed of light in all inertial frames of reference. Michelson and Morley set out to test this hypothesis by performing experiments on the speed of light in different frames of reference. Their experiments involved setting up two identical op amps, with one on a plane rocking back and forth and the other at rest. The output of one op amp was connected to the input of the other, and a signal was transmitted back and forth between the two op amps. If the speed of light were the same in all frames of reference, then the signal would travel at the same speed in both directions, and the output of the second op amp would be the same as the input to the first.

However, the results of the experiments showed that the speed of light was not the same in all frames of reference. This discovery led to the development of the theory of relativity, which suggested that the speed of light is the same in all inertial frames of reference, regardless of the motion of the observer.

This is known as the principle of relativity, and it is one of the fundamental principles of modern physics. It states that the laws of physics are the same for all observers, regardless of their relative motion. This principle has been confirmed by numerous experiments, and it is now considered to be one of the most important results of 20th century physics.
was a wave motion and it was
to expect that moving the
apparatus would alter the speed of the
light in the same way that wind
alters the measured speed of sound.
No effect at all could be discovered.
This was a surprise to the earlier
experimenters though it was
probably what Michelson and
Morley had come to expect.

However the source and receiver
are moved, the measured speed of
light in free space (commonly
written as $c$) is, to the limit of
experimental accuracy, that
predicated by Maxwell for
electromagnetic waves.

These experiments were difficult
because the speeds with which
natural effects move the apparatus
are quite small compared with $c$.
The speed of the earth in its orbit is
about 30km/s compared with $c$
at about 300,000km/s. To make the
situation worse the effects studied
depended on $(v/c)^2$.

Nevertheless, so long ago as 1892
Fitzgerald accepted the correctness
situation worse the effects studied
depended on $(v/c)^2$.

Later astronomical discoveries
revealed movements, including the
rotation of the galaxy, with speeds
about ten times as great as the
Earth's orbital motion. These factors
would also have to reduce the
apparatus to explain the

All attempts to detect these effects
of motion on the speed of light have
relied on comparing the speed in
two different directions. Until the
development of atomic clocks in the
last few decades indirect methods
had to be used and these led to the
(time that made the effects so small.

Nowadays it is possible to work in
the obvious way with one clock at
the source and another at the
receiver. The global positioning
system using artificial earth
satellites inverts the procedure,
assuming the speed of light to be
constant and deducing positions by
measuring the difference in arrival
times of radio signals from several
satellites. Any variation of the speed
of light along one path would
produce a proportional change in the
apparent length of that path, leading
to a corresponding error in position.
The accuracy of the system is
very few tens of metres, while the path
lengths are a few tens of
kilometres. Thus changes of the
speed of light of around one part in
a million would be noticed as
malfunctions of the system. I have
noted above that the Earth's orbital
motion has a speed one ten-
thousandth part of that of light,
much greater than this resolution.

As these satellites are in rapid
motion relative to the Earth the
suggestion that a stationary Earth is
an adequate explanation for the null
results of the 19th century
experiments is ruled out. There are
similar but more complex
experiments which show the limit to
be more than two orders of
magnitude smaller. These
measurements are so accurate that a
second is now defined to be the time
taken by 9,192,631,770 oscillations of
a resonance frequency of the
atom of cesium 133. The metre is
defined implicitly by specifying the
speed of light to be 299,792,458
metres per second.

It must be admitted that it is very
surprising but light waves do not
behave like sound waves or water
waves in this respect. Twentieth
century studies have shown that
there are rather few respects in
which they are similar but the others
don't seem to worry your
correspondents so much.

I have to say that most of the letter
writers reveal an unattractive
arrogance. Not only Einstein but
several others who have contributed
to the growth of modern physics are
among the greatest intellects the
world has known. How can anyone
believe that with a few minutes
casual thought (or rather lack of it)
they can discover these giants'
errors?

Michael Weatherill
File
Designing a good analogue filter can be tedious and time consuming. Filter Master Active for the PC makes design quick and easy but at a price – as John Anderson explains.

Filter Master Active is a dos based filter design and optimisation tool intended to help specifying, dimensioning and analysing analogue filters. The package is from Omicron, licensed by Intusoft of San Pedro, California. It handles a range of filter pass characteristics and allows selection of various approximations. There is also a choice of design options. I remember well the struggle of synthesizing analogue filters to solve specific problems. The task was always tedious and a tricky compromise in component selection. This product provides a good route through the problem and is fast, allowing plenty of iterations in a reasonable amount of time.

Package overview
Comprising just a slim 150 page slim paperback manual, a disc and a parallel port dongle, the package costs over £600. Its manual is professionally produced and supplemented by a number of screen examples. A dozen sheet 'application note' is supplied though in reality this is really an addendum to the manual.

Installation was simple and uneventful, taking about 1.2Mbyte of hard disc space. The files comprise a number of Borland Graphical Interface (BGI) types. These allow the software to work with a wide range of different screen formats from CGA to VGA. Automatic screen sensing can be manually overridden to force mono graphics for lap top operation for example.

Tutorial section
On starting the program you are presented with an opening menu. This is the root menu for a quite complex tree of menus used to set the options for the program, synthesize filters and output results.

The manual leads in with an excellent tutorial of the design of a tenth order Cauer filter which took longer to specify than to synthesize! In only a few minutes, the tutorial introduction took this first design from paper specification to final design. This shows the user interface to be if not pretty then at least intuitive.

These glowing comments must be balanced against a fairly crude menu tree compared with modern graphical user interfaces. This shows up again in several other aspects of the program performance. In the end however, it is functionality and productivity that matter.

Throughout the program – even in graphics mode – a context sensitive help facility is available. It is at best adequate and at worst just a short description of each command. The help contents is a list of descriptors, usually one word, presented in a rather untidy list at the top of the screen.

Filter realisation
Filter Master Active uses a cascading technique to implement the final filter design. The technique involves a decoupled modes approach where first and second order filter structures are compounded to produce the final transfer function. In practice, problems can occur with this approach if capacitive loading on the output of the op-amps is large. This leading introduces additional poles in

![Filter Type and Approximation](image-url)
the transfer function. In severe cases the current limit of
the op-amp could be exceeded and a non-linear slew rate
limit imposed. The filter synthesis technique is supposed
to ensure that capacitive loading is kept low.

During the set-up sequence there is an option to select
how the component values are to be realised. Options are
specifically based on normal component values, the exact
value or values based on series or parallel combinations of
values.

To aid inspection of the synthesized filter, it can be
'drawn' as a circuit diagram using text characters. This is
both crude and likely to cause confusion - if there was
ever a reason for using a GUI, this is it. A nice feature is
the ability to alter the individual component values. This
allows assessment of the effects of choosing more practical
component values. However this facility falls a long way
short of a Monte Carlo tolerancing facility needed to
determine the range of filter performances that might be
expected with real components.

It is important to remember that Filter Master Active is
limited to the design of active filters (those with
operational amplifiers) using only resistors and capacitors.

Producing graphs

There is a variety of frequency and time simulations that
can be run to assess the filter performance, ranging from
Bode plots to time domain response. All simulations can be run
to assess the filter performance, ranging from

A similar problem exists for the effect of op-amp
performance. Although the program allows specification of
the op-amp, this is merely appended to the Spice file.

No trimming of the filter components is provided to
compensate. An example of this is presented in the

Moving to a further aspect of the GUI, this is the
provision of aids to inspection of the synthesized
circuit. This is similar to the netlist listing in the menu.

For the example shown, the component values are
printed as they are entered, and a circuit diagram is
produced. This has a few shortcomings. For instance
the values of the components are printed in text form,

A netlist for the filter design in ascii Spice form can be
produced. This is intended to provide an overview of the
final circuit. Being based on text rather than
graphical symbols however, it can be confusing.

Once the analogue filter is designed, you can tweak it by altering the values of
individual components.

Graph display is usefully enhanced by the zoom function. With
the aid of a mouse, the section of the curve to be zoomed is
simply selected by pulling a rectangle around it.
Part of the package is a tutorial covering the design of a tenth-order Cauer filter which takes longer to specify than design.

applications sheet in the section dealing with interfacing with spice

Conclusions
This is a good product with good fundamental performance. The ability to synthesize and optimise filters quickly must improve productivity. If you need to design half a dozen non-canonic filters then the cost of the software will be easily repaid.

That said the whole program, although functional and robust, has a very crude feeling from the menu structure to the circuit drawing and printer support. Although the program does provide a spice interface, there is no netlist facility. This makes the transcription of the final design to schematic capture prone to error. But in the end these are user interface issues. In its encapsulation of filter design rules the program performs with distinction.

Further reading
The Active Filter Design Book by Moschytz and Horn, published by Wiley, provides a useful design guide for about £30.

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What The Press Said About RANGER1
For most small users, Seetrax Ranger1 provides a sophisticated system at an affordable price. It is better than EasyPC or Tsien’s Boardmaker since it provides a lot more automation and takes the design all the way from schematic to PCB - other packages separate designs for both, that is, no schematic capture. It is more expensive but the ability to draw in the circuit diagram and quickly turn it into a board design easily makes up for this.

Source JUNE 1991
Practical Electronics

Pay by Visa or Access
Integration has now reached a level where it is possible to build a computer capable of out-performing the original PC-XT on a board with a credit-card footprint, as David Guest explains.

The embedded PC is not a new idea. Historically, the PC-XT was followed by the release of the 80188/80186, which introduced the concept. Subsequently, NEC released the V40 with an additional serial port and enhanced instruction set.

Register bank swapping and interrupt-driven macro services were introduced into the next generation—the V25, making the devices much more useful in real-time systems. Finally, the later V55 family comprised two processors, the PI and SC aimed at printer/fax applications and local area network (LAN) markets, respectively.

Unlike the previously mentioned devices, the recently introduced PC-on-a-chip allows all the functions of a PC to be incorporated in embedded systems. This chip also takes advantage of PC user interfaces such as the keyboard and display, saving valuable development time.

Software tools for the embedded PC are inexpensive. Cross-compilers and emulators normally associated with micro-controller development are unnecessary. Software can easily be written easily on a high-level PC compiler.

The basic input/output system, or BIOS, has evolved with the PC. It has a well-documented interface that isolates the operating system from the differences in the hardware of the system. It provides a power-on-self-test (POST) initializing all of the peripherals in a well-defined sequence. First it configures the 8237 DMA and the 8253 timer chip to refresh DRAM. Then it initializes a data field at 400H to keep track of the hardware configuration. Next it sequences through the remaining peripherals.

Bios allows the dos operating system, and sometimes the compiler, to interface to the hardware via well-defined software interrupt calls. This is similar to the dos interface. Routines are called by the 8086 INT command with parameters being passed via the processor registers. For example, the following code would print the character “a” to the screen:

```
    mov AH,02
    mov DL, "a"
    int 21
```

The bios and dos calls are well documented in various textbooks.
Integrated PC-on-a-chip

The F8680 PC-Chip, Fig. 1, is equivalent to an XT while containing all the peripherals associated with an AT. It runs software eight times faster than the original XT. This is twice as fast as the original AT, or approximately the same speed of a low end 16 MHz 386SX with slow dram and no cache. With over one hundred configuration registers, the F8680 PC-chip provides more system features than a desktop PC. It is also optimised for use in battery powered systems.

Power management

By far the strongest selling point of the F8680 PC-Chip is its power: management facility. It places the device into a league of its own. Many of the chip’s features are convenient but not essential. The power management however encompasses the complete system usefully reducing memory and external peripheral currents wherever possible.

The F8680 PC-Chip is a static core device maintaining all its internal registers, even after stopping the processor clock. This allows it to operate from only 15µA, while still maintaining the real-time clock.

At pre-defined intervals the chip can be restored to full operation under control of the RTC or an external signal on the PWRT pin. Operating the device at 3.3V reduces the current down even further to 5µA. Even when fully operational, the device only consumes around 40mA for an 8/16 bit dram-based system to 75mA for one with dram.

When the system is active there is a fine-control feature adding up to 127 cycles to the execution time of each instruction. This reduces the frequency of memory accesses and, consequently, current consumption.

Additionally, the chip itself uses less current, but the reduction is less significant, Table 1.

Access to power management is through a BIOS call (1fH), making an easy-to-use software interface. Within the BIOS is a utility which assesses system activity and automatically controls the power management features to reduce the operating current of the system.

Memory management

On board, the PC-Chip has all the control and interface hardware for three banks of memory and system ram. It can drive dram memory directly, supplying both the multiplexed address lines and refresh cycle.

Each bank has an associated bank select register, Bank select registers, Fig. 2, define the memory cycle type, i.e. XT bus cycle, dram, sram or PCMCIA. They also define the memory size and its width, of either 8/16 bit. For CPU word transfers, the memory controller performs two accesses to byte wide memory.

There are two distinct mechanisms for controlling memory. Firstly, memory mapping maps the 16Mbyte of processor address space into physical memory, segmentable down to 32Kbyte. There can be 32 by 32Kbyte or 32 by 64Kbyte sections for the low end of memory with an additional two 512K or 1Mbyte sections for high end memory respectively.

Each of the 34 mapping registers contains two bits memory and I/O modules with a range of peripherals like modems, Ethernet, and hard disk drives. Additionally, the Vadem has a built-in scanned keypad interface and a Centronics parallel port.

This article concentrates on the F8680 PC-Chip for two reasons. Firstly it is readily available in small quantities without significant up-front costs. Secondly it is about half the price of its counterparts, at around £35 for small quantities.

Table 1. By far the strongest selling point of the F8680 PC-Chip on a chip is its power management. In active mode a feature adding up to 127 cycles to the execution time of each instruction reduces memory accesses frequency and consequently current consumption.

<table>
<thead>
<tr>
<th>Extra cycles</th>
<th>SRAM</th>
<th>DRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CHIP</td>
<td>RAM</td>
</tr>
<tr>
<td>5V 3V 5V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>127</td>
<td>46.7mA</td>
<td>26.2mA</td>
</tr>
<tr>
<td>16.6mA</td>
<td>14.9mA</td>
<td>1.3mA</td>
</tr>
</tbody>
</table>

Sram and dram current consumptions are based on six 128Kbyte chips and 256Kbyte SIMMs respectively, organised as three word wide banks of 256Kbyte.
specifying the associated bank select register, which in turn defines the physical memory parameters. An additional three bits shift the location of the section on 128K boundaries, Fig. 3.

Bank switching is the second mechanism for controlling memory. It maps 16Kbyte, 32Kbyte, 64Kbyte blocks in segments D000, B000 and C000/E000/F000 respectively. When enabled, the bank switch supplies the upper address lines, giving access to the full 64Mbyte of address space. The PCMCIA interface uses the bank switching to access large amounts of memory, often used instead of disc drives. A full set of PCMCIA configuration registers support large amounts of memory, often used instead of disc drives. A full set of PCMCIA configuration registers is significant since it is the only one that has i/o features supporting a range of PCMCIA cards.

Additional registers allow even finer tuning of memory management, but the description of how is too lengthy for a magazine article.

i/o subsystem

All of the peripherals of the PC-XT in addition to the RTC normally associated with the PC-AT are contained in the i/o subsystem. Functions used within the XT architecture are implemented in hardware and SuperState R software. This association emulates the DMA subsystem and overcomes the standard DMA device.

Provision is also made for five multipurpose control pins which can be used for address decoding and for generating signals reflecting divisions of the 32KHz clock and processor status.

bios support

For a small royalty fee a fully configurable basic input/output system - bios - is available. Accompanied by a manual, the bios configuration utility adapts the bios to your own specific system requirements.

I will outline the more salient features. Firstly, the configuration software is interactive and gives a menu structure to all the modifiable system parameters. This can directly generate a binary image of the bios with the parameters and corresponding text file. The text file can be viewed and edited, and then read back into the configuration software.

To take advantage of the sophisticated power management facilities of the chip, the bios provides an automatic power saving mode. It also uses the battery backed ram associated with the real time clock to support a range of options. These can be modified via a built-in setup screen when the system is active. This allows basic changes to the system parameters such as time and date and diskette type, which can be standard 5½in, 3½in or PCMCIA.

Additional external peripheral devices can be initialized by the bios, which is ideal for setting up intelligent output system - bios - is available. Accompanied by a manual, the bios configuration utility adapts the bios to your own specific system requirements.

SuperState R

SuperState R logic is a hardware facility that intercepts all i/o transfers, interrupt and DMA requests. It supports a supervisory operating system which provides another level of hardware isolation below the bios. This allows the interception of bios and dos calls. The chip uses such interception to simulate the real time clock with a simple 32 bit counter and other system functions.

Execute-in-place software

In small low powered systems, magnetic media are impractical. For this reason, roms are used for permanent data storage, so called rom-disks. As programs can be executed from rom, the rom disk introduces a new program format, XIP, which minimizes system ram requirements and reduces cost and power consumption.
PC ENGINEERING

Further, a minibus bug is built into the bus which provides features similar to the standard debug utility. This allows interactive modification of memory and I/O, viewing of system registers and basic assembler/disassembler functions. It also supports single stepping through code and the addition of breakpoints. Modification of SuperState R parameters is also possible via the debugger. To allow the use of keystops instead of an external PC type keyboard, the SuperState R feature provides a scannable keyboard facility.

Further reading
Chips and Technologies, California (C&T is distributed by Siretta minirelectronics, Reading, Berkshire).
Vadem VG-230 sub-notebook engine technical reference, Vadem, 1992, San Jose, California.

DOS for embedded systems

The DOS operating system provides the foundation necessary to run PC programs. PC programs come in two formats — executable files with the .com or .exe extension, and command files with the extension .COM. Executable files have a header that identifies the DOS requirements of their memory requirements. DOS will allocate the necessary memory and copy the program into memory.

Command files require no memory allocation, and will load and run faster than the .exe files. However they can only be used for programs with less than 64K of memory. Both need DOS for low level functions, such as reading a character from the keyboard or displaying characters to the VDU.

Standard DOS includes numerous features that would not normally be appropriate for embedded systems. Some companies offer a cut-down version specifically adapted for such systems.

As far as I know, there are four systems providing a range of unique features, from the use of reduced memory to embedded debuggers. They are Promdos manufactured by Appcom, distributed by DSL, RomDOS manufactured by Datatite and distributed by Exxos, and Embedded DOS manufactured by General Software, distributed by Great Western Instruments.

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A disk containing all the example listings used in this book is available at £29.96. Please specify size required.

C HERE!

If you have followed our series on the use of the C programming language, then you will recognise its value to the practising engineer. But, rather than turning up old issues of the journal to check your design for a digital filter, why not have all the articles collected together in one book, Interfacing with C?

The book is a storehouse of information that will be of lasting value to anyone involved in the design of filters, A-to-D conversion, convolution, Fourier and many other applications, with not a soldering iron in sight.

To complement the published series, Howard Hutchings has written additional chapters on D-to-A and A-to-D conversion, waveform synthesis and audio special effects, including echo and reverberation. An appendix provides a "getting started" introduction to the running of the many programs scattered throughout the book.

This is a practical guide to real-time programming, the programs provided having been tested and proved. It is a distillation of the teaching of computer-assisted engineering at Humberside Polytechnic, at which Dr Hutchings is a senior lecturer.

Source code listings for the programs described in the book are available on disk.
The previous article in this series dealt with several popular output stages, showing how their distortion could be attributed to three different mechanisms. This article examines ways of dealing with these shortcomings, and the effect of the distortion mechanisms on a closed loop output stage.

By Douglas Self.

Distortion in power amplifiers

5: output stages

From earlier work in this series, distortion from the small-signal stages may be kept to levels that will prove negligible compared with distortion from a closed-loop output stage. Similarly, future work in this series will show that distortion mechanisms 4 to 7 from my original list (EW+VVIV, July 93) can be effectively eliminated by lesser-known but straightforward methods. This leaves the third mechanism in its three components as the only distortion that is in any sense unavoidable: Class-B stages free from crossover artifacts are not exactly commonplace.

This is a good place to introduce the concept of a blameless amplifier, one designed so that all the easily-defeated distortion mechanisms have been rendered negligible. The word blameless has been carefully chosen to not imply perfection.

The first distortion, non-linearity in the input stage, cannot be totally eradicated but its onset can be pushed well above 20kHz. The second distortion, non-linearity in the voltage amplifier stage, can be effectively eliminated by cascoding. Distortion mechanisms four to seven, concerned with such things as earth return loops, power supply impedance and non-linear loading, can be made negligible by simple measures to be described later.

Large-signal distortion

The large-signal nonlinearity performance of all the bipolar junction transistor stages outlined in the previous part of this series have these features in common:

- Large-signal nonlinearity increases as load impedance decreases. In a typical output stage loaded with 8Ω, closed-loop LSN is usually negligible, the THD residual being dominated by high-order crossover artefacts that are reduced less by negative feedback. At lower impedances, such as 4Ω, relatively pure third harmonic becomes obvious in the residual.

- LSN worsens as the driver emitter or collector resistances are reduced, because the driver current swings are larger. On the other hand, this reduction improves output device turn-off, and will so decrease switchoff distortion; the usual compromise is around 4Ω to 10Ω.

The BJF output gain plots in the previous article reveal that the LSN is compressive, the voltage gain falling off with higher output currents. It is roughly symmetrical, generating third-harmonic, and is much greater at the very lowest load impedances; this is more of an issue now that 2Ω-capable (for a few minutes, anyway) amplifiers are considered macho, and some speaker designers are happy with 2Ω impedances through.

I suggest that the fundamental reason for this gain droop is the fall in output transistor beta as collector current increases, due to the onset of high level injection effects. In the emitter follower topology, this fall in beta draws more output transistor base current from the driver emitter, pulling its gain down further from unity; this is the change in gain that affects the overall transfer ratio.

The output device gain is not directly affected, as beta does not appear in the classical expression for emitter follower gain, providing the source impedance is negligibly low. This assertion has been verified by altering an output stage simulated in Spice such that the output bases are driven directly from zero-impedance voltage sources rather than drivers; this abolishes the gain droop effect, so it must be in the drivers rather than the output transistors.

Further evidence for this view is that in Spice simulation, the output device Ebers-Moll model can be altered so that beta does not drop with Ic (simply increase the value of the parameter BKT) and once more the gain droop does not occur, even with drivers. Here is one of the best uses of circuit simulation tweaking the untweakable. Gain droop does not affect fet outputs, which have no equivalent beta loss mechanism. See Fig. 12 of Part 4, where the wings of the fet gain plot do not turn downwards at large outputs.

It used to be commonplace for output transistors to be sold in pairs roughly matched for beta, allegedly to minimise distortion; this practice seems to have been abandoned. Simulation shows that beta mismatch produces an unbalanced gain droop that markedly increases low order harmonics without much effect on the higher ones. Modern amplifiers with adequate feedback factors will linearise this effectively. This appears to be why the practice has ceased.

Improving large signal linearity

It will be suggested that, in a closed loop blameless amplifier, the large signal nonlinearity contribution to total distortion (for 8Ω loadings) is actually very small compared with that from crossover and switchoff. This is no longer true at 4Ω and still less so for lower load impedances. Thus ways of reducing this mechanism will still be useful.

The best precaution is to choose the most linear output topology. The previous article suggested that the open loop complementary
feedback pair output is at least twice as linear as its nearest competitor, (the emitter follower output) and so the CFP is usually the best choice unless the design emphasis is on minimising switchoff distortion.

In the small signal stages, we could virtually eliminate distortion. If the linearity of the input or voltage amplifier stage was inadequate, it was possible to come up with several ways in which it could be dramatically improved. A Class B output stage is a tougher proposition. In particular we must avoid complications to the forward path that lower the second amplifier pole P2, as this would reduce the amount of feedback that can be safely applied.

Several authors\textsuperscript{2,3} have tried to show that the output emitter resistors of bipolar outputs can be fine tuned in value to minimise large signal distortion, the rationale being that the current dependent internal $r_e$ of the output transistors will tend to cause the gain to rise at high currents, and that this gain variation can be minimised by appropriate choice of the external $R_e$. This is not true in practical output stages whose gain behaviour tends to be dominated by beta loss and its effect on the drivers. In any case the resistor values suggested are such tiny fractions of an ohm that quiescent stability would be perilous.

In real life the $R_e$ of a CFP output stage can be varied between 0.5 and 0.2Ω without significantly affecting linearity; 0.2Ω is a good compromise between efficiency and stability.

The gain droop at high $I_b$S can be partly cancelled by a simple but effective feedforward mechanism. The emitter resistors $R_e$ are shunted with silicon power diodes, which with typical circuit values will only conduct when 4 Ohm loads (or less) are driven. This causes a slight gain increase that works against the beta loss droop. The modest but dependable improvement can be seen in Fig. 1, measured with a 2.7Ω load.

If a 100W/8Ω amplifier is required to drive 4Ω loads then it will need paralleled output devices to cope with the power dissipation. Perhaps surprisingly, the paralleling of output BJTs (driven as usual from a single driver) has little effect on linearity, given elementary precautions to ensure current sharing. However, for the 2Ω case there is a definite linearity improvement on resorting to tripled output devices; this is consistent with the theory that LSN results from beta loss at high collector currents.

**Crossover distortion**

The worst problem in Class B is the crossover region, where control of the output voltage must be transferred from one device to another. Crossover distortion generates unpleasant
high order harmonics with the potential to increase in percentage as signal level falls. There is a consensus that crossover caused the transistor sound of the 1960’s, though to the best of my knowledge this has never actually been confirmed by the double blind testing of vintage equipment.

The Vbe, characteristic of a bipolar transistor is initially exponential, blending into linear as the emitter resistance Re comes to dominate the transconductance. The usual Class B stage puts two of these curves back to back, and Peter Blomley has shown that these curves are non-conjugate, i.e. there is no way they can be rearranged to sum to a completely linear transfer characteristic. Whatever the offset imposed by the bias voltage.

This can be demonstrated quickly and easily by Spice simulation; see Fig. 2. There is at first sight not much you can do except maintain the bias voltage, and hence quiescent current, at some optimal level for minimum gain deviation at crossover; quiescent current control is a topic that could fill a book in itself, and cannot be considered properly here.

It should be said that the crossover distortion levels generated in a blameless amplifier can be low up to around 1kHz, being barely visible in residual noise and only measurable with a spectrum analyser. For example, if a blameless closed-loop Class B amplifier is driven through a TL072 unity gain buffer the added noise from this op-amp will usually submerge the 1kHz crossover artifacts into the noise floor. (It is most important to note that distortion mechanisms 4 to 7 create disturbances of the THD residual at the zero crossing point that can be easily mistaken for crossover distortion, but the actual mechanisms are quite different). However, the crossover distortion becomes obvious as the frequency increases, and the high order harmonics benefit less from NFB. See text panel Improving crossover distortion.

It will be seen later that in a blameless amplifier the linearity is dominated by crossover distortion, even with a well designed and optimally biased output stage. There is an obvious incentive to minimise it, but there seems no obvious way to reduce crossover gain deviations by tinkering with any of the relatively conventional stages considered so far. Significant improvement is only likely through application of one of the following techniques:

- The use of Class AB stages where the handover from one output device to the other is genuinely gradual, and not subject to the small doubling effects that an over biased Class B stage shows. One possibility is the so called Harmonic AB mode.5
- Non-switching output stages where the output devices are clamped to prevent turn off, and thus hopefully avoiding the worst part of the Vbe-Ibe curve.6
- Error correcting output stages implementing either error feedforward or error feedback. The latter is not the same thing as global NFB, being instead a form of cancellation.7

Switching distortion

This depends on several variables, notably the speed characteristics of the output devices and the output topology. Leaving aside the semiconductor physics and concentrating on the topology, the critical factor is whether or not the output stage can reverse bias the output device base emitter junctions to maximise the speed at which carriers are sucked out, so the device is turned off quickly.

The only conventional configuration that can reverse bias the output base emitter junctions is the emitter follower type II, described in the previous article. A second influence is the value of the driver emitter or collector resistors; the lower they are the faster the stored charge can be removed.

Applying these criteria can reduce HF distortion markedly, but it is equally important that it minimises output conduction overlap at high frequencies. If unchecked, overlap results in an inefficient and potentially destructive — increase in supply current. Illustrating this, Fig. 3 shows current consumption vs frequency for varying driver collector resistance, for a CFP type output.

Figure 4 shows how HF THD is reduced by adding a speed-up capacitor over the common driver resistance of a Type II emitter follower output stage. Taken at 30V/8Ω.

More once, these will have to be examined in the future.

Selecting an output stage

Even if we stick to the most conventional of output stages, there are still an embarrassing large number to choose from. The cost of a complementary pair of power fets is currently at least twice that of roughly equivalent BJTs, and taken with the poor linearity and low efficiency of these devices, the use of them may require a marketing rather than a technical motivation.

The seven main sources of distortion

It is one of the central themes of this series that the primary sources of power amplifier distortion are seven fold:

1. Nonlinearity in the input stage.
2. Nonlinearity of the voltage amplifier stage (VAS), 2nd harmonic, rising at 6dB/octave.
3. Nonlinearity of the output stage.
4. Nonlinearity resulting from taking the NFB feed incorrectly.
5. Nonlinearity caused by large rail decoupling capacitors feeding the distorted supply rail signals into the signal ground.
6. Nonlinearity caused by induction of Class B supply currents into the output, ground, or negative feedback lines.
7. Nonlinearity resulting from taking the NFB feed incorrectly.
the best at coping with switchoff distortion but the quiescent current stability is not of the best.

The CFP topology has good quiescent stability and low LSN; its worst drawback is that reverse biasing the output bases for fast switchoff is impossible without additional HT rails.

The quasi-complementary with Baxandall diode stage comes close to mimicking the emitter follower type stages in linearity, with a potential for cost saving on output devices. Quiescent stability is not as good as the CFP.

Closing the loop
In Parts 2 and 3 of this series it was shown how relatively simple design rules could ensure that the THD of the small signal stages alone could be reduced to less than 0.001%; it will be seen at once that these amplifiers are definitely not distortionless, though the performance is markedly superior to the usual run of hardware. THD in the LF region is very low, well below a noise floor of 0.0007%, and the usual rise below 100Hz is very small indeed. However, above 2kHz, THD rises with frequency at between 6 to 12 dB/octave, and the residual in this region is clearly time aligned with the crossover region, and consists of high order harmonics rather than second or third.

It is intriguing to note that the quasi-Bax output gives about the same HF THD as the emitter follower topology, confirming the statement that the addition of a Baxandall diode turns a conventional quasi-complementary stage with serious crossover asymmetry into a reasonable emulation of a complementary emitter follower stage.

Harmonic generation by crossover distortion

The usual nonlinear distortions generate most of their unwanted energy in low order harmonics that NFB can deal with effectively. However, crossover and switching distortions that warp only a small part of the output swing tend to push energy into high order harmonics, and this important process is demonstrated here, by Fourier analysis of a Spice waveform.

Take a sinewave fundamental, and treat the distortion as an added error signal E, letting the ratio WR describe the proportion of the cycle where E>0. Fig. 10 shows how the situation is made more like crossover or switching distortion by squeezing the triangular waveform into the centre of the cycle so that its value is zero elsewhere; now E=0 for only half the cycle (denoted by WR=0.5) and Fig. 9 shows that the even harmonics are no longer absent. As WR is further decreased, the energy is pushed into higher order harmonics, the amplitude of the lower harmonics falling.

These high harmonics have roughly equal amplitude, spectrum analysis confirming that even in a blameless amplifier driven at 1kHz, harmonics are freely generated from the 7th to the 19th at a level within a dB or so. The 19th harmonic is only 10dB below the 3rd.

Thus, in an amplifier with crossover distortion, the order of the harmonics will decrease as signal amplitude reduces, and WR increases; their lower frequencies allow them to be better corrected by the frequency dependant negative feedback. This effect seems to work against the commonly assumed rise of percentage crossover distortion as level is reduced.

![Fig. 9. The amplitude of each harmonic changes with WR as the error waveform gets narrower, energy is transferred to the higher harmonics.](image)

![Fig. 10. Diagram of the error waveform E for some values of WR.](image)
Table 1. Summary of closed loop amp THD performance.

<table>
<thead>
<tr>
<th>Stage</th>
<th>1kHz THD</th>
<th>10kHz THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter follower</td>
<td>0.0019%</td>
<td>0.013%</td>
</tr>
<tr>
<td>CFP</td>
<td>0.0008%</td>
<td>0.005%</td>
</tr>
<tr>
<td>Quasi Bax</td>
<td>0.0015%</td>
<td>0.015%</td>
</tr>
</tbody>
</table>

AP plots in Figs 5 to 7 were taken at 100Watts/8Ω, from an amplifier with an input error of ~70dB at 10kHz and a/f gain of 27dB, giving a feedback factor of 43dB at this frequency. This is well above the dominant pole frequency, so the NFB factor is dropping at 6dB/octave and will be down to 37dB (or 70x) at 20kHz. My experience suggests that this is about as much NFB as is safe for general use, assuming an output inductor to improve stability with capacitive loads. Sadly, published data on this touchy topic seems non-existent.

There is significantly less HF THD with a CFP output; this cannot be due to large signal nonlinearity as this is negligible with an 8Ω load for all three stages, and must result from lower levels of high order crossover products.

Despite the promising ingredients, a distortionless amplifier has failed to materialise, so we had better find out why...

When an amplifier with a frequency dependent NFB factor produces distortion, the reduction is not due to the NFB factor at the fundamental frequency, but the amount available at the frequency of the harmonic in question.

A typical amplifier with open loop gain rolling off at 6dB/octave will be half as effective at reducing 4th-harmonic distortion as it is at reducing the second harmonic. LSN is largely third (and possibly second) harmonic, and so NFB will deal with this effectively. However, both crossover and switchoff distortions generate high-order harmonics significant up to at least the 19th and these receive much less linearisation. As the fundamental moves up in frequency the harmonics do too, and get even less feedback. This is the reason for the differentiated look to many distortion residuals; higher harmonics are emphasised at the rate of 6db/octave.

Here is a real example of the inability of NFB to cure all amplifier ills. To reduce this HF distortion we must reduce the crossover gain deviations of the output stage before closing the loop. There seems no obvious way to do this by minor modifications to any of the conventional output stages; we can only optimise the quiescent current.

Increasing the quiescent current will do no good for, as outlined in the previous article, Class AB is generally Not A Good Thing, producing more distortion than Class B, not less.

Fig. 8 makes this painfully clear for the closed-loop case: Class AB clearly gives the worst performance. (As before, the AB quiescent was set for 50:50 m/s ratio of the gm doubling artefacts on the residual).

In this case the closed loop distortion is much greater than that from the small signal stages alone; however this is not automatic, and if the input pair is badly designed its HF distortion can easily exceed that caused by the output stage.
Misspelled words have been corrected.

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Fig. 8. Closed-loop CFP amp. Setting quiescent for Class AB gives more HF THD than either Class A or B.

Conclusions

Taking this and the previous article together, we can summarise. Class AB is best avoided. Use pure Class A or B. as AB will always have more distortion than either. Fet outputs offer freedom from some BJT problems, but in general have poorer linearity, lower efficiency, and cost more.

Distortion generated by a blameless amplifier driving an 8Ω load is almost entirely due to crossover effects and switching distortion. This does not hold for 4Ω or lower loads where third harmonic on the residual shows the presence of large signal nonlinearity caused by beta loss at high output currents.

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There is usually a trigger signal, called the clock, which controls the passing of data from inputs to outputs. The triggering event is often the low to high transition of the clock input, and the state of the inputs at this moment (and a few nanoseconds before and after) determines what state the outputs will take immediately after the active clock edge. Any changes of input levels away from the active clock edge will not affect the output.

If the outputs are fed back, so that they form part of the input to the device, the result is a state machine. A typical state machine is shown in Fig. 1. The output state is held in a set of flip-flops called a register; the same clock is shared by all the flip-flops so that data is loaded into each one simultaneously. The core of the machine is still combinatorial logic but, even if the output of the core logic changes, the output register will not be altered until the active clock edge.

Many practical systems can be defined as state machines. Consider something as common as a lift (or elevator). In a three storey building, a lift can have seven possible states (see Fig. 2): it can be stationary at a floor, or in transit between any two of the floors, moving up or down. If it is stationary it will only move if it is called to another floor; if it is moving it will only stop if it has been called to the floor which it is approaching, unless that happens to be the top or bottom.

It may appear as if there is no clock in operation, but a system like this will use a clock to sample the state of the call buttons and lift position. These signals form the inputs to the system; the outputs will act as signals to the lift motor and brake, but will also be fed back as inputs so that the logic knows what the lift is doing.

For example, a call to floor three would be ignored if the lift was descending between floors two and one, but it would be acted on if the lift was stationary at floor two or one.

Note that a practical system would require several auxiliary circuits. For example, some prioritising of the call signals to prevent hogging and a time delay for the door opening and closing, but this does not alter the principles involved.

Registered proms

A standard prom can behave as a combinatorial logic circuit, so a circuit capable of supporting state machines can be made by adding an internal register. Because state information must be logically combined with input data, some of the prom outputs need to be connected back to the

Registered functions, and state machines in particular, can fit into registered proms, registered PALs or FPLSs. Of these, FPLSs are versatile but also expensive and power hungry. As with combinatorial logic, each application needs to be decided on its merits. Geoff Bostock explains the ground rules.

![Registered functions, and state machines in particular, can fit into registered proms, registered PALs or FPLSs. Of these, FPLSs are versatile but also expensive and power hungry. As with combinatorial logic, each application needs to be decided on its merits. Geoff Bostock explains the ground rules.](image-url)
inputs. This has the effect of restricting the number of inputs available for logic connection.

Figure 3 shows how a 16K (2K x 8) registered prom could be connected to control the lift example described above. The seven states can be defined in three state bits; this leaves eight inputs free for inputs to control the lift. Some obvious inputs would be the call signals to the three floors and, perhaps, a door open indicator and emergency stop. It would also be sensible to include signals to indicate when each floor has been reached, in order to allow the lift to be stopped and the door opened.

There are also five outputs free. Possible uses for these could include signals to operate the lift motor, the door motor and one for the brake.

This configuration will just fit into a 16K prom but, as with combinatorial circuits, addition of another input would require a prom of twice the size to accommodate it. Moreover, two more states (ie nine altogether) would need another input and output because four state bits are required to define from nine to sixteen states.

Nevertheless, registered proms are available up to 64K in size and may be used for state machines. Indeed, Cypress has just brought out two proms specifically aimed at state machine applications. The CY7C258 and CY7C259 have internal feedback paths from some outputs to the input side of the prom array. Here they are multiplexed with address lines, giving the designer the option of choosing the width of the fed back state word. Each prom has a 16-bit wide output, although only eight are available in the CY7C258, and an 11-bit input with up to 11 output bits fed back.

The lift example, as described above, would just fit into one of these proms, so let us see how the system would be defined. Fig. 4a shows the state diagram for the lift controller. The seven states are defined as in Fig. 2, together with the values of B2, B1 and B0 for each state, while the arrows show the possible transitions between each state, together with the logic conditions which trigger the transition. Some way is needed to translate this diagram into a format that a PLD assembler will recognise.

This usually takes the form of state equations; the equations, which are equivalent to the state diagram, are shown in Fig. 4b. Conventionally, states are enclosed in square brackets; thus, [AT3] means state AT3. The WHILE operator refers to the present state, the IF argument is the transition condition, THEN gives the next state and WITH defines which will be recognised by a PLD logic assembler. A common format is the WHILE 1..1 IF... THEN ... notation. The WHILE operator refers to the present state, the IF argument is the transition condition, THEN gives the next state and WITH defines which will take place at the active edge of the common clock driving the state register.

Transitions between states are shown on the diagram as arrows; each arrow is labelled with the logic function which must be true for the transition to occur. This is the transition condition for the jump, which will take place at the active edge of the common clock driving the state register.

To program a PLD with this data it must be converted to a format which will be recognised by a PLD logic assembler. A common format is the WHILE [...], IF ..., THEN [...], WITH ... notation. The WHILE operator refers to the present state, the IF argument is the transition condition, THEN gives the next state and WITH defines any output which may be associated with the next state. The state equations derived from figure 4a are shown in Fig. 4b.
depends on which logic formatter is being used.

To complete this example the \( \text{door}_\text{close} \) and emergency stop signals must be defined. \( \text{door}_\text{close} \) happens automatically when a call button is pressed and the door is open, although in a practical system there would be some delay after the lift reached a floor to allow passengers time to leave or enter the lift. It is defined by the equation:

\[
\text{CLOSE}\_\text{DOOR} := \text{door}_\text{open} \& (\text{CALL}_3 \& \text{CALL}_2 \& \text{CALL}_1)
\]

Here the symbol ':=' means equals at the active clock edge.

Similarly we can write an equation:

\[
\text{BRAKE} := \text{STOP} \& \text{AT}_3 \& \text{AT}_2 \& \text{AT}_1
\]

implying that the brakes are applied when the emergency stop button is hit or when the lift is stopped at one of the floors. Note that this notation means that the brakes will only be applied as long as the stop signal is active. This is because the register is made from D-type flip-flops, which do not hold their data once an input is removed, unlike J-K flip-flops.

**Registered PALS**

Registered proms suffer from the same drawbacks as combinational proms, the chief one being that an extra input requires a doubling of array size. This can be particularly irksome in state machines whose arrays have several inputs allocated to fed back outputs. As with combinational logic, the simplest solution is to make the and-array programmable; if the or-array is fixed then the result is a PAL structure.

The circuit diagram of a basic registered PAL output is shown in Fig. 5. The registered output passes through an inverting three state buffer, but the feedback to the and-array is taken directly from the inverting output of the flip-flop. Even when the outputs are switched off the feedback is still operating. Both output and feedback are inverted, so registered PALS are effectively active-low, meaning that care must be taken over the way in which transition terms trigger state bit changes.

As with proms, D-type flip-flops are used to form the state register. Any state bit which should not change when the transition condition is removed must, therefore, be provided with a separate product term defining the 'hold' condition. We can illustrate this with a simple binary counter example.

The least significant bit always toggles when the counter is counting. It may be defined very simply by:

\[
\text{Q}_0 := \text{Q}_0 \& \text{COUNT}
\]

The next bit (Q1) toggles only when Q0 is high; this might be defined by:

\[
\text{Q}_1 := \text{Q}_1 \& \text{Q}_0 \& \text{COUNT}
\]

This definition will cause Q1 to go low whenever the transition condition \( (\text{Q}_1 \& \text{Q}_0) \) is not true, but we want Q1 to remain high when Q1 is high and Q0 is low; that is, counting from two to three. We also want Q1 to stay high if COUNT goes low, and the count is halted temporarily. To do this we must add terms to that effect, so the complete equation for Q1 becomes:

\[
\text{Q}_1 := \text{Q}_1 \& \text{Q}_0 \& \text{COUNT} \& \text{Q}_1 \& \text{Q}_0 \& \text{COUNT}
\]

If we investigate adding a third counter bit we find that the situation becomes even worse. Q2 will toggle low to high on the three to four transition, but must be held high on the next three counts, four, five and six. These three present states need two product terms to cover them:

\[
\text{Q}_2 := \text{Q}_2 \& \text{Q}_1 \& \text{Q}_0 \& \text{COUNT} \quad (\text{toggle at 3 or 7})
\]

\[
\text{Q}_2 := \text{Q}_2 \& \text{Q}_1 \& \text{COUNT} \quad (\text{hold high at 4 or 5})
\]

Every higher bit we count needs an additional product term to define the hold while counting condition. As we shall see, standard registered PALS contain just eight product terms per output, so the Q6 output would use all the product terms available to it.

Fig. 6 shows the Karnaugh map for Q2. From this it may be deduced that Q2 can be written:

\[
\text{Q}_2 := \text{Q}_2 \& \text{Q}_1 \& \text{Q}_0 \& \text{COUNT}
\]

A registered output, such as that shown in Fig. 7, can cope with any order bit in a counter chain because the exclusive-or gate allows equations like this to be programmed directly into the PAL. The standard families of registered PAL are based on the 20 pin combinational PAL16L8 and 24 pin PAL20L8. In each case a series of PALS is available with registered outputs of the form of Fig. 5 replacing four, six or eight of the combinational outputs. These make the PAL16K4, PAL16R6 and PAL16R8 from the PAL16L8, and PAL20R4, PAL20R6 and PAL20R8 from the PAL20L8.

A third family has been created by replacing four, eight or ten of the PAL20L10 combinational outputs by exclusive-OR registered outputs, as in Fig. 7. These are the PAL20X4, PAL20X8 and PAL20X10. Their principal use is in making counters: up to divide-by-1024 can be incorporated into the PAL20X10.

The PAL16R8 and PAL20R8n families may be used for making small state machines, but are limited by having only eight product terms per output, and by the need to include terms to hold the output high, as we saw with the basic counter. They are also useful in applications where synchronisation is required, when they can be considered merely as a combinational logic block driving a synchronising register.

**Field programmable logic sequencers**

Just as registered proms and PALS are derived from their combinational counterparts, so FPLSs are derived from PALs.
DESIGN

**Fig. 8.** Field programmable logic sequencer (FPLS) block diagram.

**Fig. 9a:** Below left, state diagram of a priority controller for lift calls.

**Fig. 9b:** Below right, state table of a priority controller for lift calls. FPLS programmers can accept state transition data in a state table format. This makes it unnecessary to use a logic assembler. Each present state is coded into the table, just as in an FPLA truth table, and the transition condition and next state entered on the same line. If there is more than one transition from any state then each transition must occupy a separate line, but the order in which lines are entered is unimportant except for readability. This table is the state table derived from the state diagram of Fig. 9a.

FPLAs. **Figure 8** shows a very general FPLS architecture; not all FPLSs have all the features shown in this diagram. Because the principal use of FPLSs is in building state machines, I will describe their architecture while bearing this in mind.

The state of the FPLS before the next active clock edge is called the present state, and this data is held in the buried register and/or the output register. The present state is fed back to the and-array where it is logically combined with input data. If the combination of feedback and input has been programmed into the FPLS as a valid transition condition, the appropriate product term will be high and will be fed into the or-array.

FPLSs use either R-S or J-K flip-flops as their register elements. Unlike D-types, once a high or low is established it will remain until the flip-flop is actively changed. A high from the and-array can be transmitted via programmable connections to or-terms feeding the flip-flop inputs. At the active clock edge these flip-flops will be set or reset, while any not receiving a high will remain unchanged. In this way a new present state is asserted.

If the feedback/input combination does not form a valid transition condition all the flip-flop inputs will be low when clocked, and the state of the register will remain unchanged.

As an example of how an FPLS can be used for a simple state machine, let us construct a priority control circuit for the three floor lift. The state diagram is shown in **Fig. 9a.**

The state machine interrogates each call signal in turn and accepts the call if the signal is high. Floor 2 is given extra priority as it makes sense not to by-pass this floor if the lift is moving from one to three or vice versa. The diagram is
arranged so that the third floor has priority over the first if the first floor was visited last, and the same in reverse.

The first stage in designing an FPLS for this state machine is to allocate binary numbers to each state. In this case we have given the [ASK1] state the number 000. The second floor enquiries have two states depending on the position of the lift; when it is at the first floor, or no response has been made to a first floor enquiry, we have the [ASK2] state which we are calling 010, and so on for all eight states.

An FPLS state table has three sections in each row, or transition term: these are the input conditions, the present state and the next state. The usual way to proceed is to take each state in turn and define all the possible transitions out of them. Thus, the first line in the state table in Fig. 9b is the transition from [ASK1] to [ACCEPT1], which needs CALL1 high. The next line gives the result if CALL1 is low, when the next state is [ASK2A]. In all, twelve transition terms are required, each one corresponding to one arrow in the state diagram.

Physically, each transition term occupies one AND term in the and-array, with the inputs and present state, while the next state defines the or-array connections. An 'H' in an output column causes the AND term output to be connected to the 'J' of a J-K flip-flop or the 'S' of an R-S type, while an 'L' will join it to the 'K' or 'R'.

While we have described a manual entry method for generating the state table, it is equally valid to write state equations in the syntax described earlier. For example we could write:

```
WHILE [ASK1]
IF CALL1 THEN [ACCEPT1]
IF !CALL1 THEN [ASK2A]
```
and so on.

Either the Philips SNAP program or one of the proprietary assemblers, such as ABEL, CUPL or LOG/iC, can then be used to generate the state table from the state equations.

While this example is based on an imaginary lift which is confined to three floors, it might be easily modified to a situation where three processors are competing for resources in a multi-processor environment. Two methods are commonly used in this type of application, round robin, where each subject is interrogated in turn until one is found requiring service, and last granted lowest priority, where the controller creates a queue, the last processor going to the back of the queue when it has finished using the shared resources.

One feature unique to FPLSs is the complement term; it is an inverting feedback from the or-array to the and-array. Its purpose is to allow the ELSE construct in state equations. Logically, it does this by or-ing all the defined transitions from a given state and inverting the result. This is then itself used as an input condition for the case when none of the defined conditions is true.

The physical construction of the complement array is shown in Fig. 10, and we can illustrate its use with the state table in Fig. 11a. This is a state machine which allows access to a system via an entry code; it bears some resemblance to an automatic teller system ('hole-in-the-wall'), except that the PIN is hard-wired and only three digits have to be entered.

From the state [START] an '8' must be entered; this will be accompanied by a KEY signal to indicate a key depression and will cause a jump to state [OK1]. Any other number with KEY will cause a jump to [FAIL].

Releasing key '8' changes KEY to !KEY and state [PAUSE1] is entered. This proceeds with a '1' and a '3' until state [PASS] is reached when the system can be accessed. Once the transaction is complete the system will

```
WHILE [ASK1]
WHILE [ASK2]
WHILE [ASK3A]
```

Feeding back the inverse of '8' & KEY provides a logic signal which triggers the jump to [FAIL] when gated with the valid key input. The same complement term can be used by other states without interference because any TRUE transition overrides any FALSE inputs to the OR gate which drives the feedback. Also, if all the transitions from the current present state are FALSE, no other transitions can be TRUE because their present states are not the current present state.

Fig. 11b shows how the complement term is entered into a state table. An 'A' in the complement term column (C) generates a complement, that is it connects a transition to the complement OR gate. A '!' propagates the complement back to the input array.

Fig. 10. FPLS complement term.

Fig. 11a. State diagram of a simple coded access system.

Fig. 11b. State table of a simple coded access system. The complement term found in FPLSs is used to implement the ELSE condition. In the state diagram of Fig. 11a, a transition from [START] to [OK1] is triggered by an '8' being entered along with a valid key signal. Any other number will cause a jump to the [FAIL] state. This could be achieved by making transition terms with all other possible numbers, but the complement term allows this to be done in a single term.

Feeding back the inverse of '8' & KEY provides a logic signal which triggers the jump to [FAIL] when gated with the valid key input. The same complement term can be used by other states without interference because any TRUE transition overrides any FALSE inputs to the OR gate which drives the feedback. Also, if all the transitions from the current present state are FALSE, no other transitions can be TRUE because their present states are not the current present state.

Fig. 11b shows how the complement term is entered into a state table. An 'A' in the complement term column (C) generates a complement, that is it connects a transition to the complement OR gate. A '!' propagates the complement back to the input array.
reset the state machine to [START]. [FAIL] will have the same effect except that the cash card will be retained.

The jump condition from [START] to [OK1] is easily defined as:

\[
\text{WHILE [START]}
\]

\[
\text{IF } B3 \& \neg B2 \& \neg B1 \& \neg B0 \text{ THEN [OK1]} \text{ but the jump to [FAIL] needs four terms as } (\neg B3 \& \neg B2 \& \neg B1 \& \neg B0) \text{ must be expanded to } \neg B3 \# B2 \# B1 \# B0. \text{ However, with the complement term we can write the jump condition as:}
\]

\[
\text{ELSE IF KEY THEN [FAIL]}
\]

The complement term can still be used with transitions from states [PAUSE1] and [PAUSE2] because the logic signal which is fed back, inverted, is low if any of the transition terms or-ed into it is high. Even though, while in state [START], the transitions out of [PAUSE1] and [PAUSE2] are invalid, the complement term will remain inactive unless the transition from [START] to [OK1] is itself invalid. A similar argument applies to [PAUSE1] and [PAUSE2] themselves.

Figure 11b shows the full state table for this system. The convention for entering the complement term is to use an 'A' for attaching it to an and-term, and a '!' for feeding it back to the and-array. The whole diagram can be defined in nine terms, and further reduction is possible with some simple logic minimisation. Without minimisation and the complement term, eighteen transition terms would have been required.

We can now look at FPLS device options. There are two families of FPLS based, respectively, on R-S and J-K flip-flops. The PLS105 was introduced about fifteen years ago and has a straightforward architecture, as in Fig. 12. With sixteen inputs, an eight-bit output register, a six-bit internal register, 48 transition terms and a complement term, it can cope with some very complex state machines. The coded access system described above would fit into one corner of a PLS105.

There have been a number of derivatives of the chip. Where the PLS105 needs a 28 pin package, the PLS167 and PLS168 fit into 24 pin packages by reducing the number of inputs and, in the case of the PLS167, the number of outputs. Some enhanced versions, such as the PLS405, the PLS506 and PLS105/16 have also been made. They follow the same basic architecture but may have more transition terms or register bits.

Figure 13 shows the output register of the PLS155 family. Based on a J-K flip-flop, it is surrounded by other programmable features which increase its versatility. Foremost of these is the J to K inverter. When this is active, it makes the J-K flip-flop emulate a D-type. The flip-flop type can be set for whichever is the most efficient for the application, and can even be changed in mid operation. This is described in a Philips application note, where a PLS159 is used as an eight bit shift register/counter.

Another useful feature is the ability to load the register directly from the outputs. This could be used in testing the device, to set the register into a known state, or in operation: data from a microprocessor bus could be loaded into the register, and then read back at a later time after some modification according to the input conditions.

This family also contains combinatorial i/o pins. Each device has twelve potential outputs. These are either four (PLS155), six (PLS157) or eight (PLS159/PLS179) registered with the balance of twelve bidirectional i/o. The PLS179 is a 24 pin device, with eight dedicated inputs, the others come in 20 pin packages with four inputs.

As a final example of using FPLSs, and the PLS155 in particular, we can look at the design of a Gray Code counter. The count sequence for four bits is shown in Fig. 14a. Because there are sixteen states, sixteen transition terms would be needed if this were designed as a basic state machine. The Karnaugh Maps for the four counter bits are shown in Fig. 14b, for a design using D-type flip-flops. This cuts the design to thirteen transition terms.

Note, however, that Q3 and Q2 each require three terms, but inspection of the count sequence shows that they only change their level twice, as indicated by the rings round the changes in Fig. 14a. Toggling is a function of J-K flip-flops, so if Q3 and Q2 use these, two more terms can be saved. This is not crucial if no other functions are being incorporated into the FPLS, but a reduction from sixteen to eleven terms might be important if the Gray Code counter is only one part of the overall FPLS function.

The full state table for the FPLS is shown in Fig. 14c. The symbol 'O' is used for the toggle function as both 'J' and 'K' inputs must be driven high for toggling; this is the unblown fuse condition of the FPLS. The fuse which enables the J to K inverter must also be blown for Q3 and Q2, shown by a '!' in the flip-flop control field (fc). The 'A' in this field for Q1 and Q0 leaves the inverter enable fuse intact.

To specify this function with equations is equally valid, and will give the same result if a PLD compiler is used to assemble them. The usual format for specifying the flip-flop type in any device where this is alterable is:

\[
\begin{align*}
Q3.T & := Q3 \land Q2 \land Q1 \land Q0 \\
Q3 & := Q3 \land Q2 \land Q1 \land Q0 \\
Q0.D & := Q3 \land Q2 \land Q1 \\
\end{align*}
\]

etc.
can be saved.

result, two terms state twice. As a Q3 only change shows that Q2 and count sequence.

Inspection of the count sequence.

**Fig. 14a. Gray code:**

**Q3**

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**Q0**

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**Fig. 14a. Gray code count sequence. Inspection of the count sequence shows that Q2 and Q3 only change state twice. As a result, two terms can be saved.**

**Fig. 14b.**

**Karnaugh maps for gray code count bits.**

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Edited by F F Mazda

Faidoon Mazda has worked in the electronics and telecommunication industry for over twenty years, and is currently Product and Operations Manager, Generic Network Management, with Northern Telecom. He is the author of six technical books (translated into four languages) and the editor of the Communications Engineers Reference Book published by Butterworth-Heinemann.

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The facts and figures of HF receiver performance

Jon Dyer cuts through the haze of misunderstanding surrounding receiver performance. He looks in detail at each parameter, what it means and why it's important, and shows why "dynamic" performance parameters are vital.

Receiver performance specifications can be complex. But that is a necessity, as all parameters must be specified accurately and completely if confusion is to be avoided.

The first parameter to look at is sensitivity, the measure of a receiver's capability to amplify the smallest of signals without losing any of the "intelligence" carried by the signal. Once the signal level falls close to the receiver noise level, normally expressed as a signal to noise ratio (S/N), intelligibility will be lost. Even a hypothetically perfect (noiseless) receiver would still run into thermal noise.

Sensitivity is defined as the signal voltage required to give a specific S/N in a particular receiver bandwidth, for a particular receiver mode (e.g., AM or SSB). Modulation level is specified for AM (often 30%), and a modulation deviation (e.g., 5kHz) for FM. An alternative definition for FM is to use quieting sensitivity: the input level required to reduce output noise by, say, 20dB (squelch off).

Bandwidth must also be taken into account because noise is proportional to the square root of the bandwidth.

Bipolar transistors and FETs can produce sensitivities of 0.5µVEMF for a 10dB S/N ratio (3kHz bandwidth, HF, for an SSB or CW signal) and similar levels can be obtained on FM.

Noise factor

The sensitivity figure is an intuitive way of describing the sensitivity of a receiver. But it is also rather complex, related to a particular bandwidth, temperature, receiver mode, S/N ratio, and input impedance.

A much more convenient measurement is the noise factor (NF), a single number telling everything that needs to be known about a receiver's sensitivity. It is the ratio of the S/N of a hypothetically perfect (noiseless) receiver, to that of a real receiver which adds its own noise to that of the thermal noise.

As the ratio of two ratios it is independent of bandwidth, temperature, mode, S/N, and impedance. 10dB is typical NF for an HF receiver, while at VHF/UHF noise factors of 5dB or less are common.

Noise on HF

But what happens in real life? In a wideband antenna system using a 3kHz receiver bandwidth at a quiet location, thermal noise calcu-
lated for a typical system would be $-26\text{dBm}$. If the receiver has a NF of 10dB, then its noise floor will be (Fig. 1) at $26 + 10 = -16\text{dBm}$. For most HF modes (SSB, AM, CW) an S/N of 10dB is adequate. To achieve 10dB, a signal will need to be 10dB above the receiver noise floor, which in this case is at $-16 + 10 = -6\text{dBm}$, or $0.5\ AVENTF$, shown in Fig. 1 as the horizontal dashed line.

This gives the well-known relationship that an NF of 10dB is equivalent to a sensitivity of approximately $0.5\ AVENTF$ for a 10dB S/N in a 3kHz bandwidth. Sensitivity for any other bandwidth or S/N can be calculated using:

$$Sensitivity_{\text{dB}} = NF_{\text{dB}} + S/N_{\text{dB}}$$

Figure 1 also shows that the typical atmospheric noise for a quiet area at a quiet time is between 5 and 25dB above receiver noise. Under real operating conditions on HF, our receiver with its published sensitivity of $0.5\ AVENTF$ for 10dB S/N, will need a signal of between $1\ AVENTF$ (at 30MHz) and $10\ AVENTF$ (5MHz) to give a 100dB S/N ratio — and this is for a quiet atmosphere (and no QRM)!

So, for this receiver, atmospheric noise, not receiver noise, limits performance on HF. Indeed, sensitivity could be reduced to $1\ AVENTF$ (15dB NF) without loss of performance, except perhaps at 20 to 30MHz. There is little point in reducing NF below 10dB for an HF receiver using a wideband antenna — especially as sensitivity can only be obtained at the expense of dynamic effects such as intermodulation performance.

Advertised claims of $0.15\ AVENTF$ for 10dB S/N are quite impossible. Even a perfect receiver with 0dB NF needs $0.16\ AVENTF$ ($-16\text{dBm}$) to achieve 10dB S/N, due to the thermal threshold of $-26\text{dBm}$.

**VHF and above**

Above 30MHz, as frequency increases background noise, now mainly cosmic, received by the antenna continues to fall: at greater than 120MHz it drops below thermal noise with the result that at quiet locations VHF and UHF receivers can benefit from less than 10dB NF. 2-5dB or less is quite achievable using careful circuit design.

Overall NF is usually determined by the NF of the first amplifying stage in the receiver — normally an RF amplifier (but sometimes a mixer). RF amplifiers invariably use low-noise fets, and careful attention must be paid to the circuit which couples the antenna to the first stage.

“Noise matching” is sometimes used on VHF/UHF equipment where, instead of matching receiver input impedance to the antenna impedance, the two impedances are deliberately mismatched to optimise NF.

Noise is proportional to the square root of bandwidth. If bandwidth is reduced from 3kHz to 300Hz, all noise voltages (thermal, receiver, man-made, and atmospheric) drop by a factor of $\frac{\sqrt{10}}{\sqrt{30}} = 3.16$, or 10dB. So, at this bandwidth sensitivity for the 10dB NF receiver ($0.5\ AVENTF$ in 3kHz), would be $0.5 / 3.16 = 0.16\ AVENTF$ for 10dB S/N.

This explains the continuing use of CW in the HF bands as a CW signal can still be copied when SSB would be lost in the noise.

**Selectivity**

Selectivity is the ability to tune one signal while rejecting other close-in signals, usually achieved by using crystal, mechanical, or ceramic block filters. The old constraint of a low second IF no longer applies, and in fact it is easier to design crystal filter frequencies higher than 1MHz. Standard IFs have been established at 1.4, 1.6, 9.0 and 10.7MHz, although the 455kHz IF is still very common-place using ceramic filters.

Block filters are also used as “roofing filters” in the first IF of HF receivers! They are commonly in the VHF region, using 40 to 90MHz crystal filters. VHF and UHF receivers may have a first IF of many hundreds of MHz, using surface acoustic wave (SAW) filters.

Ideal filter response is a flat top with low ripple, and steep sides going down to a $-80\text{dB}$ stopband which extends a long way out.

**Image (second channel) rejection**

In the normal superhetorodyne process, a wanted signal ($f_s$) beats in the mixer with the local oscillator (or synthesiser output) frequency ($f_{LO}$). One of the resultant products of the mixing process, usually $f_{LO} - f_s$, at the intermediate frequency (IF), is passed by the IF selectivity filter.

But another frequency, the image or second channel frequency ($f_{LO} + f_s$), also beats with the local oscillator to produce a product at the IF. This frequency must be rejected by RF tuning, either ganged to the “tune” control or using a separate pre-selector control; or by switched bandpass filters, usually automatically switched on synthesised receivers. Image

![Fig. 2. Ideal filter response with a flat top and steep sides going down to $-80\text{dB}$ stopband which extends a long way out.](image)

![Fig. 3 Third order intercept gives a good indication of intermodulation, cross-modulation and blocking performance.](image)
frequency is equal to \( f_S \) plus twice the IF. So the higher the first IF, the further away from \( f_S \) will be the image frequency, and the easier it will be to reject. Up-conversion techniques on a HF receiver will put the first IF at 40-90MHz. The image frequency will also be at VHF and so can be rejected by a simple 35MHz low-pass filter at the receiver input.

Image frequency rejection is specified as the ratio in dB of an unwanted signal above \( 1\mu V_{\text{EMF}} \) to give the same output as a wanted (on-tune) \( 1\mu V_{\text{EMF}} \) signal. 60dB of rejection is a poor performance: 90dB or more is good.

**IF rejection**

Intermediate frequency, or IF, interference occurs when a strong signal at a receiver's IF directly breaks through the early receiver stages and into the IF amplifier. IF rejection is specified similarly to image rejection, with 90dB being the target.

**Internal spurious responses**

Internal spurious responses (spurii or spurs) are responses of the receiver to self-generated noises and whistles. Problems are caused when they occur at the signal frequency or an intermediate frequency.

Oscillators and mixers may act as noise generators as can digital circuitry – especially the drive lines to multiplexed displays. Other causes are power supply harmonics, parasitic oscillations in amplifiers, and even sub-harmonics of any up-conversion IFs.

Frequency synthesizers and other digital circuits produce large numbers of frequencies, and most waveforms are digital square waves with fast rise-times rich in harmonics.

Careful circuit design, with adequate low-pass and bandpass filtering, keeps spurious outputs 100dB down on the main output, ensuring that all spurious responses are no more than 3dB above the receiver noise floor in a 3kHz bandwidth.

**Stability**

Stability is the measure of frequency drift of a receiver with time and temperature. A fully synthesised receiver can have a stability approximately equal to that of its temperature controlled frequency reference source. An oven-controlled temperature-stabilised crystal oscillator can achieve a stability of less than one part in \( 10^8/\text{°C} \) (0.1Hz/°C at 10MHz).

Sometimes stability is specified as a short-term (temperature) drift plus a long-term (crystal ageing) drift. With partial synthesis the stability is normally governed by the stability of the VFO, but with cool, buffered solid-state designs short term drift (after a three hour warm-up) of 50Hz/hour is possible.

**Dynamic performance**

So far, only 'static' performance parameters have been dealt with. This section looks at dynamic performance, which relates more closely to real-world conditions.

Dynamic effects are generally caused by large off-tune signals, making the receiver operate nonlinearly.

Two unwanted signals can intermodulate to produce a product at the same frequency as the wanted signal (intermodulation); or modulation from an unwanted signal can be transferred to the required signal (cross modulation). Alternatively an unwanted signal can reduce the sensitivity of (or block) the required signal (blocking).

One problem is that activity on the bands (especially on HF and VHF) has increased to such an extent that many large off-tune signals are always present at the receiver's input stages. It is these dynamic effects rather than the traditional sensitivity/selectivity/stability parameters that largely determine performance of the communications receiver under real-life signal conditions.

**Intercept point**

Intermodulation, cross modulation, and blocking are caused by second and third order products, as the receiver responds to these at a greater rate than it responds to the fundamental signal input (Fig. 3).

Second-order products cause the output to increase as the square of the input – twice as many dB – and third-order products as the cube of the input – three times dB. Forth, fifth, and higher order intermodulation products are normally ignored as second and third order effects predominate. Arguably the single most useful performance parameter of all is the intercept point, where two extrapolated responses cross. Third-order effects are generally more significant than second-order. Figure 3 shows how the third-order response crosses the fundamental response which is extrapolated at
120dBµV or +7dBm.

Most amplitude measurements are defined using voltages (µV, mV, dBµV, etc.). But the intercept point is usually specified as a power ratio, the dBm, where a dBm is a dB relative to a power of 1mW into the receiver input impedance.

The third-order intercept is so important because it is a single number giving a good indication of the intermodulation, cross-modulation, and blocking performance. +5 to +35dBm is considered good.

Dynamic range

Dynamic range is the span of signal amplitudes – from smallest to largest – to which the receiver responds.

The “single signal” dynamic range is limited at the low end by noise, and at the upper by gain compression: amplifier outputs start hitting the supply rails and the outputs can increase no further.

Definitions of dynamic range are often limited by the variance in the situation of a large number of signals – some of which are very large in amplitude. It is the large signals that really limit the dynamic range (again due to the receiver’s nonlinearities).

Dynamic range is best described as the range of input signals over which dynamic interference effects produce non-significant outputs, at or below the noise floor. A useful working definition is that it is two-thirds of the difference in level between the noise floor and the intercept point in a 3kHz bandwidth. Or, it is the difference between the fundamental response input level and the third-order response input level as measured along the noise floor (sometimes defined as 3dB above the noise floor) in a 3kHz bandwidth, Fig. 3.

Reducing the bandwidth improves dynamic range because of the effect on noise.

Using this definition, dynamic range for the receiver depicted in Fig. 3 is 90dB, compared with more like 130dB when a single signal definition is used.

Clearly, great care must be taken in interpreting manufacturer’s figures. Using our preferred definition, a dynamic range of 90 to 110dB for 3kHz bandwidth with an intercept point of 120 to 150dBµV (or +7 to +37dBm) is good.

Intermodulation

Second-order intermodulation products are simply equal to f1 ± f2, where f1 and f2 are the two unwanted frequencies. An example, Fig. 4, is where the two unwanted signals are at 11 and 21MHz causing a beat at 10MHz. Other pairs of signals at (say) 6 and 16MHz, or 3 and 7MHz would produce a similar product at 10MHz.

For second-order intermodulation to occur, one of the signals must be far removed from the wanted signal and can easily be rejected by any reasonably tight tuning – including the passband of any octave or sub-octave block front-end filter fitted to many modern communications receivers.

Input/output isolation around these filters must be good, or second-order intermodulation can be a real problem. On some low cost general coverage HF receivers, third-order intermodulation performance is quite good, but second-order performance is poor if using a wideband antenna without an antenna tuning unit (ATU.).

Third-order intermodulation tends to be equal in frequency to 2f1 ± f2. For example, the second harmonic of a 6MHz signal (at 12MHz) beats with a 22MHz signal to produce a 10MHz third-order product at the wanted frequency (Fig. 5). Front-end tuning should easily reject both signals. But where, say, the second harmonic of a 10.4MHz signal (at 20.8MHz) intermodulates with a 10.8MHz signal to produce the 10MHz interfering signal (Fig. 6), both unwanted signals are very close to the wanted signal, and well within the rf passband regardless of RF tuning.

Third-order intermodulation is normally considered more important than second-order. This is because it cannot be rejected by front-end tuning.

Intermodulation performance (IMP) is typically specified as the levels of two unwanted signals not less than (say) 20kHz off tone to give a 0dBµV (1µVEMF) response. A good HF receiver will have a third-order intermodulation performance of 80–100dBµV. Third-order performance should be similar, but is often not stated – which can be misleading. Statistical analysis of the actual signals received over the whole HF band using wideband rhombic antennas indicates that at least 90dB of third-order intermodulation performance is required1–3. That level corresponds to 32nVEMF and at almost any time there will be tens of broadcast (and other) stations putting 10–100nVEMF onto a wideband HF antenna, with hundreds of others in the range 1–10 mVEMF.

A simple example should help put everything into perspective.

Take the 10dB NF receiver, with its noise floor at −16 dBµV for 3kHz bandwidth, and a good IMP of 90dB (indicated by the line at the 0dBµV level on Fig. 7). Third order response will have a slope three times that of the fundamental response, with its position defined by the 90dB IMP line. The intercept occurs at 135dBµV or +22dBm (50Ω) where the extrapolated responses cross. (In practice the actual responses bend over before crossing as shown due to gain compression.)

The calculated dynamic range turns out to be 100.67dB.

In-band intermodulation

In-band intermodulation, when two signals within the IF passband intermodulate to produce extra products, is normally of little significance except where multichannel “voice frequency telegraphy (VFT)” systems such as “Piccolo” are in use. It is specified as the level of an unwanted intermodulation product relative to two equal wanted in-band signals (a product of 40dB below two equal in-band signals is good).

Cross-modulation

Cross modulation occurs when modulation from a single unwanted amplitude modulated signal transfers itself across, and modulates the wanted signal (Fig. 8). Non-linearities in the early receiver stages are the cause, and sometimes the same modulation may reappear on each adjacent signal tuned in. The parameter may be specified as the level required, in dBµV, for a 30% modulated car-
Linearity of bipolar transistors in rf amplifiers and mixers is not good. But fets are better for a VHF or UHF receiver.

Fig. 8. Cross modulation where a single unwanted amplitude-modulated signal transfers itself across and modulates the wanted signal.

As cross-modulation is a third-order effect, good third-order intermodulation performance will tend to mean good cross modulation performance. The level of an interfering signal will normally have to be higher than for intermodulation. The signal will be within the front-end tuning bandwidth of the receiver, so will typically be in the same or adjacent broadcast band to the band being received. 100-120dBµV is good.

Blocking
De-sensitising, or blocking, occurs when the large off-tune interfering signal causes a reduction in wanted signal output, through a product generated by the non-linearities of the receiver front-end.

It is specified as the level of an unwanted signal, removed from the wanted channel by at least (say) 20kHz, required to reduce a wanted output by 3dB. Blocking can often be caused by a strong CW signal, causing gain to go up and down with the keying. 90-110dBµV for a 3dB reduction is good, for a wanted 1mV_{EP} signal.

A value of at least 20kHz is specified for this and other dynamic performance parameters, to ensure that the unwanted signal will be outside the passband of the receiver IF stages. While it is suitable for a HF receiver with a good roofing filter (which might have a noise bandwidth of 12kHz or so), 50kHz might be a better figure for a VHF or UHF receiver.

Causes and cures of non-linearity effects
The only really effective solution to improving linearity is to design oscillators with very good linearity. A value of at least 20kHz is specified for reciprocal mixing, a considerable loss of performance in a "real life" band full of signals. As can be seen, it is the stopband of the filter response that has been changed, and with 50dB of reciprocal mixing, a considerable loss of performance occurs. Improving it to 70dB considerably reduces its effect on filter response.

Reciprocal mixing
Reciprocal mixing is due to high levels of unwanted signals mixing with the noise sidebands of the local oscillator/synchroniser, producing unwanted products at the wanted frequency (Fig. 9). It is specified as the dB of any unwanted signal at (say) 20kHz off-tune, above a wanted signal, to produce a noise product 20dB down on the wanted signal level, in a specified bandwidth (3kHz).

The unwanted signal, fairly close to the wanted signal, cannot be rejected by front-end filtering, and as it is not caused by front-end non-linearity, the above cures are no use. The only solution is to design oscillators with very low noise outputs, especially close-in phase noise, by employing high "Q" in the oscillator circuit, and also by using high powers in the oscillator to improve S/N.

Phase locked loops (PLLs) in frequency synthesisers can be very poor in this respect, especially single-loop designs which have low loop gain resulting in high levels of noise. Also PLL's frequently use low Q and low power VCOs in the output.

The noise produced is phase modulated and cannot be removed by limiting. Good design can produce a frequency synthesiser output noise of 90-100dBc (referenced to the carrier output), and a good fet crystal oscillator can give 110dB, ensuring a reciprocal mixing performance of 70dB.

Sometimes reciprocal mixing is specified as a 3dB reduction of snad of the wanted signal, rather than a product 20dB down on the wanted signal. In this case the figure will look almost 20dB better, at around 90dB.

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Demand for economical ways of making switch-mode supplies and electronic ballasts exhibit a unity power factor is growing. Having a non-unity power factor introduces harmonic distortion on the mains—a nuisance that electricity suppliers are becoming increasingly concerned about.

Designed for minimal component count, the new MC34262 forms the heart of a preconverter that sits between the mains supply and a switch-mode supply or ballast, Fig. 1. In the circuit configurations outlined in the preliminary data sheet, the IC has the ability to bring the power factor up to between 0.989 and 0.999. Switch-mode supplies typically exhibit power factors of 0.5 to 0.7.

Most electronic ballasts and switch-mode power supplies incorporate a bridge rectifier and reservoir capacitor directly connected to the mains. This provides raw DC to drive the main power converter circuitry.

A simple rectifier only draws current at the peaks of the mains sinusoid, where the voltage at the input exceeds the voltage over the capacitor. As a result, the current waveform comprises spikes which are rich in harmonics, Fig. 1.

Power factor correctors can be passive or active. Passive types usually contain a combination of large capacitors, inductors and rectifiers. Active types incorporate some form of high-frequency switching converter for the power processing. This is usually a boost converter configuration of the type shown in Fig. 2.

Since active circuits operate at much higher frequencies than their passive counterparts, they are much smaller, lighter and more efficient. With proper control of the preconverter, almost any complex load can be made to appear resistive to the mains. Figure 3 shows a complete 175W converter circuit. This is one of three in the note, the remaining two being similar but designed for 80W and 450W. The circuit is a peak detecting boost converter configured in current mode. It operates in critical conduction mode with a fixed on time and variable off time, Fig. 4.

A major benefit of critical conduction mode is that the current loop is inherently stable which eliminates the need for ramp compensation. This circuit operates over a wide input range of 90 to 268V AC without adjustment.

Built into the MC34262 is an overvoltage comparator to stop output voltage rising too high if the load is removed. There is also a undervoltage lock-out, maximum peak switching current limitation and a pulse metering latch. Output clamping prevents damage to the mosfet gate.

Motorola Ltd, European Literature Centre, 88 Tanners Drive, Blakelands, Milton Keynes MK14 5BP. Telephone 0628 585000.

Fig. 1. In switch-mode power supplies, straight forward mains rectifiers only draw current when input voltage rises above voltage over the reservoir capacitor. This introduces unwanted harmonics into the mains supply.

Fig. 2. Active power factor controllers for switch-mode power supplies and electronic ballasts sit between the mains rectifier and storage capacitor. Switching at high frequency, they share the current loading on the mains over the full cycle, resulting in desirable unity power factor.
This data was taken with the test set-up shown in Figure 24.

This data was taken with the test set-up shown in Figure 24.

**Power Factor Controller Test Data**

<table>
<thead>
<tr>
<th>Vrms</th>
<th>Pin</th>
<th>PF</th>
<th>Ifund</th>
<th>Current Harmonic Distortion (% Ifund)</th>
<th>DC Output</th>
</tr>
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<tbody>
<tr>
<td>90</td>
<td>193.3</td>
<td>0.991</td>
<td>2.15</td>
<td>THD 2 3 5 7</td>
<td>VO(p-p) VO lO PO n(%)</td>
</tr>
<tr>
<td>120</td>
<td>190.1</td>
<td>0.998</td>
<td>1.59</td>
<td>2.8 0.18 2.6 0.55 1.0</td>
<td>3.3 402.1 0.44 176.9 91.5</td>
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<tr>
<td>138</td>
<td>188.2</td>
<td>0.999</td>
<td>1.36</td>
<td>1.6 0.12 1.4 0.23 0.72</td>
<td>3.3 402.1 0.44 176.9 93.1</td>
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<tr>
<td>180</td>
<td>184.9</td>
<td>0.998</td>
<td>1.03</td>
<td>1.2 0.12 1.3 0.65 0.80</td>
<td>3.3 402.1 0.44 176.9 94.0</td>
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<tr>
<td>240</td>
<td>182.0</td>
<td>0.993</td>
<td>0.76</td>
<td>1.2 0.10 2.3 2.9 0.46</td>
<td>3.4 402.1 0.44 176.9 95.7</td>
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<tr>
<td>268</td>
<td>180.9</td>
<td>0.999</td>
<td>0.69</td>
<td>1.0 0.10 2.3 2.9 0.46</td>
<td>3.4 402.1 0.44 176.9 97.2</td>
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This data was taken with the test set-up shown in Figure 24.

**Fig. 3.** At 240V input, this universal input circuit brings power factor of a switch-mode PSU up to 0.993 from typically 0.5 to 0.7. It delivers up to 175W.

**Fig. 4.** This diagram shows inductor current and MOSFET gate voltage waveforms. It illustrate how the power factor corrector circuit of Fig. 3 spreads loading over the full mains cycle to obtain an almost unity power factor.
Switching regulator

Despite its very low component count, this switching regulator is around 85% efficient given 0.5A loading and a 10V supply.

Designed primarily for step-down applications, the LT1176 can also be used as a positive-to-negative power converter or in flyback mode. It has a true analogue multiplier in its feedback loop, making its responses to changes in input voltage levels nearly instantaneous.

Output current is up to 0.8A and quiescent current is just 8mA. Pulse by pulse current limiting at 1.7A is built in, as is a 100kHz oscillator. When configured as shown, the input voltage range is from 8 to 35V. In inverting and boost configurations, a self-boost facility built in to the IC allows input voltages as low as 5V.

Used as a buck converter, the IC has an output voltage range of 2.5 To 30V. Note that there are two versions of the IC, one with a fixed 5V output, the other adjustable.

Linear Technology, 111 Windmill Road, Sunbury-on-Thames, Middlesex TW16 7EF. Telephone 0932 765688.

Basic 5V Positive Buck Converter

5V Buck Converter Efficiency

PABX chip handles two trunks with twelve extensions

All telephone transmission, reception, and call-progress circuits for mixing voice and control signals are contained in a new highly integrated chip from Sierra. This chip forms the heart of a PABX capable of handling up to five external lines and twelve extensions.

A complete evaluation system for this private automatic branch exchange IC is detailed in the SC1139/391 integrated telephone systems hardware design manual. Software is also available and the manual includes PCB details.

Key elements of the chip are two matrices, one 20 by 23 and the second 4 by 4. There are also two DTMF transmitters, two DTMF receivers, a ring generator and programmable call progress monitors. Additionally, the device can handle conference calls, differentiate between fax and voice and connect to tape or RAM for recording speech. Besides switching between the various lines, the matrices connect various control devices. These include programmable gain circuits, the DTMF transmitters and receivers, call progress monitors, voice detectors and programmable bandpass filters.

Since the circuit diagrams run to fourteen A4 pages, there is only enough room to publish the block diagram.

Sierra Semiconductor, Terminal 3, 3B2 Stonehill Green, Westlea, Swindon, Wiltshire SN5 7HB. Tel. 0793 618492.

RING CPD1-CPD2 ER1-ER12 ET1-ET12 TR1-TR2 TT1-TT2

This PABX on a chip handles up to five external lines and 12 extensions. Besides switching it also incorporates a multitude of other features like DTMF transceivers, call-progress monitors, fax detection and digital gain.
Comprehensive information on driving fluorescent backlighting for LCDs is presented in Techniques for 92% efficient LCD illumination from Linear Technology. Since backlighting can be responsible for as much as 80% of battery drain, drive circuit efficiency is very important.

Cold-cathode fluorescent lamps present a complex load. Power conversion efficiency is affected by the lamp’s current, temperature, dimensions, gas constituents and proximity to nearby conductors. Drive waveform characteristics also play a role.

As the curves shown imply, predicting lamp behaviour under various operating conditions is difficult. Maximum electrical efficiency does not necessarily correspond to the best optical efficiency. It is possible to build a 94% electrically efficient circuit that produces less light output than one with only 80% efficiency. For this reason, electrical and photometric evaluation of a circuit is advisable. Methods for both are covered in the booklet.

Other factors greatly affecting efficiency are lossy display enclosures and excessively long connecting wires. Display enclosures with too much conducting material near the lamp can have huge losses due to capacitive coupling. Poorly designed enclosures can easily account for 20% efficiency degradation while high-voltage wire runs typically cause a fall of 1% per inch.

Cold-cathode fluorescent lamps represent a complex load. The voltage needed to force them into conduction, around kV, is significantly higher than their operating voltage which is typically 300 to 400V. Until their firing voltage is reached, fluorescent lamps exhibit a very high resistance but after firing, their resistance falls considerably. To compound the problem, the resistance transition is fast.

Due to the combined effects of the cold-cathode fluorescent lamp’s resistance characteristics and the frequency compensation problems associated with switching regulators, severe loop instabilities can arise. These are a particular nuisance at start-up. Once the lamp is on, it assumes a linear load characteristic, easing stability criteria.

Although fluorescent lamps can be powered from DC, it is inadvisable to do so since migration inside the lamp will quickly damage it. Typically, lamp operating frequencies are 20 to 100kHz. A sinusoidal drive waveform is preferred since it minimises RF emissions while maximising efficiency.

The design shown here is one of many solutions described and offers a 92% efficient supply for 10mA loads. With this particular circuit, drive is provided for two lamps—a typical requirement for current LCD laptop colour displays. Other features are dimming and remote shutdown which are essential for minimising battery power consumption.

Further information in the note deals with LCD biasing, low-power cold-cathode fluorescent lamps, and feedback stability. There are full chapters on mechanical design considerations, efficiency measurements and power saving techniques. There is also a well-supported section challenging a number of existing lamp driver circuits.

Linear Technology, Colseum Business Centre, Riverside Way, Camberley, Surrey GU15 3YJ. Tel. 0276 677676.
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Fast, 500V mosfet. With switching times of 5ns and a 500V breakdown voltage, Harris’s RFY10N55BE mosfet handles 10A and switches eight times faster than comparable devices, in which a 40ns fall time has been the fastest. The package contains the high-voltage mosfet, a control mosfet, a separate source Kelvin terminal and protective zeners. On resistance is 0.48Ω and input capacitance 3800pF. Harris Semiconductors (UK). 0276 686886.

Green/yellow led. Producing a greenish-yellow light, HP’s HLMA-C001000mcd led has an 8° viewing angle at 20mA. The company has, with this addition to the range of high-brightness devices, all three of the popular colours for indicators, all being suitable for outdoor use. Hewlett-Packard Ltd. 0344 362277.

Blue leds. Silicon carbide leds by IMO generate true blue light peaking at 470nm. They are available in clear or diffused 3mm or 5mm packages with viewing angles of 16° and 28° in the clear versions and 34° and 42° in the diffused type. Also announced are 3mm GaAlAs and GaP leds emitting red or green light at sufficient brightness for outdoor use: IMO Precision Controls Ltd 0391 452 6444.

Small, 60V mosfets. Three devices, the first in the Siliconix Little Foot family of surface-mounted power mosfet, are on release. All rated at 60V, the single p-channel S9404DY and the dual n-channel S9940DY and the S99480DY dual p-channel offer 100mA and 250mA on resistance and are designed for 4.5V gate drive. Siliconix. 0344 485757.

P-channel IGBT, Zetex’s ZCN0545 n-channel insulated gate bipolar transistor now has a p-channel stablemate – the ZCP0545A, in a TO-220 package. Both are 450V devices and have turn-on and turn-off times of 150ns and 350ns, handle a continuous 0.37A and have an input capacitance of 120pF. Gate-source threshold is 3.5V and drain-source saturation is 0V at 0.5A, with 60Ω on resistance, Zetex plc, 061-627 5105.

3-state op-amp, TI claims its TL02301 to be the first wide-band op-amp in a single package to have a three-state output. It will sink and source 1A and has a gainbandwidth of 8MHz. THD is 0.04%. Texas Instruments. 0294 225252.

Voltage references. Five IC precision references in the Zetex ZRT series cover the 2.5-9.8V range, producing only 50µV of output noise and with a temperature coefficient of 15ppm/°C. Current handling of the 5V device is 0.15-60mA and there is a pin for output trimming by an external potentiometer. Zetex plc. 061-627 5105.

November 1993 ELECTRONICS WORLD + WIRELESS WORLD
3.2ns logic: IDT’s E Speed double-density logic devices offer propagation delays of 3.2ns and use less power than any other logic family. IDT’FCTI8XX/7XX devices have high current output and the IDT’FCTI6XX/3XX family uses the 4Mb video RAMs. Toshiba’s range of Memory chips is the 28-pin wide-body SOIC for the containing multiple drivers and receivers and forming a one-chip type EIA232 serial interface. Dual chips. Features and performance of two synchronous first-in-first-out registers are contained in one 20ns 4K by 9 by 2 IDT2341, the first member of IDT’s double-wide 9-bit wide dual SyncFIFOs, available in 64-pin thin quad flat packs. Integrated Device Technology, 0372 363734.

Single-chip EIA-232, 875LSBC187 and 241 by T1 support the 9-pin D-type EIA232 serial interface, containing multiple drivers and receivers and forming a one-chip solution. The 187 supports data rates beyond 116kbit/s and both devices have internal charge pumps and a shutdown function to 10μA. Packaging is the 24-pin wide body SOIC for the 241 and 28-pin SSO for the 187. Texas Instruments, 0234 235525.

Memory chips

4Mb video RAMs. Toshiba’s range of video RAMs is augmented by the 162/202/165/265SF/FT/FR V6-organized memories. Access times are 60ns at 5V or 80ns at 3.3V. By using the pnp-lined fast page mode, cycle times can be reduced from 115ns to 40ns. A 512 by 16 serial memory is included. 2Mb types are also offered. Toshiba Electronics (UK) Ltd, 0276 694500.

Mixed-signal ICs

MPU supervisors. AD’s 4DM69X series monitor microprocessor power supplies and take necessary action when they drop below specified levels. Pin-compatible chips are available, but these use 80% less power at 5V and give 100mA output current, in addition to a 5ns chip-enable propagation delay and 50ns supply-to-reset response. Functions include backup battery switching, watchdog timing, and error protection and power failure alert. Analog Devices Ltd, 0592 253320.

Oscillators

SM clock oscillator. AVX’s K50 series of ceramic packaged, surface-mounted clock oscillators are claimed to be the world’s smallest at 7 by 5 by 1.8mm and come in crystal, TTL and 3.3V versions. These tri-state devices cover the 1.5-50MHz range with stabilities of 50-100ppm. Supply current at 50MHz is between 30 and 40mA, depending on model. AVX Ltd, 0252 363668.

S-band VCO. In the range 2.6-3GHz, the C-010 voltage-controlled oscillator by Z-Comm offers a 400MHz bandwidth for a 0-12V tuning voltage, with 90% linearity. An output of 15dBm/2dBm into 50Ω suits low-loss mixers and phase noise is -55dBc at 100kHz. Eurocircuits Ltd, 0153 977 1105.

Clock oscillators. ICOS’s clock oscillators are now specified at 25°, rather than an overall frequency tolerance quoted between 0 and 70°C. Adjustment can be as close as ±5ppm for 3V and 5V types at frequencies in the 250kHz-70MHz range (3V types from 4MHz). ICOS Ltd, 0406 77155.

Programmable logic arrays

FPGAs. Actel’s ACT 2 family of field-programmable gate arrays now costs less and performs better, after a process shrink from 2.5μm to 1μm resulted in a 25% speed improvement. As an example, the A1225A 2.25MHz reaches data-path speeds of 10MHz, 6MHz in a 16-bit counter system speed of 50MHz. Actel Europe Ltd, 0256 29209.

Fast 84-pin EPLD. Latest member of Altera’s MAX7000 family of erasable programmable logic devices is the 64-macrocell EPM7064, which offers 7.5ns single-level logic delays and 125MHz-in-system performance. It is supported by the MAX+PLUS II development software for PCs. Altera UK Ltd, 0628 488811.

APLA. Intel’s iF7X870 field-programmable gate array is the first in the company’s FLEX/Logic family and incorporates flexible memory and logic blocks that are easy to use as a conventional PLD. Eight macrocells are organised as eight independently configurable function blocks, internal logic carrying over configuration. Pin-to-pin delays are 10ns and there are 12 clocking options. So of each block is independently operable at either 3.3V or 5V. Jerryn Distribution, 0732 743743.

Fastest 28-pin PLD. Latice Semiconductor’s QAL 26CV12C is claimed to be the fastest 28-pin PLD available at clock frequency of 142MHz. It takes a typical 10mA supply current and provides 1.2 times the logic density of the standard QAL 22/20 being contained in either 28-pin dip or PLCC packages with center-pin supply and ground. Micro Call Ltd, 0844 261939.

Power semiconductors

Step-down switcher. Maxim’s MAX7298 is a 5V, 3.3V and 3.3V DC-DC switching regulators working from 8-40V input and rated at 2A. An on-chip oscillator removes the need for a large number of external components. Cycle-by-cycle current limiting protects against overcurrent and output shorts and there is micropower shutdown and adjustable current limiting. Maxim Integrated Products Ltd, 0734 845255.

Micropower LDO regulator. National says its LP3956 is the first dual, micropower, low dropout regulator, with 470mA dropout, 170μA quiescent current and 250mA output and provided with shutdown pin, error flag pin, auxiliary comparator and an additional 75mA regulator to ensure data retention during system shutdown. LP3957 is a fixed 5V, 250mA LDO regulator in a TO-220 package for higher power. National Semiconductor, 0793 697592.

IGBTs. A new silicon structure developed by Toshiba is used in the MG300/180V2Y/S40 and MG340/360V1US47 insulated-gate bipolar power transistors to provide operating voltages of 1700V up to 360A. The 30, 90 and 180A types are dual half bridges and the 240A and 360A versions single IGBTs. These devices hard switch at up to 20kHz. Saturation voltage is 3.2V. Toshiba Electronics (UK) Ltd, 0276 694600.

Passive components

New capacitors. National packages for Kyocera’s ceramics designed for use in high-moisture power supplies are in radial, four-terminal and dual-in-line form in both through-hole and SMT types. Finish is dipped lacquered, back-fill boxed or uncoated. Other types such as screw fixing being available to order. AVX Ltd, 0252 336868.

Thick-film resistors. When high-voltage transients occur, as in inductive switching, laser trimming across the resistor body can cause localised hot spots and cracking. Murata’s new components are trimmed longitunally, leaving no weak points and achieving a tolerance of ±0.2%. Components are made to customers’ requirements. Murata Electronics (UK) Ltd, 0252 811666.

Chip coil. LQ221A ultra-miniature chip coils by Murata are made in thick-film form to obtain a ±5% tolerance and low stray capacitance. Self-resonant frequency is over 2GHz at 8A, minimum Q is 10 at 500MHz. Resistance is between 12 and 24Ω, depending on value and maximum current of 250mA. Package size is 2 by 0.5mm, surface mounted. Murata Electronics (UK) Ltd, 0252 811666.

8.3F backup capacitor. NEC’s SuperCaps are extremely high-value capacitors intended to replace batteries in backing up circuitry. Values are as high as 3.3F and a 256-bit ram, for example, can be supported for 50 hours by a 2.2F SuperCap. Reliability is ensured by the method of charge storage – at the interface between activated carbon and sulphuric acid – and NEC claim that there is no limit to the number of allowable charge/discharge cycles. NEC Electronics (UK) Ltd, 0908 691133.

Crystals. Micro-Crystal oscillators are made by means of an advanced photolithographic technique, which results in increased resistance to shock and vibration and confers low ageing characteristics. Over-controlled, voltage-controlled and standard clock oscillators are offered in the range 100kHz-50MHz, depending on model, and the oscillators are contained in all ceramic packages. The company offers a custom design service. Stanton Components Ltd, 0376 340902.
Line-match transformers. MTLM-1200 series line-matching transformers from microSpire feature a return loss specification that exceeds BS415, 624 and 6301 and are approved to B&BT EN41003. Transformer return loss is 16dB or better over 0.2-4kHz (24dB in network) and 26dB over 0.2-3kHz. Distortion is 0.1% or better. At DC dielectric strength in 1mm tests is 7kV - 4kV RMS. As standard, impedance is 600Ω, but others are available. SUtech Interconnection Ltd. 0256 51221.

EMI filters. The smallest member of TDK's ACR range of compact, surface-mounted, interference-suppression filters measures only 1.6 by 0.8mm and provides 120uA impedance at 100MHz. Other models in the range exhibit 40-600Ω at 100MHz. Resistance of 3-1.3Ω and current ratings of 0.1-0.5A enable their use as signal-line suppressors. TDK UK Ltd. 0737 772323.

EMC protection. Field-by-Telematic combines RFi filtering, surge and ring suppression, which eliminates ringing caused by surges and transients. Hitachi Denshi's V-860 60MHz cursor-readout real-time oscilloscope has three channels: six traces and delayed sweep and cost £750. Setting values are displayed on-screen and the cursors provide direct readout of voltage, time and frequency. Maximum sweep speed is 5ms/div. and Y sensitivity is 100MHz/div. Trigger hold-off is provided, as is a hybrid separator. Hitachi Denshi (UK) Ltd. 081 202 4311.

Current-sensing shunts. Four terminal current-sensing shunts in the PLC range by Kyoritsu covers the 0.005-100Ω range with 0.05% tolerance at 25°C. Typical component is 0.1Ω±1% at 10W carrying 30A; change resistance by less than 0.1%, with 10 measurable EMF change between the copper terminals. Kyoritsu Engineering Co. Ltd. 071 405 6060.

Oscillographic recorder. Marston's ORP1200 recorder is the first of a range designed to use thermal paper rather than the more expensive ultraviolet-sensitive type, producing A4 or A3 output. ORP1200 offers 100k samples sampling, 14-bit resolution and a range of recording display and memory functions. It is available with four or eight channels, with a high-voltage AC module and a high-sensitivity 14-bit input module with signal conditioning, an additional option being the recording of 16 channels of logic alongside the analogue traces. Marston Instruments Ltd. 0494 435000.

Power supplies

Low-noise PSUs. Gresham's GSM 392 and 393 miniature power supplies use linear techniques rather than switched-mode methods to achieve a 1mV RMS output noise. Three outputs are 5V - 1A. -12V-150mA and 5V-1A and ±15V-15mA, with stabilisation of 0.05% and regulation 0.2%, for a full-load change. Chassis or PCB-mounted versions are available and solder-pin spacing is to DCS or European or US standards. Gresham Power Electronics Ltd. 0722 430600.

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PSU chips. Voltage detectors and voltage regulators used in Seiko's watches are now offered to the industrial market. In the SOT86 package (4.5 by 4.25mm footprint) the SCI 7700 diodes cover 0.9V to 5.3V at a quiescent current of 1μA, while the SCI 7710 regulators produce ±5V to ±5V at a similar quiescent current on outputs up to 15V. A free copy of Seiko's catalogue is on offer. Hero Electronics Ltd. 0525 953615.
Quadrate hybrids. DOP series quadrate hybrids from Synergy Microwave cover 10-500MHz with 5 1 bandwidths, offering 1dB insertion loss in the 5 1 band with an amplitude unbalance of 0.8dB. Phase balance is 4°, isolation 20dB and VSWR 1.5:1 on all ports. Chronos Technology Ltd. 0998 85471.

Discoidal filters. Oxley's dE27 range of discoidal feedthrough filters provide up to 650dB of loss at 10GHz in a 50Ω system, without resonances. They fit a 3.50inch hole, are solder mounted and are hermetically or epoxy sealed. Voltage handling is 200V DC up to 85°C, derating to 100V up to 125°C. Values are 10pF-5nF. Oxley Developments Co. Ltd. 0229 52621.

Switches and relays
Solid-state relays. C P Clare has released the 140 Series of solid-state relays, which are in 1 Form A and 2 Form A, handling 400V load (DC or AC peak), 250mA local current and having an on resistance of 6Ω. Switching speed is 1ms at 5mA drive current and the units are in 6-pin and 8-pin dips. C P Clare Corporation. 0460 41717.

Transducers and sensors
Digital pots. Control Transducers's 500 Series of Digipots now includes models providing 540, 1000 and 1024 lines per revolution. These devices allow users to program a range of converters so that convert rotary movement to digital form for input to counters or controllers, working continuously at up to 10,000rev/min, if necessary. Output is two-channel quadrature at TTL levels. Control Transducers, 0234 217704.

Tilt sensor. Dual sensitivity in the Cine angle transducer, selected by jumper, transforms the normal sensitivity of ±45° to ±10° when sensitivity is increased from -60°V to ±200mV. Two versions offer plus and minus analogue output or analogue ratiometric output. Accuracy is ±0.1% up to 10° and about 1% of reading at ±45°, with a 300ms time constant and frequency response of 0.5Hz. Kynmore Engineering Co. Ltd. 071 405 6060.

Software
FPGA synthesis. Actel's Designer field-programmable gate array software is now offered with the Integra Synthesis Software. ACTMap FPGA fitter, which provides a simple route from PALs to FPGAs. ACTMap converts Palasm or EDIF output into binary decision diagrams which are then decomposed into BDD representation of Actel's logic

Connectors and cabling
Optical-fibre connectors. Quick Shot ST compatible tamped-bayonet connectors by ITT Cannon offer fast, simple and safe termination of the fibre. A special holder eliminates the danger of burnt fingers, a stripped fibre being placed in the holder, which has temperature indicators, the whole going into an oven. When the epoxy is molten, the holder is taken out of the oven, a stripped fibre inserted and the assembly left to cool. The use of blue epoxy allows quick, one-stage polishing. ITT Cannon, 0256 473171.

Data loggers. An entirely new style of data logger, the S-PCX and associated equipment, is announced by Laplace Instruments. Two types of logger have eight analogue inputs, with an external battery pack, optional card reader and 512Kbyte memory cards. Both are programmed and interrogated from a PC via the software provided. Any combination of 5, 10 or 20mA, thermistor, 1, 10 and 100mV and thermocouple can be handled, depending on model, with resolutions of 1 part in 1000 to an accuracy within ±1%. Laplace Instruments Ltd. 0692 500777.

Flat NiCd cells. Energy density of Saft Nife's flat prismatic nickel-cadmium cells is now increased by at least 5% to give over 30% better than cylindrical types. With 1.2V nominal voltage, the smallest GP4 type now has 350mAh rated capacity and measures 47.5mm by 16.4mm by 5.6mm. The cells are now more freely available in bandwidths from 0.5MHz to 1000MHz, with 0.7dB typical frequency response of 0.5Hz.

Radio communications products
SM power dividers. Leaded, surface-mounted two-, three-, and four-way power dividers by Synergy Microwave are available in bandwidths from 2MHz to 1000MHz with 0.7dB typical insertion loss above the theoretical split loss. The SLD series has amplitude unbalance of 0.4dB, phase unbalance of 3° and isolation of 15- 25dB between outputs. SLO devices offer 3-1900MHz bandwidth with 0.26dB insertion loss and better amplitude and phase balance. Chronos Technology Ltd. 0998 85471.

Computer
Development and evaluation
HPVEE for Windows, H-P's Visual Engineering Environment, originally a Unix application, now runs under Windows for PCs. HPVEE is a programming environment that allows users to create test programs by clicking connections with a mouse to give a speed increase over text entry as in automatic place-and-route software. Updates of Designer and its Windows version carry no additional charge. Actel Europe Ltd. 0256 25259.

Logic compiler. Stag claims to supply the world's fastest and friendliest logic compiler - CUPL for Windows, which is an FPGA and PLD language supporting combinations of state machine, truth table and Boolean entry methods. There are four different minimisers at varying levels, including Quine-McCluskey, and polarity optimisation. Output is in several formats, including Open PLA, Palasm and XNF for Xilinx. Stag Programmers Ltd. 0707 332148.
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Versatile twin amplifier has many uses

Combining a current-feedback amplifier in the same package as a transconductance amplifier produces a versatile building block, as Ian Hickman explains.

There are many dual op-amps available, but the subject of this design brief is not a dual, but rather a twin amplifier. The eight-pin LT1228 from Linear Technology contains an operational transconductance amplifier (OTA) with a maximum bandwidth of 75MHz. Its second element is a useful current feedback amplifier, or CFA, with a bandwidth of 100MHz.

Single-ended current output of the transconductance amplifier is tied internally to the non-inverting input of the current-feedback amplifier, which can act as a buffer. This junction is also brought out to a pin. Since the non-inverting input resistance of the CFA is very high, the transconductance amplifier is effectively isolated from the CFA.

Figure 1a. Electronic gain control is an ideal application for operational transconductance amplifiers. This design has a bandwidth of around 20MHz and is adjustable from -18 to +2dB. Curves in (b) show frequency characteristics for three CFA gains. Bandwidth of the OTA section is presented in (c), THD versus input level is illustrated in (c)ii and small—signal control—path bandwidth versus I_set is shown in (c)iii.
One of the more obvious applications for an OTA is as an electronically-controlled variable gain stage. Figure 1a shows such a circuit with an input resistance of 10kΩ, a gain range of -18 to +2dB and a -3dB bandwidth of around 20MHz. Its input may be differential as shown, or unbalanced, inverting or non-inverting, in which case R1A or R2A respectively may be omitted. Gain is directly proportional to Iset, the current into pin 5 of the device. Compensation for two internal diode drops in the gain setting section is provided by the Thevenin source arrangement, R1 and R6. Assuming stabilised 15V rails, this arrangement ensures that any set gain remains constant within 1% over the device’s full temperature range of -55 to +125°C. Resistor values need changing if a different negative supply rail voltage is used. If the negative rail is not stabilised, compensation may be achieved via an LT1004 supply rail voltage is used. If the negative rail is not stabilised within 1%, this arrangement ensures that any set gain remains constant within 1% over the device’s full temperature range of -55 to +125°C.

If maximum expected input is less than 10V pk-pk, the 10kΩ resistors at the input may be reduced, giving an increased gain. If an increase in A1 is not needed, R2 may be increased. This demands less gain from the CFA and increases the circuit’s bandwidth. However, any substantial increase in bandwidth may be limited by the bandwidth of the transconductance amplifier section, which is shown in Fig. 1c. The gain A1 in Fig. 1a is given by

\[ A_1 = R_2 (R_2 + R_{1A}) A \times 10 \times I_{set} \times R_1 (R_1 + R_2) / R_2 \]

If total harmonic distortion of the transconductance amplifier as a function of input signal amplitude is shown in Fig. 1c ii, in the application in Fig. 1a, I_{set} is basically a direct current whose value is adjustable for any desired gain. In some applications, such as Fig. 6, high-frequency signals may be inserted in the control path input at pin 5. Figure 1c iii shows the small signal control path bandwidth versus I_{set}.

Electronically tunable filters
Another major application for transconductance amplifiers is electronically tuned filters. A single-pole filter is the simplest possible type, offering a flat pass-band with a -6dB/octave roll-off in the stop-band. Such a filter can be electronically controlled over a wide range, as Fig. 2 illustrates.

For operation as a low-pass filter the high-pass input should be grounded, and vice versa for high-pass. With the two inputs tied together, an all-pass filter response is obtained.
In the all-pass filter based oscillator, (a), the 0.6V Vbe of Tr1 stabilises amplitude at 1.2V pk-pk. It does this by robbing Iset from IC3 until the loop gain just equals unity. Curve (b) shows open loop gain and phase as Bode and vector plots while (c) gives output waveforms of IC1 and IC3. Scales are horizontal 125ns/div vertical and 500mV/div. In (d), output spectrum from IC2 shows second harmonic content 38dB below the fundamental 2MHz output. All other harmonics are greater than 40dB down. Scales horizontal 2MHz/div-vertical 10dB/div.

adjusting the current I_set into pin 5.

If the low-pass input is grounded instead, a high-pass response is obtained, with the same -3dB corner frequency and unity inverting gain in the pass band. With the two inputs tied together, an all-pass response is obtained. This is as predicted by the Theorem of Superposition, passing from zero phase shift at 0Hz through 90° at the corner frequency to 180° at high frequencies.

Two LT1228s can be configured to give electronically tunable versions of any of the standard second order filter sections. Part of the data is the ingenious circuit shown in Fig. 3, which accepts inputs up to 3V peak to peak.

Unlike circuits designed with conventional integrators, this version of the state-variable filter does not need a third inverting op-amp. This is because the OTA integrators have both inverting and non-inverting inputs available. If one were used, then a high-pass output would also be available. The circuit provides the novel feature of logarithmic tuning sensitivity. As a result, it could be turned into a logarithmic sweep generator. To do this, the value of the damping resistor R_d would have to be raised and antiparallel diodes connected in series with it. Oscillation would also need to be ensured by including negative damping to the non-inverting input, pin 3, of the upper OTA.

Oscillators

All-pass circuits can also be configured as oscillators. The first such example probably predates WWII and several such designs having appeared in this journal. One of these was a very low distortion audio oscillator covering 20Hz to 20kHz and using an ingenious distortion out-phasing scheme.

Figure 4a shows the circuit of an all-pass oscillator I have experimented with. Since both of the all-pass stages are non-inverting at dc, a third LT1228 was added to give the necessary inversion. This addition permits overall negative feedback and hence stability at 0Hz. It also stabilises oscillation amplitude. Figure 4b shows the gain and phase of the circuit with the loop broken.
but with $I_{in}$ applied to pin 5 of IC3 equal to what it is when the loop is closed.

At the corner frequency of the two all-pass stages, each contributes 90° phase shift, giving a total loop gain of exactly unity, non-inverting, and hence stable oscillation. This occurs at a level which just turns on $Tr_1$ on positive-going peaks, reducing the $I_{in}$ available to IC3 as necessary.

Figure 4c shows output waveforms of IC3 (leading trace) and IC1 with tuning control RV1 set for a 2MHz output. Low distortion and accurate quadrature are both evident. The circuit operates from well below 1MHz to beyond 5MHz. By 5MHz the quadrature phasing is less than 90°, due to the onset of additional loop phase shift in the inverting stage IC3.

Beyond about 7MHz, the quadrature phasing becomes so marked that the circuit switches to a different mode of oscillation. There is around 60° of phase shift in each of the three stages and operation in this mode continues to 25MHz or more. Figure 4d shows the output spectrum of IC3 at 2MHz (horizontal division=2MHz, start = 0Hz). At 1MHz and below all harmonics are more than 40dB down.

The OTA is versatile. Among other things, it allows an electronically-controlled resistor to be simulated by grounding its non-inverting input and connecting its inverting input to its output. If the output is taken positive relative to ground, the OTA will sink current, or source if taken negative, just as a resistor would.

Figure 5a shows this arrangement used as part of a spot frequency Wien Bridge oscillator operating from a single supply. The OTA acts as an attenuator to stabilise the oscillator's output amplitude.

To avoid distortion due to overdrive, the gain of 34 supplied by the CFA keeps the swing at the input to the OTA down to 15mV. This precaution is necessary since for lowest distortion the LT1228, like all OTAs, can only accept a limited input swing.

Total harmonic distortion reaches 0.2% at 30mV rms input. An OTA's permissible input voltage swing is limited. This is because there is no emitter to emitter degeneration in the input stage, as is clear from Fig. 5b. Operational transconductance amplifiers are frequently required to operate with no overall feedback to keep the inverting to non-inverting input voltage to a small value.

Grounding an OTA's inverting input and connecting its non-inverting input to its output also simulates a resistance, a negative one in this case. Figure 5c shows such a negative resistor.

It is connected across an rf tank circuit, so as to cancel the losses and raise the tuned circuit's dynamic resistance $R_d$ to infinity. Here, the 9.1kΩ/1kΩ network at the OTA's input keeps the drive to a level that the device can handle linearly. Again, a transistor is used as a detector to sense output amplitude from the CFA buffer. It also adjusts the $I_{in}$ of the OTA to stabilise oscillation amplitude.
An intriguing possibility is the use of this circuit to maintain a constant very low level of oscillation in the tuned circuit of a simple radio receiver. Level would remain constant over the entire tuning range and the circuit would act both as an automated reaction control and as AGC. Such a receiver could handle both AM and SSB signals, offering very good selectivity due to the tuned circuit operating at a very high Q.

**Sinewave frequency doubling**

An OTA can also function as a squarer, and hence as a frequency doubler. Current swing at the output of an OTA is proportional to the amplitude of the signal applied to the inverting or non-inverting input. It is also proportional to the magnitude of I_set and therefore to the product of the two quantities.

If a signal is applied simultaneously to both the inverting and I_set inputs, output current will contain a component representing the square of the input voltage. The resulting circuit is a two quadrant multiplier. Signal input can be bipolar but the I_set current must always be greater than zero, or the device simply cuts off. So the input merely modulates the magnitude of I_set, which is always positive. The dc component of I_set is responsible for a component in the output current corresponding to the original input.

To try the scheme out, I made up a doubler circuit using the LT1228 on the lines described but with a crucial addition. Fig. 6. Since the signal is applied to the inverting input, pin 2, all components of the voltage developed across the 100Ω load resistor at the output are inverted in phase relative to the input. As a result, the component of the input voltage in the output can be phase cancelled by adding in a component from the input via the upper 1.2kΩ resistor, leaving just the squared component. Since the square of \sin(wt) is (1-sin^2(2wt))/2, the circuit will thus double the frequency of an input sinewave to 2wt radians per second. Due to phasing, it will have no component at the original wt. The circuit is purely aperiodic. Apart from the trimmer at pin 2, no frequency sensitive components are involved.

Trimming extends the operating frequency range of the circuit by compensating for slight phase shift in the OTA at higher frequencies. Output will therefore be a pure sinewave at twice the frequency of the input, assumed to be a sinewave, over a wide range of frequencies. However, it would be wise not to rely on as much suppression of the fundamental input as illustrated in Fig. 6c.

As a final example of the many applications for this versatile part, Fig. 7 shows the circuit of a video cross fader. This uses two LT1228s in the feedback loop of an LT1223 CFA. Each of the two video inputs is applied via a 1kΩ resistor to the OTA section of each LT1228, the CFA sections being unused.

Both OTA output currents are connected to the inverting input of a further CFA. This input is a low-impedance current-driven type. Negative feedback is applied from the output of the CFA to the non-inverting input of each OTA via a 1kΩ resistor. In this way, unity gain is given to each signal when the wiper of the 10kΩ potentiometer is at mid-travel.

The amount of signal from each input passing to the output is set by the ratio of the set currents of the two LT1228s – not by their absolute value. Both set currents remain high over most of the potentiometer’s range. This keeps the bandwidth of each signal in excess of 15MHz, even when attenuated by 20dB. By this time, the other signal is dominant in the output video, and as the pot reaches the end of its travel, the attenuated signal is turned off completely.

**Reference**

USING RF TRANSISTORS

Choosing the right device

How does the intended application affect transistor choice? And what type of device would give the best performance? In this extract from their book RF Transistors: Principles and practical applications, Norm Dye and Helge Granberg answer both questions.

Looking first at low power, and the needs of a low noise amplifier, the main transistor selection criteria are operating frequency and noise figure. The most practical consideration is probably to choose a transistor characterised by the manufacturer with the necessary noise parameters. These are minimum noise figure at a given frequency, noise resistance and source resistance for minimum noise.

Manufacturers frequently plot gain and noise figure contours for a specified bias condition and frequency of operation. These are extremely helpful in making the necessary trade off between optimum gain and optimum noise when designing the low noise stage.

Choosing a transistor for other low power applications is generally simpler than for either low noise or high power because the choices are fewer. Most low power transistors have similar breakdown voltages although a few are designed for higher voltage use.

Occasionally, a special low power transistor designed to operate at very low voltages and low current will crop up. But generally all that need be done is to select a low power transistor with sufficient current rating for an intended application and with a high enough cut-off frequency to provide the desired gain at the operating frequency. Where switching is involved, the higher the cut-off frequency, the faster the switching capability of the device.

Package type can be an important consideration when choosing a low power transistor. The same die is frequently offered in metal can, plastic stripline opposed emitter (SOE), surface mount, and hermetically sealed metal-ceramic packages. Usually, the smaller the package, the lower the package parasitics and the better the RF performance of the die – especially at higher frequencies.

High power applications

A wide choice of high power rf transistors, i.e. devices greater than 1W, presents additional problems in selection. The major distinctions are in voltage of operation, operating frequency and output power, Fig. 1.

Assuming the application is an amplifier, other factors include linearity and bandwidth required, efficiency, thermal requirements for reliability and, of course, the type of package. Ruggedness, defined as the ability to withstand unfavourable load environments, is also a factor.

Voltage. Operating voltage is usually a predetermined specification, but in some applications – such as fixed location transmitters – there may be a choice. In these cases, designers must determine the advantages and disadvantages of low and high voltage designs. There is no significant difference in input impedance and matching. But output impedance is highly dependent on operating voltage and power output level.

Depending on power level, the operating voltage that gives the lowest impedance transformation required of the load impedance, usually 50Ω, should be selected. In multistage designs, the drivers and predistortion are often operated at a lower supply voltage than the power amplifier stage – partly due to their naturally higher output impedances. The result is a closer match to the input of the following stage.

Frequency. Choice of operating frequency is more straightforward. Manufacturers generally grade high-power rf transistors by frequency as well as voltage. Also, a transistor with adequate gain at the desired operating frequency should be selected.

High frequency transistors can always be used at lower frequencies, although special attention needs to be paid to stability, ruggedness, and cost. Normally, gain in rf transistors decreases with increasing frequency. When used at frequencies below their normal operating range, the gain will be higher and may create instabilities.

High frequency transistors are built using shallower diffusions, lower collector resistivity and less emitter ballasting – all necessary to achieve greater amplification at higher frequencies. Unfortunately, these are also the opposite of what is needed to improve ruggedness of a transistor. Gain and ruggedness at a...
given frequency are a trade off in device design.

Finally, high frequency transistors cost more than lower frequency transistors, all other factors being equal. So, choose a transistor that will give the desired gain, but no more, at a given frequency.

Power. The third major factor, output power, is an easier choice - simply select one that will give a sufficient level. Design of an amplifier line-up should always start at the output stage, working back from that point to select transistors. Gain available from the output transistor then sets the requirements for the driver stage.

Bandwidth considerations
Circuit design usually determines bandwidth. But at higher frequencies, the Q of the input impedance of a power transistor increases. This makes it more difficult to achieve broad band circuit designs. As the transistor's power rating and operating frequency increase, input and output impedances of the device decrease.

Think of it this way. Higher power transistors are simply low power transistors connected in parallel. Resistors in parallel result in a lower overall resistance; capacitors in parallel result in a higher overall capacitance. The result is an input impedance for high-power, high-frequency transistors that is too low to be practical for circuit designers having access only to the terminals of the transistor.

Manufacturers have alleviated the problem of low input impedance and high Q of high-power, high-frequency transistors by placing impedance matching networks inside the device package, near to the die. These networks only raise the impedance of the transistor as seen at the edge of the package but also transform impedance values to reduce the reactive components, and hence Q.

Impedance matching
An internally-matched transistor causes less difficulty in broad band circuits over its specified frequency range. In general, bipolar transistors designed for VHF and rated for 40-50W higher use internal matching techniques. At UHF the corresponding numbers are 10-20W and at 800MHz about 5W.

Internal matching networks are low-pass filters usually optimised for the high end of the specified spectrum range, where power gain and impedance levels are lowest. Most rf power devices for operating below 1GHz have only internal input matching. But internal output matching is also applied to higher power UHF transistors and most microwave devices.

Normally, the input matching network consists of an LCL combination, where L is the distributed inductance of the die bonding wires and C is a mos capacitor, Fig. 2.

Obviously, these internal matching networks place some bandwidth limitations on device operation, particularly at frequencies above the rated limits of operation. For example, a matched transistor designed for operation in the 225-400MHz range should perform well within this band.

Above 400MHz, power gain will drop sharply and the base-to-emitter impedance will increase in its reactive component. There comes a point where the given drive power cannot be transferred to the die itself. At an even higher frequency, the internal matching network will have a point of resonance where the input impedance becomes extremely high and the device's power gain is minimal.

Below the low end of the specified operating range, the internal matching network has a diminishing effect. However, at some intermediate frequency, 100-200MHz in this case, the matching network may produce an even lower input impedance than without internal

Table 1. Summary of specific characteristics of each device type. Note that the table focuses only on silicon mosfets in the fet category and some of the characteristics may not apply to jfets and other depletion mode fets. Similar electrical sizes for each are assumed for the impedance comparison.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Bipolar</th>
<th>Mosfet</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Z_{in}/R_s/X_e$ (2.0MHz)</td>
<td>3.80 — j2.0Ω</td>
<td>19.0 — j3.0Ω</td>
</tr>
<tr>
<td>$Z_{in}/R_s/X_e$ (150MHz)</td>
<td>0.40 + j1.50Ω</td>
<td>0.40 + j1.50Ω</td>
</tr>
<tr>
<td>$Z_{in}$ (load impedance)</td>
<td>Nearly equal for each transistor, depending on supply voltage and power output.</td>
<td>Required for linear operation. Low current source, such as resistor divider is sufficient. Gate voltage can be varied to provide an AGC function.</td>
</tr>
<tr>
<td>Biasing</td>
<td>Not required, except for linear operation. High current ($I_C/hFE$) constant voltage source necessary.</td>
<td>Low order distortion worse than with bipolar for a given die size and geometry. High order inter modulation better due to lack of ballast resistors and associated non-linear feedback.</td>
</tr>
<tr>
<td>Linearity</td>
<td>Low order distortion depends on electrical size of die, geometry and $h_{FE}$. High order intermodulation is a function of type and value of emitter ballast resistors.</td>
<td>Superior stability because of lack of diode junctions and higher ratio of feedback capacitance versus input impedance.</td>
</tr>
<tr>
<td>Stability</td>
<td>Instability mode known as half $f_s$ troublesome because of varactor effect in base-emitter junction. Lower ratio of feedback capacitance versus input impedance.</td>
<td>Over-dissipation failure less likely, except under high voltage conditions. $h_{FE}$ decreases with temperature. Other failure modes: gate punch through.</td>
</tr>
<tr>
<td>Ruggedness</td>
<td>Usually fails under high current conditions (over-dissipation). Thermal runaway and secondary breakdown possible. $h_{FE}$ increases with temperature.</td>
<td>Input impedance more constant under varying drive levels. Better stability, better high order intermodulation, easier to broadband. Devices and die can be paralleled with certain precautions. High voltage devices easy to implement.</td>
</tr>
<tr>
<td>Advantages</td>
<td>Wafer processing simpler, making devices less expensive. Low collector-emitter saturation voltage makes low voltage operation feasible.</td>
<td>Input impedance more constant under varying drive levels. Better stability, better high order intermodulation, easier to broadband. Devices and die can be paralleled with certain precautions. High voltage devices easy to implement.</td>
</tr>
<tr>
<td>Disadvantages</td>
<td>Low input impedance with high reactive component. Internal matching required to increase input impedance. Input impedance varies with drive level. Devices or die can not be easily paralleled.</td>
<td>Larger die required for comparable power level. Non-recoverable gate puncture. High drain-source saturation, which makes low voltage, high power devices less practical.</td>
</tr>
</tbody>
</table>
matching. This is due to the lesser effect of the series $Ls$ and the remaining shunt $C$.

Dropping further in frequency, the effect of the internal $Ls$ and $Cs$ will reach a point where a normal input impedance is approached. As a result, the internally matched transistors may not be suitable for bandwidths wider than those that the transistor was originally designed for.

There are certain design techniques for external circuitry that allow matched transistors to be used at lower frequencies and for extended bandwidths, with somewhat compromised performance. But such matching circuitry is usually complex. Furthermore, the device impedance profile at these frequencies – not given in most data sheets – must be known.

**Mofets versus bipolar**

It appears that extremely wideband amplifier designs are only possible with mosfets. For rf power purposes, the technology has been available for approximately fifteen years, although most of the breakthrough has occurred within the past five.

No internal impedance matching is used with mosfets, except in rare cases at 800-900MHz and higher frequencies. Such data sheet bandwidth specifications as 2-175MHz, 100-500MHz, and 500MHz are misleading since all unmatched mosfets, as well as bipolar transistors, are operable down to DC if stability can be maintained. They can also be used at higher than the specified frequency limit, keeping in mind the normal 5dB per octave power gain roll off.

Since the input impedance of a mosfet is several times higher than that of a comparable bipolar transistor without internal input matching, multi-octave bandwidths can easily be realised with proper circuit design. But because a mosfet is a high voltage device by its nature ($R_{DS(on)}$ compared to bipolar $V_{CES}$) its performance in low voltage applications may be challenged by its bipolar counterpart.

**Fet or BJT?**

There are now two basic types of rf power transistor – bipolar junction and field effect. Bipolar junction transistors, or BJTs, yield superior performance in some applications. In others, field effect transistors do a better job. Only two types of bipolar junction transistor are commercially available today, NPN and PNP.

Despite their inferior performance over NPN types, PNP transistors are primarily used in land mobile communications equipment requiring a positive ground system. All UHF and higher frequency devices are NPN due to their higher mobility of electrons as majority carriers, translating into higher cut-off frequency and improved high-frequency power gain.

Far more types of fet are commercially available for rf power use. The static induction transistor, or sit, is a version of a depletion-mode junction fet and metal gate Schottky fet, or mosfet. Usually, the mosfet is made of gallium arsenide and is also a depletion-mode type.

Another depletion-mode device is the standard junction fet. But this is only practical in low power pre-drivers and mixers, etc. The most common rf power fet is the vertical channel silicon mosfet. This device comes in a number of varieties of die structures, each having slightly different characteristics of $R_{DS(on)}$ and the various capacitances. It has been available since around 1975, and numerous improvements have been made in its performance and manufacturability.

There is also a lateral channel power mosfet in existence, consisting of a series of small signal fets connected in parallel on a single chip. Due to its lateral channel structure, it consumes more die area for a given power rating than the vertical channel device. As a result it is cost effective. However it has extremely low feedback capacitance, $C_{GS}$, resulting in an increased stability and higher gain at high frequencies.

Both these silicon mosfets are enhancement-mode devices. For the drain-source channel to conduct, their gates require positive voltages with respect to the sources. Conversely, a depletion mode fet conducts when the gate and source are at an equal potential, and requires a negative gate voltage for turn off (depletion).

**Comparing parameters**

With rf amplifiers, a major difference between a BJT and a mosfet is the need for base/gate bias voltage. An BJT only needs base bias for linear operation. There is very little difference in its power gain between a biased (class A, AB, or B) and an unbiased condition (class C).

In an unbiased enhancement-mode fet, gate input voltage swing must overcome the gate threshold voltage to turn the fet "on" with its positive peaks. Some fets have their gate threshold voltages specified as high as 6V. If the dc gate voltage is brought closer to its threshold level, a smaller voltage swing is needed to overcome it. Since in each case the gate-source rf impedance is about the same, the actual power gain can vary as much as 5-6dB depending on the initial threshold voltage and frequency of operation.

For linearity, a fet also needs to be biased in class A or AB operation. Since no dc current is drawn, the bias source may be a simple resistor divider, whereas a BJT requires a constant voltage source of 0.65-0.70V with a current capability of $I_Cpeak/I_{PEAK}$.

RF power design engineers accustomed to circuit design with BJTs are beginning to look at fet designs and learn about the differences in parameters and behaviour between the two types of semiconductors. Table I. Circuit design with fet is very similar. The same rf design practices – grounding, filtering, bypassing, and creating a good circuit board layout – all apply.

For each type of device, some precautions must be taken. Fets are sensitive to gate rupture. This is caused by excessive dc potential or an instantaneous transient between the gate and the source. The effect can be compared to exceeding the voltage rating of a capacitor, usually resulting in a short or leakage.

A power fet can be "restored" in some instances by applying a voltage lower than the rupture level between the gate and the source. The current must be sufficient, but not higher than 1.25A, to clear the gate short. A higher current would fuse one of the bonding wires to the area of the short on the die.

Some cells will always be destroyed, but with larger devices – 50W and higher – no difference in performance may be noticed. However, long term reliability can be jeopardised, and the practice is not recommended where high reliability is required.

A weak spot with the BJT is the possibility of thermal runaway. Devices with diffused silicon emitter ballast resistors are less susceptible than those having nichrome resistors. The diffused silicon resistors have a slight positive temperature coefficient; the nichrome ones have near zero coefficient. However, the diffused resistors are non-linear with current. Devices using them are less suitable for applications requiring good linearity.

The main reason for thermal runaway of a BJT is that $h_{JE}$ increases with temperature. In a mosfet, $g_{m}$ goes down, trying to turn the device off. In contrast, the gate threshold voltage decreases by about $1mV/°C$, making the temperature profile of a gate-biased device dependent on the initial value of $g_{m}$ and the voltage of operation.

Figures of merit for a BJT and fet are defined as the emitter periphery/base area and gate periphery/channel length respectively. In practical terms these relate to the ratio of feedback capacitance to input impedance. This is because linear geometries produce lower feed-
back capacitance for common emitter and common source configurations.

It appears that devices with higher figures of merit are more stable. This would be true, except that power gain is also higher, leading to instabilities through stray feedback. At a high frequency, feedback capacitance produces positive feedback due to phase delays.

One more BJT instability mechanism is a result of a varactor effect in its diode junctions, mainly the collector-base. This “half fB” is usually a steady spurious signal at half the frequency of the excitation. Lack of junctions in a fet mean this phenomenon is unknown in mosfet power circuits.

Matching impedance

The largest difference in impedance matching can be seen in the base-emitter and gate-source impedances. At dc the mosfet has an infinite gate-source impedance, whereas the BJT exhibits the impedance of a forward-biased diode.

At higher frequencies, depending on the device’s electrical size, the gate-source capacitance, Cgs, is enhanced by the Miller effect. This, together with the wire bond inductances, forms a complex impedance which may be lower than that of the BJT. Output capacitance Cov/Coss is almost equal for both types, of equivalent electrical size. Output capacitance has a large effect on the efficiency of an amplifier. This is because it must be charged, to around twice the supply voltage, and discharged again during each cycle of the operating frequency. Power used in charging is dissipated in the amplifying device. At a single frequency, a part — but not all — of the capacitance can be tuned out since its value varies with the output voltage swing.

Power loss due to output capacitance for a single ended BJT amplifier, for example, can be defined as:

$$P_L = (2C_{ov}(V_{CC})^2) \frac{1}{f}$$

where $P_L$ is power loss, $f$ is frequency and efficiency is $P_{out}/(P_{in} + P_L)$.

Power loss is directly related to capacitance and to the square of the supply voltage. So a higher operating voltage does not always result in higher efficiency, as commonly thought.

Equivalent parameters and their designations for bipolar transistors and mosfets are compared in Table 2. Note that all parameters are not applicable to both types of devices.

### Table 2. “Equivalent” parameters of bipolar and mosfet transistors.

<table>
<thead>
<tr>
<th>Bipolar</th>
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<td>$BV_{DSO}$</td>
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<td>$BV_{CES}$</td>
<td>$BV_{DSS}$</td>
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<tr>
<td>$BV_{CEO}$</td>
<td>$BV_{DGO}$</td>
</tr>
<tr>
<td>$BV_{EBO}$</td>
<td>$V_{GS}$</td>
</tr>
<tr>
<td>$V_{G}$ (\text{\text{(forward)}})</td>
<td>$V_{GS}$</td>
</tr>
<tr>
<td>$I_{CES}$</td>
<td>$I_{DSS}$</td>
</tr>
<tr>
<td>$I_{EBO}$</td>
<td>$I_{GS}$</td>
</tr>
<tr>
<td>$V_{CE(SAT)}/V_{DS(SAT)}$</td>
<td></td>
</tr>
<tr>
<td>$f_t$ (\text{\text{(f)}})</td>
<td></td>
</tr>
<tr>
<td>$G_{FE}$ (\text{\text{(f)}})</td>
<td>$G_{DS}$</td>
</tr>
<tr>
<td>$C_{eb}$</td>
<td>$C_{oss}$</td>
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<tr>
<td>$C_{ob}$</td>
<td>$C_{oss}$</td>
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<tr>
<td>$C_{rb}$</td>
<td>$C_{tss}$</td>
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<td>vibration meter</td>
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<td>£100</td>
</tr>
</tbody>
</table>

INDEX TO ADVERTISERS

Anchor Surplus Ltd ........................................ 977
Alternative Distribution (UK) Ltd ......................... 1031
Bull Electrical ............................................. 1086
Citadel Products Ltd ........................................ 1026
Chelmer Valve Co ........................................... 977
Cook International .......................................... 975
Dataman Programmers Ltd .................................. 1045
Display Electronics Ltd ..................................... 1015
Electrovalue Ltd .............................................. 981
Ericsson Systems ............................................ 1023
Essex University ............................................. 979
Flash Designs .................................................. 979
Halcyon Electronics Ltd ..................................... 1043
IPK Broadcast Systems Ltd .................................. 1043
Intergated Measurement ..................................... 1043
Invotron Ltd ................................................... 1006
Johns Radio .................................................... 1024
JPG Electronics .............................................. 1006
Kare Electronics ............................................. 1014
Kestral Electronics .......................................... 1014
Labcentre ....................................................... 970
M&B Electrical Supplies Ltd ................................ 1016
M&B Radio (Leeds) ........................................... 981
MOP Electronics ............................................. 989
Number One Systems ........................................ 1007
Pico Technology Ltd ......................................... 1031
Powerware ..................................................... 979
Ralph Electronics ............................................ 1056
Seetra Ltd ...................................................... 1002
SMC Ltd ......................................................... 1031
Stewart of Reading ................................................ 981
Surrey Electronics Ltd ....................................... 1007
Telnet ............................................................ 989
Tsiin Ltd ......................................................... 999
Ultimate Technology ......................................... 1006

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