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25 years of space

Cellular radio

Real-time clock for 6502

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Cover photos Illustrate David Whitman’s place on space exploration starting on a.p.s. Photography by courtesy of American Radio History.

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Additionally, the UDS package includes a comprehensive manual on how to use the development system.

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Additionally, the UDS package includes a comprehensive manual on how to use the development system.

CIRCLE 48 FOR FURTHER DETAILS.
NEWS COMMENTARY
IC design in the universities

British universities are to integrate their computer-aided engineering facilities and have announced through the University Grants Committee their commitment to five packages which will cover all their needs for C.A.E. facilities. The announcement follows a year of product evaluation by a university's working party, chaired by Dr Peter Jones of Manchester University. Dr Jones says that the purchase of professional, high-quality tools, worth about £25m in the commercial marketplace, represents "the biggest, co-ordinated step in the teaching of integrated circuit design arrangements in the world." Professor Eric Dagless, another member of the committee adds that the purchase of the best tools available would ensure that the universities would produce the "kind of graduates required by British Industry.

The orders have been placed with a combination of British and US/European suppliers. The following products have been offered: products able to run on a comprehensively range of micro, mini and mainframe computers. The British contribution is by Racal-Rodac, Quados and Silicon Microsystems. GenRad are supplying their British-designed HIL0 simulator and Silver-Laco, with head offices in California and Belgium, is contributing a variety of CAD packages. All the companies have agreed to forego their licensing fees and make the systems available to all the universities wishing to participate. So far around 45 universities are adding or developing courses which will include the design of integrated analogue and digital circuits.

RACAL-RODAC

Racal-Rodac are providing the first suite of software which integrates the entire design cycle for mid-sized silicon devices. The processes of design capture, simulation, layout, verification and pattern generation are carried out on a single database ensuring total compatibility throughout the design stage. This database at the heart of the system enables a well-structured hierarchical approach to design.

The design process begins by entering the data in a circuit schematic form or by means of a hardware description language (HDL). This is linked directly to a simulator which can perform both logic and circuit analysis, individually, and simultaneously. Functional level simulation can also be carried out by means of a high-level programming language.

Because a transistor has its full description in the HDL, not only its topological but also its electrical characteristics are assigned. The width, length, area, associated resistance and capacitance together with timing information must conform to the HDL description before running full on-line net list comparison between the physical design data and the physical layout topology. Real-time checking is the facility built in to assist the designer to correct any violation of the design rules. The combination of rule checking and debugging ensures optimum use of silicon area simplifies circuit modification, and removes many of the error message listings which occur with post-design simulation.

Quados is a computer that is easy to use and is designed in the design of the Transputer.

QUADOS "Silicon for the people" is the slogan for Quados (Icchip design on silicon) of Cambridge, who have an educational entry.

Haroon Ahmed, Peter O'Keefe and Andrew Hopper, directors of Quados with their electron beam.

SILICON MICROSYSTEMS (SMS)

Silicon Microsystems offer a silicon brokerage — they can have wafers manufactured by a number of semiconductor processing houses and provide themselves the final testing and packaging. They can also provide a number of design tools including a library of five and three-micron c.mos macroes. These are design system and process-house independent. This means that they may be incorporated into a wide range of design systems and also provide multi-source for any device developed under the SMS software system. SMS services range from semi-custom gate array devices through standard cell components to full custom I.C.

GENRAD

Hiho is a logic simulator developed at Brunel University and further developed and supported by GenRad's Design Engineering Group in Parnham. The software is used for logic and timing verification, fault simulation and test pattern generation. It has been adopted by many semiconductor houses in designing full or semi-custom devices by and by many systems houses for designing at p.c.b. level with standard devices. Hiho was designed to be powerful and can be ported on a wide range of computer systems and workstations. These range for mainframe IAX and IBM's to Apollo and the UK manufactured Whitechapel workstation. A recent addition is the IBM RT PC. Hiho can also work in conjunction with software and hardware products from the car suppliers. These include Silver-Lisco, Mentor, Daisy, Racal Rodac, and many others. Valid, Tektronix/Cae, Hewlett-Packard, Compaq, Intergraph and Intergraf all offer Hiho as the core simulator of their workstations and markets it as part of their systems. Waveform patterns created during the design and simulation process can be used in the preparation of complete test programs for both VLSI and PCB ATE.

SILVER-LISCO

Silver-Lisco is the amalgamation of a Silicon Valley company with a software house of semiconductor processing houses and provides themselves the final testing and packaging. They can also provide a number of design systems to use verified an I.C. circuit.

Eureka projects announced

Eureka is a European collaboration to develop high-technology products to compete in the world markets. Unlike Esprit or the Alveo project, which are undertaking long-term research into advanced technology, Eureka is aimed specifically at practical projects leading to marketable products.

At least 25 projects are under discussion, covering such technologies as pharmaceutical products, image processing, telecommunications, new engineering materials, environmental technology and advanced manufacturing.

Sixteen projects have been announced recently covering a wide range of technology and expertise:

1. Eurom: the development of a flexible automated factory for the production of p.c bs.

2. Cersei: European centre for image synthesis, to improve market and computer image technology.

3. ES2: Automatic design and production of integrated circuits using direct write-on-silicon.

4. GAAs: Development of design and manufacturing processes for the production of monolithic gallium arsenide microwave integrated circuits.

5. Mobile robot: Development of fast-moving robots for public safety applications such as natural disasters and anti-terrorism.


7. Eureka advanced software technology for the development of "software factories" incorporating software engineering.


10. Chemical waste destruction: the use of high-powered lasers for the detection and destruction of impurities in finished products and in waste products.

11. GTO thyristors: the development of a complete set of gate turnoff thyristors for use in railway traction systems.


15. Aprox: Advanced project for European information exchange, especially applied to the aerospace industry.


Each of the projects has a differing number of European participating countries spread over a timescale of between two and six years.
Electrical engineering vital for Britain’s future

An increased awareness of the contribution made by the electrical engineering profession to the national economy and greater emphasis on the education and training of young engineers for the future are essential if Britain is to compete successfully in world markets and redress its current unfavourable balance of payments.

This was the message given to MPs by IEE President Admiral Sir Lindsay Blyth. Sir Lindsay was speaking at a Seminar organised by the IEE in association with the Institute and Parliament Trust on ‘Chartered Electrical Engineers and their place in Industry and Society’.

Sir Lindsay stressed the contribution made by the electrical, electronic and associated manufacturing industries to Britain’s balance of payments. With annual sales of nearly £25,000M in 1984 alone, these industries provided more than half of all engineering sales. He also pointed out that as the industry moves into higher technologies the need for greater numbers of professional engineers will continue to rise.

“In order to meet this need”, said Sir Lindsay, “we must devote much more of our efforts and resources to produce more highly qualified engineers of all disciplines.”

Sir Lindsay pointed out that the number of applications from schoolchildren to take electrical engineering at University had more than doubled over the last twelve years as had the quality of graduates accepted. However, he warned that the quality of teaching in mathematics and physics must be improved if this encouraging trend is to continue. “This”, he said, “may well be the most significant shortcoming of all and we must seek ways to tackle it.”

The IEE President also highlighted another “potentially serious barrier to progress” — the difficulty in recruiting greater numbers of lecturers, ideally high achievers in their late 20’s or early 30’s, with good industrial experience.

“Sad”, he said, “the rigid university salary scales do not provide competition with industrial salaries for these good people and some way must be found to solve this problem”.

Sir Lindsay suggested that the “provision of industrial consultancies might bridge this gap and, in addition, build a link between universities and industry that will be of great benefit in future years”. Sir Lindsay also disclosed that the IEE is willing to administer such a scheme and will be pursuing the idea with industry and Government.

Sir Lindsay ended his address with a warning that it would be at least 10 years before changes to the system of engineering education was reflected in improved industrial performance.

“I would ask you all to recognise the very long term scales involved… So please do not expect instant successes from any changes which are made”.

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ELECTRONICS & WIRELESS WORLD APRIL 1986
Intelligent real-time clock

This real-time clock can be added to any 6502 computer. As an example, interfacing details are given for the Apple II.

Timing is controlled by a 32.768kHz crystal. The variable capacitor at pin 15 (Fig. 1) and other 15-16pF should be connected between pin 14 and the negative rail. This improvement is not mentioned in the 58174 data sheet.

Apple II Interface

The 50-pin expansion slots at the rear of the Apple monitor board provide a variety of signals: data and address buses, timing power supplies, timing control signals and in addition, three chip-select signals. Also accessible is pin 2 of the processor, the RDY signal. Unfortunately, the timing requirements of the clock chip make it necessary to derive the chip-select pulses by address decoding and to lengthen the read pulse further by the use of the RDY signal.

The Apple memory-map reserves 16 bytes for input-output signals to devices at each slot (at locations $0000, x+$8 to $03F) plus a common area of 2K bytes extending from $0800 to $0FF for program memory. A further 16 bytes of address space are reserved for use dedicated to slots 1-7, but these have not been used.

Table 1: internal registers of the 58174.

<table>
<thead>
<tr>
<th>Register</th>
<th>$A7</th>
<th>$A6</th>
<th>Mode</th>
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<tr>
<td>0</td>
<td>0000</td>
<td>Write only</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Tenths of seconds</td>
<td>0001</td>
<td>Read only</td>
</tr>
<tr>
<td>2</td>
<td>Seconds</td>
<td>0010</td>
<td>Read only</td>
</tr>
<tr>
<td>3</td>
<td>Tens of seconds</td>
<td>0011</td>
<td>Read only</td>
</tr>
<tr>
<td>4</td>
<td>Minutes</td>
<td>0100</td>
<td>Read or write</td>
</tr>
<tr>
<td>5</td>
<td>Tens of minutes</td>
<td>0101</td>
<td>Read or write</td>
</tr>
<tr>
<td>6</td>
<td>Hours</td>
<td>0110</td>
<td>Read or write</td>
</tr>
<tr>
<td>7</td>
<td>Tens of hours</td>
<td>0111</td>
<td>Read or write</td>
</tr>
<tr>
<td>8</td>
<td>Days</td>
<td>1000</td>
<td>Read or write</td>
</tr>
<tr>
<td>9</td>
<td>Tens of days</td>
<td>1001</td>
<td>Read or write</td>
</tr>
<tr>
<td>10</td>
<td>Day of the week</td>
<td>1010</td>
<td>Read only</td>
</tr>
<tr>
<td>11</td>
<td>Month</td>
<td>1011</td>
<td>Read only</td>
</tr>
<tr>
<td>12</td>
<td>Tens of months</td>
<td>1100</td>
<td>Read only</td>
</tr>
<tr>
<td>13</td>
<td>Days of the month</td>
<td>1101</td>
<td>Read only</td>
</tr>
<tr>
<td>14</td>
<td>Start</td>
<td>1110</td>
<td>Read only</td>
</tr>
<tr>
<td>15</td>
<td>Interrupt status</td>
<td>1111</td>
<td>Read only</td>
</tr>
</tbody>
</table>

Fig. 1. The 5MS8174 is a metal-gate e-mos clock-calender IC. Features include low-power standby operation, an interrupt timer and automatic calculation of leap-years.
Fig. 2. Hardware interface for the Apple II computer. The unit gives a continuous time display at the bottom of the screen.

The firmware for the real-time clock occupies 256 bytes of 2K eprom, located in the common area from $C8F00$ to $C8FF$. The F0 registers of the clock are situated at $C8F00$-$C8FF$. Thus the card should be inserted in slot 7 even though no use has been made of the input/output strobos dedicated to that slot.

The decoder is designed such that, if necessary, an eprom can be located on boards which are designed to occupy different Apple slots. The memory-select signals $MS_{1}$ to $A_{1}$ drives the eprom's chip-select pin. The chip-select signal $CS_{1}$ derived from $A_{1}$ to $A_{2}$, is combined with the output from pin 11 of IC$_{1}$. A further signal $BS$, derived from $A_{1}$ to $A_{2}$, produces a clock select signal $CS_{0}$ to access the 16 memory locations $C8F00$ to $C8FF$. If required, the eprom can be confined to the 256 bytes from $C8F00$ to $C8FF$ by moving the link on the board to pin 6 of IC$_{1}$.

Software

The software consists of 256 bytes of machine code located at $C8F00$. Absolute addressing has been used throughout: the only ram locations affected are the text window limit ($E23$) and the vectors at the top of page 3. No registers are affected by interrupts.

The functions of the clock-chip's 16 internal registers are listed in Table 1. The first 13 of them keep the time: the short interval is in tenths of a second and the longest a year.

At the bottom of the screen the time display shows months, day of the week, hours, minutes and seconds. The circuit generates the interrupts which update it.

When operated from a 5V supply, the clock can be programmed to generate interrupts at 0.5, 5 and 60s intervals. It cannot generate interrupts in the battery-backed mode. After an interrupt has been generated it must be cleared by reading register 15, the interrupt register, three times.

After powering the circuit, disable the display before enabling or setting. To set the clock, CALL (5053). Enter the date and time at the flashing cursor, pressing return each time. The clock starts with seconds at zero when minutes are entered.

In monitor mode, the time may be read by typing control-J return or CFSAG.

To disable the display, CALL (5070). The machine will operate normally whilst the clock continues to keep time. The display can be re-started by CALL (5053). IRQ is vectored using 83F0P8 to the clock.

To use the clock in machine-code programs use JSR CFSB and read digits from the display. Alternatively, use LDA C8F0X, followed by AND C8F0X to read the clock directly.

(The next article will describe an electronic programmer.)

Table 2: Memory dump of the clock software.

<table>
<thead>
<tr>
<th>Hex</th>
<th>Decimal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
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<td>...</td>
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</tbody>
</table>
Improved Hilbert transformer for s.s.b. speech

The ‘out-phasing’ method of s.s.b. modulation, using a Hilbert transformer, can be used for speech, since the ear is insensitive to phase

Single-sideband is s.s.b. modulation can, in theory, be achieved by the so-called ‘out-phasing’ method, which depends upon the identity

\[
E_{\text{in}} \cdot \cos(\omega t + \phi) \leftrightarrow E_{\text{in}} \cdot \cos(\omega t + \phi) + \frac{E_{\text{in}}}{2E_{\text{out}}} \cdot \sin(\omega t + \phi)
\]

This last represents s.s.b. modulation of a carrier of frequency \(2f\) by a waveform \(E_{\text{in}} \cdot \cos(\omega t + \phi)\), which can be split into even- and odd-sideband components, the even sideband being also known as the lower sideband, u.s.b., and the odd sideband the upper sideband, u.s.b., i.e., half modulation. Thus, in order to implement an s.s.b. modulator using this principle, we require a device which will convert a given waveform \(E_{\text{in}} \cdot \cos(\omega t + \phi)\) into a pair of related waveforms \(E_{\text{in}}(\omega t + \phi)\), \(E_{\text{in}}(\omega t + \phi)\). Such a device is called a Hilbert transformer, since \(S(\omega)\) is precisely the mathematical Hilbert transform of \(S(t)\) defined by

\[
S(\omega) = j\omega S(t) dt.
\]

In general, true Hilbert transformers present some difficulty in implementation but, fortunately, from a practical point of view, a major application is in s.s.b. broadcasting where one can exploit the fact that the human ear is substantially insensitive to the phase of audio signals. Thus, for speech s.s.b., it is sufficient, given a speech waveform \(S(t) = E_{\text{in}}(\omega t + \phi)\), to produce two waveforms:

\[
g(t) = E_{\text{in}}(\omega t + \phi) + \frac{E_{\text{in}}}{2E_{\text{in}}} \cdot g(t)
\]

and

\[
g(t) = E_{\text{in}}(\omega t + \phi) + \frac{E_{\text{in}}}{2E_{\text{in}}} \cdot g(t)
\]

where the \(g(t)\) are arbitrary functions of the \(w(t)\). Note that since \(g(t)\) is \(g(t)\) with a \(w(t)\) phase shift at all frequencies, the ear will not distinguish between \(S(t)\) and \(g(t)\).

Although the device which produces \(g(t)\) and \(g(t)\) from \(S(t)\) is not a true Hilbert transformer, for speech s.s.b. it is just as effective. It is such a device which we consider here, and conventionally known as the Hilbert transformer.

In practice, even this type of device cannot be realised with perfect precision over infinite bandwidths as seen at all frequencies, but is always, engineering compromises must be sought. The device is often considered here as a single stage, single ended circuit implementation which, of course, can also be realised in the form of a hybridised circuit. In such a circuit, the analysis given below permits the designer to select component values, but the explicit circuit described was implemented in discrete components and in consequence uses parallel values of resistance and capacitance, using series or parallel combinations where necessary to achieve sufficient accuracy.

Basic circuit

Various circuit topologies can be considered. It is desirable to achieve the desired aim but one which has been widely used and which forms the basis of the present article is shown in Fig. 1. This gives a phase shifter which is a function of both frequency and by suitable choice of components can be made to give a flat phase shift over a wide range in which, in theory, is constant for all frequencies and in practice is certainly substantially constant over the audio range.

A further circuit, which can be used for the same purpose, gives all phase shifts, and by suitable choice of components can be made to be constant and equal to that of the first circuit, and more importantly the phase shift can be made almost zero (or less than that of the first circuit. Thus by feeding both circuits with an input \(S(t)\), two outputs \(g(t)\) and \(g(t)\) can be obtained as desired.

The relative phase shift is precisely \(w\) only at four frequencies and there is a trade-off between the maximum phase shift within the operating bandwidth and the minimum of the bandwidth.

A circuit of this type has to be considered a practical one in which the bandwidth is strictly confined to the normal ‘speech’ bandwidth of 300 to 3000Hz. Within this band it is not possible to achieve good performance, and any better than can easily be exploited but outside it, performance drops off quite rapidly.

Since, in many applications, filtering is also used to achieve adequate suppression of the unwanted sideband, a major function of the out-phasing technique can be to ease the specification requirements of the filter response, particularly in relation to the steepness of its skirts.

It therefore occurred to the author that it might be desirable to extend the bandwidth of the device for the expense of a small degradation of performance within that bandwidth. However, it was first necessary to define acceptable performance limits.

Phase and amplitude tolerances

A fully comprehensive analysis is highly complicated, but for present purposes it is sufficient to consider modulation by a single stage of frequency to separate the effects of amplitude and the phase errors.

Suppose that we attempt to achieve the output phase-transformation of our Hilbert transformer by the out-phasing method, but that our Hilbert transformer introduces a phase error \(\phi\) and that in addition (in an underdetermined process) a practical amplitude error \(A\). Then, we might, of course, normalise nominal

amplifier to unity.) Thus our ‘u.s.b.’ output will be

\[
X(t) = A \cdot \frac{\cos(w t + \phi)}{R} \cdot \cos(\omega t + \phi) + d
\]

and suppose \(A\) corresponds to the desired sideband, so that ideally \(B = 0\). Then after some manipulation we obtain

\[
A^2 = 1 / (1 + A^2 + A^2 + A^2)
\]

Then

\[
B^2 = A^2 / (1 + A^2 + A^2 + A^2)
\]

We may obtain Table 1 for unwanted sideband level (u.s.b.) compared with the wanted level

\[
A = 0.01, 0.03, 0.05, 0.06, 0.08, 0.1, 0.12, 0.14, 0.15
\]

\[
\text{u.s.b (dB)} = -46, -56.5, -32.3, -30.7, -28.3, -26.4
\]

Considering now a phase error only (i.e., \(A = 0\))

\[
B^2 = A^2 / (1 + A^2 + A^2 + A^2)
\]

\[
\text{u.s.b (dB)} = -46, -42.1, -37.7, -35.2, -33.2, -31.6, -30.3, -29.1, -28.1, -27.2
\]

Subsequently obtained above an band extending from 240Hz to 375Hz which, in conjunction with well designed balanced modulators and combiner, should permit attenuation of a u.s.b. of better than –30dB over this band. The extended bandwidth should also ease the off requirements of filters used to enhance u.s.b. suppression.

In fact, for easing filter requirements, the lower frequency limit is probably more significant than the upper and a slightly different design may be preferable, as described later. However, the author’s requirements at the time were not confined to attenuating to the lower frequency limit.

The analysis given below derives the expression of the circuit and of theoretical performance and allows designers who so wish to implement different phase performance bandwidth compromises.

Discrete-component design

It is inevitable that performance will depend on the accuracy of component values. For the discrete component version, it is noted that silver-mica capacitors and high-stability resistors are used with values not exceeding 1% tolerances. Good quality accuracy components are available the designer can exploit this (as shown later).

In addition, the operational amplifiers should have high input impedance and high voltage gain to drive the audio band. As well as low offset current. The authors have used type CA3140 amplifiers. The experimental version also introduced further as shown in Fig. 2. The circuit is shown divided into two sections, the output being taken at the point of adjustment. The signal bandwidth is hindered in both of the circuit. This is shown divided into two sections, the output being taken at the point of adjustment. The signal bandwidth is hindered in both of the circuit. This is shown divided into two sections, the output being taken at the point of adjustment.
since, as will appear later, the circuit component values must be derived from these values by a rather obvious process, it is desirable to minimize any approximations until these component values are obtained, especially since the total parameter variation over the whole range from n = 3 to n = 4 is only about 7% in some instances.

Now from (16) and (17) if

or \( b' + b'' - C_2 + b'' = 0.1 \)

i.e. \( b' = 0.921 b'' + 0.921 \)

(20)

Table 3

<table>
<thead>
<tr>
<th>( n )</th>
<th>( a^2 - b )</th>
<th>( \phi' )</th>
<th>( \phi'' )</th>
<th>( \phi'' )</th>
<th>( \alpha )</th>
<th>( \text{angular error (deg)} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.0</td>
<td>10.6667</td>
<td>5.2479</td>
<td>0.016005</td>
<td>3.57990</td>
<td>1.46952</td>
<td>0.93</td>
</tr>
<tr>
<td>3.2</td>
<td>10.0432</td>
<td>5.3268</td>
<td>0.017969</td>
<td>3.68850</td>
<td>1.47616</td>
<td>0.93</td>
</tr>
<tr>
<td>3.4</td>
<td>11.0295</td>
<td>5.4057</td>
<td>0.019685</td>
<td>3.63775</td>
<td>1.48090</td>
<td>1.12</td>
</tr>
<tr>
<td>3.6</td>
<td>11.9081</td>
<td>5.4847</td>
<td>0.021123</td>
<td>3.69506</td>
<td>1.49956</td>
<td>1.22</td>
</tr>
<tr>
<td>3.8</td>
<td>11.9823</td>
<td>5.5637</td>
<td>0.022331</td>
<td>3.72089</td>
<td>1.50692</td>
<td>1.33</td>
</tr>
<tr>
<td>4.0</td>
<td>11.9754</td>
<td>5.6427</td>
<td>0.024717</td>
<td>3.74428</td>
<td>1.51237</td>
<td>1.43</td>
</tr>
<tr>
<td>4.2</td>
<td>11.9756</td>
<td>5.7217</td>
<td>0.027265</td>
<td>3.77241</td>
<td>1.51841</td>
<td>1.54</td>
</tr>
<tr>
<td>4.4</td>
<td>11.9762</td>
<td>5.8006</td>
<td>0.029546</td>
<td>3.79053</td>
<td>1.52438</td>
<td>1.65</td>
</tr>
<tr>
<td>4.6</td>
<td>11.9785</td>
<td>5.8796</td>
<td>0.032479</td>
<td>3.80805</td>
<td>1.53005</td>
<td>1.76</td>
</tr>
<tr>
<td>4.8</td>
<td>11.9828</td>
<td>5.9587</td>
<td>0.035797</td>
<td>3.82503</td>
<td>1.53495</td>
<td>1.87</td>
</tr>
<tr>
<td>5.0</td>
<td>11.9897</td>
<td>6.0358</td>
<td>0.039504</td>
<td>3.8415</td>
<td>1.53894</td>
<td>1.99</td>
</tr>
</tbody>
</table>

For a given value of \( n \) we can then obtain \( T_1 = \frac{y}{Y} \) from (21). From (8) we can obtain \( T_1 = \frac{k}{n} \), and from (10) \( T_1 = \frac{a}{n} \) and \( T_1 = \frac{a}{n} \). From (8) we obtain the value of \( n \) thus completing the design.

A commonly used circuit has \( a = 1, b = 0.256 a, c = 3.5 b, d = 1.477 a \) which accords well with Table 3 but corresponds to a bandwidth of about 11.4. Then \( n \) should be less than 24B at least from 173 to 1.5kHz.

The function of the circuit is to provide an upper limit of 500Hz for the same peak angular errors as above.

### Second design

If the chief interest centers on the lower frequency limit, as in cases where relaxation of filter requirements is a major aim, it may be preferable to use components as given below. These should give a lower "limit" of 1kHz and an upper "limit" of 500Hz for the same peak angular errors as above.

#### Component design value

<table>
<thead>
<tr>
<th>( C_1 ) and ( C_2 )</th>
<th>6800pF</th>
<th>3900pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_1 ) and ( R_2 )</td>
<td>2200 ( \mu )F</td>
<td>2200 ( \mu )F</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>( C_1 ) and ( C_2 )</th>
<th>6800pF</th>
<th>3900pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_1 ) and ( R_2 )</td>
<td>2200 ( \mu )F</td>
<td>2200 ( \mu )F</td>
</tr>
</tbody>
</table>

#### Third design

In some applications, adequate n.s. suppression may be obtained by filtering alone at frequencies near to the lower end of the band, e.g. above say 2.5kHz. In such a case almost the sole purpose of the outphasing technique may be to ease the filter requirements at the lower end of the band.

Using the analysis provided one can readily design for this case also, but the design in Table 4 may be considered as an example.

### Third design

In the experimental circuit the author wished to be able to adjust the value of \( \mu \) empirically (and differentially in the two cases of the circuit) in this case also, but the design in Table 4 may be considered as an example.

### Conclusion

Figures 2 and 3 show the circuit as implemented and the performance obtained.
combined with the natural spectrum of speech should make energy levels from 0 to 3000Hz on the unwanted sideband very low compared with the main wanted sideband energy. Spurious tones when combined with multiple filters, excellent u.s.b. should be readily attainable over the range from 100Hz upwards.

component design suggested value implementation

| C1 and C2 | 4700pF | 4700pF |
| C2 and C3 | 2557pF | 2200pF shunted by 300pF |
| R1 | 180kΩ | 180kΩ |
| R2 | 330kΩ | 330kΩ |
| R3 | 4.3kΩ | 68kΩ shunted by 120kΩ |
| R4 | 210kΩ | 420kΩ shunted by 420kΩ |
| R5 | 33kΩ | 33kΩ |
| R6 | 100kΩ | 100kΩ |
| R7 | 11.593kΩ | 120kΩ shunted by 330kΩ |

(4) Further shunt component of 22pF gives precisely the nominal value rather than the nominal 1.25% error in the simpler implementation.

The design procedure is summarized as follows (with a = 1).

Define operating bandwidth B as the ratio of the higher (U) frequency in the band over which optimum performance is required or is achievable.

(a) If the bandwidth B is the prime interest, calculate Next and find a and if from table 3, interpolating if necessary.
(b) If the signal phase error is the prime interest, use this to determine a and from table 3, interpolating if necessary. (The equations permit extensions of table 3 for precise interpolations to be calculated if required.)

2. \( R = \frac{1}{2} \left( \frac{1}{a} + \frac{1}{v} \right) \). (10)
3. Find the "center" frequency \( f = \sqrt{f_C f} \) of the filter, and \( f_N \) will be known. If \( 63 \leq f_N \leq 210 \), it will be known approximately and \( f_{CD} = f_N = f_C \) so that a "better" \( f_{CD} \) can be chosen.

4. Then \( T_1 = 1/2T_2/\pi \).
5. Choose a convenient value for \( C_1 \); for most of the audio range, \( C_1 \) will probably be selected in the range 1000 to 10,000pF.
6. Find \( R_1 = T_1 C_1 \).
7. Find \( R_2 = R_1 \).
8. Use a convenient \( f_C \) and \( f_N \).
9. Choose \( R_6 \) and \( R_6 (C_3) \) and 100kΩ respectively are suggested depending on gain requirements.
10. Find \( R_3 = R_2/\left( 1 - \left( 1 + 1.75 \right) \right) \) (11.593kΩ for suggested values of \( R_6 \))
11. Find \( C_2 = C_3 \).
12. This defines one half of the circuit.
13. Select suitable value for \( C_3 \) (The same valve as for \( C_1 \) is often convenient).
14. Find \( R_4 = \left( T_1 C_1 \right) \).
15. \( R_6 \) and \( R_9 \) are shunted by \( R_6 \) and \( R_9 \).
16. Put \( C_4 = C_5 \).

This defines the other half.

Finally, it should be pointed out that if higher accuracy components can be employed (as in certain hybrid realizations) then the designer can achieve either better performance over the band or the same performance over a wider band.

The outphasing method

If a high frequency carrier \( c_{01} \) is amplitude modulated by a low frequency waveform \( s(t) \), the resulting high frequency waveform \( a(t) = c_{01} s(t) \) is a double-sideband (d.s.b.) signal in which essentially the same information \( s(t) \) is carried in frequencies above \( f_{CD} \) (the upper sideband) as in those below it (the lower sideband).

Slightly \( s(t) \) represents a carrier-suppressed d.s.b. signal. Normally amplitude modulation (a.m.) includes a carrier component also and can be written as \( a(t) = c_{01} s(t) \), where \( a(t) \) is a constant usually chosen to exceed the peak negative value of \( s(t) \). However, the presence or otherwise of the carrier component is irrelevant to the following discussion. If

\[ s(t) = a \cos(\omega t + \phi) \text{ then } s(t) = a \cos(\omega t + 1 + \phi) \]

then

\[ \cos(\omega t + \phi) \cos(\omega t + \phi) = \cos(2\omega t + \phi) + \cos(\omega t + 2\phi) \]

This is the outphasing method.

If we now generalize \( s(t) \) from a sine wave

\[ s(t) = a \cos(\omega t + \phi) \]

which can represent any waveform, the same technique can be used by now. \( s(t) \) is a waveform for which much frequency component has the same amplitude as in (2) but is phase shifted by exactly \( \pi \). A device which performs this function of converting \( s(t) \) into \( s(t) \) or into \( s(t) \) is called a Hilbert transformer.

In practice the filtering method involves very sharp cut-off - far sharper than is possible with the outphasing method. The outphasing method is difficult to control to give better than 30 to 40 db suppression of the unwanted sideband. It can, however, be used to ease the cut-off requirements of the filters in a composite system where the filter provides adequate suppression at frequencies remote from the carrier while the outphasing technique greatly improves suppression near to the carrier on the "sides" of the filter response.

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Using current conveyors

Produced from current mirrors and op-amps, current conveyors can be used in a wide range of circuits from oscillators to frequency-dependent negative resistors.

One of the first requirements for current activated circuits is to be able to make a direct copy of a current. This function is nearly always performed by matched transistors configured as current mirrors to produce a current transfer ratio of unity. Previous articles in Windows World have looked in detail at the operation and performance of current mirrors to the treatment here will only be in outline.

Figure 1 illustrates the form of the current mirror used for precision circuits. Transistors T1 and T2 form the basic mirror of the mirror operation with T3 and T4 helping to equalize conditions for T2 and buffer the current transfer ratio against output voltage swings.

Using matched transistors in the CA3061AE, i.e. package as a four-transistor mirror permits a current transfer ratio of unity to be obtained up to a current of 10mA over a voltage swing of ±1V with an error of less than 1% and an output resistance approaching 50Ω. Main parameters affecting mirror accuracy in a four-transistor mirror are transistor current gain and base-emitter voltage mismatch between the transistors.

For p-n-p transistor mirrors overall mirror transfer ratio is approximately the same, even though transistor current gain falls more rapidly with current, since it is compensated for by the greater transistor current. The output impedance of p-n-p transistor mirrors remains high and the current mirror output is limited only by the output impedance of the devices driving the output node.

There is also a small component of current mirror offset for p-n-p transistors in the unequal bias currents of the op-amp. This can be easily reduced by around 50% at the output using a 50kΩ variable resistor connected between the output of the op-amp and the positive supply.

In practice, transistors used to produce a range of op-amp allowing accurate current transfer to be used with current mirrors. The problem is to be that this will produce a slight change in output current for a given change in input current.

For applications where it is possible to tolerate lower accuracy, three-transistor mirrors (T1, T2) or even basic two-transistor mirrors (T1, T2) may be acceptable. The symbol used to denote a current mirror is as in Fig. 2, no matter how many transistors are used.

Ampifiers circuits with a controlled output current can be configured by voltage-controlled current sources (VCCS, or transconductance amplifier) and current-controlled current sources (CCCS, or current amplifiers). Many published circuits have shown how operational amplifiers (op-amps) may be used to produce these two functions. Unfortunately nearly all of them suffer from problems of excessive tight resistor matching to balance negative feedback, and any slight deviation in performance because of component imbalances is very serious.

The most useful technique is undoubtedly that of op-amp supply current sensing, as in Fig. 3, where a copy of the op-amp current is reproduced at the output. Output current is therefore equal to the input voltage divided by R4, thus producing a transconductance amplifier.

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CURRENT CONVEYORS

Fig.5. A class II + current conveyor can be produced from a single op-amp and two current mirrors.

amp bias current and input x reflects the voltage at y and performs as an open-circuit stable current terminal. A class II - conveyor can be produced by simply adding a second pair of mirrors cross-coupled to produce a phase inversion between l1 and l2, as in Fig.6.

How do they perform? Using the usual CA3066AE mixed transistor arrays and an LM301 op-amp with a compensation capacitor of 39pF results in a small-signal bandwidth greater than 1MHz, again limited by the p-n-p transistor array performance beyond this region.

Transfer distortions of around 65 to 70dB can be expected, depending on loading conditions (ideally at an open, with an effective capacitance to ground at terminal x of about 4pF). It is worthwhile employing good circuit layout techniques to minimize this value to avoid compromising conveyor performance at high frequencies.

If required current gain can be introduced into the conveyor by including a two-resistor current mirror arrangement in the feedback loop, similar to that of Fig.4. A feedback connection of the current mirrors may also be used if extremely low distortion with unusually high load impedance are required.

There is little known about elegant circuit arrangements, known as a translinear circuit, due to Gilbert that uses a set of transistors arranged in a ring. One version of this is shown in Fig.7.

Now, the relationship between collector current l1 and base-emitter voltage VBE for a transistor may be written as

\[ I_C = I_L \exp\left(\frac{V_Y}{V_T}\right) \]

where \( I_C \) is reverse saturation current of the transistor and \( V_T = \text{thermal voltage} \times K \).

Assuming matched transistors, \( I_L \) is the same for all devices and operating at normal current levels, the balance of collector currents in Fig.7 may be written as

\[ I_{L1} = I_{L2} \]

If \( I_{L1} \) and \( I_{L2} \) are held constant and equal at a value \( I_L \) by using current sources and the input current injected at \( I_{L1} \) we can write simply that \( I_{L1} = I_{L2} \) for the polarity shown. This property can be used to good effect by adding a pair of current mirrors and a long-tailed pair, as in Fig.8.

Transistors \( TR_1 \) and \( TR_2 \) and current mirror \( CM \), if used as a voltage follower that accurately transfers input voltage \( V_x \) from point y to point x. As a result of \( V_x \) and \( I_{L1} \) both zero the translinear cell forces \( I_{L1} \) and \( I_{L2} \) to be equal and hence output current \( I_{L1} \) to be zero.

If there is an input current \( I_L \) either injected directly at \( x \) or as a result of a copy of \( V_x \), appearing at x connected to an impedance, then operation of the translinear circuit will ensure that \( I_{L1} = I_{L2} = I_L \). Finally, output currents \( I_{L1} \) being the differences in mirror currents \( I_{L1} \) and \( I_{L2} \) will equal \( I_L \). These are just the properties of a class II + current conveyor.

Using mixed transistor array CA3066AE to build the translinear conveyor circuit of Fig.8 results in a bandwidth of around 1MHz, again limited by the same shortfalls in p-n-p transistor performance.

Fig.6. The addition of a further two cross-coupled mirrors results in a class II - conveyor.

The accuracy of its performance is similar in other respects to the previous circuits in Figs. 5, 6. The main difference is in the translinear circuit where the frequency of unity gain where the frequency of current sources must be taken in increasing a value for current source since it sets an upper limit directly on the maximum possible output current.

Current conveyor applications

By virtue of their flexibility current conveyors may be used to produce circuits and functions, some readily apparent, others more obscure. Observations from their basic operating principles may readily be used to configure VCC, VCC, and VCC and VCC sources with additional components, except for a single additional resistance in the case of VCC and VCC sources to define the limits of capacitance by controlling the term \( R_1 \) and \( R_2 \) with nearly equal values of \( R_1 \) and \( R_2 \).

Another interesting area of application for monolithic fabrication, with the bonus of increased accuracy due to better device matching on the same chip.

The useful circuit property of a grounded negative resistance can be produced using only a single grounded resistance and a class II - conveyor as in Fig.9. Because of the positive phase relationship between the currents \( I_1 \) and \( I_2 \) voltage applied at \( x \) will express a resistance equal to \( -R \). The resistor may of course be replaced by a general impedance \( Z \). A fully floating negative resistance or impedance without any ground reference can be synthesized by the addition of a second conveyor to produce the symmetrical circuit of Fig.10.

An example of filter design using current activated circuits is shown in Fig.11. Making \( Z_1 = Z_2 = R \) and using a capacitance \( C \) produces an all-pass filter with a voltage gain of unity where the frequency of unity gain where the frequency of current sources must be taken in increasing a value for current source since it sets an upper limit directly on the maximum possible output current.

Conveyors may also be used to design oscillators whose frequency is determined by grounded capacitors with tuning from a single grounded resistor element, Fig.12 - both important considerations in monolithic circuit fabrication. The circuit may be changed in that of a voltage controlled oscillator (vco) by replacing \( R_1 \) by the channel resistance of a field effect transistor, except for a single additional resistance in the case of VCC and VCC sources to define the limits of capacitance by controlling the term \( R_1 \) and \( R_2 \) with nearly equal values of \( R_1 \) and \( R_2 \).

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Fig. 13. A grounded inductance converter and a capacitor requires the addition of an inverting conveyor.

Fig. 14. A fully floating frequency dependent negative impedance converter can be synthesized from only two class H - current conveyors.

Fig. 15. Typical f.d.n.r. frequency response curve showing steep resonance peak and sudden phase change.

with the load at terminal two. Using a 500 signal source connected at terminal one with 1kΩ resistors as Z1, Z2, Z3, and Z4, and 100pf capacitors for Z1 and Z2, produces the results shown in Fig. 15. At low frequencies the large negative resistance generated by the circuit produces 180° phase inversion between input and output with a very low gain.

As frequency increases, the synthesized negative resistance at some point becomes equal to the sum of the source and load resistance and the circuit exhibits a very high gain.

At resonance this gain is theoretically infinite but in practice is limited by the linear range of circuit operation or power supply voltages. This is comparable to a value of around 40dB as shown in the diagram.

Conclusion

Current activated circuits form an alternative approach to the more usual voltage activated ones where lower load impedances and smaller voltage excursions may offer an operating advantage. They can be used to design a wide range of circuit functions from current amplifiers through to gyrators and frequency-dependent negative impedances for active filter design.

References

could handle an additional 3,500 subscribers in the Paris area. During peak hours, the French PTT has been installing 450MHz facilities in Lyons, Marseille and Nice, which will provide room for another 150 users in each of these areas.

Waiting lists for the new saturated car telephone service in France are growing. Despite the French PTT's announcements of additional frequencies, the new system will not be able to cope with future demand and the lack of spectrum coverage is a major problem.

Aware of the severe capacity problems, the French PTT has decided to offer a new type of service, the Téléphone de Voiture réseau. This network, which was introduced by the French PTT in 1965, allows car owners to place calls without having to subscribe to a fixed-line service. It is a direct-dial car telephone service that can be used anywhere in France, even in rural areas. The French PTT claims that this service will be available to all car owners by the end of 1986.

The French PTT also continues to build new equipment for its high-frequency network. As of the end of 1985, the French PTT had installed 23,000 ES1000 lines, which are capable of handling 30,000 subscribers. The French PTT is hoping that this new service will help to alleviate the problems of future capacity requirements.

In addition to its car telephone service, the French PTT offers a number of other services, such as the Téléphone de Voiture réseau, which is a direct-dial telephone service that can be used anywhere in France. The French PTT is also building new equipment for its high-frequency network, and is hoping that this will help to alleviate the problems of future capacity requirements.

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Land Mobile Radio

Nigel Cawthorne reports on the IERE's third international Land Mobile Radio conference.

The three-day Land Mobile Radio conference, held by the IERE, was attended by nearly 200 delegates from 40 countries and represented more than 200 companies. The conference featured a wide range of papers, including discussions on first-generation systems and their evolution to the next generation. Many of the papers addressed the technical challenges and opportunities associated with the development of new systems and technologies.

Digital cellular

Tony Potter, BTDM, discussed the current state of digital cellular systems in the UK and the potential for future developments. He highlighted the importance of digital cellular technology in providing higher quality services to users.

BCC ENGINEERING

The BBC Designs Dept. is currently working on the development of a new cellular system, which is expected to be ready for deployment by the end of the year. The system will support voice and data services and is designed to be compatible with existing systems.

AN ANSWER ABOUT 'Q'

I now have an answer to my question about 'Q'. It turns out that the value of 'Q' is determined by the characteristics of the system. The answer was provided by a colleague who works in the field of electronics.

NEW LOGIC SYMBOLS

Letters published to date do not reflect much enthusiasm for the 'new symbols'. I suspect that more problems will result from their introduction than there will be benefits gained. It does seem that all the implications of introducing new symbols are not yet sufficiently understood. I wonder just what degree of involvement 50% of the addressees have had.

There are three serious problems which should be considered careful thought to the introduction of new symbols in the documentation of electronics. Firstly, no significant benefits have been made of introducing the new symbols or of supporting their use through educational means. Engineers and managers should take a critical look at the financial implications for their product documentation and production costs and see if they predict that the final cost to the nation will be enormous. Secondly, I have seen extremely heavy going and frequently ambiguous and generally inadequate.

Secondly, there will be a dramatic increase in documentation errors, due to the over-complexity of the new symbols. It has always been true that new symbols are sufficiently checked their introduction; the new symbols will only make the checking of the documentation seem safer. Thirdly, new education systemseem unable or does not even try...
choe, an attitude which is aggravating for the methods which consider documentation and technological applications as an expensive overhead, to be written off at any time.

Finally, one must consider the trends for illustration in technical redefinitions, which is often the case, more than once, to the point of unreasonability (again, a necessary, but not a cost-effective). Generators of documentation have to be aware that essential detail in the new symbols will easily be lost, through the lack of adequate defined through a function.

The traditional shaped symbols for basic gates immediately convey their function. The new symbols depend entirely on tiny characters to indicate the function; if these become illegible the entire symbol becomes undefined.

Random functions have for a long time now (the symbols depicted by: +, OR, full stop - AND. So why in the space age are we hurried with new, equally ambiguous, symbols? V = G & G & AND. Perhaps V and G make sense in French or some other language, but the space area has been covered in Ren Koo's letter to RF-8213.

Perhaps the changeover period will never happen, and the result that technological progress may have become able to eliminate any need for any symbol. A decade ago, American computer systems were using a hundred different kinds of circuits, each with its own functions on the basis of only input and output parameters. The 'associated' design engineers were unable to utilise even one circuit function, because the CAD had done all the designing, that they had to generate corresponding circuitry.

Maybe one day, CAD systems will be able to design circuits by producing problems, by listing of indubitable black boxes.

Denis R. O'Brien
Lancing
West Sussex

MATHS PUSHERS

From a dictionary of the English language I find: MATHEMATICS (n) a group of related sciences, consisting of the science of number, quantity, space and shape, and the science of logic as developed from these sciences. Thus, it is related to: mathematics, to learn. SCIENCE (n) a systematically organized body of knowledge concerning the material and physical universe; ... (from: Latin: specula-; to look, to see, to learn)...

The Sonic Pathfinder, a spectacle-frame-mounted ultra-sonic guidance system, was the winning entry in the Electronics Category of the 1986 RAE Microwave and Communication Competition.

Despite the considerable interest aroused in the world of the competitors, a manufacturer for the device was not forthcoming. Yet another setback was that, although the design is neat and logical, it failed to meet the Blind Mobility Research Unit at Nottingham University, no funds could be raised to purchase the purchase of devices for the field trials. The proposed field trials involve placing thirty devices blind clients for a period of six months each.

The good news is that things are, at last, widely. Large due to the efforts of the veteran blind ball player Walter Thomsen, a new charity, MOREL, has been created, the aims of which is to give financial help so that blind and disabled people may benefit from electronic aids. MOREL has been created, its first aim, that of raising the money to finance the field trials, has been accomplished due to the efforts of Charles Dunstan, the well known charity for the blind in the green Mobility Centre in Birmingham has agreed to take responsibility for this project. In total, this may also result from noise of mechanical inaccuracies inside the sound originator, and the nature of the sound wave within the wave guide. It is not just a case of the sound coming in the wrong direction, but also the shape of the incident subsonic waves. A B and B signals output from the shield encoder are derived by applying a function to the input signal.

Perhaps the most exciting development is that, at the end of last year, at the invitation of the Royal Guide Dogs for the Blind, the centre took four Sonics Pathfinders out to produce a map of the city. The experiment is a permanent and cumulative error.

Mark Winder
Reading University

WHATEVER HAPPENED TO THE SONIC PATHFINDER?

After reading A. J. Crofts shaft encoder, it followed up in JRF Cl 89, I was perturbed to see yet another shaft encoder idea that will not work properly appearing in your pages. Even more troubling is the fact that I apparently wrote one of these. In fact, the idea is not to find the Blind Mobility Research Unit at Nottingham University, no funds could be raised to purchase the purchase of devices for the field trials. The proposed field trials involve placing thirty devices blind clients for a period of six months each.

The circuits described in JRF for November 1985 (p.71) and February 1986 (p.93) do both give a continuously increasing count for a small mechanical encoder. Therefore, the (ideal) shaft encoder interface must cause the counter to oscillate between two operating states. This is a true reflection of the shaft encoder.

The February version, most likely attributed to me for some, March issue, p.33 - Ed), claims to solve the problem, but it does not. This can be seen by considering the effect of a reversing moment 90 degrees later than the one shown in the circuits. The result is that two counts in the same direction, instead of a single count. Not only may there be false counts with these interfaces on a mechanical basis, but there could also result from noise of the Blind Mobility Research Unit.

For the collection of field trial data, the Portable Test Telescope, the sheltered workshop and the Regional Test Centre, which are for the Disabled in Mainland PortReal, the sheltered workshop and the Regional Test Centre, which are for the Disabled in Mainland PortReal, have established a good rapport. The test was designed for a more or less workable system. As the result of intermodulation distortion does not exist and the receiver is a sound transducer, and if damage to the peripheral hearing cells causes this progressive damage, there is likely that these hearing hair cells are damaged. However, the only to receive signals, not to transmit, they are a part of a negative feedback system employed by the ear to improve the signal-to-noise ratio of the transducer mechanism.

It is possible to sharpen the shape of the hair cell to avoid the loss of tone which occurs on purely mechanical grounds, but necessary if an adequate degree of frequency analysis to be performed — is most probably accomplished by some form of frequency filter, within the brain, in the feedback path to the flanking hair cells.

Interestingly, it has been found that the cochlea also emits sounds, identical to those received, but with a small delay of a few milliseconds, presumably due to the response time lag of the feedback loop, and that in some cases, to a noise signal in the ear, the sounds due to this can be detected, emerging from the cochlear microphonics. Indeed it is the indeed a feedback system in the inner ear, with the comparator element being the acoustically coupled central auditory pathway, and the hair cells in the ear at one or more specific frequencies, this situation can be due, in some cases, to feedback loop interactions. This simple system can be a very high gain differential amplifying circuit. Since an inadvertent increase in loop gain, at this point, is frequently, it seems possible that this could be due to oscillations in the hair cells, so that the projecting cells via a negative feedback loop, giving a greater degree of microphony in the feedback path.

Also, the few milliseconds delay in the response of the feedback loop, noted above, makes the cochlea serve as a rapid automatic gain control in response to the hypothesis — which arose from the observation of evidence, which can be plausibly explained. However, it can be difficult to distinguish between these two different sources of sound. To an electronic engineer with an interest in audio technology, the result of this change in chord could be much more than a change in their ears frequency range — that the craving for unusual firsts. To take for granted that there are no significant effects of missing some of the features. The resulting feeling of freedom to show off noticing the important features. As the Principle of Coherence are merely the result of the fearsome designs.

NEVER may we give us a clue as to where to look to find the theory that the Pringle of the cochlea story is no longer possible, because if that is wrong it will have been proven. Therefore, Newson’s principles being wrong, or it not being permissible to show off noticing the important features. As the Principle of Coherence are merely the result of the fearsome designs.

J.L. Linley Hood
Tuasont
*Professor Colin Blakemore, BBC
Radio 3 Letter

RELATIVITY

I fear that Mr Gerrard (Feedback March 1986) may be in for a shock if he hopes that the process of hardening up will set up a straight choice between classical space-time theory, with victory to the former.

That space and time are both absolutes is a fantastic theory. During the past fifteen or so years I have been working at the US Naval Observatory, Washington, has unequivocally shown the existence of the phenomenon of time dilation. This finding has been a logical branch of classical theory, leaving only relativity on the field, whether the classical theory measured accurately precisely with the predictions of that theory. We have got no other champion of special relativistic theory.

With respect to the "invariance of relativistic" begins in the 1905 paper "On the Electrodynamics of Moving Bodies" Einstein makes it quite clear. After pointing out that there was both theoretical and experimental evidence to suggest that the laws of physics might follow from simple axioms, he considered the more general principle of the invariance of the speed of light.

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RAKE'S PROGRESS

I feel bound to speak for the RAE which has recently expressed views on electromagnetic radiation which are at best eccentric and at worst outrageous.

Mr Cartz claims: (1) that Maxwell's equations only apply to homogeneous bodies: (2) that there is no interaction between nature than the two constants c, the speed of light, and the impedance of free space; (3) that electric field E and the magnetic field H in an electromagnetic wave are coupled as Maxwell's equations imply; (3) Maxwell's equations are correct; (4) the laws of experimentally generated electromagnetic fields.

I can only conclude that Mr Cartz's view of Maxwell's equations stems from his failure to understand the principles of mathematics and physics. He also always bemoans the use of analogies in science, in stating boldly that he is right and most of the scientific community is wrong. This is an untenable position.

Take for example the equations quoted represent a very particular case of Maxwell's equations i.e. the one-dimensional case with no sources charges or currents. The interesting physics of electromagnetism (existence from aerials or even laser beam) and the implications of light etc. from inside out is of course no longer valid. And I am sure we have lost over what does he expect?

Moreover, with regard to point (3), Maxwell's equations are three-dimensional and therefore must be applied in three dimensions, and that there is no magnetic monopoles. Thus these equations can not give physical insight into problems related to something to satisfy the ego of mathematics as Mr Cartz seems to think.

Regarding point (5), Mr Cartz gives a nice, but inaccurately, a moving between a moving tapered plate of a rod and a travelling plane plane-polarized electromagnetic wave with a wedge profile. He claims that this analogy proves that E and H do not interact or are not coupled. The essential point here is that they are coupled as required by Maxwell's equations and this couple determines that their ratio could be anything. Mr Cartz gets his analogy on the basis of visual requirement that the width to height was very narrow, which is an absolute constant. The fact that E is a constant is only an as a consequence of Maxwell's equations and has nothing to do with his interpretation.

The mechanism of the coupling was never explicitly explained. At any point, as it changes it generates a power a perturbative F field by Faraday's law which is an integral statement about the rank-2 electromagnetic tensor (F = dB/dt). As E field changes, it turns perpendicular to the wave vector according to a second Maxwell equation (B = curl E) and the electric and magnetic fields are related by Faraday's law. In a million miles from being misconception.
High-speed interface buffer/2

Using a d-to-Converter output as an address, this buffer interface stores 500 million words in 16Kbyte of memory.

To produce a low-power indication six bits have been made of the 74LS93 register-counter, which goes low when all eight counter outputs are high. When the data word IFF has been reached, pin 11 of IC113 is low.

Gate pin 12 of IC113 now goes high, raising pin 6 of IC127. This only happens during data acquisition when pin 5 of IC108 is high.

If pin 10 of IC108 is now connected to pin 10 of IC106, this converter flag on pin 11 of IC127 will be locked out and data acquisition stops. If this feature is not used, the channel containing data word IFF will be unprotected so all data will be lost in this particular channel. Pin 10 of IC108 can also be used to stop the conversion at any time. Overlay output pin 6 of IC144 goes low immediately after a reset pin 5 of IC144. Resetting pin 1 of IC144 can be done either manually or by computer, as computer-to-buffer connections.

The pseudo converter flag generates the same 900ms sequence as a normal converter flag, but now the remaining IC133 addresses all the memory locations in sequence. When OE is enabled, any value may appear after power-up. All these words are overwritten by data word because, of the clear signal on IC144, this will be the only value appearing on the outputs of IC144 when the bus-driver output is enabled.

This continues until RCO of IC127 goes low, when pin 6 of IC127 goes high and pin 7 sets a pseudo RDRO signal. The same 600ns RDRO operation follows and all memory locations are checked to make sure that they contain zero. This is done with the eight NOR gates IC1.

If any location does not contain zero, bistable output pin 9 of IC127 goes high and stops pin 9 going high again. This pseudo RDRO expands this sequence to 600ns low on line RCO of IC127. During the converter data-acquisition run, the test point must always be high. The entire reset/check procedure takes about 110ms.

Fig. 6. Computer-to-buffer connections. Data is stored in the buffer without computer intervention.

by J.F. van der Walle M.I.E.E.
Computer-to-buffer connection

The illustration of external connections shows how to connect the buffer to the computer. Because of the great variety of computers this is only a general diagram.

If the computer wants to have access to data in the buffer it sends an RDRQ signal, to pin 11 of IC10 in the buffer and simultaneously places the address word in the 16-way data bus.

This read request is processed by the buffer logic (see bus system — data out) and the data belonging to a specific address word is stored in IC10 by clock signal pin 8 of IC10.

Pin 6 of IC10 sets the computer flag bistable device and a Read-data flag is sent to the computer. Immediately, the computer sends an Enable signal to IC14 which also resets the computer flag bistable circuit. Now a data word from IC10 is placed into computer memory through the 16-way data bus.

This procedure is only used for checking contents of a specific channel while data acquisition takes place, Fig. 6.

Block transfer

When a channel in the buffer has collected 25 counts the Data-ready flag is set through pin 6 of IC10. Address-word zero and a Read-request signal to pin 11 of IC10 are sent back by the computer.

From here, the procedure is as above from the Read-request processing point, but pin 6 of IC10 still locks out the converter flag. Address-words 0000 to 1FFF are now seen sequentially, each followed by its own data word, for storing in computer memory.

Address word 1FFF resets the Data-ready flag (pin 6 of IC10) through address-word buffer IC14 and a 13-input Nand gate. The channel has taken in 512 25th data words the converter resumes its data-acquisition.

Conclusion

The buffer-interface has proved to relieve the computer to such an extent that it essentially becomes a stand-alone device. With direct memory-block transfer, the computer is only used for magnetic tape data dumping and display.

Fig. 5. Logic controlling the high-speed buffer-interface, left. Storing of a 25 counts converter data word takes about 900ns.
25 years of man in space

A chronicle of man's achievements in space since Yuri Gagarin became the first man in orbit — and prospects for the future

by David Whitehouse

It is a bright April morning at the Tyuratam Cosmodrome, about 230 miles southeast of Baku in the Soviet republic of Kazakhstan. An ordinary-looking tourist coach pulls up beneath a skeletal steel tower, which supports a 125-foot rocket. Two men, dressed in orange flight suits and white helmets, emerge from the coach, shake hands and touch helmets. One of them climbs a small flight of stairs towards a lift and turns to wave. At the top of the rocket he turns, feet first, a cramped spherical capsule and the door is sealed behind him.

Yuri Alekseyevich Gagarin, born March 9th 1934 near Smolensk, the son of a carpenter and a conventional school teacher for only a year, was about to become the first man in space. In less than two hours he would be back on the ground and his name would be on everyone's lips.

After a short delay due to a faulty valve, the Vostok-1 rocket ignited at 9.07 am Moscow time. The slim of the lift-off, first seen in the week seven years later, shows the rocket's shadow moving over the flat steppe around Tyuratam. "Off we go!" shouted Gagarin.

Breathing a normal atmosphere, Gagarin entered orbit a few minutes later. "The sky," he said, "looks very, very dark and the Earth is blue." He said that zero gravity was very relaxing and a welcome change to the g-forces of lift-off. Two hundred miles about the Earth, the rocketers fire during Vostok 1's first pass over Africa and re-entry begins.

The spherical capsule with Gagarin inside separates from the rocket stage and plunges deep into the atmosphere, glowing red as its protective coating shields the first spaceman from the fiery heat of re-entry. At 13,000 ft, a drogue parachute is deployed, followed by the main parachute at 8,000 ft. In 108 minutes Gagarin has travelled 23,400 miles and lands in a field near Sverdlovsk, watched by a cow and two farm workers. Gagarin had been promoted to major during the flight as it had been announced to the world. The Russians had not only placed the first object in space, Sputnik-1 and a half years earlier, they had also put the first man in space and to many it seemed inevitable that they would also land the first man on the Moon.

President Kennedy's Day of Pigs (ascoincided with Gagarin's flight and, less than two weeks later, Western prestige was further undermined when an Atlas rocket exploded above Cape Canaveral while trying to get the first Mercury capsule into orbit for an unmanned test. Although the United States didn't know it at the time, their one-Mercury capsule was rather more sophisticated than its Soviet counterpart.

Less than a month after Gagarin's pioneering flight, 25-year-old Alan Shepard sat in a Mercury capsule called Freedom 7 atop a Redstone rocket. Unlike Gagarin's flight the world was watching. At 9.34 am, Mercury-Redstone 3 took off and sent Alan Shepard into a 15 minute and 28 second sub-orbital flight. During his brief ride he tested the Mercury systems in preparation for an orbital flight.

Two months later Gus Grissom made a repeat performance of the mission. But in between the two flights President Kennedy delivered a historic speech. Against expert advice, and with the US having only 15 minutes of manned space experience, Kennedy said, "I believe this nation should commit itself to achieving the goal, before this decade is out, of landing a man on the Moon and returning him safely to the Earth." The stage was set; prestige was at stake and space exploration had barely begun. It had been turned into a race for the Moon.

In August, five months after Gagarin's flight, the Soviets made another step. Germain Titov, at 25, was the youngest man ever to go into space. He had made 17 orbits of the Earth. The massive leap from 1 to 17 orbits resulted from the need to land the Vostok 2 craft in the prime recovery zone, which would be overflown every 24 hours or 17 orbits. Titov was the first man to sleep in space and also the first to be spacecuck.

The second year of spaceflight, 1962, saw many barriers removed. In February, John Glenn became the first American to orbit the Earth in Friendship 7 after three launch postponements. Friendship 7 was the first rocket to attract worldwide attention; but, in fact, it was only the tenth American orbit in orbit. After the chimpanzee Enos was recovered from the Atlantic Ocean in November 1961 NASA confirmed that the third and final Mercury suborbital flight was to be cancelled and the astronaut assigned to the orbital mission. So, Glenn, instead of flying the most anonymous Mercury mission, got the flight that the original seven Mercury astronauts coveted most. It was a bitter blow for Deke Slayton who was to have flown the first orbital flight. Before the next Mercury flight he was grounded because of a heart flutters and had to wait until 1975 to go into space. In May, Scott Carpenter became the third man in space and the Earth to go into orbit, but meanwhile the Russians were planning a space spectacular.

At the time, the Vostok 3 and Vostok 4 missions, launched August 11th and 12th 1962, appeared to be a brilliant technical and propaganda success. But the West did not know much about the Soviet space programme and gave the dual Vostok flight more attention and significance than it deserved.

For a short time after Vostok 4 entered orbit, the two manned spacecraft were only four miles apart. But, despite an eminent British scientist predicting a Russian lunar landing by 1965, the close approach of the two Vostoks was not a true rendezvous, since neither had the ability to maneuver from orbit to orbit to effect a true rendezvous. The ability to rendezvous in space, vital to any Moonflight, had yet to be demonstrated.

There were two more flights before the Mercury project officially ended on June 12th 1963. Six astronauts had spent a total of 2 days 5 hours and 27 seconds in space at a cost of 382 million dollars. The US space programme was to move onto the two-man Gemini project. The Russian space programme, however, although the West didn't realise it at the time, was running into serious difficulties.

During the early days of June 1963, rumours emanating from Moscow spoke of the impending launch of a woman into space. More details emerged: a man was to be launched first, to be joined by a woman the following day. Valeri Baikovski blasted off in Vostok 5 on June 14th to be followed two days later by the first woman in space, Valentina Tereshkova in Vostok 6. There is a rumour that Tereshkova was the back-up woman cosmonaut who flew after the prime candidate was incapacitated the day after Bykovsky's launch. True or not, Tereshkova seems to have had a memorable flight; she is said to have pleaded to come home but was kept in orbit for three days. Bykovsky, on the other hand, stayed in space for 81 orbits and 2 million miles, equivalent to travelling to the Moon and back four times! He still holds the record for the longest solo spaceflight and in these days of multi-man missions seems unlikely to lose that honour.

Like Mercury, the Vostok project ended after its sixth flight. Soviet manned spaceflight had cooled down 15 days 22 hours and 31 minutes, 13 days ahead of the US. The fact that no other woman followed Tereshkova into orbit until Sandra Cristovatsky in 1982 lends weight to the suspicion that her flight was simply one more stunt in Premier Khrouchtchev's series of space spectacles. The next one was to be very dangerous and foolhardy indeed.

The newspaper of the West carried banner headlines of the flight of Vostok 1 on October 12th 1964. Before any two-man crew had been into space, the Russians were launching three. Spectacular leap it seemed, but it wasn't. It was probably the most perilous space mission ever undertaken, and all because of Khrouchtchev's quest for new space spectacles to maintain the Soviet Union's psychological lead over the United States in the space race. Two men, three of them having begun cosmonaut training only six months earlier, were crammed into a stripped-down, one-man Vostok spacecraft. There were no space suits or oxygen supplies. Fortunately the mission ended after 24 hours. They may have had something to do with the down fall of Nikita Khrouchtchev, who talked to the crew by phone during the flight was apparently censored in mid-sentence. The only manned spaceflight of 1964 ended safely, but it could have easily been a very different story.

The last Russian space spectacula occurred in March 1965, when the two-man Voskhod 2 was...
launched just five days before the same-minded launch of the first American Gemini mission. The mission launched just over a day and a half after Alexei Leonov became the first man to walk in space. His spacewalks gave the green light to astronauts performing useful work in space and ultimately the Moonwalks. But Leonov had great difficulty in returning to the spacecraft. His spacewalk had ballooned, meaning that he spent most of the 23 minutes 44 seconds outside trying to get back in. From now on he was to steal the show.

The two-man Gemini missions were the second step on their way to the Apollo missions on which the Moonwalks would be based. The spacecraft became increasingly more sophisticated and the techniques and docking techniques more refined. The first Gemini flight was in March 1965, and Gemini 3 with Gus Grissom and John Young onboard was the start of a new chapter in space exploration. Gemini 3 was the first spacecraft to simulate the rendezvous, closer, and return to Earth experience of the Apollo's mission. The Gemini craft had the first ever on-board guidance computer and a 100% oxygen atmosphere. Later Gemini carried in emergency space life-support and unique hard shell system. Ed White became the first American to walk in space during Gemini 4, which also rendezvous and docked with the Gemini rocket. During that mission the two-man spacecraft failed to dock, and Wally Schirra had to make a manual entry of 6g, probably the most stressful entry ever performed. Gemini 4 and 5 took the lead in exploring the environment and space away from the Russians. The motto of Gemini 5 was ‘Climb, or bust.’ It was also the first mission to try and get men to space from the crew, however, failed to achieve the specially constructed targets but did see a rocket lift-off and the wake of their recovery ship. As one newspaper wrote of the flight: ‘Now for the Moon shot.’

Gemini 6 and 7 were in space at the same time and practiced rendezvous, the greatest hurdle for a Moon mission. The rendezvous, docking technique and space experience gained during the Gemini program showed that the United States was becoming a routine, success, was practiced successfully and it was time for the first deployment of the American SSTO. That emergency was provided by Gemini 8, which was commanded by Dave Scott aboard. They were both 26 years old, and they had set a new American record of 42 days in space. Their tank was the first space docking, attaching their Gemini craft to an Agena target vehicle. They did this without a hitch, but when they tried to manoeuvre the combined Gemini-Agena the trouble began. A rogue thruster sent them into a spin. ‘We’re hating off,’ said Armstrong. The two craft separated, but the trouble got worse. Though the Agena steamed, Gemini continued to spin once every second with the possibility of a catastrophic collision. Armstrong again: ‘We’ve got serious problems...we’re tumbling end over end...we can’t turn anything off!’ Analyzing on their backs saying ‘The End’ when they got to the spacecraft there was a sign fixed to say ‘Last chance. No returns. Shelby will close after this performance.’ However, Shelby had cleared the way to a cost of 218.2 million dollars and over 20,000 days in space. It was now to be the time of Aberdeen and Apollo I. The year 1967 was tragic on one space exploration. Four astronauts were dead in their craft on the ground, one on Earth, astronauts Grissom, and White and Chaffe had been carrying out a ground run-through inside an Apollo Command Module. The spacecraft lifted off on a pad 34, a fire, caused by a short circuit and the spacecraft to lift off, was caused by a short circuit and the spacecraft to lift off, was caused by a short circuit and the spacecraft to lift off in seconds inside, showed with Michael Collins how to change orbit rendezvous and rendezvous with Gemini 7. Collins made a spectacular rendezvous inside the spacecraft on the ground, two years later. April 1967 saw the flight of Apollo 4 and Apollo 5, the two manned flights were the first of the Gemini rockets and the Russian rocket was used for ‘union’. It was the first flight on which the veteran command pilot Vladimir Komarov was a member. It was the second time to land around the Moon. Did they still have dreams of a manned lunar landing of their own? Apollo 5 was an Apollo 1968 and 1969, to the year of the Russians. Russia had launched Soyuz 4 and 5 with a one and three-man crew. Both craft docked in space, reaching to Russia’s claim of the first experimental space mission. All eyes were on the Americans and their five new spacecraft for the Moon landing.

It was reuned by Apollo 7 in October 1968. Within a year, two men would walk upon the Moon. Apollo 7 was a 19-day engineering shakeout of every system, the Apollo Command Module and Service Module to ensure their Moonworthiness. Activities and manoeuvres were designed to simulate and reproduce the en-route performance of an actual lunar mission. The mission was a great success and the way was now clear for a non-landing trip to the Moon two months later. But before then the Russians were making a move.

The manned Soyuz 3 went aloft to rendezvous with the unoccupied Soyuz 2. They only got a couple of hours before one of the Russian crew was rushed to hospital. Russia’s new space craft and the Russian word for ‘union’. It was the first flight with a closed-circuit communications.

‘I believe this nation should commit itself to achieving the goal, before this decade is out, of landing a man on the Moon and returning him safely to Earth.’ John F. Kennedy 1961.

Armstrong placed his left foot on the surface of the Sea of Tranquility on July 20, 1969. It was the end of an era, the price of the moon was won and the dream was beginning to fade.

Armstrong placed his left foot on the surface of the Sea of Tranquility at 21ST 3:54 am BST on July 21st 1969. It was the end of an era, the price of the moon was won and the dream was beginning to fade.
Shuttle mission 41C in April 1984. Astronauts Nelson and Van Hoften had just completed repairs on the Solarmax satellite in the background.

space for a two-day mission. It was the first time a space vehicle had ever flown for the first time with men aboard. One of these men was John Young, who was entering space for the fifth time. Nine years earlier he had walked upon the Moon during Apollo 16. He has flown on the Space Shuttle more than once and will fly again.

When the fourth shuttle flight landed on Independence day 1982, President Reagan was there to greet it and declare the space shuttle operational. He went on to direct NASA to investigate a more permanent presence in space. It cannot have escaped his attention that, as he spoke, four Russians and a Frenchman were in orbit aboard the Saluyt 7 space laboratory. Two other men were due to stay in space for what was then a record 211 days.

While America developed its space shuttle, the Soviets had other goals. The history of the development of the Soviet Space Station is not an altogether happy one. The world’s first space station, Saluyt 1, was launched in 1971, but the first crew failed to dock with it and was left to the second crew to take up residence. But this mission ended tragically as they undocked. As an open valve caused rapid decompression and the crew died within seconds. Saluyt 1 was never used again and the redesign of the Soyuz craft took two years.

The next two space stations, Saluyt 2 and Cosmon 537, failed to become operational. Saluyt 3 had improved living and working quarters, but the rendezvous and docking problem remained, and the second crew aborted their mission, docking the end of Saluyt 3.

Saluyt 4 fared better, being occupied for 300 days. Saluyt number 5 was both a scientific and spy platform. Saluyt 6 was a much improved station over its predecessors, with two docking ports. Spacecraft called Progress, basically a stripped-down Soyuz flying on auto, could dock with it to deliver supplies. Soyuz stayed for 367 days, among which flight engineer Valeri Ryumin spent almost a year in space and traveled 150 million miles — further than the distance to Mars!

Saluyt 7, the current station, was launched in 1982 and is even more improved, with strengthened docking facilities. In 1984 a crew of 73 days on record 238 days outboard but there were problems: fuel leaks, damaged solar panels and battery problem. Extensive spacewalks were conducted in 1984 to repair it and in 1985, following a malfunction whilst unmanned, a repair crew had to dock with an essentially dead space station before bringing it back to life.

In 1985 it was abandoned when a crew returned to Earth in a hurry after one of them became ill. It seems unlikely that the ageing Saluyt 7 will be visited again. On February 10 they launched a radically new space station, Mir, which means peace. It has six docking ports and individual cabins for each crew member and, although details are still sketchy, it is a major improvement on Saluyt 7.

In the meantime the space shuttle had become operational, deploying satellites and carrying men and women into space to perform experiments. We have even seen astronauts flying free using backpacks to capture errant and malfunctioning satellites for repair in space or return to Earth. Even US Senators have hitched shuttle rides in space. Although there were problems with space ports and an optimistic launch schedule, the shuttle programme was going well until its 25th flight which, after delays, blasted off from Cape Canaveral on the morning of January 28th, 1986.

The sight of the fireball that destroyed Challenger with the force of a small nuclear weapon only 73 seconds into flight will be remembered by all who saw it. Following the death of the crew of seven, all space shuttles are grounded until the cause of the catastrophe is found. There is overwhelming evidence that a rupture of one of the powerful solid-fuel rocket boosters caused the fatal explosion.

And so, on the 21st anniversary of Gagarin’s flight and the 50th anniversary of the first shuttle flight, where do we go? When shuttle flights resume we will see the construction of a space station during the mid-1990s on which six astronauts will work for up to four months at a time. It will be a quantum leap in space technology.

Beyond the year 2000, attention has turned to the type of space vehicle that will succeed the space shuttle — this time, a totally reusable craft capable of a transatlantic vehicle capable of direct flight into space and passenger flight across the world in an hour. Perhaps may even become a major space-faring nation if its concept of a spacecraft with an air-breathing engine, called HOTOL (Horizontal-Off-Landing) is developed.

The Soviets are also developing their own space shuttle, in two versions. The larger version is very similar to the US design, though less sophisticated. The smaller shuttle, called Buran (snowstorm), seems to be a quick response vehicle of some kind, possibly carrying anti-satellite weapons. The Soviets also have on the pad at their Tyuratam launch base a heavy-lift launch vehicle that will become the most powerful rocket in existence and will be used to place large complexes and payloads into orbit. The problem is that the rocket at the core of this launch vehicle, called SL-X-16, which will also be used to launch the large Soviet shuttle, has encountered serious problems and is holding back their manned space program. When these problems have been overcome, and there are recent rumours that they have, the Russians are poised for some remarkable space activity. It is not inconceivable that they will mount a manned mission to Mars as early as 1992, which is seven years before any possible US mission.

It is remarkable that we have come so far in such a short time. Just eight years separate Gagarin’s flight from the first Moonwalk, and it is only nine years between the last Moonwalk and the first flight of the space shuttle. In this time, the advances in space technology during this space has been breathtaking and staggering. What will we have done when we celebrate 50 years of space in 1996, or even 75 years from now? Will we have bases on the Moon and on the red sands of Mars?
Digital audio editing — 2

by John Watkinson

Penultimate article in this series outlines the mechanisms needed to assemble edits

Samples representing the waveform of audio signals are carried within a video-like waveform by the v.c.r.s in the mastering system. Unlike real video signal, which is broken up into frames and will be edited at frame boundaries, the audio samples represent a continuous signal and it must be possible to perform an edit at any point within the frame. Fig. 1 shows that when the assemble takes place, the out-point of the old recording and the in-point of the new recording are brought together. It is not possible to record a discontinuous pseudo-video waveform on the v.c.r.s, so the solution adopted is to move the samples and the sync pulses can be continuous in the area of the edit.

The edit point may have any position within the video frame, but v.c.r.s are designed to edit at frame boundaries. Fig. 2 shows that the desired effect may be obtained by setting the v.c.r. into record at a frame boundary, and re-recording what is already on the tape up to the edit point, where the new recording will commence. It is not possible to simply switch between the old and new sample streams, as this could produce an audible click at the edit point. Fig. 3 shows that a cross fade in the digital domain requires a multiplier, which changes the sample values according to the gain coefficient supplied. A cross fade can be achieved by multiplying the outgoing samples, by decreasing coefficients, and multiplying the incoming samples by increasing coefficients, then summing together the products. The slope of the coefficient generator can be controlled by the operator to determine the speed of the cross fade. To control the relative levels of the assembled recording the operator has a fader which can produce coefficients for a digital gain control stage in the player sample stream to the cross fade. As explained in an earlier article, data carried in the pseudo-video waveform are interleaved in 35-line blocks in the 1610 format. There will be an unavoidable delay caused by the interleave process in record, and by the de-interleave process on replay. When the recorder is required to begin at a frame boundary, it is necessary to supply the samples to be recorded in advance so that following the interleave delay, they will have the same timing as the recording. This advance of the samples to be re-recorded can only be achieved by playing back the end of the old recording in advance and storing the samples in a memory. The recorder will need to roll past the edit-point twice for each edit, firstly to load the memory, and secondly to perform the edit. This has the added advantage that only one p.c.m. adapter is required to decode and de-interleave the new recording because the old recording can be supplied by the memory. As the cross-fade period can be several frames, memory must be large enough to accommodate the recording until it has completely faded out.

Samples of the new recording need to slip with respect to sync, achieved by manipulating the gain of editor memory as a delay. The delay necessary is not immediately obvious for two reasons. Firstly, the samples from the replay of the new recording will be delayed by the de-interleave process, but they must be supplied in advance by an amount of time equal to the encode delay. Thus the delay needs to be reduced by one encode delay plus one decode delay. Secondly, the low cost industrial v.c.r.s cannot be relied on to accelerate to frame lock at the same rate when they are rolled by the editor. There is a possibility that the recorder and the player will lock up to reference with a one frame time error between them. To overcome this problem, the editor deliberately rolls the player a few frames ahead of the recorder, and delays the playback samples by the corresponding amount. If the player locks up a frame late with respect to the recorder, the editor can detect this by comparing the timescodes from the two v.c.r.s, and the delay can be reduced by one frame, or 1470 samples. Alternatively, if the player locks up frame early, the delay can be increased by the same amount.

As a consequence, the delay given to the samples from the player is a function of the relationship of the out-point and the in-point to the frame timing of the two v.c.r.s, the encode/decode delay at the p.c.m. adapter, and the state of lock achieved by the v.c.r.s during the pre-roll. The editor's microprocessor takes care of the calculations, which do not concern the operator.

A tremendous asset of electronic editing is that the subjective effect of an edit can be assessed using a simulation without changing the recording on any of the tapes involved. The preview mode is identical to the real edit, with the exception that the recorder fails to record, and the operator can hear what would have been recorded via the d.a.c. in the p.c.m. adapter. The in-point and out-point can be trimmed and the cross-fade time changed any number of times until the desired result is obtained by repeating the preview. In the area of edit preview there is a detail difference between the Sony editor and the T.V.C. editor. In the Sony machine, only one area of the recorder out-point is stored, and the editor must roll the player to rehearse an edit, whereas in the T.V.C. unit, the recorder out-point samples and the player in-point samples are stored, and a rehearsal can be carried out from the memory without rolling the tape.

To permit correct monitoring of the rehearsal or at the edit by the d.a.c. in the p.c.m. adapter, there is an additional complication. During the pre-roll prior to the edit, the p.c.m. adapter supplies samples from the recorder which are delayed by the de-interleave process. When the samples from the recorder that were previously loaded into the memory are reached, these must be read out with an advance, to overcome the encode delay. To allow continuous monitoring in this transition, the samples from the pre-loaded memory are subjected to a delay equal to one encode delay plus one decode delay, so that they will be time aligned with the delayed samples from the recorder, even though they are supplied in advance to the encoder. This delay function requires an additional area of memory in the editor. There are three main areas of memory required: the pre-recorded loader data memory, the player timesbase corrector memory and the monitor delay memory.

The complete sequence of events in an edit can now be described with reference to Fig. 4. The in and out-points are located as per Part 1, and the edit process is enabled by the

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Fig. 1. Artificial frame structure imposed on continuous audio samples by the use of pseudo video cannot be allowed to restrict the time accuracy of edits. It is therefore necessary to slide data along with respect to the frame timing to prevent the potential gap shown here from being formed.

Fig. 2. As a v.c.r. can only begin to record at a frame boundary, an edit is possible to allow frame accuracy by re-recording the existing information from the beginning of the frame to the edit point. This old data is stored in memory prior to the edit taking place.

Fig. 3. It is not possible to simply switch between two sample streams because this risks the production of a step waveform. The correct procedure is a short crossfade in the digital domain.
A.P.C. design on the BBC micro

The article discusses the design of a P.C.B. for the BBC microcomputer. It explains the process of creating a P.C.B. and the considerations involved in the design, such as the choice of components and the layout of the board. The article aims to give readers an understanding of the design process and the importance of each step.

The design includes the use of discrete components and integrated circuits. It is designed to be easily sold for the hobbyist market. The article includes diagrams and schematics to illustrate the design process.

The article highlights the importance of choosing the right components for the design, as well as the consideration of cost and space constraints. It also provides guidance on how to create a layout that is efficient and easy to understand.

The design is intended to be used by hobbyists and enthusiasts who want to build their own computer systems. It aims to provide a practical and hands-on approach to computer design, allowing readers to gain a deeper understanding of the components and the design process.

The article also covers the assembly and testing of the P.C.B. It provides advice on how to ensure the reliability of the design, as well as tips on troubleshooting any issues that may arise during the testing process.

Overall, the article offers a comprehensive guide to designing a P.C.B. for the BBC microcomputer, covering the design process from start to finish. It is an excellent resource for anyone interested in computer design and building their own computer systems.
A look inside: computer aided metallurgy – 2

Video processing and computer technology combine to allow automatic analysis of metal crystals

Presentation is a critical part of any computer data display. The data printing format is controlled by the software of the analysis computer and can be designed to suit the needs of a variety of end users. An additional requirement is for the display of the video information forming the source of analysis as well as the final results produced by the computer. This would be easy using two video monitors, but this solution is costly and of limited effectiveness. There are then two alternative ways of showing the two pictures on the same monitor screen at the same time:

- superimpose the text onto the picture of the crystal structure
- split the screen into two parts, one part for the display of the structure and one part for the processing information.

Superimposition is usually not effective on a picture with a high white content, as can be observed by anyone who has watched a badly subtitled film on television. This can be overcome by putting a small border around each letter so that it stands out from the background, but this is a costly solution for only a limited effect.

Because the picture of the crystal structure is aesthetic rather than functional, it is quite acceptable for only part of it to be displayed on the screen at any one time. In this case, the bottom of the picture has been given over to the display of data, achieved by video switching between camera and computer outputs. The first solution of total superimposition is easily implemented by the simple analogue mixing of the two video source outputs; quite acceptable as the signals are synchronized.

An interesting effect of the partial superimposition can be achieved by having the computer output displayed full-screen and gating the camera output video. This allows the processing computer a full screen output if any further information display is required, and also allows highlighting of important information by display within the screen area not used by the camera display. The system was designed with a teaching environment in mind. It would be very useful to have this type of split-screen display so that the output could be fed to a lecture-room c.c.t.v. system for a class of students to witness results.

Split-screen generator comprises a 12-bit counter (IC 19, 20 & 21) and a 12-bit magnitude comparator (IC 22, 23 & 24). The magnitude comparator is designed to indicate when a certain number of lines per frame have been displayed from source 1 and then to switch to source 2. For the time before the count exceeds the set value (again set by d.i.l. switches on the prototype), S1 on IC25 will be enabled, and the video from the camera will be displayed. After the set value has been reached, S2 on IC25 will be enabled, and the video from the processing system will be displayed.

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Video sync stripper. As outlined previously it is required to provide the video camera with sync pulses from the processor system video output. The type of camera to be used with the system will dictate the final form of the circuit. It would be acceptable to take the video sync information directly from the camera video output provided that the processor video display generator can be genlocked.

The extraction circuit uses two op-amps driven into clipping. The first inverts the video and also clips part of the signal. Because the device is powered by -3 volts on the negative rail, the video is further clipped. The second op-amp does the same while inverting the output of the first so that the video information is completely removed. The sync pulses are then clamped to 5V to be TTL compatible. The mixed sync output of the circuit is then complete. Field sync pulses are extracted using the RC filter and are cleaned by IC2b.

Video level detector. Designed around a high-speed operational amplifier, circuit has a high enough slew-rate to cope with a 4MHz input signal (for maximum resolution). The levels of 'black' and 'white' will differ from application to application so the threshold voltage of the comparator can be set to any voltage likely to occur in the video signal. Any level above the threshold will be treated as peak white or logic 0 and any level below will be black or logic 1.

The circuit also registers sync pulses as black level but this is of no consequence because the output of the latch is not integrated during this period. The comparator responds to the video level continuously but the latch has been designed to latch the first black level it sees after it has been cleared. This detects the presence of black within the element. It also means that the latch has to be cleared immediately before the start of the element for meaningful data to be recovered.

System clock generator. All timing considerations of the circuit are based either on the video sync information or on a 4MHz clock. This could conveniently from the clock signal for a dedicated processing system if required. For this system, a VCO has been used to provide the signal but it would be equally acceptable to derive the clock from whatever computer system is to be used. Clock frequency is not a variable parameter and any reduction in frequency results in a reduction in percentage of the video picture processed.

Latch select circuit. The Eight-bit latch select line goes high at the beginning of the first element. The signal needs to change state at some time between the end of the first element and the beginning of the second. To achieve this a retriggerable monostable is used to delay the change of state of this line, as shown in the timing diagram. This is then gated by various other logic circuits to produce the final data clocks for the two serial-to-parallel data latches. Latch A must be clocked when the data from the first sample is present and Latch B is to be clocked when data from the second sample is present.

Serial/parallel converter. The circuit also contains the comparator output latch for the video circuit. The flip-flop D input is determined by the 'data valid' signal, which is only high when a valid element position is encountered. Thus the latch only recognises the presence of a black video sample when the data valid signal is high. The latch can then be interrogated by the appropriate serial-to-parallel converter.
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Channel Capacity
the meaning of Shannon's formula

Shannon's well known theory is statistical in nature, and requires large numbers from which to derive an average result.

Part of section of concentric hypercubes of 2TW dimensions and radii M, corresponding to the transmitted message and S to the received signal.

The communication channel is said to be perfect if there is zero noise, perfect reception, and transmission. This is an ideal situation, and is not realizable. Shannon's formula is analogous to the 2TW hypercubes, and its application in a statistical sense is a significant achievement.

The equation for channel capacity, C, is given by:

\[ C = W \log_2 \left( 1 + \frac{P}{N} \right) \]

Where:
- \( C \) is the channel capacity in bits per second
- \( W \) is the bandwidth in Hertz
- \( P \) is the power of the transmitted signal in watts
- \( N \) is the thermal noise power density in watts per Hertz

References:

Electronics & Wireless World April 1980

Dangers of r.f.I.
The very real problems involved in electromagnetic interference are still relatively unknown to the general public. The problem is complex and the control is understood by only a few in a few specific industries. It is not widely known that substantial reductions can be obtained without significant cost or inconvenience. The key to solving the problem is to recognize that the solution lies in understanding the physical principles involved and applying known techniques.

Optical processing
The development of low-attenuation fiber-optic systems has opened up new possibilities in communication and computing. The use of optical fibers can provide higher bandwidths and lower loss than is possible with conventional copper wiring. This has led to the development of systems that can transmit large amounts of data over long distances, which can be useful for applications such as long-distance telecommunication and data transmission.
Amateur Radio

Morse did the disabled

B.J. Frost, G6UTN of Norwich was interested in reading the comments about the special value of Morse code to the deaf and very hard of hearing. In 1980, he wrote a note to the Journal of the British Inter-societies Communications Association (JIC) about the potential of using Morse code as a means of communication for the deaf and very hard of hearing. Frost's interest in Morse code led to the development of a device that allowed the deaf and very hard of hearing to communicate with others using Morse code. This device consisted of a microphone that would transmit the voice of the deaf or hard of hearing person, and a Morse code transceiver that would then send the Morse code signal to the receiver. The receiver would then decode the Morse code signal and translate it back into audible speech. Frost's device was successful in allowing the deaf and very hard of hearing to communicate with others using Morse code, and it was widely adopted by the deaf and hard of hearing community. The device was also adopted by the general public, and it became a popular way for people to communicate with each other using Morse code. The device was later improved and developed further, and it became a valuable tool for the deaf and hard of hearing community. It was a significant advancement in the communication technology of the time, and it helped to improve the quality of life for the deaf and hard of hearing community. It also helped to break down communication barriers and allowed the deaf and hard of hearing to participate in society on an equal footing with others.
Phase-locked loops

Does the basic p.i.l. shown in the first diagram lock in a wide range when its v.c.o. runs at twice the input frequency? If you answer no then look at the second diagram. In this circuit, f₀ can be set around 2MHz by the potentiometer. Free-running frequency of the v.c.o. is about 4MHz, which is twice input centre frequency f₀. Using an oscilloscope, you will find that lock range BW₀ is around 20% of f₀/2. Although this is less than the usual lock range of BW₁, when f₀ = f₁, it is still wide enough for many users. A second question arises - is BW₀ constant? The answer is no. Duty-cycle of the input frequency, k₁ determines BW₁, where k₁ = t₁/t₀ and t₀ is the duration of the input signal above the average level. From the graph, BW₀ is zero for symmetrical sine waves, when k₁ = 1 and maximum when k₁ = 0 or 1. Range BW₀ is half of BW₁, which is acceptable in practice.

Importance of this special case is that the circuit will lock even if the input signal polarity changes continuously as in a.d.c./a.c. (180° phase shift).

A.R. Moubayed
Autoilight
Aleppo
Syria

Automatic keyboard repeat

Closing the switch for a brief period causes a single pulse at the output, but closing the switch and holding it closed causes a single pulse followed by a delay then a stream of pulses. When the switch is open, non-inverting input to the amplifier is held at ground and output is driven low. The diode and R₀ discharge the capacitor rapidly. Inverting input is held positive with respect to non-inverting input by R₀. Closing the switch sends point Q positive to raise the output so that R₀ charges the capacitor and point P moves toward Q. Releasing the switch before point P reaches point Q results in only one pulse, but if the switch is held, a stream of pulses is produced.

Time before auto-repeat starts is 0.7(R₀C₀). For values shown, delay is about 1.5ms and repeat frequency is 3Hz.

S.J. Kenley
Warril
Merseyside

Oscilloscope bar display

Simple switching and 4:1 d.t.a. converter makes it possible to show up to eight analogue inputs simultaneously on an oscilloscope as a set of bars indiciations.

Multiplexer inputs are selected sequentially by the counter whose outputs feed a simple 3bit d.t.a. converter consisting of three inverters and resistor ladder. Output from the converter provides x deflection for the oscilloscope. Each multiplexer input has an x deflection associated with it.

Mpx x/ pV X/ µpV
0 3V
1 3.6V
2 2.2V
3 0.7V
4 -0.75V
5 -2V
6 -3.6V
7 -5.0V

A small square-wave signal of about 140mV is added to each 1.4V step to stretch out the dots. Dwell time for each point is (4µs) -1 which is 0.4ms. Each spread pulse is about 12500Hz, or 4µs, so there will be 256 cycles in each bar.

This gives eight equally-spaced dots on the x axis.

To improve legibility, a small square-wave is injected into the d.t.a. converter, changing dots to dashes. When a voltage is present on the multiplexer input, the dash is pulled into a bar. On a count of eight, the counter is reset. With inputs limited to 3.5V and the oscilloscope y input set to 200mV, a full-scale signal has 256 lines in 2.5cm and therefore appears as a bar.

R.G. Birkett
Loudon

Led flasher

I haven’t seen leds wired this way before. Current is limited by internal resistance of the gates and total led series resistance is about 8000Ω.

R. Kirwan
Wolverhampton
West Midlands

Electronic & Wireless World April 1986

ELECTRONICS & WIRELESS WORLD APRIL 1986
CIRCUIT IDEAS

Linear voltage-controlled resistance and conductance

Voltage-controlled resistance and conductance give versatility in electronic design. Applications include tuning elements in active filters and variable-gain attenuators. They usually use intrinsic device characteristics like small-signal forward resistance of a diode, which is inversely proportional to junction current, or drain-source resistance of a J-FET; most such methods make use of a very small linear region and have disadvantages.

The first circuit is a linear and accurate voltage-controlled conductance using a four-quadrant analog multiplier and voltage-to-current converter. Assuming that the multiplier input resistance is high enough, circuit behaviour is expressed as follows:

\[ G_{\text{eff}} = \frac{V_1}{V_2} \cdot R_{\text{multiplier}} \cdot R_{\text{VOC}} \]

where \( R_{\text{multiplier}} \) is the multiplier scale factor, usually in 1000 volt.-1, \( R_{\text{VOC}} \) is the converter \( v/o \) transconductance and \( V_1 \) is the signal voltage control.

Using \( G_{\text{eff}} = (R_{\text{multiplier}}/R_{\text{VOC}}) \), a voltage-controlled resistor can be built by making use of a gyration terminated at its output by a voltage-controlled conductance as described above. For this circuit, bottom equivalent input resistance is:

\[ R_{\text{VOC}} = \frac{V_2}{G_{\text{eff}}} \]

José M. Miguel
Escola Técnica Superior d'Enginyers de Telecomunicació
Barcelona
Spain

Simple test equipment for microcomputers

Two easily built test aids simplify fault finding in microcomputer, bus and peripheral hardware.

When a microprocessor involves transferring information over the data bus, instruction op-codes or data are read by the microprocessor from memory, or data is written to memory by the processor. Similarly, data written to or read from input/output ports has to be transferred over the data bus.

To analyse these data bus transfers, the address and control-bus contents have to be viewed simultaneously. The address represents either a memory or i/o port location while the control bus indicates the type of operation being carried out.

To capture and display data bus transfers, a logic state analyser is often used. These instruments have become the mainstay for testing computer systems despite being expensive and physically large.

For field-service or commissioning of an industrial system, simple test equipment often suffices for initial analysis of data bus transfers. As an example, the i/o stages of an industrial scheme may be verified by connecting a simple data-bus analyser to the system and executing either the main control program or a specially written test program.

This allows individual inputs from proximity detectors, control switches and analog-to-digital converters to be read from the data bus and checked against their expected values. Similarly, values may be written to output ports, and any data captured directly from the data bus compared against those detected outside the computer system.

This article describes two simple items of test equipment for use in verifying the kernel elements of a computer and microprocessor data bus values. The description is for Z80 and 6502 family microprocessors but the approach may be extended to any processor by studying their timing diagrams.

For many years, G. B. Williams was a Senior Research Officer in Electronics at the Welsh Laboratories of British Steel working mainly on microprocessor based measurement systems for the steel industry. He spent four years at Queen's College of Higher Education as Senior Lecturer in Microelectronics. Mr Williams is currently a Senior Lecturer in Microelectronics at the Welsh Glomar Institute of Higher Education, Swansea and is the author of a recently published book "Troubleshooting on Microprocessor-based systems."

Using static rams for rom development

When developing programs, flying leads and batteries can be avoided by using a 6116 static ram with a few active components mounted on its back.

Once programmed and powered down, the ram may be removed from the programming unit and transferred to a new circuit without loss of data. Data retention time is more than 10 min with LP3 suffix rams and good quality capacitors.

Note that the ram pins are floating while out of the socket so static electricity prevention measures are needed.

Stephen Teobald
Harborne
England

Fig. 1. This 'free-running' arrangement forces byte 7F onto the data bus when S3 is closed. At reset the processor reads 7F, sees that it represents a no-operation instruction and steps to the next memory location to read the next data byte. This byte is also 7F so the processor steps to the next location, and so on, stepping address lines through every location sequentially. At address FFFF, the cycle repeats.

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NOSP tester

In a microprocessor, free-run mode involves disconnecting the data bus and forcing a no-operation type instruction into the processor as illustrated in Fig. 1. For the 808 the standard NOP instruction is represented by hexadecimal value 00h; to implement this instruction for Fig. 1, all data bus lines into the microprocessor would have to be tied to ground.

An alternative, simpler scheme makes use of the LD A,A instruction which copies contents of the A register back into itself and consequently represents a "no-operation" type instruction. This instruction's code is 0000h, which may be implemented by pulling all the data bus lines high through a 10k resistor network and pulling most-significant line D7 low with switch S0.

The data bus is disconnected from the microprocessor by an external 2-line-in-line set of slide switches; S0 is opened and S2 closed. This disconnects the 808 from the external data bus lines and the LDA instruction is forced into A.

Operation of the circuit is best understood by considering the 808 just after reset. Following reset, the 808 attempts to read the first memory location by placing value 0000h on the address bus and pushing the RD control line low (active). Data read from the data bus becomes the op-code for the processor's first instruction.

With the tester attached, the processor is forced to read the LD A,A instruction, which it duly executes. Now, the 808 program counter is incremented to 0001h, then it and its value is placed on the address bus. From this new location the processor expects to read the op-code of its second instruction. This instruction is again LD A, A as the processor issues address 0002h and executes another read-from-memory operation.

The overall effect is that the 808 issues every possible address from 0000h to 00FFh.

When the processor issues address 00FFh, the next instruction set its program counter back to 0000h and the cycle is repeated. The 16 address bus lines may be considered as outputs from a 16-stage binary counter with line A0 exhibiting the highest pulse-repetition frequency and the most significant.

by implication; if it passes this test, then it is assumed to be functional.

Retraining the NOP tester

Most microprocessor systems do not include the hardware needed to implement the free-run test. Fortunately, in most systems, the microprocessor is in a socket and can be removed. By constructing a suitable harness, the free-run test can be applied to such a system. Figure two illustrates a harness suitable for 820 or 6502 based systems.

For Z80 microprocessors, the true NOP with a code of 0000h can be used. This involves removing the pins from the wire-wrap socket directly to the turned pin socket with the exception of pins 7-10 and 13-15 which are the data bus lines.

Wire-wrap pins for the data bus are cut short and tied together; the common line from these pins connects to pin 29 on the wire-wrap socket (ground). Thus all data bus lines into the microprocessor are held low and the Z80 is forced to execute the NOP instruction.

The processor is unplugged from its socket on the printed circuit board and plugged into the wire-wrap socket. The complete harness then plugs into the vacant socket.

For 6502 microprocessors the only NOP instruction has the value EA, which makes it a test harness; pins 26-33 are cut short on the upper wire-wrap socket, with the remaining half connected across the turned pin socket. Pins 29, 31, 33 and 34 are wired to pin 1 of the wire-wrap socket (ground) and pins 26, 27, 28 and 30 are tied to +5v.

This forces the bit patterns for EA, the NOP instruction into the 6502 device. A forty-way test clip attached to the processor gives access to the various bus signals for checking kernel elements.

Data bus analyser

Information present on the data bus during normal operation may be extracted using relatively cheap, home-built test equipment. This simple data bus analyser is portable and easy to use, and should prove beneficial when testing i/o sections of an industrial control system, or for initial verification of bus activity from a system's components.

Electronics & Wireless World, 1986

Fig. 3. Using the data-bus analyser, information on the data bus during normal operation is easily extracted.

Fig. 4. Z80 memory read and write cycles. Read and write cycles for i/o ports are similar but slightly longer due to an extra wait state.
mainly differ in that an extra clock period (a wait state) is included in the timing.

The analyzer is set for a Z80 by linking S1 to either MREQ or IRQ to enable the upper octal comparator. The qualifying address is set onto the two-eight way diode switches S1 and S2. Link S1 is then selected for either a read or write operation.

Assume that we want to examine the data byte transferred from memory location 1000, during a read operation. Switch S1 is to be tied to logic 1 enabling the comparators for a memory-request operation. Switch S2 is set to logic 1 and address 1000 is set onto switches S1 and S2. Link S1 is set to its read position enabling the input of data to be captured directly from the microprocessor output test using a 40-pin test clip.

When the incoming address agrees with the address provided and that MREQ is low (active), the lower comparator output will go low (active). This is qualified by the state of the RD control line which goes low during the memory read operation.

At the end of the transfer, data bus states are still valid and the RD signal can be used to latch information on the data bus into the 74LS74 octal flip-flops. The information is then displayed on the TIL311 hexadecimal display.

For the memory write operation, link S1 is connected to the WR signal. A valid word value written to the selected memory location is subsequently displayed.

The Z80 has two simple input/output ports. One transfers data from the accumulator of the processor to the I/O bus using the lower half of the address bus to convey the I/O address. The upper half of the address bus, lines A15 to A16, contains the accumulator value and is thus a variable quantity.

For this type of bus transfer, it would be beneficial to ignore the upper half of the address bus and link S1 is included for this purpose. When link S1 is put into its I/O position, the upper comparator is ignored and 74LS74 from link S1, connects directly to the enable input of the input buffers.

The alternative form of I/O transfer uses the Z80 C register to store the address and contents of the B register are ignored on the upper half of the address bus. The instruction format is

```
INC (R) or DEC (R)
```

where R is one of the 28 internal registers.

The contents of the B register are known during a bus transfer, then the data bus value transferred. This instruction format may be captured using all 16 address lines. Alternatively the upper half of the address bus may be ignored and the I/O address qualified using only the lower comparator and 74LS74 connected.

Assume that you want to capture the value read from port P0. Design S2 is set to its IORQ position and S1 set to I0. The upper comparator is disabled and the port address is set on switches S1 and S2. Am I/O position.

When the port address appears on the lower half of the address bus and an I/O operation is indicated by the IORQ control signal and a low state of the I/O bus, the lower comparator would also go low (active). The rising edge of the RD control signal causes the data bus states to be latched into the 74LS74 and subsequently shown on the TIL311 display devices. When writing to an output port, link S1 would be made to the WR control signal.

The analyzer forms a small, low cost kit of test equipment which can be used to capture and display data written to or read from memory locations and input/output ports.

**5682 analysis**

Unlike the Z80, the 6802 microprocessor, is a memory mapped device and as such does not provide explicit memory request or I/O request control signals. Separate RD and WR control signals of the 6802 are integrated into a single RDWR control line which in a logic one state indicates a read operation while a logic zero state indicates a write operation.

Input and output ports are treated as memory locations which dictates that I/O ports form part of the total memory space of the 6802 based system. Timing for 6802 read and write operations is shown in Fig. 5.

**5682**

```
Refering to Fig. 5, for a 6562 system link S1 is permanently made ground to the lower terminals of the comparators because no explicit memory or I/O request signals are available from the 6562. A wait state is therefore taken to be memory transfer.

Link S1 remains in its M position so that all 16 address lines are tied to ground, a memory or I/O address and link S1 is put into its 6562 position. Link S1 is set for a read or write operation. The 74LS74 latch requires a positive going edge to latch the data on its inputs to its outputs and an inverter is hence required to convert the sense of the \( \phi_1 \) clock timing.

To capture the value read from the memory locations, the bus state is supplied from the address EFO40, for example, link S1 would be set to 'R' and address EFO40 set on-eight way switches S1 and S2. Output of the lower comparator goes low (active) when these conditions are satisfied. For read operation, S1 is in the R position and the signal is inverted by gate IC0. Control signal IC1 is inverted by gate IC0 which causes a positive going edge on pin 71 of the 74LS74; this in turn latches the data bus value to the outputs of the 74LS74 which are then displayed.

The write to a memory location or output port is captured in the same way except link S1 would be set to its W position.

**Conclusion**

The data bus analyzer provides an accurate, small instrument for capturing data bus transfers from a Z80 or 6562 based system. The instrument requires about 100mA of current which in the event that it cannot be supplied by the system under test, can be obtained from a separate power supply. Usually however, the system under test has sufficient spare current capacity to power the unit and its supply is taken directly from the processor's supply pins on the test clip attached the processor under test.

Both the NOP tester and the data bus analyzer are simple instruments which can be carried around by field service and communications engineers. Both can provide valuable insight into the operations of a microprocessor based system.

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CIRCLE 79 FOR FURTHER DETAILS.

ELECTRONICS & WIRELESS WORLD APRIL 1986

Fast c-mos gate arrays  
The AV family, three new series of high-speed c-mos gate arrays from Fujitsu, has a typical propagation delay time per gate of only 1.4ns, making them one of the fastest gate-array families available in volume production. The devices combine 1.8m geometry and high gate density with low power consumption for optimized performance. There are 14 device types within the three ranges and all available. Features of the new series include a single supply, typical turn access time of 26ns, and a wide variety of input level options t.t.l. input/output levels, c-mos input level and Schmitt-trigger input. Package options include dip, flat-pack, pin-grid arrays amongst others. The basic AV series comprises five devices with the number of gates ranging from 2560 to 8000 and up to 160 signal pins. The three devices in the AVM series incorporate blocks of ram with the gate array. They are 2 bit deep, 2357 gates with 1Kbit ram or 4040 gates with 2Kbit ram. The special feature of the third series, AVB, is the high output drive capability of 10mA. It is designed with input pull up/pull down resistor options, a c-mos level input buffer and a Schmitt-trigger input, as well as a t.t.l. level compatible input/output. Six devices range from 200 gates to 2050 gates with from 40 to 80 signal pins. The AV family is fully supported by Fujitsu's c-a.d. system which automates l.s.i. design work for error-free fabrication with a short time span. The system performs a complete logic simulation, incorporating a.c. parameters and capacitive loading. Software is available for use on such c-a.d. workstations as Daisy, Mentor and Valid, and a simplified customer interface which only requires logic and test information to complete the design stage. Fujitsu can provide a seven-week turn around from design approval to complete ICs. Power and ground

Learn to make an l.c.  
A training course in semi-custom design has been organized by Texas Instruments Ltd and Daisy Systems in which participants take a real integrated circuit design of their own choice all the way through layout and design to finished circuit which are being produced using Tt's electronic design and layout editor, EEL. To help the promote the use of c.a.d. in semi-custom circuit design, the two companies have set up seminars followed by workshops providing intensive hands-on training on the design of semi-custom products. The Daisy workstation and Tt's EEL combination can reduce the time to produce an I.C. from concept to samples to two weeks. For further details on courses and delivery details contact SemiCustom PCC, Texas Instruments, Manton Lane, Bedford MK41 7PA. EWW 213

PC with Dash  
Dash is the name of a circuit (schematic in U.S. parlance) and documentation system. It enables circuits to be created quickly and because design data is automatically captured, a variety of key documents including net lists, materials list and design check reports, can be printed at will, using Dash post-processors. Features include a high-speed graphics editor, mouse-driven commands to move, copy, erase and draw signals and bus lines. It is possible to "zoom" into an area for closer detail and even move one component about on the design area while still connected; dragging its connections behind. The system incorporates a library of over 1200 symbols (with pin-outs and pin functions) for discrete components, popular families of ICs in t.t.l, c-mos and e.c.t. Symbols may be chosen and then directed to the display by single key-strokes. There is a text editing facility that allows full annotation of the diagrams. If designs require gate-arrays or non-standard i.c.s. libraries created by the semiconductor companies are available on Dash-compatible disks. Symbols for new components can be created easily; 16-pin block symbols can have their pins numbered with functions, power and ground connections in a few minutes. The Dash system, with the aid of optional software, is capable of high-speed post-processing for the creation of net lists, materials lists and design checks. A large design file can be processed in about 30 minutes, which, claims FutureNet, is two to four times faster than rival systems. The system can be networked with other Dash systems or with larger computers for further processing and central data storage and can also be interfaced with most large c.a.d.c.a. systems and so can be used as a "front end" for Application, Cadam/France, Computer Vision, Sci-Cards, Racal/Redac, Spie, Teglas and others.

Up-dated and GM Design recently responded to customers' requests to include surface-mounted p.c.b.s. All the software is designed and written in the U.K. GM Design, 104 Tanners Drive, Kidlington, Milton Keynes MK14 5BP. EWW 211

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The Thurlby OM358 gives any oscilloscope an 8 channel display. Observing many waveforms simultaneously can be essential when analysing sophisticated equipment. Application areas include microprocessor based products, data transmission systems, A to D converters, frequency synthesizers etc. The OM358 is ideal for digital equipment (it can often solve problems that would otherwise need a fast logic analyser) but, unlike dedicated logic test instruments, it is equally suited to analogue waveforms. The OM358 has a bandwidth of 35MHz and 3% accuracy calibration. Each input has an impedance of 1MΩ - 20pF and accepts signals up to ±6V. An 8 channel, 4 channel, or single channel display can be selected with triggering from any channel. Colour data sheet with full specifications available.

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Circle 20 for further details.
Semi-custom linear circuit

An analogue integrated circuit has been developed by Raytheon which contains a variety of pre-designed programmable circuit cells that can be interconnected by the addition of a second (top) layer of metal. The bottom layer of metal is used to fabricate the structural components, including 12 "gain blocks", 55 independent small-signal transistors (16 p-n-p and 39 n-p-n) all capable of 300 V operation, four n-p-n, 100 mA switching transistors, 17 thin-film resistors with values ranging from 12 to 150 kΩ and a tolerance of 5% and 148 aluminum capacitors with minimum feedthroughs, each with a capacitance of only 0.006 µF.

The device is called RL120 and can be used for a wide variety of linear applications. The macrocell gain blocks can be configured as any combination of 6DB, 32 dB or 4304 type op-amps or as 339 or 355-type voltage comparators. The design method can be adapted to most types of c.a./d.c.. workstations.

Raytheon are adapting the Spice suite so that computer circuit simulation will be possible.

Other features of the macrocells are: a low bias current, a rate of 0.022 pA/µsec, unity gain bandwidth to 200 MHz, and a selectable supply voltage range between 2 and 36V. The temperature coefficient of the thin film resistors is 100 ppm. Further details from Raytheon Semiconductor, Ogilvie Road, High Wycombe, Bucks HP12 3DS, EWW 215.

CAE physical modelling system

Chips may be tested and "exercised" at vector rates of up to 10 MHz, using 32 vectors to test CDD7900, a modelling system from Caddx. The user can plug up to 512 vectors into the system in parallel and can generate up to 256 output vectors. A buffer of 256 x 96 bits stores the 512 bit vectors. After a part is initialized, the entire stack of inputs is executed to obtain the proper output for a particular step in the LEC operation. Since the system may have conflicts during the initialization, the circuit is correct at the time of measurement. The instrument is based around a 68010 processor and has 3.5 Mbyte of memory and a 40 Mbyte hard disk. It costs about £45000, Caddx Ltd., Prudential House, Euston Road, London NW1 2JU.
Megacell from Piezsys

A new application-specific I.C. design system has been introduced by Piezsys to make full use of semiconductor technology and c.a.e.c.a.d. As Megacell, Piezsys claims that through is use, it is possible to minimize design time and cost while making the best use of the silicon areas. Using some traditional and database-based methods, Megacell, the circuit designer can compile large structures and, as memories, programmable logic arrays and arithmetic logic units if the precision performance needs are not already met from the Megacell library. The software has been developed by Piezsys to specifications set by its own v.i.s.i. design engineers. They have insisted that the system can be addressed in plain language, is easy to learn, and may be used simply and straightforwardly by electronic design engineers.

To simplify design and to improve the design function, Megacell uses four basic types of cell. Microcells are the low-level logic elements similar to those in other gate-array libraries. Paramacs provide memory and logic function created from parameters set up by the system designer. Supercells, from Piezsys's own library, replicate standard i.s.i.s functions and include some standard portfolio or passive devices and provide sufficient area for complex circuits. Supercell is the only block that can be used directly in the Cadence circuit simulator. The designers can combine or use all the blocks in any area to form a library with a minimum of overhead.

A complete block of a circuit can be defined as a cell and then used in a number of locations. Using a hierarchical nesting system, cell blocks can include all other cell blocks which themselves include cells. There are two methods of data capture. The circuit can be defined as a 'netlist' or it can be input through the circuit diagram using any of the many graphic workstations, like Futurenet, that can handle the Megacell library.

Design verification and simulation and the automatic generation of test patterns is carried out by a suite of software called Classic. This is an event-driven simulation that uses parallel processing to enhance performance and shortened simulation time than Megacell. Classic can accommodate not only "1", "0", "don't know" and "high-level control", but also rising and falling edge detection to help the designer identify possible "race" or "glitch" large cell structures, such as memories. This feature includes the ability to assist designers in developing test vectors and performing fault simulation to ensure the reliability of the design. Piezsys has proven these tools by the successful production of over 2,000 designs during the development process.

Layout and routing are carried out using the Megacell Layout Editor (MLE). The designer can position the cells and MLE will check to ensure conformity with layout rules and the geometry of the printed circuit produced by Classic. Routing of the conductors between cells can be automatic or, if any part of the circuit is beyond the scope of Classic, it can be routed by hand, leaving the rest to autorouting. The system works on a graphics terminal with "mouse" control. Two layers of metallization are used, corresponding to top and bottom layers, and where they cross they may be joined through "via" holes.

Once the layout and routing is complete, checks can be carried out on the capacitive or leakage rate. This test data is fed back to the simulator for further testing. The masks for producing the final chip are generated and checked as well as final test patterns for automatic test equipment.

There are different methods for using the system: the user can get the software and design use it on a Vax computer; the customer can also go to a third-party design house which has the system installed, or get the project designed by Piezsys themselves. The final output and test patterns are then sent to the Piezsys silicon foundry for silicon processing and testing.

Further details from Piezsys Semiconductors Ltd, Cheney Manor, Swindon, Wilts SN2 3QW. E.W 219

Scientific and Card Ediowation

The Stride 440 is a low-cost desk-top workstation for the scientific community developed by Equinox. Built around the 8095 processor running at 12MHz, and implemented in a 3Mbyte of ram, the unit can have an optional floppy disk drive and 3Mbyte of rom. This features both flexible and hard direct drives; the latter with a capacity from 10 to 110Mbyte. A tape backup unit is optional. Single-wire networking of standard and networked systems is available.

Suitable for fast math processing or for card/ace and other engineering applications, the workstation runs the full ANSI-standard Fortan 77. This system exploits the full addressing abilities of the 88095, allowing virtually unlimited size programs as well as providing standard scientific and mathematical structures.

There are language extensions to allow the user to write programs to convert programs written in Fortran 66 dialects. The Stride 440 also supports Unix V, and has been used by Inmos for their implementation of Occam programming for the Transporter. It costs around $90,000.

The software is supplied by Equinox.

Computer Systems Ltd, 114 Curtain Road, London EC1A 3HA, E.W 2 200

Surface-mounting cam

Prepared to share their knowledge of the design, development and manufacturing services for surface mount technology, is Nichelot Interconnect, a company in Haslinghton. They are prepared to show how they can move industry from their surface-mounted assembly operation. Visitors are given a detailed presentation on the processes involved with particular emphasis on the factors affecting yield. These include processing, design, equipment and the quality of both p.e.s.

High-speed Computer Engine

A hard-wired accelerator can dramatically speed up the tasks of a c.a.e. workstation. Mentor Graphics have introduced the Compute Engine that uses some of the latest computer technology. It is a reduced instruction-set computer with parallel processing and has a throughput of 300Mips. This, paradoxically, can provide up to 100 times the speed of processing of a typical workstation. The accelerator can be used in all workstation applications - simulation, placement, routing, design rule checking on data formatting, and unlike some single architecture accelerators. The architecture of the Compute Engine is tailored and designed for the tasks of the user with a single pipeline or high-level language source code into an object code, fully optimized for the engine's parallel processing. The software package includes a complete set of program development tools which allow rapid application development in a standard high-level language. The Compute Engine is priced at £25900 and includes a coprocessor 4Mbyte memory board to fit the Apollo DN50 and DN500 workstation complete with the software application upgrade. 10Mbyte memory boards are available at £34100 and £17900 respectively. Additional software upgrades cost £3800 per application. Mentor Graphics offer similar global accelerators for the entire range of Apollo workstations. Mentor Graphics have a plant in Western Centre, Western Road, Bracknell, Berkshire RG12 1RJ. E.W 225

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