ELECTRONICS & Wireless world
APRIL 1984
85p

Competition award

GPIB combiner
More on the 68008
Synthesized tv modulator
Centronics/teleprinter interface
Testing microprocessors at home

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www.americanradiohistory.com
The range includes sine-square oscillators, synthesized signal generators, function generators and pulse generators.

Designed and manufactured in Britain, all instruments in the range are backed by the Farnell reputation for value for money performance.

Detailed information will be sent if you respond to this advertisement.
Competition award

Microprocessor-based ultrasonic pulse-echo-system depicted on cover is described elsewhere in this issue by Tony Heyes.

NEXT MONTH

Pausaid, a training aid for sufferers from certain motor speech disorders. This device won second prize in Wireless World's recent design competition.

Variable-speed video playback begins a series on combining servo head tracking with digital timebase correction that allows playback to broadcast standard over a wide range of speeds.

Dr Murray chose to avoid criticising Relativity Theory in his recent Heretic's Guide. He makes good the omission by drawing attention to one of Einstein's rare but crucial mistakes.

Designer of WW Scientific Computer, John Adams, describes another computer design, this time a disc-based CP/M-compatible system.

Current issue price 85p, back issues (if available) £1.06, at Retail and Trade Counter, Units 1 & 2, Bankside Industrial Centre, Hoplton Street, London SE1

Available on microfilm: please contact editor.

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THE MIND-FORG'D MANACLES

COMMUNICATIONS COMMENTARY

Video phone • Home video • Amateur radio

SONIC PATHFINDER

by A. D. Hayes

DESIGNING WITH THE 68008 MICROPROCESSOR

by A. J. Barth

CIRCUIT IDEAS

Low-noise oscillator • Reducing crossover • Valve biasing

ASSEMBLY LANGUAGE PROGRAMMING — TELEPRINTER INTERFACE

by R. F. Coates

MATCHED FILTERS FOR RADAR AND SATELLITES

by G. N. Robinson

TESTING MICROPROCESSORS AT HOME

by C. Carson

SYNTHESIZED TELEVISION MODULATOR

by R. Wilkins and L. Cergei

LETTERS TO THE EDITOR

TEMPERATURE • Operating forth • GPIB interface

GPIB COMBINER

by B. Greaves

NEWS OF THE MONTH

Rival des • European electronics desk • Satellite seascaping

AMPAL – REPLACEMENT FOR THE NTSC SYSTEM

Exclusive details of new American colour system

STORAGE OSCILLOSCOPES

Survey of digital storage instruments

NEW PRODUCTS

RF • Microwave • Video filters • Computer products

APPOINTMENTS

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Terms of business: CWO. Postage and packing valves and semiconductors 50p per order. CRTs £1.50. Prices excluding VAT, add 15%. Price ruling at time of dispatch. In most cases, prices of valves and USA valves will be higher than those advertised. Prices correct when going to press. Account facilities available to approved companies with minimum order charge £10. Carriage and packing £1.50 on credit orders. Over 10,000 types of valves, tubes and semiconductors in stock. Quotations for any types not listed. S.A.E.

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Test Equipment

**Philips PM3207 15MHz Oscilloscope £325**
Compact, portable, lightweight oscilloscope designed for field and workshop use. 15MHz bandwidth with 5mV sensitivity. TV and auto triggering from either channel with adjustable level. Add and invert facilities and X-Y mode. Large screen with internal graticule.

**Hameg HM103 10MHz Oscilloscope £158**
This small oscilloscope has been designed specifically for field service personnel and advanced electronic hobbies. Single trace. 10MHz bandwidth with 2mV sensitivity. TV and auto triggering with adjustable level. Internal illuminated and in-built component tester.

**Philips PM3217 50MHz Oscilloscope £850**
High 2mV sensitivity, dual trace. 9 x 10cm display with small spot size. High light output and illuminated graticule, auto trigger mode. TV triggering on line and frame. Full X-Y display facilities. Comprehensive second time base facility. Compact dimensions and low weight. Philips PM3215 Single time base £655

**Hameg HM203-4 20MHz Oscilloscope £264**
Designed for general purpose applications in industry and education. Versatile triggering performance at least 40MHz. Dual trace X-Y operation. TV triggering, add and insert mode and component tester makes the price/performance ratio of this scope most attractive.

**Philips PM3219 Storage Oscilloscope £2675**
Provides comprehensive, cost effective storage of single shot transients and slow frequency events. Variable persistence and variable storage. Auto erase between 1 and 10 seconds, and read button facility. Auto store up to 1 minute, up to 24 hours in 'bake sit' mode. 6mV sensitivity at 50MHz

**Hameg HM204 20MHz Oscilloscope £365**
High performance scope with peak value triggering up to 50MHz. Versatile triggering facilities and variable hold off control. Dual trace, delayed sweep mode. 2 modulation. X-Y operation, internal illuminated graticule and component tester complete the attractive specification.

**Philips PM3256 75MHz Oscilloscope £1245**
Tough, light-weight ruggedised unit, with shoulder strap that can be used in harsh service environments. Fast trigger circuits to over 100MHz. TTL triggering is standard. Trigger view third channel and full X-Y display. Dual trace with 2mV sensitivity and delayed time base. Philips PM3254 Single time base £1145

**Hameg HM605 60MHz Oscilloscope £487**
Outstanding performance with versatile triggering to 80MHz. Sensitivity 1mV to 30MHz and 2mV above. Bright display from 14V CRT. Switchable 1kHz/1MHz probe cable. Dual trace, delayed sweep X-Y operation. 2 modulation, internal illuminated graticule and component tester.

**Philips PM3267 100MHz Oscilloscope £1295**
Versatile and economic instrument designed for advanced electronic environments. Separate main and delayed time base controls with comprehensive triggering facilities and trigger view third channel. Dual trace. 2mV sensitivity, full X-Y display. Z modulation and internal illuminated graticule.

**Hameg HM705 70MHz Oscilloscope £588**
General purpose scope with multitude of operating modes and trigger facilities. Extremely bright and well defined displays, with 8 x 10cm screen and internal illuminated graticule TV triggering, Z modulation, X-Y display facilities and sweep delay mode. Dual trace.
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SINGLE CHANNEL AUTOMATIC GAIN CONTROL AMPLIFIERS

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TAS4862 Gain 28dB adjustable. Maximum output 63dBmV. Power requirement 14V 170mA.

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TSS3662 Gain 12-32dB adjustable. Maximum output 62dBmV. Power requirement 14V 36mA.

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TSD100B3 Band III driver amplifier. 10dB gain. Maximum output 30dBmV Power requirement 14V 10mA.

TSD300UHF UHF driver amplifier. 10dB gain. Maximum output 30dBmV Power requirement 14V 10mA.

TSD1045 Single channel UHF driver amplifier. 10dB gain. Maximum output 40dBmV. Power requirement 14V 10mA. (Quote channel required)

DISTRIBUTION AMPLIFIERS

TLD242 Domestic distribution amplifier. 1 input, 1 output. Gain 26dB. Maximum output 420dBmV.

TLD32B Domestic distribution amplifier. 1 input, 2 outputs. Gain 16dB. Maximum output 2x 39dBmV.

TSD246 40-80MHz. Gain 20dB. UHF VH. Maximum output 460dBmV.

TSD248 40-80MHz. Gain 20dB. UHF VH. Maximum output 460dBmV.

TDD245 Separate UHF/UHF inputs. Gain 26dB UHF, 22dB VHF Maximum output 462dBmV.

TSD254 40-80MHz. Gain 20dB UHF. Maximum output 54dBmV.

TSD260 40-80MHz. Gain 25dB UHF. Maximum output 60dBmV.

TSD565 Gain 58dB UHF, 58dB VHF, 42dB FM. Maximum output 650dBmV.

REPEATER AMPLIFIERS

TSC3660 Repeater. Gain 16-36dB UHF: 10-30dB VHF. Maximum output 60dBmV.

TSC3665 Repeater. Gain 16-36dB UHF, 10-30dB VHF. Maximum output 65dBmV.

TSC3910 Repeater. Gain 10-30dB VHF. Maximum output 80dBmV.

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Telex 354480 INSIGHT GP

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AC/DC Electronic Components

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 Oscilloscope
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 1800 cm/μs
 Variable Persistence
 Superb Condition
 Price: £3,000

 Illustrated with 7603 Mainframe (Extra)

SAVE £2,586
 On New Price

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 These units are unused.
 A4 size. High sensitivity
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 sweep speed — better
 than 70cm/second
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SAVE £637
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 7D01 with DF1.
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 1024 words deep. State
 and timing with up to
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 Price: £2,000

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 Counter/Timer 9514
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 100ns to 10 Sec Period
 IEEE Interface
 Superb Condition
 Price: £850

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 1611A Logic Analyser for
 Microprocessor Based Systems
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 2140A 5MHz
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 Price: £3,000

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 We stock a complete range of
 Plug Ins for use with 7000 and 5000
 series Mainframes.

TEKTRONIX TM500
 SERIES
 We stock a very wide range of these
 versatile modular equipments

MISCELLANEOUS
Avo
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SINEWAVE INVERTERS
FROM CARACAL 200-1000 VA

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Caracal inverters employ modern pulse width modulation technology which is replacing obsolescent tuned-type (ferro-resonant) inverters, by giving higher efficiency throughout the load range, very low standby current, and lower weight.

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Telex: 892301 HARTRO G

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The basis of this considerable advance is the PANTECHNIK 74 Heat Exchanger, designed and manufactured by UK. By eliminating the laminar air flow found in conventional, exotred heatsinks, heat transfer to the environment is greatly enhanced.

For the situation of the 1.2kW amp stems from its division into 4 potentially separate amplifiers of 300W each (downrated with cost savings to 150W). These can be paralleled, increasing current capability or seriesed (bridged in pairs) doubling output capability. In consequence a large variety of amplifier/road systems can be implemented.

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P.S. Spacs, as ever, are exemplary.

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<tr>
<th>Part type</th>
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<td>27128 300ns</td>
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LIVERPOOL L25 3NH
Tel: 051-428 8495

WWW - 062 FOR FURTHER DETAILS

DEC TERMINALS

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TEKTRONIX GRAPHICS

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<td>4D010-1 Terminal</td>
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<td>4D082 Printer</td>
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The mind-forg'd manacles

The affair at Government Communications Headquarters earlier this year goes much deeper than the question of banning union membership. Certainly the ban and its implications for civil liberties may well be a serious matter to some of our readers who work at GCHQ as engineers or technicians. But this dispute is only one immediately obvious sign of a more general and widespread process: the technicization of society — a process that threatens not only liberty but the very existence of democracy in what we call the free world.

If "technicization" only meant gadgets and machines to make life and work easier it would be welcome. But here we mean not just the hardware/software itself but the characteristic mode of thinking and feeling that determines the way the machines and systems are designed, the way they are used and, more recently, the way that people and machines have to interact in complex systems of command and control.

This mode of thinking and feeling is an iron in the soul of technocrats everywhere, East and West: the iron of technical necessity. Given an apparent "problem" in which certain constraints, factors and other data are fixed, there are certain options which can be clearly defined. Rational judgment shows one solution to be measurably superior to the others. It is objectively inescapable and therefore necessary. It has nothing to do with morality, wisdom, compassion or any other such human foibles. It is the "right" solution within its own terms of reference.

Sir Geoffrey Howe said that GCHQ "must provide a service which can be relied on with confidence at all times." Given the political and military premises from which this intelligence gathering system has arisen, Sir Geoffrey's "must" is a technical necessity. And the equally inescapable conclusion is that any people involved in this system must be prevented from interfering with the service it provides, regardless of their motives.

From this, a perfectly rational expedient could emerge: reduce the dependence of the system on human beings. Systems like GCHQ could probably be made less vulnerable by increasing the ratio of machine intelligence to human intelligence. With modern information technology, and expert systems and "fifth generation" computers not far off, this outcome is more than likely.

Responsibility would be centred in the smaller group of people left in charge. They, necessarily, would be absolutely loyal to, and identified with, the system. Like "company men", they would feel a threat to the organization as a threat to themselves.

This kind of process is already happening within the organizations of modern industrial states. It is clearly dangerous. The small number of technocrats in real control of these organizations always have better, more specialized knowledge of what is happening than have the legislators and representatives of the people who are supposedly making the rules that determine our lives. As specialists they are only expected to offer guidance, but this guidance increasingly takes the form of the already-prepared decision, the logical outcome of technical necessity, which the lay legislators cannot reasonably refuse to endorse.

Representative democracy is being undermined by the information-power of technocrats who are not answerable for anything beyond the technical effectiveness of their systems.

Britain, like other industrialized nations, is no longer instinctively understood as a human, geographic and historic entity. In the minds of many it is an economic machine designed to produce a yield, the more efficiently the better. The beginnings of this mental transformation were discerned two centuries ago by William Blake. In his poem London, after speaking of the "charter'd" streets and Thames — places reduced to legal definitions — he exclaims: "In every voice, in every ban, The mind-forg'd manacles I hear."
Narrow-channel tv

Ever since the early experiments in providing two television systems in Germany in the mid-1930s, including the use of 90-line mechanical scanning, the cost of providing the necessary bandwidth has been daunting. Even when a “permanent” Berlin-to-Leipzig tv-telephone service opened in May 1936, public interest was less than expected. With two tv-telephone offices in Berlin and one in Leipzig the cost for a telephone call was 3.50 Reichmarks, but one suspects the service was heavily subsidized.

When Bell introduced their public Picturephone service a decade or so ago it proved a commercial disaster and led most telecommunications authorities to limit their interest to teleconferences for business purposes rather than video telephones. Broadcast-quality television signals need as much bandwidth as about 960 telephone circuits, though a video telephone showing talking heads can make do with about 1.5MHz bandwidth as an analogue signal. British Telecom has been developing a 313-line colour system that uses digital transmission at 2.048Mbit/s, including speech, as part of the European COST 211 project. Analogue transmission of 1MHz analogue 313-line pictures is possible over audio-pairs of telephone lines up to distances of about 1.5km without intermediate repeaters.

A new American system of narrow-band tv has been developed by Widecom Inc. of California. It uses extremely sophisticated bandwidth compression to squeeze the video signal into a data stream of 56kibits/second (i.e. bandwidth about 28kHz) which is slow enough to be transmitted over the standard digital telephone circuits proposed in the USA or with BT’s System X. The aim is to provide a new transmission medium that has video transmission charges no greater than for speech transmission.

Developed under American defence funding, the system provides colour pictures of talking heads, graphs and engineering drawings to a quality standard comparable with that of many consumer video cassette recorders, although quality degrades sharply if the picture is panned, since the system will not cope with fast motion.

The codec can provide bit reduction ratios as high as 1440:1 on video digitized initially at 80Mbit/s. Compression to 1.5 Mbit/s is achieved by removing spectral and spatial redundancies from the bit stream. Further compression uses temporal redundancies by frame skipping, interpolation and conditional replenishment. Compression thus makes use of five processes: filtering and subsampling of chrominance components gives 2.5:1 reduction; a 2:1 sub-sampling in each direction yields 16:1; 2d subsampling in both direction reduces pixel-to-pixel decorrelation yields 6:1; frame skipping and interpolation 3:1; and conditional replenishment 8:1. The current design is based on special Schottky t.t.l. and low-power Schottky t.t.l. devices, since arithmetic and logic operations up to 14-million/sec are required. The 56kbit/s systems are claimed to be already in production for Government and commercial applications. A smaller, lower-cost model is reported under development. Whether the cost of complex processing, together with picture origination and display equipment, could be reduced to the level needed for public video telephone applications remains to be seen.

Home video pay-tv

The first pay-tv system based on the use of video-recording during the downtime of broadcast transmitters has been launched in Chicago by ABC’s “TeleFirst”. The idea is to provide overnight transmission of films in scrambled (encrypted) form for play-out by the subscribers at convenient times. The service aims to provide viewers each month with four major new films, some months before these are released to cable operators, plus 16 to 20 “early release” films at roughly the same time as they are available on film cable channels.

Monthly subscription fee is $25.95, but subscribers can claim a $2 credit for any early-release film they do not wish to record. Home video nets of this type have been advocated as alternatives to cable and DBS by Sony who are supplying the addressable decoders for the Chicago service ($40 per home or $75 installed). Chicago at present has about 17 per cent of homes with video recorders. TeleFirst are selling VHS and Betamax recorders from about $400 with credit facilities.

Meanwhile cable tv continues to grow in the USA. Home Box Office is the major pay television service on the 5200 cable and MDS (microwave distribution system) networks with 13,500,000 subscribers by the end of 1983, a 59% increase since May 1982. Showtime had 4.75 million subscribers on 2900 systems (up 58% in 18 months) with Cinemax on 200 systems and 2.7 million (up 87%) subscribers.

Of the “basic” cable programmes, Ted Turner’s WTBS-Atlanta channel can reach 27.65 million homes on 5717 systems but has been overtaken by the entertainment and sports ESPN channel on 7074 systems having 28.5 million subscribers. Cable operators have been gaining about 400,000 subscribers a month to reach a total of over 34 million or 40.5% of all US television homes.

Twin-oscillator amplifier

M. Nakahama and J. Ikenoue of Kyoto University have proposed a system of linear amplification using a coupled system of two synchronized oscillators with a hybrid element. Experimental verification has been achieved using two 9GHz Gunn oscillators, but the Japanese engineers believe the technique could be applied at optical frequencies between two laser diodes. In the absence of an external signal, the two oscillators are mutually synchronized in antiphase state and output is cancelled at one port. When external signal power is fed from the port, the oscillators change towards an inphase state so that combined power appears at the port in accordance with the input power.

Satellites and insurance

Disastrous successive failures of the booster engines on the two communications satellites launched from the Challenger space shuttle in early February seem bound to have significant knock-on effects on the costs of systems based on geostationary satellites. Insurance pay-out, including loss of revenue elements, has been estimated at well over $150-million.

In the 1960s, during the planning of the Intelsat system, a rule-of-thumb estimate was one failure in five, and this figure continued to be reflected up to about 1980 when, for DBS planning, insurance premiums to cover two launches and in-orbit for two satellites for five years were estimated at about $20-million for a $100-million project.

Insurers, however, are by nature a cautious community and it seems doubtful if today it would be possible to obtain cover on either Space Shuttle or Ariane operations at such a rate. Potential operators and insurers for DBS must also be concerned at the sparsity of in-flight life-data for high-power travelling-wave-tubes, and the relatively small number of vulnerable transponders.

Military and experimental satellites normally do not carry insurance and it is difficult to ascertain what percentage of satellites, particularly in higher orbits, successfully fulfill their mission functions. But it is claimed that for 12 commercial launches in 1983 no insurance claims were made.

OECD before ITU?

The American administration is seeking to involve the Organization of Economic Co-operation (OECD) in the planning of international telecommunications policy and regulation of the radio-frequency spectrum. The aim appears to be primarily to counter the increasing politicization of the International Telecommunications Union by providing a planning forum at American, Japanese and Western European countries could discuss radio regulatory planning and policy in advance of the ITU meetings. However this ignores the major differences between telecommunications administration in Europe and the USA and involves the risk of a further polarization of the attitudes of Third World and Eastern European bloc countries.

The FCC is currently preparing the way for the extension of the American medium-wave broadcasting band between 1605 and
1705kHz. American radio amateurs will use 1900 to 2000kHz, with those communication services currently using 1600 to 1705kHz moving up in frequency. A problem for listeners is that many existing broadcast receivers do not extend up to 1705kHz.

FCC as part of its “deregulation” policy is withdrawing from any disputes over the allocation of call-letters to broadcast stations and will no longer insist that the call-signs should be in “good taste”!

Of the 5000 comments filed with FCC during 1983 on the proposal to issue “no-code” v.h.f. amateur radio licences, only about one in 20 was in favour. The proposal has now been dropped.

AMATEUR RADIO

Sweepers and creepers
In 1959, two Americans, N. C. Gerson and W. H. Gossard at Palo Alto, California reported the discovery of a new form of “atmospherics” that they have termed “sweepers”. They described these as sounding like “clicks, twinks, hisses and swishes” sweeping through parts of the h.f. band. Their paper (J. Atmos. Terr. Phys., vol. 17, 1959, pp. 82-4) speculated that these were in some way connected with Type I or Type III solar bursts. In 1977 two Indian engineers reported (J. Inst. Electron & Telecommun. Eng (India) vol. 23, no. 1, 1977, pp. 19-21) detailed observation of sweepers between 20 and 25MHz, again ascribing the signals to a natural phenomenon. In 1978 I drew the attention of radio amateurs to these sweepers (Radio Communication January 1978). One result was a series of careful observations, including tape recordings, made by Ted Cook, ZS6BT in Johannesburg.

Subsequently a careful analysis was made on professional equipment in the UK of the South African recordings. These proved conclusively that the 25MHz sweepers were not natural phenomena but resulted from long-distance propagation of signals from unstable industrial r.f. heating equipment, nominally operating in the industrial, scientific and medical (ISM) frequency bands.

I see that Norman Fitch, G3FPK has recently reported similar interference in the 14MHz amateur band. There is little doubt that this originates from 13.5MHz industrial equipment, again proving that powerful r.f. generators such as welding equipment can cause interference many miles distant without being converted to an aerial. One of the clues that led to iden-

tification was Ted Cook’s observation that few sweepers were heard in South Africa during the European lunch-hour!

Current industrial equipment includes 12 and 25kW r.f. generators nominally on 13.56MHz and used for such industrial processes as rapid curing of synthetic resin adhesives in the wood industry, etc. It seems surprising that more care is not taken to ensure compatibility and/or absence of parasitics with such high-power “transmitters”.

Grenada aided military
As further details emerge of the activities of 22-year-old Mark Barellella, KA20RK, at the Grenada medical school last October it has been admitted that his transmissions “inadvertently aided US troop movements”. His transmissions were widely monitored by the media and did much to reassure the parents of the American students. The first American amateur he contacted due to the invasion. It reminded him that the USA had no third-party amateur-radio traffic agreement with Grenada. This was waived by FCC but broadcasters were not permitted to conduct over-the-air interviews with him on the grounds that amateur radio rules strictly prohibit the use of the band for business communication. The all-news station, WTOP in Washington D.C., claimed a two-hour “scoop” in reporting that the evacuation of the medical students was about to take place, based on monitoring the transmissions from KA20RK. FCC has subsequently endorsed these activities with James McKinney, chief of the Mass Media Bureau, claiming: “I have not heard an ounce of criticism from anyone about the way the amateurs conducted these operations. Grenada constituted one more shining hour of Amateur Radio public service for the benefit of all Americans.”

Is “amateur” derogatory?
Last year I reported the feeling of some radio amateurs that the University of Surrey’s Uosat project had been directed primarily towards scientific rather than amateur-radio experimentation, and had taken advantage of the facilities of the international amateur satellite service while at the same time had shown surprisingly reluctance to be associated with “amateur radio” in The reason, it later appeared, was that the university disliked the ambiguity of the term “amateur” as defined in the Dictionary of “amateurish” as inexpert, lacking professional skill. The RSWG has which has existed to serve “amateur radio” for so many years, now appears to agree with the views of the university to the extent where it is suggested that it may run a competition to find a better name! Since the Society already frowns on the long-established term “ham” and dislikes being confused with Citizen’s Band activities, and since the term “community radio” is already spoken for, the search may be a difficult one.

Meanwhile the University of Surrey is pressing forward with construction of Uosat-B for an early launch. Again its objectives are largely scientific, and not telecommunications. It would be welcomed more enthusiastically by British amateurs if the University were less reluctant in admitting that the satellite will operate as part of the “amateur” service.

GaAs on 144MHz?
The superior low-noise performance of gallium-arsenide devices compared with silicon devices is well-established at microwave frequencies. But in recent years the reduced cost of some dual-gate GaAs fet devices has led a number of amateurs into using these at the relatively low frequency of 144MHz, claiming exceptionally good strong-signal performance. This claim is disputed by Chris Bartram, G4GDU, of MuTek, who has found that, on measurement, the GaAs devices have third-order intercept points of the order of 40dBm, roughly the same as for good silicon devices. They also have a “bath tub” noise characteristic that results in noise figures at 144MHz slightly higher than at 430MHz. He believes that the idea that GaAs devices provide exceptionally good dynamic range is largely a myth, although one that is already influencing a number of enthusiasts.

In brief
During the flight of the Columbia space shuttle Dr Owen Garriott, W5FL, recorded identifiable calls from 290 stations including about six in the UK. The number of real-time two-way contacts however was Vt is hoped that amateur radio operations will be repeated in some future flights. Problems arising from leakage of cable television signals on frequencies within the 144MHz band have been reported from the British Telecom installation at Milton Keynes. . . . The death occurred last December of Eric “Bill” Yeomanson, G31HR, former president RSGB, who did much to establish the Raynet emergency network and to popularise the use of amateur r.t.t.y. . . . The DTI has confirmed that the installation of transceivers by short-wave listeners is legal provided that they do not use the transmitting facilities . . . Mobile rallies at the University of Leeds on April 1, and Pavillion Gardens, Buxton and Patric Pavillion, Swansea on April 8 . . . RSGB National Convention 1984 at NEC, Birmingham on 28-29 April will include technical sessions and an h.f. convention. . . . A new edition of “The AMSAT UK Guide to amateur satellite operation” is available to non-members of AMSAT for £1.25 including postage (AMSAT-UK, 94 Heron gate Road, Wanstead Park, London E12 5EQ).
The Sonic Pathfinder is designed to give the independent blind traveller information relating to objects in and to the side of his path. It presents only that information relevant to safety and efficiency, and displays the information in an easy to understand format. The device does not aim to provide a surrogate for vision, rather to provide a limited amount of supplementary information over and above that obtained from the user's other senses. In common with all previous electronic travel aids for the blind the aid is not able to provide protection against holes in the ground; consequently, this is a 'secondary aid' to be used in conjunction with a cane or a dog.

General description

During the last fifteen years many electronic guidance aids have been developed by engineers and physicists and introduced to the blind. They have met with almost total failure. In response to the problems so created — namely, that devices which clearly are capable of providing the blind user with much of the information denied him because of his handicap are, nevertheless, found to be unacceptable — the Medical Research Council and the Department of Health and Social Service jointly created the Blind Mobility Research Unit and placed it in the Department of Psychology at the University of Nottingham. Over the years this unit has developed evaluative procedures capable of giving objective measures of a user's performance with any aid, thus enabling us to highlight the shortcomings of existing aids and to achieve an understanding of the informational requirements of the independent blind traveller. The Sonic Pathfinder is an attempt to embody, within a practical device, the many insights gained during the work at Nottingham.

The aid is an ultrasonic, pulse-echo device, mounted on a spectacle frame, and with an auditory display: Fig. 1 shows the aid being modelled by the author. The prime function of the aid is to detect and indicate the distance of any obstacle which lies directly in the blind pedestrian's path. In the absence of any obstruction ahead, it reverts to its secondary function of indicating the presence and range of obstacles to the left and right of the travel path. Like the simpler hand-held Nottingham Obstacle Detector, the aid represents the distance of the nearest object in terms of the notes of the musical scale — one note being assigned to each of the one-foot-range zones. Again, like its predecessor, the aid is a digital device, no attempt being made to provide an analogue signal to give textural information. This is done to avoid information overload. Moreover, if a blind user really wants to distinguish between a tree and a lamp-post he can reach out and discover this by touch.

The user listens to the display through two small earpieces, one mounted on each side of the spectacle frame in close proximity to, though not actually in contact with, the ear. Time division multiplexing is employed between the three receivers and the two earpieces so that the distance of any object which lies, within range, to the left of the main travel path is signalled only in the left earpiece whilst an object to the right is signalled only in the right earpiece. An object which lies directly ahead produces a signal at both earpieces and, in this way, creates a central sound image. In the absence of any obstacle within the area viewed by the aid the display is totally silent.

With the aid in use, the pedestrian is able to walk parallel to the inner shore line — the hedge or wall — by keeping the repeating note at the 'inner' ear at a constant pitch. He is at the same time able to tell when he passes a tree or lamp-post on the outer shore line by the interposition of the occasional note in the other ear; such objects are vital landmarks for the blind. If he encounters an object lying directly ahead, the side information is no longer provided and information relating to the central hazard is presented to both ears. As an additional 'attention grabber' the central display is arranged to have a repetition rate four times that for the side information — some 16 times a second. Only when the hazard is circumnavigated does the aid revert to giving side information.

Early prototypes of the aid were made using c.m.o.s. integrated circuits. A number of these prototypes have been evaluated using blind volunteers and the results have been most encouraging. However, some shortcomings were identified during the evaluation. For example, although users were advised to switch the aid from long range to short range — from 8 ft down to 4 ft — when trying to negotiate narrow openings, they tended not to do so. By changing to a microprocessor-based system it has been possible to develop software information processing algorithms and thereby achieve an automatic adjustment of the range. These techniques are discussed later.

Circuit description

Use has been made of the Intel 8048 family of microprocessors. Referring to the circuit diagram shown in Fig. 2, it is seen that, for convenience of programming, the prototype devices use the 8035 version of the microprocessor in conjunction with an external memory, the 2716, and associated latch, the 74LS373. When the software has been finalized, the program will be masked into the internal memory of the low-power, c.m.o.s., version of the 8048. All outputs are taken from port 1. Those for the two transmitters, T_L and T_R, and that for the display output, are buffered via a Darlington driver. Outputs P11 and P12 are used as control lines for the c.m.o.s.
two-pole analogue switch, the 4052. One pole of this switch is used to select the current receiver transducer and the other to short out one of the earpieces when the side receiver transducers are in use, or neither earpiece when the centre receiver transducer is in use. The analogue receiver in Fig. 3, is based on the LS404 quad amplifier and is designed to have a peak response at 40kHz. I am indebted to Allan Greaves of B.T. Research for suggesting the design of this stage. The output of the amplifier is inverted using one of the Darlington drivers before being fed to input T1 of the microprocessor. Other inputs to the microprocessor are T0, the short/long range switch, and the higher half of port P2 which usually sits high but may be connected to earth via a hex. switch, which is used to select various software options. All timing is derived from the micropro-

Fig. 2. Main circuit diagram of the guidance aid.

Fig. 3. 40kHz analogue amplifier. Amplifier i.e. is LS404.

transmitters are used, convergently rather than divergently splayed to avoid the 'hole in the middle'. Unfortunately, using two transmitters at the same frequency produces a diffraction pattern resulting in the aid having 'corridors of insensitivity'. This is overcome by reversing the phase of one of the transmitters at appropriate intervals. The multiplexing and transmitter phasing is controlled by a single register, named MULTI, such that:

0 0 0 0 0 0 0 0 look left, out-of-phase
0 0 0 0 0 0 0 1 look centre, out-of-phase
0 0 0 0 0 0 1 0 look right, out-of-phase
0 0 0 0 0 1 1 look centre, out-of-phase
0 0 0 0 1 0 0 look left, in-phase
0 0 0 0 1 0 1 look centre, in-phase
0 0 0 0 1 1 0 look right, in-phase
0 0 0 0 1 1 1 look centre, in-phase
0 0 0 1 0 0 0 RESET TO
0 0 0 0 0 0 0 look left, out-of-phase
For each step of MULTI the transmitters are activated for a 0.5 ms burst of 40kHz. Precise frequencies, both in-phase and out-of-phase, are obtained from software loops controlling the appropriate bits of the output port.

During the transmitter pulse and for a short time afterwards the receiver must remain off. This the 'dead time' is necessary to prevent the receiver from triggering due to cross-talk. For short range pulse-echo systems it is necessary to set this time to a minimum value. However, this minimum is critically dependent upon component and wiring layout and is therefore difficult to pre-set. Using the microprocessor it has been possible to write a software routine which uses the first twenty-four transmission pulses after switch-on to 'dynamically' determine and set the minimum usable 'dead time'.

The elapsed time between the transmitter pulse and the receipt of the first echo determines the musical note displayed to the user. The notes are obtained from a software timing loop, the parameters of which are obtained from a 'look-up' table.

Interference from other ultrasonic sources has been largely eliminated by the inclusion of a software-controlled digital filter: the processor has a cycle time of 2.5 Jis. The output of the analogue receiver amplifier is sampled every 4 cycles until a change is detected, confirmatory samples then being taken every 5 cycles, provided each one is the inverse of its predecessor; if not, after a 3-cycle delay, the 4-cycle sampling is resumed. This mixture of 3, 4 and 5-cycle sampling ensures that any 40kHz waveform is detected, no matter what its phase relationship to the internal clock of the processor. By requiring nine successful samples before an echo signal is regarded as genuine, the digital filter has an effective bandwidth of 6kHz cycles. This is more than adequate to cater for the Doppler shift introduced in the frequency when the user is approaching the object from which the echo is received. For example, at a walking speed of 5 mile/h the receiver will detect a change of 40kHz, i.e.

Priority is given to objects in the centre of the user's path – Centre Echo Priority – by failing to increment MULTI when a central echo is detected. And, if after a period of repeated central echo an echo is not detected, bit 2 of MULTI is complemented and one last 'look' is taken in the centre, this time with the opposite transmitter phase inter-relation, before the aid reverts to its left/right scanning mode.

Information-processing algorithms

The difficulties encountered during the evaluation by users trying to negotiate narrow gaps may be illustrated with reference to Fig. 4. The figure depicts a plan view of a subject standing still and facing an open doorway leading onto a corridor. Very small rotations of the head produce three different musical notes: a note of low pitch corresponding to the distance to the far doorpost the centre-echo-priority algorithm ensures that these notes are presented to both ears, giving no obvious impression of the existence of a gap. Furthermore, very small head movements produce a jangling sound which is very difficult to interpret. (The user will only realize he is facing a gap when he notices that one of the notes has a higher pitch than the other two!) How much better the information display would be if the aid had a maximum range greater than d2 but less than w! If this were the case small head rotations would produce a note of low pitch corresponding to distance d1, a note of higher pitch corresponding to distance d2 and a middle position in which these two notes are presented alternately to the left and right ears, giving an unambiguous indication of an opening in the centre.

It has been found possible to achieve this desirable display by the introduction of an algorithm which I have named the Ratchet. Essentially the action of the Ratchet is to reduce the range of the aid to that of the nearest object in the central region and to maintain this limited range for a certain time, the Ratchet hold time. In order to avoid numerous undesirable side-effects certain constraints must be placed on the Ratchet algorithm. For instance, referring to Fig. 4, a crude Ratchet with a hold time greater than, say, 2 seconds would result in the near doorpost – the note corresponding to the distance d1 – alone being displayed. This seems inappropriate, since the far doorpost – distance d2 – is sufficiently close that it could be encountered within the 2 second hold time, even if, as in this case, the subject is moving from a standing start. Consideration of walking speed, acceleration and reaction times have led to the action of the Ratchet being restricted to the four outer zones of the aid. Thus the Ratchet never reduces the range of the aid to less than 4 feet.

A careful choice of Ratchet hold time is crucial if other undesirable side-effects are to be avoided. In the above example a Ratchet hold time of 2 seconds was chosen, a duration long compared to the time taken for the user to make head rotations but short compared to the time required to negotiate the doorway and move into the comparative open space of the corridor. Although in these circumstances the choice of 2 seconds for the Ratchet hold time is appropriate it does, however, produce one unfortunate consequence. If a user is using the side signal of the aid in order to maintain a travel line parallel to the shore line at a distance of 3 feet, and if he were momentarily to rotate his head towards the shore line, the Ratchet would immediately be invoked and the range of the aid set to 4 feet (4 feet, not 3, because of the restriction described above.) Thus from that moment, for the duration of the Ratchet hold time the user has only the protection of an aid with a range of 4 feet. In these circumstances this is serious because he is not moving from a standing start and may be travelling at 4 mile/h! The solution is to use a Ratchet hold time proportional to the time the invoking object remained in 'view'. Thus a quick 'glance' towards a near object would produce a hold time considerably shorter than would a prolonged 'stare'. It does, however, remain necessary to limit the Ratchet hold time to some maximum value – 2 seconds seems to be appropriate.

Having made the Ratchet hold time dynamically determined one has, in effect, produced an aid, the range of which is governed by the walking speed of the user. That is to say, instead of an aid with a range of 8 feet, we have an aid with a range of 2 seconds! Rather an odd concept. However, given the information-processing demands inherent in independent blind travel and the moment-to-moment problem solving nature of blind travel it would seem highly desirable to have an aid which was limited to providing informa-

**The author**

Tony Heyes is a Senior Research Fellow with the Blind Mobility Research Unit, Department of Psychology, University of Nottingham. Trained as a physicist, Dr Heyes went blind while researching into crack propagation at the Cavendish Laboratory, Cambridge. After eight operations the sight of one eye was saved and a new research interest created. Dr Heyes received a Ph.D. in Physics from Cambridge in 1967 and a second Ph.D. in Psychology from Nottingham in 1979.
tion solely about those objects which would be encountered during the next 2 seconds of travel.

Figure 5 illustrates what may happen when our blind subject takes a pace forward. Large head rotations are now required to bring the door posts into the central region of the aid and there is a high probability that the Ratchet will be released before the doorway is negotiated. When this happens the aid returns to having an 8 foot range and the Centre Echo Priority algorithm ensures that the musical note corresponding to the corridor wall is displayed rather than the side information about the door posts. The undesirable effect may be eliminated by yet another information processing algorithm - the Clamp.

The Ratchet can only be invoked and sustained by signals received in the central, forward facing receiver. The Clamp, on the other hand, may be invoked and sustained by any signal received in the nearest zone of the aid (zone 1) whether left, right or centre. The Clamp operates for a fixed duration (1.2 seconds) and has the effect of reducing the aid to a single-zone device. By increasing the length of near zone to two feet and reducing the ranges of the other zones so that the overall range of the aid remains equal to 8 feet the Clamp provides an effective solution to the problem described with reference to Fig. 5. The presence of one or the other door post in the side regions of the near zone prevents the far corridor wall from being perceived no matter how slowly the

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**Fig. 6. Flow chart showing information processing in Sonic Pathfinder.**
Designing with the 68008 microprocessor

A member of the 68000 8/16/32 bit processor family, the 68008 has an internal 32-bit architecture and an eight-bit external data bus. This second article shows how it is used with other microcomputer components - rom, ram and peripheral devices.

Interfacing the 68008 to memory, peripherals and other microcomputer devices is straightforward. The examples shown here are practical circuits using the popular 74LS z.t.l. family. When the separate examples are brought together to form a complete system numerous circuit rationalizations can be made. In the case of very high volume designs f.t.l. tends to be replaced by custom circuits.

68000 with rom

A practical minimum 68008-based system could employ one 8kbyte rom to contain program code and reset vectors. Fig. 3 shows the 68008 interfaced to an 8kbyte rom, MCM68764. The eight-bit data bus and the low-order address lines of the MPU are connected to the rom on a one-to-one basis. The high-order address lines are used to allocate different portions of the one megabyte address space to various memory and peripheral devices in the system. A 74LS138 1-of-8 demultiplexer is driven by these lines to generate a chip-select signal for each device. The demultiplexer is enabled by the 68008 address strobe signal (AS) which indicates when a valid address is on the address bus.

During a read operation on the rom the m.f.u. sets up the read/write signal (R/W) and places the appropriate address on the address bus. Signal AS is activated by the processor enabling the demultiplexer to chip-select the rom. As part of the asynchronous bus cycle, hardware must activate data-transfer-acknowledge (DTACK), to indicate to the processor that data from the rom will shortly be valid on the data bus. A 74LS175 quad D-type flip-flop acts as the DTACK generator for the rom. The rom chip-select signal EROM/CS releases the flip-flops from their cleared state which allows a logic zero to propagate from one Q.

Fig. 3. 68008 interfaced to rom.

Asynchronous data bus enables the bus cycle time to be re-tuned to the speed of the currently accessed memory or peripheral.
output to the next on successive rising edges of the 8MHz clock. The fourth Q output generates the active low DTACK which signals the 68008 to read the data on the data bus and to terminate the bus cycle. The DTACK delay time is governed by the number of flip-flops and the frequency of the clock, and is chosen to suit the rom access time (approximately 450ns in this case).

In this example the R/W signal and all of the high-order address lines have been included in the rom chip-select logic. This enables the detection of illegal operations such as writes-to-rom and access to some unused memory space. In a price-sensitive product this may be considered a luxury and the inverter and the five-input or-gate could be omitted.

**68008 with ram**

Interfacing the 68008 to static ram is similar to the rom case except that the read/write signal connects directly to the ram or rams and is not included in the chip-select logic. Dynamic ram interfacing is more complex because they require refreshing and address multiplexing logic. Fig. 6 shows the 68008 connected to eight MCM6664 4Kbit dynamic rams providing 64Kbytes of read/write memory. The D input and Q output of each dram are connected to a different 68008 data line – only one dram is shown in Fig. 4 for clarity. The 16 low-order address lines are multiplexed together using two 74LS257 quad two-input multiplexers to form the row address and column address needed by the drams.

Like the rom circuit a 74LS175 quad D-

**Fig. 4. 68008 interfaced to ram. High-density rams require the m.p.u. address to be multiplexed into a column and row address**

- type flip-flop is used as DTACK generator. Where the ram and rom, or any other device used, have the same data access time a single generator may be used for these devices. If a single generator is shared among several devices having different access times much of the benefits of an asynchronous bus are lost since the processor executes an unnecessarily long bus cycle for the faster devices. However, in a very price-conscious design where minimum device count is paramount, this may be an acceptable engineering compromise. As well as generating the ram DTACK the 74LS175 also provides the dram control signals, row address strobe (RAS), column address strobe (CAS), write (W), and the switching signal SEL for the multiplexers. AS, R/W and data.

**Fig. 5. 68008 dynamic ram refresh controller. The MCM6664 64K drams use a simple pin-1 refresh technique. Here the m.p.u. operation is temporarily suspended while a block of eight internal memory rows are refreshed.**
Fig. 6. 68008 with M68000 type peripherals have on-chip DTACK generators which provide the return handshake signal for the asynchronous data bus.

68008 with M68000-type peripheral

Many M68000 peripheral devices have 8-bit data buses and some may be configured for eight or 16-bit buses. In these cases the data bus lines D0-D7 are connected on a one-to-one basis with the 68008 data bus. For the few peripherals with only 16-bit buses, a 16-bit interface can be constructed using two octal transceivers and a couple of gates.

Fig. 6 shows a typical interconnection between the 68008 and the 68230 parallel interface/timer (PI/T). The PI/T register select inputs (RSi) are controlled by the low-order address lines A16-A15. Note that address line A15 is not used in this example. While it is quite acceptable to use A15 making it a “don’t care” places the byte-sized internal registers of the PI/T on 16-rather than eight-bit boundaries in the memory map. This preserves complete software compatibility with programs.
written for the 68000 m.p.u. (which does not have an external A6 signal). M6800-type peripherals have an on-chip DTACK generator so the DTACK pin is connected directly to the 68008 DTACK, and may be or-wired with the DTACK signal from other peripherals. The interfacing of interrupt signals is described later.

**68008 with non-M68000-type peripheral**

Non-M68000-type peripherals do not have on-chip DTACK generators and are usually accessed synchronously using the M6800-peripheral signals enable (E) and valid peripheral address (VPA). Fig. 7 shows the interconnection of the 68008 with a 6850 a.c.i.a. Each time such a device is accessed during a m.p.u. bus cycle, the 68008 VPA input is used for the returning handshake instead of DTACK. VPA signals the 68008 to perform the current bus cycle synchronously. Data transfer is made on the falling edge of the E clock which the 68008 provides for the peripheral. A J-K flip-flop (1/2 74LST73) generates VPA whenever any M6800-type peripheral in the system, such as the a.c.i.a. is chip-selected. A second flip-flop provides a valid memory address (VMA) used by many of these devices.

**68008 interrupt logic**

Fig. 8 shows the interrupt connections for a typical small system. A M6800-type peripheral (68230 P/T) uses interrupt priority level 7 for its parallel interface and level 5 for its timer. A M6800-type peripheral (6850 ACIA) uses level 2. The three interrupt request signals (PIRQ, TIRQ and ACIAIRQ) are priority encoded by the 74LS148 priority encoder which generates a three-bit binary number corresponding to the interrupt level. Two bits of the three-bit number are presented to the 68008 via its interrupt priority level inputs IPL1 and IPL0/2. These input pins indicate the encoded priority level of the peripheral requesting an interrupt. The 68008 uses three pins to encode a range of 0-7 but due to pin limitations only two pins are available on the 68008. By connecting the IPL0/2pin to both the IPL0 and IPL2 inputs internally the 68008 encodes values of 0, 2, 5 and 7. Level zero is used to indicate that there is no interrupt depending and level seven is a non-maskable edge-triggered interrupt. Except for level seven, the requesting level must be greater than the level contained in the processor status register before the 68008 will acknowledge the request.

Interrupt acknowledgement (IACK) is indicated by the processor function code outputs FC0, FC1 and FC2 all logic high. The address lines A1, A2 and A3 contain a three-bit binary number corresponding to the interrupt priority level being acknowledged. In Fig. 8 a 74LS138 1-of-8 demultiplexer decodes the individual IACK for each peripheral device (IACKx). For M68000-type peripherals IACKx is connected to an input pin on the peripheral for this purpose (e.g. PIACK or TIACK on the 68230 P/T). When this input is activated the peripheral places the vector number (binary 0-255) on the data bus and then it activates the DTACK signal. The 68008 reads the vector number and uses it to nd the start address of the required interrupt handler from its interrupt vector table. Non-M68000 peripherals, not capable of this vectored interrupt method, need hardware to provide the v.p.a. signal. Asserting VPA during IACK signals the m.p.u. to use one of the autovectors to find the appropriate interrupt handler. The nand-gate J-K flip-flop used as VPA generator here is the same as that in Fig. 1.

**Other circuit elements**

No special multi-phase clocks are required by the 68008. An SMHz t.t.l. clock generated from a crystal and several inverters is sufficient. A double-frequency master clock is useful for producing certain timings such as those for controlling dynamic memories. A watch-dog timer should be used in asynchronous microprocessor systems to detect attempts by software to access non-existant memory. It may be constructed in similar fashion to the DTACK generators shown but connected to the 68008 bus error input (BERR). Its time-out period should be longer than the slowest memory or peripheral device in the system. Power-on reset logic could comprise a 555 timer and several invertors.

**Microcomputers as 68008 peripherals**

Low-cost single-chip microcomputers, like the MC6805 family, may readily be connected directly on the bus. E.g. the MC6805 has internal 8-bit processor and peripherals, and can be connected to the bus through an external interface. The MC6805 has an 8-bit processor and can be connected to the bus through an external interface. The MC6805 has an 8-bit processor and can be connected to the bus through an external interface. The MC6805 has an 8-bit processor and can be connected to the bus through an external interface. The MC6805 has an 8-bit processor and can be connected to the bus through an external interface.

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**Motorola peripheral devices**

- 6821 PIA Peripheral interface adapter
- 6822 IA Industrial interface adapter
- 6829 MMU Memory management unit
- 6835 CRTC Mask programmed c.r.t. controller
- 6840 PTM Programmable timer module
- 6844 DMAC Direct memory access controller
- 6845 CRT CRT controller
- 6847 VDG Video display generator
- 6850 ACIA Asynchronous communications interface adapter
- 6852 SSSDA Synchronous serial data adapter
- 6854 IADC Advanced data link controller
- 6872 IPC Intelligent peripheral controller
- 6853 HIM Bus interrupt module
- 68230 PIT Parallel interface and timer
- 68440 DDMN Dual direct memory access controller
- 68450 DMAC Direct memory access controller
- 68451 MMU Memory management unit
- 68452 SAM Bus arbitration module
- 68454 IMDIC Intelligent multiple disc controller
- 68459 PDL Phase-locked loop
- 68499 GPAI General-purpose interface adapter
- 68501 MPC Multi-protocol communications controller
- 68552 DUSC Dual universal serial communications controller
- 68564 SIO Serial input output
- 68590 LANCE Local area network controller for Ethernet
- 68652 MPPC Multi-protocol communications controller
- 68653 PGC Polynomial generator and checker
- 6866 IPEC Enhanced programmable communications interface
- 68681 DJIAR Dual universal asynchronous receiver/transmitter
- 68802 LNET Local area network controller
- 68901 MFP Multi-function peripheral
- 14424 A to D Microprocessor compatible a-tod converter
- 14681 RTC Real time clock + ram

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APRIL 1984

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www.americanradiohistory.com
Low-jitter crystal oscillator

While constructing digital audio equipment, a need arose for a very low noise 12MHz crystal oscillator with t.t.l. output. Designs using logic gates have too much jitter so I developed this circuit comprising a conventional crystal oscillator, buffer and t.t.l. comparator. The oscillator must be well shielded and its separately-stabilized power supply introduced via feed-through filters.

D. G. Malham
Department of Music
University of York

Serial data-frame converter

My requirement was for converting eight-bit serial RS232 data into seven-bit data serial data. Input to the first uart is converted to t.t.l. level by a 7400 i.c. instead of the usual 1489 receiver to save money. I wanted a fixed data rate of 300 baud but simple switching on the 4702 generator inputs allows other data rates to be selected.

Serial data enters the uart on the left at input RRI; this uart is set for eight-bit serial data words. Parallel data passes from this uart to the second one under handshake control between the data-received output, DR, and transmitter-buffer register load input, TBRL, and between the data-received reset input, DRR, and transmitter-register empty output TRE. A 74121 monostable i.c. is included to comply with timing requirements. The second uart is set for seven-bit serial data words and transmits through a 1488 driver at output TRO. Inclusion of switches allows data frames to be set to any combination and the circuit is easily modified for two-way communications.

Stephen Evans
Cradley Heath
West Midlands
Reducing op-amp crossover distortion

Crossover distortion in op-amp push-pull outputs operating in class AB mode worsens when driving low impedance loads at high frequencies. But fortunately the output can usually be forced to work in class A mode, as shown here where an op-amp connected as an inverter has an external current sink. Operating mode of the op-amp is changed considerably. The n-p-n output transistor $T_1$ is forced to carry a quiescent current equal to $I_m$, while p-n-p transistor $T_2$ is switched off as long as $I_{out} > -I_m$.

Bearing in mind that 741 output current is limited at about 16mA, $T_1$ continuous current should be set so that maximum undistorted output swing $I_m$ is less than 8mA. Advantages are absence of crossover distortion, reduction of other forms of 741 distortion due to higher operating current of $T_1$ and increased phase margin of the whole amplifier since slow lateral p-n-p output transistor $T_2$ is removed from the signal path. Disadvantages are an increase in quiescent current and reduced output swing. Distortion reduction using this technique ranges from 20 to 40dB.

Giovanni Stocchino
Rome
Italy

Alternative biasing for valve amplifiers

In this configuration, i.e. voltage regulators allow accurate setting of quiescent current and maintain the setting for the life of the valve. Another important feature is the absence of d.c. in the transformer primary winding which minimizes core distortion. Regulator input current is

$$I_{in} = I_{out} + I_q = \frac{V_{out}}{R_t} + I_q$$

Quiescent current drawn by the regulator, $I_q$, is typically around 7mA for a 7805 regulator and varies by only between 1 and 1.5mA for a 20V input change. Cathode current is the same as the regulator input current and is solely determined by output voltage and load resistance, both of which are constant. Values shown are those used to convert my Leak Stereo 20 amplifier.

J. S. Spicer
Melbourne
Australia

Precise single pulses

Referring to D. A. Haines' circuit in the November 1983 issue, precise single pulses equal in width to the clock period can be obtained using only two D-type bistable i.c.s.

A. Dhurkadas
Cochin
India
Assembly language programming

Centronics-to-teletypewriter interface

In this final assembly-language application, Picotutor's processor is turned into a low-cost interface for driving a teleprinter from a microcomputer. But you don't need to know anything about assembly-language to use this simple circuit.

Bringing concepts introduced in previous articles together, this final application example is a larger project for driving a Creed teletypewriter from a Centronics parallel interface such as found on most microcomputers. Software for the interface was developed on the Picotutor assembly-language trainer. If you have a later version of this kit, software for the interface is already programmed in; those of you with earlier versions can have your processor reprogrammed for a small charge. For readers just interested in the interface hardware the preprogrammed processor may be obtained separately.

Teletypewriters - used by British Telecom for the Telex service - have been around for many years and have remained almost unchanged in design. Many find their way on to the amateur-radio surplus market and are widely used by amateurs for 'radio teletype,' often known as r.r.t.y. Being readily obtainable and cheap they represent an ideal low-cost printer for a home computer. A Creed 7E teletypewriter was used to design the prototype but other models should be just as easy to adapt. Printing is on 216mm-wide plain paper in roll form.

There are two main design problems when interfacing a teletypewriter to a microcomputer. For compatibility with signals transmitted over telephone lines, teletypewriters are designed for use with high-voltage drive signals. Secondly, serially-transmitted data used to control teletypewriters, called Baudot, is quite different from ASCII code sent in parallel form (i.e. more than one bit at once, in this case eight) through the Centronics interface. The first problem is a hardware one and easily solved by replacing the original drive circuit in the teletypewriter, both RS232 and TTL levels are accepted by the circuit presented. The second problem is taken care of by the MC68705F3 single-chip microcomputer used in Picotutor.

Printer interface

The Dragon Computer printer interface on which the prototype was based is a Centronics type, devised by printer manufacturer Centronics Data Computer Corp. It sends characters to the printer one at a time under control of 'handshake' signals. Timing for the data transfer is shown in Fig. 1. The computer first places the ASCII code for the character to be sent on the eight data lines. Only seven lines are required to select one of the 128 ASCII codes so the adaptor software ignores data-bit seven. The printer then receives a negative-going data strobe pulse from the computer to tell it that there is a character waiting for it on the data lines. Upon receiving this pulse the printer reads the character on the data lines and sends an 'acknowledge' pulse to the computer to indicate that the character has been read and that another character may be set up on the data lines. A 'busy' signal is also sent to the computer to stop it sending further characters while those already received are being printed; characters are normally printed line at a time. When printing is finished, the 'busy' signal ceases and the computer is allowed to send the next 'data-strobe' pulse if there is another character to be printed.

Baudot code

Character code used by the teleprinter is in five-bit serial Baudot form. Only five bits means that there are only 32 possible combinations but we need to send more than this. Letters of the alphabet and numbers 0-9 alone add up to 36 characters. Baudot code solves this by having two modes, letters (LTRS) and figures (FIGS). LTRS and FIGS are two unique codes which set the receiving teleprinter to the appropriate mode. With the exception of 'space,' 'carriage return' and 'line feed,' all other codes will print one of two different characters depending on the mode set, i.e., either a letter or a number/punctuation mark (see 'Noncomp teleprinter interface,' P. C. Barton, October 1983 issue).

For instance, letter Q and figure 1 both have the same five-bit code - which one is printed depends on which 'mode' character was sent last. Data is sent serially down a single pair of lines and the format, shown in Fig. 2 is similar to the RS232 serial code. When no transmission is taking place, the signal line remains in the 'mark' state, which in the case of this modified teleprinter interface is zero volts. A character to be sent is preceded by a start bit, which puts the signal line into the 'space' state (+5V) for one data-bit period. Length of the data-bit period is determined by the data rate, which for a teleprinter is normally fixed at 50 baud (50 data-bits per second so one data-bit period is 20ms). The five data-bits are then sent and finally a stop signal which is the 'mark' state for at least one and a half bit periods.

by R. F. Coates

Fig. 1. Centronics interface timing diagram. Eight parallel data lines carry ASCII-coded signals from the computer under control of these signals. Data strobe, when low, tells the printer that there's a character on the data lines. Busy and acknowledging signals are sent to the computer by the printer to give 'handshaking'.

Fig. 2. Teletypewriter serial data is similar in form to that usually sent down RS232 links, and travels at 50 baud.
Converter
The adaptor is divided into two sections—the ASCII to Baudot parallel-to-serial converter and the teletypewriter t.t.i. driver interface. The converter consists of the Motorola MC68070SP3, suitably programmed, and a few passive components. This section performs most of the work. Its job is to read ASCII characters from the computer, convert them to equivalent Baudot code, send out a LTRS or FIGS-mode code if necessary and send the character out serially at 50 baud to the teleprinter; the hard work is all done in software.

Converter software
Software flow is shown in Fig. 3 and the relevant part of the Picotutor-monitor in assembled form, see over. This program list was produced by the development system used to write the software for Picotutor. Such a list is produced when the source code is assembled by an assembler program, to provide the object code for programming into the 68070 eprom. The assembly-language source program, i.e. what is written by the programmer and typed into the development system, is below and to the right of the source-line page heading. Everything to the left of this is produced by the assembler. Column headings are LOC—the hexadecimal address (location). OBJECT—object code, the result of assembling. M—not used with this type of program. STAT—the statement number of each line. Comment lines begin with * and are not allocated a statement number. E—column holds an error code if there is an error in the line. LINE—line number.

Note that hexadecimal numbers are preceded by an H and enclosed by single quotation marks in assembly language used with this development system. Similarly, binary numbers are preceded by a B; if there is no prefix or quotation marks then the number is assumed to be decimal, or a label.

The first function of the converter software is to set up the 68070 peripheral ports and initial states required. Circuit diagram Fig. 4 shows that all eight lines of port A are used for parallel data input from the computer, so these are set to inputs by CLR PORTAD which sets the port A data-direction register, d.d.r., to all zeros (inputs). Port B is not used, but three of the four port C lines are used as outputs as these require different treatment.

Carriage return. For carriage return, the subroutine TPROUT sends the character in CHAR to the teletypewriter. The teleprinter takes a long time to send the heavy carriage from one end to the other, so a delay loop is introduced before going on to the next character. Also, when the Dragon sends a carriage return signal, it really means carriage return and line (feed or new-line) so after carriage return line feed is sent in a similar way. Note that with the BBC micro, whether carriage return with line feed or just carriage return is sent is determined by software. It should be configured to send just carriage return, which is the default setting.

Line feed. This is sent to the teleprinter as before but a further shorter delay is inserted. The program then branches back to get the next input character.

Space. This code is sent out and the program branches back to get the next input character.

If the code isn’t one of these three then it’s one which requires the teleprinter to be in the appropriate mode. Testing bit seven of the code indicates the mode required, and testing the LFLG, BITSTR bit flag indicates which mode the printer is in.

Bit manipulation instructions need the bit number within the byte and the byte address. Flag LFLG is equated earlier in the source file (not shown) to give the bit number, and similarly BITSTR is equated to a ram byte address. If the teleprinter is not in the correct mode, then the appropriate subroutine, LTRSET or FIGSET, is called to send the mode code and alter LFLG,BITSTR. The character code is then sent and the program then loops back to CHIN where the BUSY line is cleared, acknowledgement of receipt of the last character is sent, and the next character waits for.

Characters or mode codes are sent to the teletypewriter by calling subroutine TPROUT. This first sends the start bit by setting PC0 high (serial-data-out) for one data-bit period (20ms) by calling subroutine WA150B which loads the accumulator with value eight and passes to subroutine WAIT which executes a 2.5ms-delay loop for the number of times indicated in the accumulator, and then returns from the subroutine. On return, the five data-bits are sent one at a time, bit zero first, by a loop which sets PC0 according to the state of each bit of the data code in turn and Port C d.d.r. is set up by writing FF (all ones or outputs) to it. These three outputs also have to have an initial value; G-port line PC2 is set to (+5) to indicate busy, PC; is set to one, the normal state for the acknowledge line and PC0, the serial data output, is set to zero. To ensure that the teletypewriter is in the LTRS mode, an LTRS code is sent and an LTRS flag in ram is set. Both of these functions are performed by the LTRSET subroutine.

The main loop of the program is now entered, the BUSY signal is released and a pulse is sent to acknowledge receipt of the last character — if there was one. Next the program waits for a character to be sent by repeatedly testing the data-strobe line for a negative pulse. The data strobe line from the computer is connected to the 68070 interrupt input, but the line is not used as an interrupt in this application. At power-
DOS5F A009 687 1240 TPRI BSR WAIT 50 BAUD PERIOD
DOS600 A5A 688 1241 DECI DECRED COUNTER
DOS601 A4F 689 1242 BNE TPRI AND DO NEXT BIT UNLESS FINISHED
DOS603 A102 690 1244 BCLR OUT,PORT FINISHED CHARACTER, SET O/P LOW FOR STOP
DOS605 A60C 691 1245 LDA #500H/3/2 PULSE WHICH IS 1.5 DATA BITS LONG
DOS607 2002 692 1246 BRA WAIT BRANCH AND RTS
1247 K
DOS609 A608 693 1251 WAIT SB OR LOAD#500B
DOS609 A609 694 1252 * WAIT - WAITS FOR 2.5MS MULTIPLIED BY NUMBER IN A
1253 +
DOS609 B723 695 1256 WAIT STA DELAY STORE DELAY MULTIPLE
DOS60C 4F 695 1257 CLR
DOS606 269D 697 1258 WAIT DEC
DOS611 3A23 698 1261 DEC DELAY
DOS613 2699 699 1262 BRA WAIT!
DOS615 81 700 1264 RTS
1265 P
DOS616 1510 701 1266* FISSET - SENDS 'FIGS' CODE TO TELEPRINTER & CLEARS 'FLAG' BIT
1267 *
DOS616 1540 702 1270 LDA #FIGS
DOS616 A004 703 1271 BAA LTRSI
DOS616 1510 704 1277 LTRSET BSET LFLAG, BITSTR
DOS616 E000 705 1277 LDA #RTS
DOS620 EC22 706 1279 LTRSI LXI CHAR SAVE ORIGINAL CHARACTER
DOS622 BF4F 707 1280 STX TEMPI
DOS624 B722 708 1281 STA CHAR STORE LTRSI/FIG CODE
DOS626 A0C8 709 1282 BSR TPRIOUT AND SEND IT
DOS628 81F 710 1283 LDX TEMPI RECOVER ORIGINAL
DOS62A BF22 711 1284 STX CHAR
DOS62C 81 712 1285 RTS
1286 *
DOS62E 1B181B1B 1287 *
DOS62E 1B181814 1288* TABLE - ASCII TO BAUDOT CONVERSION TABLE
1289 WHERE MY BAUDOT EQUIVALENT EXISTS, 'SPACE' IS SUBSTITUTED
1290 *
DOS62E 1B181B1B 1291 TABLE DATA #18', #18', #18', #18', #18', #18', #18', #18'
DOS62E 1B181B1B 1292 DATA #18', #18', #18', #18', #18', #18', #18', #18'
DOS62E 1B181B1B 1293 DATA #18', #18', #18', #18', #18', #18', #18', #18'
DOS62E 1B181B1B 1294 DATA H'18', H'18', H'18', H'18', H'18', H'18', H'18', H'18'
DOS62E 1B181B1B 1295 DATA H'18', H'18', H'18', H'18', H'18', H'18', H'18', H'18'
DOS62E 1B181B1B 1296 DATA H'10', H'08', H'06', H'04', H'02', H'00', H'08'
DOS62E 1B181B1B 1297 DATA H'09', H'07', H'05', H'03', H'01', H'09', H'07'
DOS62E 1B181B1B 1298 DATA H'08', H'08', H'08', H'08', H'08', H'08', H'08', H'08'
DOS62E 1B181B1B 1299 DATA H'07', H'07', H'07', H'07', H'07', H'07', H'07', H'07'
DOS62E 1B181B1B 1300 DATA H'06', H'06', H'06', H'06', H'06', H'06', H'06', H'06'
DOS62E 1B181B1B 1301 DATA H'05', H'05', H'05', H'05', H'05', H'05', H'05', H'05'
DOS62E 1B181B1B 1302 DATA H'04', H'04', H'04', H'04', H'04', H'04', H'04', H'04'
DOS62E 1B181B1B 1303 DATA H'03', H'03', H'03', H'03', H'03', H'03', H'03', H'03'
DOS62E 1B181B1B 1304 DATA H'02', H'02', H'02', H'02', H'02', H'02', H'02', H'02'
DOS62E 1B181B1B 1305 DATA H'01', H'01', H'01', H'01', H'01', H'01', H'01', H'01'
DOS62E 1B181B1B 1306 DATA H'00', H'00', H'00', H'00', H'00', H'00', H'00', H'00'

![Computer printer socket diagram](image)

**Fig. 4.** Picotutor can be connected to act as a Centronics-to-teletypewriter interface as shown, but an alternative is to use just the microprocessor as in Fig. 5.
up the interrupt mask bit (1) in the condition-code register is set and interrupts are ignored until this bit is cleared, which it isn't in this program. The state of the interrupt pin tested by using branch-if interrupt-low/high instructions. Instruction BIH CHIN1 branches back to itself until the data strobe goes low. On the low strobe, the program proceeds by reading the data character into the index register from port A and setting the BUSY line.

**ASCII-to-Baudot conversion**

Converting ASCII to Baudot code is simple. The ASCII character set consists of 128 characters, represented by hexadecimal values of 00 to 7F. There is a 128-byte table in the program (TABLE) which contains a byte with the Baudot equivalent for each ASCII code. Five bits of each byte in the table represent the character (b0-b4) and bit seven indicates whether the character requires LTRS (b7 high) or FIGS (b7 low) mode. Instruction LDA TABLE.X loads the accumulator with the Baudot equivalent of the ASCII code in the index register. The accumulator is loaded with the contents of a memory location in the table. This address is an offset equal to the ASCII value in the index register added to the starting address of the table. For example, ASCII code for letter A is 41. This value is added to the address of TABLE, 62D, to give the address in the table of 66E which contains Baudot code for A. Bit 7, being high, indicates that LTRS mode is required. The Baudot code is also stored in ram register CHAR for later use. Tests are made on the code to see if it is a space, carriage return or line feed waits for one data-bit period. Finally a stop bit is sent which is a logical zero for one and a half bit periods, calculated by the assembler at LDA DL50B*1/2. Label DL50B is the one-bit period delay value required by subroutine WAIT and is determined early in the list by assembler directive DL50B EQU 8. The rest of the operand field tells the assembler to multiply that value by three and divide by two.

**Converter construction**

The teletypewriter software must be in the 68705 eprom. Recently distributed versions of Picotutor include this software but earlier versions will need reprogramming (read on). To find out which software release you have, examine memory location D9; if it holds 00 you don't have the teletypewriter software, if it contains 12 then you do.

The converter can either be constructed as a stand-alone unit or Picotutor can be used. Construction details for adapting a Picotutor are shown in Fig. 4, and those for a stand-alone unit in Fig. 5. Note that with both of these circuits, additional driver gates are not used on the 68705 outputs, but strictly speaking they should be. Inputs on a Centronics interface normally have 1kΩ pull-up resistors to +5V. This means that the driver must be capable of sinking at least 6mA, which is outside the specification for PC1 and PC2 outputs of the 68705. However, the BBC micro uses 4.7kΩ pull-up resistors and the Dragon 10kΩ which it will drive satisfactorily. If you have a computer that requires drivers, Fig. 5(a) may be used. This simple circuit is easily constructed on Veroboard. Power to drive the 68705 can be taken from the Dragon through the interface cable. With other computers it may be necessary to provide a separate +5V supply.

The printer interface connector used on the Dragon is not a standard Centronics one, presumably for reasons of cost, but is a 20-way ribbon cable insulation-displacement socket. Looking into the Dragon connector on the side pin 1 is at top right and numbers on the circuit diagram refer to the conductor number of the assembled socket and cable, counting conductors from pin 1. If the adaptor is to be used with another type of computer, the connections may need to be altered to suit (details should be given in the manual). The BBC microcomputer uses the same connector as the Dragon and pin numbers are the same except that all even pin numbers are connected to ground. This means that the BUSY signal is not used and an alternative 5V source of +5V will have come from inside the computer.

Conductors at the other end of the ribbon cable are taken to the appropriate pin of the 68705 and unused conductors cut off. Insulate these well. The ribbon cable should be shorter than 30cm if buffers are not used. Output from the adaptor to the teletypewriter can be any twin flex; length here is not too critical.

To enable the teletypewriter to accept t.t.l. level signals sent by the converter, some minor modification is required. If your teletypewriter has a separate terminal unit and interconnecting cable, these are not required and can be discarded. The motor is driven from 240V a.c. mains. This input is taken to the input of the mains filter on the far left of the teletypewriter, underneath. The electromagnets are to be driven by the input from the adaptor and they move an actuating arm one way or the other depending on the state of the input signal. This movement is passed on through the mechanical print mechanism to decode the character and print it.

All original connections to the electromagnets should be removed and the circuit shown in Fig. 6 constructed and connected to them. The electromagnets are on the right-hand side of the unit, on top, but, the connecting block for them is underneath, directly below. It consists of four connectors as shown in Fig. 7. Original connections should be removed and the middle two connected together and the outer two taken to the interface circuit board. This board can be constructed on Veroboard from the circuit in Fig. 6 and can either be mounted in space underneath the teleprinter or in a separate box. Which way round the electromagnet

---

**Fig. 5. Excluding a small circuit for raising the signal driving the teletypewriter, this microprocessor is used in Picotutor to complete Centronics-to-teletypewriter interface. Buffers, shown separately, may be needed to feed the inputs of some computers (see text).**
connections are made is important, but is best found by trial and error as described later.

The circuit of Fig. 7 was designed to accept either RS232 or t.t.l. levels and so the first section converts the input to 0 and + 5-volt levels. This then drives three logic gates which give complementary signals to drive the two Darlington transistors. One or other is on according to the input state thus sinking current through one of the 2.7kΩ resistors and coils, giving a reversal of current through the coils for a change of input state.

Setting up

The adaptor can now be connected to the computer and the teletypewriter interface.

Centronics-to-teletypewriter interface

Programmed microprocessors and kits of parts including p.c.b. and mains transformer are available from Magneta Electronics Ltd, 135 Hunter Street, Burton-on-Trent, Staffordshire DE14 2ST for £24.98 and £12.97 respectively, including vat. Case and hardware cost a further £3, and postage is 50p for each order.

For those who already have the Picotutor or any 68705s of their own and require the latest software release or wish to use a crystal instead of resistor oscillator, the 68705 can be re-programmed by the author for an inclusive cost of £2 by sending it to 57 Dalebrook Road, Burton-on-Trent, Staffs DE15 0AB. State whether a crystal or resistor clock is to be used.

The program for the teleprinter interface is included in the latest version of the Picotutor monitor (version 1.2) which also has some minor modifications to the monitor and the software for the teletypewriter interface and mini-organ (November 1983 issue). The mini-organ runs from address '0A4' or alternatively will run automatically at switch-on if PB1 is tied to ground and PB0 to +5V. This turns Picotutor into a stand-alone organ.

First check that the electromagnets have been connected up correctly. With everything connected up, switch on the computer and teletypewriter. If you are using Picotutor key in go 0A1 to run the program. The stand-alone version automatically runs the program at power-up. If the electromagnet connections are correct, the teletypewriter motor should run and nothing else happen, but if it clatters away seemingly trying to print something, but not actually doing so, then the two connections from the interface board to the electromagnets should be reversed.

The printer is now ready for trying out, but the variable resistor on the adaptor may need adjusting before intelligible results can be obtained. This resistor sets the clock speed of the 68705. Data rate timing depends on this resistor. Using Picotutor, R2 will need either to be replaced by a 22kΩ variable (or a selected fixed resistor). If you are using a crystal for timing (the eprom has to be reprogrammed for this, see December 1983 issue) a crystal of 3.2768MHz should be used, which will give the correct data rate without adjustment.

Enter a line or two of text into the computer and then send this to the telley typewriter, using the LLIST command in the case of the Dragon. The teletypewriter should now attempt to print something. Adjust the variable resistor until the printing becomes intelligible; the setting is not critical.

Conclusions

One difficulty with this arrangement is that not all ASCII characters are available in Baudot. In most spaces, a print is spoken where there is no Baudot equivalent, with these exceptions.

By altering the table, any character can be made to print as you wish, so it is possible to alter this to suit your needs. I mentioned earlier that if you are using Picotutor you need to key in the program start address, but a stand-alone unit will run the printer adaptar at switch-on using PB0. When the 68705 is powered up, all peripheral pins are programmed as inputs. On Picotutor, all port B lines are pulled up to +5V by the 270Ω resistor network (see circuit diagram, December 1982 issue) but in Fig. 5 (stand-alone circuit) PB0 is tied to ground. At switch-on, or when reset is pressed, the monitor program tests the PB0 input. If it is one, it runs the monitor program, if it is zero, it jumps to the computer/teletypewriter adaptar program and runs that.

For those following the 'Assembly language programming' series, I hope that this description of a real application of the 6805 and the software listing will help to show some of the techniques of programming. When learning to program it is extremely useful to look at programs other people have written to get ideas and for this reason the complete source listing for the Picotutor monitor is available if required and is advised if full use of the facilities on the Picotutor is to be made.

Unfortunately, because of its size (about 25 pages) it is not possible to publish it but copies may be purchased through Magneta Electronics (see box).

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Designing with 68008

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The 68008, as used in the Picotutor, is a high-performance microprocessor which has been optimized as intelligent peripherals having a 68008-type interface, the interface being emulated by m.c.u. software. Some of the m.c.u. i/o ports are used to provide the peripheral data bus D0-D7, chip-select (CS), read/write (R/W) DACK, IACK, and register select (RS) lines. Port lines programmed as inputs (CS, R/W and RS) are monitored by the on-chip software to determine 68008 accesses. And with the port lines used for D0-D7, DACK and IACK, the m.c.u. may be programmed by the 68008, and provide vectored interrupt acknowledge cycles. To the 68008 the m.c.u. behaves just like any other M68000 family peripheral.
Matched filters for radar and satellites

Surface wave, charge transfer and digital v.l.s.i. devices enable complex and powerful matched filters to be made. Geoffrey Robinson describes some examples that illustrate their different forms and uses.

by G. N. Robinson B.Sc.

Since graduating from Salford University in 1975, Geoff Robinson has worked for Marconi Avionics on the AEW Nimrod project, and for Marconi Communication Systems where he is currently a principal engineer in the space and microwave division. During this time he has also spent three years at Leeds University working on an experimental spread spectrum system which will form the basis for a Ph.D thesis.

A matched filter is therefore the same as the amplitude spectrum |X(ω)| of the signal to which it is matched. The output of the filter, y(t), is found by convolving x(t) with h(t)

\[ y(t) = \int_{-\infty}^{\infty} x(\tau) h(t-\tau) d\tau \]  

From Fig. 1(c) the matched filter has caused considerable distortion of the input signal x(t). This distortion is typical of all matched filters which in general produce a 'peaked' symmetrical output, similar to y(t), when their matched signal is the input. Substituting equation 1 in equation 3 gives

\[ y(t) = \int_{-\infty}^{\infty} x(\tau) k X^*(\omega) \exp(-j\omega t_0) d\tau \]  

\[ y(t) = R(t-t_0) \]  

The output therefore is the autocorrelation function R(τ) of the matched signal. This often serves as an alternative definition of a matched filter: i.e. one whose output signal is the autocorrelation function of its input signal.

The 'peaked' output obtained from a matched filter is exactly the type of response needed to detect the presence of a signal buried in noise. The matched filter is, in fact, the optimum device for detecting weak signals and it is therefore no surprise to learn that it forms the basis of many radar and digital communication receivers. In digital communications, matched filter considerations generally only arise when transmitter power is limited, such as in the case of satellite communication.

Before discussing the use of matched filters in satellite earth stations it is necessary to review some of the fundamentals of digital transmission. Digital information, whether computer generated or from some other source such as p.c.m.-encoded voice, is usually available prior to transmission in the form of an n.r.z. rectangular waveform, as shown in Fig. 2(a). To transmit such a waveform without distortion would require an infinite bandwidth in theory. The waveform can be considered to be made up of the sum of individual pulses as in (b) which are confined to a time interval t seconds. If the n.r.z. waveform is filtered to limit the bandwidth, the effect on the individual pulses is to stretch them so that they are no longer entirely contained in their original time slot.

The effect of one particular low-pass filter is shown in Fig. 2(c). If the filtered n.r.z. signal is sampled at the points shown the tails of the individual pulses will affect the sample values in the nearby time slots. This effect, known as intersymbol interference (i.s.i.), can be avoided if the filtering is performed in accordance with Nyquist’s vestigial symmetry theorem. This theorem, put forward by Nyquist as long ago as...
1928, states that the zero crossings of the waveform in (c) occur at the sampling instants (giving no intersymbol interference) if the filter is either an ideal 'brick-wall' low-pass filter or an ideal 'brick-wall' low-pass filter with a transition band modified to give odd symmetry about the cut-off frequency. The theorem also requires the original n.r.z. waveform to be converted into a sequence of impulses so that the spectrum at the input of the filter is flat over the filter bandwidth. A class of widely used filters which satisfy this theorem are the raised-cosine filters. The amplitude response of the raised-cosine filter with various values of excess bandwidth or roll-off factor $\alpha$ are shown below. A linear phase characteristic up to the zero transmission frequency is also required. In any bandwidth-efficient data transmission system with no intersymbol interference, overall channel filtering should therefore be as shown or equivalent to it for an r.f. modulation system.

**Satellite data transmission**

Although the overall channel response for interference-free data transmission has been specified, the apportioning of this response between the various transmitter and receiver filters is a complicated problem. It is true, however, that if the transmission medium is linear between the transmitter and the receiver then the optimum split of the overall response is an equal division of the filtering between the transmitter and the receiver. The frequency response of the identical transmitter and receiver filters is therefore the square root of the response shown. This filter, known as a root cosine roll-off filter, is therefore only 3dB down at half the signalling frequency as opposed to 6dB in the diagram.

The equal division of the overall Nyquist response results in a matched filter at the receiver. This then simultaneously combats both intersymbol interference and the effects of noise. Although most satellite channels are non-linear due to the operation of transmitter high power amplifiers at or near saturation, the matched filter concept is still used in many earth station designs. A number of major satellite operators have specified this type of system including Intelsat who have made root 40% cosine roll-off filtering mandatory for their 120Mbit's t.d.m.a traffic service through the Intelsat V satellites. The earth station receiver filter mask specified by Intelsat is illustrated next, being nominally a root 40% cosine roll-off filter.

The actual filters used to realise these responses are generally based on standard filters such as Butterworth, Chebyshev or elliptical filters. The filter shown below consisting of a sixth-order Butterworth filter followed by a stage of delay equalization realises a root 100% cosine roll-off low-pass filter.

**Radar**

Most radar receivers use matched filtering, although prior to about 1960 this was relatively trivial and merely involved the optimizing of conventional i.f. bandwidths. The usefulness of a matched filter, from a radar designer's viewpoint, is directly proportional to the time-bandwidth product of the filter, obtained by multiplying signal duration by filter bandwidth. Unfortunately the complexity of a matched filter is also proportional to its time-bandwidth product. The type of matched filters previously discussed in relation to digital communication generally have time-bandwidth products of the order of unity and are consequently not considered to be complex. In radar, however, the designer provides a time-bandwidth product in the range 10,000 to 100,000.

The main motivation behind the early matched filter development which led to the invention of the pulse compression radar was the need to obtain good range resolution with limited peak powers. Long range detection requires a large pulse energy which with a conventional power-limited radar means increasing the pulse duration. This causes a direct reduction in range resolution and accuracy. If instead of increasing the pulse duration the pulse bandwidth is increased, an improvement in range resolution in proportion to the time-bandwidth product is obtained.

The most well-known pulse compression technique uses the frequency chirp waveform shown next together with its dispersive delay-line matched filter. The matched filter output, which is the compressed pulse, is shown below. The sin x/x-shaped pulse has a peak which is VBT times larger than the original chirp signal amplitude. Dispersive delay lines, that is delay lines with a delay proportional to frequency, are today generally fabricated using acoustic surface wave technology and a wide variety are currently available "off the shelf".

The more complex matched-filter receivers which have also to satisfy the additional requirement of being able to process many different waveforms often resort to digital techniques. Bottom diag. is a flexible arrangement which performs matched filtering by multiplication in the frequency domain, rather than by convolution in the time domain, as in the previous filters discussed. In this method the signal is first sampled at a very fast rate, anything up to 200MHz, and then passed through an a-to-d converter. Blocks of digitized samples are then converted into corresponding blocks of frequency samples by a fast Fourier transform circuit. Then next these samples are multiplied by stored coefficients which represent the conjugate spectrum of the signal. Finally the transform circuit is re-configured to perform an inverse transform on the samples.
Testing microprocessor-based systems at home

Though the design of microprocessor systems is not particularly difficult, testing is not so simple for the first-time builder without access to logic analysers or emulators. Here are some simple procedures that highlight hardware and software problems.

The design of simple microprocessor systems is not a particularly difficult task. Provided that one adheres to the correct loading rules for both current and capacitance, the design can be as easy as putting toy building bricks together. However, testing that the system - hardware or software - works is not so simple for the amateur or first-time builder who does not have access to logic analysers or plug-in microprocessor emulators. This article identifies some simple procedures to highlight both hardware and simple software problems. The discussion is based around the 8085 microprocessor but applies to virtually any microprocessor having a ready input.

Developed in the mid-seventies by Intel, the 8085 is an update for the 8080 chip set. Because the device has only 40 pins, Intel multiplexed the lower eight address bits with the eight data bits on lines designated AD0-7. Fig. 1. Figure 2 shows typical timing for the 8085 during a memory read and illustrates how AD0-7 are multiplexed. The 8085 produces a clock output that is half the frequency of the source at X1 and X2; the timings of all the other signals produced by the microprocessor are related to its edges.

Shortly after the start of T1, the lower eight bits of the memory address appear on lines AD0-7 and are guaranteed to be stable before the negative edge of ALE, generally used to latch the address into an eight-bit buffer such as a 74LS373 (see Fig. 3). As this is a transparent buffer, the address will be passed through the buffer whenever ALE is high, and latched on the negative edge. The address is stable some time before the latching and the use of a transparent latch ensures that the address is available early in the read cycle, so that it can be used by other circuitry such as chip select logic. This is a great advantage when using fast microprocessors.

Around the start of T2, the memory address bits are removed and AD0-7 goes tristate, waiting for data to be read in during T3.

Figure 3 shows how this might be achieved in hardware terms. Some designers add an additional latch on the upper eight address lines, which can glitch when certain instructions are executed.

During a write cycle the multiplexing of AD0-7 follows in a similar fashion, address being valid before the trailing edge of ALE and valid data long before the rising edge of WR.

Ready

The 8085 has a ready pin which can be used to extend the length of read or write cycles to compensate for slow peripheral chips or to handle devices not always available such as dual-ported memory. Figure 4 shows how the ready pin is sampled by the

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(Figures and diagrams are not transcribed, but are included in the natural text format.)

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by Colin Carson
8085 in the middle of T2, although it must be stable for a period before the sampling, the set-up time. If ready is low when sampled then on completing the T2 cycle, the 8085 produces another T2 cycle rather than going on to T3. This will repeat until the ready pin is sampled high.

The test procedures mentioned here make use of the ready pin, and the fact that signals such as RD, WR and AD0–7 remain unchanged during the not ready period.

**Reset**

After the 8085 is reset, it reads the contents of the memory location whose address is 0000. It then continues to read from consecutive locations, decoding and executing them until instructed to jump to a different address. However, if the ready pin is forced low before the 8085 is reset the microprocessor sits doing repetitive T2 cycles with the address 0000 at the outputs of the latches, RD low and waiting for valid data. This valid data should be the contents of the first location in prom and will invariably be the first byte of the three byte instruction LXI SP which sets up the internal stack pointer.

**First test procedure**

1. Check that the Hold input is not being driven high. Hold will force many of the 8085 outputs tristate.
2. Pull the ready input low, taking care not to damage any chips driving this pin. If necessary remove the 8085 from its socket and bend the ready pin so that it does not make contact on reinsertion. Then using a crocodile clip and lead ground the ready pin.
3. Reset the 8085.
4. Using a logic probe or oscilloscope, check the address lines are all low.
5. Check the address pins on the prom are all low.
6. Check the chip select logic is driving the chip select pin on the prom low.
7. Check that RD is driving the output enable on the prom low.
8. Check the correct eight bit data for location 0000 is present on AD0–7.

By following this step-by-step procedure simple hardware faults can be highlighted but because all the address lines are low, this will not show up shorts between them. To further exercise the hardware and trace simple software faults a single step facility is required, such as that in Fig. 5.

**Single step**

The next step is to step the microprocessor through instructions, monitoring the data and address buses until something unexpected happens. When the circuit is on, the flip flop and hence ready can be either low or high. After the power-on reset, the 8085 produces an ALE to latch the lower address byte 00. Signal ALE is inverted by G3 clearing the flip flop and ready goes low. This condition will continue until the push switch S1 is depressed, which after debouncing by G1 and G2, clocks a high through the flip flop. Ready goes high and the 8085 completes reading the first instruction and issues the address for the next byte. Once again the flip flop is cleared and the microprocessor waits for S1. In this fashion S1 can be used to single step the 8085 through each byte of each instruction. Take care to ensure that G3 does not overload the ALE line, which can drive a maximum of five normal LS t.i.l. loads.

Using this circuit the microprocessor can be stepped through its program in prom until something goes wrong. Often it will only take a few instructions to highlight shorted address or data lines, although the tester will obviously need to be able to spot certain 8085 op-codes such as jumps, calls, interrupts and returns. The beginner to the 8085 should learn a lot...
Synthesized television modulator

As well as providing 5.5 and 6MHz sound, this modulator can be accurately switched to any desired U.H.F. channel.

by R. Wilkins & L. Cergil

shows a basic phase-locked loop whose programmable divider ratio is supplied from the microprocessor.

Microprocessor

The MC6805-P2 m.p.u. is an eight-bit microprocessor with a built-in software capacity of 1Kbyte of rom, 64 bytes of ram, and twenty t.t.l/c.mos-compatible bidirectional input/output lines. Eight of the lines are i.e.d-compatible. The microprocessor is designed for low-cost high-volume applications; normally the makers of the device would produce a rom pattern from the customers software, and manufacture at least several thousand parts. For the one-off however, there is an eprom version that can be loaded with software and if necessary erased and loaded again many times over and the MC68705-P3 version was chosen for this application. Its task is to take in the channel number from the two b.c.d. thumbwheel switches, do the necessary calculations and send the division ratio to the programmable divider. As the information sent to the programmable divider is latched into the divider the microprocessor unit need only send the information when it needs changing. This has the advantage of keeping radiation from the microprocessor to a minimum, which is essential in r.f. applications.

As the microprocessor is only checking the thumbwheels, two new lines of the time, it can be given additional work to do. Firstly, if the requested channel is less than 21, the microprocessors presume that the user has made a mistake, lights a lamp and sends the data for channel 21 to the programmable divider. Similarly, if a channel greater than 68 is requested, the light comes on again and channel 68 is sent. Secondly, as sound may well be required as well as vision, the micro-

Roger Wilkins' schoolboy interest in radio was complemented by an HND from Kingston Polytechnic and lead him into a career in consumer electronics. For the last 15 years he's been involved in the design of colour television receivers in London, Bradford, Geneva and now Gosport. His previous job was as an applications engineer with Motorola in Geneva, which is where this project was completed. Working now for Thorn EMI Ferguson on chroma and video circuits, his original interest in radio is still alive, with emphasis on receivers and amateur radio.

Lubomir Cergil, born and educated in Czechoslovakia, now lives in Geneva. Well qualified academically, his early career was in pure research, firstly at the Czechoslovak Academy of Science and later as a visiting scientist at CERN. He then worked for Motorola in Geneva on c-mos and e.c.l. and now specializes in eight-bit c-mos microprocessors.
processor can control a second phase-locked loop, synthesizing either a 5.5MHz or a 6.0MHz sound carrier.

Modulator
In Fig. 1 the circuit blocks that are enclosed by the broken line were the result of heavily modifying a Mullard ELC1043 television tuner. But as the purpose of this article is to describe the application of frequency synthesis, only an outline of the necessary modifications to the tuner are given. The changes, shown in block form in Fig. 2, follow an original article by Trundle (Practical Television, April 1975).

Three further changes were necessary beyond the circuit described by Trundle. Firstly, the length of the oscillator tuning line was increased so that the whole u.h.f. band could be covered by the oscillator. Secondly, a 64 pre-scaler was fitted inside the tuner box and coupled up to the oscillator output. Thirdly, the original black-level stabilizing circuitry was improved. The result of the modifications was a tuner box that required and produced the signals shown in Fig. 3.

Phase-locked loops
Fig. 4 shows the contents of a UAA2000 which is the device chosen for both phase-locked loops in this application. The crystal frequency chosen was 4MHz, and is used as a clock for the microprocessor as well as the second UAA2000. In both phase-locked loop circuits, the output from the reference divider is 976.5625Hz, the frequency that the u.h.f. oscillator must be divided down to. For example, channel 44 is 655.25MHz, and this must be divided by 670975 to make it equal the reference frequency. Part of the division ratio is fixed at 64 by the tuner pre-scaler and there is an additional fixed +2 in the UAA2000. The programmable divider must therefore divide by 5242 to obtain the correct result. Calculation of the ratio provided by the programmable divider is done by the microprocessor.

The UAA2000 accepts data in serial form made up of 18 bits. Data are transferred into the shift register on positive-going edges of the clock, and latched into the programmable divider after the enable signal goes high. The required waveforms and their timings are depicted in Fig. 5, together with the format of the serial data word. The first four bits are used in v.h.f./u.h.f. operation and are all zero in this application. The last 14 bits are the binary equivalent of the division ratio, with the first bit, bit five, being the most significant. Fig. 6 shows the data, clock and enable waveforms for channel 44. This requires a programmable division ratio of 5242 which has a binary equivalent of 000101000111010. The order of the binary number is reversed however to satisfy the requirements of the UAA2000 shift register.

For the sound channel modulation, the microprocessor sends the binary equivalent of 2816 for 5.5MHz or 3072 for 6.0MHz.

Circuit description
The complete circuit diagram is shown in Fig. 7. The incoming video has its sync. tips clamped to a voltage adjusted to match ELC1043 a.g.c. characteristic.

A sound carrier is generated using a Hartley oscillator tuned by an MV2112 diode. Its output frequency can be either 5.5MHz or 6.0MHz depending on the data fed into the phase-locked loop divider. The sound carrier output, as well as being fed back to the UAA2000 to complete the loop, is added to the video via an 18pF capacitor. A locally generated 700Hz tone frequency modulates the sound carrier, though an external modulation may be connected. The correct 50µs pre-emphasis is provided by the 2.2nF capacitor connecting the audio to the Hartley oscillator. An ever-increasing frequency response is prevented by the 10kΩ resistor limiting the maximum amplitude at about 15kHz.

The two phase-locked loops have the same circuit but different filter time constants. Values used for the calculation of the loop filters are

\[ K_0 = 0.8 \text{ volt/rad} \]
\[ K_0 = 84.5 \times 10 \text{ rad/s/volt for vision} \]
\[ K_0 = 571 \times 10 \text{ rad/s/volt for sound} \]

Both UAA2000s share the same data and clock, but have different enable signals for obvious reasons.

Software description
Because there is no hardware or timer interrupt used in the system, the software is organized as depicted in Fig. 8.

Initialization. After power is applied or the reset activated, the microprocessor starts with the initialization subroutine. The following operations are performed. Input/output relations are established on ports A and B. Port A is configured as eight input lines, on port B only the line FB3 is configured as input; all remaining lines are outputs. The UAA2000 circuits are set into the starting conditions, in that the input VDR, DATA, CLOCK are set into logic state 1. The starting address of the program — which is the initialization — is stored under the reset interrupt priority. The MC6805P2 or MC68705 can be reset three ways: by initial 'power-up', by the external reset input (RESET), and by an optional low-voltage detect circuit. Input data for vision. In this subroutine, the switches are read and debounced. The value is read in b.c.d. and compared to the value previously read. If there is no difference, no further action is required.
and the program execution is diverted to the next subroutine. If there is a difference, the b.c.d. is transformed into the n.c.b. value. The result of the transformation is compared to the value for channels 21 and 68. If the new value is lower than that for channel 21, the value for channel 21 is considered correct. On the other side of the scale, if the new value read is greater than 68, the value for channel 68 is considered correct. In both cases the lamp is switched on, signalling an incorrect value read from the switches.

In the next step, the division ratio for the UAA2000 circuit is calculated. The result is 14 bits long and stored in two registers. Input data format for the UAA2000 is 18 bits long and consists of the band code, which is four bits long and the input frequency division code, which is 14 bits long. High-to-low transition on the v.d.r. allows an access to the new data. The new data starts with the band code first, followed by the input frequency division ratio code, most significant bit first. During this operation the timing must be guaranteed, as required by the data sheets for the UAA2000.

**Data input sound.** Information about the sound frequency is on the pin PB2. The input frequency division code for the sound is altered only if there was a change with the previous reading. The values that are to be sent to the UAA2000 for sound are stored in the same registers as the vision values, and the same routine for code generation is used as for the vision code. At this stage the program is returned to the reading of the possible new data for vision and the process continues.

**Fig. 8. Software flowchart for both sound and vision loops.**
Testing microprocessor-based systems

about its operation by making practical use of this circuit.

Displays

Examining the address and data buses with a logic probe or oscilloscope for a dozen or so instructions starts to prove rather tedious and if serious use is intended then it is worthwhile adding some displays and a high-speed multiple step.

Data and address can be displayed on individual l.e.d.s or more expensively on seven-segment displays. Either way, the addition of displays must load the 8085 as little as possible and certainly via buffers.

One approach is to wire the buffers etc to a 40 pin i.e. clip that fits over the 8085.

Figure 6 shows an array of seven-segment displays D7 to D0. Displays D1 and D2 register the upper address byte and are driven from a 74LS373 latched on a buffered version of ALE so that it only presents one LS load. Each display is a TIL311 which includes the relevant decoder. Other displays can be used although not all can display the hex codes A to F satisfactorily, or alternatively single l.e.d.s could be driven from each bit. Consideration must also be made of the extra power consumption this type of circuit requires. Displays D3 and D4 show the lower address byte and D5, D6 the data. And IC3 can be either a straight buffer such as an 81LS95, or a latch clocked by RD or WR so that either can be monitored. Note that this circuit loads AD0-7 with two buffers.

Multiple step

A multiple-step facility can easily be incorporated, as shown in Fig. 7. The capacitor value can be varied to suit personal choice.

There are many other enhancements that can easily be made, however the circuits and notes described here have to be found quite adequate for simple hardware and software debugging.
TEM-WAVE PHYSICS

Lest the fierceness of Mr Catt's response to Mr Dalton (February 1984 issue) obscure what he said, could I diplomatically support all that was contained in his letter while at the same time describe a situation where E and H are 90° out of phase. This should please Mr Dalton.

But first let me remind Mr Dalton that the opposite of "static" is "dynamic" and not "oscillatory". The last is just one of many modes of motion which need not even be periodic. This is particularly important because the example 1 propose to give for E and H being 90° out of phase is static. This should please Mr Catt.

Starting from Maxwell's equations it is easy to derive equations of wave propagation for E and H, the solutions of which are

\[ E = f(x - ct) \]

and

\[ H = \frac{1}{c} f(x - ct) \]

where \( f \) can be any function, not just sinusoidal or even periodic e.g. a digital (level) change, a single pulse — square or any other shape.

The variation (f) of E matches precisely the variation of E (also f) whatever f happens to be. There is no delay between E and H or, in the case of f being sinusoidal, no phase difference. As Mr Dalton states there is no causality between E and H. However, and this may be part of the origin of Mr Dalton's error, there is a rotation of 90° from E and H which is right handed about (not along) the direction of propagation. Thus if f is sinusoidal E and H are in phase but at right angles to each other in space, at time.

If the equations above are divided one into the other then

\[ \frac{E}{H} = j \frac{c}{\mu} = Z_0 \]

where \( Z_0 \) is the wave impedance of free space (about 375 ohms) which is independent of f.

If E and H were sinusoidal and 90° out of phase as Mr Dalton suggests, then \( Z_0 \) would be the tangent i.e. from minus infinity to plus infinity. This would make it difficult for a wave to propagate. At the very least it would imply causality if one knew which occurred first and at worst would mean changing the title of your illustrious magazine.

This brings me to the example of E and H being out of phase and possibly the other half of Mr Dalton's confusion.

Suppose that a sinusoidal wave described by

\[ E_1 = E_0 \sin \left( \frac{2\pi}{\lambda} (x - ct) \right) \]

has superimposed on it an equal wave but travelling in the opposite direction, say by reflection, described by

\[ E_2 = E_0 \sin \left( \frac{2\pi}{\lambda} (x + ct) \right) \]

Some trigonometry reduces the sum of these to

\[ E_1 + E_2 = 2E_0 \sin \left( \frac{2\pi}{\lambda} x \right) \cos \left( \frac{2\pi}{\lambda} ct \right) \]

or \( Z_0 E_0 \sin \left( \frac{2\pi}{\lambda} x \right) \sin \left( \frac{2\pi}{\lambda} ct \right) \)

Similarly

\[ H_1 + H_2 = -2H_0 \cos \left( \frac{2\pi}{\lambda} x \right) \sin \left( \frac{2\pi}{\lambda} ct \right) \]

This results in the well-known standing wave where the nodes of H correspond with the peaks of E and vice versa i.e. 90° out of phase. When E is a maximum, H is zero everywhere. Then H grows and E decreases until it is a maximum and E is zero and so on cyclically. Thus the standing wave has all the appearance of transforming itself from an entirely electric form to an entirely magnetic one and vice versa. But it is just an illusion, for as Mr Catt states, there is no causal relationship between E and H for a single wave, still less is there any between two in which we only observe their interference pattern.

This, I hope, explains the source of Mr Dalton's confusion.

Finally I would like to disagree with Mr Catt (or in very much a way only concerning his references. Carter in his book "The Electromagnetic Field in its Engineering Aspects" pages 266 to 276 is quite specific about there being a delay (or phase difference in the sinusoidal case) between E and H, both in his diagrams and text, and of which the above is, in my view, an accurate paraphrase. They correspond, though in different words, with the views expressed by Mr Catt.

E. O. Richards

Hitchin, Herts.

PS: For those who share Mr Catt's disgust with sin and cos I commend a closer look at Walsh functions, an introduction to which appeared in these pages in January 1982. An excellent book on the subject is "Walsh Functions and the Engineering Applications".

OPERATING FORTH

The articles by Brian Woodroffe and Roy Eason on the description and applications of the Forth language have been admirable and must have done much to popularise this elegant little computer language. In particular Mr Eason's introductory paragraphs are as concise an explanation of Forth as I have seen anywhere.

Of all the features of Forth the one which seems to be over-emphasized is the manner in which it is extensible, i.e. that new words, defined by the user, can be added to the dictionary thereby extending the language. This mechanism is not unique to Forth. Most languages especially the so-called block-structured ones have similar features. In Algol, Pascal and Coral 66 the section of code which carries out one job on an input signal from the user is called a procedure and then given a unique name. Therefore, whenever that particular little job needs to be done, the controlling program merely calls that procedure by name. Similarly the procedure can be incorporated into bigger procedures and so on. Most large operating systems with a job control language have a similar arrangement. Sequences of commands are put into a named file (a macro) that can then be considered as an extension to the j.c.l. since invoking it causes the machine to obey the command sequence it contains. That macro may also be incorporated in further macros. Where Forth scores is surely the simplicity with which its new words are defined.

It is this simplicity and conciseness which are its real advantages. Forth is not just another language. It is also a complete miniature operating system. In size, it requires much less memory than most compilers would require as their workspaces.

In implementation it means that Forth can be installed on most machines quickly and economically, especially if the FIG-Forth model is used. In operation, it means that a new user can sit down at any keyboard and use Forth without needing a week or more to learn how to drive the host computer first (the problem that ADA is striving to beat). Time on development is saved and, due to the structures of Forth, so is time and effort in testing. Any project manager on a tight budget will tell you how valuable these savings can be.

I don't wish to eulogise Forth, for it is not the perfect language by any means. But its more unusual virtues are very real and deserve recognition. It comes much closer than any other so far to my personal ideal of a Universal Assembler Language that I can afford.

L. J. Smith

Barnet Herts.

'CURRENT DUMPING'

Readers may be interested in the basis on which 'current dumping' is founded. In the Wireless World for January 1973 and October 1974 I published two contributions on 'error take-off', as I now call it, which preceded P. J. Walker's AES lecture on current dumping in March 1975.

However, Vanderkooy and Lipshitz have very clearly shown in the J.AES (Jan./Feb. 1980, Fig. 6) the connection, reproduced below. It may well help others who wish to develop error take-off circuits, of which current dumping is a successful example.

A. Sandman

London NW3

WIRELESS WORLD APRIL 1984

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FORTH COMPUTER

Although James Kidd and I agree about what makes the 6809 so suitable for FORTH, I disagree with his rankings: 1 data stack access 2 NEXT 3 control stack access. As NEXT is executed every time any code fragment finishes it is executed as often as all other fragments put together. Hence it is the most critical code sequence in any implementation. It is the execution frequency and not the static frequency of occurrence that matters (i.e. those things at the centrel of loops matter more than those outside). Continuously the execution time of 80% (or is it 66%) of the code has minimal effect on the overall performance. Hence the fast execution of infrequently encountered instructions (e.g. divide, string search versus add, move etc) is almost irrelevant and hence the RISC argument. It is a mistake to make a virtue out of anything that extends NEXT not only because NEXT is time critical but also because error correction and program testing in a high level interactive environment should be done with the tools of that environment and not with the aid of single step debugging.

The FORTH primitives DOCOL and SEMIS are the most commonly executed. Implemented inefficiently between processors which do not support two stacks should investigate the potential of making the control stack the processor "normal" stack and maintaining the data stack via a user pointer. This should benefit the 8088's control stack operations (DOCOL, SEMIS) only push and pop values. This would leave BP free to access the data stack using indexing modes as noted by J. O'Connor. The 8088 BP register is used for the control stack in the FIG model.

The 9900 series memory to memory architecture appears to be peculiarly unsuited to computation and FORTH for most operations involve the "call" and the "return" of data accessing memory whereas more normal architectures (e.g. 6800/8080 etc) seldom require more than one. Texas have dropped their 99/4A home computer (9995 based) and their latest personal computers incorporate more mainframe products. However, the 9995 by virtue of its own on-chip memory that could be programmer maintained as an instruction cache could be an interesting prospect for FORTH. Caching is a method of keeping recently accessed data (or instructions) in fast on-chip memory which makes the whole memory system look faster. It is similar in concept to paged virtual memory between disc and main memory which FORTH has. I leave it to the interested reader to follow this up. (The Z8000 with genuine on-chip cache looks especially interesting in this respect.)

Mr Bacon goes on to castigate me for trying to make some allowance for the processor's required memory speed. In any design with a half decent size of memory the cost of that memory will be more than that of the processor (in my case 4:1 approximately), hence it is reasonable to make some allowance for higher cost of faster memories. Hence my crude attempt to rationalize processor speed with memory access time. As James Kidd points out access time does not linearly scale with clock rate (especially if wait states are used). However, some allowance must be made. Also as James Kidd points out my design should use 350ns eproms, although I still use 450ns parts with a standard 6809 running at 1.5 MHz. As the read/write control signals (MR, WE etc) are conditioned by the processor clocks there is no problem if the chip selects glitch upon a clock edge change.

The on-chip memory used as a program cache is the main reason why Texas were able to show the 9995 running the Intel benchmarks faster than the 8088. One would expect the 9995's performance to be less good if the program could not fit the cache. So there are problems about the suitability of the benchmark as a performance indicator for the target application. Similar reservations should be borne in mind when looking at the Seive of Eratosthenes results. If your application is scientific (floating point operations dominate) then the Seive results will not be a good indicator. You should think in terms of a processor that supports numeric co-processor (i.e. a newer 16-bit or a mini), but if you want to run FORTH then in most any environment the 6809 takes a lot of beating.

It is not true that 'in most high level languages most time is spent pushing garbage'. Today's compiler technology is such that an optimizing compiler will produce more efficient code than a human. Not only will it be done correctly every time but the compiler is much less likely to get a global picture. Hence reasons why neither Ximnos (Occam for the transputer) nor Xerox (for the Mesa system) issue detail of the machine instruction set, for the compiler will produce optimum machine code. Today no operating system kernels are written in compiled code (e.g. Unix in C). High-level languages are accepted as the means to get programs to work more quickly and thus save programmers' time. Note however if a fast program runs, unless it runs correctly, it is wasting programmers' time.

Dr Croker of Woking has written to me pointing out that the FIG model for the 8088 is a coded sub-optimally NEXT can be shortened to the four byte macro 'LODSW, MOV BX, AX, JMP [BX]' improving NEXT's speed by about 40%. It is not true that as originally coded there have to be multiple copies of NEXT for the 84/75 as there can be 4 byte jump (+32k bytes) and not a near jump (+127 bytes) as Martin Bacon supposes. Second, by keeping the top of data stack a register (e.g. DI), make the stack always be improved (e.g. @ becomes MOV DI, [DI] etc). This technique can be applied to any simulation of a zero address machine. I looked into this when I coded my 6809 (top of stack in D) but I felt the disadvantages to the branch primitives (OBRANCH, (LOOP) etc) would outweigh the benefits to the data primitives (6, + etc).

Mr Carter of Nottingham has also written to me showing that my method for producing a 11ns data transfer routine can be improved. He points out that as the transfer loop does not affect the carry flag then it can be cleared upon loop entry. This is then tested for upon possible loop exit and in the normal case it will loop back. However when the sector transfer is completed the NMI interrupt occurs to set the carry flag in the saved context hence letting the processor exit the loop. As the interrupt does not cause the loop exit but only flags for it there is no need to have differing interrupt vectors. He also points out that if the WD1793 exhibits an interrupt latency near its maximum rather than typical value my data transfer loop could fail, requiring a re-try (i.e. 500ns typ, 3000ns max).

Further failings in my proof readings have been detected by constructors. The full list of errors appears to be:

- pins 39/40 of the 6821 p.i.a. are shown reversed June page 56.
- power supply op-amp is MC3405 July page 61.
- power supply op-amp pins 5/6 shown reversed July page 61.
- 6809 interrupt pins are irq 3, irq 4, nmi 5 May page 56.
- LS1122 for pin 9 read 11, for pin 11 read 13 May page 56.
- dot clock oscillator 51P connects to IC10 pin 9 not 8 June page 56.
- Some constructors' computers hang upon producing the log on message. I have been unable to reproduce this. It is apparently cured by pulsing an interrupt low.
- LS139 see corrections in June issue, page 58.
- LS138 pin 15 label 'v' not 'u' June page 56.

A source listing is also available.

Brian Woodroffe
Edinburgh

PRECISION PREAMP

I should like to thank Mr Armstrong (Letters, January) for the interest he has taken in my latest preamplifier design. Unfortunately I am in the position of having to contradict virtually everything he says. At the end of my article I expressed the pious hope that anyone wishing to dispute points of the kind raised by Mr Armstrong would arm themselves with objective evidence (i.e. actual measurements). Sadly, he has not done this.

I was not surprised that I failed to convince everyone that tone controls could actually be useful; although it is less than ten years since a preamp without them would have been un-thinkable, since then fashion and dogma have been invading a field in which the technical challenges have largely been overcome. Omitting the tone controls will not save a lot of components, as you must retain not only the high-impedance buffer, but also the tone-control op-amp, in order that the balance control can be retained. This also keeps all in and puts in phase. I should like to emphasize that with the controls set centrally the signal undergoes no spurious phase shift or detectable degradation. Nonetheless, here are the details for a no-tone-control version.

(a) Delete R25, and C19 to C21, and also the treble control.
(b) Replace R30 and the bass control with short circuits, and change R19, 19 to 1.7k. This should be satisfactory, though I must emphasize that I have not tested it exhaustively.

I do not believe that I have neglected any of the important parameters of electrolytic capacitors. They are quite adequately reliable when operated with no polarizing voltage; only the application of a reverse bias greater than 1V is likely to cause breakdown of the dielectric film. This of course cannot happen when an electrolytic is being used as an audio coupling capacitor, because the voltage across it does not change significantly during any cycle of normal audio frequency: if it did then it would act as a low-cut "filter". Of course, no-one in their right mind

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would attempt to define a critical time constant using a wide-tolerance electrolytic, though I do wonder quite how well Mr Armstrong understands this point.

It should also be unnecessary for me to point out in a journal of WW's calibre that the reason op-amps do not saturate themselves with their own offset voltages is because they have d.c. negative feedback, not despite it.

Mr Armstrong's next point surprises me; if any preamps have been built using nothing but non-polar electrolytics, then I should think they were very expensive and bulky. All a waste of money too, because this faked "electrolytic capacitor cross-over distortion", which is, I assume, what he means, simply has no existence in reality. Any old electrolytic will pass an audio signal with less than 0.001% harmonic distortion (the limit of my Sound Technology testgear) and no questions asked. I fully understand that many people will consider sinewave testing hopelessly unhip, and will claim that this alleged audio degradation mechanism, like so many others, is only audible on critical listening to music of a specified genre. However, like many engineers, I find it hard to believe in a degradation mechanism that is intelligent enough to tell the difference between music and sinewaves, and only mangle the former. I can imagine that a complicated circuit could be devised with this property—a "pathological amplifier", but I do not see how such an inevitably complex mechanism could lurk inside a humble capacitor.

Similar objections apply to the mysterious failings in non-gold connectors. While it is in theory possible for a rectifying contact to be set up, in practice it just doesn’t happen; if it did it would be instantly audible as gross distortion. It is instructive to set up the above-mentioned testgear with the oscillator output returned to the analyser input via the connector under test, and to attempt to generate distortion (even 0.001% would do) by loosening or maitaining it. Having failed to produce a convincing rectifier from a series of ancient connectors, and various scraps of oxidized wire, I was eventually driven to using a rusty iron nail as one contact. This was capable of generating some second-harmonic distortion, but while it may be relevant to crystal sets it has nothing to do with hi-fi.

There is no point in worrying about electrolytics or connectors in the signal path. Not only are they normally harmless, but any signal your hi-fi system is likely to encounter will have already passed through hundreds of both in the recording process. The complexity of modern mixing desks and multi-track recorders is such that only real, rather than mythical, engineering considerations are given house-room.

Mr Armstrong, like all too many hi-fi enthusiasts, has come on strong with assertions but without a single shred of objective evidence.

D. R. G. Self
London E3

XY PLOTTER

I was most interested in the article on constructing a cheap X-Y plotter in the January issue of Wireless World and in the follow-up letter on drawing straight lines in the subsequent issue. You may be interested that a complete straight line drawing program is to be found in the Sinclair ZX81 BASIC Programming manual on page 121. This is the first edition dated 1980 – I have not checked that it is still in there in any subsequent reprints. I have implemented this program in machine code on the Wireless World Nanocomp, two of the 7-segment displays being used to indicate the rotation of the stepper motors.

I understand that this is an implementation of a Digital Differential Analyser algorithm (it integrates a constant). It would only need a second routine with an inverter to draw circles or parts of circles, this being a digital equivalent of a sine/cosine generator using two integrators and an inverter (I am an analogue computer enthusiast myself). Maybe there is someone out there who may like to investigate?

M. D. J. Foreman
Department of Computer Studies
Bristol Polytechnic

FUEL LEVEL SAFETY

I am concerned about the safety of the "Fuel-level indicator" Circuit Ideas, (January 1984). When used with liquids like petrol, precautions to prevent a static discharge from the tank to the "outer copper tube" should be taken. The connections to the copper tubes comprising the sensing capacitor should be in a vapoour-free region, lest a mechanical failure occurs while the circuit is live.

C. D. H. Williams
Durham University

PREFERRED HISTORY

I'm afraid that both Watson (November 1983) and Scott (January 1984) impute too formal a construction of the preferred value series. It has, by the way been variously called the stepped incremental series, logarithmic and exponential series. Many laws could no doubt be fitted closely to the values but that is not how the system was designed.

At the outbreak of the 1939-45 War, the standard series for resistors was 10, 15, 20, 25, 30, 35, 40, 45, 50, 60, 75, 100. From these 35, 45 were frequently omitted by manufacturers. These omissions were of academic interest only, since designs called for almost any value required viz. 140 or 2300 or 37500, which values were generally found by selection.

However the rapid build up of sophisticated electronics in 1940 to '45, saw industry being slowly choked by demands for large quantities of outlandish valued resistors. The process of selection had been passed back from the user to the manufacturer, and action had to be taken to relieve the situation. The same of course was happening in other components, particularly valves.

In October 1941, the MAP, MOS, and Adm. set up the Inter-Services Component Committee. With representatives in the design establishments, it was intended to control the supply of components, and to prevent wastage of manufacturing effort. One of its aims was also to standardize on components, to simplify stockholding by the Services supply branches, and to simplify servicing. One of its early tasks, through its technical committee ISTEtech C was to try to devise a value series, and at the same time reduce the number of values in the basic (20%) series.

A number of draft proposals were made in a memorandum sent to the Design Establishments, TRE, ADRDE, RAE and ASEE, as well as equipment manufacturers. There were many uncomplimentary remarks thrown around concerning what many considered to be interference, until it was realised that (a) the ISCS meant business and (b) ultimately standardization would be in the interest of designers as well as the War effort in general.

The initial series hinged around the R x 5 1/5 sequence. When explored this gave a reasonable series at the lower end of the scale: 10, 15, 22.5 (rounded to 22) 33, but from here, the scale widens 49.5 (rounded to 49), 73.5 (rounded to
73) and 109.5. Clearly the range should fit into the decade better.
Possibly a disproportionate amount of effort was put into the problem, remembering that we were in a crucial stage of the War, and that if any real benefit was to come out, the solution had to be found quickly, as otherwise it would be too late to affect production within the foreseeable future. In the meantime vast numbers of new equipment items were being designed using the decimal series.

One event however concentrated the minds wonderfully. A ship carrying a bulk consignment of resistors from the USA was sunk. Many equipment items were intended to be totally provisioned by this consignment, but one of them was the GL3 (AA No 3 MK2) which required over a million resistors mainly for the Presentation display unit. Immediately, The Rankophone Co. (EMI), who were responsible for the PU and already resistor manufacturers on a relatively small scale, set up a vast crash programme to produce not only those components themselves, but also to study other manufacturers. They used the spiralised carbon process and I enclose some samples of the resistors made at that time, including also some wirewound ones (on glass).

In expanding production the company produced preferred series of their own for use by their own designers, arguing that any decimal value could be satisfied within its tolerance by the nearest preferred value. Their series was 10, 15, 23, 37, 68, 100 in the values 23 and 32 could equally have been 22 and 33: they were simply the nearest whole numbers to 20, 25 and 30-35 respectively. Similarity 47 is the near equivalent of 45 and 50, and 68 that of 65 and 70. The important thing however is the recognition that it is possible to build a series built on tolerances.

In the meantime other thoughts had also turned to the use of tolerances to delimit the series, using the tolerance limits to touch or just slightly overlap. Thus any value resistor as manufactured could be assigned a unique value, within its tolerance. If we consider the 20% series the following are the possible figures:

<table>
<thead>
<tr>
<th>Value</th>
<th>10</th>
<th>15</th>
<th>23</th>
<th>37</th>
<th>68</th>
<th>100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>10 15 23 37 68 100</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

In most cases however, the +20% tolerance of the higher choices (69-73) exceeds 80 (+100–20%) by substantial amounts. If the tolerance band overlaps are minimized and equilized, the most likely series becomes 10, 15, 22, 33, 47, 68, 100. Similar methods can be used to fix the 10 and 5% series.

The preferred value list was promulgated in late 1942 or early 1943 and was published in WW and other periodicals in March 1943 (WW vol. 49 no. 3 page 71). The scales were not so much in mathematical, but were good old compromise born of the necessity to simplify manufacture. They were, even so, too late to have a significant effect during the War. They became however lastingly effective for resistors, but although capacitor lists have quoted the standard values since the 1950's, it is only in the last few years that they have become almost universal. Though there were still continued murmurings about different scales (see for instance Bowen, WW vol. 50 no. 8 August 1944 page 253).

The arguments about the basic structure of the E series have flared from its early days, but one of the most effective explanations came from 'Cathode Ray' in WW in 1952 'Why 47' (vol. 59 no. 2. page 77).
Donald H. Tomlin
Malvern
Worcs

**GPIB/IEEE488 INTERFACE**

It was with great interest that we read the article by A. G. Ray in your February issue, entitled "An IEEE488 Interface for the BBC Micro," and we totally agree that the BBC machine with an IEEE488 interface is a powerful combination for automated testing and measurement.

However, we were most surprised to learn that this was the first IEEE 488 interface available for the BBC Micro, since we have been manufacturing and marketing such an interface for more than six months!

Our interface, the CST Procyon, has been extensively featured in the electronics press, and Wireless World itself has carried advertisements for it. So it was some shock to learn that Mr Ray was unaware of its existence.

From the information given in his article, it would appear that Acorn's design philosophy has been different from our own in that we have tried to make our interface easy to use. To appreciate the difference between the interfaces, it is only necessary to compare the article's example program with an equivalent one for our own interface.

1. **DISC**
2. result%=OPENOUT("RESULTS")
3. **IEEE**
4. 90 siggen%=7
5. 100 dvn%=3
6. 110 FOR frequency%1000 to 10000 STEP 100
7. 130 PRINT#siggen%,"0.1V","+",STR$(
8. (frequency%)+"Hz"
9. 160 INPUT#dvn%,reading$
10. 180 response=20*LOGVAL((reading$(0.1*0.7071))
190 **DISC**
200 PRINT#result%,freqency%,
210 *IEEE
220 NEXT frequency%
250 **DISC**
260 CLOSE
270
There are three principal areas in this example where the CST Procyon Interface is simpler to use than the Acorn.
1. When the interface is initialized, the Procyon makes sensible default assumptions - these make it unnecessary to include lines 60 to 80 of the Acorn program.
2. The organisation of channel and file handling is different: the Procyon handles all device addressing automatically, so, when a string is sent to a device, the interface unaddresses any previous listeners and then addresses the target device to listen. This removes the need for a separate command channel and lines 40, 50, 120, 140, 150 and 170 in the Acorn program are unnecessary.
3. The Procyon provides simplified file handling for use with devices with single primary address these are automatically opened when the interface is initialised and may be used without further use of the OPEN command.

We understand from Mr Ray that prototypes of the Intelligent Interfaces design, complete and working, reached Acorn as long ago as November 1982. No changes were made for the production units, the first of which were delivered to Acorn in November 1983.

Though it is perfectly valid to do so. This simplification allows us to eliminate the OPEN and CLOSE commands in lines 90 and 100, 230 and 240.

These simplifications will make programs considerably shorter and much easier for the uninitiated to understand.

Polling is another area in which the Procyon is simpler than the Acorn: serial and parallel polls are both easily and quickly done using the BGET# command on special channels allocated by OPEN.

For a serial poll: (of device 7)
serial poll = OPENIN(1950 "SA7")
response = BGET# serial poll and for parallel poll: (of all devices)
parallel poll = OPENIN(1950")
response = BGET# parallel poll

The Procyon interface also allows all bus commands to be sent individually. Here, we use a different operating system interface - the "Commands" or command line interpreter OSCLI. We also use the mnemonic recommended by the IEEE488 standard, rather than the cumbersome Acorn command strings:

Acorn - PRINT %cmd%, "LOCAL LOCKOUT"
CST Procyon - 1.LO

Many powerful operating system features of the Procyon can be used because of its similarity to such filing systems. The commands "LOAD" and "SAVE" may be used to move blocks of binary data, with a maximum rate of over 50 kilobytes per second; the "SPOOL" and "EXEC" commands and the DFS utilities "DUMPS", "INF", "CAT", etc. may be used in the same way as other filing systems.

Users who wish to use the interface as a simple talker/listener are given full software support rather than being left with the vague advice to PEEK/POKE into hardware registers.

The Procyon uses secondary addresses to select between the various functions which are implemented. One selects the filing system on the device and this can be used for transferring programs and data between BBC machines and other computers. It is both faster and more standardised than the RS432 interface.

Another secondary address sends incoming characters to the device machine as standard for all other filing systems software support is also provided for passing control of the bus from one controller to another.

Assembler programmers have a choice of using the standard filing system calls in the "usual" way, which is sufficiently straightforward to be worthwhile in the Procyon system, or they can use a low level interface corresponding to the mnemonics star commands, but accessed through calls to Osbyte 139 (*OPT).

The Procyon interface is available in a special version optimised for use with CBM disc as an alternative to the disc filing systems and allows for use of CBM hard disc units. Support is also provided for the widely used Torch Z80 second processor within the standard interface. A bus analyzer rom will also be released shortly.

The many features of the Procyon Interface are fully explained and documented in a 130 page manual, which includes a tutorial section to help the novice user through the first steps of setting up an IEEE488 system.

Guy Jennings
Procyon Research Ltd
Martin Barnes
Cambridge Systems Technology.
The GPIB, HPIB, IEEE-488 or IEC625 bus is well known and widely used because of the ease with which it may be used to interconnect many peripheral devices. GPIB-compatible devices are made by many manufacturers and range from printers and disc units to industrial power controllers, network analysers and digital multimeters. A dozen or so of these devices are simply attached to one computer or controller using the specially designed connectors which can be plugged into each other. The 24 wires which make up the bus simply run in parallel from one device to the next. The main disadvantage of the bus is that only one controller may be connected to the string of peripherals at one time. However, with the GPIB combiner described in this article, up to six controllers can be linked via separate 24-core cables. A single 24-core cable leads from the combiner to the peripherals which are “daisy-chained” in the usual manner.

The prototypes for this design have been in use for over three years where a varying number of CBM Pet computers have needed to be connected to a varying number of printers and disc units. They have been very successful and the users are rarely aware of the existence of the combiners. However, the Pet does not use all of the functions which are provided for in the IEEE definition of the bus (in particular the serial and parallel poll sequences) and I cannot guarantee that the combiner will work with controllers built by other manufacturers.

Table 1 shows the designations of the 24 lines which make up the bus. The 16 signal lines all use negative logic, i.e. zero volts is logic one. At each device on the bus, each line is driven by an open-collector buffer and at each buffer there is a two resistor arrangement to pull up the line to about +3V when the transistor is off (Fig. 1). In this way all lines of the bus are nodes of a wired-or gate. That is, any device can pull a particular line low, but it is only when all devices are not pulling a line to zero that it floats high. The high state is also the idle state for all lines.

The operation of most of the lines of the bus is not altered by the functioning of the combiner and so a full description of the bus is not presented here. An accurate and readable description of the working of the bus is given in the references.

The bus functions by entering various modes in which different devices have control over different lines. For most communications, only four states are used. These are:

- **Idle mode**: this is the quiescent state which must exist before any communications can occur. All lines are high except possibly for remote enable (DEN) which is hardwired low is some systems. In particular both ND AK and NRF D are high, a state which can always be used to detect the idle mode.
- **Device talker mode**: in this mode the controller is receiving a string of bytes from a device connected to the bus. The bytes are transferred along the bus on the eight data lines DA0-DA7. Handshaking is performed using the three wires ND AK, NRF D and DAV. The talking device drives DAV while the controller drives ND AK and NRF D. When the talker comes to send the last byte in the string, it also pulls EOI (end of identity) low. EOI is normally high. The controller recognizes this signal and will then prepare to terminate the data transfer and return to idle mode.
- **Device listener mode**: this is similar to the talker mode except the controller and device swap control of the lines NRF D, ND AK, DAV, DAV-DA7 and EOI. Hence bytes are transferred from the controller to the device. (Many devices such as printers are listen-only devices.)
- **Command mode**: it is likely that more than one device will be connected to the bus, and so before communications can take place the controller must transmit information to select one (or possibly more) of the devices present. Also, many physical devices have several logical registers within them and these too must be distinguished. The solution is to give each physical device a distinct device address (or device number). The different registers within a device are also given a number – the secondary address. Both halves of the total address are integers in the range 0 to 30. It is this information that is sent in command mode. Command mode can always be identified by ATN (attention) being low.

### A typical transaction

A transaction is the complete sequence of events from leaving to returning to idle mode. Table 2 shows the steps of a typical sequence – the reading of one line from an open disc file or a paper tape reader. Ten separate events have been identified starting in the idle mode at event one. For each event shown, the lines DAV, NRF D and ND AK complete one handshake cycle and the byte shown on DA0-DA7 is transferred from one device to another. The byte on DA0-DA7 is true when DAV (data valid) is low. All transactions start when ATN goes low as in event two.

**Event 2**: the controller puts ATN low to wake up all devices and command mode is deemed to have been entered. All devices have to respond at this point since they do not yet know which of them is to be addressed in the coming transaction. Each device temporarily enters device listener mode (although this is more properly called acceptor handshake).

The controller now sends out a command byte selected from Table 3. In this example the transaction will be data coming from a device to the controller, so the

---

**Table 1. GPIB line designations**

<table>
<thead>
<tr>
<th>Pin name</th>
<th>Type</th>
<th>Mnemonic</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Data</td>
<td>DA0</td>
<td>Data 0 (least significant)</td>
</tr>
<tr>
<td>2</td>
<td>Data</td>
<td>DA1</td>
<td>Data 1</td>
</tr>
<tr>
<td>3</td>
<td>Data</td>
<td>DA2</td>
<td>Data 2</td>
</tr>
<tr>
<td>4</td>
<td>Data</td>
<td>DA3</td>
<td>Data 3</td>
</tr>
<tr>
<td>5</td>
<td>Control</td>
<td>EOI</td>
<td>End of identity</td>
</tr>
<tr>
<td>6</td>
<td>Handshake</td>
<td>DAV</td>
<td>Data valid</td>
</tr>
<tr>
<td>7</td>
<td>Handshake</td>
<td>NRF D</td>
<td>Not ready for data</td>
</tr>
<tr>
<td>8</td>
<td>Handshake</td>
<td>ND A K</td>
<td>Negative data acknowledge</td>
</tr>
<tr>
<td>9</td>
<td>Control</td>
<td>IFC</td>
<td>Interface clear</td>
</tr>
<tr>
<td>10</td>
<td>Control</td>
<td>SRQ</td>
<td>Service request</td>
</tr>
<tr>
<td>11</td>
<td>Control</td>
<td>ATN</td>
<td>Attention</td>
</tr>
<tr>
<td>12</td>
<td>Control</td>
<td>REN</td>
<td>Remote enable</td>
</tr>
<tr>
<td>13 or A</td>
<td>Data</td>
<td>DA4</td>
<td>Data 4</td>
</tr>
<tr>
<td>14 or B</td>
<td>Data</td>
<td>DA5</td>
<td>Data 5</td>
</tr>
<tr>
<td>15 or C</td>
<td>Data</td>
<td>DA6</td>
<td>Data 6</td>
</tr>
<tr>
<td>16 or D</td>
<td>Data</td>
<td>DA7</td>
<td>Data 7 (most significant)</td>
</tr>
<tr>
<td>17 or E</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>18 or F</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>19 or H</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>20 or J</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>21 or K</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>22 or L</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>23 or M</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>24 or N</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
</tbody>
</table>

---

**Fig. 1. In full circuit of the combiner only one control section is needed but a separate interface section is needed for each user.**

---

**by David J. Greaves**
upper three bits of the command byte are 010. Since the device number that data is being read from is eight, the other five bits are 01000. This byte is communicated to all devices on the bus using a standard DAV, NRFD and NDAK handshake.

**Event 3:** this event occurs only when a secondary address is needed. Again a command byte is selected from table three, but this time the top three bits are 011. This tells the device that the low-order five bits are the secondary address to be used for the forthcoming data transfer. Only the device which recognized its device number during event two will need the secondary address, but all devices handshake the bus while ATN is still low — they are watching out for their own device number. It is because more than one device can be handshaking the bus at one time that the open collector, wired-or structure is used.

At the end of event three the controller puts ATN high and the remainder of the devices which were not selected return to idle mode.

**Event 4:** since this is an example of a device talking to the controller, the controller is now waiting for the first data byte from the addressed device. It sets up NRFD and NDAK and waits for DAV to go low signifying that the byte is present on DA2-DA7. If DAV does not go low within a reasonable length of time then the controller can only assume that device eight is broken, switched off or non-existent.

**Events 5-8.** The controller goes on reading bytes for as long as it likes. The device sourcing the data cannot stop sending bytes even if it has run out of data — it must pad with nulls. However it can indicate that it would like to stop with the EOI on. On the CBM Pet the Basic variable ST is set to 64 when an EOI is detected. If the program then continues fetching further data with, say, an INPUT# or GET# statement then ST is set to 2.

**Event 9:** when the controller has had enough data it again puts ATN low to re-enter the command mode. All devices set up NRFD and NDAK in order to receive a command byte. The controller sends 5FH which is the untalk command.

**Event 10:** finally, the controller puts ATN high. All lines are now in idle mode ready for the next transaction.

**Logically connected transactions**

Consider the case where a program has been written on the controller to transfer a file from one device to another, one byte or line at a time. This might be the case when listing a disk file on a printer. In the original IEEE488 standard there is provision for such a process to be set up by the controller and run as a single transaction. However, the average user will not bother to consult lengthy texts to find out how to do this. Instead he will write a simple program such as

```
 40 INPUT #1,A5
 50 PRINT #2,A5
 60 GOTO 40
```

This uses two separate transactions for each line of the file and although this is not particularly undesirable, it does cause the bus to pass through idle mode many times during the execution of the program.

From the point of view of the combiner the only way that it can detect that a user has finished with the bus is the presence of the idle mode. However, in this example, the user has not finished and will be immediately submitting another transaction. It is undesirable that another user should interrupt and gain control of the printer (say) during an idle period half-way through the first user's job.

The combiner overcomes this problem by providing a special re-admit period. This is an interval of about 1.5 seconds after a particular user has finished a transaction during which that user alone can submit further transactions. If he has no further work to do then the next controller that is queued is allowed to proceed; or if there is none, the bus becomes free.

There is a disadvantage of the re-admit period: when two users are quite separately using two peripherals it works out that one of them is continually waiting for a 1.5 s gap in the other's transaction stream. Only then can they swap roles.

**Circuit description**

The combiner consists of eight sections: six interface sections, one control section and a power supply. The sections are interconnected by an internal bus and most of this bus also leads directly off to the peripheral devices. Figure 1 shows one interface section, the control section and the internal bus.

The interface sections are very simple as all except two of the signal lines from the controller lead directly through it to the internal bus. DAV and EOI are only connected through to the internal bus when a particular interface section is enabled by the control section. EOI must normally be isolated because of a limitation on the early Pet computers. To prevent excessive flicker on the Pet screen when scrolling was taking place, a programmable output pin was connected so that the screen could be blanked, under software control, during scrolling. Unfortunately, when all of the outputs from the computer's three versatile interface adaptors (v.i. as) had been assigned, there was none left to use for this blanking signal. Instead, the pin that controls EOI on the g.p.i.b. connector was used for this purpose as well. The two consequences are that the screen sometimes blanks when using the bus and that the computer produces an extraneous EOI pulse every time the screen scrolls. The EOI half of the interface section is therefore provided to stop these spare pulses from interrupting other users' transactions.

The DAV half of the interface section is provided so that the combiner can pull a

---

**Table 2. Typical sequence of bus events making read up a bus transaction: reading the line BLUE <CR> from device 8, register 4, in this example.**

<table>
<thead>
<tr>
<th>Event</th>
<th>Mode</th>
<th>Control of</th>
<th>Data on</th>
<th>ATN</th>
<th>EOI</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>idle</td>
<td>command controller</td>
<td>00-all high</td>
<td>high</td>
<td>high</td>
<td>Guesiessent state Controller requests that device 8 should talk</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>all devices</td>
<td>48H</td>
<td>low</td>
<td>high</td>
<td>'Secondary address'</td>
</tr>
<tr>
<td>3</td>
<td>command controller</td>
<td>all devices</td>
<td>64H</td>
<td>low</td>
<td>high</td>
<td>Data B</td>
</tr>
<tr>
<td>4</td>
<td>talker</td>
<td>device 8 controller</td>
<td>42H</td>
<td>high</td>
<td>U</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>talker</td>
<td>device 8 controller</td>
<td>56H</td>
<td>high</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>device 8 controller</td>
<td>45H</td>
<td>high</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>device 8 controller</td>
<td>00H</td>
<td>high</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>all devices</td>
<td>5FH</td>
<td>low</td>
<td>high</td>
<td>return</td>
</tr>
<tr>
<td>9</td>
<td></td>
<td>all devices</td>
<td>00</td>
<td>high</td>
<td>high</td>
<td>Controller commands UNTALK</td>
</tr>
</tbody>
</table>
| 10    | idle | — | — | 00 | high | *

*If these were the last byte in a file, EOI would be low.*

**Table 3. Command byte meaning**

<table>
<thead>
<tr>
<th>DA7</th>
<th>DA6</th>
<th>DA5</th>
<th>DA4</th>
<th>DA3</th>
<th>DA2</th>
<th>DA1</th>
<th>DA0</th>
<th>Interpretation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>n</td>
<td>n</td>
<td>n</td>
<td>n</td>
<td>n</td>
<td>Cause device nnnnn to go into talk mode</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Untalk command</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Cause device nnnnn to go into listen mode</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>n</td>
<td>n</td>
<td>n</td>
<td>n</td>
<td>Use secondary address nnnnn</td>
</tr>
</tbody>
</table>

Note: 'nnnnn' is a five-bit binary number in the range 0 to 30. Device number 31 is illegal.
controller’s DAV line low without pulling the DAV line of the internal bus low. The interface section holds this low unless it is enabled, in which case it connects it to the internal bus. When a controller wants to use the bus, the first thing it does is to test its DAV line to see if it is high. If the controller finds it low, it sits in a software loop until it does go high. This loop or “hang” is the basis of the combiner’s queuing system. Because the interface sections are not normally enabled, when a controller wants to start a transaction it normally finds DAV low and goes into a hang.

Circuit IC1 in control section is the master clock and runs at a few hertz. Assuming the busy bistable (IC5a and IC5b) is clear, clock pulses are transmitted through IC2a into IC1. IC3 is a four bit counter and is decoded by IC4 so that the interface sections are each enabled in a “round-robin” fashion. If a particular controller has a transaction ready it will see DAV go high as its interface section is enabled and put ATN low (event 1). ATN is connected to IC4 and this sets the busy bistable, stopping IC3 at its present count.

Some Pet users have effected the facilities provided by this combiner purely by modifying the g.p.i.b. handling software within their computers. However, this approach has a number of drawbacks, among which is the problem IC9b is designed to solve. What can happen is that the software checks that the bus is in idle mode (i.e. not being used) and then starts its transaction with the assertion of ATN. Meanwhile, on another user’s machine the same software can be running just a few microseconds further on. Because time must elapse between the execution of the idle mode check and the execution of the instructions which assert ATN, both controllers get the impression that the bus is free and both assert ATN at once. On the combiner described here, there is a safety period of one clock cycle after an interface section has been enabled and then disabled during which the controller can still assert ATN and gain control of the bus.

The buffers in the interface sections are bidirectional and need to know whether it is a controller or a peripheral device which is driving DAV and EOI. This information is sent along the TX lines which are controlled by IC10b in the control section of the combiner. If ATN is low then it is command mode and the controllers drive DAV and EOI. IC9 is a 3-to-8 line demultiplexer and provides a simple way of recognizing the command bytes that the controllers send. In fact it is a bit too simple since it does not work with device numbers in the range 16-30! A more complex detector must be used instead of IC9 if it is desired to use these device numbers. The direction bistable (IC10c and IC10d) is set depending on whether a talk or listen command byte is detected and when ATN again goes high at the end of the command mode (event 3 in the example) the TX lines take up the information from this bistable.

All the circuitry in the combiner remains passive until the command mode is again entered at the end of the transaction. When either the unlisten or untalk command byte is sent, IC9 detects it and sets the completion bistable (IC1a and IC1b). IC9a, another four bit counter, and IC1b together form a retriggerable monostable capable of high duty cycles. Whenever ATN goes low, IC9 is reset, and when it goes high, clock pulses from IC1 feed through IC1b causing it to count up until it reaches 15. This takes about 1.5 seconds and provides the re-admit period after ATN has gone high and the bus finally returned to the idle mode. If no new transactions are started by the enabled controller during this period, then the completion bistable will still be set and the busy bistable will be cleared. The circuitry which does this is IC8c and IC7. However, continued on page 62.
Plymouth satellite tv system bounces back

Despite the setback of being rejected by the Part report, the direct broadcasting by satellite system developed at Plymouth Polytechnic has just been successfully demonstrated. The development team from the Polytechnic's communications engineering department is led by Dr Martin Tomlinson. At the time of the Part report, Dr Tomlinson said "Given the funds, I have no doubt that we could meet the deadline [1986] and offer the UK a system that could put us ahead of the world in satellite tv broadcasting long into the future. Most of the technology required for our system already exists." He has since said that funds have been obtained from an undisclosed US source, and the successful test was carried out using a NATO satellite. This makes a nonsense of the Part rejection of the system which found it "elegant and ingenious" but claimed that there was not enough time to meet the deadline. There are two years left for "fine tuning".

Part selected the IBA's Multiplexed Analogue Component (Mac) system. A licence to operate two channels of d.b.s. was granted to the BBC, but they have been unable to reach an agreement on standards with other European broadcasters and have virtually abandoned the project.

Details of the system were described by Dr. Tomlinson in our issue of January 1983. In essence it separates chrominance and luminance signals and transmits both. Each signal is quantized into sixteen amplitude levels and coded into a digital signal. At the same time an error signal from the quantization process is generated. Sound channels are transmitted separately as a 2Mbit/s stream digital signal and there is an additional 2Mbit/s data stream provided. The luminance, chrominance, sound and any data signals are time-division multiplexed into a composite 60Mbit/s digital stream. The analogue quantization error signals are also time-division multiplexed and are then phase modulated onto the carrier at a low level along with the digital bit-stream so that analogue and digital components are all transmitted together, using the same carrier. As the analogue modulation is at a low level, no error is caused in the digital information. At the receiver fairly simple demodulating and demultiplexing circuits recover the signals and they are converted back to analogue form with the quantization error signal, used for correction, re-imposed on the signals. The system offers, it is claimed, very high bandwidth and signal/noise ratio on both luminance and chrominance with no crosstalk between them. Encryption for subscription TV services may be easily provided. Dr Tomlinson is now confident that this is by far the best system yet devised and has high hopes that it will be accepted internationally.

Dish antenna allows denser satellite spacing

A smaller dish aerial with an improved performance will enable more countries to use more communications satellites, according to British Telecom, who designed it. The 5.5m-diameter dish is based on the geometry of an optical telescope invented by James Gregory, a 17th century Scottish mathematician, and the design is known as Offset Gregorian. The traditional design of earth terminal aerials has been based on Cassegrain geometry, with a parabolic dish, a convex subreflector and a feed usually placed symmetrically in the centre of the dish. This works well for large, 8m or more, diameter reflectors but the performance falls off as the diameter is reduced. The Gregorian design uses a shallower parabolic dish, an offset concave subreflector and an offset feed to give a performance at least as good as that of larger diameter Cassegrain aerials.

Placing the subreflector and its supporting structure to one side eliminates the block to power caused by the subreflector. It is possible to achieve a narrower beam with reduced sidelobes. This will become important if plans by Intelsat are put into operation. At present there is a limit to the number of satellites which can be placed in equatorial geosynchronous orbit. A slot is provided every 3° allowing a maximum of
120 positions. The proposal is that the angle be reduced to 2°, creating an extra 60 locations. This would reduce the distance between satellites from 2,200 to less than 1,500km and would require earth station antennae to produce narrower beams to avoid interference between satellites. The new design meets these requirements.

The 14GHz up-link has a 5dB beam width of 0.27°, which means that when it reaches the satellite the beam is only 336km wide. Radiation at angles greater than 1° from the beam axis is at least 10dB less than from a conventional antenna. The offset design also gives a lower angle of elevation for a given beam angle. In the illustration, the beam angle of elevation is 30° while the dish elevation is only 20°. This helps to reduce wind loadings and makes it less obtrusive. Erected on the roof of a BT building in Ealing, London, the first use of the antenna will be on a transatlantic digital transmission service, Sat-Stream.

Is European electronics beaten?

"Common Market countries will have to regard each other as friendly partners, rather than foreign threats, if they are to have any hope in catching up with their non-European competitors in the electronics industry," says Ian Mackintosh, head of the market research organization that bears his name. Each nation," he said at a recent conference in Milan, "must create a national strategic plan for electronics, which is fully in tune with the overall interests of the European Community. Only then can the European companies have any hope of fighting back to a position of parity with such competitors.

"Over the last 20 years or so, the electronics industry in Europe has increasingly fallen behind the rapid pace set by companies in the US, Japan and some parts of SE Asia, so that today, with only a few honourable exceptions, Europe's electronics companies are no longer leaders in terms of either market share or innovation."

Dr Mackintosh pointed out that although there were potentially formidable resources of finance and talent, these had been dissipated by management failure and financial caution, compounded by governmental indifference. Looking at a ten-year forecast of worldwide markets and production, he predicted an electronics trade deficit in the European Community of $16 billion by 1992.

Operated by voice-entry terminal, microcomputer, disc drive and voice synthesizer, this voice-activated domestic appliance demonstration system cost about £3000 to build, though it is expected that production systems could be sold for under £1000. A vocabulary search is made prior to using the voice print which is built up over a period of training sessions. Initiated by Mal Hyams for the DTI travelling exhibition The Concerned Technology, the system was constructed in six weeks by Voice Input Ltd of St Ives, Cambridgeshire.

Ultrasonic eye probe

An ultrasonic data imaging and recording system for an eye scanner has been developed at Harwell for use in the Moorfields Eye Hospital. The scanner was originally developed in the mid-70s and has been used in the clinical diagnosis of eye disorders. In operation a low-energy pulsed beam of ultrasound is scanned in a raster movement across the eye; the reflected signals may then be recorded and processed to give an image of the interior of the eye.

The new system can display the images directly on to a standard TV screen and they may be recorded using a standard video recorder. The image processing equipment consists of a dual memory unit through which the captured data is transferred to a temporary store. Subsequent processing involves co-ordinate plotting and transfer of the data to a picture store for manipulation and display. The system makes extensive use of programmable circuits which allow variations of scan and of picture presentation to be made by simple changes in software. It is built around an LSI-11 computer.

A key element of the system is the development of video synchronisation techniques which will ensure that the processed data emerges as a genuine video signal, compatible with any standard unmodified v.c.r. This development overcomes the main criticism of ultrasonic inspection methods, that they were very inconvenient to use. The system has applications in industrial non-destructive testing. Indeed it was the NDT Centre at Harwell that developed the system. For on-site testing the raw scanning data can be recorded on a v.c.r. for later processing and display.

Coax centenary

Just one hundred years ago, Werner Siemens described a new method for constructing an induction-free cable. "It consists of individual conductors covered by a sheath which forms the common return conductor," he wrote to Ludwig Lüffler. The concept was patented in Germany on March 27, 1884, as a solution to the problem of "induction-free cables of lightweight design." It was not until the Berlin Olympic Games in 1936 that a coaxial cable was put to a practical use when a link was set up between Berlin and Leipzig. By using a carrier wave it was found possible to transmit 200 telephone calls and a tv signal simultaneously. Current techniques using an 18-core cable permit the transmission of 100 000 calls and 18 tv signals.
Receivers for amateur tv
Licences have been granted for five amateur tv repeater stations to be established in the UK. As they are all set in the 1.2 to 1.3GHz allocation, it is thought that this will lead to a much wider use of the band and preserve it for the amateur service.

<table>
<thead>
<tr>
<th>Callsign</th>
<th>Location</th>
<th>Channel</th>
<th>Vision freq. (kHz)</th>
<th>Sound freq. (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GB3GV</td>
<td>Leicester</td>
<td>RMT-1</td>
<td>1276.5</td>
<td>1311.5</td>
</tr>
<tr>
<td>GB3UT</td>
<td>Bath</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GB3TV</td>
<td>Luton</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GB3UD</td>
<td>Stoke-on-Trent</td>
<td>RMT-2</td>
<td>1249.0</td>
<td>1318.5</td>
</tr>
<tr>
<td>GB3VR</td>
<td>Worthing</td>
<td></td>
<td>1255.0</td>
<td>1324.5</td>
</tr>
</tbody>
</table>

Receivers on channel RMT-1 will receive a.m. or f.m. signals and retransmit them on a.m. only. RMT-2 channels are likely to be f.m. only. Vision transmissions are 625-line, negative-going video with positive-going synchs. F.m. signals are limited to a 6.5MHz deviation with CCIR pre-emphasis. Sound frequencies shown in the table are for a.m. systems. F.m. systems will contain a 6MHz sound subcarrier. Aerial polarization is horizontal. It is expected that GB3GV, GB3TV and GB3VR are to be operational almost immediately. Further details may be had from the British Amateur Television Club, Telephone: 0533 600108.

Extra-long play compact disc
A new performance of Beethoven's Choral symphony, lasting 71 minutes, has been issued on one side of a compact disc. Although designed to last for up to 74 minutes, the discs have mostly been made with a playing time of less than one hour. One reason for this stems from the difficulty of achieving precision moulding in the outer areas of the disc (readers will recall that the disc is scanned from the inside outwards). Less-than-perfect mouldings can cause birefringence, a double refraction phenomenon that makes signal detection virtually impossible. The discs are injection moulded from the centre which is why it is difficult to get the right degree of accuracy at the outside edge. Denon engineers at the Kawasaki plant of Nippon Columbia Co. near Tokyo, investigated varying the temperature of the mould and the plastics and also the injection speed and pressure, and adjusting the thickness of the stamper. They believe that this will not only increase the playing time of the digital discs but also increase the overall precision of the recordings.

Farewell Westinghouse?
A system by which railway train brakes are actuated electrically rather than by air is being tested by British Rail. Trialling trials are being held and an electric actuator has been mounted in the bogie of a passenger coach in regular use between London and the West Midlands where it will be subject to all the normal shocks and vibration experienced by rolling stock. The actuator is being operated against a dummy load and plays no part in the braking of the train. Brake callipers are applied through a large step-down gearbox from a small d.c. electric motor. The motor is powered from a battery which is constantly recharged through the train's power supply. The motor has been designed to withstand the actuating current when in a stalled condition with the brakes applied. As with the air system, invented by George Westinghouse in 1872, a fail-safe approach means that the brakes are automatically applied in the event of a system failure. The electronic control of the system offers a stepped degree of brake pressure, switching a current to the actuator.

Save telecom industry say unions
Trades unions in companies manufacturing telecom equipment are joining the British Telecom Union in pressing parliament to adopt key amendments to the Telecommunications Bill that would protect British industry. They see their jobs at companies like Plessey, GEC, and STC as being at risk. The companies themselves have certain misgivings and Lord Westwood, chairman of GEC, is also pressing for amendments in the House of Lords. The amendments would stop overseas manufacturers selling telecom equipment in Britain while the markets in their countries are not open to British manufacturers. To open the British market to foreign competition without any reciprocal agreement would be catastrophic, according to a spokesperson for the various telecom communication workers unions.

Videoconference on videoconferences
Appropriately enough, the International Teleconference Symposium, to be held on April 3 to 5, links participants from four continents by satellite. In the first-ever live link-up on such a scale, those taking part will be able to see and hear each other from conference centres in London, Tokyo, Philadelphia, Sydney and Toronto. The London centre will be the Royal Lancaster Hotel, which will be fitted with large projection tv screens. Also at the hotel will be an exhibition of equipment and services. The symposium will be taking full advantage of the digital compression techniques developed in the UK which only transmits changes in a picture rather than the whole frame. The symposium also heralds the transatlantic teleconferencing services which will soon provide a link to Canada and later in the year to the USA. A service within Britain will also commence this year.

Despite their problems they can still join a union!
AmPALS — replacement for the NTSC system

Following the decision by the FCC to phase out the current 525/60 NTSC system, American broadcasters have been looking at PAL to see if its colour fidelity can be achieved without the drawbacks of the eight-field sequence. This report — leaked from the working party studying the competing systems — details the system most likely to be adopted.

Since the introduction of the PAL colour broadcast system, it has become clear that it does successfully overcome the major failing of the NTSC system, i.e. sensitivity to chrominance phase errors, but that a penalty is paid in the complexity of broadcast equipment designed to handle it. The major problems with PAL arise because of the quarter-cycle difference between subcarrier and line frequencies necessary to make up the chrominance spectrum spreading caused by the V-switch interleave with the luminance sidebands. This causes the PAL structure to have four-line groups of burst phase, whereby the sequence only repeats every eight fields. This causes difficulties in video editing where a four-field edit causes a 180° phase jump in the video, which timebase correctors convert into a picture shift to restore subcarrier phase to reference. A further difficulty is that the original PAL specification did not define the subcarrier H phase relationship, with the result that video tapes from different sources will not colour frame without adjustment to equipment.

The criteria by which the system has been designed are

- colour accuracy as good as or better than PAL
- four-field sequence length maximum
- use as many existing components as possible
- eliminate drop-frame time code.

It was decided that a phase-alternating system was mandatory to equal the PAL colour accuracy and eliminate the NTSC hue control. A novel approach has been used whose performance can exceed that of the PAL system. In AmPAL® the RGB camera signal is converted into the PAL U and V colour difference signals as normal, but the alternating line principle is achieved by interposing U and V on alternate lines. On even lines, U is horizontal in the phasor diagram and V is vertical, whereas on odd lines V is horizontal and U is vertical (a). Fig. 1(b) shows the resultant phase az as broadcast on successive lines, and (c) shows the signal az' as received with a phase error. This is decoded to ab, on the even line, and V is too small because of the phase error. On the odd line, however, az' becomes ad, and V becomes too large because of the phase error. Line averaging, as in (d), gives an almost correct V signal. Similarly, the line averaging of U gives an almost correct signal. As in PAL, the phase error becomes a saturation error not a hue error.

---

**Fig. 1**

**Fig. 2**

**Fig. 3** Subcarrier phases shown correspond with the AmPAL® definition of subcarrier H phase for video signals recorded on tape.

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Wireless World April 1984
Sonic pathfinder continued from page 29

subject moves. Only when he steps through the doorway is the user informed of the existence of the corridor wall. Indeed, it is only then that this information becomes relevant.

After introducing the Clamp it became necessary to reduce the maximum Ratchet hold time to 1.5 seconds. The voice of the Ratchet and the Clamp will not be perceived by the user during normal use of the Sonic Pathfinder. The various durations used in the algorithms have been chosen to correspond to those involved in human movement. Consequently the user does not, contrary to what might be expected from the above description, experience objects leaping in and out of his perception. There is only one weird side-effect; all objects disappear if the user walks backwards!

Since the aid uses only readily available components it is capable of being made relatively cheaply; current estimates suggest £50, leading to a final selling price of some £250. The final device would be powered by a 9 volt rechargeable battery and the user would have to plug in the charger for an overnight charge once a week. Training in the use of the aid would be provided by Mobility Officers of which there presently exists some 120 throughout the UK. Current experience suggests that some 15 hours of training will be necessary.

The work described in this paper was funded by the DHSS and carried out under the general supervision of Professor C. I. Howarth. Special thanks are due to the Unit technician, Carl Espin, who has helped in the assembly of numerous prototypes.

References

GPIB combiner continued from page 28

if a new transaction does start, either a talk or listen command will occur and reset the completion bistable. Then, when the readmit period completes, nothing will happen.

Because the re-admit period and "round robin" polling of the controllers both use similar circuits, there is an average latency of half the re-admit period on all one-off transactions, even if the bus is completely free. To overcome this, on one prototype a second NE555 counter was fitted running at about 150Hz. This was connected into IC2A instead of IC1 thereby increasing the response time. The colossal disadvantage of this is that the pretty display caused by the interface section i.e. d's flashing in turn is completely lost.

The two push buttons are termed clear and reset. Pushing "reset" generates an interface clear signal (IFC) and resets all devices on the bus. If any old-style Pet disc units are connected then they will need re-initializing. Pushing "clear" is generally a good way to get rid of a "bus-hogger".

Alternative interface sections
An alternative circuit for each of the six interface sections, Fig. 3(a) uses the MC3446 integrated circuit of Fig. 3(b). The MC3446 contains four-line driver-receivers specifically designed for interfacing with the bus, their equivalent circuit being exactly as shown in Fig. 1. The driver transistor is guaranteed to sink 48mA and an absolute rating of 150mA is specified.

If very long lengths of cable are to be used, then buffers similar to those already on EOI and DAV can be made up for the other lines of the bus. These extra buffers must still be enabled only when the enable line from the control section is low and must buffer in the correct direction depending on the TX signal. That is, DAV or DAV always go in the same direction as EOI and DAV and NDAK and NDAK always go in the opposite direction, ATN and REN always go from the controller to the peripherals and SRQ always goes from the peripherals to the controller. IFC is best neglected.

When one user is performing a large transaction such as printing a list on a printer, other users who are queued and awaiting access to the peripherals may change their minds and decide to do something else that does not use that peripheral. In this case some means of exiting from the queue or "unhanging" their controller is required. In the case of the Pet computer, pressing buttons on the keyboard is to no avail, the only solution being to unplug the g.p.i.b. connector from the rear of the computer. To reduce connector wear, it may be preferable to fit four pole push-to-break buttons in series with the lines NDAK, NRD, DAV and ATN. Operation of this switch has the same effect as removing the connector. The controller sees that DAV has gone high, asserts ATN, finds that NRD and NDAK are both high (an error condition) and aborts its transaction.

References

Improving colour television decoding
We regret that David Read's final articles describing a one-line PAL comb decoder have been postponed due to pressure on space. In the meantime you may be interested to read of the new PAL modifications proposed for North America, described on the previous page.
Digital-storage oscilloscopes

According to one market study digital storage is the fastest growing segment of the oscilloscope market. In 1982, digital storage represented 13% of the oscilloscope market and is expected to represent 33% by 1987.

In recent years faster ICs have led to the introduction of more and more oscilloscopes using semiconductor memory to store the waveform in digital form. In terms of flexibility, digital-storage techniques offer much more than is possible using an oscilloscope with a storage tube. They also allow extremely slow waveforms to be displayed, and indefinite storage. However, high-quality storage-tube instruments allow persistence of the screen to be varied, they are faster and they generally offer higher resolution. If waveform capture is the only facility required over the functions of a normal oscilloscope, storage-tube instruments can work out cheaper than digital ones; storage tubes and their drive circuits are complex but developments over many years have brought prices down.

Concepts of digital storage

In the digital storage oscilloscope, an analogue-to-digital converter changes the signal from the input amplifier into binary words which are stored in memory. Some manufacturers call this device a digitizer. The number of binary words produced in a given time – the sampling rate – is governed by an accurate timebase clock signal and determines horizontal resolution of the stored waveform (not necessarily the displayed waveform). This same clock drives a counter which steps through the addresses of memory locations to put each word sampled sequentially in the memory bank.

Vertical resolution of the stored waveform is determined by the number of bits in each binary word. Converters used in oscilloscopes are usually eight, nine or ten-bit devices giving a resolution of 256, 512 or 1024 steps respectively. Generally speaking, the more bits the converter has, the longer the conversion time, but there are ways of shortening conversion time by using two converters and sampling them alternately.

Once in memory, the stored waveform in binary form can be displayed by feeding it to a digital-to-analogue converter to drive the tube vertical amplifier. For each binary word clocked out of memory, a counter driving a further d-to-a converter is incremented. Output of this second converter forms a ramp which drives the tube horizontal amplifier. The waveform only has to be clocked out of memory fast enough to stop screen flicker so these converters, the tube amplifiers and the tube need not be high speed unless the oscilloscope has an analogue mode.

In practice, things are usually a lot more complicated than this because processing circuits are invariably included to improve fidelity of the reproduced waveform and the digital circuits lend themselves to the inclusion of many enhancements. Using just a d-to-a converter as described above, the display consists of a number of dots but as frequency of the input signal rises, the dots become further apart. With fast periodic waveforms this can result in a confusing display through a phenomenon called perceptual aliasing, i.e. one’s mind tends to join the wrong dots together. About 25 dots for every cycle of a sinewave are needed to present a recognizable display. To avoid this, interpolators are often included to join the dots. Interpolators are optimised to work best with either pulses or sinewaves, not both.

Due to the sampling method, trying to store and display signals at frequencies higher than the time-base setting permits gives strange and misleading results through aliasing. The simplest demonstration of this is to imagine a sine wave being sampled at periods exactly equal to one cycle of the sine wave. All the samples would be exactly the same and the interpolator would produce a tidy straight line. Shift one of the frequencies slightly and the results are even more confusing. To avoid this the sampling rate should always be twice as fast as the highest frequency in the signal. Anti-aliasing filters (similar to...
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bandwidth limiters but with a higher roll-off rate) may be used but obviously, these obscure part of the signal.

**Triggering**

One of the main features of a digital-storage oscilloscope is pre-triggering – the ability to trigger after or in the middle of an event rather than before as is the case with a conventional oscilloscope. Before triggering occurs in pre-trigger mode, the memory is constantly updated with the current input signal. When triggering occurs, the memory is frozen if the pre-trigger is set to 100%, or otherwise allowed to run for a set interval after triggering so the one can see what happened both before and after the trigger point.

There are many unpredictable types of fault that can be detected by a storage oscilloscope that can't be detected by any other means because of this feature. What happens just before a failure is usually much more important than what happens just after but the failure itself is the only trigger source. Pre-triggering also lets one see the initial section of a transient that is lost on a conventional oscilloscope because of the trigger-level setting and response time.

Digital triggering by setting the trigger level as a binary value and comparing it with the value at the a-to-d converter output is often used. This results in stable and repeatable triggering. Some oscilloscopes allow trigger hysteresis to be set and/or have a bi-trigger mode for use when one is not sure whether the transient to be captured is positive or negative.

**Digital-storage oscilloscopes**

<table>
<thead>
<tr>
<th>Model</th>
<th>Oscilloscope plug-in</th>
<th>Channels</th>
<th>Max vertical range (mV)</th>
<th>Resolution</th>
<th>Memory (Kbytes of word)</th>
<th>Analogue bandwidth (Hz)</th>
<th>Pre-triggering expansion factor</th>
<th>Horizontal expansion factor</th>
<th>Stored waveforms</th>
<th>Interrogation</th>
<th>Cursors</th>
<th>Average waveforms</th>
<th>GRPB</th>
<th>Graph order back trigger</th>
<th>Price £</th>
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* Depends on plug-in  
Not applicable  
Fitted as standard  
Optional
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Clifton Chambers, 62 High Street
Saffron Walden, Essex CB10 1EE
Tel: (0799) 24922 Telex: 81875G

Hameg Oscilloscopes Ltd. wish to remind readers that in addition to those listed last month, amongst their distributors are:

Electronic Brokers Ltd.
81/85 King's Cross Road
London WC1N 9LN
Tel: 01-833 1166

Audio Electronics (Cubegate)
301 Edgware Road
London W2 1BN
Tel: 01-724 3564

HRS Electronic Components
Brass House Pass I
Birmingham
Tel: 021-643 0705

Acro Instruments
PO Box 25
Wokingham, Beds

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01-661 3130
are either nine or ten-bit devices, rather than eight. A 4K-word memory in an oscilloscope using a ten-bit converter is larger than a 4K-word memory in an instrument using a nine-bit converter, or at least it should be.

Memory segmentation is usually possible, which means that more than one waveform can be stored at the expense of resolution (or stored at the same resolution at the expense of part of the waveform depending on how you look at it). Using 512 words of memory to store a waveform means a horizontal resolution of 512 steps which will give a good reproduction of the original waveform when the memory section is displayed in full. The reason why most digital oscilloscopes allow much more memory than this to be used for a single stored waveform is that they invariably have a zoom facility which allows one to look at a part of the waveform in detail.

Flexibility

Memory output can easily be converted for viewing on the c.r.t., but it can just as easily be fed to a digital plotter or a computer or a disc drive for permanent storage, provided that the instrument has the right interface circuits and outputs. Digital circuits used for the storage process, triggering and time base also lend themselves to computer control, and hence many digital oscilloscopes have at least an optional GPIB (IEEE488) interface for this purpose.

Resolution and accuracy

Resolution is not synonymous with accuracy. Imagine a 10V ramp signal driving a 100% accurate eight-bit a-to-d converter and driving the converter binary output word from zero to full scale (255). For each 0.039% increase in the ramp, the binary output signal increments by one. If the ramp now represented as a series of binary numbers is converted back to analogue form by a digital-to-analogue converter, d-to-a, it becomes a staircase waveform with 256 steps; lower amplitude input signals give a decreasing number of steps but resolution remains within 0.39% of full scale. Resolution therefore defines the degree of change in the converter input value that can be represented in the binary output signal.

As far as accuracy is concerned no converter is absolutely linear, even under static conditions. As the rate of change in the input signal increases, linearity worsens and a point is reached where output codes that should appear are skipped. In a digital-storage oscilloscope, the dynamic transfer function of a converter is important in determining the fidelity of reproduction of waveforms which have fast components. Non-linearities and missing codes at various frequencies are parameters well worth looking at. If accuracy was determined by resolution alone, a 10-bit converter would offer an accuracy in the region of 0.1% but in practice, digital storage oscilloscope accuracies are usually in line with similar quality conventional analogue oscilloscopes as far as amplitude measurement is concerned. Cursors used on many digital oscilloscopes though reduce human and parallax errors when making comparisons.

Kikusui's DSS6522 with roll mode for looking at slow waveforms (top) and the Nicolet 4094 with 4562 plug-in and disc drive (bottom).
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www.americanradiohistory.com
Double Forth

One particularly useful feature of the Microkey 4500 computer is that it can accept input from two independent keyboards and display the results on two monitors. This means that for program development or for text manipulation it acts as two computer. The ability to drive two monitors can have many uses. For example it is possible to have one screen displaying a control program while the other shows the results. The computer is based around the 6502 processor but may be alternatively fitted with a 6809 with no hardware modifications. In this configuration it can run the Flex operating systems. An add-on 68000 second processor extension is planned.

The 'native' language for the computer is an extended combination of Forth-79 and FIG-Forth with an assembler and a screen editor. Being developed is a Logo-type extension to Forth, a graphics facility and a power systems engineering package. Through Flex a number of other languages may be used including Pascal and C.

Some clever techniques are employed to make maximum use of memory. Screen information may be written to the video display memory which occupies the same memory area as the ram which may be accessed during a read cycle; thus the video ram is 'invisible' to the user. All 12K ram and 32K rom may be accessed to allow maximum use of the memory, though the ram may also be divided into two distinct areas of 64K each for the two-user mode.

High-resolution graphics are possible with 640 by 200 elements in 16 colours. In monochrome, it is possible to produce 1200 by 200 dots. There are three bidirectional parallel ports and a full RS232 communications port as well as an expansion bus using a similar pin-out to Apple computers. One or two Sony 3.5in disc drives may be fitted into the computer and up to two more may be added. A Winchester drive will be available.

The designers see their computer being of most use in educational, industrial, scientific and medical fields and are willing to offer a wide variety of hardware and software configurations to suit specific applications. The basic system without a monitor or disc drive (but including a disc interface and a high-quality professional keyboard) costs £650. Microkey Ltd, 98a St James Street, Brighton, Sussex, BN2 1TP.

WW301

More than a multimeter

Claiming to offer more measuring facilities than any multimeter, the Philips PM2519 is called a 'digital measurement centre'. Apart from all the volt, ohm and amp measurements with an accuracy of 0.1%, it includes a counter to measure frequency up to 1MHz, dB may be measured on both a.c. and d.c. voltage ranges, and there are 16 reference values built in to provide relative measurements. Included in the display is logarithmically scaled bar graph which indicates some digitally displayed values, providing a virtual analogue display for the easy setting of null values. The bar graph may also be used in the relative reference mode, enabling rapid and simple adjustment to a specific value, held in the internal non-volatile memory.

The PM2519 has a self-test facility and in the event of a fault, the built-in signature analysis fault finding technique ensures fast detection and repair. The meter is available in two versions; with an IEEE488 interface bus to enable computer-controlled testing at £495, or without for £285. A battery back-up pack is available to make the instrument fully portable. Pye Unicam Ltd, York Street, Cambridge CB1 2PX.

WW302

Build your own computer

A high-resolution-display computer, based on the MC6809E, is a British design from Micro Concepts of Cheltenham. The Microbox offers a minimal cost approach so that functions may be added as required. But the designer stresses that this is a 'no compromise' approach which equals or even exceeds the capabilities of the best personal computers. These include 60K of main system ram, disc controller for two 5 1/4", 40 or 80-track drives, two RS232 ports, a Centronics printer port and a parallel keyboard input port. An additional 128K ram is reserved for display and for 'silicon disc'. The ram-based silicon disc looks to the system like a conventional floppy disc with a capacity equal to a 40-track single-sided, single density disc; however the access time is a lot faster. The same principle is applied to the rom area; eprom cartridges, called 'discs' in this context, will accept up to four 8, 16, 32 or 64K eproms each, up to a maximum of 256K.

These slot into a port that is fully buffered and isolated so that the rom discs may be changed while the system is powered. A built-in eprom programmer is included in the design.

The display offers several alphabetic, numeric and character formats including 106 columns by 24 lines and 128 columns by 72 lines. Use of the NEC 7220 graphics controller chip gives a 768 by 576 element display with high-speed drawing through the inbuilt vector generation. Such facilities as pointers, lines, rectangles, circles, arcs and the ability to fill an area are provided.

For disc operation, the Flex system was selected because it is hardware independent and a considerable range of software is already available. Implementation is taken care of by the auto-configuring boot program which is included in the supplied system support monitor so there is no need for any knowledge of hardware or software to get the system going. This 8K rom contains all disc, console and graphics drivers plus 27 diagnostic and utility commands.

The start-up kit consists of a bare, 12-hole-plate p.c.b. measuring 305 by 241mm, a 76 by 100mm eprom carrier board, the system support eprom, system utilities on a 5.25in disc, computer - controlled testing facilities, the organization of a variety of hardware and software, and a list of components and suppliers. All for £95 from Micro Concepts, 8 Skillcornere Mews, Queens Road, Cheltenham, Glos GL50 2N1.

WW303

Commodore enhancement

A plug-in rom for the Commodore 64 home computer adds nearly 100 Basic commands to its operation. Particular areas of improvement are in the high resolution display facilities, the organization of sprite, colch text displays, sound commands have been improved to give synthesizer capabilities. There are many new commands to improve the ability to program in machine code and to give the Basic more of a structured approach.

Input and output control has several new commands and there are many others. One of the criticisms of the Commodore 64 has been its inadequate Basic and this toolbox addition seems to be very useful in correcting this. Known as RG Basic, the rom comes with an 82-page manual for £57.50 (inclusive) from Kuma Computers Ltd, Unit 12, Horseshoe Park, Pangbourne, Berks RG8 7JW.

WW304
Massive Eprom
By combining a number of eprom chips onto a ceramic substrate, it is possible to get eproms with up to 256Kbits of storage into a standard d.i.l. package. Included on the substrate is decoupling capacitors and decoding to provide the configuration so that externally it behaves as a single unit with pin functions conforming to JEDEC standards. 32Kbyte versions are available in n.mos and c.mos, with a 16Kbyte version in c.mos only. A 16K by 16 version will become available soon. Electronic Design Europe Ltd, Shelley House, The Avenue, Lightwater, Surrey GU18 5RF.

WW309

Single-chip modem
A single-chip c.mos f.s.k. modem has been produced by TI. It incorporates filters which conform to the CCITT V23 standard, having a transmit modulation at 75, 150, 600 or 1200baud and receive demodulation at 600 or 1200baud. It offers full duplex operation up to 1200baud receive and 150baud transmit or half duplex at 1200baud both ways. It operates from a single 4 to 6V supply with a consumption of only 35mA and is ideal, according to Texas, for communications by telephone between home/personal computers, intelligent terminals, credit card readers, viewdata terminals etc. Texas Instruments Ltd, Manton Lane, Bedford MK41 7PA.

WW310

Video filters
A range of 22 filters from Barr & Stroud has been designed to cover all known current requirements for both analogue and digital video processing applications. The range consists of nine luminance low pass filters, four chrominance low pass, three luminance/chrominance YUV filter combinations, four sub-carrier band pass and two sub-carrier band stop filters. The sub-carrier filters, used to isolate the chrominance and luminance information in colour tv systems, are available in NTSC and PAL versions. In addition to the standard range, the manufacturers are willing to provide a made-to-measure service. Barr & Stroud Ltd, Melrose House, 4 Savile Row, London W1X 1AF.

WW306

A and D i/o board for IBM PC
A single board containing both analogue and digital inputs and outputs is available for the IBM personal computer. Costing £495 (less in o.e.m. quantities), the DT2808 includes an on-board programmable clock and its own processor. It provides 16 channels of a-to-d with 10-bit resolution and two channels of d-to-a with 8-bit resolution, there are also 16 lines of digital i/o. The board is intended for use in industrial control, data logging, product testing, and quality assurance. Energy management and security systems are also among the applications. The on-board processor acts as interface between the board and the host computer. It controls all the i/o functions on the board and includes self-test functions it may be programmed through its internal microcode, or through a special software package available from the manufacturers. Data Translation Ltd, 430 Bath Road, Slough, Berks SL1 6BB.

WW312

Conect 36
Strips of 0.025in square pins and receptacles, made in straight and right-angular form have beryllium copper contacts. With a standard 0.1in pitch, the makers say that they are ideal for mother/daughter module connectors. They come in standard lengths of 36 connectors and are notched to break off a desired length. Robinson Nugent Ltd, 74 London Road, Riverhead, Sevenoaks, Kent.

WW313

Polyester decoupling
A new range of metallized polyester 5mm-lead pitch capacitors has been designed to replace the more expensive multi-layer ceramic types used in decoupling. The small size allows high density packing on a p.c.b. and with this in mind the makers have printed the value, from 100pF to 1µF, on the top for easy identification. Leads are ready-cropped and are provided with mounting 'feet'. Sufflex Ltd, Risca, Newport, Gwent NP1 6YD.

WW314

Reference diode
A 2.5V reference diode offers a tolerance of 5mV or 0.2%. The LT1009 is a precision trimmed shunt regulator diode, with a temperature drift of less than 25ppm/°C. It operates over a wide current range, from 400µA to 10A, with a dynamic resistance of 0.6Ω. A third terminal is supplied to allow the reference voltage to be altered by 2% to calibrate out any system errors. Dialogue Distribution Ltd, Watchmoor Road, Camberley, Surrey GU15 3AQ.

WW315

Spectrum interface
A printer interface for the Sinclair ZX Spectrum includes both RS232 and Centronic interfaces. It is able to implement the Copy command which allows the printing of a high resolution screen image. This is available for a number of popular printers including Epson, Star and Seikosha and will give a full colour image with the Seikosha GP700 printer. The ZX Lprint III costs £34.95 inclusive from Euroelectronics, 26 Clarence Square, Cheltenham, Glos GL50 2UJ.

WW316

Ribbon-cable cutter
The KT80 ribbon-cable cutter is made from steel with plastics-covered handles. It has a hollow ground hardened steel blade which is provided with a toggle-lever action so that all conductors are cleanly cut at the same time. The g.r.p. anvil has a built-in guide to ensure that a cut is made at right angles. The blade and angle are replaceable and spares are included. Klippon Electricals Ltd, Terminal Works, Power Station Road, Sheerness, Kent ME12 3AB.
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The OM358 is ideal for digital equipment (it can often solve problems that would otherwise need a fast logic analyser) but, unlike dedicated logic test instruments, it is equally suited to analogue waveforms.

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Thurlby Electronics Ltd
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HC
SPECIFICATION

5 channel stereo, 12
AC DC
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O/load Protection: All
AC -DC, 20 MEG
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**CDD DISKETTES AT CRAZY PRICES!**

<table>
<thead>
<tr>
<th>Code</th>
<th>Type</th>
<th>Price</th>
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<tbody>
<tr>
<td>TD1</td>
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<td>5½ 80 TRK single sided</td>
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<td>5½ 80 TRK double sided</td>
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</tr>
<tr>
<td>TD7</td>
<td>8 100 TRK double sided</td>
<td>£3.99</td>
</tr>
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</table>

10 per box. Prices per diskette quoted. Discounts for quantity.

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<tr>
<th>Code</th>
<th>Type</th>
<th>Price</th>
</tr>
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<tr>
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<td>40 60 OSM Print per 1000</td>
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<tr>
<td>T60.14</td>
<td>288 80 OSM Print per 1000</td>
<td>£4.95</td>
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<th>IBM PC 8088+</th>
<th>T138 8088/8087 Dual CPU, Internal Disk, 1 MB RAM, System Disk, Software, User and Reference Manuals, £1595</th>
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<td>IBM PC 8088+</td>
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<tr>
<td>IBM PC 8088+</td>
<td>T142 8088/8087 Dual CPU, Internal Disk, 16 MB RAM, System Disk, Software, User and Reference Manuals, £5495</td>
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</tbody>
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<thead>
<tr>
<th>Model</th>
<th>Type</th>
<th>Price</th>
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<tr>
<td>TD3</td>
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<td>£248</td>
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**BBC COMPATIBLE DUAL DISK DRIVES**

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<td>TD3</td>
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**BBC COMPATIBLE DUAL SWITCHABLE DISK DRIVES**

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<tr>
<td>TD1</td>
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<td>TD2</td>
<td>400K</td>
<td>£510</td>
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</table>

The drives include connecting cables, user manual, disk formatter ex of VAT & CARR.

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X-Y
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Component Tester

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Component Tester

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Wireless World April 1984
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<tr>
<td>2SC2517</td>
<td>0.50</td>
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APPLICATIONS

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