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- **Accuracy**: ± 3%.
- **AC or DC coupling**: Also available from Electrolog.
- **Price subject to change without notice.**

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**Tektronix UK Limited**

PO Box 89, Harpenden, Herts. AL5 4LP
Tel: Harpenden 601141 Telex: 20009

Regional Telephone Numbers: Maidenhead 8628 7321, Manchester 061 428 0799,
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**METERS**

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<td>HP</td>
<td>20mA, i/o print, cassette &amp; DMA</td>
<td>£2500</td>
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  - £300.00
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<td>716145s 5 volt</td>
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<td>282145s Texas type</td>
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**12-HOUR**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Price</th>
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<tr>
<td>100A</td>
<td>12-Hour Analog, Full Day, 12-Hour</td>
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<td>100B</td>
<td>12-Hour Analog, Full Day, 12-Hour</td>
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<td>100C</td>
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<td>100D</td>
<td>12-Hour Analog, Full Day, 12-Hour</td>
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<td>100E</td>
<td>12-Hour Analog, Full Day, 12-Hour</td>
<td>£375.00</td>
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**24-HOUR**

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<td>200A</td>
<td>24-Hour Analog, Full Day, 24-Hour</td>
<td>£220.00</td>
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<td>200B</td>
<td>24-Hour Analog, Full Day, 24-Hour</td>
<td>£265.00</td>
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<td>200C</td>
<td>24-Hour Analog, Full Day, 24-Hour</td>
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<tr>
<td>200E</td>
<td>24-Hour Analog, Full Day, 24-Hour</td>
<td>£400.00</td>
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</tbody>
</table>

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<table>
<thead>
<tr>
<th>Model</th>
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<td>136 R</td>
<td>137 R</td>
<td>138 R</td>
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</table>

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wireless world

Engineering — or dominoes?

During the 1940s, at a grammar school in the north of England, the most wonderful things on display in the glass case outside the science laboratories were a cloud of glass-fibre wool and some coal with a fossil leaf in it. The glass was impossible because everyone knew that glass was hard and brittle and yet here was this soft (though scratchy) stuff made from it, and the coal was just so unimaginably old — older, even, than the physics master who had, some said, discovered fire. Simple things, goodness knows, but worth a couple of lessons in the physics class.

In those days, there was little talk of wireless in the classroom, let alone 'electronics'; classes were taken up with interminable experiments on the latent heat of vaporization and the laborious plotting of magnetic fields. Then, one day, a visiting teacher told the class of his wartime work on radar, speaking of microwaves, metallic insulators and times measured in microseconds. This was a great deal more wonderful than the glass wool and bits of coal and led to rather a lot of daydreaming for some of the class.

Science teaching has advanced greatly in the ensuing 35 years. Microcomputers are becoming commonplace and labs are stocked with oscilloscopes, signal generators and all the other impediments of the electronic '80s. Pupils handle circuitry switching at 3ns or oscillators working at several gigahertz or truly compendious i.c.s with remarkable nonchalance, if the youngsters seen on television programmes or in the news as competition winners are anything to go by.

It is, in goes almost without saying, necessary for the modern pupil to have the use of advanced, modern equipment. It is right that programming microprocessors should have taken the place of connecting components, in school, as in the world of work. A micro, given the correct data and program, will do exactly what is expected of it very efficiently, as can be verified by a glance at the storage oscilloscope or logic display, but where is the striving? And, without the striving, where is the learning?

Is there a danger of producing a great number of people who call themselves electronic engineers but whose knowledge of electronics stops short at an ability to program and an awareness of the cheapest supplier of interfaces?

The only answer to all these weary, half-baked questions is that undoubtedly that is exactly what engineers will be like, and quite soon, too: there is no reason why they should be any different. It has been said for years that the microprocessor is a component, to be used as any other component. There can be little advantage to a user in knowing the precise details of the internal working of a micro — it can be regarded as a machine which will do its job when asked. It is not necessary to know the finer points of oscilloscope design to use one to its fullest extent: neither is it necessarily necessary to know more than the capabilities and characteristics of a micro, or any other i.c., to obtain the maximum performance from it. And when the remaining parts of circuits are also integrated, there will be no pressing need to understand the use of power transistors, or passive components, either, unless one has to design the i.c. 'Systems engineering' will be supreme.

This is not, of course, to say that all engineers will be satisfied without a detailed knowledge of exactly what happens inside the i.c. Perhaps these people will be the originators — the ones who, because they know more of the internal operation, will be able to apply it with a greater imagination. But do not decry the simple user of modules: he will know all he needs to know.
MICROPROCESSOR-CONTROLLED LIGHTING SYSTEM

Stage and theatre lighting control is a complex task — yet a task easily handled by a microprocessor. As even the simplest of microprocessors can be programmed to provide control data for controlling a lighting system, these articles concentrate on using an existing microprocessor board to process and store complex lighting patterns set by conventional faders, and cover interfacing from digital data, to human input, to light dimmers. Software for the 8085A processor used in the prototype will be discussed in the third and final article.

by John D. H. White and Nigel M. Allison

This system is designed to simplify the control of complex lighting patterns as used in theatres and studios or at pop concerts. The prototype described in these articles made use of a commercially available 8085A processor board to control up to 256 lighting channels with 8-bit accuracy phase control. Here, we discuss the system's hardware and its ability to linearize the relationship between lamp brightness and fader position.

Background

Before the introduction of high-power semiconductors the brightness of lamps in lighting systems was controlled by variable resistors or inductors. The cost and size of such inefficient power-control methods meant that systems were kept small and were usually difficult to operate. With high-power thyristors, it was possible to construct very compact dimmers which could be controlled remotely. Initially, this improved power control was used to copy the previous systems; however, the compact nature of the dimmers meant that much larger lighting systems could now be built and controlled. At present, "portable" lighting systems with 80 separate output channels are in common use for pop-group concerts and even larger systems are employed in TV studios and theatres.

All-lighting-control systems may be split into two separate sections — the power-control section (the dimmers) and the control desk, which is used to control the dimmers. These are usually remote from each other, being connected by multi-core cable. Although the size of lighting systems has increased over the years, the control facilities have remained rudimentary. A small number of digitally controlled desks are commercially available, though these are expensive and tend to be used in large, fixed installations.

The most common type of circuit used in an analogue control desk is outlined in Fig 1. Each row of channel faders (presets) is voltage driven by a master fader (master preset). Outputs from each preset for a given channel are then gated together through diodes; thus the final output from the control desk is the largest preset voltage for each channel. In this way, each master preset can be used to recall a stored lighting pattern (i.e. stored in a row of presets). Because of the cost of faders, the number of master presets is usually fairly small. For pop-group concerts and certain stage applications, the ability to control continuously the brightness of each light is forfeited to allow the storage of a greater number of lighting patterns. The patterns are created and stored by positioning pins, containing diodes, in interchangeable matrix boards, as indicated in Fig 2.

As the dimmers will use different mains phases (total power requirements may exceed 5000W for a large system), a standard interface format between the control desk and dimmers is necessary. A direct voltage of 0-10V has become the convention in most lighting systems, 0V corresponding to the lamp being off, and 10V to full brightness. Figure 3 shows the schematic lay-out of a typical dimmer module. The d.c. control voltage is compared with a ramp synchronized with the line frequency, hence phase-control of the load is possible.

Before considering the output hardware, one other question that needs answering: how many control bits are required to give apparently stepless light output variations? For a very wide range of lighting conditions, it was found that seven bits were sufficient for "stepless" light control. Since the microprocessor is an 8-bit device and most of the integrated circuits used to construct the system are 4-bit devices, it was decided to use 8-bit codes throughout. This also provides some immunity to the effects of truncation errors in the output code from software calculations.

Circuit description

Because of the large number of output channels each dimmer unit must be kept simple and economical. Also, since one may wish to increase the number of output channels in the future, a modular design is advantageous. The overall output-control layout is shown in Fig 5. Each dimmer module is enabled so as to accept data from the microprocessor data bus by a 2-bit code derived from the 8 low-order bits of the address bus. Hence up to 256 dimmer modules can be given a unique address. Conventional output ports could have been used to enable data transfer to each dimmer module. However, the 8085A processor instruction set contains only one output-port instruction (OUT port) and this can only be used in a direct-addressing mode, i.e., the second byte of the instruction must contain the port address. The restriction of direct addressing makes this method unsuitable for use in a lighting-control desk because of the large number of outputs required. The solution is to employ mapped-memory output, which uses a section of "memory locations" for
Subjective brightness control

For full-wave control using a triode, or inter-parallel connection of two thyristors, the m.s. output voltage, \( V_{\text{out}} \), is

\[
V_{\text{out}} = \frac{V_{\text{in}}}{\sqrt{2}} = \frac{27}{\sqrt{2}} = 24.2 \text{ V}
\]

where \( V_{\text{in}} \) is the r.m.s. supply voltage and \( V_{\text{out}} \) is the d.c. output voltage. Thyristors and their associated parts are shown in the circuit diagram.

- The effectiveness of the lamp filament is determined by the size of the filament and its temperature. The filament is found to be a normal filament, with its temperature determined by the filament temperature.
- The filament temperature, \( T \), is given by

\[
T = \frac{V_{\text{in}}}{R}
\]

where \( R \) is the resistance of the filament and \( E \) is the voltage drop across the filament.

- The filament temperature, \( T \), is found to be a normal filament, with its temperature determined by the filament temperature.

Output. This arrangement allows any instructions which write to memory to be used as output instructions, giving considerable advantages in the software as indirect addressing is permitted. A small amount of extra hardware is required to determine the address lines to enable the outputs.

The digital equivalent to the linear-voltage ramp in an analogue dimmer is an 8-bit binary code counting from 0 to 255 in each half-cycle. The 8-bit synchronous clock is derived by multiplying the line frequency. The counter is reset every line half-cycle by a zero-crossing detector.

Each dimmer module compares the latched 8-bit code from the control desk to the 8-bit code from the counter. When the counter output is greater than the control desk code, a 12-bit code is latched to gate the thyristors, hence accurate phase control of the lamps is possible.

The complete lighting system will contain one address-decoding and dimmer-enable module, one frequency-multiplexer module, three counter and reset modules (one for each phase used), and one dimmer module per output channel.

Address decoding and dimmer enable module

The eight high-order bits of the address bus are compared with a bit pattern set by wire links to determine the location of the 356 output addresses in the memory map. Two cascaded 7445 4-bit magnitude comparators, see Fig. 6, generate a high-level signal when all input bits are equal. This signal, the M/D and WR control signals and the system enable signal, \( E \), enter a NAND gate to provide a signal which is high when valid output

Frequency multiplier module

A 51.2kHz clock signal for the 8-bit counters, shown in Fig. 7, is obtained by multiplying the line frequency by 1024. The phase-locked loop (NE565) has a feedback divider chain consisting of five 7447 dual D-type flip-flops. The capture range is set at ±2Hz. The i.f. output signal to the phase comparator is at half-wave rectified main frequency. Although t.r.l. compatible, the square-wave output of the v.c.o. will only provide a current of about 1mA, so the output is buffered to drive the counter and divider chain.

Synchronous counter and reset module

This circuit, shown in Fig. 8, generates an 8-bit binary code which counts from 0 to 255 in half a line period. The 51.2kHz signal from the frequency multiplier is used to clock two cascaded 74161A 4-bit counters. The CLEAR inputs of these counters are used to reset the counter at the zero-crossing points of the mains. The full-wave rectified a.c. is applied to the voltage comparator (741). The output of the op-amp is inverted and converted to t.r.l. levels by the following common-emitter stage.

Dimmer module

The 8-bit code from the control desk, through the data bus, is stored in two 7475, 4-bit bistable latches, Fig. 9. These latches are enabled, i.e., do not pass the data bus is transferred to their Q outputs, when the data module is addressed by its own 2-bit dimmer enable signal, E1 and E2. Data stored in the latches is compared to the output of the counter by the two cascaded 7455s. When the count from the counter is greater than the latch data, the 51.2kHz signal is gated to the thyristors through some buffer stage and pulse transformer. Some interference of transient protection is provided by the inductor and capacitor.

System performance

Some advantages of feeding data to a large number of channels have already been mentioned. Also, since the access time for each dimmer is less than the 40ns (the maximum data-access time being permitted by the processor), no processor WAIT states are involved in transferring data. Thus, of course, maximizes the data transfer speed for updating the dimmers and
Fibre optics at ITT

Joining optical fibers, especially in the field, is very difficult. ITT have developed a fibre optic splicing kit, the OFSK-10. Primarily intended for the joining of 50/125 micron single-mode grade fibres and other fibres of an all-silica construction, the kit uses an electric arc to fuse together the two ends. A V-groove jig has been developed to locate the ends accurately so that very high quality splices can be achieved. Testing fibres in the field can also be a problem; it is very unlikely that the engineer has access to both ends of a cable and needs some method of locating a fault in a cable which can be up to 15km long, between repeaters. An answer has been provided by ITT in the OFRP-5, an optical fibre reflectometer. If a short pulse of high intensity light is launched into an optical fibre, a small proportion of the light is reflected back towards the source from every point in the fibre. The reflections are "backscatter" caused by imperfections in the molecular structure of the silica. The power of the reflected light, measured at the source end, decreases exponentially with time, and by inference, by distance with the distance of the fibre into the input. The OFRP-3 uses a laser to launch a laser into the fibre and can measure and record the response from the reflections. Joints along the cable can cause extra reflections causing a peak in the response. Faults in the cable will cause drops in the responses. The OFRP-4 performs the same function as the reflectometer which includes an alpha-scanstic display of all the relevant parameters. With the use of a crrier or any part of the response can be looked at in more detail and the oscilloscope with all the data display can be printed out for permanent record. The "scope and printer are incorporated into the equipment which fits into a portable case. All the controls and the printer are incorporated in the lid. The laser fires behind a locked hatch and cannot be switched on until connected to a cable. Any fault can be traced within the first six metres by using a broad-spectrumisc display over a length of 15000m.

The OFRP-3 can trace faults in an optical fibre to within six metres over a length of 15000m.

helps to produce a highly interactive lighting system.

The effect of linearizing the luminous output of the lamp with the position of the fader is indicated in Fig. 10. The output code FF corresponds to the lamp being off, and the code 00 corresponds to full brightness. The slight delay at the start is due both to transparency errors in forming the inverse function mentioned earlier and to slight measurement difficulties. It could be removed by incorporating a suitable offset in the output coding, but from an operating point of view there are quite distinct advantages in having a definite "lamps off" position on the faders. In the system, the 256 values of this inverse function are held in a "hook-up table" in the operating software. For a non-microprocessor system, there is no reason why these values could not be contained in a p.r.o.m.

The complete operating system not only provides routines for inputting and outputting data, but also various methods for processing the stored lighting patterns. In the next article, the control desk will be discussed.

The OFRP-4, an optical fibre reflectometer, which is used to measure the reflectance of a fibre optic cable. A special cable has been developed to withstand voltage potentials of up to 55kV. In parallel with the development of the cable, the built-in features of a design of an i.e.d. edge connector array for providing the integral pulse firing signals for each element. The link is to be commissioned in 1985/86.

Another new application is a cable television link which is to be given a trial by British Telecom to 18 houses in Milton Keynes. The trial will use optical transmission based on p.f.m. (pulsed frequency modulation) in which the signal frequency modulates a square wave carrier which then drives an i.e.d. source. All the transmitter and receiver modules include the modulators and demodulators and have been supplied by ITT Leeds.

It is already running a cable service in Milton Keynes. For the trial the programmes are down-converted into baseband and separated into individual channels (at 6 MHz P.A.L. video with sound). In addition a channel is formed consisting of the f.m. program feeds on carriers in the range 6 to 7MHz. Each channel is fed to its own transmitter and a cable is connected to the transmitter and a distribution point. The cable used for the 3.5km primary link contains fibre of better than 35dBKm and 400MHz-km bandwidth-distance product. From the distribution point the secondary link of between 50 and 200m goes to each customer. Signal information and channel selection is made at the customer's end and fed back from the customer's end to a microprocessor control which provides the channels and can store any information about transmission on both primary and secondary links. In the house the signal is re-amplified, demodulated to baseband and then up-converted to uhf so that it can be fed into the aerial socket of an ordinary tv.

The effect of linearizing the luminous output of the lamps in relation to the fader position.

If the 1950s were the decade in which linear electronic circuits, previously implemented using thermal valves as their active components, were progressively taken over by transistors, then the 1960s were the decade in which such circuits, built up from an assembly of discrete components and transistors, were increasingly constructed using integrated circuits. As simple packages of purpose-built circuits, containing all the necessary active and passive components in a single lump, the term "integrated circuit" was coined at this time to describe this packaged assembly of components.

While it was the enormous assembly in the field of digital computers, which convinced the i.c. manufacturers of the enormous benefits of scale, it was the consumer market which provided the chance of profitable manufacture away from the large integrated circuits.

The realization that there was a large potential market set the design departments of many of the larger semiconductor manufacturers exploring the possibilities for useful functional packages. Clearly, an i.e.d. functional block which could be used with a relay and a timing capacitor to provide switching or timing functions, as, for example, in a washing machine or a darkroom enlarger timer, would be an i.e.d. circuit. An early such i.c.s were evolved at the end of the 1960s. Of these, by far the most successful was the Signetics 555. An i.e.d. number of manufacturers have copied it in identical form — in the process of what is known as "second sourcing" and produced in dual (556), quadraple (558) and c.m.o.s. (559) forms, along with some improved devices having the same pin configurations, such as the LM555.

With the possible exception of the ubiquitous i.e.d. operational amplifier, few integrated circuits have had such an appeal to the hobby electronics constructor, with several complete books of circuits having been published showing possible applications for this device. Yet, in spite of this, to most of its users, its method of operation remains needlessly obscure, and many are put off by the apparent side-effect of the internal and external circuitry.

The 555 group of i.c.s is one of the most popular ever made, with an enormous variety of applications in oscillators and timers. John Linsley Hood explains its internal design and method of operation.

Circuit description

The 555 is fundamentally intended to give an output voltage waveform, as a 'one-shot' or in a repetitive manner, at a low enough output impedance to operate a simple switch or a sensitive relay. To simplify the calculations for the timing RC chain — in which these constant RC's are in seconds, it is convenient to use volts as a unit of time. For the time taken for a capacitor C to charge through resistor R to 63.2% of the applied voltage after the internal voltage switching levels are chosen so that the external timing capacitor charges through about the same time difference. A simple block diagram showing the internal arrangement is given in Fig. 1.

In this, the heart of the circuit is a bistable 'flip-flop' with an external overriding reset input R. The two normal inputs are the threshold and the trigger, connections, both of which are fed in through relatively high-impedance buffer amplifiers, connected, respectively, to reference voltages of VR and VCC, derived from the 15k resistor chain. Two buffered outputs from the flip-flop are provided through amplifiers A1 and A2, which is the first of which is a normal 'system' output, layout, as typically used in t.i.c. logic, to give a fairly low output impedance, and good current-sourcing characteristics. The second output, from A3, is derived simply from a single transistor 'open collector' stage.

The way in which the 555 would normally be connected to operate as a 'one-shot' timer driving a relay, is shown in Fig. 2(a). The input to the trigger is the discharge (open-collector amplifier) output are joined together, and taken to the junction of the relay R and the timing capacitor C. The timing cycle is initiated by a momentary operation of a push-switch connected to the trigger input. This sets the Q output of the 555 and the relay is closed, providing a connection of the non-inverted outputs from A1 and A2 to a high state. In the case of A1, this would have a low output impedance, so the output becomes an open circuit, so that the capacitance C is free to charge up towards the Vcc - Vr.
Fig. 2. Connection for a free-running oscillator, with a frequency determined by the constant-current source and the value of \( C \).

Timing capacitor discharged and at a potential close to the 0 volt line level, ready for a further timing cycle to be initiated, by an input at a level less than \( V_{TH} \) being applied to the Trigger. The output waveforms are shown in Fig. 2(b).

Since the Trigger input is also taken to the bistable through a impedance buffer amplifier, it is practicable to connect this to the timing circuit as well, without imposing too much of a static load. This will convert the circuit into a 'free-running' sawtooth generator, with an output of \( V_{TH} \) as shown in Figs 3(a) and 3(b). Moreover, if the timing resistor \( R \) is replaced by an appropriate constant-current source, the output at point A will be a highly linear waveform, suitable for use in a time-base generator, and with a source input available at the override reset of the bistable.

The bistable flip-flop is itself a very simple arrangement, shown schematically in Fig. 4(a) and in its practical form in Fig. 4(b). In this circuit, if the input (1) is taken high, even momentarily, the output will also go high and remain at that state. Similarly, if the input is taken low, the output will also follow, and remain. The fact that the transistor circuit of \( T_2 \) and \( T_3 \) can be made to behave like this depends on the characteristic that a transistor turned hard on will have a collector-emitter voltage drop of only some 0.1 to 0.4 volts, depending on construction and \( I_C \) and \( I_B \), whereas the minimum voltage necessary at the base, for conduction, will be at least 0.5 volts in a silicon device.

The way in which this circuit is organized, with respect to its output circuitry, is threshold, trigger, and reset inputs, is shown in Fig. 5. Because the transistor \( T_R \) in the reset circuit, acts as a switch directly connected between the positive end of \( D \) and the discharge circuit open-collector amplifier, this will cause \( T_R \) to be turned off, with \( T_3 \) and \( T_4 \) turned on. This will reset both \( A_1 \) and \( A_2 \) outputs to the low level.

While this input, being connected later in the circuit than the trigger input, will over-ride the trigger signal, if the trigger input is held low, the circuit will revert to the operating condition, with \( A_1 \) high and \( A_2 \) open circuit, as soon as the reset signal is removed.

The two input amplifiers used in the threshold and trigger circuits, are of similar form, as shown in Figs 6 and 7, using Darlington connected, four-transistor, long-tailed pairs. However, it should be borne in mind, as explained in the first article of this series on the 741, that the integrated circuit manufacturing process does not normally allow the construction of \( p-n-p \) transistors, within the i.e., which have a very high current gain, except in the circumstance that their collectors are directly connected to the substrate, (which is normally the 0V line).

Since the input \( p-n-p \) transistors of the trigger circuit do not meet this condition, they must be of the 'lateral' type, which gives an inferior input impedance to this amplifier to that of the \( n-p-n \) input devices.
DIGITAL, MULTI-TRACK TAPE RECORDER

The final article in this series describes the motor speed control circuitry and the power supplies. The few modifications to the original tape recorder, used as the basis for this design, are also presented, with advice on adjustment of bias, equalization and signal level.

by A. J. Ewins, B.Tech.

The VLF910 cassette deck used in the Hart version of the Lindsey Hood cassette recorder uses only one motor for the capstan drive, take-up spool and rewind spool. In spite of this, and though relatively cheap, its specifications are excellent and the success of the digital recorder design is due in no small part to this excellent deck. The motor used is called a frequency-servo type and consists of a motor unit and tachogenerator. Earlier versions of the VLF910 deck used a motor, type R14-7430, 6VYD, with a built-in tacho generator which produced an a.c. output with amplitude and frequency proportionality to its speed. When running at the normal tape speed of 1.78 in/s, the frequency output was approximately 4560Hz. Later versions of the VLF910 deck use a different motor, type MMX-6H2L5R, which, instead of a tachogenerator, has a rotating magnetic disc attached to the motor shaft and an associated Hall-effect i.e. When running at a tape speed of 1.78 in/s, the output on one of the pins of the Hall-effect i.e. is a pulse train of frequency about 912Hz. (Although the figure of 912Hz is claimed as approximate with research Department, London Transport.

Fig. 47. Motor speed control circuitry and 'in-lock' indicator.

The block diagram of the tape-recorder speed control circuit was shown in Fig. 11 in part 2 of the series: Fig. 47 shows the circuit of the reference frequency selector, v.c.o. and phase sensitive detector. The v.c.o. and p.s.d. are contained within the c.o.m.s. phase-locked loop i.e., type 4046. So that the tape-recorder speed control can be self-contained, the v.c.o. is used as the frequency reference source in the absence of any external reference. Using the values for the timing capacitor and resistor as shown, the 541 variable resistor is adjusted to give an output frequency of 4551Hz. (This is the same as the tape-clock frequency of 22.755Hz divided by 50.) In the absence of an external frequency input, the reset input to the 4017 counter will be at the logic 0 level. The output from the v.c.o. clocks the counter so that eventually the 5 output becomes logic 1, disabling the counter. In this condition, the carry-out, CO, is at logic 0. The output from Nand 2 is thus at logic 1 and the output from Nand 3 is the inverted v.c.o. signal. Nand 4 inverts this signal yet again, presenting a non-inverted v.c.o. signal to the input of the Ex-Or p.s.d., whose other input is that from the tachogenerator pulse shaper. When the phase-locked loop of the speed-control system is in lock, the frequency from the tachogenerator pulse shaper is exactly that of the v.c.o., but it lags a phase by about 90°. Consequently, the D input to the D-type flip-flop is at the logic 1 level when the Ck input goes positive, putting a logic 1 on the Q output of the flip-flop, lighting the i.e.d. and giving a visual 'in-lock' indication. With logic 0 on the Q output, the audible indicator is silent. In the event of a loss of lock the i.e.d. will flash and the audible indicator will wrablate at a frequency dependent upon the rate of slipage between the two frequencies.

The output from the p.s.d. is passed to the motor drive circuit of Fig. 48(a) or (b). It is filtered by a lead-lag low-pass filter, consisting of the 100k input resistor to the 351 op-amp and the 39k plus 50pF capacitor (11µF in Fig. 48(b)) feedback loop. The low-frequency gain of the inverting op-amp is limited to unity by the 100k feedback resistor. The resulting output from the op-amp drives the motor via the emitter-follower circuit using a Darlington power transistor, TIP122. The 10k resistor and base-collector feedback capacitor of 1nF provide some necessary high-frequency cut-off to the emitter-follower stage. The values of the filter components were found by trial and error to produce a stable and trouble-free p.i.l. servo system under all conditions of Play, Rewind and Fast Forward operation of the deck.

The direct offset voltage produced at the output of the op-amp by the potential divider circuit on the non-inverting input is essential to the self-starting action of the servo system. The 20k resistor should be adjusted such that the p.i.l. finds lock in one or two seconds after pressing the Play, Rewind or Fast Forward keys. If the voltage on the non-inverting input is too low, the p.i.l. will not find 'a lock', the motor speed remaining too low; if it is too high, the loop will find and lose its 'lock', the motor speed ending up too high. When a satisfactory setting for the 20k resistor has been found it will be observed that the tachogenerator waveform leads the v.c.o. output by a little more than the ideal 90°. This phase difference will change with varying load conditions but should not vary so much as to lose lock.

The tachogenerator pulse shaper circuit shown in Fig. 48(a) is that for the motor with the built-in tachogenerator, while that in Fig. 48(b) is for the motor with the mechanically coupled magnetic disc and Hall-effect sensor. Because the output from the speed sensing circuit of Fig. 48(b) is exactly double that of Fig. 48(a), the output from the pulse shaper is divided by 2. C.m.o.s. circuits of Fig. 47 and the pulse shapers of Figs. 48(a) and (b) are powered from a 15V supply, which is provided by a 15V, 100mA regulator powered by the cassette recorder's 20V stabilised supply line. The 20V supply powering the

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Fig. 48. Motor drive circuit and tacho pulse shaper. Version for motor Type R14-7420, 6TYHD is at (a), while that used for motor Type MMX-6H2L5R is shown at (b).

20V supply from tape recorder

20V supply from tape recorder

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motor drive circuit is that normally supplied to the positive lead of the motor, switched by the various keys of the cassette deck.

Motor modifications
Both types of motor may be removed from their outer casings by careful removal of the back-plate. For motor type R14-7430, 03YRD, the built-in electronics should be completely removed. The tachogenerator output is identified by two yellow leads, whilst the motor contacts are two terminal posts to which the internal p.c.b. is soldered. The two yellow leads should be extended, and two wires, red and black, should be soldered to the two terminal posts of the motor, making certain which is the positive and negative terminal. Rearrangement of these two motor connections will result in the motor running backwards, but no damage will be done.

With the back off the motor type MMX-6HLSB, the frequency output of the Hall-effect sensor should be identified before any modifications are carried out. This is done by rotating the motor from a nominal 12V source and using an oscilloscope to identify the frequency output pin of the i.c. Having adjusted the power of the built-electronics, this automatically breaks the internal servo loop. A check is made between the positive pin of the motor drive to the negative supply line. Connections then need to be made to the positive pin of the built-in electronics, the positive pin of the motor drive, the negative supply line of the built-in electronics and the frequency output pin of the Hall-effect i.e.

Use of the reference frequency circuit
When operated with the rest of the digital electronics of the recorder, the reference frequency for the speed control circuit is supplied to the reference frequency input of the recorder, for that of the motor speed control circuit, the instability produced by the belt drive mechanism is removed by 470 nF. This is shown in block form in Fig. 11 of part 2. During the recording process, the

The reference frequency is the TC frequency of 22,755.516Hz as obtained by a 455 Hz oscillator. When this source is connected to the external frequency input of the motor speed control circuit, the digital v.c.o. source is automatically "knocked-out". The 4017 counter of Fig. 47 is continuously reset by the presence of the external frequency source, the result that CO remains in the logic 1 level and the output at logic 0. The external frequency source thus passes through Nands 2 and 4 and the input of the p.a.d., the output of Nand 3 being permanently maintained at logic 1. In playback, the reference frequency presented to the speed control circuit is that from a v.c.o. whose output frequency is dependent upon the average voltage at its input, which is the filtered output of a p.a.d. Comparing the crystal-controlled TC with the recovered TC from the recorded data of one track of the tape-recorder. Thus, on playback, the speed control of the tape is maintained by a p.a.i. servo system within the recorder. Some readers may have this very curious case and wonder why the output from the p.a.d. comparing the crystal and recovered tape-clocks is not simply connected to the motor driver circuit. The answer to this is to consider the speed dynamics of the motor and the playback servo loops are totally different. On record, the tachogenerator is directly coupled to the motor, but on playback the recovered tape clock is mechanically coupled to the motor through the capacitor and belt drive. It is not possible to achieve a p.a.i. by the more obvious method as the motor is well regulated and disturbed, locking up, any vibration of the belt drive. The solution used here is very much more satisfactory, as it offers a very convenient method of switching from a variable reference frequency on record to another (on playback). Having by a very much lower natural frequency for the p.a.d. at an external frequency generator, for that of the motor speed control circuit, the instability produced by the belt drive mechanism is removed by a 220 pF capacitor. This is shown in block form in Fig. 11 of part 2.

Power supplies
The Hart version of the Linsley-Hood cassette recorder is mains-powered but can very conveniently be made to operate from a 24 volt d.c. source. Because there was a requirement for the recorder to be operable independently of a mains supply it was decided that it, too, should be capable of operating from 24 volts d.c. As a result, the power supply of Fig. 49 was designed and constructed. Since a very large number of c.m.0.s. Ics are used in the digital circuitry, it was decided that they were worth protecting from any overload spikes. Consequently the 'crowbar' circuit was added in the event of an overload, the transistor is triggered, causing the fuse in the positive supply rail to the 7815 regulator to blow. An overload of approximately 16 volts is needed to trigger the 'crowbar' circuit.

A switching inverter circuit, shown in Fig. 50, is used to generate the negative rail voltage. The heart of the circuit is the 7840 switching inverter. Using the values indicated, the output voltage from the switching inverter circuit across the 47µF capacitor should be approximately -48 volts, at a load current of about 120 mA. This type of switching inverter does not operate in the usual manner of varying load conditions, so a shunt regulator is used to drop the -18 volts to -15 volts. Approximately -15 volts to the -15 volt pin of the various analogue and digital i.c.s in the circuit; there is thus no need for the 2N3053 transistor to be fitted with a heatsink. The 2N2905 transistor of the switching regulator also dissipates little power and needs no heatsink.

Modifications to tape-recorder
The Miller-coded data recorded on tape is effectively a series of square-shaped pulses, ranging in frequency from about 5 kHz to 11 kHz, which should be recorded, or distorted by the recorder. It is possible. The transient response of the tape-recorder is more important, in its present form, than a flat frequency response. To obtain the desired record/replay characteristics, the signal level, bias and equalization must be adjusted. Firstly, the frequency response of any tape-recorder is the wider, the lower the signal level. In normal use, the level of the signal to be recorded is a compromise between frequency response, distortion and signal-to-noise ratio: too high a level results in distortion and too low a level results in a poor signal-to-noise ratio. The signal-to-noise ratio is not a problem in the present use of the tape-recorder since the Miller-coded data is recorded at a constant level signal with no amplitude variation. The recording level can thus be fixed, thus improving the quality of the signal in terms of frequency response and distortion, provided, of course, it is not reduced to a level where noise imposes itself on the signal. The level of the high-frequency bias can have a considerable effect upon the recorder's frequency response; high levels of bias producing an attenuation to the high frequency signals but some reduction in distortion.

Finally, adjustment of the equalization characteristic has a great effect upon the amount of high-frequency bias and modifies considerably the transient response of the recorder. In addition to all the possible adjustments, mentioned earlier, it must be forgotten that the quality of the tape used is of prime importance. The author formed a considerable liking for Marxel UXDLX II cassette tapes, with a CRO-type tape, requiring a high bias level and a 70µh equalization characteristic and has all the usual advantages of good frequency response, etc. The cassettes are also very convenient from the replay amplifier point of view since there is no Installing tape available - other tapes may perform just as well - but the tape recording should be set up using this tape. Having satisfactorily adjusted the tape-recorder to operate with the digital electronics, other brands of tape may be tried to determine their suitability.

When I began with the Miller-en-coded data on tape to discover how well the recorder performed, a problem occurred with the transport mechanism that was not immediately appreciated. The replayed signal, having passed through the peak detector and Miller decoder, was found to contain errors in the data stream which were initially thought to be due to the recorder's limited frequency response. Consequently, I experimented at length with the various adjustments mentioned earlier. Subsequently, the main reason for the errors in the decoded data was found to be due to inaccuracy in the take-up spool of the tape-recorder, which was caused by incorrect operation of the 'slipping-clutch', mechanism driving the take-up spool. The slipping-clutch was not, in fact, slipping, but the brass bush on the end of the slipping-clutch spindle, in contact with the rubber-tyred pulley of the take-up spool mechanism, was slipping. The problem was effectively cured by taking the slipping-clutch mechanism apart and 'sharpening' its compression spring. The author is pleased to be able to say that a second tape-recorder, bought from Hark Electronics at a later date, has a cassette deck with a modified slipping-clutch mechanism that gave no such problems. However, as a result of this fault, the author discovered a number of adjustments that should be made to the recorder to improve its record/replay characteristic of the Miller waveform.

- The 0dB recording level of 2.25 volts r.m.s. at the output of the recording amplifier should be increased to about 4dB to 1.42 volts r.m.s., which corresponds, on playback, to an output of about 250 mV r.m.s., i.e. 4dB down on the original 400 mV level. The "VU" meter circuit should be set up using this tape. Having satisfactorily adjusted the tape-recorder to operate with the digital electronics, other brands of tape may be tried to determine their suitability.

When I began to use the Miller-en-coded data on tape to discover how well the recorder performed, a problem occurred with the transport mechanism that was not immediately appreciated. The replayed signal, having passed through the peak detector and Miller decoder, was found to contain errors in the data stream which were initially thought to be due to the recorder's limited frequency response. Consequently, I experimented at length with the various adjustments mentioned earlier. Subsequently, the main reason for the errors in the decoded data was found to be due to inaccuracy in the take-up spool of the tape-recorder, which was caused by incorrect operation of the 'slipping-clutch', mechanism driving the take-up spool. The slipping-clutch was not, in fact, slipping, but the brass bush on the end of the slipping-clutch spindle, in contact with the rubber-tyred pulley of the take-up spool mechanism, was slipping. The problem was effectively cured by taking the slipping-clutch mechanism apart and 'sharpening' its compression spring. The author is pleased to be able to say that a second tape-recorder, bought from Hark Electronics at a later date, has a cassette deck with a modified slipping-clutch mechanism that gave no such problems. However, as a result of this fault, the author discovered a number of adjustments that should be made to the recorder to improve its record/replay characteristic of the Miller waveform.

- The bias oscillator frequency should be raised from about 55kHz to nearer 80kHz by replacing the capacitor, C24 (10µF), of the bias oscillator circuit with one of 6.8µF and by changing R30 from 150 ohms to about 200 ohms.

- The 70µs playback equalization characteristics must be used and a slight improvement may be obtained by changing the value of C6, on the replay board, from 33µF to 18µF.

- The bias level should be high with the 47k variable resistor adjusted for the highest level possible. This should be read in bias voltage, as measured at the junction of the 47k variable resistor, and the 220µF capacitor (C13 or C14), of about 10V r.m.s.

- The actual bias level does not appear to be very critical, but a high level produces a steadier signal, on replay, with less amplitude fluctuations. The recorded signal has a low-frequency content below 5.5kHz and the recording level should be high with the 47k variable resistor adjusted for the highest level possible. This should be read in mmf, as measured at the junction of the 47k variable resistor, and the 220µF capacitor (C13 or C14), of about 10V r.m.s.

- The actual bias level does not appear to be very critical, but a high level produces a steadier signal, on replay, with less amplitude fluctuations. The recorded signal has a low-frequency content below 5.5kHz and the recording level should be high with the 47k variable resistor adjusted for the highest level possible. This should be read in mmf, as measured at the junction of the 47k variable resistor, and the 220µF capacitor (C13 or C14), of about 10V r.m.s.
50MHZ stays good

In the February WAA the author suggested preamplifiers that “fewer transatlantic signals have been heard on 50MHz this winter although some 28/30MHZ cross-band working remains possible”. J. R. R. Baker, GW3HWH, near Aberystwyth, Dyfed, a devoted 50MHz enthusiast, feels my comment does less justice to what, in his view, has been an even more fascinating period than two years ago at the peak of Sunspot Cycle 21. Then, he admits, there were outstandingly strong 50MHz signals that enabled a number of British amateurs to work all ten American “call areas”. Altogether some 150 British amateurs and more than 20 western European stations participated in the transatlantic cross-band working. A few European stations, including about a dozen in Holland, were permitted to transmit on 50MHZ.

Good results were also achieved during the 1980-1 season, with rather more Central American and Caribbean signals. No higher hopes were held for the 1981-2 season, yet GM4HWH considers it has proved as good, if not better, as the two previous years: a few openings in late October, daily openings throughout November (except November 7), almost daily in December, and occasional openings in January/February. Baker, who has been making contact with the Americas for over 40 years, says he has made his 449th cross-band contact for the season, compared with about 400 in each of the last two previous years, including many Caribbean and South American stations. Ken Ellis, G3KWH, contacted 48 of the American States. Several British amateurs made 750MHz contacts with Canadian VE1A.

These results, two years after the peak of Cycle 21, are being regarded as so encouraging that it is proposed to publish a regular newsletter for 50MHz enthusiasts (from G4HCC or G4HHL for modest payment to cover postages and stationery).

The GaAs Mosfet

The current availability of lower cost gallium-arsenide devices, including dual-gate mosfets at around £3 or less, means that receivers with noise figures of under 1dB are available for £15. Such devices can now be achieved by amateurs on 144 and 432MHz. Devices include the 3SK97 and 3SK80. Region 1 reports that the Irish Radio Transmitters Society will be 50 years old in June and will soon become available from European firms. For example, D. J. Robinson, G4FRE, has measured the noise figure of a C. Dennis, EL129 (formerly DNX) who is widely believed to have been the owner of the world’s first non-professional experimental wireless station, established in 1898. During World War II, those Irish amateurs who were not enrolled in the Forces, offered their services as listening stations.

Awards knocked

Bill Verrall, VK5SW, writing in Amateur Radio, has strongly attacked many of the proposals of the emphasis on DXCC and other “Award collecting” by amateur radio operators. He believes these have led to such abuses as “dx nets” claiming exclusive occupancy of spot frequencies; an increase in the amount of deliberate jamming and interference; use of illegally high power; spurious frequency operation by “radio-operators” that spreads interference over many channels; blanket soliciting for “dx-peditions” funds and extraction of payment for QSL cards; and the use of QSL cards bearing political or “religious” messages. He also condemns the recognition of unhabitable rocks and reefs as “countries” and the risks that this involves for those who set up stations at locations which may at times be entirely covered by the sea; “boosting” QSL cards that may be entirely fake, or sent or sold to stations with which no contact has been made, and the comparison made with the standard RTTY report (59/0). J. P. Arendale, VK3KAIU, Federal president of the Wireless Institute of Australia, has pointed out that despite the growth in the number of training courses by clubs and educational bodies, newcomers still need more practical assistance from active and competent amateurs of experience: “the newcomer has to learn the ways of amateur radio, the procedures and the standards, and the various general man’s agreements about such matters as band limits, correct repeater operating, etc. . . only a few clubs provide practical “hands-on” experience”.

In brief

Gerald Stancey, G3MCK identifies the “Early French Resistance survivor set” in Toulon museum (“Clandestine Radio—the early years” February issue) as an early SOS equipment, type A. He has also drawn attention to a book published in France “Armement Clandestin” by Pierre Lorain, F2WLF, which includes details and circuit diagrams of a number of British and German set manufacturers. The photograph by the way was taken by Dick Rollema, PA6E "... The 1982 RSGR HVF Convention is at Sandbach Golf Club, in May this year... The March Amateur Radio Society Exhibitions is at Belle Vue Leisure Park, Manchester, on April 4th. The Northern Amateur Radio Society has its third annual rally at Tamar Secondary School, Paradise Road, Millbridge, on May 8th... PAT HAWKER, GIVA WIRELESS WORLD APRIL 1982

E.P.R.O.M. PROGRAMMER

Most commercially available e.p.r.o.m. programmers are expensive as they include software and other facilities to enable them to be used on their own. The cost of a programmer can be significantly reduced if it is designed for use with an existing microcomputer processor system, as will be shown in this article. The design presented is for 2708, 2716 and 2732 e.p.r.o.m.s, but with small modifications other devices may be programmed by

by H. S. Lynes

Sooner or later, probably all serious microcomputer system users in the hobbyist field will consider incorporating a programable e.p.r.o.m. (erasable programmer- readable only memory). Unfortunately, commercial e.p.r.o.m. programmers are expensive and include facilities not essential for the enthusiast, who usually only wants to program the occasional device.

Commercial programmers fall into two main categories: those in the first category are expensive, have built-in address display and use “personality cards” for programming different e.p.r.o.m. types. Units in the second category are much more expensive. They have all the facilities of programmers in the first category but also include built-in d.v.t., tape interface, printer port, etc. All these programmers use computer software and require random-access memories to enable e.p.r.o.m.s to be programmed or modified at will.

But if an existing microprocessor system is used to control an e.p.r.o.m. programmer, these facilities are unnecessary. I therefore explored the possibility of adding e.p.r.o.m. programming hardware to an existing system. The first problem is to decide on a suitable e.p.r.o.m. to be programmed. In this case an erasable 2708 e.p.r.o.m. was chosen. This is available from most computer and microcomputer dealers for a few pounds costs. The 2708 is an 8K x 8 device but a 12K x 8 device would probably be more suitable and is available from the same sources.

A programmer was designed for the 2708. The programmer has a number of advantages over existing designs. These include its small size, that it can be made for about £25 (even less if a spare 2708, etc., is not purchased) and that the 2708 in the programmer is the same as the 2708 available from the microcomputer dealer. This means that the programmer is designed around the microcomputer and the existing interface is the 2708. This eliminates the need to modify the microcomputer interface if one wants to use the interface for different applications.

Fig. 1. The three e.p.r.o.m.s for which the programmer was designed with tables showing control and programming logic requirements.
encountered was that programming requirements for different types of e.p.r.o.m. can be vary considerably. Also, there is no standardization in pin configurations. So, taking into account the popularity, price and availability of various e.p.r.o.m.s, it was decided that the programmer should be designed for 2708 and 2716 (5V supply) e.p.r.o.m. types. As the 2532 looked promising at that time it was also included. The latter device is similar to the 2716 both in pin assignments and programming requirements, although its inclusion meant that an additional address line would be needed. Design objectives were thus as follows:

**Table 1: Wiring from the 8255 p.p.i. and supplies to the e.p.r.o.m. programming board. Lines with prefix PA are for addressing and lines with prefix PB are for data. Prefix PC denotes lines used for both address and data.**

<table>
<thead>
<tr>
<th>E.p.r.o.m. socket pin numbers</th>
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<tbody>
<tr>
<td>1</td>
<td>PB-4 lines</td>
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<td>30</td>
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</table>

For the 2708, I used data published by Intel, which covers the subject of e.p.r.o.m.s at length. This data was used to define the programming pulse rise-and-fall time limits of 0.5μs-2μs. For the 2716, Mosek data was used (which agrees with Fairchild and Hitachi data), and for the 2532, Hitachi data. The latter manufacturer's data was easiest to understand. Pin configurations and level requirements are given in Fig. 1. Although these three devices are at present the most popular, readers designing new systems using e.p.r.o.m.s might want to omit the 2708 programming facility, since one 2716 can be obtained for less than the price of two 2708's. Furthermore, the 2708 must be programmed in small stages sequentially — a process often called "spray-coat" programming. This is inconvenient when developing using 1K × 8 devices but if 2K or 4K devices are used, the method is intolerable. Fortunately, later devices may be programmed bit-by-bit as required. Inclusion of the 2532 programming facility is now justified, since it can be obtained for less than the price of two 2708's. The reasons for not including the 1702 among the chosen e.p.r.o.m.s are that in my view, programming of it requires twisted logic, it is relatively expensive and it cannot be used with the software for the chosen devices in read mode. The programmer was designed for use with a 6800 microprocessor system but it is based on an 8255 programmable peripheral interface (Intel or National Semiconductor). Some extra logic is required to drive the 8255 control pins but this p.p.i. provides three 8-bit ports and programming is relatively simple. If the 6821 had been chosen, two I.C.s would have been required and programming would, in my view, have been more difficult: there is no reason why support devices should not be chosen for their ability to fulfil objectives.

The 8255 is used in mode 0 (see manufacturer's data for further information) with the 8-bit ports A and C as outputs and port B as either input or output depending on the control word stored in one of the device's four memory locations. By changing port B from output to input it is possible to check that data entered into the e.p.r.o.m. has been correctly received. This function corresponds to the verify function of expensive programmers.

Since e.p.r.o.m. bits are all at logic 1 when the memory is empty, it would be possible to check the amount of memory available in partly full 2716/2532 devices. Unfortunately, the 6800 uses instruction FF to store the index register so confusion could result if the end of the existing program used FF as an instruction or address.

It is advisable to finish programs with three 00's to avoid the risk of placing a new program over the top of an existing one.

![Fig. 2. Simplified block diagram of the programmer.](image)

**WIRELESS WORLD APRIL 1982**

![Fig. 4. Address decoding for the 8255 and one other device (see text).](image)

![Fig. 5. Circuit for selecting the most significant digit of the p.p.i. address (see Fig. 4).](image)
also, a careful note of the current program state of each e.p.r.o.m. should be made. colour coding the i.c.s makes it easy to log their history.

figure 2 is a block diagram of the programmer, and logic conversion for driving the 8255 r.d and w.r lines from the 6800 is shown in fig. 3. if an 8080 processor is used to control the programmer, this conversion is not required.

the 8255 address, see fig. 4, requires four consecutive locations. in my system the address is fully decoded, but the four most significant address lines can be altered using a d.i.d. switch as shown in fig. 5. the four locations are from x500 to x503, where x may be from 0 to f depending on the d.i.d. switch setting. being able to change the address is useful if the 8255 is to be used as a general purpose port, as opposed to being dedicated to e.p.r.o.m. programming.

table 1 shows lines from the p.p.i. to the board on which the programming socket, switching between 2708 and 2716/2712 functions, and a voltage regulator were mounted. in the table, pins 18 to 21 of the programming socket are shown as the 2708. in practice, pins 18 to 21 are connected to a 4-pole, 2-way d.i.d. switch so that they may be taken to p.c3, p.c2, p.c6 and p.c5 respectively when 2716/2712 e.p.r.o.ms are to be programmed. p.c is 22v and p.c4 a 12v signal, the conditioning circuits of which will be shown later. p.c is used to check logic but it could be used to detect changes on pins 18 to 21, or even omitted to reduce the number of lines from the p.p.i. circuit to the programming board. 37 lines were used, as shown in the table but by omitting unwanted lines, combining the 0v rail and bringing in the 30v supply separately, the total may be reduced.

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Digital filter design

Accuracy, versatility and a rapidly declining cost will ensure that digital filters take over from their analogue counterparts. A new sense gives their theory, design techniques and microprocessor implementation.

Program exchange by telephone

There is a growing need to facilitate the easy exchange of programs and data from one person to another, Philip Barker discusses program distribution and the design and implementation of software systems capable of loading source code programs into memory.

Orchestral sound, halls and timbre

Taking the Kingsway Hall as a model, Denis Vaughan investigates the effect of concert hall shapes and sizes, and the working of the filtering of the outer ear on timbre and perceived directionality.

On sale April 21
Arthur C. Clarke honoured

The science writer, Arthur C. Clarke has been chosen by the Radiocommunication Bureau to receive the seventh Marconi Fellowship Award by the Marconi Fellowship council.

British Telecom has been chosen in recognition of scientific achievement for the benefit of humanity in the field of telecommunications and science and technology.

The award is in recognition of transoceanic communications satellites as early as 1945 in the Wireless World article ‘Extra-terrestrial relaying: can we establish regular communications over the oceans?’ We issued a reprint of the article with ARA in 1981 issue. In it the address clearly states the scientific approach to solving the problems of launching artificial Earth satellites and the use of such satellites for communications over the oceans.

The award is for contributions to the development of transoceanic communications technologies and his work has been used by VPL, Ltd. to produce a series of black and white television transoceanic communications systems.

Clarke’s other interests include the use of space technology for observing the Earth and the use of a satellite to detect and measure solar activity. He is currently working on the development of a solar-powered satellite for the Science and Society programme.

The award ceremony will be held this month and will be attended by representatives of the Marconi Foundation.

Teletext, a new electronic data service

One way to mass market viewers is believed to be the growth of private satellite systems which are compatible with Prestel, used by the industry in one way or another. A new approach to this is the development of a more attractive Prestel package for the consumer.

The idea is to work on a package on an agreement with a satellite operator, providing an overall package which would include the service, the antenna and the receiver.

In February of this year, a Commitment Conference was held in London to plan a further campaign for 1983. The first result of this, a commitment by the industry, is likely to be a reduction in the cost of viewers to the consumer and some improvement in the service and the quality.

Further analysis of this is being carried out by the companies in the industry and will be reported in the next few weeks.

The companies are already running at hundreds of thousands of phones a week. The documents are not yet on the switchboard in the Radiocommunication Bureau and London Information have told us that they have recently supplied copies of压缩的 publications and a large number of letters to electronic firms.

This is good news for the consumer who will benefit from the lower cost and better service.

Free specifications and standards

London Information have started a free consultancy service, which is to be held in the new year, and will accept the plans and standards or other documentation which they may need for their projects.

The documents are not yet on the switchboard in the Radiocommunication Bureau and London Information have told us that these are regarded as ‘unacceptable’ by the R.S.D.B. which immediately called for urgent discussions with the Home Office.

The new schedule, as printed, not only introduces the new international standards and definitions but also introduces a number of changes to the earlier standards.

The Home Office, as well as the Home Office, is expected to receive a new schedule of frequency dependencies, classes of service and various other documents from the International Radio Regulations.

A report on the progress of the Home Office in the preparation of the standards, as printed, not only introduces the new international standards and definitions but also introduces a number of changes to the earlier standards.

The Home Office, as well as the Home Office, is expected to receive a number of new documents from the International Radio Regulations.

The new schedule, as printed, not only introduces the new international standards and definitions but also introduces a number of changes to the earlier standards. New documents have been added to the schedule, including a range of options to the Home Office, which offer a wider range of options and different levels of service.

The boards are interested in the introduction of a MultiSuite system with 24 address lines for up to 16 messages to the home office. The computer is manufactured by Bletchley's factory in Luton, Luton, and is to be marketed through a network of distributors throughout Europe. The majority of the computers are likely to be sold to O.E. M. A version of the computer is being produced and this will also be offered on Xenix.

Xenix and the supermicro

Xenix is the name of a computer operating system for use on 16-bit microcomputers. It has been developed by Microsoft and is an implementation of Unix, a software system originally developed by Bell Laboratories for use on DEC microcomputers, first on the PDP-11. Xenix is the 16-bit operating system which seems likely to be the standard, much as CP/M has become for the 8-bit processor. One advantage is that it is simple and easy to use.

All this is by way of introduction to the Bledsoe 600 Xenix computer which uses the Z8001 16-bit microprocessor. The Z8001 runs at 4Mhz and can address up to 8 megabytes of memory through a 23-bit address bus. The Bledsoe computer is a general-purpose application for professional system designers and engineers and may be used in simulation, process control, image processing, instrumentation, scientific workstations. It may also be used for office automation equipment, communications networks, banking/financial systems etc. The new customers are the Monotype Corporation, who will use the computer for typesetting and precision, Software information services company.

The computer is modular design, configurable, from a range of options to meet the requirements of the user who offers a wide range of options and different levels of service.

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Eddie Bledsoe, the managing director of Bledsoe Computer Systems believes that Xenix will be very popular in scientific and educational applications because of the widespread use of Unix in DEC computers. As Xenix is in the forefront of users of Xenix, he intends that his company will maintain that position and become a leading centre of expertise in Xenix.

7. Zing has given their official blessing to CP/M and Unix and have warned that manufacturers should be wary of "lockbox" systems. Traditionally a new computer system engendered a new operating system which became 'machine-dependent'. So if a computer system was selected, the system was designed around it and the user became stuck with it. If, however, the operating system was selected first then a number of manufacturers could offer computers which operated the system. CP/M and Unix are candidates but some systems are being marketed as "Unix-like", for example, but do not have the universal application or common development of the original. There is a feeling that the world may become entirely "Unix-like" and CP/M and Unix both operate under Unix.
SIMPLE POWER AMPLIFIER

Complementary Hexit devices offer improved performance over the equivalent bipolar output stage and allow simplified drive circuitry. This design delivers 60 watts into a four-ohm load, 32 watts into an eight-ohm load, from a ±30V supply.

by Peter Wilson
International Rectifier Co

The split power supply rails of this design give good rejection of supply voltage ripple allowing both a simple supply circuit to be used and the load to be directly coupled. The output devices operate in the source follower mode, which offers a two-fold advantage: the possibility of oscillation in the output stage is reduced as voltage gain is less than unity, and signal feedback through the heat-sink is eliminated as the drain terminal, which is electrically connected to the tab on the TO-220 package, is at a direct voltage.

Symmetrical output is achieved by providing a "boot-strapped" drive to the gate of the n-channel device from the output. The use of the bootstrap circuit, C2, R5, R6, also allows the source to operate at near constant current, which improves the linearity of the driver stage.

The diode clamp the bootstrap circuit, restricting the positive voltage at the gate of Tr5 to +VCC to maintain symmetry over load conditions.

Transistor Tr5 and resistors 11, 12 & 13 provide gate-source offset voltage for the output device with R17 variable to adjust quiescent current for variation in threshold voltage. A degree of temperature compensation is built into the circuit as both the emitter-base voltage of Tr5 and the combined threshold voltages of the I.e.n have a temperature coefficient of -0.3%/deg C.

The class A driver transistor operating at a nominal bias current of 5mA set by R3 is driven by the p-n-p differential input pair biased at 2mV by R4. Component C2 sets the closed-loop gain of the amplifier, R7/R4 and provide low-frequency gain boosting. Additional components R4, C connect to the output and ground suppress the high-frequency response of the output stage, allowing the h.f. performance of the amplifier to be determined by the input circuit. Component R4, C4 at the input of the amplifier define the input impedance and suppress noise.

To achieve 60 watts into a four-ohm load, the current in the load is 3.9A r.m.s. or 5.5A peak. To sustain this source current, the n-channel Hexit, IRF533, requires a gate-source voltage of 5V.

As peak load voltage at 22V, gate voltage to achieve peak power in the positive sense is VGS = VDD = 27V. A similar calculation for the negative peak, using the p-channel device IRF9533, shows that a negative gate bias supply of ±24V is required. Consequently, a ±30V supply is adequate for a 60 watt output, provided that the supply voltage does not fall below ±2V when loaded: a source impedance of one ohm or better. When the supply voltage impedance is high, use a higher voltage supply together with complementary Hexit of a higher voltage rating - IRF552/IRF553.

When an eight-ohm load is used, 32 watts output power can be achieved from a ±30V supply with source impedance better than two ohms.

The curves drawn in Fig 1 show the power consumption of the amplifier, output power and power dissipated in the f.e.t as a function of r.m.s. output current with ±30V supplies and four and eight ohm loads. It can be deduced that the maximum power dissipated in the devices is 56 watts and 28 watts with four and eight ohm loads respectively. Limiting the case temperature to 90°C and making an allowance for the thermal impedance of insulating washers, heat-sink requirements are 0.5°C/watt with a four ohm load and 1.67°C/W with eight ohm load. Smaller heat-sinks may be tolerated if the amplifier is not operated continuously at rated output power.

Open-loop gain measured with gate and source connections to the f.e.t's broken is 30dB, ±SB points occurring at 15Hz and 60kHz. Fig 2. Closed-loop curves are shown for amplifier gains of 100 (R7 = 4700Ω) and 20 (R7 = 220Ω). In both cases the curve remains flat to within ±1dB between 15Hz and 100kHz with an eight ohm load. The slew rate of the amplifier, measured with a 2V pk-pk square wave input is 13V/μs positive-going and 16V/μs negative-going. The discrepancy can be balanced out by addition of a series gate resistor for Tr5.

Reduction of the closed-loop gain from 100 to 20 produces a significant improvement in distortion figure, Fig 3. Considering the simplicity, performance is quite acceptable. The output stage quiescent current was adjusted to 100mA and can influence the distortion measurement significantly if allowed to fall below 50mA.

The dependence of the quiescent current in the output stage and of the output offset voltage on power supply voltage are given in the Table. Current is set by first adjusting the potentiometer R13 for minimum offset voltage — turned fully anticlockwise if the p.c.b. layout shown is used — and apply the power supply voltage, the positive supply passing through an ammeter with 1A f.s.d. It is then adjusted until the meter reading is 100mA with ±30V supply. Remove the meter from the circuit before applying an input signal to the amplifier.

When assembling the printed circuit board, mount the passive components first, ensuring the correct polarity of electrolytic capacitors. Then solder in bipolar transistors, checking for correct pin identification. Finally mount the f.e.t's, avoiding static discharge by shorting the pins together to ground and using a ground lead from the printed circuit board for correct component placement. Check the copper side of the board for solder bridges between tracks, and remove them. Check for dry solder joints visually and electrically using a resistance meter and rework if necessary.

Now apply power to the amplifier with heat dissipation fitted. Adjust potentiometer R13 for minimum offset (fully anticlockwise on the p.c.b. layout) connect an ammeter in series with the positive supply and adjust R13 for a reading between 50 and 100mA.

If a loudspeaker load is connected in circuit, protect it from d.c. overload with a fuse. With the quiescent current set, confirm the output stage offset voltage is zero ±100mV. Excessive and erratic variation in quiescent current as R13 is adjusted indicates circuit oscillation or faulty wiring. Oscillation can only be satisfactorily identified and suppressed using an oscilloscope. Also, supply decoupling capacitors should be mounted close to the amplifier output stage and load ground point.

Additional circuit components have been added to ensure high-frequency stability of the complete amplifier. Placement and values depend to some extent on the printed-circuit board layout. Observe the given time constants when designing the printed circuit board.

Keep the length of connecting lead to the gate terminals of Hexit to an absolute minimum to avoid oscillation of the power output stage. Series gate resistor R13 suppresses oscillation, but too high a value limits slew rate. Series resistor R13 suppresses amplifier oscillation caused by capacitive coupling to the base of Tr.

Phase shift in the amplifier when driving a reactive load can lead to high-frequency instability. With a capacitive load, the addition of a small air-core choke 3μH with an 8Ω tap load restores stability. The final value of the choke is determined by its reactance and may be checked over the frequency range.

With the current set, remove the ammeter from the positive supply and apply a signal to the amplifier input. Signal level required for full rated output is 150-160mV for a gain of 100, and 770 to 800mV for a gain of 20. Clipping of the output waveform when operating at rated power indicates poor supply regulation and is remedied by reducing the input signal amplitude and derating the amplifier. Alternatively a lower-impendence supply. Amplitude response of the amplifier can be checked over the frequency range.
According to Mr. S. Allen of the NRPB, one revised their existing 10 mW/cm² rate, and it is expected that the Americans will gesture new frequency-dependent standards and ACGIH (American Conference of Governmental Most western countries. In America, the ANSI accepted that measurements in the near field, and hence assessment of potential health hazards, are more complex than in the far field. Taking into account near-field effects when determining maximum safe-level standards would nevertheless be sensible.  

As an article recently published in Radio Communications gives a good account of f.r. radiation hazard, as far as the radio amateur is concerned. The authors state that reports of "non-thermal" effects of f.r. radiation, mostly emanating from Eastern Europe, should be "regarded with suspicion," and go on to say, "there is no evidence that f.r. radiation produces long-term damage of the kind associated with ionising, i.e., cancer or genetic damage." Not a hint is given that the authors feel the accepted maximum level might be too high. But not everyone is happy with the situation. Mr. Herbert Goldwing, for one, summarizes the opposing point of view in an article called "Microwave hazards" published in the IEEE Spectrum.

The first of these graphs provided by Mr. Harlin of the NRPS shows f.r. radiation penetration and absorption versus frequency for a given tissue. Combined effects of penetration and "focusing" (or geometry and high refractive index) in a potato are illustrated in the two other graphs taken from the journal Microwave Power.

REFERENCES


Further reading


SITUATION NORMAL...

In your February issue, Fox Hewer requested the "SNAPU" as a coinage of War II. I think he and you readers might want to know its pre-war origin.

During the war it was my pleasure to work for a time with two clever and humorous American Western Electric telephone engineers, and they told me that before the war had had to go to telephone exchanges where there was trouble and rectify it. When they arrived at the site an engineer would make a brief estimate of how serious the trouble was, establish a telephone link to his headquarters and send back a code word. His home base would therefore know that he had arrived where the problem was, have a rough idea of how long it would take to clear them and have a telephone number where he could be contacted if need be. There were three code words: SNAPU, SNAPUP, and FUBAR (all foiled up) or (words to that effect) — TARPU — "Things are really foiled up," and FUBAR — "Foiled up beyond any repair." The latter would be sent, for instance, a telephone exchange had been seriously damaged by fire or flood, while SNAPU would be used for a situation where cables or machinery had been damaged but where repairs or replacement would be relatively straightforward.

SNAPU became widely used in many situations during the war, but strangely the other code words were never understood. It would be a pity if this bit of folk lore was lost.

C. V. Harlen Northwood Middlesbrough

WIREDEECKER

As a radio amateur, I have often been annoyed by the phrase "woodpecker" used to describe transmitters which have plagued the f.r. bands for many years. There has been no official explanation of the purpose of these transmissions, and various theories have been expounded in the media, ranging from UFOs causing death rays. However, as a result of accidentally coming across some of these signals on a laboratory spectrum analyser, and storing the waveforms as a wave is received, I now think I found a better way to light on their structure and purpose.

The first of these graphs provided by Mr. Harlin of the NRPS shows f.r. radiation penetration and absorption versus frequency for a given tissue. Combined effects of penetration and "focusing" (or geometry and high refractive index) in a potato are illustrated in the two other graphs taken from the journal Microwave Power.

The interesting feature is the presence of "glitches" in the top of the pulse, the pattern of which remains the same from pulse to pulse, and which occur at intervals which are multiples of 100 ns. This led me to suppose that the glitches formed a binary sequence of length 31 bits.

I also guessed that the glitches arose from phase irregularities in the transmitted signal, the finite width of the glitches resulting from the finite bandwidths of the system and/or spectrum analyser. Thus, arbitrarily assigning a zero to the first data bit, the original Manchester pattern could be reconstructed, with 0 representing degrees and 1 representing 180 degrees. This gave me the pattern 0000111010011011110110011010001.

The step was to turn out to be a maximum-length, pseudo-random binary sequence, which was generated by a 5-bit shift register with feedback from the parity function of the contents of stages 5 and 5.1 sequentially.
When the On button is pressed, C discharges via the low-voltage winding, inducing an inductive voltage of 1250, 514, and 283 V across the series of output transistors. As a result, the output stage will initiate the transmission of the output data. To ensure a smooth transition from high to low voltage levels, a capacitive coupling scheme is employed. The output stage uses a common-source amplifier configuration, which allows for a low output impedance and high input impedance. This configuration is particularly suitable for driving long transmission lines with minimal power consumption.

Data Storage

I would like to comment on two articles in the January 1982 issue of Wireless World: "Sag to M bic" and "Industrial application of library automation." Both articles discuss the impact of modern technology on traditional library systems and the potential for improved efficiency and access to information. The former article highlights the benefits of using computerized library cataloging systems, while the latter focuses on the integration of library automation with other aspects of information management. Both articles provide valuable insights into the evolving landscape of library services and the role of technology in shaping the future of this important sector of society.

Low-Frequency Sound

I have just read the letter of S. Frost of Edinburgh, who replies to my earlier letter concerning the noise generated by the two high-power loudspeakers. He notes that the noise is generated by the loudspeakers when they are driven at high power levels. However, he is concerned about the potential impact of this noise on the audio performance of his system. He suggests that the noise may be reduced by using lower output levels or by employing active noise cancellation techniques.

The New Electronics

The article by Hugh Jackson in your January edition of Wireless World is a fascinating read. It explores the concept of "the new electronics" and its implications for the future of the industry. Jackson argues that the rapid pace of technological advancement is leading to a paradigm shift in the way we think about electronics, from a focus on hardware to a focus on software and information processing.

In his article, Jackson highlights the importance of software in shaping the future of electronics. He suggests that the rise of the internet and the growth of the mobile computing market are driving a revolution in the way we interact with technology. He notes that the convergence of hardware and software is creating new opportunities for innovation, particularly in areas such as the Internet of Things (IoT) and artificial intelligence.

Jackson also discusses the role of drones and autonomous vehicles in the future of electronics. He suggests that these technologies are revolutionizing the way we think about transportation, surveillance, and disaster response. The rapid pace of development in these areas is creating new possibilities for the future of electronics.

In conclusion, Jackson's article is a thought-provoking read that provides a valuable perspective on the future of the electronics industry. It is a reminder that the pace of technological change is rapid and that those who are able to adapt to this change will be well-positioned to succeed in the future.
RECEIVERS FOR OPTICAL FIBRE COMMUNICATION

During the next few years optical fibre systems will be used increasingly for long-distance telecommunications with emphasis on achieving greater bandwidth and greater spans between repeaters. In this rapidly developing subject it is essential to be aware not only of the latest published results but also of the underlying principles to fully appreciate the potential of optical communication. With this in mind, Dr Garrett reviews both the best reported performance in detectors and the areas where there is still room for improvement.

Optical fibre communication systems are beginning to be used extensively for data and for long-haul systems. The fibre “generation” of systems operates in the near infrared—a wavelength of about 0.85 µm, where light can be made from gallium arsenide and detectors (or PINs). At slightly longer wavelengths, 1.3 to 1.6 µm, glass fibre is a better transmission medium, having enormous bandwidth and extremely low attenuation—0.5 dB/km or even less. Fiber systems are being used to carry carrier services, and the cost comes down, it will become economic to use fibre systems at lower data-rates as well, and also to transmit television or entertainment or for teleconferencing.

The three basic functions of an optical receiver are to convert the signal from an optical to an electrical form, to amplify the signal, and to remove the variations in the transmitted message. The first of these is performed by an optical detector. Amplification is not specific to the detector, as the transmitted signal contains the special design of the front-end of the receiver, and detection determines the sensitivity. Estimation and regeneration of the message then takes place at the receiver and various system impairments; only the more basic ideas are covered; for more depth refer to the bibliography. In these functions, an optical receiver seems similar to its radio receiver. However, optical receivers are quite different in the way in which they perform. Here, energy detection, universal in radio practice because of its excellent sensitivity and simplicity, is the only choice that provides meaningful performance in optical receivers. It requires a local oscillator which matches the arriving signal in frequency, phase, and polarization. Today’s semiconductor lasers have spectral line-widths of 30 MHz to 1000 GHz, and current fibres do not provide a predictable polarization at the receiver end. Although there are advantages of increased sensitivity and use of frequency and phase-shift keying have some attraction, these systems are still in the research stage, and other problems, today’s systems use incoherent (direct), detection, in which the wavelength of the optical carrier is sensed.

Unity-gain detectors

The device which converts the optical signal to an electrical form must be efficient at the operating wavelength and must respond at a speed appropriate to the message data rate or frequency band. One may want to require a certain average power which can be operated at ambient temperature from a certain voltage or be capable of operation with a small, light, and reliable device. Semiconductor photodetectors all fit these requirements remarkably well, and there is little interest in other types of detector for optical telecommunication, as the operating wavelength of optical fiber communication systems is far from the terrestrial environments. Photodetector design and operation involve the device structure, in which there are considerable differences, and the device must be designed so that the field required to deplete the device is large enough for the device to be useful in a broad 0 kHz to 350 MHz, so that several tens of microns of silicon must be depleted for almost complete absorption. Very little of the incident radiation is absorbed in the undepleted region of the junction. For the silicon p-i-n photodiode structure used in practice. It is a silicon device designed for the wavelength range of 0.85 µm, with a nominal absorption region 30 µm thick in low-doped material. The absorption coefficient of nondepleted material is about 10 cm⁻¹ at 660 nm and 30 cm⁻¹ at 550 nm, so that several tens of microns of silicon must be depleted for almost complete absorption. A disadvantage: coupled with the high density of states in the conduction band it means that the absorption length is large, which degrades the performance of an optical receiver. The other possible materials are the so-called group III-V compounds, binary compounds of elements from group III and V such as gallium arsenide and indium phosphide. To detect light at 1.55 µm, a material with a bandgap in the region of around 0.7 to 1.0 µm. The binary III-V compounds such as GaAs, InP, and GaInAsP. In other materials, the bandgap can be adjusted over a wide range by selecting a suitable composition. Reverse bias is used to shift the detectors in germanium by one or two orders of magnitude typically because of the much smaller density of states in the conduction band. Recently, the H-HEV compounds such as GaAs/AlGaAs have also been used as these materials are used for high-speed photodiodes in communication systems. The second device illustrated has an absorbing layer of InGaAs deposited on an InP substrate, and the p-n junction is formed by diffusing a dopant such as Zn into the absorbing layer. This device is designed for a wavelength of 1.0 to 1.1 µm, in which the InGaAs layer has a high absorption coefficient, around 100 cm⁻¹, so that a thin absorbing layer is needed, about 3 to 10 µm. This makes the response fast, but any long-term incident radiation is absorbed in the undepleted substrate. The efficiency is reduced considerably. It is not easy to construct a detector with a high efficiency, i.e. through the InP substrate, which is transparent at wavelengths beyond 0.95 µm.

The quantum efficiency of a photodiode is the number of carriers pairs formed on average for each incident photon. It is less than unity in practical devices for three main reasons: carriers are partially reflected; some carrier pairs are formed in undepleted material and do not contribute to the output currents; and some carrier pairs recombine before reaching the terminals of the device. To improve the quantum efficiency, the surface of the device is often being nearly intrinsic. The wide depletion reduces the junction capacitance too. The device illustrated has 100µm in diameter and has a capacitance of less than 0.1 pF. At wavelengths beyond 1 µm, silicon becomes increasingly transparent and a different material is required for photodetectors intended for communication systems. GaAs has a maximum absorption region 30 µm thick in low-doped material. The absorption coefficient of nondepleted material is about 10 cm⁻¹ at 660 nm and 30 cm⁻¹ at 550 nm, so that several tens of microns of silicon must be depleted for almost complete absorption. A disadvantage: coupled with the high density of states in the conduction band it means that the absorption length is large, which degrades the performance of an optical receiver. The other possible materials are the so-called group III-V compounds, binary compounds of elements from group III and V such as gallium arsenide and indium phosphide. To detect light at 1.55 µm, a material with a bandgap in the region of around 0.7 to 1.0 µm. The binary III-V compounds such as GaAs, InP, and GaInAsP. In other materials, the bandgap can be adjusted over a wide range by selecting a suitable composition. Reverse bias is used to shift the detectors in germanium by one or two orders of magnitude typically because of the much smaller density of states in the conduction band. Recently, the H-HEV compounds such as GaAs/AlGaAs have also been used as these materials are used for high-speed photodiodes in communication systems. The second device illustrated has an absorbing layer of InGaAs deposited on an InP substrate, and the p-n junction is formed by diffusing a dopant such as Zn into the absorbing layer. This device is designed for a wavelength of 1.0 to 1.1 µm, in which the InGaAs layer has a high absorption coefficient, around 100 cm⁻¹, so that a thin absorbing layer is needed, about 3 to 10 µm. This makes the response fast, but any long-term incident radiation is absorbed in the undepleted substrate. The efficiency is reduced considerably. It is not easy to construct a detector with a high efficiency, i.e. through the InP substrate, which is transparent at wavelengths beyond 0.95 µm.

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given an anti-reflecting dielectric coating like the blooming of a camera lens; the surface reflection coefficient must be reduced from around 30% to almost zero. If the light has to pass through undepleted material, as in the lower diagram, it is kept as thin as possible or made of a semiconductor which is transparent at the wavelength of interest. Recombination of carriers within the depletion region is generally minimized by reducing deep-level impurities and crystal defects as far as possible.

The depletion layer thickness d is determined by the applied voltage V and the doping level N0.

When is the electric charge and is the the relative dielectric constant, typically to 15. Junction capacitance is

Where A is the area of the junction. These detectors are usually operated at 3, assuming a device diameter of 100 µm. The device of 100 to 1000 µm² are available in silicon, so that a few tens of microns of silicon can be depleted at 5 to 10 volts. In the device of 100 to 1000 µm² the best are available, so that 15 to 20 volts are required to deplete a wafer, and that is the maximum operating voltage which is typically 0.1 to 0.5 pF for a high-speed detector so that the capacitance of a packaged device is usually dominated by the package.

The reverse bias leakage current (dark current) of a photodiode is important because the shot noise on this current can be the dominant noise source in some situations. The dark current is caused by current leakage in the device, which is typically a few parts per million. This is because the device as well as the depletion region (bulk leakage). Surface leakage is minimized by adopting the device with a passivating layer: methods vary from one material to another. The two most important minority carriers from the undepleted

Fig. 1. Silicon p-i-n photodiode is suitable for PIN photodiodes from 0.8 to 1.0µm (bottom).

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Fig. 2. Silicon p-i-n diode chip, top, 1mm square with 100µm circular pin, and bonding pads beside it. Chip capacitance is below 0.1 pF, and reverse bias leakage current is around 50 pA at 10V bias. Quantum efficiency at 0.85µm wavelength, corresponding to gallium arsene diode injection laser, is 0.5. Active area of InP/GaAs photodiode is 1.0x1.0 mm in diameter. The quantum efficiency is also higher than 80% for 1.0 µm, but the problem can be overcome by illuminating through the substrate. anti-reflective coatings also increase efficiency.

Fig. 3. Depletion voltage and junction capacitance as functions of the depletion layer thickness and the material. Parameter k is the ratio of ionization rates for electrons and holes.

Fig. 4. Avalanche gain as a function of field strength and the material. Parameter k is the ratio of ionization rates for electrons and holes.
when the threshold d is set between 0 and 1 photons. The error probability is then P_e = \frac{d}{2} and one cannot have zero error probability with finite m. For P_i = 10^{-3}, m = 11.5 and for P_i = 10^{-4}, m = 20.

In an analogue system, we are interested in the signal-to-noise ratio (SNR) at the output of a pre-detection bandwidth B which smooths fluctuations over an integration time T = 1/B. If the noise ratio arrives at r then the number m which arrives, on average, is given by m = rB. At the output of the signal, the power is proportional to m, while the noise power is proportional to r − m. Thus, the signal-to-noise ratio is just m.

\[ m = T \sqrt{r} \]

For example, a 30dB signal-to-noise ratio and a 1MHz bandwidth requires, average, \( 2 \times 10^{20} \) photons or 40 nW at a wavelength of \( 0.7 \mu \text{m} \).

That is the best performance one could expect, even with a perfect detector and a noiseless amplifier, limited only by the quantum fluctuations in the incoming optical signal. In real life, amplifiers are not noiseless because electrons in the conductors move with randomized velocities with respect to the amplifier itself. Using conventional component amplifiers, an input capacitance of 10pF and a bandwidth of 10MHz would need to have an input resistance of about 1000 MΩ. This is the photodiode. The mean square thermal noise in a bandwidth B due to a resistance R is \( kT_\text{m} = \frac{1}{2} \pi^2 kT \) at room temperature for an R of 5 kΩ. The noise figure F ranges from 0.2 to 1.9 if we use the average generated across R due to m photons at a wavelength of 1 μm. Detected in time is \( T \), m at \( 10^{-6} \times B \) watts. The signal-to-noise ratio is

\[ \frac{1.6 \times 10^4 m^2}{8.3 \times 10^4 \times 3 \times 10^4 m} \]

so that in a digital system of 22 dB ratio, m is about 20,000 photons in a bit period (taken as 1/2 B here). This is 1000 times or 30dB greater than the quantum limit, which justifies ignoring quantum noise in this calculation. As 30dB can be transduced into a period of about 1 μm at 3 μm by a 60° bend. Generally, the slope of a quantum noise situation is such. There are four ways of increasing the receiver sensitivity to consider. Reducing amplifier noise is one way, obviously – discussed later – another way is discussed in the next section, and in the last section, this two other ways are considered: optical amplifiers and coherent detection.

Avulanche photodiodes

An avalanche photodiode generated by an electric field may gain sufficient energy so that when it is scattered by the lattice a particle has sufficient energy to form an electron-hole pair. The newly created carriers can then cause impact ionization and the avalanche effect.

Impact ionization is useful and current gain. If the type of carrier were capable of causing impact ionization the avalanche process would advance across the high field region and carry the high field region, increasing exponentially with distance while remaining finite. Avalanche breakdown would be expected in an ideal material. However, both carrier types can cause impact ionization, with different efficiencies, providing a regeneration or positive feedback mechanism which can lead to avalanche multiplication.

In principle one cannot even get near to it because of extra noise introduced by the random impact ionization process. Consider a steady optical power P incident on the detector. The resulting multiplication is

\[ n = \frac{C}{2m} \]

where C is the noise excess factor for the avalanche gain process (0 < c < 1). If x is small, as with a silicon diode, the optimum gain is large and the maximum in signal-to-noise ratio is broad. The diode can, in fact, be used to vary the sensitivity of the receiver so provide a.g.c. When x is near unity, less improvement is possible, the optimum gain is lower and the maximum must shaper. Such diodes may be difficult to control for optimum performance.

The theory of the avalanche process and the statistics of excess avalanche noise are important in the study of optimum amplifiers; but they are beyond the scope of this article. Relevant papers discussing this and co-workers in the bibliography for further details. Part 2. To make an avalanche photodiode in silicon with a fast response simple a photodiode junction will not do because most photos in applications are used with a cascade of two or more p-n junctions. In silicon, avalanche breakdown is only reached at 50% of the bandgap, and is about 3.5 volts. Thus, avalanche breakdown is only reached at 50% of the bandgap, and is about 3.5 volts. Thus, avalanche breakdown is only reached at 50% of the bandgap, and is about 3.5 volts.

The characteristic x is related to a, the ratio of ionization rates for holes and electrons. The characteristic x is related to a, the ratio of ionization rates for holes and electrons. The characteristic x is related to a, the ratio of ionization rates for holes and electrons. The characteristic x is related to a, the ratio of ionization rates for holes and electrons.

\[ \sqrt{I_m} = \frac{x}{a} \]

where I_m is the excess noise factor x close to unity. Filled squares are for \( p-n \) a p d receivers in section 2.5.

above 10 to 15. There also noise shown associated with a value of k close to unity.

How is this current gain used to improve the sensitivity of an optical receiver? Current gain arising from avalanche gain increases the signal voltage across the amplifier input and so improves the signal-to-noise ratio as the amplifier noise is unaffected. However, the current gain also increases the quantum noise by the same amount as the signal, so that one cannot get beyond the quantum limit. In practice one cannot even get near to it because of extra noise introduced by the random impact ionization process. Consider a steady optical power P incident on the detector. The resulting multiplication is

\[ n = \frac{C}{2m} \]

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HEATING-FUEL SAVER

Over the season some saving can be made in heating fuel bills by switching on later when the weather is less cold. This feature is usually incorporated in large systems but the unit described, which may be built at low cost, is intended for domestic use. There is an outdoor temperature sensor which is not essential but may be used to monitor the heating system.

The outdoor sensor is a thermistor, of which the resistance (Rt) must be known, or measured, at three relevant temperatures, for example 0°C, 10°C, and 20°C, which is connected in series with a fixed resistance R0 across a stabilised voltage. By appropriate choice of R0 (see appendix), the relationship of the mid-point voltage (V0) to temperature can be quite well linearised, as shown in the table. The timing circuit uses a slow-rising voltage V3, and a comparator to close the switching relay when V0 crosses V1. The ramp voltage V4 is generated digitally using a data-a-converter in the prototype the popular Ferranti ZM432E, clocked at 1.12f. to give for example a delay of one hour per 10°C.

The power supply section shown in Fig.2 is suitable for a standard 24V d.c. oil-based relay, of which the coil resistance is typically 470 ohms. If a different voltage is used, R0 should be adjusted to give 8.12V input to the regulator.

Counting-up

In Fig.3, the 425 internal counter is brought to a high state. The internal resistance ladder is connected to the internal reference source (Vref) by joining pins 15 and 16, and the analogue output V2 at pin 14 is then given by:

\[ V_2 = V_{ref} \times \frac{256}{N} \]

where N is the count reached. The counter has eight stages, and the maximum count is (1+2+4+8+16+32+64+128) or 255. The nominal resistance is 2.56V, giving 10mV/percent, but its exact value is unimportant, since the thermistor Rt is also supplied from Vref as well as V2.

Thus the count must be made up in the second and so on the relay via comparator IC0, which is given by:

\[ V_{out} = \frac{V_{ref} - R_0}{R_0 + R_{ref}} \]

Thus the number required to make Ve exceed V2 and so turn on the relay via comparator IC0 is given by:

\[ N_{min} = \frac{V_{ref} - V_2}{V_2} \times 256 \]

The table shows N values for various temperatures, relating to RS code 151-237 thermistor, which is a close-tolerance device (+0.2°C). Resistance Rt must be made up to within 1% from metal-film resistors. Other thermistors can be used by measuring them and calculating the appropriate R0 (see appendix). Setting-up is easier if test-resistances are made up to substitute for the thermistor at say 0°C, 10°C, and 20°C, and in the prototype these were built in using a four-way switch.

Circuit operation

The 425 is clocked, pin 4, from a conventional 555 oscillator divided by a c.m.s. 4040B. The 425's internal counter is reset by R1, at switch-on, the same function is performed by the 4040's capacitor, which is used to delay the rise of point B. The 4040 (alone) is also reset via R2 when C eventually goes high, so this point at this time is low, causing the i. e. to d. to go continuously.

The selection of IC2 is used to drive a milliammeter from V1 to indicate outdoor temperature, and almost any f.s.d. can be used up to say 5mA. In the prototype an existing 0-100 scale was used for degrees Fahrenheit, and the bimetal shown, and R5 gives a reading of approx 32°C at 0°C, which can be trimmed by the mechanical zero adjustment. The resistance of R5 was made up to give a swing of 36 divisions between 0°C and 20°C (32°F) and any contact type meter may of course be remotely mounted, perhaps alongside your parameter.

Checks

The eight counter outputs of the 425 are available at pins 5-7, and 9-13, and in that order they have weights 1, 2, 4, 8, 16, 32, 64 and 128. A contact could, for example, be made at pins 6, 15, 16, and 20, and R5 corresponds to pins 12, 10, 6, and 5 (and the rest low), and this allows the counting to be checked using the test resistances, and the 'fast' setting of S1. An error of less than 1% is not important. The 555 timing can be checked by a frequency meter, or from the i.e.d., which flashes 64 times the 'slow' 425 count.

Variations

The basic circuit still has a long delay in cold weather, for example 69 counts at 0°C. The delay can be compensated by advancing the time-clock, it is more elegant to suppress it by 'jumping', clocking the 425 directly from the oscillator, point F, until an appropriate count is reached. Figure 4 shows two possible circuits, (b) being preferred in the prototype. The logic shown may be realised in various ways, but diodes and transistors are cheap, and may be laid out on Veroboard. If it is required to use the thermistor when the time-clock is off, the delay unit must be continuously-powered, and reset may then be modified to Fig. 5, in which the time-clock signal is detected by a transistor-type opto-isolator. Reverse voltage is limiting, so resistors should pass 50mA, and may be replaced by a capacitor, say 0.1uF, provided it is a type suitable for continuous mains working. The intermittent output allows the 10uF capacit.

Fig. 3. Delay and thermometer circuits. Unless otherwise stated, diodes are 1N4148 or equivalent, and transistors general-purpose, such as BC548 (NPN) and BC558 (PNP).

The method of calculating Rs does not provide initial reset even if the delay unit is powered up with the time-clock on. Since the 425 count stops at switch-on, it stores the switch-on temperature, which may be read out later in the day by switching IC2, input to V1 (425 pin 14) rather than V4. However it is necessary at the same time to break the normal pin 14 connection, because the feedback with C high raises V1 above its actual switch-on value.

Thermistor mounting

The RS device is a small bead, about 1.5mm diam. For the prototype, a 1.6mm hole was drilled nearly through a 12mm cube of aluminium, then enlarged partway to a push-fit for a 4mm tube about 10cm long, which in turn fits through a 4mm hole drilled in the frame of a north-facing window. The thermistor leads were extended by 702 wires, and the assembly pushed down the tube, so that the thermistor bead entered fully into the 1.6mm hole. A bonded heat-conductive grease was used to improve thermal contact, and the block and tube were painted dull black. Thin twisted wire was used for connection. If a long run is needed, it would be advisable to decouple V1 ground via 10K to suppress any hum pick-up.

Appendix

The usual thermistor formula is \( R_t = A \cdot 10^{(B/T) - C} \), where T is absolute temperature in degrees Kelvin (K = °C + 273), and A (ohms) and B (K) are nominally constant. B is often around 3,000, and A is a small fraction of an ohm. Values can be deduced from measurement at any two temperatures, but since they are only approximately constant, calculations are best restricted to interpolation only.

As the table shows, the linearity between calibration points is good, and it is acceptable over a larger range. It may be noted that, from Thévenin's theorem, the same value of Rs applies in a circuit using a constant current through Rs and R5 in parallel. Maximum thermistor power occurs when Rs = R5 and for Fig. 3 is 1.28/15.485, about 80mW. For beading device, in free air, would produce about 0.18°C self-heating. When using lower-resistance thermistors, the possibility of self-heating error should be borne in mind.

![Diagram](https://via.placeholder.com/150)

**Fig. 1.** In-line connection of delay unit between time-clock and load.

**Fig. 2.** Power supply section. The regulator may be 100 mA or 1 A type.

**Fig. 3.** Delay and thermometer circuits. Unless otherwise stated, diodes are 1N4148 or equivalent, and transistors general-purpose, such as BC548 (NPN) and BC558 (PNP).

**Fig. 4.** Counting-up: 4/4, jump to 64; 4/8, jump to 80. Numbers in circles are 425 pin numbers, circles below the direct connection of Sp to pin 4.

**Fig. 5.** Opto-isolator reset, for use when delay unit is independently powered. With this circuit emit components 100n, 10μF from Fig. 3.

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**HEARING-AID IN A CUP**

by David Ryder, Ph.D.

The table shows N values for various temperatures, relating to RS code 151-237 thermistor, which is a close-tolerance device (+0.2°C). Resistance Rt must be made up to within 1% from metal-film resistors. Other thermistors can be used by measuring them and calculating the appropriate R0 (see appendix). Setting-up is easier if test-resistances are made up to substitute for the thermistor at say 0°C, 10°C, and 20°C, and in the prototype these were built in using a four-way switch.
Low-power grid blanking

Electron-beam blanking at the first grid can involve much higher voltages than cathode blanking but is sometimes desirable. This circuit was designed for digitally-controlled grid blanking of a camera tube used for quantitative light measurements. The grid voltage (equal to V2) can be accurately controlled during the active picture line and transitions to and from the blanking potential are short, at about 200 and 300μs respectively, with no ringing when a Schottky t.t.i. input is used.

Because grid-leakage current is extremely low, the high voltages required can be achieved by switching the connections of a charged capacitor. When the input-signal goes high, T2 is turned off and T1 and T3 turn on so that the voltage over capacitor C, Vc, is the difference between the rail voltages, V+, V-. The output at g1 is held at the negative rail, which controls the beam current.

When the input goes high, T1 and T3 are turned off and T2 turned on, so that the more positive side of C is taken to V+, and the negative side consequently to the blanking potential, V_. V_, which is also 2V+. The droop in blanking potential caused by leakage through T3 is negligible in normal use. There is no droop in the beam-control voltage as T3 remains sufficiently conductive throughout the active line. The g1 lead must be kept well away from the target connection to avoid interference.

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Telephone-line interface

Conventional telephone-interface circuits use relays and/or transformers for loop detection and speech coupling. In this circuit, a 5V positive-voltage regulator is used to feed a constant current to the telephone line. The line current is set by R2, and the regulator output provides a logic signal that will "follow" dialling pulses from the telephone.

As this circuit provides unbalanced transmission to the telephone, it is only suitable for normal (intercom type) exchanges. A ring circuit could be provided by a third wire to the telephone. Acknowledgement to the Director of Research for permission to publish this information.

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Z80 memory mapping

R.a.m. sets for interrupt restart vectors and e.p.r.o.m. write protection are provided by this automatic memory map and switch for a Z80 microprocessor system. On power-up, or after a reset, a 2K-byte e.p.r.o.m. (2716) occupies addresses 0000 to 07FF and a 2K-byte r.a.m. in address mapped to F000-FFFF. After a reset, the Z80 will perform an op-code fetch from location 0000. The e.p.r.o.m. will be selected after MRQ is activated. The instruction at locations 0000 to 0002 is JP F003 and the circuit will automatically switch r.a.m. and e.p.r.o.m. locations after the third memory access. The next op-code fetch will occur at location F003, causing execution to continue from the next contiguous location in e.p.r.o.m. Locations 0000 to 07FF are now occupied by the 2K r.a.m. so it is possible to initialize and modify the interrupt restart vectors, hence providing a greater degree of flexibility.

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Testing p.r.b.s. generators

Readers experimenting with p.r.b.s generator may find this circuit useful for evaluating possible feedback configurations. Driven by an external clock at any speed up to a few hundred kHz, it gates clock-pulses to an external counter for exactly the duration of one complete sequence, maximal or otherwise, so that the final counts shows the number of steps in the sequence. The generator is preset so that the count begins almost immediately.

The shift-register shown has 5 effective stages and is negative-edge triggered (e.g. 4006’s); for a positive-edge triggered shift-register the inverted clock-signal is used.

When the system is at rest, both flip-flops are in the reset state and no clock-pulses occur at the output. Point A is low, so the auxiliary counter is held at zero and the input to the shift-register is held high. After a maximum of n clock-cycles all the stages of the shift-register will be in the high state, and the system ready to start.

The start button sets the start flip-flop on the next negative-going transition of the incoming clock-signal, contact-bounce has no effect. Point A goes high. This allows the generator to run normally, with its output (from stage n of the shift-register) controlling the auxiliary counter. When the generator output is high, the counter advances one count on each positive-going transition of the incoming clock-signal, when the generator output is low the counter is held at zero.

Once per complete sequence the generator output remains high for n consecutive clock-cycles; the counter then reaches the count of n causing point B to go high until the counter is reset (nominally a half clock-cycle later).

Because all stages of the shift-register were initially preset to the high state, the first signal at B occurs during the n'th clock-cycle from the start. This signal sets the gate flip-flop. This in turn allows clock-pulses to appear at the output, and also resets the start flip-flop while maintaining point A high so that the system continues to run. These conditions continue until the next signal appears at B exactly one sequence later, and resets the gate flip-flop; then the clock-pulses cease to appear at the output, point A goes low, the generator ceases to run, and, after a maximum of n clock-cycles, the system is back in the ready state.

Pressing the reset button will return the system to the ready state at any time.

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DESIGNING WITH MICROPROCESSORS 13

Clear-cut step-by-step procedures for the design and implementation of d.m.a. interfaces are described. Specifically, it is proved that in the case of action/status peripherals the interface reduces to two wires.

by D. Zissos* assisted by Glen Stone*

The block diagram of a d.m.a. system is shown in Fig. 1. The function and operation of the address decoder, the d.m.a. controller and the cycle-steal logic has been explained in the previous article (February, 1982). Briefly what happens is this: The programmer sends to the d.m.a. controller (by means of a/b instructions) three items of information specifying (i) the starting memory address, (ii) the size of the block, and (iii) the direction of transfer, followed by the 'go' command. On receipt of the 'go' command, the d.m.a. controller activates the peripheral interface by pulling enable signal E in Fig. 1 high (E = 1). When activated, the interface monitors the status signals of the peripheral, and requests a cycle steal when the peripheral is ready. When the microprocessor responds, the interface and the d.m.a. controller generate the appropriate command signals needed by the peripheral and the memory chip for the transfer of one item of information (usually a byte) between them. At the end of each cycle steal, the memory address is incremented/decremented, and the word count is decremented (n = n-1). This process continues until the word count reduces to zero (n = 0), at which time the interface is disabled and the end-of-transfer signal, e, is generated.

D.m.a. interfaces

The function of d.m.a. interfaces is to request the microprocessor to go on hold when the main memory is to be accessed, and to generate the appropriate signals needed by the peripheral when the memory becomes accessible. In the case of cycle-steal systems, as we have already seen, the hold request is generated each time the memory is to be accessed, and removed after a memory cycle is granted.

The block diagram of a suitable d.m.a. interface, assuming logic signals throughout, is shown in the shaded section of Fig. 2. It operates in the following manner:

When logic block 1 recognizes that the peripheral is ready to be accessed, it sets flip-flop 3 by pulling its clock terminal. Its output is ANDed with the enable signal E to produce the cycle request signal c. (Assume c = 1). When the requested memory cycle is granted, line h is pulled high and a pulse is generated on line k. Signal h being high, and E = 1, activates logic block 2, which responds by generating the appropriate command signals needed by the peripheral for accepting or receiving an item of information. Similarly, pulse k activates the d.m.a. controller, which initiates either a memory read or a memory write cycle. At the end of the memory cycle the microprocessor resumes normal activity, until the peripheral becomes ready, which causes logic block 1 to pulse the clock terminal of FF3. This pulls the cycle-steal line c high and sometime later a link between memory and logic block 1 is established for a memory cycle. The process repeats itself until the last item has been transferred between the peripheral and memory. At this time the d.m.a. controller generates end-of-transfer signal e, to inform the system that the requested block transfer has been completed. The system responds by turning signal E off; this disables the interface.

To prevent the word count from wrapping round, that is changing from all 0s to all 1s, after the last piece of information in our block has been transferred in or out of the main memory, it is necessary to disable the interface before the peripheral becomes ready. Because software responses invariably involve a time lag, depending on system activity at the time and on the level of priority assigned to the e flag, it cannot be used for this purpose. The most straightforward method in such a case is to use signal e in Fig. 3 of the previous article to disable the interface. Signal e, the reader will recall, changes to 1 at the end of the block transfer, that is when the word count becomes zero. Otherwise, the design and implementation of peripheral interfaces in d.m.a. systems, as indeed in all digital systems, is uncomplicated and is carried out using well-defined step-by-step procedures.

The two-wire interface

In the case of action/status devices and no external signals, signal e, is generated directly by the peripheral, thus eliminating the need for logic block 1 and FF3 in Fig. 2. This reduces the peripheral interface to logic block 2, as shown in Fig. 3.

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Now, to avoid possible problems resulting from peripherals being activated while data transfers take place, a peripheral will be activated when a cycle steal is terminated; that is, when the value of h changes from 1 to 0. Since action/stores peripherals are activated by pulling their action terminal high, it follows that

That is, logic block 2 reduces to a single inverter, as shown in Fig. 4.

The detailed circuit implementation of a d.m.a. system is shown in Fig. 5.

D.m.a. software
Because in d.m.a. systems transfers of data between a peripheral and the main memory take place, automatically, software is needed only to send initializing information to the d.m.a. controller in Fig. 1, and to clear the end-of-transfer signal, if it is implemented as an interrupt flag. The initializing information, as we have already explained, consists of the following items:

- the starting address,
- the block length,
- the direction of transfer, and
- the 'go' command.

It is transferred into the d.m.a. controller in the following manner. The programer loads the accumulator with the initial memory address and executes an Out instruction with address A1. This pulses the load terminal of the two counters, which transfers the accumulator contents (the initial memory address) into counter I. At the same time, because the two counters are connected in cascade, the contents of counter 1 are pushed into counter 2. The programmer then transfers into the accumulator the block length and executes the same Out instruction. This causes the memory address in counter 1 to be pushed into counter 2, and the value of the block length (held in the accumulator) to be loaded into counter 1.

LITERATURE RECEIVED

SE Labs have issued a new shortform catalogue on the company's range of instrumentation tape recorders. There are a large number of recorders for laboratory or field use with a variety of numbers of track and recording speeds up to 24000, as well as digital recorders. Data Recording Division, SE Labs (EMD) Ltd, Spit Road, Potters Bar, Hertfordshire W41 0TD.

The Micro Focus Newsletter has been produced to keep readers up to date with the latest COBOL computer language products and developments. COBOL is an increasing use in microcomputers and Micro Focus have announced a COBOL II which may be used on both mainframes and minis. The Newsletter is available free from Micro Focus, Sacsia Road, London NW8.

RS Catalogue. The latest edition of the catalogue from RS Components Ltd has 344 pages and includes a newsheet called Rapid Scan, which is running a competition to find out who is RS's longest standing customer. Anyone who can find an old catalogue, delivery note or invoice from RS (or RadioShack as they were then) could win a magnum of champagne. The catalogue lists as additions to its contracts over 75 items including data transmission cables, splashproof connectors, a bubble desk task for p.c.b.s., a front panel with keyboard and the p.c.b.s for a programmable timer. The catalogue is available for free from RS Components Ltd, PO Box 427, 13-19 Ewthew Street, London EC2P 2HA.

24-page catalogue of panel meters, multimeters and test equipment is available from Beckman-Geor, who are at 9 Torment Estates, Westcliff, Essex. WPPN 27EL.

A four-page catalogue of panel meters, multimeters and test equipment is available from Beckman-Geor, who are at 9 Torment Estates, Westcliff, Essex. WPPN 27EL.

The French company Radiant offer a short catalogue of microwave components, including transitions, couplers, attenuators, relays and mixers. Write to Microwave Components, Ltd, Instinctive Road, Farnborough, Hampshire.

A wide range of TMK testmeters including digital multimeters, clamp ammeters and industrial thermometers, is detailed in literature from Harris Electronics (London), 108 Gray's Inn Road, London WC1X 8AX.

The French company Radiant offer a short catalogue of microwave components, including transitions, couplers, attenuators, relays and mixers. Write to Microwave Components, Ltd, Instinctive Road, Farnborough, Hampshire.

The 1981/12 Colorado Video short form catalog describes a series of specialized video instruments, designed for CATV or telecommunication, computer video input and output, frame alignment and analysis. The UK agents are Anaplex Ltd, Pearl House, Bartholomew Street, Newbury, Berkshire RG1 4 SL.

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by J. H. Asbery, Ph.D., M.I.E.E.

The detector can also be used with other synthesizer circuits to eliminate one pole of the switching system. An ultrasonic signal is superimposed on the d.c. voltage of the resistor chain of the keyboard. When a key is pressed, this signal appears at the input of IC1, which switches on the modulators at a steady rate and switches them off at a steady rate where the key is released. Collector resistors R4 and R5 of TR1 and TR4 can be common to all generators and should be positioned close to the amplifier to avoid pick-up from the common earth wiring.

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Reference

As previously stated, hard discs have a thin coating of magnetic material and rotate at high speeds. Readers familiar with other magnetic recording systems will realize that ideally, the head should not be forced against, or at least touch, the recording medium. But because of the speeds at which the disc is moving, the fragility of the medium, a gap is essential. Therefore, the head is designed to "fly", on the layer of air on the rotating disc. Consequently, the head is of low mass, so the gap between head and disc can be kept constant over the whole surface of the disc and a small degree of warping can be compensated for. Figure 1 outlines the read/write head's structure.

The magnetic field is carried by the slider and consists of a permeable core with a coil wound round it. A paramagnetic barrier on the head core forces the flux out of the head onto the medium. Resistance of the magnetic circuit depends mainly on the air gap. The slider and the disc so the write flux is a function of the distance height of the head above the recording medium to about ten times that of the flying height.

Slippers. Current "state-of-the-art" slippers fly at less than 20 micro-inches (0.5 micron) above the disc. It is obvious that the lower the flying height, the more significant reading and writing becomes, but what isn't perhaps apparent is that the major design problem is making the slipper fly low enough. Lift rises rapidly as the separation distance so as to reduce as close to the disc, some of the lift has to be dumped. Early slippers had two small blades, as shown in Fig. 1a, which in Fig. 1b shows a third generation design, with a large longitudinal bleed groove, designed for flying heights of above 20 micro-inches. The second example, 2(c), is designed for use below 20 micro-inches and has substantial bleed grooves and vertical working surfaces. Although the surface of this slipper appears flat to the naked eye, it is actually formed to a high degree of accuracy in a compound curve.

Suspension. The slipper is mounted at the end of a rigid mechanical arm in the medium. The force with which the head is pushed toward the disc by the spring is equal to the lift of the ideal theoretical every time the data is a binary one. It can be seen from Fig. 2(a) that this approach is of no use in a single track system. If the clock occurs, it is not possible to reconstruct the clock.

by J. R. Watkins

As displayed with. As the slipper negotiates a warp it will pitch and roll, in addition to rising and falling, but it must be prevented from yawing. Downthrust is applied to the slipper at its aerodynamic centre by a spherical thrust button and the required degrees of freedom are provided by a flexural gurnal.

The shape of the head/cantilever and the spring compliance have a natural resonance which must be set away from expected warp frequencies. Some cantilevers are fitted with synthetic-rubber dampers to control unwanted resonances.

Other essentials of the cantilever are the head support ramp, which lifts the head clear of the disc as the positioner retracts, and some means for aligning the disc, which is not to align all of the heads to the same distance from the spindle at a given cylinder.

Handling and setting head assemblies requires care and skill; in some cases acid from a fingerprint is sufficient to etch the slipper surface and destroy its aerodynamic nature.

Encoding techniques

With the exception of some non-interchangeable disc drives, only one head is active at any time. A production tolerance of ±10 µm at the actual lateral position of the head gap and the ideal, and this dimension may be several wavelengths at the highest frequencies. As a result it is not generally possible to use parallel encoding in disc drives. This constraint largely defines the encoding techniques used.

As in all modern digital recording, the medium has a linear rate of magnetization, N-S and S-N. Devices have been made using the unmagnetized state, these must be considered obsolete. The write process consists of supplying sufficient current to almost saturate the medium first in one direction, then the other. No erase process is necessary, as writing the cylinder address or the reverse recording. Some heads do, however, have erase pulses, which are used to erase the track
tape.
tion, artificially advances transitions subject to delay on reading, and delays advanced transitions by taking a running sample (usually four) of data stored in decoding the patterns to generate different clock times in a tapped delay line. M.f.m. requires a running sample, so the two processes are sometimes combined in one circuit.

Recently, a different approach to high density recording has been developed. Central to this approach is that transitions are not permitted at successive active edges of the write clock. Figure 5(a) shows that the four combinations of any two data bits may be expressed as three-bit codes which do not contain successive 'one'. There are, however, four combinations of adjacent pairs of bits to violate the rule, Fig. 7(b). In these cases, the six bits are substituted by alternative bit patterns which must follow certain conditions: firstly, that the substitution contains no adjacent ones, secondly that the substitution ends in zero so that no subsequent data can violate the rule, and thirdly the position of the ones is chosen to generate transitions at sequential integer multiples of the write-clock period. Figure 7(c) shows that the highest density results from a data stream of 011111 and that this requires only six transitions for eight data bits. At maximum density, m.f.m. requires only one transition per bit, so the relative efficiency is 66% or 33% greater. Fig. 7(c) also shows that the lower density can be achieved by writing a scheme below the maximum, and that seven even steps exist in the periods between any two transitions. This evenness allows effective phase-locked noise rejection to be employed and the transition time of reading data pulses can be accurately predicted. In addition, precompensation is only required to the first peak detector output and so is the highest density, as at all lower densities the transitions are far enough apart to make peak-shift distortion insignificant. This recording technique is known as 2/3 (precompensation) and for good reasons. It is difficult to imagine a method which would achieve a significant improvement in efficiency over it. Encoding is performed by a p.r.o.m. which takes a running sample of data in the same way as m.f.m. Similarly, reading requires phase-locked circuits, with a further p.r.o.m. containing the reverse truth table to the encoding p.r.o.m.

Circuits

The same head is used for both reading and writing, and as stated, usually only one head is active at one time. The circuits involved in recording, writing and head selection come together at the read/write matrix where the flexible hard cables plug in. It can be seen from Fig. 8 that the centre-tapped heads are isolated by connecting the centre tap to a separate voltage, which reverse-blanks the matrix diodes. The centre tap of the selected head is made positive. When reading, a small current flows through both halves of the head coil, as the diodes are forward biased. Opposing currents in the head cancel, but read signals resulting from flux transitions on the disc can pass through the forward biased diodes to become differential waveforms on the matrix bus. During a write, the current from the write coil is alternately through the two halves of the head coil. Further isolation is necessary to prevent write-current voltages destroying the read amplifier inputs.

Write-current programming. The flying height changes of relative velocity which is governed by the track radius. It is possible to program the write current from the current cylinder-address register such that the write flux remains essentially constant, despite changes in flying height. The number of write-current steps is usually between two and eight across the working surface of the disc, although some drives dispense with write current programming altogether. In Fig. 9, the write current is generated by holding the base of a transistor at a temperature-compensated reference voltage and by selecting different emitter resistors with transistor switches. As the current source is usually at about -40V, the switches are fed from the drive logic through level shifters. The write current is directed through the head by a pair of transistors in series with the current generator, which are driven in a complementary fashion by a bistable. The purpose of write

Figure 4 also introduces the concept of the 'bit cell', i.e. the time taken to record one bit. In a simple encoding system, there must be a minimum time period per bit cell to carry the clock. Figure 4(b) shows a popular encoding technique, where each bit cell begins with a clock transition, and may or may not contain a further transition, depending on whether the data bit is a one or a zero. As the presence of the second transition doubles the recording frequency, the technique is known variously as f.m. or double-frequency recording. Data separation can be very simple, provided the signal-to-noise ratio is adequately high. The signal-to-noise ratio is determined by any intrinsically medium noise and the electromagnetic environment, but also by the accuracy of the transducer. Consider for example, the example of Fig. 4(a). Originally, data is written along path A, but positioner inaccuracy means that new data is being written along path B. Subsequently a read may take place along path C, where it will be seen that the read signal is degraded by the previous recording. The solution to this problem is to incorporate two erase gaps in the head, which erase a small area either side of the new data after writing. In Fig. 5(b) it can be seen that the peak erase pulse has a margin of unidirectionally magnetized oxide. The process is called 'tunnel erase' or 'side erase', and is generally employed on drives with relatively simple positioners. Such devices usually have low recording densities and accordingly a generous flying height, giving them the advantage that they can be used reliably in environments that would normally be considered unsuitable.

F.m. is easy to decode, but it is also fairly extravagant with transitions. Any encoding method in which the number of transitions per data bit can be reduced has to be an improvement, because for a given flying height, and hence a given minimum wavelength, a greater data density is possible.

In the next generation of read electronics, it is possible to relax constraints on the clock information through phase-locked-loop techniques. With this approach, it is acceptable for a bit cell to contain either clock information or data but both are not necessary. The read clock comes from a p.i.o. which continues in the absence of a transition at clock time, and which corrects its own frequency by continuously comparing its own phase with that of data or clock transitions. In Fig. 4(c) it can be seen that the write current is reversed at the bit-cell centre for a one, and that the problem of successive ones is handled by reversing the write current at the bit-cell boundary. It is interesting to compare the number of transitions required for the example of Fig. 4(b). On reading the data, the p.i.o. can be used to open a 'time window' at the centre of the bit cell, so that only transitions corresponding to a binary one can pass through. Obviously, the system only works if the p.i.o. is synchronized, so a series of zeros, or preamble, is fed before each block to allow the loop to lock. A unique synchronizing pattern de-locates where actual data begins. This phase-locked-data-recovery technique is used with modified-frequency modulation encoding (or Miller encoding) and allows the arrival time of read pulses to be predicted, and therefore noise pulses to be rejected. This means that a suitable s-t-r ratio can be tolerated than with f.m. encoding, allowing tunnel erase to be dispensed with. In any case, drives employing the m.f.m. technique are likely to have more accurate positioners.

Where f.m. requires signal-to-noise ratio, m.f.m. requires minimum phase error, if the phase-locked data recovery is not to be upset. In Fig. 6, a head is depicted reading closely packed transitions. Owing to the spacing between the head and the medium, pulses generated tend to run into one another such that the waveform peak positions do not correspond to the actual position of the transitions. The phenomenon is referred to as peak-shift distortion, and is overcome by introducing an adjusting time changes during the write process. This technique, presented by a read/write head produces a 'time window' at the bit-cell centre through which only data '1' pulses are read. The presence of a data '1' causes an extra transition at the bit-cell centre. In m.f.m. recording, shown at (d), a data '1' causes a transition at the bit-cell centre but the only other transitions are at the bit-cell boundaries between successive zeros. Both types of transition are used to synchronize a p.i.o, which opens a 'data window' at the bit-cell centre through which only data '1' pulses are read.

In Fig. 6 (a), track B has been written over track A, but through wide tolerances on the position repeatability, some of the original data remains at the edge of path B. If the new data is read while the head travels the same path as it did when the original data was written, remaining original data will be read together with the new data, hence the signal-to-noise ratio will be degraded. At (a), the problem is solved by including two erase heads, one on each side of the write head, so that whenever data is written, any original data at either side of the track will be erased.
encoding is to decide at what time to clock the bistable so that a transition is written by the current reversal.

Reading. When not actually writing, the write-current generator is turned off and the write-isolation diodes are reverse biased. The read isolation gate is enabled, allowing the differential read signal into the read d-e amplifier. This amplifier raises the amplitude of the read signal to a constant level suitable for data recovery, and filters out unwanted signals. To this end the linear amplifier often contains both bandpass filters and an a-c loop. In some cases, the linear amplifier's input and the a-c capacitor are shorted during the address mark to stabilize the gain in the shortest possible time after entering a block. The address mark is a short section of the track preceding a data block and contains no transitions. A-c squelch is relevant as the block is entered, and the linear-amplifier gain reduces from maximum using the fast attack slope of the forward-based signal rectifier.

The constant-amplitude read signal now passes to the peak detector, as the position of the signal peak corresponds to the position of the transitions on the disc. In Fig. 10(c) an amplitude waveform is compared with a delayed version of itself. The comparator changes state at the signal peak. A differential version of this type of peak detector is shown in Fig. 10(e). The principle holds equally well if one signal is phase advanced, and thus the delay is sometimes substituted by the RC network shown.

The detected signal is fed to an appropriate data separator, which splits the signal into data and clock information to pass to the deserializer, which recreates data words.

To be continued...
Fig. 4. brought high (5), signaling that it is ready for the next byte of information. In Fig. 7, RXST is inverted and connected to RXRDY, in which case data is transferred at a data rate determined by the bus handshake.

The Drive Bus Output (DBO) signal is low when data is being transferred from the AD7555 analog converter to the IEEE bus, and high when information is being sent to the data acquisition system. In Fig. 6, the signal is used to enable (or disable) a set of transceivers.

TAD (Talk-Addressed) and LAD (Listen-Addressed) are active low when the device is addressed to talk or listen.

SST (Status Select) is used to select either data or status information via a data selector (74157). The STS (Status Status) and STRDY (Status Ready) signals operate similar to the TXST and TXRDY signals when sending status information during a serial poll. STRDY can be formed from an inversion of STS.

RTL (Return to Local Input) is tied high in this application, since the device is operating only in remote control.

CLR issues a negative pulse when the device receives a Device Clear command. This will reset all functions within the device.

TRG (Trigger output) issues a negative pulse when the device receives a DT (Device Trigger) command. It is not used in this application. The IST (Instrument Status Input) is used in parallel poll enable.

For more information on the above signals see the Fairchild 96LS488 data sheet.

Data acquisition system

Figure 7 shows the complete circuit diagram of the data acquisition system. A brief review of each i.e. should help to understand its operation before the more complex timing of the system is discussed. Circuits IC1,2 are quad interface interrupt. This occurs when a conversion is complete.

Data (Status) is held low when data is being transferred to the IEEE bus, or high if status information is being transferred during a serial poll. In this application, it is used to select either data or status information via a data selector (74157).

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Data (Status) is held low when data is being transferred to the IEEE bus, or high if status information is being transferred during a serial poll. In this application, it is used to select either data or status information via a data selector (74157).

The STS (Status Status) and STRDY (Status Ready) signals operate similar to the TXST and TXRDY signals when sending status information during a serial poll. STRDY can be formed from an inversion of STS.

RTL (Return to Local Input) is tied high in this application, since the device is operating only in remote control.

CLR issues a negative pulse when the device receives a Device Clear command. This will reset all functions within the device.

TRG (Trigger output) issues a negative pulse when the device receives a DT (Device Trigger) command. It is not used in this application. The IST (Instrument Status Input) is used in parallel poll enable.

For more information on the above signals see the Fairchild 96LS488 data sheet.

Fig. 3. Simplified data transfer sequence.

Fig. 4. brought high (5), signaling that it is ready for the next byte of information. In Fig. 7, RXST is inverted and connected to RXRDY, in which case data is transferred at a data rate determined by the bus handshake.

The Drive Bus Output (DBO) signal is low when data is being transferred from the AD7555 analog converter to the IEEE bus, and high when information is being sent to the data acquisition system. In Fig. 6, the signal is used to enable (or disable) a set of transceivers.

TAD (Talk-Addressed) and LAD (Listen-Addressed) are active low when the device is addressed to talk or listen.

SST (Status Select) is used to select either data or status information via a data selector (74157). The STS (Status Status) and STRDY (Status Ready) signals operate similar to the TXST and TXRDY signals when sending status information during a serial poll. STRDY can be formed from an inversion of STS.

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For more information on the above signals see the Fairchild 96LS488 data sheet.
transceivers (MC3441) and are designed to meet the IEEE standard 488.1975. The data direction is controlled by the DRI output of the 96LS488 (IC). When it is
low, data is transferred to the D2 and
transferred from the bus when DRI is high. Switches S1-S5 are used to select the address of the device. As an example-
For an address of 16, S1 is open, while S2, S3, S4, and S5 are closed. (Address is
10000 = 16). Switches S6-S9 are used to select the operating mode of the 96LS488
Fairchild data sheet gives more in-
formation on this). For a talker/listener on
speed, M0 and M1 are high, and M2 and M3 are low (ie, S6 and S7 are open).
Since all information is transmitted in
parallel ASCII code, it is necessary to
de-code this to binary. The 6331 (IC2)
is a 32 x 8-bit r.o.m. which is used for
this purpose, whose outputs are shown in Table 1. The address latch, IC7 (74C175),
holds the address of the selected channel, its output being connected to the input of
IC4 (AD7506), a 16 channel multiplexer,
which in turn selects the appropriate an-
alog signal to the a-d converter subsystem (AD5755). On completion of a conversion, the b.c.d. data is held in internal latches, and can be accessed by control of the DMC pin. The
IEEE transmit handshake signals are used to
access this information during a read-back cycle. A data selector IC8 (756157) and
45 digits and a carriage return to the 96LS488. When DS is high, b.c.d. data
from the a-d converter is selected, and
when DS is low a CR code is selected.

The ferrite, m.o.s. t.i.l. inverter (IC9) produces the 4.096 MHz clock with the
crystal, whilst IC7 (74C93), a 4-bit binary
counter, divides this by four, producing a
1.024 MHz clock for the AD5755.
The two multiplexers/selectors (IC23)
used to transfer either data or status
information to the 96LS488. When DS is
low, data information is selected (TS-T5),
and when high the status byte is sent.
The concluding article will continue this
circuit description and include a program for scanning 16 channels.

For dividing in the range 16c:N=256,
whether or not N is a prime number is
important. If N is not prime, N = N1 N2
and the divider can be made up using
two programmable divide by 1 to 16 circuits
described in the previous article. These
may be connected either asynchronously
or synchronously, the latter method being
the fastest. To divide synchronously it is
necessary to enable the 742163 inputs as
shown in Fig. 9. To divide asynchronously,
the output of the divide-by-N1 circuit
has to be connected to the input of the

by Gerard Girolami

and Philippe Bamberger

SYMMETRICAL-OUTPUT DIVIDERS

Expanding on February’s article, the author first shows how further hexadecades may be added to the previously described binary-programmable counter. A basic b.c.d.-programmable counter follows and to conclude, details of how to add further
decades. These circuits are designed to accept and provide equal mark-to-space ratio
digital signals, and are programmable in integer steps. As frequency-dependent
components are not used, the speed of each circuit is only limited by the speeds of the
logic devices used.

that used for the 1-to-16 programmable counter except that the relationships in equations
and (3) given in the previous article must be changed to force the counter to ‘oscillate’ around the transi-
nion points at counts 127 and 128. The new equations are:

1. \[ L + D = 255 - 2^N \] (4)
2. \[ D - E = 127 \] if \( D \) is even
3. \[ D - ( 2^N - 1) = 127 \] if \( D \) is odd.

These relationships can again be imple-
mented using two binary adders as shown in Fig. 10.

As shown previously, it is possible to find the logic relationships between input and
load data as follows,

\[ L_0 = L_1 + L_2 \]

and so forth up to

\[ L_0 = (L_1 + L_2 + L_3 + L_4) \]

\[ L_0 = 0 \]

\[ D - L \]

B.c.d. programmable counters

If division ratios from one to nine only are required, the previously described binary-
programmable circuit may be used. If, however, a zero is to be inserted anywhere in a
decade counter, and the maximum divi-
sor range of one to ten is required, the
counter is able to ‘oscillate’ at the 4.5-
transition, rather than at the 7.8 transition as was the case with the binary-program-

This means that as Q0 is used as the output, the signal obtained will
not be square. In fact, if the dividing ratio is from 1 to 6, there will be no output
at all. It is easy to get round this problem by producing a logic 0 for the divided
out and logic 1 for the remainder, but this creates some problems—
more circuits are required

— even with a synchronous counter, it is difficult to predict the output, so the
clock will have to latch the output

— the maximum operating frequency is
lowered.

So, division ratios from one to nine, it is more practical to use a binary-counter
circuit. But the decade counter can be used to advantage if division ratios up to 100, or
even greater, are required. The following describes such dividers for ratios 1/2<sup>n</sup>≤100, and further expansion. For ratios 1/2<sup>n</sup>≤100, two dividers are connected synchronously and are made to 'oscillate' around a given transition (at p to p+1). It should be obvious from the previous paragraph that a binary counter will still have to be used for the most-significant decade (m.s.d.).

If the output obtained is to be square, as it is to be free to choose a division ratio from 1 to 100, it is necessary to use the transition between counts 79 and 80 (or 799 and 800 if three decades are used) as the starting point.  

### Table 1: Diverter, load and detect (L, D) and \( T \) for the b.c.d. programmable counter. This table is not given in full as it is obvious how omitted values are derived from the values given.

<table>
<thead>
<tr>
<th>Divisor</th>
<th>Load</th>
<th>Detect</th>
<th>( T )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>75</td>
<td>70</td>
<td>89</td>
</tr>
<tr>
<td>2</td>
<td>79</td>
<td>74</td>
<td>85</td>
</tr>
<tr>
<td>3</td>
<td>78</td>
<td>74</td>
<td>85</td>
</tr>
<tr>
<td>4</td>
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<td>40</td>
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</tr>
<tr>
<td>59</td>
<td>30</td>
<td>123</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>63</td>
<td>63</td>
<td>129</td>
</tr>
<tr>
<td>30</td>
<td>30</td>
<td>129</td>
<td></td>
</tr>
</tbody>
</table>

### Bibliography
- J. L. Huertas, Square-wave frequency divider provides symmetrical output for odd divisors. Electronic Design, 21 September 1975, p.100.

**ASCII KEYBOARD TESTER**

A time-saving method for detecting faulty keys or data lines. Traditionally keyboards have been tested by using a voltmeter or an oscilloscope in conjunction with a table of ASCII codes. This takes a long time and can be prone to error. The tester described here can detect faults quickly and easily.

**by Waleed Habib Abdullah**

---

*WIRELESS WORLD APRIL 1982*
Figure 1 shows a block diagram of the tester. The ASCII code of each key is stored in an e.p.r.o.m. which holds an "image" of the keyboard. When a key is pressed, the coded output may be compared with the stored code from the memory. Any mismatch will cause i.e.d. indicators to light. A counter is used to address the memory and is incremented by the keystroke stroke from the keyboard. Each time a key is pressed, the counter increments to the next address. Thus the keys must be tested in a set sequence governed by the order that they are programmed into the e.p.r.o.m. The full circuit is shown in Fig. 2. There is an up/down switch to reverse the counter, switches to set a specific address in the memory, a counter disable switch, 'reset' and 'key test' pushbuttons.

With the counter enabled and reset and switched to the 'up' mode, it is possible to press all the keys in sequence to check for errors. If no i.e.d. is lit, then the keyboard has no fault. If a i.e.d. should light then the corresponding bit can be tested inside the keyboard. It is possible to back-track and retest a key by reversing the sequence with the up/down switch. A fault may come from an individual key or from a data line. In the latter case, the same i.e.d. will remain lit when a number of keys are tested. To test a specific key the counter is disabled and the address of the key is entered on the switches. Pushing the key-test button will effect the comparison. Alternatively, one location in the memory (for example address 00) could be left vacant. Then with the counter set to that address, and disabled, the pressing of any key will cause the code coming from that key to be displayed on the i.e.d.s.

**Electrometer**

Voltage, current, resistance and charge functions are included in Keithley's model 614 electrometer. On the three measuring ranges for voltage, current, resistance and capacitance, the d.c. ranges are from 10µV to 100nV, from 10µA to 10µA, from 100kΩ to 10MΩ and from 1µF to 100µF. The a.c. range is 10µV to 100nV. The d.c. ranges have a resolution of 10µV and the maximum possible current reading is 2mA. Less than 20µVpp is present over the terminals on all current ranges. Resistance up to 200GΩ may be measured, also in nine ranges and resistance on the lowest range is 1Ω. Three other ranges are used for charge measurements down to around 100pC; on the lowest range and up to 20nC on the highest. Outputs are provided for a chart recorder and for guarding when making voltage and current measurements. A rechargeable lead-acid battery is included. Keithley Instruments Ltd, 1 Botham Way, Reading, Berks RG2 6NL.

**Waveform Recorder**

Digital waveform recorders are a new venture for Hewlett Packard but with their past experience in test and measuring instruments they have been able to jump in at the deep end. The HPI140 is a so-called 'universal' waveform recorder, that is, it can be used on its own or under the control of a computer. A 10mA n-o-d. converter providing sampling rates up to 2MHz and a 16K-by-10-bit memory that can be divided into a maximum of 32 segments from part of the system. Digital triggering is used to trigger times before or after the event, and trigger voltages, may be set and read accurately. One of the functions of two adjustable cursors is to pin-point a section of a waveform for vertical and/or horizontal zoom; these cursors may also be used to set trigger points. The front panel is, of course, designed ergonomically but nevertheless holds some 50 push buttons and one multi-purpose knob. With this in mind, up to four front-panel settings may be stored and recalled at will. All the front panel controls, and data io, are accessible through the HP-interface bus and 16-bit parallel d.m.a. (direct memory access) at transfer rates of up to 320 words per second. Hewlett Packard Ltd, 306-314 Kings Road, Reading, Berks RG1 4ES. WW101

**Tools**

This company has a wide range of tools and has recently introduced two kits, in wallets with zip, for routine servicing. The more elaborate of these contains 25 tools, including a miniature soldering iron, de-soldering braid, solder, pliers, screwdrivers, a hairpin, an i.e.d. extraction tool, scissors, a wire stripper and a range of screwdrivers and adjusting tools. Seven tools are contained in the smaller kit, pliers, side-cutters, tweezers and four screwdrivers. The former, the 'computer-service wallet, sells at £19.50 including v.a.t. and postage, and the latter, the 'industrial wallet', at £13.50, also includes Toolcool Ltd, Parkwood Industrial Estate, Sutton Road, Maidstone, Kent ME15 9LZ.

**Wireless World**

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**P PRODUCTS**

**V的产品**

**Waveform Recorder**

数字波形记录器是Hewlett Packard的新产品，但凭借其过去的测试和测量仪器经验，他们已经能够迅速进入这一领域。HPI140是一个所谓的"通用"波形记录器，这意味着它可以单独使用，也可以在计算机的控制下使用。一个10mA n-o-d.转换器提供采样率高达2MHz，16K-by-10-bit的内存可以被分成最多32个部分。数字触发器用于在事件之前或之后触发，并且触发电压可以设置和读取准确地。该功能有两个可调光标，用于垂直或水平缩放；这些光标也可以用于设置触发点。前面板的设计当然以人为本，但仍然保留了50个推钮和一个多功能旋钮。考虑到这一点，最多可以存储和调用四个前面板设置。前面板的控制和数据输入输出都通过HP总线访问和16位并行d.m.a.（直接内存访问）进行传输，传输率为每秒320字。Hewlett Packard Ltd, 306-314 Kings Road, Reading, Berks RG1 4ES. WW101

**Tools**

此公司拥有广泛的产品，最近还引进了两个工具套装，装在拉链钱包中，用于常规维修。更复杂的套装包含25个工具，包括微型烙铁、防锡剂、镊子、螺丝刀等，还包括工具拔出器、剪刀和一套螺丝刀。前者，"计算机维修包"，售价为19.50英镑（含增值税和邮费），而后者，"工业包"售价为13.50英镑，还包括Toolcool Ltd, Parkwood Industrial Estate, Sutton Road, Maidstone, Kent ME15 9LZ.

**Wireless World**

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NEW PRODUCTS

118 are low-pass filters, the first with a cut-off frequency of 3.4kHz and the second (suffix A) with a cut-off frequency of 1.8kHz. Under the latter version, the upper part of the voice-frequency channel is left free to carry data. Lastly is the 119 high-pass filter with a cut-off frequency of 300Hz and an upper limit of 5kHz. Supply rails between 2.5V and 18V are required for these modules. Bazz and Stroud, Melrose House, 4-6 Saddle Row, London W1X 1AF. WW395

ANTENNAE FOR MOBILE RADIO
A Swedish company, Alligan Ansa AB, has produced two antenna, one for the aerostatic and land-mobile distress frequencies of 121.5 and 243MHz, and the other as omnidirectional broadcast type for transmit and receive in the range 225 to 6000MHz. The first, called simply type 4104 (shown in

photos) operates on both distress frequencies simultaneously and can be used in base stations, on mobile-radio units and ships, or on board aircraft travelling at less than 220miles/h. The second, type 477, is a base-station antenna covering the 225 to 4000MHz frequency range without tuning. In the middle of this range, the antenna's gain is 4.8dB. The maximum average transmitting power is 1.5kW. Alligan Antenna AB, Box 500, 5-184 Oskarshamn, Sweden. WW306

MODULAR ORGAN KIT
A "budget-priced" electronic organ with features only previously available on more expensive instruments is claimed for the Werts Comet. Installed non-exclusively in the UK from Germany by Aura Sounds in kit form as well as in transportable and spinet versions, it can be bought in stages, the basic organ comprising four packs retailing £1293. Further packs include auto- accompany, registration memory/piano, and string/pizzicato facilities, bringing price to about £1900 against a factory built price of £3,600. Send in your keyboards — up to four can be connected with sections of the organs assigned to them — over £128 in kit form. The makers claim substantial "recreating" and interesting tonal colours including synthesizer effects and guine voices as well as the more-traditional drawbar and orchestral sounds. How far the claim to realism is justified is obviously open to question, especially with auto-accompany, but it seems much the best at simulating pipe organs. In addition to features now common to electronic organs and synthesizers that rely on voltage-controlled filters and amplifiers, this microprocessor design also has a program memory for 20 registrations. A key memory can play background chords after notes are released. A digital transporter can also pitch the organ in any key so that tuning is not required. Aura Sounds Ltd, 17 Upper Charter Avenue, Bemerton, Yorks. WW307

GENERAL PURPOSE ROBOTS
Hydraulically driven robot arms which can be controlled either manually or by computer are manufactured by Powertran Cybernetics for industrial, educational or home use. Complete systems range in price from around £500 to £800. Send in your keyboards — up to four can be connected with sections of the organs assigned to them — over £128 in kit form. The makers claim substantial "recreating" and interesting tonal colours including synthesizer effects and guine voices as well as the more-traditional drawbar and orchestral sounds. How far the claim to realism is justified is obviously open to question, especially with auto-accompany, but it seems much the best at simulating pipe organs. In addition to features now common to electronic organs and synthesizers that rely on voltage-controlled filters and amplifiers, this microprocessor design also has a program memory for 20 registrations. A key memory can play background chords after notes are released. A digital transporter can also pitch the organ in any key so that tuning is not required. Aura Sounds Ltd, 17 Upper Charter Avenue, Bemerton, Yorks. WW307

CABLE SIMULATOR
Characteristics are important in digital communication systems, especially when p.c.m. regeneration are concerned. To reduce the amount of floor space often required for testing such designs, Wandel and Goltermann have introduced the PKM-1 for simulating cables with conductors between 0.6 and 4.4mm diameter. Cable attenuation is displayed on a digital readout and adjusted by means of two potentiometers in range of 1dB at a frequency of 1MHz. Both balanced and unbalanced inputs and outputs are provided and a version of the PKM-1 with a 77kHz reference frequency can be supplied. A price of £2000 to £20000 level meter for measurements on voice channels in local and remote networks has also been recently introduced by the same company. This meter has an analogue dial readout, a digital frequency display and a built-in generator. Wandel & Goltermann GmbH & Co, Pforststr 5, Mülheim, 5, D-47141 Erkrun, P. R. Germany. WW309

Professional readers are invited to request further details on items featured here by entering the appropriate WW reference number on the reverse reply-paid card.

CW AND RTTY TERMINAL
A communication terminal for encoding/decoding Morse or Burst is manufactured by Polemark Ltd with built-in display, keyboard and real-time clock. The Microcan is a portable unit, microprocessor controlled, and has a 2KB byte r.a.m. and 4KB r.o.m. part of which contains some frequently used abbreviations and test text which may be called using simple key commands. Both modulator and demodulator are incorporated for c.w., i.f.a.k. and t.a.k. (audio-frequency shift keying). On receive, speed tracking is automatic and three fixed speed may be set when transmitting and both transmit and receive speeds are displayed on the screen. Receive and transmit may be carried out simultaneously. The terminal is packed so that it may be conveyed to a location and third fixed speed may be set by pressing a button on the side, and the output of the speaker may be connected to a terminal.
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Initially, you would be involved in a 9-12 month familiarisation period by a rotational attachment to our four maintenance areas and the Projects Department.

After successful training you would be employed on the maintenance of a wide range of broadcast equipment in our Central London Studios near Oxford Circus, from which the ITN national news programmes are networked.

Successful applicants will join ITN in early September, 1982. Starting salaries will lie within the range of £5,120 (at 18) rising to £6,427 at age 20.

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86 Wall Street
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The successful candidate should be a Member of the Chartered Institution of Building Services or a Member of the Institution of Mechanical Services and should also be a Member of the Institution of Electrical Engineers.

Applicants should provide full details of the candidate and the County Council will be pleased to receive applications from women and disabled people. Details of applications will be treated in confidence.

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Further information and application form available from: Dr. J. K. Fullilove, Chairman, Department of Electrical Engineering, Science Research Laboratories, University of Essex, Wivenhoe Park, Colchester CO4 3SQ.

GCHQ

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- Microcomputer Systems (embedded microcomputer applications, microprogramming, architectural)
- Microwave and Millimetre Wave Propagation (scattering from precipitation particles, space frame reverberation)
- Digital Communications (detectors, noise processes, signal design, switching)
- Picture Coding and Processing (data reduction, adaptive filtering and coding, feature extraction)
- Satellite Communication Systems (business systems, protocols and video services, intermodulation studies)
- Telecommunications Switching Systems and Software (computer control, software production, tables and viewers)
- Visual Displays and Television Engineering (computer graphic input systems, stereo and colour displays)

Further information and application form available from: Dr. J. K. Fullilove, Chairman, Department of Electrical Engineering, Science Research Laboratories, University of Essex, Wivenhoe Park, Colchester CO4 3SQ.

Appointments

Technicians in Communications

GCHQ

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