

PRACTICAL

ELECTRONICS ^{60B}

FEBRUARY 1984

90p

Computer Terminal

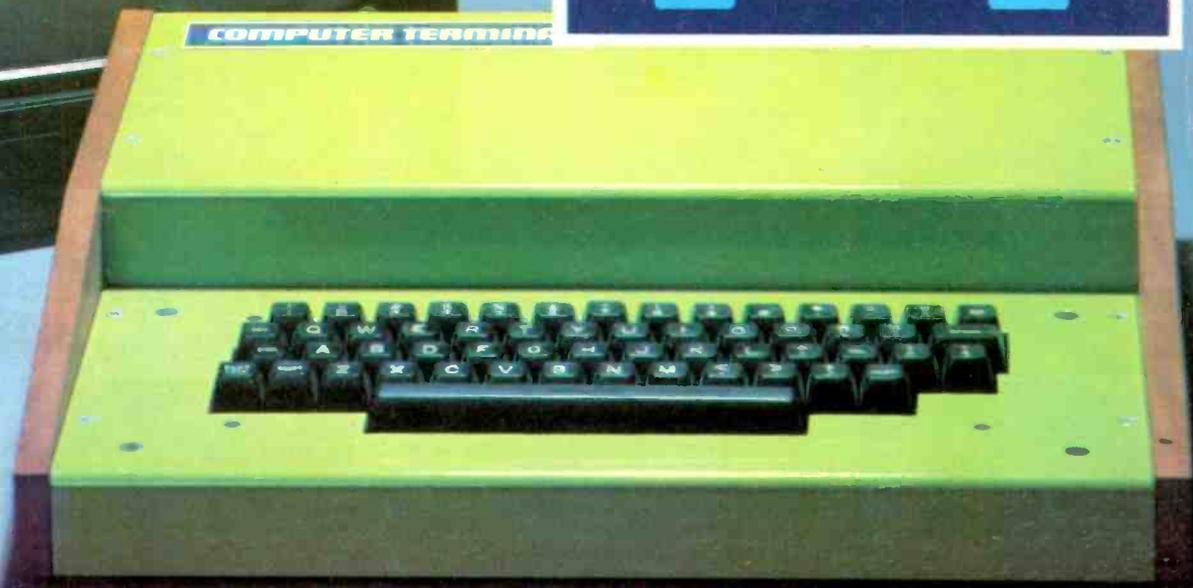


Plus...

**TEMPERATURE
CONTROLLER**



and
CLOCK TIMER



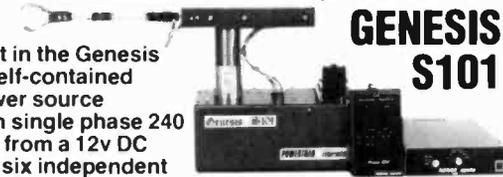
Buyer's Guide: MONITORS FOR HOME COMPUTERS

Low-price robots from POWERTRAN

— hydraulically powered
— microprocessor controlled

The UK-designed and manufactured range of Genesis general purpose robots provides a first-rate introduction to robotics for both education and industry. With prices from as low as £425, even the home enthusiast can aspire to his or her own robot.

Each robot in the Genesis range has a self-contained hydraulic power source operated from single phase 240 or 120v AC or from a 12v DC supply. Up to six independent axes are capable of simultaneous operation and all except the grip axis have sensing devices fitted to provide positional control by a closed loop system based on a dedicated microprocessor. Movement sequences can be programmed by means of a hand-held controller or the systems can be interfaced with an external computer via a standard RS232C link.



GENESIS S101



GENESIS P101

The top-of-the-range P102 has dual speed control, enhanced memory and double acting cylinders for increased torque on the wrist and arm joints. There is position interrogation via the RS232C interface, increasing the versatility of computer control and inputs are provided for machine tool interfacing.

All Genesis robots are available either ready-built or in kit form. The latter provides not only extra economy but also valuable additional training as an assembly project.



GENESIS P102



HEBOT II Turtle-type robot

For under £100, Hebot II takes programming off the VDU and into the real world. Each wheel is independently controlled by a computer, enabling the robot to perform an almost infinite number of moves. It has blinking eyes, a two-tone bleep and a solenoid-operated pen to chart its moves. Touch sensors coupled to its shell return data about its environment to the computer enabling evasive or exploratory action to be calculated.

The robot connects directly to an I/O port or, via the interface board, to the expansion bus of a ZX81 or other microcomputer.

HEBOT II

Weight 1.8kg
complete kit with assembly instructions £85
Interface board kit £10

MICROGRASP



A real, programmable robot for under £200! Micrograsp has an articulated arm jointed at shoulder, elbow and wrist positions. The entire arm rotates about its base and there is a motor driven gripper. All five axes are motor driven and four of these are servo controlled giving positive positioning. The robot can be controlled by any microcomputer with an expansion bus — the Sinclair ZX81 being particularly suitable.

MICROGRASP

Weight 8.7kg, max. lifting capacity 100g
Robot kit with power supply £145.00

Universal computer interface board kit £48.50
23 way edge connector £2.50
AX81 peripheral /RAM pack splitter board £3.00

GENESIS S101

Weight 29kg, max. lifting capacity 1.5kg
4-axis model (kit form) £425

5-axis model (kit form) £475
5-axis complete system (kit form) £737

GENESIS P101

Weight 34kg, max lifting capacity 1.8kg

6-axis model (kit form) £675
6-axis complete system (kit form) £945

GENESIS P102

Weight 36kg, max lifting capacity 2kg
6-axis system (kit form) £1175.00

Powertran Correx microcomputer self-assembly kit £295.00



POWERTRAN cybernetics Ltd.

PORTWAY INDUSTRIAL ESTATE, ANDOVER, HANTS SP10 3PE. TEL (0264) 64455

ALL PRICES ARE EXCLUSIVE OF VAT — ALLOW 21 DAYS FOR DELIVERY.



PRACTICAL ELECTRONICS

VOLUME 20

No. 2

FEBRUARY 1984

CONSTRUCTIONAL PROJECTS

COMPUTER TERMINAL Part 1 by Ray Pinchin	16
Remote VDU/keyboard terminal	
CLOCK TIMER by T. J. Johnson	24
Four digit clock with output relay for switching 10A at 240V	
STARDESK Part Two by Peter Newbury	32
Construction details	
TEMPERATURE CONTROLLER by T. J. Johnson	50
Provides a temperature controlled output for switching mains appliances	

GENERAL FEATURES

SEMICONDUCTOR CIRCUITS by Tom Gaskell BA(Hons)	28
LED bargraph drivers (UB..B Series)	
MONITORS FOR HOME COMPUTERS by M. Tooley BA and D. Whitfield MA MSc CEng MIEE	44
Specifications explained — buyers guide	
VERNON TRENT AT LARGE	56
INTRODUCTION TO DIGITAL ELECTRONICS by M. Tooley BA and D. Whitfield MA MSc CEng MIEE	60
Part 5 of our electronics course	
MICRO-BUS	67
A monthly focus on micro's for the home constructor	

NEWS AND COMMENT

EDITORIAL	13
NEWS AND MARKET PLACE	14
Including Countdown and Silicon News Corner	
BAZAAR	21, 40, 68
Free readers' advertisements	
INDUSTRY NOTEBOOK by Nexus	22
News and views on the electronics industry	
SPECIAL OFFER-CASSETTES	30
PATENTS REVIEW	43
Improved stereo TV	
SPACEWATCH by Frank W. Hyde	59
SERC scientists 'weigh' a black hole	

**DUE TO LACK OF SPACE PART FIVE OF EXPANDING THE VIC 20 AND
MICRO-FILE HAVE BEEN HELD OVER TILL NEXT MONTH**

OUR MARCH ISSUE WILL BE ON SALE FRIDAY, FEBRUARY 3rd, 1984
(for details of contents see page 31)

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WATFORD ELECTRONICS

33, CARDIFF ROAD, WATFORD, HERTS WD1 8ED, ENGLAND

Tel. Watford (0923) 40588. Telex: 8956095 WAELEC

ORDERS NORMALLY DESPATCHED BY RETURN OF POST

ALL DEVICES BRAND NEW, FULL SPEC. AND FULLY GUARANTEED. SEND CASH, P.O.'s OR CHEQUE WITH ORDER. GOVERNMENT AND EDUCATIONAL INSTITUTIONS OFFICIAL ORDERS ACCEPTED (ACCESS ORDERS BY TELEPHONE 0923-50234). TRADE AND EXPORT INQUIRY WELCOME. P & P ADD 60p TO ALL CASH ORDERS. OVERSEAS POSTAGE AT COST. PRICES SUBJECT TO CHANGE.

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POLYESTER RADIAL LEAD CAPACITORS: 250V; 10n, 20n, 15n, 22n, 27n 6p; 33n, 47n, 68n, 100n 8p; 350n, 220n 10p; 330n, 470n 15p; 680n 18p; 1µ 23p; 1µ 40p; 2µ 46p.

ELECTROLYTIC CAPACITORS (Values in µF): 500V: 10µF 52p; 47 78p; 63V: 0.47, 1.0, 1.5, 2.2, 3.3, 8p; 4.7 9p; 10 10p; 15 12 12p; 33 15p; 47 12p; 68 16p; 100 19p; 220 26p; 1000 70p; 2200 95p; 50V: 68 20p; 100 17p; 220 24p; 40V: 6.8 15p; 22 3p; 33 12p; 330 47p; 330 47p; 220 90p; 25V: 4.7, 10, 22, 47, 8p; 100 11p; 150 12p; 220 15p; 330 22p; 470 25p; 680, 1000 34p; 1500 42p; 2000 50p; 3300 70p; 4700 92p; 18V: 2.5, 4.0, 8p; 47, 68, 100 9p; 125 12p; 220 13p; 330 16p; 470 20p; 680 34p; 1000 27p; 1500 31p; 2200 36p; 4700 79p.

TAG-END TYPE: 64V: 4700 245p; 3300 198p; 2200 139p; 50V: 50V: 50V: 2200 116p; 40V: 4700 160p; 25V: 4700 98p; 10,000 320p; 15,000 345p.

TANTALUM BEAD CAPACITORS: 35V: 0.1µ, 0.22, 0.33, 0.47, 0.68, 1.0, 1.5 16p; 2.2 33 18p; 4.7, 6.8 22p; 10 28p; 16V: 2.2, 3.3, 16p; 4.7, 6.8, 10 18p; 15 36p; 22 36p; 33, 47 50p; 100 95p; 220 100p; 10V: 1.5, 2.2 26p; 3.3, 4.7 50p; 100 75p.

SILVER MICA (pf)
2, 3, 4, 7, 6.8, 9, 10, 12, 18, 22, 27, 33, 39, 47, 50, 56, 68, 75, 82, 85, 100, 120, 150, 180 15p; 220, 250, 270, 330, 360, 390, 470, 600, 800 & 820pf 21p; 1000, 1200, 1800 30p each; 3300, 4700 60p each

SIEMENS multilayer miniature capacitors
250V: 1nF, 1n5, 2n, 3n, 4n7, 6n8, 8n2, 10n, 15n, 22n 7p; 18n, 27n, 33n, 47n 8p; 39n, 56n, 68n 9p, 100n 11p; 100V: 10n, 12n, 15n, 150n 11p; 22n 13p; 33n 18p; 47n 23p; 68n 30p; 1µF 34p; 2µF 50p

CERAMIC CAPACITORS: 50V
Range 1pF to 6800pF 4p; 10nF, 15n, 33n, 47n 5p; 100n/30V 7p

POLYSTYRENE Caps: 10pF to 1nF 8p; 1n5 to 12nF 10p

RESISTORS 5 LL Package: 7 Commoned, 1000f, 6800f, 1k, 2K2, 4K7, 10k, 47k, 100k 24p. 8 Commoned: (9 pins) 150f, 180f, 270f, 330f, 1k, 2K2, 4K7, 6K8, 10k, 22k, 47k, 100k 26p.

POTENTIOMETERS: Carbon Track, 0.25W Log & Linear Values
500f, 1K & 2K (LIN ONLY) Single 34p
5K (D-2M) single gang 34p
5K (D-2M) single gang D/P switch 80p
5K (D-2M) dual gang stereo 90p

SLIDER POTENTIOMETERS
0.25W log and linear values 60mm track
5K (D-2M) Single gang 70p

PRESET POTENTIOMETERS
0.1W 50Ω 2.2M Mini Vert. & Horiz. 8p
0.25W 220Ω 4M7 Vert. & Horiz. 12p

RESISTORS Hi-stab, Miniature, 5% Carbon.
0.25W 20E-4M7 E24 3p 1p
0.5W 20E-4M7 E12 3p 1p
1W 20E-10M E12 6p 4p
1% Metal Film 51Ω-1M E24 8p 6p

TRANSISTORS

AC127/8	35	BC441	34	MJE2955	99	TIPI41	105	2N2904A/05A	25	25C1923	50
AC176	28	BC461	34	MJE3055	70	TIPI42	105	06A/07A	26	25C1945	225
AC187/8	32	BC477	40	MJE377B	40	TIPI47	120	2N2926G	10	25C1953	90
AD142	12	BC517	40	MJE377	60	TIPI95	60	2N3053	25	25C1957	90
AD149	79	BC547/8	12	MPP105	30	TIP3055	60	2N3054	55	25C1969	140
AD161/2	42	BC549C	14	MPSA05	25	TIS88A	30	2N3055	40	25C2028	85
AF118	95	BC556/7	15	MPSA06	25	TISS90	30	2N3056	140	25C2029	200
AF139	40	BC558/9	15	MPSA12	32	TISS90	30	2N3155	199	25C2078	170
AF239	55	BC570	16	MPSA55	30	TK100M	70	2N3202/3	10	25C2091	85
BC107/8	10	BCY17/2	20	MPSA56	30	VN106AF	110	2N3207/4	10	25C2166	185
BC107B	14	BD131/2	48	MPSA70	30	VN89AF	99	2N3270/6/7	10	25C2314	65
BC108	14	BD135	45	MPSU02	55	VN89AF	120	2N3708/9	10	25C2465	125
BC108C	14	BD135	45	MPSU05	55	VN89AF	120	2N3710	10	25C2547	30
BC109	10	BD136/7	40	MPSU06	55	VN89AF	120	2N3711	179	25D234	75
BC109B	14	BD138/9	40	MPSU52	65	VN89AF	120	2N3712	199	25K45	90
BC109C	14	BD140	40	MPSU55	60	VN89AF	120	2N3713	210	25K288	225
BC147/8	9	BD245	45	MPSU56	60	ZTK107/8	11	2N3819	27	25J83	225
BC147B	10	BD965A	150	OC23	170	ZTK107/8	11	2N3820	38	25J85	225
BC148C	10	BD965A	150	OC28/36	220	ZTK107/8	11	2N3822/3	45	31N28	112
BC149	9	BF194/5	12	OC41/42	75	ZTK107/8	11	2N3826	90	31N40	112
BC149C	12	BF198/9	18	OC70	40	ZTK300/2	28	2N3866	90	31N40	112
BC157/8	10	BF220	30	OC76	50	ZTK300/2	28	2N3903/4	15	40251	150
BC159	11	BF224	25	OC81/82	50	ZTK300/2	28	2N3906/5	15	40311	60
BC167A	10	BF244A	28	OC83/84	40	ZTK300/2	28	2N4427	80	40313	130
BC168C	10	BF244B	29	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC169C	10	BF256B	35	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC171/2	11	BF257/8	32	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC173	11	BF259	35	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BE177/8	16	BF594/5	30	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC179/81	20	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC182/3	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC182L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC184L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC186/7	26	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC187	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC187L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC188	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC188L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC189	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC189L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC190	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC190L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC191	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC191L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC192	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC192L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC193	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC193L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC194	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC194L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC195	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC195L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC196	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC196L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC197	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC197L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC198	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC198L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC199	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC199L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC200	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70
BC200L	10	BF800/1	25	OC83/84	40	ZTK300/2	28	2N4859	78	40361/62	70

LINEAR IC's

555 CMOS	85	LM324	30	SAB2009	595	ZN419CE	180	8088	£18	SF96364E	800	74S299	540	7472	35	74221	80	LS76	22	LS320	160	4034	140	4517	275
702	75	LM334Z	30	SG4202	295	ZN423E	130	81LS95/96	120	SOP256AL	850	74S301	350	7473	35	74246	100	LS78	40	LS323	175	4035	45	4518	40
709C 8 pin	35	LM335	128	SN76023N	350	ZN425E-8	130	81LS97/98	120	TMS2716-3	725	74S365	250	7474	30	74247	100	LS83	40	LS324	150	4036	278	4519	30
710	48	LM339	47	SN76023P	350	ZN426E-8	130	81LS100	120	TMS4047	100	74S373	400	7475	60	74248	130	LS85	55	LS325	150	4037	115	4520	30
741	14	LM344	60	SN76023Z	350	ZN426E-8	130	81LS101	120	TMS4164-15	395	74S374	365	7476	35	74249	120	LS86	28	LS326	290	4038	110	4521	90
747C 14 pin	65	LM349	115	SN76477	420	ZN429E-8	130	81LS105	120	TMS4416-2	475	74S412	380	7480	50	74251	60	LS90	30	LS327	290	4039	280	4522	125
748C 8 pin	36	LM358	60	SN76488	480	ZN429E-8	130	81LS106	120	TMS4500	650	74S416	380	7480	50	74252	100	LS91	55	LS328	365	4040	40	4526	60
753 B pin	185	LM377	175	SPB629	350	ZN1034E	100	8212	820	TMS4532-3	300	74S471	620	7482	80	74253	175	LS93	35	LS329	60	4041	40	4527	65
810	159	LM379	475	SP0256AL	850	ZN1040E	665	8214	425	TMS4532-3	300	74S472	1150	7483	50	74273	175	LS95	35	LS352	60	4042	40	4528	50
9400CJ	350	LM380	75	TA7120	125	ZN2A234E	850	8216	100	TMS4532-3	300	74S473	1150	7484	50	74274	175	LS96	45	LS353	60	4043	40		

SPEAKERS	81, 0.3W, 2", 2.25", 2.5", 30W, 2.5" 40Ω; 64Ω or 80Ω	80p
DIODES	AA119 15 AA129 20 AA130 15 BA100 15 BA113 20 BY100 24 BY126 12 BY127 14 CRO33 250 OA9 40 OA47 12 OA70 12 OA79 15 OA81 20 OA85 15 OA90 8 OA91 8 OA95 8 OA200 4 OA202 4 IN1914 4 IN1916 6 IN4001/2 5 IN4003 6 IN4004/5 6 IN4006/7 7 IN4148 4 IN5401 15 IN5404 16 IN5406 17 IN5408 19 IN541 15 IN521 9 6A/100V 40 6A/400V 50 6A/800V 65	15 20 15 15 20 24 12 14 250 40 12 12 15 20 15 8 8 8 4 4 4 5 6 6 7 4 15 16 17 19 15 9 40 50 65
BRIDGE RECTIFIERS	1A/100V 18 1A/100V 20 1A/400V 25 1A/600V 34 2A/50V 30 2A/200V 40 2A/400V 46 2A/600V 65 2A/100V 83 6A/600V 125 10A/200V 218 10A/600V 298 25A/200V 240 25A/600V 396 BY164 56 VM18 50	18 20 25 34 30 40 46 65 83 125 218 298 240 396 56 50
ZENERS	1N710 4 39V 400mW 5 8p each Range: 3V3 to 33V 1.3W 15p each	4 5 5 15
VARCAPS	MVAM2 168 BA102 30 BB105B 40 BB106 40	168 30 40 40
TRIACS	3A/100V 48 3A/400V 56 3A/800V 65 3A/100V 60 8A/400V 69 8A/800V 118 12A/100V 78 12A/400V 85 12A/800V 188 25A/100V 480 30A/400V 525 30A/800V 825 T2800D 120	48 56 65 60 69 118 78 85 188 480 525 825 120
SCR's	0.8A/100V 32 5A/300V 38 5A/400V 40 5A/600V 48 8A/300V 40 8A/600V 95 12A/100V 78 12A/400V 85 12A/800V 188 25A/100V 480 30A/400V 525 30A/800V 825 T2800D 120	32 38 40 48 40 95 78 85 188 480 525 825 120
SOLDER PINS	100 75p 500 370p	75p 370p
DIAC	ST2 25	25

OPTO	LEDS price includes Clips TL209 Red 3mm 14 TL211 Green 3mm 10 TL212 Yellow 14 TL220 2" Red 12 0.2" Yel, Grn, Amber 14 Green/Yellow 45 Rectangular LEDs with two part clip, R, G & Y 18 Rectangl. Stackable 48 LEDS 15 Triangular LEDs R&G 16 0.2" Flashing LED Red 58 0.2" Bi colour LEDs 58 Red/Green 65 Green/Yellow 52 0.2" Tri colour LEDs 85 Red/Green/Yellow 85 0.2" Red High Bright 59 High Bright Green or Yellow 46 LD271 Infra Red (emit) 65 TL322 Infra Red (emit) 250 SFH205 detector 118 TL78 (detector) 55 TL38 90 TL181 82; TL100 50	14 10 14 12 14 45 18 15 58 58 65 52 85 85 59 46 250 118 55 90 50
7 Segment Displays	TL321 5" C An 120 TL322 5" C Cath 120 DL704 3" C.Cth 125 DL707 3" C.Anod 125 FND357 or 500 130 +1.3" Green C.A. 140 +1.3" Red or Green 150 Bargraph 10 seg 250 Bargraph NSM5914 500	120 120 125 125 130 140 150 250 500
CRYSTAL DISPLAYS	3 1/2 digit 485 4 digit 530 6 digit 625	485 530 625
ALUM BOXES	4x2 1/2" 85 4x2 1/2" 2 1/2" 120 4x4 1/2" 120 5x4 1/2" 105 5x2 1/2" 1 1/2" 99 5x2 1/2" 2 1/2" 130 5x4 1/2" 120 6x4 1/2" 120 6x4 1/2" 150 8x6 1/2" 210 10x4 1/2" 240 10x7 1/2" 275 12x5 1/2" 260 12x8 1/2" 295	85 120 120 105 99 130 120 120 150 210 240 275 260 295
CRYSTAL CLAD BOARDS	Fibre Single-D 95 Glass sided 95 6" x 8" 100p 6" x 12" 175p 225p	95 95 100p 175p 225p
VEROBOARDS	0-1" Clad Plain 180 "VO" Board 395 "DIP" Board 395 Vero Strip 144 2 1/2" x 5" 95p 3 1/2" x 5" 275p 3 1/2" x 7" 275p 4 1/2" x 8" 395p Pkt. of 100 pins 55p Spot Face Cutter 150p Pin insertion Tool 185p	180 395 395 144 95p 275p 275p 395p 55p 150p 185p
PROTOD-DECs	Vero block 405 S-Dec 395 Euro breadboard 395 Birmboard 1 695 Superstrip SS2 113	405 395 395 695 113
VERO WIRING PEN and Spool	Spare Wire (Spool) 75p Wire Wrapping Stakes 100	75p 250p

0.5" LIQUID CRYSTAL DISPLAYS	BPX25 250 BPW21 320 BPX65 320 IL74 65 IL74 115 ILQ74 220 ILC76 Darlington Isolator 135 TL111 70 OC71 120 ORP12 78 2N5777 50 4N33 135 Pin diode 610 Schmitt Receiver 610	250 320 320 65 115 220 135 70 120 78 50 135 610 610
VOLTAGE REGULATORS	1A TO220 Plastic Casing +ve -ve 5V 7805 40p 7905 45p 12V 7812 40p 7912 45p 15V 7815 40p 7915 45p 18V 7818 40p 7918 45p 24V 7824 40p 7924 45p 100mA TO92 Plastic Casing 5V 78L05 30p 79L05 50p 6V 78L06 30p 9V 78L09 30p 12V 78L12 30p 79L12 50p 15V 78L15 30p 79L15 50p	40p 45p 40p 45p 40p 45p 30p 30p 30p 30p 50p 50p
SLIDERS	SLIDE 250V 1A DPDT 15 SPST 35 1A DPDT C/OFF 14 DPDT 48 1A DP ON/OFF 40 4 pole on/off 54	35 48 54
SWITCHES	TOGGLE 2A 250V 1A DPDT 15 SPST 35 1A DPDT C/OFF 14 DPDT 48 1A DP ON/OFF 40 4 pole on/off 54	35 48 54
PUSH BUTTON	Spring loaded 60 Latching or SPST on/off 54 Momentary 6A SPDT c/over 110 SPDT c/over 160 DPDT c/over 160 DPDT C/OFF 88 DPDT on/off on 185 DPDT Biased 145 DPDT Biased 205	60 54 110 160 160 88 185 145 205
MINIATURE	Non Locking 15p Push to make 25p Push break 25p	15p 25p 25p
ROTARY (Adjustable Stop Type)	1 pole/2 to 12 way, 2p/2 to 6 way, 3 pole/2 to 4 way, 4 pole/2 to 3 way 48p	48p
ROTARY: Mains 250V AC, 4 Amp	64p	64p
OIP SWITCHES: (SPST) 4 way 65p;	6 way 80p; 8 way 87p; 10 way 100p; 16 way 140p	65p 80p 87p 100p 140p
AMPHENOL PLUG	24 way IEEE 475p 36 way Centronics 525p	475p 525p
ASTEC UHF MODULATORS	6MHz Standard 325p 8MHz Wideband 450p	325p 450p

DIL SOCKETS	Low profile Wire wrap 8 pin 8p 25p 16 pin 10p 42p 18 pin 16p 52p 20 pin 20p 60p 22 pin 22p 65p 24 pin 25p 70p 28 pin 28p 80p 40 pin 30p 99p	8p 10p 16p 20p 22p 25p 28p 30p
ZIF DIL SOCKET	24 way 565p 28 way 750p 40 way 799p	565p 750p 799p
DIL PLUGS (Headers)	Pins Solder IDC 14 38p 95p 16 42p 100p 24 88p 138p 28 185p 290p 40 195p 218p	38p 42p 88p 185p 195p
RIBBON CABLE (price per foot)	Ways Grey Colour 10 15p 28p 16 20p 40p 20 30p 50p 26 40p 85p 34 60p 85p 40 70p 90p 64 100p 135p	15p 20p 30p 40p 60p 70p 100p
DIL CONNECTORS:	Pins 9 15 25 37 way way way way	9p 15p 25p 37p
MALE	Solder 80p 110p 160p 240p Angle 150p 210p 250p 355p Strait 170p 160p 220p 310p	80p 150p 170p
FEMALE	Solder 105p 160p 200p 338p Angle 165p 215p 290p 440p Strait 175p 200p 300p 420p	105p 165p 175p
COVERS	80p 75p 75p 90p	80p 75p 75p 90p
EDGE CONNECTORS	2x18 way 180p 2x22 way 199p 2x23 way 170p 2x25 way 225p 2x28 way 210p 2x30 way 245p 2x36 way 295p 2x40 way 315p 2x43 way 395p 2x75 way 550p	180p 199p 170p 225p 210p 245p 295p 315p 395p 550p
SIL SOCKETS	0.1" 185p 0.2" 198p 0.25" 215p 0.3" 235p 0.36" 230p	185p 198p 215p 235p 230p
JUMPER LEADS	20pin 26pin 34pin 40pin 1 end 160p 200p 250p 300p 2 ends 290p 370p 480p 525p	160p 200p 250p 300p 290p 370p 480p 525p

PCB Male with latch	Strt. Angle 10 way 90p 99p 85p 16 way 130p 150p 110p 20 way 145p 166p 125p 26 way 175p 200p 150p 34 way 205p 236p 169p 40 way 220p 250p 190p 40 way 235p 270p 200p	90p 130p 145p 175p 205p 220p 235p
PCB Female Header	Strt. Angle 10 way 90p 99p 85p 16 way 130p 150p 110p 20 way 145p 166p 125p 26 way 175p 200p 150p 34 way 205p 236p 169p 40 way 220p 250p 190p 40 way 235p 270p 200p	90p 130p 145p 175p 205p 220p 235p
Female Card-Edge Connector	Strt. Angle 10 way 90p 99p 85p 16 way 130p 150p 110p 20 way 145p 166p 125p 26 way 175p 200p 150p 34 way 205p 236p 169p 40 way 220p 250p 190p 40 way 235p 270p 200p	90p 130p 145p 175p 205p 220p 235p
TRANSFORMERS (mains Prim. 220-240V)	3-0-3V, 6-0-6V 100mA; 9-0-9V 75mA; 12-0-12V 75mA; 15-0-15V 75mA; 6VA; 2x6V-5A; 2x9V-4A; 2x12V-0.3A; 2x15V-2.5A 250p 12VA; 2x4V5-1.3A; 2x6V-1.2A; 2x12V-0.5A; 2x15V-0.4A 345p (36p p&p) 12VA; 6V-1.5A 6V-1.5A; 9V-1.2A 9V-1.2A; 12V-1A 12V-1A; 15-8A 15-8A; 20V 6A 20V-6A 385p (60p p&p) 50VA; 2x6V-4A; 2x9V-2.5A; 2x12V-2A; 2x15V-1.5A; 2x20V-1.2A; 2x15V-3A; 2x20V-2.5A; 2x30V-1.5A; 2x40V-1.25A; 2x50V-1A 965p (60p p&p)	250p 345p 385p 965p

BEEBFONT ROM	This is a character FONT ROM that gives you 5 16x16 predefined FONT. The ROM is ideal for high quality demonstration on screen and when used in conjunction with EPSON printer, allows printing of letters etc. in mixed type faces. The package is complete, including an Editor to design your own Fonts and several spare Fonts which could not be fitted in the ROM can still be run from RAM. Supplied complete with ROM, software on DISC/tape and Manual. Price £45
IDC CONNECTORS (Speed block type)	2 rows 10 way 90p 99p 85p 16 way 130p 150p 110p 20 way 145p 166p 125p 26 way 175p 200p 150p 34 way 205p 236p 169p 40 way 220p 250p 190p 40 way 235p 270p 200p
EURO CONNECTORS	Gold flashed contacts DIN 41612 2x32 way 275p DIN 41612 2-3x32 way 295p DIN 41612 3x32 way 360p
FEMALE SOCKETS	Strt. Angle 10 way 90p 99p 85p 16 way 130p 150p 110p 20 way 145p 166p 125p 26 way 175p 200p 150p 34 way 205p 236p 169p 40 way 220p 250p 190p 40 way 235p 270p 200p
MALE PLUGS	Strt. Angle 10 way 90p 99p 85p 16 way 130p 150p 110p 20 way 145p 166p 125p 26 way 175p 200p 150p 34 way 205p 236p 169p 40 way 220p 250p 190p 40 way 235p 270p 200p

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1.5MHz	420
1.6MHz	395
1.8MHz	395
1.8432M	200
2.0MHz	200
2.4576M	200
2.5MHz	225
2.56250M	220
3.2768M	150
3.57954M	300
3.6864M	300
4.0MHz	150
4.032MHz	290
4.194304M	200
4.433619M	100
4.5MHz	200
4.80MHz	200
5.0MHz	160
5.185MHz	300
5.24288M	390
6.0MHz	140
6.144MHz	150
6.5356MHz	150
7.0MHz	150
7.168MHz	250
7.68MHz	200
8.0MHz	150
8.08333M	395
8.967237M	175
9.00MHz	200
9.375MHz	350
10MHz	175
10.5MHz	250
10.7MHz	150
10.24MHz	200
12.0MHz	175
12.528MHz	300
14.31818M	170
14.7456M	175
14.7655MHz	250
15.0MHz	200
16.0MHz	200
18.0MHz	180
18.432M	150
19.968MHz	150
20.0MHz	200
24.0MHz	170
24.930MHz	325
29.695MHz	150
26.670MHz	325
27.125MHz	295
27.145M	190
27.548MHz	300
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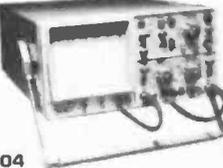


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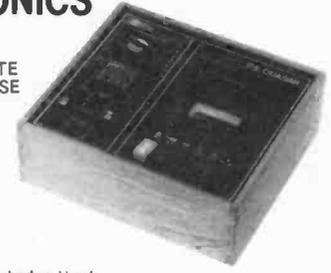
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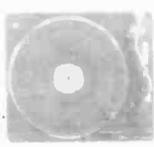
3 speed, manual, auto, setdown; with auto return.

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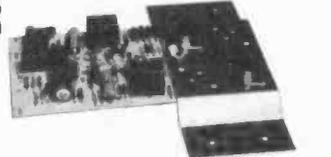


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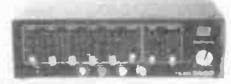


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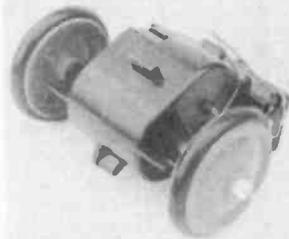
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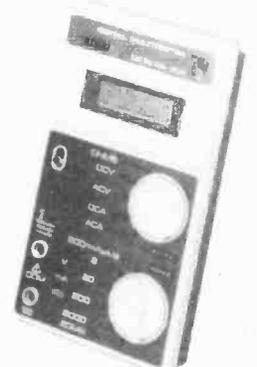
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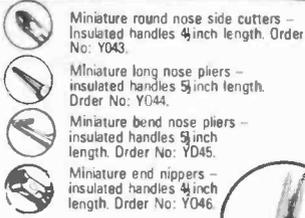
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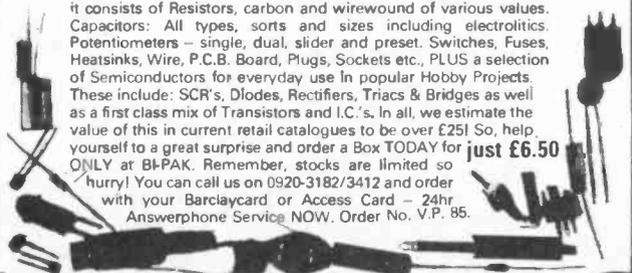
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SN75183	0.62	
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SN75189	0.44	
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SN75452BP	0.24	
SN75453BP	0.24	

SN75454BP

SN75454BP	0.24
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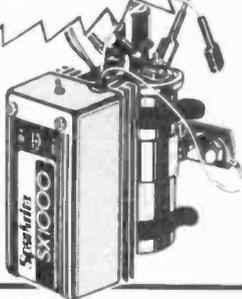
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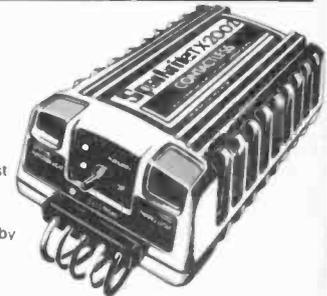


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AT-40 Electronic Car Alarm

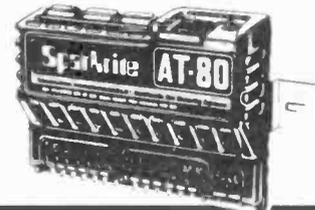
- Guards doors, boot, bonnet from unauthorised entry ● Armed/disarmed using concealed switch ● 30 second delay-to-arm: 7 second entry delay ● Can alternatively be wired to exterior key switch ● Flashes headlights & sounds horn intermittently for 60 seconds when activated ● Security loop protects accessories ● Low consumption C-MOS circuitry.



NEW

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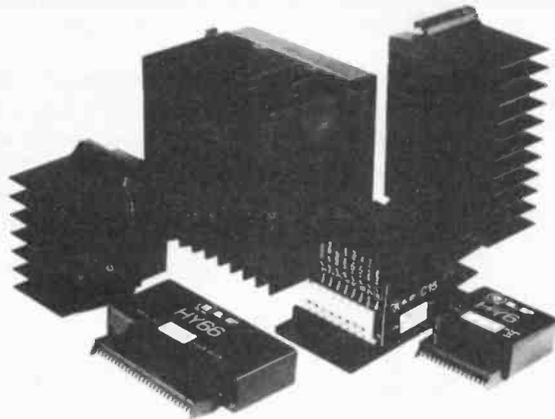
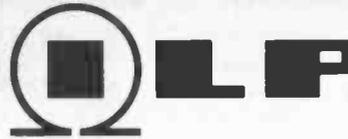
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BIPOLAR MODULES

Module Number	Output Power Watts rms	Load Impedance Ω	DISTORTION		Supply Voltage Typ	Size mm	WT gms	Price inc. VAT
			T.H.D. Typ at 1KHz	I.M.D. 60Hz/7KHz 4:1				
HY30	15	4-8	0.015%	<0.006%	\pm 18	76 x 68 x 40	240	£8.40
HY60	30	4-8	0.015%	<0.006%	\pm 25	76 x 68 x 40	240	£9.55
HY6060	30 x 30	4-8	0.015%	<0.006%	\pm 25	120 x 78 x 40	420	£18.69
HY124	60	4	0.01%	<0.006%	\pm 26	120 x 78 x 40	410	£20.75
HY128	60	8	0.01%	<0.006%	\pm 35	120 x 78 x 40	410	£20.75
HY244	120	4	0.01%	<0.006%	\pm 35	120 x 78 x 50	520	£25.47
HY248	120	8	0.01%	<0.006%	\pm 50	120 x 78 x 50	520	£25.47
HY364	180	4	0.01%	<0.006%	\pm 45	120 x 78 x 100	1030	£38.41
HY368	180	8	0.01%	<0.006%	\pm 60	120 x 78 x 100	1030	£38.41

Protection: Full load line, Slew Rate: 15V/ μ s, Rise time: 5 μ s, S/N ratio: 100dB. Frequency response (-3dB) 15Hz - 50KHz. Input sensitivity: 500mV rms. Input Impedance: 100K Ω . Damping factor: 100Hz > 400.

PRE-AMP SYSTEMS

Module Number	Module	Functions	Current Required	Price inc. VAT
HY6	Mono pre amp	Mic/Mag. Cartridge/Tuner/Tape/Aux + Vol/Bass/Treble	10mA	£7.60
HY66	Stereo pre amp	Mic/Mag. Cartridge/Tuner/Tape/Aux + Vol/Bass/Treble/Balance	20mA	£14.32
HY73	Guitar pre amp	Two Guitar (Bass Lead) and Mic + separate Volume Bass Treble + Mix	20mA	£15.36
HY78	Stereo pre amp	As HY66 less tone controls	20mA	£14.20

Most pre-amp modules can be driven by the PSU driving the main power amp. A separate PSU 30 is available purely for pre amp modules if required for £5.47 (inc. VAT). Pre-amp and mixing modules in 18 different variations. Please send for details.

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Model Number	For Use With	Price inc. VAT
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PSU 41X	1 or 2 HY60, 1 x HY6060, 1 x HY124	£13.83
PSU 42X	1 x HY128	£15.90
PSU 43X	1 x MOS128	£16.70
PSU 51X	2 x HY128, 1 x HY244	£17.07

Please note:

X in part no. Indicates primary voltage. Please insert "0" in place of X for 110V, "1" in place of X for 220V, and "2" in place of X for 240V.

MOSFET MODULES

Module Number	Output Power Watts rms	Load Impedance Ω	DISTORTION		Supply Voltage Typ	Size mm	WT gms	Price inc. VAT
			T.H.D. Typ at 1KHz	I.M.D. 60Hz/7KHz 4:1				
MOS 128	60	4-8	<0.005%	<0.006%	\pm 45	120 x 78 x 40	420	£30.41
MOS 248	120	4-3	<0.005%	<0.006%	\pm 55	120 x 78 x 80	850	£39.86
MOS 364	180	4	<0.005%	<0.006%	\pm 55	120 x 78 x 100	1025	£45.54

Protection: Able to cope with complex loads without the need for very special protection circuitry (fuses will suffice).

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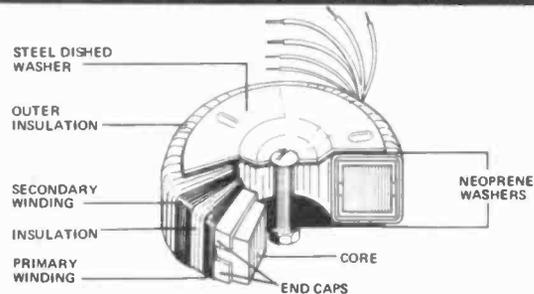
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120	4	11.73	625	9	31.63

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GOOD AND BAD

In line with much of the rest of industry electronics companies have had a mixed year in terms of profitability. The recently published Jordan Survey shows the fortunes of 500 UK electronic and electrical companies during 1982. While some well known names have achieved remarkable profits against sales, others have shown dramatic decreases in turnover and substantial profit drops.

A few examples of well known companies will give an illustration: Farnell Electronics achieved almost 25 per cent profit against turnover. Amstrad Consumer Electronics achieved an increase in turnover of more than 98 per cent, while Celestion International registered a trading loss of nearly £1.3 million. Perhaps more interesting is that a number of companies have managed to reverse a downward trend. Muirhead for instance have moved from a loss of almost £2.3 million in 1980 to a profit of more than £1.2 million in '82.

WAGE RATES

The survey covers many areas concerned with finance, including average

wage rates calculated from the wage bill and number of employees. Average wage of the top thirty companies is over £7,900 and at the top of the list IBM UK Holdings Ltd. are paying an average wage of £13,700. The top thirty include Digital Equipment, ICL, National Panasonic (UK), Hewlett Packard, JVC (UK) Ltd., Ampex, Burroughs Machines, Pirelli UK, RCA, BICC, Robert Bosch, Racal, Pioneer High Fidelity (GB) and Rank Precision Industries Ltd., plus others whose names are not quite so familiar.

Obviously not all the figures can be taken at face value, for instance a new company last year should have little problem in achieving a substantial increase in turnover this year. A company that employs only a few "directors" may come top of the average wage table; but, in general, those examples shown above are realistic.

One point that comes to mind when reading the list of companies on the wage table is that there are a sprinkling of Japanese based organisations in the top 30. Perhaps it is not only the lower wage bill in the Far East that makes them profitable—could it be that they are simply good business men?

GUARANTEE

One thing that is clear is that being in electronics is no guarantee of profitability. While many high technology companies are flourishing some—even in relatively new areas—have financial problems. The position of the American video games companies springs to mind in this context with names like Atari showing losses in this particular area (as opposed to their home computer sales).

However, even the giant Texas Instruments has found it uneconomic to compete in the home computer market. TI have now ceased production of their home computer and moved right out of this area. Osborne has its problems as has Victor who make the Sirius computer; both companies are operating in what is accepted to be the flourishing world of personal computers, with systems aimed at the business user.

The moral must be that you have to be good to survive in any market.



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We are unable to offer any advice on the use or purchase of commercial equipment or the incorporation or modification of designs published in PE. All letters requiring a reply should be accompanied by a stamped, self addressed envelope, or addressed envelope and international reply coupons, and each letter should relate to one published project only.

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MULTITASKING ZX81

You would not think that even major surgery could turn the ZX81 into a fast, multitasking machine, so it comes as a surprise to learn that changing just one i.c. achieves exactly this.

Swap the ZX81's Sinclair BASIC ROM for David Husband's ZX81 FORTH EPROM, and you have a machine that will run about 300 times faster, and can work a schedule comprising many different "background" jobs (multitasking) without the use of interrupts.

Up to 63 different tasks may be timetable/priority activated, although ten simultaneous tasks is a practical limit if editing new programs is not to be painfully slowed down. Like we humans, the more divided the computer's attentions, the slower becomes its execution of individual tasks.

Requiring at least 2K RAM, the EPROM provides user-defined split screen format, it being possible to run the editor whilst the "execution" screen is running a program. ZX81 FORTH is a compiler directive

language (quite unlike BASIC) and does not use fig-FORTH's inner interpreter approach—a departure that makes it faster than fig-FORTH. ZX81 FORTH matches fig-FORTH's standards but lacks some of the vocabulary (restricted by memory space). On the other hand, it includes extra words for multitasking.

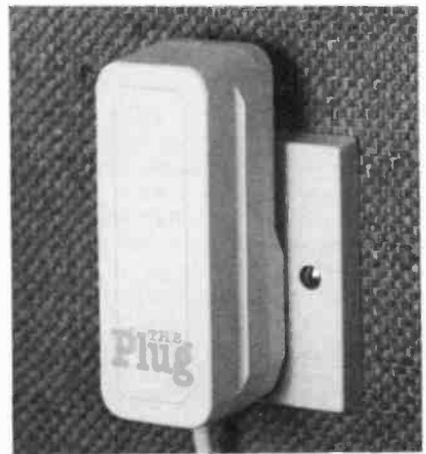
The ZX81 FORTH EPROM is available from David Husband, 2 Gorleston Road, Branksome, Poole, Dorset BH12 1NW. Tel: 0202 764724. Price: £25 plus VAT (includes manual). Ready converted ZX81s are also available.

The ZX81 FORTH operating system and language incorporates a realtime clock, but has only integer arithmetic, although an extension ROM p.c.b. containing floating-point arithmetic and other refinements is to become available.

PI's PLUG

Microcomputers suffering from amnesia need no longer be terminal cases!

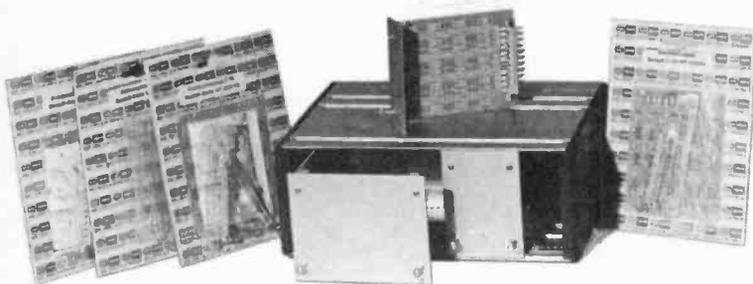
Spikes and holes in the domestic mains electricity supply (caused by switching off and switching on electrical equipment) can create havoc for microprocessor users—at worst, a complete crash, at best, a corruption of vital data.



To prevent downtime, reprogramming and to enhance the microcomputer's reliability, Power International's 'PLUG'—a neatly packaged RFI filter and transient suppressor of innovative design contained in a modified 13 amp plug case—effectively absorbs spikes in the power line and reduces their voltage to a tolerably safe level.

The cost of the plug is £15.50 (including post, packing and VAT) from Power International Ltd., 2A Isambard Brunel Road, Portsmouth, Hants.

MODULAR RACK SYSTEM



Just one of the equipment housing options available from the 1984 Bicc-Vero catalogue (Hobby Herald) is the KMT Card Frame range, in kit form.

This system is extremely flexible and incorporates an extruded aluminium and plastic box into which can be plugged different sized modules each with their own front panel, veroboard and edge-connector. There is ample access for interconnections between modules within the unit. A further advantage is the partitioned rear section in which power supplies can be both electrically and thermally segregated.

The 1984 Hobby Herald costs 50pence, it contains over 100 new products, the KMT system however costs slightly more: around £12 for the box, with modules extra. All available from, Retail Department, Bicc-Vero Electronics Ltd, Industrial Estate, Chandler's Ford, Hants SO5 3ZR (04215-62829).

ERL's LEAD

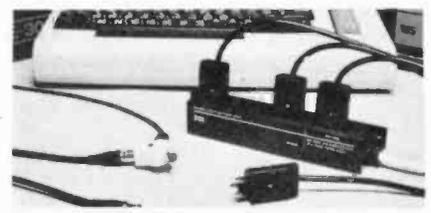
The increasing popularity of home computers, video, and hi-fi separates means that many households are suffering from a proliferation of cable 'spaghetti' in their living rooms. To overcome this problem ERL has developed the multiplug.

This is a compact four-way mains distribution unit. Supplied with high quality three core cable and plugs the complete unit measures only 175x35x35mm. It can be mounted either on a wall or directly onto the back of the equipment.

Alternatively it could form the basis of a simple do-it-yourself housing for computer, television, video or hi-fi equipment. The unit is rated at thirteen amps and can handle up

to six amps at each outlet. The recommended retail price is £7.95 or less.

ERL has also developed the Aerial Adaptor. It's a switched two way adaptor which allows the user to select either of two coaxial inputs (such as roof top aerial or computer) into the TV monitor. Alternatively it can be used with a stand alone games unit as well as a micro computer. The recommended retail price is £1.50. Both products are available through electrical, hi-fi and computer stores.



MARKET PLACE

CAPACITANCE METER CM200

The newly released CM200 from Thurlby Electronics Ltd is a digital capacitance meter which has a maximum delay between connecting a capacitor and getting the first valid reading of less than half a second. This rapid settling combined with a reading update rate of 3 per second makes the meter unusually fast to use.

The CM200 has a 4½ digit liquid crystal display with a maximum reading in excess of 25,000 counts. It measures capacitance between 1pF and 2,500µF to an accuracy of 0.2%.

Very low power consumption enables the CM200 to operate for several hundred hours from batteries. Alternatively it can be operated from the a.c. line adaptor supplied with it.



A special input socket arrangement allows for the direct connection of a wide variety of capacitors, or for the connection of standard test leads. A zero calibration control enables the user to null out up to 25pF of test lead capacitance.

The CM200 costs £89 plus VAT. Details from Thurlby Electronics Ltd., New Road, St Ives, Cambs. Tel (0480) 63570.

Silicon News Corner

CTS Microsystems ♦ CTS108AGB high specification precision op. amp. Extremely low offset voltage.

♦ CTS00061B hybrid high voltage, high current driver. 45V supply and 1.5A pulsed load. Ideal for non-linear resistive loads such as incandescent lamps.

♦ CTS111GB voltage comparator with input currents around 100 times lower than 710. Can drive lamps or relays direct (up to 50V @ 50mA).

♦ CTS0041ZB general purpose diff. input op. amp. gives output of 200mA.

♦ CTS2111EB dual voltage comparator (2 x CTS111GB type comparator).

♦ CTS2108AEB dual op. amp. Contains two "108A" type precision op. amps. with extremely low offset voltage

♦ CTS2101AEB dual op. amp. comprises two "101A" type devices featuring high gain, s/c protection and excellent temp. stability.

♦ CTS0034CB dual high speed level shifter interfaces TTL/DTL to MOS/JFET

♦ CTS861GB cermet hybrid i.c. is a log. (i.f.) amplifier, 10MHz to 100MHz. Voltage gain of 12dB.

♦ CTS0024GB very wide bandwidth, high slew rate op. amp. for buffers, D/A & A/D converters and high speed comparators. Useful gain to 50MHz.

♦ CTS0033ZB voltage follower (high speed buffer) for line driving.

Exar Systems Inc. ♦ XR-14412 contains everything necessary to construct a complete FSK modulator/demodulator (modem) system, in either US or CCITT standard.

♦ XR-2120 self-contained CMOS bandpass filter set designed to realise the BELL 212A compatible 1200bit/sec. PSK modems.

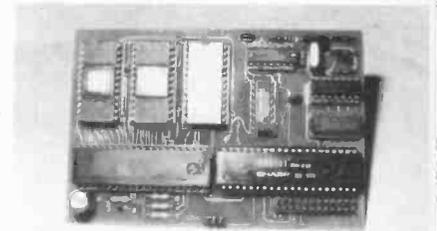
♦ XR-2123 contains the heart of a full duplex BPS modem.

CTS and XR devices both available from Rastra Electronics Ltd., 275-281 King Street, Hammersmith, London W6 9NF. Tel: 01-748 3143.

CONTROL 65

Control 65 is a small low cost micro controller p.c.b. allowing 'stand alone' terminals to have intelligence and flexibility. A +5V supply is all that is required to make the compact 75mm x 100mm p.c.b. into a versatile controller offering 16 TTL compatible Input/Output lines, up to 8KB of EPROM decoding, 2KB of user RAM plus the popular 6502 microprocessor. Onboard links allow 2716, 2732 EPROM type devices to be used. PI/O interrupts are serviced for fast I/O response times.

The card, which can be easily programmed, is supplied with full user notes and circuit diagram at a price of £49.95 plus VAT from J.P. Designs, 37 Oyster Row, Cambridge (0223) 322234.



Countdown . . .

Please check dates before setting out, as we cannot guarantee the accuracy of the information presented below. Note: some exhibitions may be trade only. If you are organising any electrical/electronics, radio or scientific event, big or small, we shall be glad to include it here. Address details to Mike Abbott.

Which? Computer Show Jan. 17-20 '84. NEC. T1
 BEX Bournemouth (Business Equipment). Feb. 8-9. Pavilion. K
 Electrex Feb. 27-March 2. NEC, B/ham. L3
 Scotest March 6-8. Anderson Exhibition Cntr., Glasgow. T
 Scottish Sensors March 6-8. Anderson Ex. Cntr., Glasgow. T
 Home Appliances International March 12-15. NEC, B'ham. M
 Business Telecom March 13-15. Barbican Cntr., London. O
 Electro-Optics/Laser International March 20-22. Metropole, Brighton. T1
 Scottish Computer Show March '84. Holiday Inn, Glasgow. T1
 All Electronics/ECIF May 1-3. Barbican, London. E

Biotech Europe May 15-17. Wembley Conf. Cntr., London. O
 Scotex June 5-7. Royal Highland Exhibition Halls, Ingleston, Edinburgh. O5
 IBM System User Show June 12-14. Wembley Conf. Cntr., London. O
 Surface Treatment & Finishing Show June 25-29. Birmingham. M
 Networks July 3-5. Wembley Conf. Cntr., London. O
 Cable July 10-12. Wembley Conf. Cntr. O
 Building & Home Improvement Sept. 25-30. Earls Court, London. M
 Computer Graphics Oct. 9-11. Wemb. Conf. Cntr., London. O
 Software Expo Oct. 16-18. Wemb. Conf. Cntr., London. O
 Computers In The City Nov. 20-22. Barbican, London. O
 Data Security Nov. 20-22. Barbican, London. O

E Evan Steadman ☎ 0799 26699
 K Douglas Temple ☎ 0202 20533
 L3 Electrex Ltd. ☎ 0483 222888
 M Montbuild ☎ 01-486 1951
 O Online ☎ 09274 28211
 O5 Institute of Electronics ☎ 0706 43661
 T Trident ☎ 0822 4671
 T1 Cahners ☎ 0483 38085

COMPUTER TERMINAL

PART ONE RAY STUART

THE computer terminal (glass teletype) presented in this article is a serial device being connected to the host computer system via an RS232 link (which is compatible with the BBC's RS423 link). The display consists of 1024 characters arranged as 16 rows each of 64 characters, with the full 128 ASCII character set being supported (see Fig. 1.1). Seventeen of the 32 ASCII control characters are displayed as graphic characters whilst the remaining fifteen provide facilities such as BEL and the various cursor movements (see Table 1.1). Three of these, DC2, DC3 and DC4, together with a small amount of extra circuitry, provide the options of controlling external devices, such as a cassette recorder motor, selecting normal or reverse video, or any other function the reader may care to include.

The computer terminal will drive either a normal television or video monitor, and operate in full or half duplex, with the data format and Baud rate selected by printed circuit board mounted switches. The majority of components are mounted on a single-sided, double Eurocard size p.c.b. A double-sided through-plated-hole p.c.b. was considered but rejected on cost grounds, even though it would eliminate the use of links. The system is housed in an easily constructed case with wooden end plates and painted aluminium panels, to give it a professional appearance.

CIRCUIT DESCRIPTION

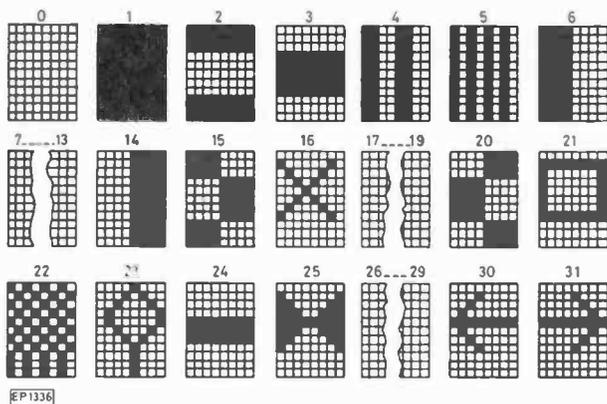
The system is designed around the Thomson SFF96364 cathode ray tube controller (CRTC). This chip contains all the logic necessary to generate the address lines to update and refresh the memory as well as provide the horizontal and vertical sync pulses. In addition, the cursor position can be controlled by means of the C0, C1, C2, inputs. This facility is very useful as it allows characters to be positioned at random, a definite improvement over a mechanical Teletype.

The characters to be displayed are stored in a 1K x 7 bit memory, comprising seven 2102 1K x 1 memory devices IC1 to IC7. A seven bit memory allows the full 128 ASCII character set to be implemented. This type of Random Access Memory (RAM) has separate data input and output lines. It was first thought that it would be better to use a single device such as the 6116; however, as these devices have common data inputs and outputs it would be necessary to include two tri-state buffers. It is true this would reduce the component count, but it would also increase and complicate the p.c.b. layout.

Parallel data from the keyboard is fed to the transmitter section of the 6402 UART (Universal Asynchronous Receiver Transmitter). This device converts the keyboard's parallel output to serial form suitable for transmission to the



Fig. 1.1. The ASCII character code (below), and the graphic characters (above) available using the specified EPROM data. (Listing available from PE Poole office by sending 6 x 9 in. SAE)



Decimal	Char.	Decimal	Char.	Decimal	Char.
000	NUL	043	+	086	V
001	SOH	044	,	087	W
002	STX	045	.	088	X
003	ETX	046	:	089	Y
004	EOT	047	/	090	Z
005	ENQ	048	0	091	[
006	ACK	049	1	092	\
007	BEL	050	2	093]
008	BS	051	3	094	↑
009	HT	052	4	095	↖
010	LF	053	5	096	
011	VT	054	6	097	a
012	FF	055	7	098	b
013	CR	056	8	099	c
014	SO	057	9	100	d
015	SI	058	:	101	e
016	DLE	059	;	102	f
017	DC1	060	<	103	g
018	DC2	061	=	104	h
019	DC3	062	>	105	i
020	DC4	063	?	106	j
021	NAK	064	@	107	k
022	SYN	065	A	108	l
023	ETB	066	B	109	m
024	CAN	067	C	110	n
025	EM	068	D	111	o
026	SUB	069	E	112	p
027	ESC	070	F	113	q
028	FS	071	G	114	r
029	GS	072	H	115	s
030	RS	073	I	116	t
031	US	074	J	117	u
032	SPACE	075	K	118	v
033	!	076	L	119	w
034	”	077	M	120	x
035	#	078	N	121	y
036	\$	079	O	122	z
037	.	080	P	123	{
038	&	081	Q	124	
039	'	082	R	125	}
040	(083	S	126	~
041)	084	T	127	DEL
042	*	085	U		

LF=Line Feed FF=Form Feed CR=Carriage Return DEL=Rubout

host system. These signals do, however, need to be transformed from TTL levels to the RS232 levels of +12 volt and -12 volt. This is achieved by IC18b, logic "0" being represented by +12 volts and logic "1" by -12 volts. Incoming data from the host system is converted from RS232 to TTL levels by IC21a before being fed to the UART's receiver section. This section works in the opposite mode to the transmitter section in that it converts serial data to parallel data. When a complete character has been received, the UART produces a strobe to inform the SFF96364 that a character is available. Pins 35 to 39 on the UART allow it to be programmed so that the data format is compatible with that of the host system. Table 1.2 indicates the possible formats that may be selected by means of S5 to S10.

By making a very simple modification to the p.c.b. it is possible to install an AY-5-1013 type UART in place of the 6402. The only difference between these two devices is that the AY-5-1013 requires a -12 volt supply whereas the 6402 does not. All that is required is to connect the UART's pin 2 to the -12 volt line by a short length of wire.

Not only does the data sent to the host system have to be in the correct format as stated above, it also has to be transmitted at the correct speed. A crystal controlled Baud rate generator IC16, whose output frequency is selected by switches S1 to S4, is therefore included in the design. S1 to S4 should be set for the desired Baud rate (55 to 19200 Baud) by referring to Table 1.3.

Switch S11 is included to allow the "glass teletype" to operate in either full or half duplex. In most applications the host system echoes the received character back to the sending device, which is called *full* duplex. However if the

Cursor movement	Key	Hexadecimal code (ASCII)	Execution time
Cursor left	CTL/H	08 (BS)	8.3mS
Cursor right	CTL/I	09 (HT)	8.3mS
Cursor down	CTL/J	0A (LF)	8.3mS
Cursor up	CTL/K	0B (VT)	8.3mS
Page clear and home cursor	CTL/L	0C (FF)	132mS
Carriage return and erase to end of line	CTL/M	0D (RC)	4.2mS
Erase current line	CTL/Z	1A (SUB)	8.3mS
Line feed	SHIFT CTL/K	1B (ESC)	8.3mS
Home cursor	SHIFT CTL/L	1C (FS)	132mS
Carriage return	SHIFT CTL/M	1D (GS)	4.2mS

Function	D ₇	D ₂	D ₁	D ₀
Cursor left	0	0	0	1
Cursor right	0	1	1	1
Cursor down	1	0	1	0
Cursor up	0	0	1	1
Clear screen	1	0	0	0
Carriage return	1	1	0	0
Erase line	1	1	0	1
Line feed	0	0	1	0
Home cursor	0	0	0	0
Normal character	1	1	1	1

Control EPROM outputs

NB D₃ = BEL = A
 D₄ = DC1 = B
 D₅ = DC2 = C
 D₆ = DC3 = D
Table 1.1. Terminal functions available through the RS232 link

host system does not echo the character, or if the glass teletype is to be tested, it should be set to *half duplex*. In this mode the glass teletype's output is directly connected to its input, which is disconnected from the host system's output.

The seven bit word from the UART's receiver is fed to a 2716 Erasable Programmable Read Only Memory (EPROM). This, the control EPROM, is programmed to provide the SFF96364 with data so that the various cursor movements can be implemented, as well as control external devices. The EPROM program is available from PE. The seven bit word from the UART's receiver is also fed to the series of gates IC17a,c,d & IC18b,d & IC19b,c,d. For normal characters (alpha-numeric and graphic) the outputs from these gates are the same as their inputs as the SFF96364's Clear Screen line (pin 13) is at logic "1". However, if the code for clear screen (CTL/L) is received, the SFF96364 will hold the Clear Screen line at logic "0". This forces the outputs of these gates to the ASCII code for *space* (20 HEX), whilst the SFF96364 writes this code into all the RAM's memory locations thereby effectively clearing the screen.

CHARACTER GENERATOR

The RAM's outputs are latched by IC8 before being fed to the character generator EPROM IC12, a second 2716. Readily available character generators, such as the RO-3-2513, are normally used in this type of design, but they will only support either upper or lower case alpha-numeric characters. The use of a 2716 EPROM is not only a cheaper solution, it also allows this system to have both upper and lower case alpha- numerics, plus some graphic characters. In addition the use of an EPROM allows the reader to produce whatever character set he or she may desire. For example, one application may require the Greek alphabet instead of lower case. The method of devising the EPROM data will be discussed later.

Switch	Format
S9	OFF No parity bit
	ON Parity bit
S5	OFF Even parity
	ON Odd parity
S8	OFF 2 Stop bits
	ON 1 Stop bit
S7	ON 5 Character bits
S6	ON 6 Character bits
S7	OFF 7 Character bits
S6	ON 7 Character bits
S7	OFF 8 Character bits
S6	OFF 8 Character bits

NB S10—not used

Table 1.2. Formats selected by S5-S10

Baud rate	S1	S2	S3	S4
50	ON	ON	ON	ON
75	ON	ON	ON	OFF
110	ON	ON	OFF	ON
134.5	ON	ON	OFF	OFF
150	ON	OFF	ON	ON
300	ON	OFF	ON	OFF
600	ON	OFF	OFF	ON
1200	ON	OFF	OFF	OFF
1800	OFF	ON	ON	ON
2000	OFF	ON	ON	OFF
2400	OFF	ON	OFF	ON
3600	OFF	ON	OFF	OFF
4800	OFF	OFF	ON	ON
7200	OFF	OFF	ON	OFF
9600	OFF	OFF	OFF	ON
19200	OFF	OFF	OFF	OFF

Table 1.3. Baud rate selection

Fig. 1.2. PSU and video mixer circuit diagram

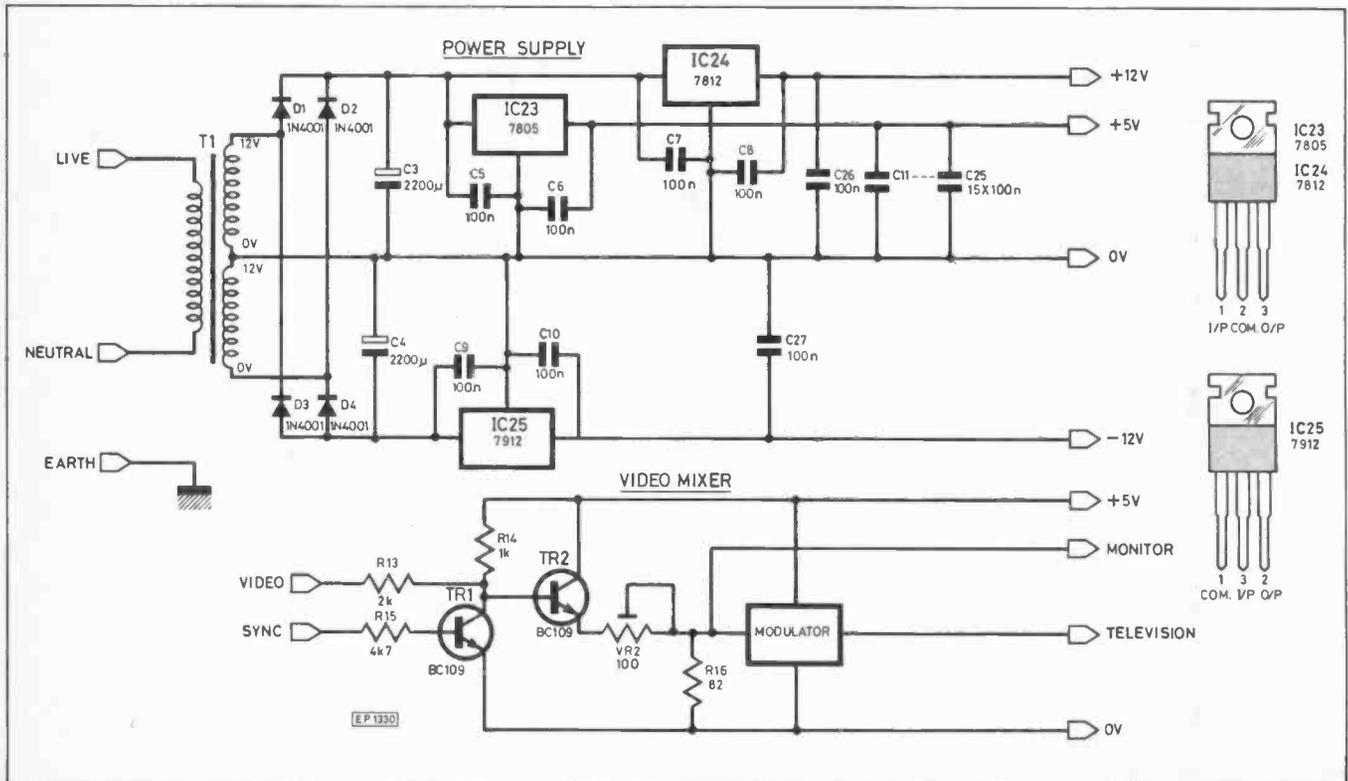
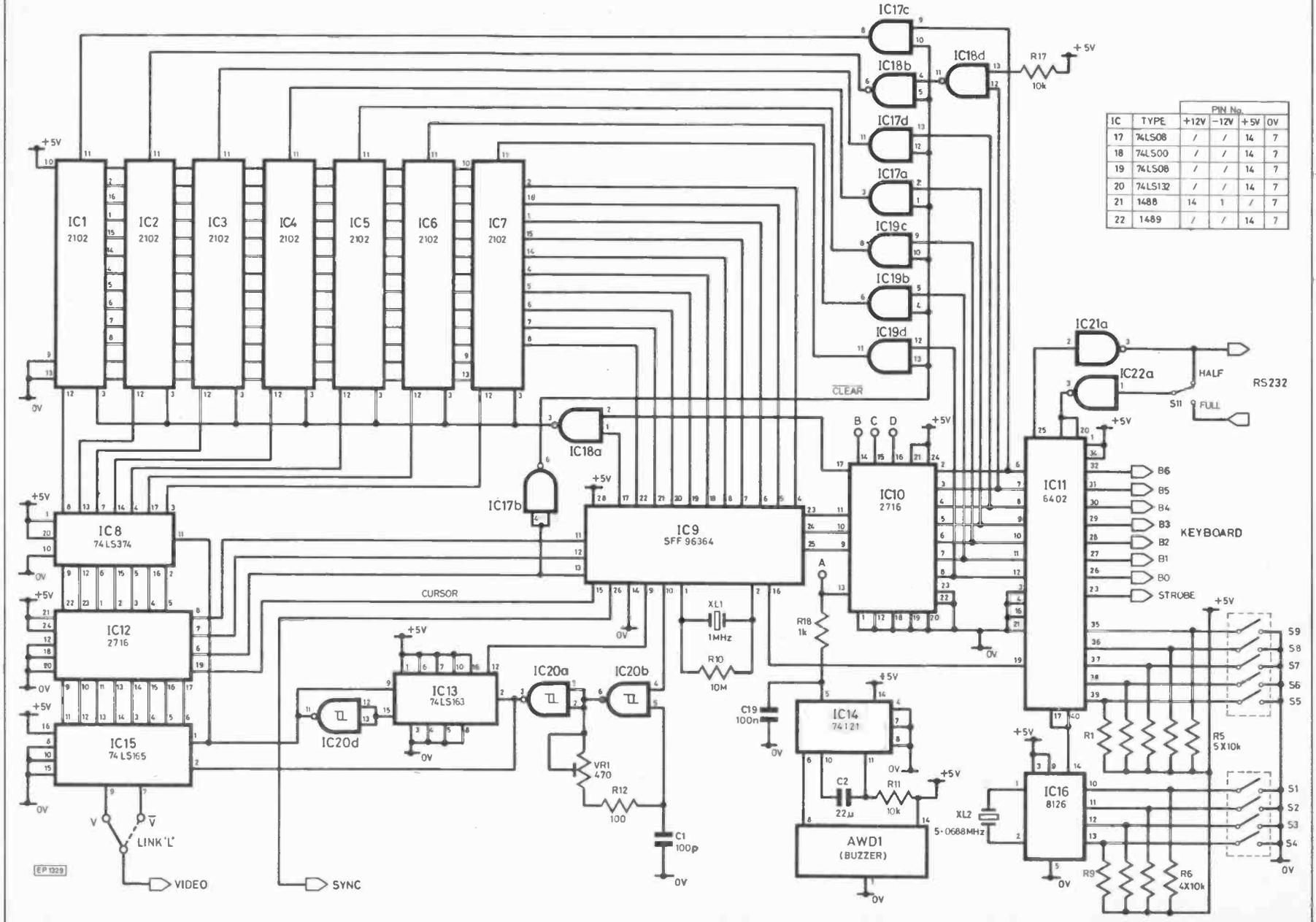


Fig. 1.3. Full circuit diagram



IC	TYPE	PIN No.			
		+12V	-12V	+5V	0V
17	74LS08	/	/	14	7
18	74LS00	/	/	14	7
19	74LS08	/	/	14	7
20	74LS132	/	/	14	7
21	1488B	14	1	/	7
22	1489	/	/	14	7

EP1329

The output from the character generator EPROM is loaded into a shift register IC15. This device provides two complementary outputs which can be used to provide either normal or reversed video as required, via link "L". IC20a and IC20b are connected to form a gated oscillator running at approximately 13MHz, the dot rate clock. This clock is fed to the shift register to provide the required series of dots to form the characters on the screen, i.e. the video signal. As each character is eight bits wide IC13 and IC20d divide the dot rate by eight to produce the character rate clock. This is fed to the shift register and the latch, thereby setting the dot sequence for the next character. This arrangement allows the EPROM's address lines to be set one character before being output from the shift register, thereby giving the EPROM sufficient time to access the data. A variable resistor VR1 allows the dot rate, and hence character width, to be altered to suit the video monitor, or television used.

A second output from IC13 is fed back to the SFF96364 so that correct synchronisation of the character generator row counter output (R0,R1,R2) may be achieved. During the time between the last character on a line and the first character on the next line being displayed no information should be output from the shift register. To achieve this the SFF96364 outputs a signal from pin 10 that inhibits the 13MHz dot rate oscillator, thereby preventing spurious data being displayed on the screen.

The video output from the shift register IC15, either normal or reversed, and the sync. pulses from the SFF96364's pin 26, are combined by TR1 and buffered by TR2 to produce a composite video signal suitable for driving an external video monitor, and the onboard UHF modulator type UM1233. The latter's output may be used to drive a standard television. VR2 is included to allow the composite video voltage to be adjusted to suit the monitor, or television used.

An output from the control EPROM (03) is produced whenever the ASCII character CTL/G (BEL) is received. This signal is fed, via a filter (R18,C19) to IC14, a monostable whose output pulse is used to energise a small on-board buzzer for approximately half a second to produce the BEL facility. The buzzer's duration may be adjusted to suit requirements by altering the values of R11,C2.

POWER SUPPLY

The majority of the circuit works on 5 volts, but the RS232 link requires +12 volts and -12 volts. In addition keyboards using the AY-5-2376 keyboard encoder also require -12 volts. The centre tapped output from transformer T1 is rectified by the bridge rectifier D1 to D4, and smoothed by capacitors C3,C4. Two 78 series and one 79 series voltage regulators IC23 to IC25 provide the required voltage levels, and are mounted on a heat sink. Capacitors C5 to C10 decouple the regulators whilst C11 to C27 decouple the p.c.b. circuitry.

PICTURE GENERATION

Before discussing the method of calculating the EPROM data it is worth considering the method by which a video display is generated.

Careful examination of a domestic television screen will show that the picture is composed of a number of horizontal lines. The picture is generated by an electron beam scanning the screen, line by line, starting at the top left-hand corner. The time taken to produce one complete picture or "frame" is 20ms, i.e. fifty times per second.

When a line is complete, the beam is returned to the start of the next line, during which time no information is displayed. This is also the case when returning from the end of

the last line to the beginning of the first. This is called "fly-back".

To generate the required picture, the intensity of the beam is varied according to the level of the video signal, thereby producing light and dark patches on a monochrome television.

Fig. 1.4 shows how the word "GLASS" is generated by the scanning beam. As the system scans line by line the word is built up by displaying a sequence of dots. First the top row of the characters is displayed, followed by the second row, then the third and so on until the characters are complete.

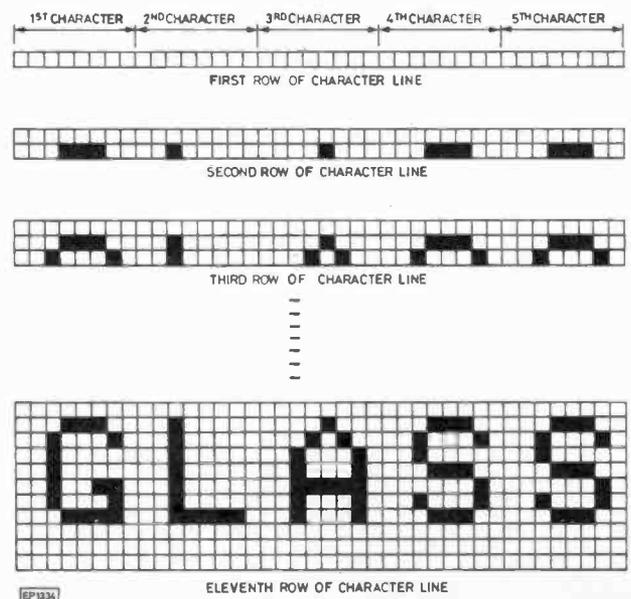
This sequence is repeated for a complete frame, whereupon the beam is returned to the top left-hand corner of the screen ready to repeat the frame.

CHARACTER GENERATOR EPROM

Fig. 1.5 shows the format for the character "E". As can be seen, the character is contained within a cell 8 dots wide and 11 dots high. For alpha-numeric characters columns 1, 2 and 8, and rows 1, 9, 10 and 11 are blank to provide inter-character spacing both vertically and horizontally. EPROM address lines A3 to A9 are provided by the latch IC8, and select which character is required. As each character consists of 11 rows, the row displayed is determined by the EPROM's A0 to A2 address lines; these are fed by the SFF96364's R0,R1,R2 outputs. However, the reader will have noticed that although the character displayed has 11 rows, only data for 8 rows is stored in the EPROM. The reason for this is that the SFF96364 provides the same data on the EPROM's A0 to A2 address lines for row 1 as it does for rows 9, 10 and 11. Therefore, whatever is programmed for row 1 will appear in rows 9, 10 and 11. Reference to the graphic characters shown in Fig. 1.1 will confirm this.

For normal alpha-numeric characters, row 1 is always blank, but this may not be so for graphic characters. A point to consider when using or designing graphic characters is due to the internal operation of the SFF96364. This is such that should a dot be present in the first column of the first character in a line, or in the last column of the last character in a line, it will produce a line to the left or right extremities of the screen respectively. A similar effect occurs if a dot is

Fig. 1.4. Formation of the word "GLASS"



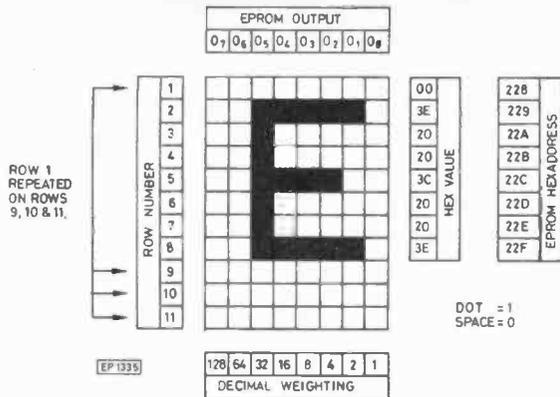


Fig. 1.5. Format of character "E"

present anywhere in the top row of a character on the top line of the display. In this case a vertical band to the top extremity of the screen will be displayed.

EPROM address line A10 is controlled by the SFF96364's cursor output (pin 15). This address line has the effect of dividing the EPROM into two sections, a lower half when A10 is low and an upper half when A10 is high. Reference to the EPROM's contents will show that all memory locations in the upper half of the EPROM contain the same value (3E HEX). Thus whenever a cursor is required a small horizontal line is displayed in place of whatever character was in that position. The cursor signal is switched at approximately 3Hz by the SFF96364 thereby producing a flashing cursor. The reader may alter the cursor format to suit his application by altering the data stored in the upper half of the EPROM, taking into consideration the restrictions described above regarding the design of graphic characters.

To calculate the eight data bytes required for a particular character, that character should be drawn in an 8 x 11 matrix, bearing in mind the above comments. The value of each byte is determined by adding the weightings for each dot in a row together and then converting that value to its hexadecimal form. The eight words are stored consecutively in the EPROM, row 1 first followed by row 2 and so on.

The address of the first byte is found by using the following formula:

Start address = ASCII character number x 8 where all values are Hexadecimal.

For example consider the character "E" (Fig. 1.5) start address = 45H x 8H = 228H.

CONTROL EPROM

It was stated earlier that the SFF96364 has the capability of cursor position control. Table 1.1 shows those available together with their respective ASCII control characters and execution times. In order to determine which cursor control is required, if any, the SFF96364 examines the status of its C0, C1 and C2 inputs. The tables also indicate which codes correspond to which facilities. These signals are provided by IC10 the control EPROM via its D0, D1 and D2 outputs. EPROM output D7 determines whether the ASCII character present is to be displayed or not; (logic "1" = print, logic "0" = inhibit).

A 2716 type EPROM has 8 outputs. With four used for cursor control, four remain to be used for the control of external devices, such as the BEL facility described earlier. As a 2716 EPROM has 2K memory locations and only 128 are used, one for each ASCII character, only the lower address lines, A0 to A6 are used, address lines A7 to A10 are connected to ground.

Should the reader wish to produce his or her own character set and/or control functions, the control EPROM should be programmed so that the memory location with the same value as the character's ASCII value contains the appropriate control byte.

For example, if the ASCII character "NUL" (00) were to be replaced by a graphic character, the byte stored at memory location 00H should be changed from 06H to 87H, the code for a normal printing character.

NEXT MONTH: Construction and testing is covered, along with how to drive additional features, and interface to the BBC microcomputer.

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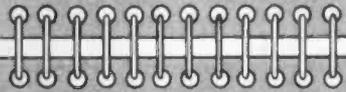
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INDUSTRY NOTEBOOK

By Nexus



Futurism

Beware the new pseudo-science *futurism*. It pretends accuracy in forecasting given adequate data input with computer processing. We already have this in economic predictions and apart from a very generalised trend, up or down, there is large disagreement between economists of different schools.

This is not to say that all economic forecasting is valueless. Clearly it is necessary to take a 'view' on the future when planning, whether it be on the simple level of personal finance, the complexities of government policies or that of multinational corporations. The trouble is that one has to make assumptions and hope they are reasonably correct. One may assume, for example, an average summer and predict an average harvest. But in 1983 worldwide there was a succession of droughts, floods, hurricanes which seriously distorted many economies.

Equally unpredictable for international trading nations is the impact of outside events which depend on people, even more unpredictable than the weather. 1983 saw the world in turmoil, the cold war accelerating, hot wars proliferating, default of debtor countries. And, on a more limited scale, the possible domestic traumas such as an upsurge in union militancy or even a political scandal which may embarrass a government to the extent of cabinet reshuffle and temporary loss of confidence.

With such volatility in local and world affairs it is doubtful that even the most powerful computer complex fed with the most accurate and up-to-date data can reliably predict the future from week to week, let alone ten years ahead which is what some advocates of futurism would like us to believe.

My prediction for 1984, unaided by computer, has one fundamental assumption and that is an absence of nuclear war. Given that, I believe that trade and industry will further recover, unemployment will marginally improve, people will still grum-

ble even though they are demonstrably better off. Electronics will remain the growth industry of the decade.

My long-term prediction is for a continued improvement in the standard of living. This view is based on historical projection which tells us that for the past 40 years our economy has been in 'crisis' every year and yet there has been consistent gain over the period measured in terms of home ownership, hours worked, holidays, pensions, longevity. There are always difficulties but they are always overcome. Short-term ups and downs when averaged out show steady gain in living standards.

Distributors

Electronic engineers like to be associated with genuine creative activity. To be a project leader or a member of a team responsible for a technical breakthrough or an acknowledged best-in-the-world product is something to be proud of.

But if your interest is just in making money then to be a humble peddler of components is the thing. An investor can also do well in the business. A recent listing revealed that £1,000 invested in Farnell in 1966 would be worth almost £103,000 today. Number two on the list is Diploma, another distributor, with old friend Electrocomponents fourth with £64,560 return on £1,000 invested in 1967. Of the manufacturers Rascal is leader with £75,000 for £1,000 invested in 1965. GEC is way down at Number nine and Plessey one from the bottom of the top twenty at Number nineteen with a return of £5,450.

In April 1983 Lex Service Group bought the Jermyn Group for £15 million cash. Such is the lure. Last October Lex spent another £3.5 million buying two distributors in West Germany.

I call them humble peddlers for that is what they are. The supermarkets of the industry. But like their high-street equivalents the profitable ones are those with the most sophisticated data-processing and management techniques for stock and credit control. High investment and high volume are the order of the day and fierce competition ensures good service to the industry.

There are still a few small distributors, mainly of specialised components, who might be categorised as corner-shops. They also exist on service, assisted by low overheads. It would be a pity to see them go.

Open Warfare

The price war in small business and home computers continues to intensify. And this before the Japanese are fully in the market and the IBM challenge yet to appear in the UK for another few months.

Texas Instruments has withdrawn hurt from the personal market having lost over 200 million dollars in nine months but stuck with having to honour 12-month guarantee periods on recent stock-clearance sales. The service operation must result in further loss as up to 20 per cent of some makes of machine (not necessarily TI) are reported to fail in their first year.

With prices tumbling by up to 50 per

cent it is clear that margins are being squeezed to the limit in the hope that increased volume will maintain profits. But already it would seem that some manufacturers are on break-even or less on the original purchase and relying on peripheral purchases later on to generate the real profit. Once a customer is hooked it is almost inevitable that he will want to enhance his system.

Futurism is rampant in this area. It automatically fails because the input data is suspect. A number of analysts are making projections, all with conflicting results. The biggest error is in claimed market share which when added up from the various manufacturers often exceeds 100 per cent.

Ma Bell and BT

The final break-up of AT & T, the giant USA telephone company, occurred on New Year's Day. It included divestiture of local Bell Telephone companies by the parent with consequent re-formation into several new companies.

Naturally, our own trade unions are attempting to equate privatisation of British Telecom with the break-up, by the order of USA courts, of AT & T. As part of their opposition to privatisation the BT Unions Committee has issued a report "The American Experience" pointing out all the difficulties and disadvantages of demolishing an existing monopoly.

BT responded by pointing out that privatisation plans for BT are quite different in kind and that most of the comparisons and conclusions in the report are misleading and confused. Sir George Jefferson, BT's chairman, is enthusiastic on privatisation which, he maintains, will free them from the web of government interference and control and is the best way to succeed in the years ahead.

Sir George's view on the unions is, "They are consumed with a nostalgia for a past that advancing technology and changing markets have made obsolete". And to ram the message home he quotes TUC leader Len Murray who is on record as saying "The countries with the highest standard of living are those which cope best with structural changes in industry".

The actual American experience will be watched with interest. Like our own BT executives, those in Ma Bell see the break-up of monopoly power, which also imposed restrictions, as a great new opportunity to expand and flourish. Time alone will tell.

Upturn

Recovery from recession continues unabated led by the USA's economy. The spin-off in electronics is world-wide. Motorola is spending £11 million on a fully automated IC packaging plant at the company's East Kilbride premises creating over 100 new jobs. The plant will package chips from Motorola production lines in Munich and Toulouse as well as the East Kilbride product. The revealing and encouraging fact is that the new plant is needed because Motorola's Far East assembly operations cannot keep pace with expanding demand.

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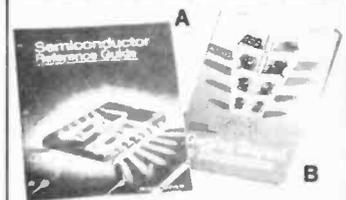
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CLOCK TIMER

T.J. JOHNSON

THE Clock Timer presented here enables any single appliance to be switched on and off at any time within a 24 hour period. The unit features a four digit clock operating in the 24 hour format, and a relay output capable of switching up to 10 amps at 240 volts.

The on and off times are easily programmed and may be verified at any time within the timing period. The timing period may be set to operate once only or repeated every 24 hours.

A typical application would be in conjunction with an electric heater, to switch on and off at predetermined times.

BLOCK DIAGRAM

The Clock Timer is based on the AY-5-1230 i.c., the details of which are given in Fig. 1. A simplified block diagram of this i.c. is shown in Fig. 2.

The set time logic takes the programming information from the input switches, either on or off times or clock time, and presents this information to the on/off memory or clock logic as appropriate. As the clock time approaches that of the 'on' time in the memory, various comparators detect this coincidence and switch the output on. A similar sequence occurs when the clock time reaches the 'off' time stored in the memory.

The switch marked repeat allows this timing period to be performed again after 24 hours. If this switch is not operated, the set times are cleared after the timing period.

Two l.e.d.s are provided to give the user an indication that on and off times are set and are currently stored in the memory.

CIRCUIT DESCRIPTION

The full circuit of the Clock Timer is shown in Fig. 3. The i.c. requires a supply of approximately 15V and this is given by the simple power supply consisting of T1, BR1 and C1. C2 and R21 provide the necessary 50Hz clock signal for the i.c.

The seven transistors TR1 to TR7 are segment drivers and are connected to the appropriate segments on the multi-

plexed displays X1 to X4. TR9 to TR12 are the digit drivers for each of the four displays. Transistor TR8 is the seconds indicator driver, and drives the two l.e.d.s D1, D2 at a pulse rate of once per second. The two l.e.d.s D3 and D4 are the off and on indicators respectively. These l.e.d.s illuminate when an off or on time has been set.

The last transistor, TR13, drives the relay which, via its single contact, supplies an output of 240V at the p.c.b. terminals.

The three switches S1-S3 are all centre off/biased both ways types and perform the following functions: S1—this switch in conjunction with S3 sets either the 'on' or 'off' times when placed in the correct position, or when the switch is in the normally off position and again using S3, sets the clock time; S2—this switch, depending on the position, either cancels the programmed times or turns the output on and off with each activation of the switch; S3—used in conjunction with S1 to set the various times. When in the normally off position the clock is allowed to run.

The last switch S4 is used to set the Clock Timer in either the 'once only' or the 'repeating' mode.

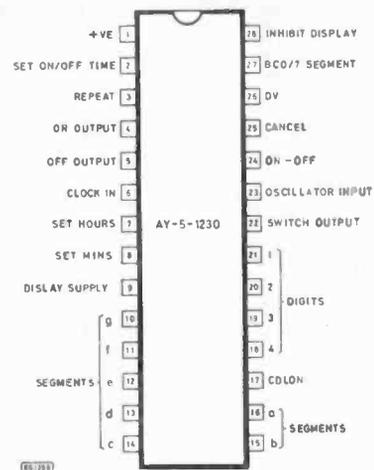


Fig. 1. The AY-5-1230 i.c.

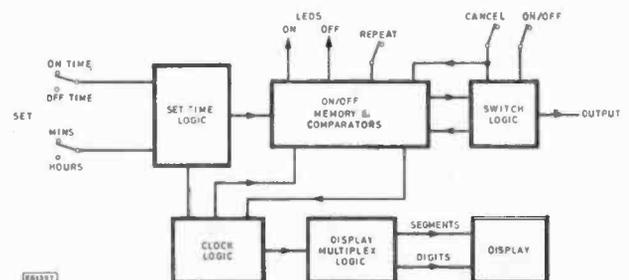


Fig. 2. Block diagram of the Clock Timer



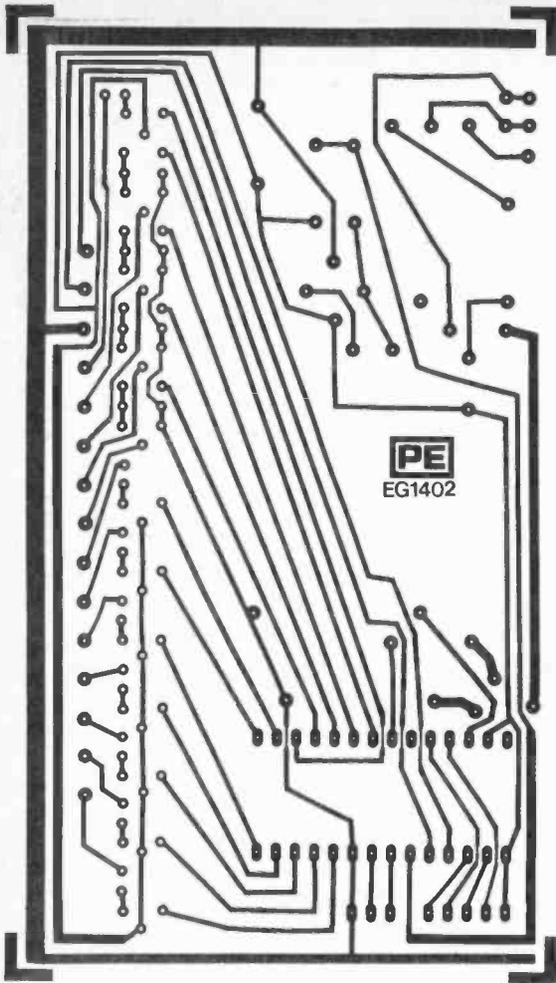


Fig. 4. P.c.b. design for the Main Board

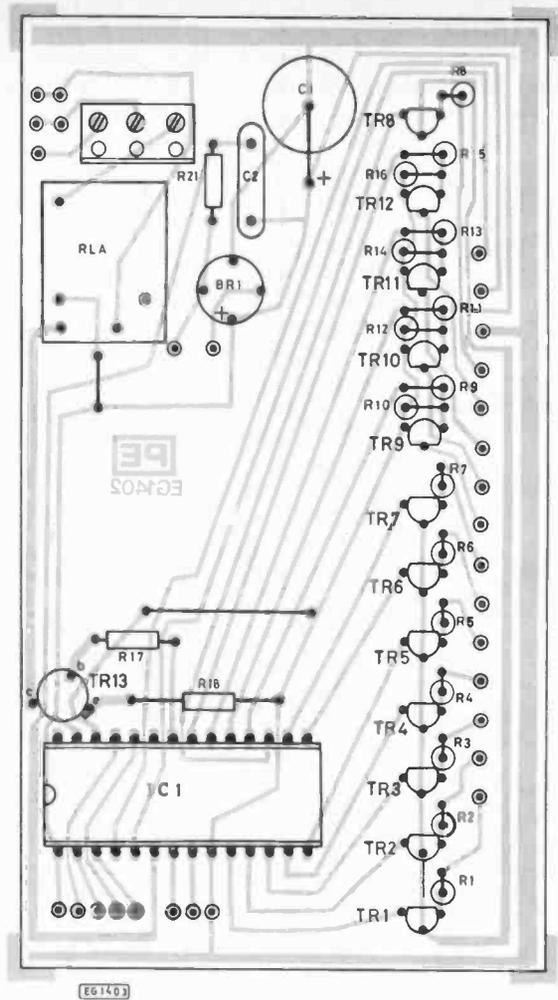


Fig. 5. Component layout of the Main Board

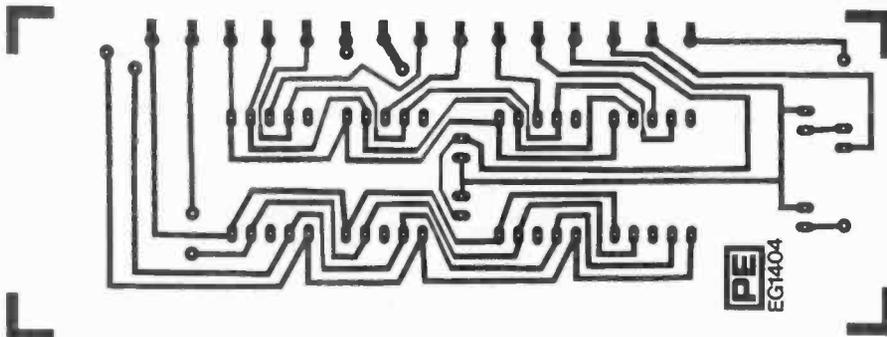


Fig. 6. P.c.b. design for the Display Board

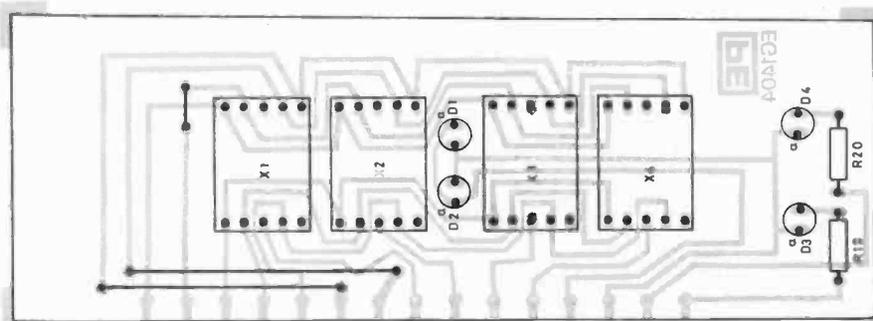


Fig. 7. Component layout of the Display Board

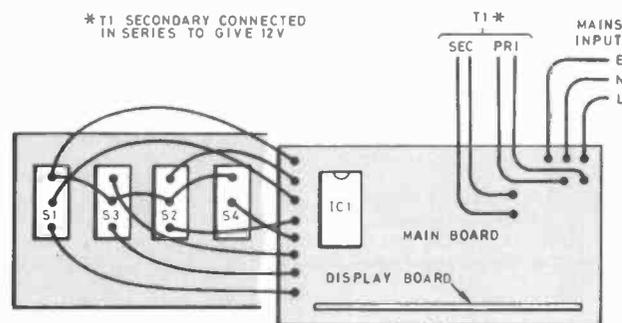
CONSTRUCTION

All the components with the exception of the switches are built on two small printed circuit boards; the track patterns and component layouts are shown in Figs. 4, 5, 6 and 7.

The two p.c.b.s are mounted at right angles to each other, with the display board being soldered to corresponding Veropins in the lower board. It is advisable to mount the two boards mentioned in the way described before any components are mounted. This is particularly important as the space between the transistors and the display board will not allow the middle pins to be soldered without damage.

Remember that the area around the relay carries mains voltages and should be checked very carefully after construction. The mains input lead may be soldered directly to the copper pads as in the prototype, or soldered to Veropins. In either case ensure that the three separate leads cannot touch each other if they are accidentally disturbed.

Finally the switches can be wired up according to Fig. 8, using, say three inches of ribbon cable. At this stage the switches are not mounted inside the case and the i.c. is not inserted into its socket.



EG1424

Fig. 8. Wiring diagram

CASE

For the case specified in the components list, the dimensions of Fig. 9 are exact. Check though that the transformer can actually fit inside the case and does not come into contact with any wiring or other components. A number of small holes may be drilled in the rear panel to allow for ventilation.

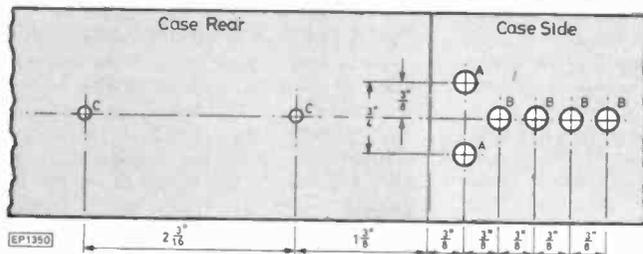


Fig. 9. Case drilling details

TESTING

The usual checks such as looking for solder bridges etc, should be carried out. This is particularly important in the region of the relay, as mains voltages appear here as soon as the Clock Timer is connected to the mains. One or two layers of insulating tape over this area will prevent any accidents.

Connect the Clock Timer to the mains and measure the voltage across C1. This should be about 17V or so, any higher indicates a fault and should be investigated. Next check the voltages on the pins of the socket. All except pins 1 and 27 should show little or no voltage with pin 6 at about 8V. Pins 1 and 27 of course should show the supply voltage.

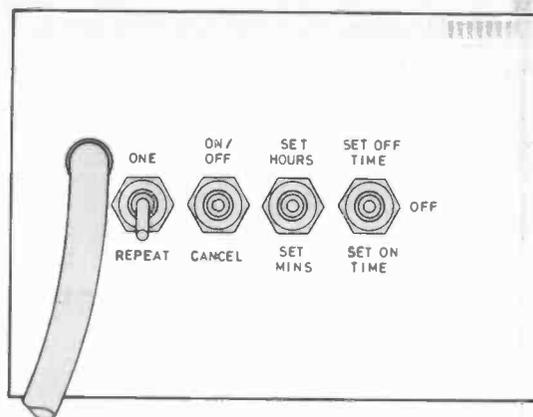


Fig. 10. Annotation for the switch bank

If all is well the unit is switched off and the i.c. plugged into place. Upon reconnection of the mains supply, the four digit display should illuminate and show '0000'. Operation of S3 to either position should start the clock and start the seconds i.e.d.s pulsing.

SETTING TIME

Assuming the clock is running correctly, the exact time may be set. Place S3 in the 'Set Hour' position, the hours should advance at twice per second. Release S3 when the correct hours have been reached. Next put S3 in the 'Set Minutes' position and allow the display to reach the desired time. Once again the display should advance at twice per second. During setting of the minutes, if the time required is accidentally passed, then the switch is held on and the display allowed to go round again until the correct time has been reached. Note, the minutes will not overflow into the hours thus causing the hours display to advance.

To set either an on or off time the following procedure is adopted. Set S1 to the required function, say 'Set on time', and while holding S1 in this position, use S3 to set the hours and minutes as described above. Once the correct time has been reached, both switches can be released thus setting the 'on' time. A similar procedure is adopted when setting the 'off' time, only this time S1 is placed and held in the 'Set off time' position.

Assuming both an 'on' time and an 'off' time has been set, the two i.e.d.s will indicate this fact by turning on. If only an 'on' time has been set then only the 'on' i.e.d. will illuminate, with the result that the output will switch off ten minutes later after the programmed time. This provides a foolproof method of operation ensuring that, if an off time has been forgotten, then no damage to the controlled appliance can occur.

To allow the Clock Timer to perform the programmed on and off times every 24 hours the repeat switch S4 is operated. To cancel the set times, S2 is operated once only to the 'cancel' position. Note that the times are not erased from the memory when cancelled, and although they will not cause the output to switch on and off, they may be recalled for further use. An example here is when the 'once only' mode has been selected but it is required for the Clock Timer to perform the same times a further time. To bring the times back into operation, S1 is set to both positions whereupon the two 'time set' i.e.d.s should illuminate, indicating the output will be switched at those times. This procedure can also be used at any time to check the state of the memory.

The second position of S2 allows the user to turn on or off the output at any time without waiting for the timer to switch the output. Each operation of S2 to the 'on/off' position turns the output alternately on and off. ★

SEMICONDUCTOR CIRCUITS

TOM GASKELL B.A. (Hons)

LED BARGRAPH DRIVERS (U2..B SERIES)

THE l.e.d. bargraph is a popular way of displaying rapidly changing information; it is often more rugged and versatile than an analogue meter movement, yet it can be easier to read when its displayed value is changing than a 7-segment readout.

In the September '83 issue we discussed the UAA 170 light spot driver, which proved to be excellent for driving many l.e.d.s as a moving bar, but was unable to produce a moving bar, or 'bargraph' effect. Furthermore, it was only available as a linear device, since the logarithmic version was being discontinued.

The LM 3914, LM 3915, and LM 3916 are popular i.c.s to use for these specific applications, although in turn they present their own particular constraints on the designer; they are expensive if only a small number of i.c.s are to be driven, and they are intended to drive the l.e.d.s in parallel, which can consume a great deal of power and limit the permissible current drive to very low levels. Although there are design techniques which can be employed to drive the l.e.d.s in series, these cannot necessarily be used in all circuit arrangements. Hence, although these devices are unsurpassed in many applications, there are some cases in which better alternatives are available.

These are the "U2..B" series from AEG-Telefunken, comprising the U237B, U244B, U247B, U254B, U257B, and U267B. They are all 8-pin d.i.l. integrated circuits designed for driving up to five l.e.d.s each in a series arrangement, which dramatically reduces the total drive current required. The voltage thresholds at which the l.e.d.s turn on are fixed, and while this can occasionally complicate the preceding circuitry, in most cases it makes the i.c.s very easy to design with.

THE FAMILY

The six integrated circuits are arranged as three pairs of devices; U237B and U247B are conventional linear law devices, U257B and U267B are logarithmic law devices, and U244B and U254B are 'overlapped' or smooth transition devices with a linear law. (The l.e.d.s fade in slowly, rather than turn on and off abruptly, giving an apparently smoother response). The thresholds of operation for the various i.c.s are shown in Fig. 2. Each pair of devices have their thresholds interleaved, so that each device can be used on its own or two can be used together, with common inputs, to drive ten l.e.d.s. (Each i.c. driving alternate l.e.d.s in the bar).

The pinout and specifications for the whole family are shown in Fig. 1. A number of the specifications have their figures taken from actual measurements made on the i.c.s in the applications circuit, due to the very limited information available from the manufacturers. The

nominal constant current feed to the l.e.d.s is specified at 20mA. In practice, this was measured to be 22mA, and hence the quiescent current of 23mA shows that the i.c. only consumes approximately 1mA over and above the l.e.d. driving current.

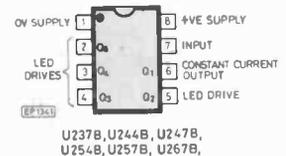


Fig. 1. Pinout and specifications for U2..B family

Characteristic	Notes	Min	Typically	Max	Units
Supply voltage		12	15	25	V
Quiescent current	(Irrespective of number of l.e.d.s driven)		23 *		mA
Constant current output	Drive current to l.e.d.s		20		mA
Hysteresis of comparators			10		mV
Constant current source voltage	Voltage between pins 6 & 8			2.0	V
Input bias current			-0.31 *		μA
Input resistance	Pin 7		40 *		MΩ
Variation in voltage comparator thresholds	Error in input voltage detection circuitry			±30	mV

* As measured on prototype

OPERATION OF THE CIRCUITRY

Fig. 3 shows a block diagram of the internal circuitry of the i.c. family. The only slight exceptions are the U244B and U254B, which have gradual transition comparators in place of the Schmitt trigger comparators. The operation of the circuitry is quite straightforward, if a little 'upside down' conceptually! D1 is the least significant l.e.d. (i.e. at the bottom, or the left hand side of the display) and D5 the most significant (top, or right of the display). With the input at 0 volts all the comparators are turned on, and hence all the driver transistors are turned on, so the current from the constant current source is sunk from pin 6 to 0 volts; no l.e.d. is turned on. As the input, pin 7, slowly rises in voltage, it reaches a point where the uppermost comparator in Fig. 3 turns off (because its inverting input voltage exceeds the non-inverting input voltage). Hence, the uppermost transistor also turns off, allowing the current to flow through

D1 then via the transistor connected to pin 5 to 0 volts. Higher input voltages cause successive transistors to turn off, allowing more l.e.d.s to turn on.

PRACTICAL CONSIDERATIONS

The supply voltage must be at least sufficient to allow for the total forward voltage drop of the l.e.d.s. This depends on colour and type, but is typically 1.8 to 2.2V for red, and 2.0 to 2.5V for yellow and green l.e.d.s. Allowance should also be made for the 2V maximum drop across the constant current source.

Typically, this results in a minimum supply voltage of 13V for red, and 15V for green or yellow, with a mixture of colours falling between these figures.

A decoupling capacitor must be provided between pin 6 and 0 volts; a 100n disc ceramic capacitor is ideal. Without this, spurious oscillations can cause several l.e.d.s to illuminate

	D1	D2	D3	D4	D5
U237B	0.2V	0.4V	0.6V	0.8V	1.0V
U247B	0.1V	0.3V	0.5V	0.7V	0.9V
U257B	0.18V(-15dBV)	0.50V(-6dBV)	0.84V(-1½dBV)	1.19V(+1½dBV)	2.0V(+6dBV)
U267B	0.10V(-20dBV)	0.32V(-10dBV)	0.71V(-3dBV)	1.0V(0dBV)	1.41V(+3dBV)
U244B	0.2-0.28V	0.38-0.48V	0.56-0.64V	0.74-0.82V	0.92-1.0V
U254B	0.11-0.19V	0.29-0.37V	0.47-0.55V	0.65-0.73V	0.83-0.91V

Fig. 2. L.e.d. illumination thresholds

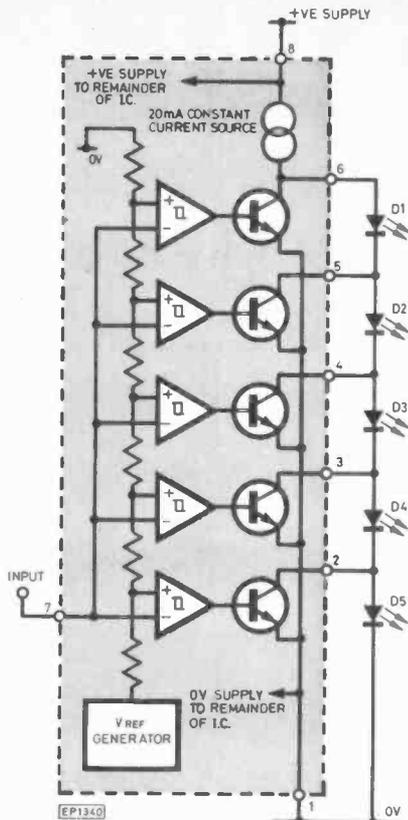


Fig. 3. Block diagram of driver family

simultaneously at the point of turn on and turn off of one of them.

Finally, although the input impedance is very high indeed, problems can arise with high impedance driving circuitry. A capacitor placed across the input, with a very high value resistor across it as a load, can be slowly charged up by the i.c.'s input, giving a false display reading. Typically, try to keep the driving impedance 100k or less.

Fig. 4 shows the circuit of a very simple audio level meter based on the logarithmic law i.c. U267B. (The ear's response to sound amplitude is approximately logarithmic, hence the use of this particular device). IC2 provides amplification of the input signal, and D1 rectifies it. This half-wave rectified signal is smoothed by C2, with R3 determining the attack time of the bargraph, and R4 with R5 the decay time. Note that the l.e.d.s are shown upside down, with D5 normally appearing at the top of the display, and D1 at the bottom.

Fig. 4. Simple audio level meter

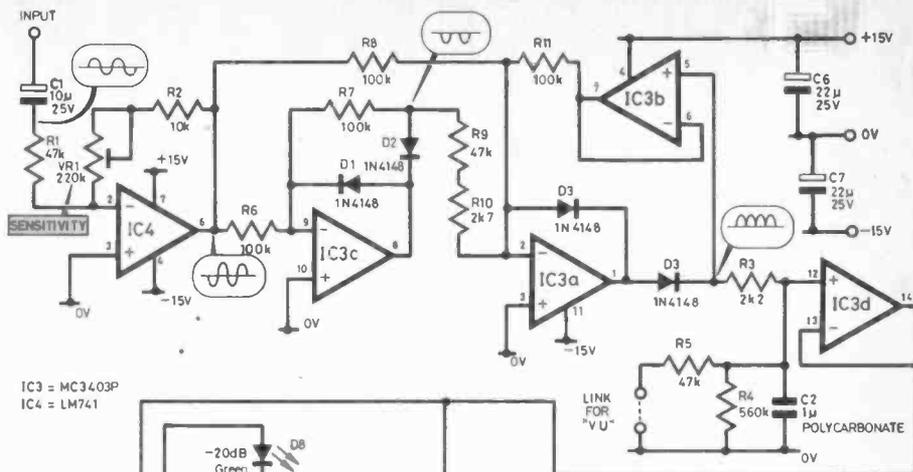
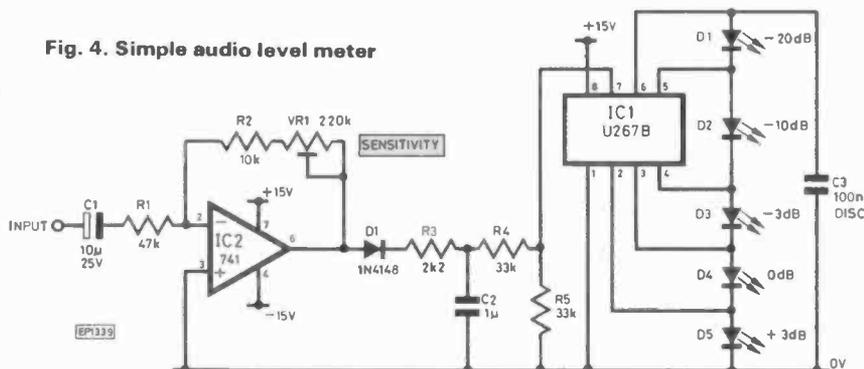


Fig. 5. PPM/VU meter with peak overload indication

APPLICATIONS CIRCUIT

Fig. 5 shows the circuit diagram of a sophisticated PPM or VU audio level meter, based on the principles shown in Fig. 4. To provide an accurate response to both positive going and negative going peaks of the audio signal, full-wave rather than half-wave rectification must be used.

Precision rectifiers based on op amps are used to overcome the inherent forward voltage drop which would be produced by a conven-

tional full-wave rectifier. Two precision half-wave rectifiers are used in series, IC3c, with D1, D2, R6, and R7 forming the first, and IC3a, with IC3b, D3, D4, R9, R10, and R11 the second. IC3a provides adjustable amplification of the input signal, and R9 in series with R10 adds the output of the first rectifier to the input signal (feeding into the input of the second rectifier) in the ratio 2:1. When summed together in this ratio, these two waveforms produce an inverted full-wave rectified signal. The second precision rectifier is used to invert this signal again, and charge C2 via R3, giving an attack time of approximately 2.5 milliseconds. R4 determines the decay time constant of the system, which is approximately 1 second, to correspond with the PPM (peak programme meter) characteristic used extensively in broadcasting. For a faster, more conventional, 'VU' decay, R5 should be linked to 0 volts. IC3b is used as a unity gain voltage follower in the feedback loop of IC3a, to prevent R11 having an unwanted loading effect on C2, which would cause the decay time to be far too short for a PPM characteristic. IC3d is another unity gain voltage follower which prevents the inputs of IC1 and IC2

from having any unwanted effects on C2.

IC1 and IC2 are used in a very conventional way, with the exception of the peak overload indication. When D17, the top i.e.d., is turned on, the output voltage on IC2 pin 2 rises above 1.5V. This turns on TR1, charging of C5 and turning on the *p.n.p.* Darlington pair TR2 and TR3. When D17 is turned off, the charge on C5 takes several seconds to decay away, so TR2 and TR3 remain turned on for a short while, illuminating D17 via D7 and R14. Hence, whenever D17 is illuminated at a 'peak', it remains on for several seconds after the signal amplitude drops again, giving an easily recognisable indication of 'overload'.

CONSTRUCTION

Fig. 6 shows the Veroboard layout of the meter. If used horizontally, the components should face downwards for correct orientation. Take care with the bending of the i.e.d. legs, since it is very easy to damage the devices themselves. The values of R3 and R4 (or R5) can be adjusted to give the dynamic characteristics required and the value of R1 or VR1 can be altered to change the sensitivity of the system. (Keep R3 above 2k, though, or IC3a will not be able to supply enough instantaneous charging current for C2). Most conventional, FET, or BIFET op amps will suffice for IC4, with a similar quad op amp for IC3. The transistors can be most medium to high gain types, but beware of different pinouts.

Although these applications show only the

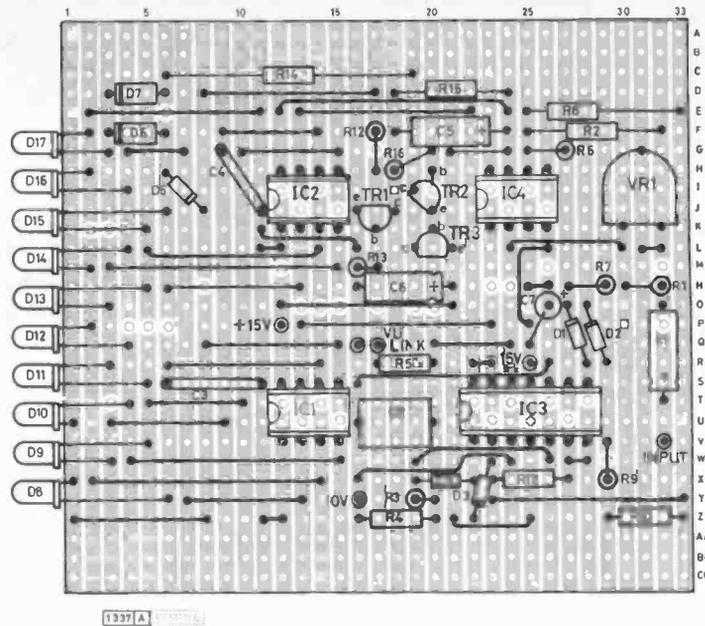


Fig. 6. Board layout of meter

logarithmic law i.c.s in use, the design of circuitry using the other i.c.s is directly comparable. The whole family is a useful addition to the range of i.c.s available for i.e.d. bargraph driving. AEG-Telefunken have just started incorporating some of the drivers with i.e.d.s all in one package; the D620P, D630P, and D634P. The basic i.c.s, though, probably

offer the greatest flexibility at the moment, and can be obtained from: **Coles Harding, 103 South Brink, Wisbech, Cambs, PE14 0RJ.** (0945-4188). The U237B and U247B are £3.36 each, the U267 is £3.30 and the others are £3.60 each. These prices include postage, but add VAT. (Minimum order is £10).

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Feature article...

INMOS The BRITISH chip manufacturer

PRACTICAL

ELECTRONICS

MARCH ISSUE ON SALE FRIDAY, FEBRUARY 3rd, 1984

STARDESK

Part Two
Peter
Newbury

IN this part final circuitry and constructional details of the board will be given.

MASTER DIMMER AND TIMED CROSSFADE

On the Stardesk, there are just two controls, the master dimmer/crossfader and the timer delay potentiometer (Fig. 8). The master control, VR7, is fed with 10V stabilised, and the output from the slider buffered and fed through a variable resistance VR5. If the timer control is set to minimum, then the voltage on C34 will follow that on the slider with a negligible delay. At full resistance, the voltage on C34 takes about a minute to catch up. TR24 presents a high impedance to the voltage on the capacitor to prevent inaccuracies occurring at high values of VR5, and the resulting output is fed to the first of two op-amps. Note that TR24 is a BC184 or similar high gain type. All the other transistors, with the exception of course of the f.e.t. in the audio section, are common or garden types. I have specified BC172, but almost any *n.p.n.* small signal device could be used. TR24 however, needs the maximum gain so that there is no voltage drop across VR5 when it is at maximum.

The op-amps are two sections of an LM3900 used to avoid the need for a further supply rail. The output of the first op-amp supplies the 'B' bus. This is the common feed to the preset sliders in the lower or 'B' row. The inverted output results in the 'A' bus for the top row of presets.

D52 and D53 monitor the outputs of the op-amps and are situated at the bottom and top of the master A/B slider respectively.

IC24 (Fig. 9) is a central switching point used to inform the static section as to which channels are performing what duty. Three of the address inputs (A0, A1, A2) receive information as to what channels have been selected for sequencing effects. The other eight inputs, A3-A10, are divided amongst the flash buttons. This input information is then correlated and the eight outputs fed to the 'C' switches in each 4016. Selection of any particular channel for a

sequence effect, or the operation of the flash button on that channel, disables the static dimmers for that channel.

It may seem a waste to have used over 70% of the 2716 for eight basic on/off operations, but since the principle of using the memory to route the sequence effects left the rest of the memory unused, and since wiring the flash buttons via the memory would obviate the need for additional circuitry around the buttons, the result was really a foregone conclusion.

STATIC SECTION AND OUTPUT STAGE

Fig. 9 shows the circuit of one of the eight left hand sections of the Stardesk. This circuit includes the two preset sliders, flash button and quad bilateral switches which, following instructions from the rest of the unit, decide what that particular channel will be doing.

Working back from the comparator stage, an op-amp, being one quarter of one of two LM3900s, the input current on the inverting input is compared with that on the non-inverting input. Since the ramp generated by TR2/3 in Fig. 1 has its highest value at the beginning of each half cycle of mains, the signal input to the inverting input of the comparator will have to be at a maximum for the output of the op-amp to go negative and switch the MOC3020 opto-triac (IC36-43). As the value of the ramp decreases through the half cycle, the qualifying input current at the inverting input falls, and the output stages will therefore trigger at lower signal levels, be they derived from the preset sliders, the sequential section, or the flash buttons. However, the lower the value of the ramp, the later in the half cycle is the triac switched, and the lower the total power fed to the load. Thus is the dimming action accomplished.

If the blackout line is at a logic low, which will be the case if the blackout button has been operated, no signal will reach the comparator through bilateral switch A. If the mixer is on, and switch A is effectively 'closed', the next obstacle to be considered is switch B, which is off when the strobe switch

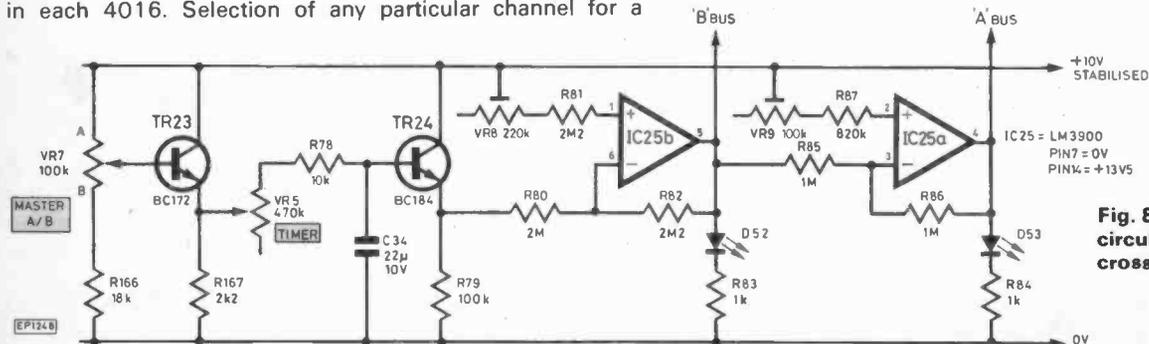


Fig. 8. Master dimmer circuitry and timed A/B crossfade

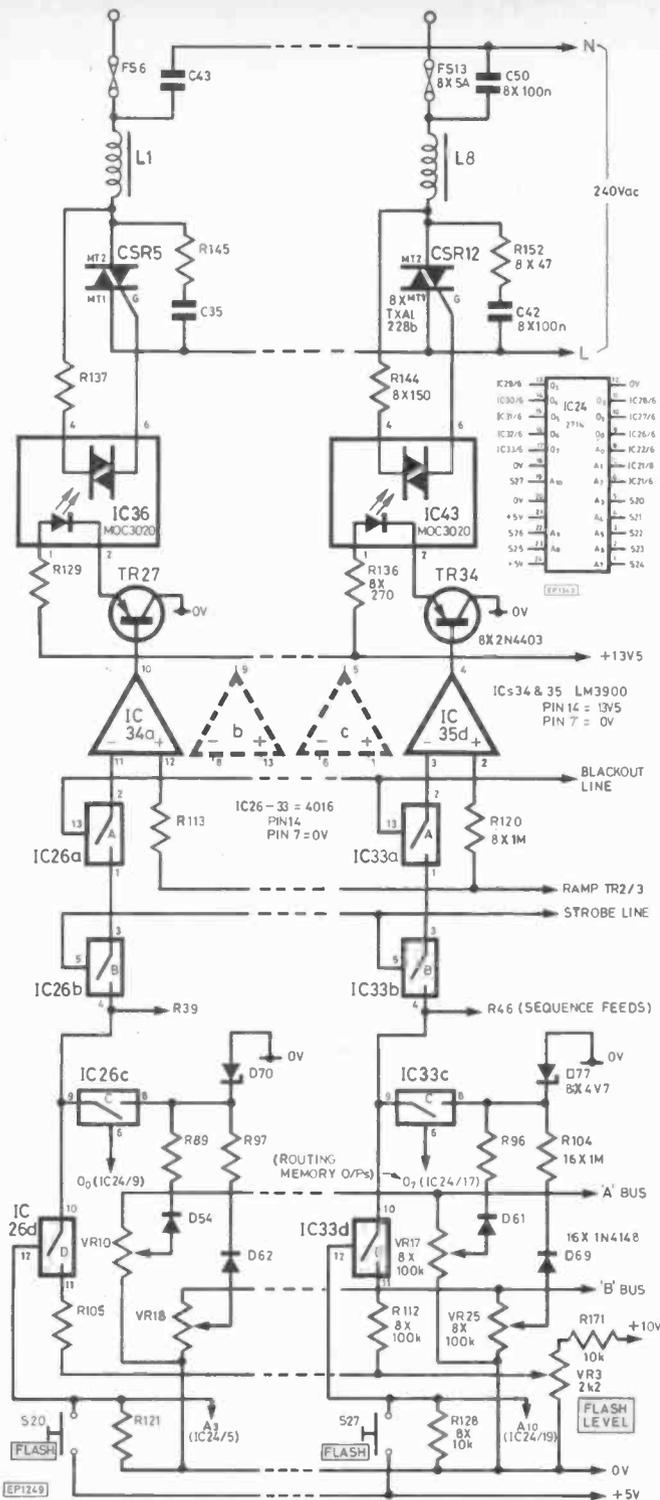


Fig. 9. Static section and the eight main outputs, the first and last of which are shown. The heavy current carrying neutral line is achieved on the board by reinforcing the track with heavy gauge tinned copper wire and ample solder. Note the CSRs are TXAL 228b

is operated, being connected directly to pin 8 of IC19 (Fig. 6). If the strobe function is not selected, and the control voltage on switch B is high, then the signal input to switch B may come from a variety of sources. If the channel in question is not part of a sequence group, switch C will be 'on' and the outputs from the preset sliders will be presented to the op-amp input.

If, on the other hand, that channel is part of a selected sequence group, then the control signal on switch C, which comes from IC24, the routing memory, will be removed and

the output of the slider presets replaced with the signal from the sequential circuitry. The feed resistor from the sequential circuitry does not interfere with the current balance mentioned since the base-emitter junction of the buffer transistor driving each of the 150k resistors is a diode in its own right.

A word about the eight Zener diodes, D70-77. The control voltages for the 4016 switches are all rather less than 5V, with the exception of the flash button, which provides exactly 5V to the 'D' section of each. I say rather less since the blackout and strobe lines are derived from TTL gate outputs and the routing memory outputs provide the fourth control signal.

For proper operation the supply voltage must therefore also be 5V. This in turn limits the maximum input voltage to each switch to 5V. The flash level input is limited by the potential divider comprising R171 and VR3; the sequence input could never rise above about 4V, and the only problem is therefore the slider outputs. When the sliders are in operation there is no problem, since the inputs and outputs of switches A, B and C are all at the potential of the op-amp input, viz 0.5V. When the dimmers are disabled, however, the input voltage to switch 'C' can rise to nearly 10V if either slider is at maximum. This will cause faulty operation of that section of the 4016, with part of the signal being leaked through to the op-amp input. The input to switch 'C' is thus clamped by the Zeners to within the device operating limits.

AUDIO SECTION

Although the audio section (Fig. 10) has a balance control, this is merely for fine adjustment, the input stage comprising an AVC amplifier. The input signal may be from a few hundred millivolts to in excess of 50V, depending on the choice of input resistor. With the link wire behind the earth terminal in place the input impedance is 1M, and the maximum input signal for proper operation is about 5V. With the link cut, or removed, the input impedance is 10M and the higher range of inputs acceptable. The output of the first op-amp, one of the remaining two sections of IC25, is taken to the balance control, but is also rectified to provide d.c. bias for TR35. TR35 is used to shunt the feedback path comprising R160/161, but, as the bias increases, its effect becomes less and less, and the gain of the stage reduces. The balance control serves to compensate for the necessary difference between the outputs of the op-amp for low and high input signals, without which difference the bias on the f.e.t. would not change. The control also provides a degree of latitude to meet the personal whims of the user. The slider of the balance control is taken to the final half of the LM3900, IC25c, the gain of which is arranged so that the output is fairly heavily clipped. This output is then rectified and a small degree of smoothing applied via C54. This capacitor is somewhat arbitrary in value and could be changed, if required, to suit personal preferences.

Having obtained this audio derived chain of pulses, the signal is routed as follows: a three way electronic switch similar to the routing bank described earlier comprises ICs 44, 45 and 46. The first two are quad NAND gates, and the third, because a three input gate is required to produce the reset pulse, is a 74LS10 (triple three input NAND gate). Unused inputs are tied to supply positive. The audio signal is taken to two gates of IC45 and the other gates taken to the outputs of the chase and halt flip-flops not connected to the l.e.d. indicators. When a particular function is selected that output will be high, and, when the audio signal is also high, the appropriate gate will give a low output. For the chase effect, the output of IC45a pulls down, through D15, the enable input of the second section of IC11, advancing the count rate and eventually the sequence. Since the audio

derived signal, is not heavily smoothed, the rapidity of pulses from that circuit causes the 4520 to be clocked often and the sequence then advances with the music.

Earlier it was mentioned that some good effects may be obtained using the chase function. This is because, although the sequence is advanced in this manner, the number of pulses at the OE input of the sequence memory is unchanged and thus clever manipulation of the speed and attack controls will decide whether the chase effect is sharp and positive, or more gentle and relaxed. When the audio halt function is selected, IC45d operates, producing an active low signal which is then inverted by IC45b and applied to the clock input of the same 4520 counter via the blocking diode D16. R33 and C18 (see Fig. 4) provide a time constant, without which the effect of the train of pulses would not be cumulative and would not therefore produce any noticeable effect.

When the 'off' button is depressed, the outputs of each of the gates IC45a and IC45d are held high and any audio effect is cancelled.

CONSTRUCTION

With the exception of the suppressor chokes, which are too heavy to be mounted and are instead encapsulated in a tray behind the board, the whole mixer, including power supply and output stage, is assembled on one double sided p.c.b. To avoid the possibility of shorts, and bridges, bearing in mind the close proximity of components, both sides of the board on the author's unit were printed with solder resist. The board offered by the supplier in the parts list is also prepared in this manner. The saving in time spent finding shorts and the like well exceeds the small cost involved in this process.

As far as the case is concerned, whilst it is certainly possible for the constructor to make his own, if he has the tools

at hand, cutouts are specialised, particularly for the switches, which have rectangular pads with rounded corners. Thus the ready-made and printed panel and case are recommended.

Fig. 11 shows the component layout, looking at the top side of the board. Not all of the components are topside mounted owing to the dictates of space and also because of the height of certain components. Amongst the components that are rear-mounted are C3, C6 and C59. C6 is not only rear-mounted, but rear-soldered as well so the leads will have to be left a little longer to facilitate this. If a lot of vibration is anticipated, C6 may be taped to C3.

In the underside layout one value of slider is used, this explaining the use of a buffer transistor on the crossfade control, and the need for a Darlington buffer on the effects master, when a lower value control would have done away with the first transistor. In the same manner, because the rotary controls used are of the 'through-board' variety and not freely available, only two types, 2k2 and 470k, were used. Hence the need for an extra resistor on the attack control. All the triacs used are 8A rated and must have isolated tabs, since they are mounted to a small subchassis *cum* heatsink which is in turn bolted to the case proper.

When assembling the board, it is a good idea to insert and solder the terminal pins in the output stage first, since these are a tight fit. Fitting these first will preclude the gnashing of teeth when other components are inadvertently broken. Start with the lowest profile components, such as resistors and diodes first. Next fit the medium height components such as transistors and then the i.c.s. Note that R54 has one end terminating under IC33.

The layout of the transistors shows the emitter, base and collector connections clearly. The shape of the case is only an indication and will not necessarily agree with the device package obtained. All i.c.s, with the exception only of the

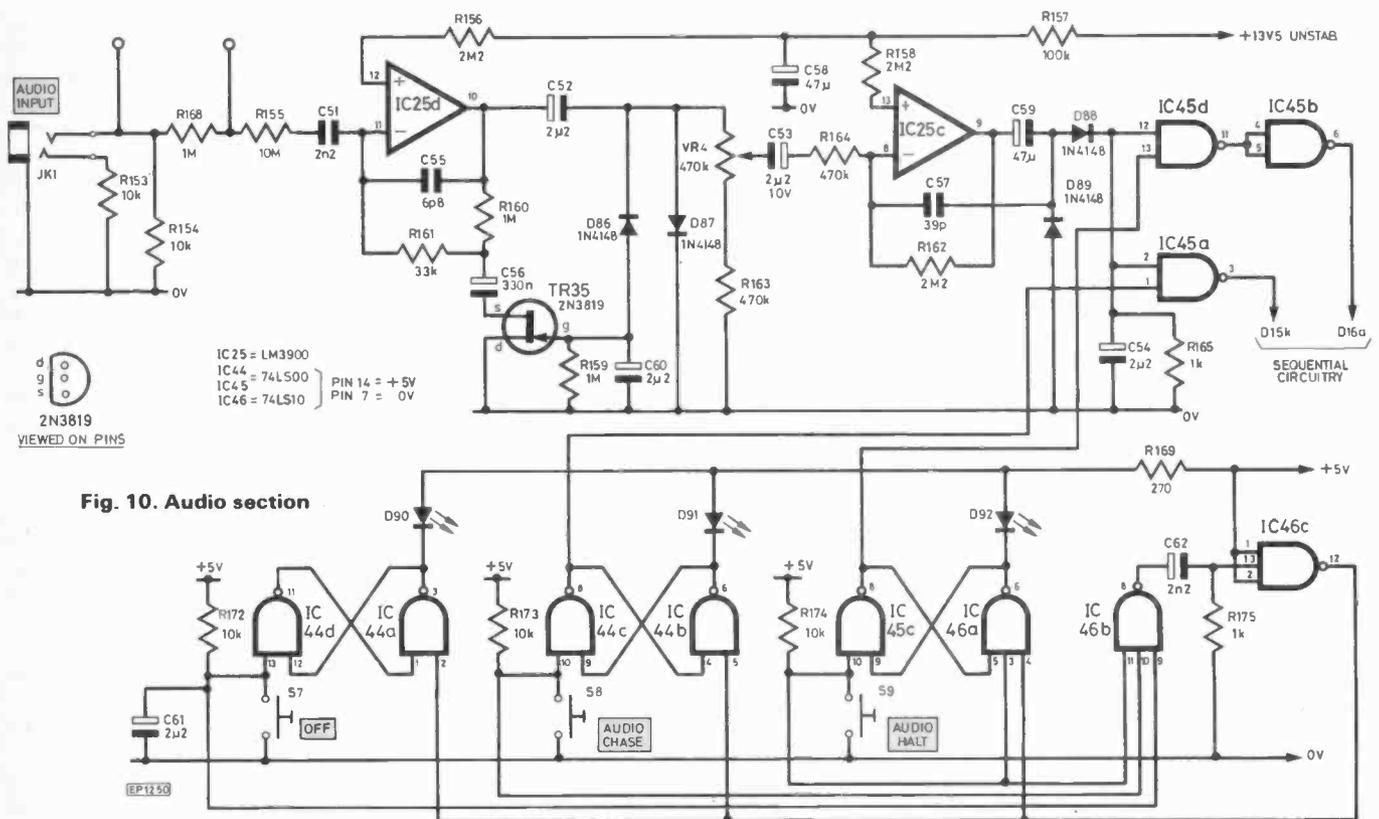


Fig. 10. Audio section

T = SPADE TERMINAL (MOUNTED WITH SPADE AT REAR OF BOARD)

⊙ = 1.3mm TERMINAL PIN MOUNTED THROUGH BOARD FROM FRONT

⊙ = 1.3mm TERMINAL PIN MOUNTED THROUGH BOARD FROM REAR

* = COMPONENTS BEHIND BOARD

⊙ ALL TRs EXCEPT TR35

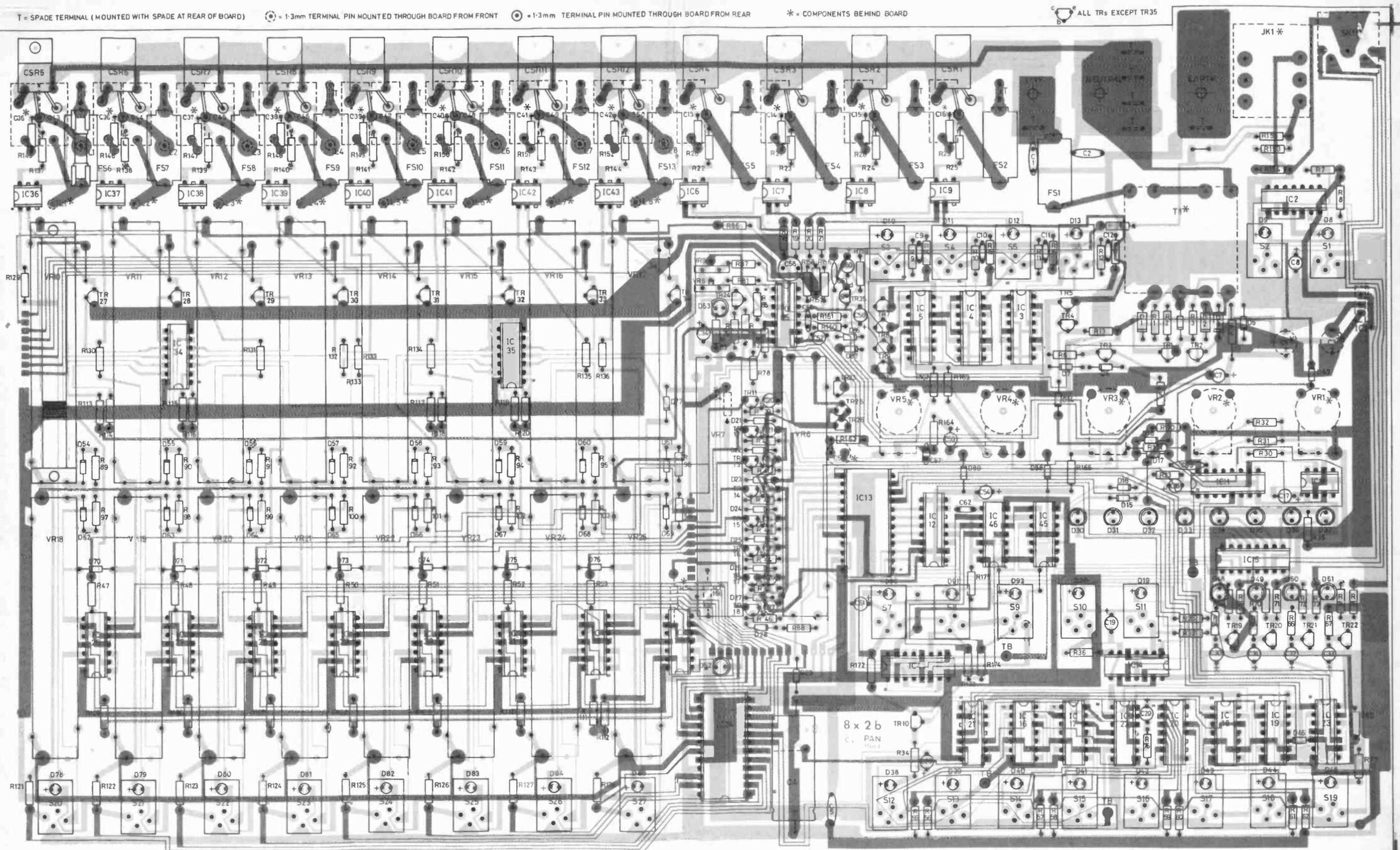
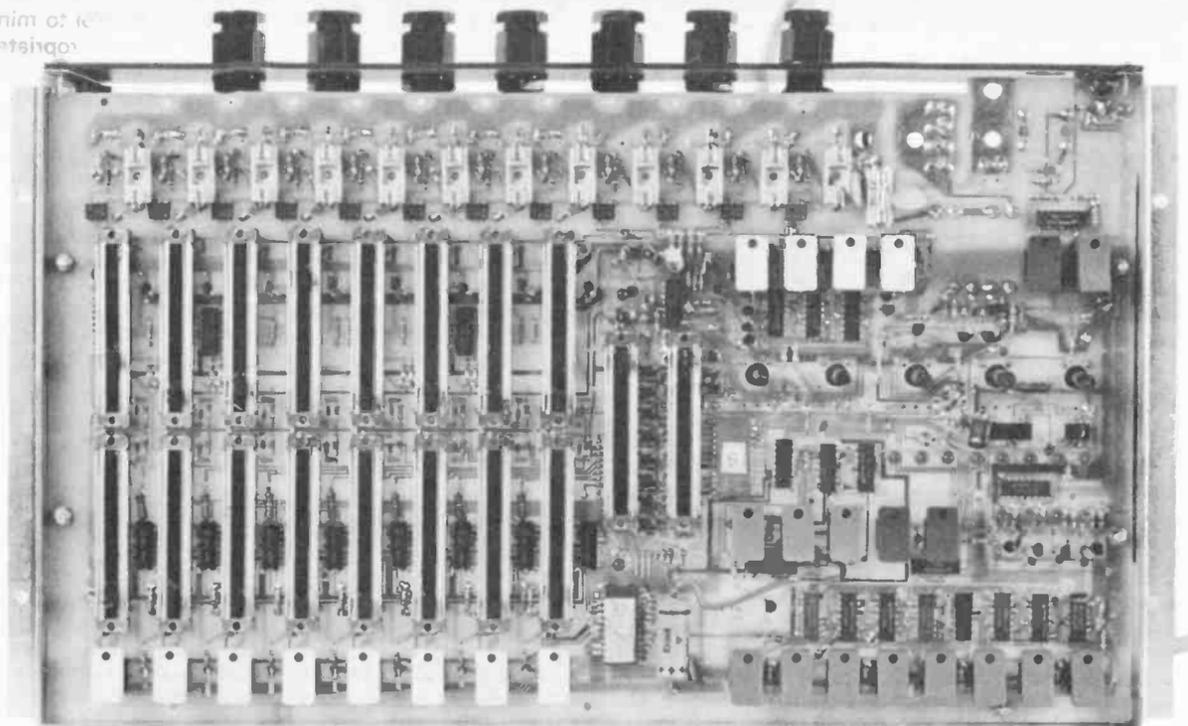


Fig. 11. Component layout

EP142 EC120



Board assembly

and neutral inputs and connect to the mains, via an isolating transformer if at all possible; if not take care.

It is a good idea to have the front panel at hand to identify the controls. Check immediately for 5V on the output of the 7805, and 10V on the cathode of D5. If these voltages are not in evidence you must find out why before proceeding. If all is well check that the supply positive and ground terminals of all the i.c.s are at the correct potentials. Now, assuming all is still well, observe which i.e.d.s are lit. The blackout lamp should be lit, and since operation of the unit stems from this pair of gates, any malfunction here should be investigated first. Check the operation of the 'Mixer on' and 'Blackout' switches back and forth. Next, the programme routing group of switches. The 'Off' i.e.d. should be flashing. If it is not, check the 'Sequence speed' control and advance to maximum, since in the lowest setting the 'Off' lamp will stay off for long periods. The 'Off' lamp should flash. Now check the operation of the other eight buttons, paying no attention at this time to what the rest of the unit does. If all is in order press the 'Off' button again. The 'Audio off' i.e.d. should be alight. Check operation of the two audio effect switches and again return that section to the 'Off' mode. The programme select i.e.d. should be lit, as should one of the eight programme selected i.e.d.s. Check that the programme indicator advances one position with each depression of the manual button. Check that the auto function can be selected and then return to the manual mode. Although no circuitry is incorporated to set the independent sections to 'off' on switch-on, experience so far has shown that this is invariably the case. Operate each independent switch in turn, when the corresponding i.e.d. should illuminate at substantially less brilliance than the other i.e.d.s illuminated so far. It is a good idea at this point to check that the zero voltage pulse is in evidence on the collector of TR1 (scope at 20ms and 5V/cm) and that the pulse is arriving at the clock input (pin 5) of IC5. At this stage operate the 'Mixer on' switch, with all four independent outputs switched on. The i.e.d.s should now come up to full brilliance. Leave the independent circuits switched on since

you will need to check correct operation when the strobe function is brought into play. Leave the mixer in operation, i.e. do not operate the 'Blackout' switch again.

It is worth mentioning here that one should keep a good eye on the blackout and programme routing switch i.e.d.s in particular when working on other parts of the board. A temporary short, or the earth lead of the scope dropping off, or some similar disturbance may well cause these circuits to reset. In the case of the bottom row of switches, there may be no i.e.d. on at all, due to a reset pulse being generated whilst there is no switch depressed. The same may happen with the audio section. Once in normal operation the desk will not however be disturbed by external influences.

On the subject of oscilloscopes, it is not absolutely essential that one be used for checking. If the desk does not work first time round though, a scope will be found to be invaluable. Remember when using such a piece of equipment around the area of the 4016 bilateral switches that the impedances are in the orders approaching megohms, and that the op-amps are current operated. A scope having an input impedance of 1 megohm (quite typical) will produce false readings and incorrect operation of the desk if connected in the wrong place. The same applies to many test meters.

SETTING THE STATIC SECTION

The next step is to set up the static section. Reduce the crossfade time to its lowest setting, move the A/B master slider to the lower (B) setting and adjust the preset VR8 until the voltage on the 'B' bus, which is the line connecting the top ends of the lower set of sliders, is at 10V. Move the A/B slider up fully to the 'A' position and repeat the process for the 'A' bus adjusting VR9. Checking first, as mentioned above, that the mixer is still 'on' and that the programme routing is set to 'off', advance all the 'A' sliders in turn, when each i.e.d. should illuminate. For the time being we will not worry about the exactness of setting up, since the initial setting up is merely to aid us in checking that the unit is

eight main MOC3020s, are soldered both sides of the board. Take extreme care to avoid bridging pins together.

CHIP PROGRAMMING

It could be that some constructors intend to program the two chips themselves if they have a Softy or similar machine available to them, and wish to put off the task for a while. In that case it would be wise to leave out the 'Effects master' slider and C4 to facilitate ease of installation of these devices. The programmes for the two memories are available on application to this magazine. Alternatively they can be bought programmed.

Before soldering the sliders in place note that R84 is soldered under VR7. Ensure that this is done before fitting VR7. Note also the polarity of the sliders. There is only one correct way to fit these and that is so that the support lugs locate correctly.

Be sure to fit the 'X' rated capacitors, which are rear mounted, before soldering the triacs to the terminal pins, since the solder joints for the capacitors are under the triacs. For that matter, it is a good idea to leave the fitting of the triacs until the board is actually in the case, since the soldering of the leads after the triacs have been screwed down will obviate resoldering and realigning later and possible damage through stress and strain.

The keyboard switch sets come in three pieces plus, of course, the i.e.d. These are the switch proper, a i.e.d. holder into which the switch fits, and a push on rectangular keypad. For ease of assembly and to avoid possible error, the board layout is such that all the switch i.e.d.s are mounted round the same way, i.e. with the anode to the right. The anode is usually the longer of the leads, but this should not be assumed to be the case as not all manufacturers follow this standard and it can be very annoying to find some or all of the i.e.d.s inserted incorrectly when the unit is turned on, apart from the risk of damage to i.e.d. and switch alike when one attempts to reverse the diode. To check, look into the i.e.d.; the cathode is the lead with the larger, triangular end to it. All diodes on the layout diagram are shown with the cathode marked +. This corresponds to the banded end on the 1N4148s, 1N4000, and Zeners and to the short lead on the i.e.d.s. It does not indicate the +ve terminal for the i.e.d.

HOLE ROLES

Note the three sets of '10 in line' holes; one set on the far left of the p.c.b., one immediately to the left of the A/B crossfade slider and the third, running horizontally, immediately below the A/B and effects master sliders. These were included in the board layout for the convenience of the author, and are in order to provide for a feed to a slave unit from the driver transistors TR27-34. Holes are already in the board for fitting a drive resistor for a duplicated output stage. The resistor should be 330 ohms, assuming that the slave unit, which should have its own 12V supply, has no indicator i.e.d.s. If these are to be included, the resistor should be lowered to 270 ohms.

The second set of holes are a convenient test point for the output of the sequence section and are also outputs for possible expansion of the desk. The third set have the first three holes obscured with through board connections, but in total comprise the essential information for the bilateral switches, plus the outputs of the routing memory, IC24. Again, they provide handy test points. In the event of the desk being expanded, these latter two sets of holes would be fitted with Molex p.c. connectors, which would also act as through board connectors where required.

The four large holes in the p.c.b. in the region of the mains inputs are for 18 or 25mm M6 bolts which should be fitted with washers both sides of the board to encourage current distribution. To these are fitted crimp terminals to facilitate mains live, neutral and earth connections. The board neutral track should be reinforced with a 16g length of tinned copper wire soldered at either end. The soldering should be liberal, and should encapsulate the wire, which should extend along to the live input terminal. The idea of this is to provide the best current handling possible for the feed to the triacs. At full power on a resistive load, the right hand end of this track carries 50A. This should be borne in mind when arranging a power feed to the unit; a 13A wall socket is only good for 250 watts per channel!

The output stage section is rated at one kilowatt per channel of resistive load. Having said that, this figure should be derated to 750 watts per channel if using tungsten halogen lamps, which although resistive, have high operating temperatures, and consequently a very low cold resistance. This does not matter so much when using the static section since the changes in output to the lamps tend to be gradual, but is important when using the sequencer section, since the low cold resistance means greater surge currents on turn-on and thus a far greater I²t loss in both the triacs and along the track to them.

When the mains transformer, which should be the last item fitted, apart from the triacs, is in place, the constructor may then like to observe his or her handiwork and decide whether to test the unit before fitting it in its case. Bear in mind that although the output stage cannot be checked at this point, the rest and most complicated areas of the board are rather more accessible when the board is not in the case. In fact, once the desk is tested and any gremlins dealt with, it is quite easy to service in the case, simply by removing the front and rear panels. As mentioned at the beginning of the article, the triacs and fuses are actually accessed without dismantling the unit. For initial faultfinding, though, the board is probably better off free on the bench. Do please remember that the top portion of the board is live on both sides regardless of the absence of the triacs. If you are using the case assembly offered in the parts list, it will have a tray behind the front panel into which the chokes locate. At this stage it is a good idea to pot these into position using a polyester resin, or, if you are feeling rich, silicon rubber compound. The author used polyester resin and considered it quite acceptable. The suppression chokes comprise, basically, as many turns as possible of heavy gauge wire wound on a laminated core. It is possible to make these yourself if the laminations and suitable wire (at least 0.8mm) are to hand, but in the long run it makes for a considerable saving in time and effort (have you ever tried to wind heavy gauge copper wire) to use the ready made ones available as shown in the parts list. These have self soldering leadouts and therefore scraping is not required.

TESTING

Assuming that both memories have not been fitted and completing assembly, start by checking for shorts on the three supply lines. Also, since the board is not yet in the case, attach a small heatsink to the 7805 regulator. If nothing else is available, a 2p with a hole drilled in it, or a pipe clip, will do (a plastic pipe clip will not). Move all the channel sliders to zero, and just before turning on have one last check for bridges, shorts, and equally important unsoldered joints, and that the through board links are in place (eight including the three below the A/B slider) since the continuation of supply and ground lines around the board rely on such connections. Connect a pair of wires to the live

basically correct in operation. Furthermore, do not be concerned that the l.e.d.s illuminate quite brightly early on in the raising of the slider. The important matter is the proper operation of the output stage and to get a true representation of output stage condition via a l.e.d. would necessitate much more circuitry, since the illuminance of it is dependent only on the current passing through and thus tends towards being linear. The load on the output however is receiving power that increases on a square law basis, ignoring lamp ballistics etc. If the l.e.d.s do not illuminate, or come on immediately, check the ramp waveform at the emitter of TR2 and that it is arriving at the op-amps. When doing this the scope should be set on d.c. to check the position of the ramp relative to zero volts. Gradually move the A/B slider to the 'B' position and observe that all channels dim to zero uniformly, then advance the 'B' sliders to maximum and check for correct operation. Leaving both sets of sliders at full, press the 'Blackout' button. All eight l.e.d.s should extinguish and the independent circuit l.e.d.s should dim, showing those channels to be in the standby mode also.

Switch the mixer on again and press the second button in the programme routing group. This button routes the sequence to channels 1-4 and the dimmers on those four channels should now be disabled, whatever their setting, and instead a sequential effect will be displayed. This is best checked initially with the speed and attack controls at maximum. Select each of the eight programmes in turn, using the 'Manual' button and then press the 'Auto' button. The programmes should now cycle through automatically. The dimmers should still be functional on channels 5-8. As well, check the next four switches, shifting the four channel programme to channels 2-5, 3-6, 4-7, 5-8 in turn, and finally operate the seventh switch, marked 1-8, which should disable all the dimmers and put in instead an eight channel sequence. It is worthwhile, at a later time, when all the rest of the basic functions have been checked, to check each and every programme in each and every mode of operation, since they are all in different sections of the memory e.g. just because programme No. 4 is correct on channels 1-4 does not automatically mean that it will be correct on channels 5-8, or for that matter in the strobe mode. And so indeed to the strobe button on the far right. Depress this, and all the dimmers should be disabled. Similarly the independent circuits should be seen to be on standby by virtue of the reduced brilliance of the indicator l.e.d.s.

The selected programme should now be indicated on the strobe l.e.d.s, and the display will take the form of flashes owing to the differentiating effect of the resistor capacitor combination on each output of IC23. Fill and empty routines are pointless for strobes, and the effect of the strobe circuitry is to reduce all such programmes to straightforward chase effects. This results in similarity between some strobe sequence programmes which could only be avoided by having yet another set of programmes. This was felt to be unnecessary.

At this stage check that the pulses appear at the output DIN socket at the back top edge of the board. The pin connections are given in Fig. 7.

Operate the 'Blackout' switch and check that the strobe function is disabled along with the other facilities.

Switch the mixer back on and select the programme route 1-8. Adjust the sequence speed to about one change every 5 seconds and then gradually reduce the setting of the attack control, noting the fading up and down of the l.e.d.s.

Switch the programme routing off, and return the speed and attack controls to maximum. All eight channel l.e.d.s should now be on fully, since both sets of sliders are at the

top of their travel. Set the 'Flash level' control to minimum and press each flash button in turn. The appropriate l.e.d. should extinguish. Now, depressing and releasing any button continuously, rotate the 'Flash level' control gradually, noting the increasing level of brilliance of the l.e.d. in question. It is not really necessary to repeat this on the other seven channels, since you have already confirmed that each channel is receiving the 'flash' signal.

Set the programme routing to 1-8 again, and apply an audio input which is in keeping with whether the wire link is in position or not. Initially it will be best to choose a level somewhere in the middle of the operating range. Set the 'Sequence speed' fairly slow, and with preferably a signal input having some 'light and dark'. Press the 'Audio chase' button and note the chase effect. Raise the speed to maximum and now operate the 'Audio halt' control, again finding the optimum setting using the 'Audio balance' control. The sequence will temporarily halt with the beat of, or with crescendos in, the music. If the setting of the balance control is too high the sequence will tend to stop for excessively long periods.

TIMED CROSSFADE CHECK

All that remains now, before the final assembly is done, is to make a final check of the static section. First though, check the operation of the timed crossfade by advancing the timer control to maximum, and then performing an A/B crossfade at normal speed. The A and B indicator l.e.d.s should undergo the A/B transition in 10 seconds or so. To ensure that any variation in timing due to component tolerances errs on the high side the calculations for the timing components were generously on the upper side of 10 seconds and it will probably be found that for a 95% crossfade, 15 seconds will be achieved. Rotate the timer control back to the minimum setting and, taking each channel in turn, perform the following checks. Reduce the 'A' and 'B' sliders to zero, with the crossfade in the 'B' position. Connect the scope to pin 2 of the appropriate MOC3020, and set as before, and confirm that it is switched to d.c. operation. If a scope is not available, the tests will have to wait until final assembly has taken place. The only signal observable should be the ripple on the supply, at about 13.5V. The signal should not change until the 'B' slider is advanced about 5% of its travel. This is to allow a margin at each end of the track. As the slider is advanced a narrow rectangular wave will appear, increasing in width until, at approximately 5% from the top of the track, it has disappeared, showing the output of the op-amp and driver transistor to be completely switched. Return the 'B' slider to zero, move the crossfade control to the 'A' position and repeat with the 'A' slider. Remember that any adjustment of the presets must start with the 'B' preset, and not the 'A' preset, since the 'B' preset defines the range of voltage scan initially. Having done this, set both controls at halfway and move the crossfade back and forth, making an adjustment to one or the other slider to achieve the same mark space ratios for both 'A' and 'B' controls. During the transition there should now be no, or negligible, dip or reduction in the width of the waveform when the crossfade is central. It is possible that when the two sliders are set very near the bottom end, say 10% of travel, that a small amount of dip may be noticed. This can be ironed out with an amount of playing around, but in practice such cheese-paring adjustments are not necessary.

This all sounds rather long winded, but having set the first channel up correctly, which in fact only takes a minute or so,

it only remains to check that the other channels are in fact operating in the same manner. If one is not, suspect a wiring or component fault rather than faulty operation due to tolerances. As a final check, which need not be made on all channels, ensure that advancing the timer control to maximum whilst a fader is up full does not prevent the output from fully switching. A few seconds will need to be allowed for the timer circuit to settle to make this check, and if any small spikes do appear (this is unlikely) the 'B' and 'A' presets will have to be readjusted.

The only test left now is that of the output stage, and this can be done as soon as the board is dropped into the case from the front, bolted in position and the triacs and regulator affixed, using heatsink compound. When screwing the board into the case, note that there is not a lot of clearance on the fixing nearest IC1. It may be necessary to use an insulating washer under the screw head. The aluminium bracket that the triacs screw into must be spaced from the board with a fibreglass insulator such as supplied in the kit of parts to prevent the neutral rail shorting to ground.

Connection of the board is by push-on receptacles, except for the mains input, which connection is made onto terminal bolts via crimp connectors as mentioned previously. The choke wires connect to two terminal pins. One pin is immediately behind and just above the top end of each of the 'A' sliders and the other pin about 20mm from its respective output spade terminal, which in turn nestles between the suppression capacitors.

When all the wiring is completed and checked over, connect 12 lamps to the output terminals, with the common neutral line going to one of the four spade terminals by the neutral input terminal. All push-on connectors used should

be either the ready insulated type or should have 'boots' fitted. Do not forget to take an earth line from the input earth terminal to the case.

If a scope was available and the previous tests have been carried out, it only remains to check that the output stages work correctly and that the independent switching functions correctly when the desk is switched to 'Blackout'. If you wish to monitor the signal on the load, use a dropper arrangement comprising a 2M2 resistor from the load to the scope input, a 220k resistor across the input and a 220k resistor from the scope ground terminal back to the desk neutral terminal. Remove the mains earth to the scope temporarily, and take care! Even better use an isolating transformer.

For those without a scope, measure the incoming mains as accurately as possible, and carry out the checks described previously measuring the voltage obtained across the load. A digital multimeter is ideal for this task; the author is not fond of digital meters for the majority of applications, preferring the ability of the analogue instrument to show trends in fluctuating values to the greater accuracy of its digital counterpart, but in this case both maximum output across the load can be checked, and also the lower end voltages, without the changing of ranges and the ensuing risk of wrapping a pointer around its end-stop. As for the scope tests the zero and maximum outputs should be obtained at 5% and 95% of the slider travel. Once this is all completed, the desk is ready to add that extra something to your performance or show. ★

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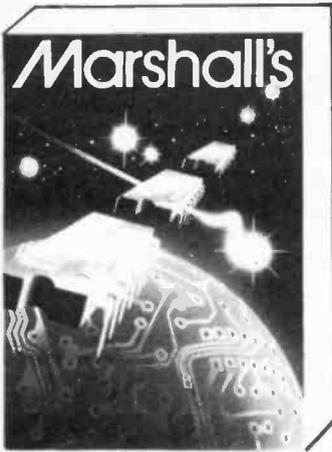
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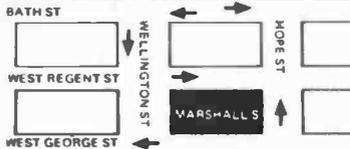
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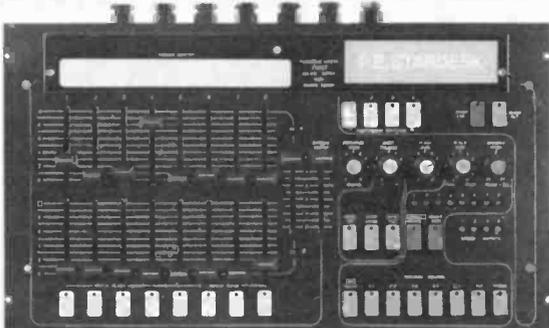
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IMPROVED STEREO TV

European patent application 0082205 from Sanyo of Japan, suggests ways of improving the multiplex stereo system already used on a limited scale for TV transmissions in Germany, and proposed for the rest of Europe. The patent application is particularly interesting because it gives a useful run down on the existing service technology and some of the problems being encountered. Although the Germans are keeping very quiet about these problems, it is surely significant that the service has expanded far less than promised when it was introduced at the Berlin Funkausstellung three years ago. At last year's show, for instance, there was virtually no emphasis on TV stereo sound.

Whereas in Japan, two sound channels are multiplexed on a single sound carrier, in Germany two separate carriers are used. The Germans say this is because there is less risk of breakthrough between channels, but the Japanese system seems to work very well. More likely Germany wants to deter Japanese imports by using a different system. There have been attempts by the Germans at patenting what is essentially well known technology. The Sanyo patent gives a brief run down on this technology.

The normal sound carrier has, in Germany, a frequency 5.5MHz higher than the video carrier. The second sound carrier has a frequency of 5.7MHz above the video carrier, and is set at a level 7dB below the main audio. For stereo music right plus left channels are sent on the main carrier and right only on the auxiliary carrier. For bilingual operation one language is sent on the main carrier and the other on the auxiliary. This gives compatibility with existing receivers. But stereo receivers must have a

switched matrix to cope either with stereo or bilingual. The matrix is switched by tone signals sent with the programme (which, incidentally, can cause "birdie" inter-

switched in for stereo to decode left and right, but left out of circuit when there is a different language on each carrier. The problem in practice, we now learn from

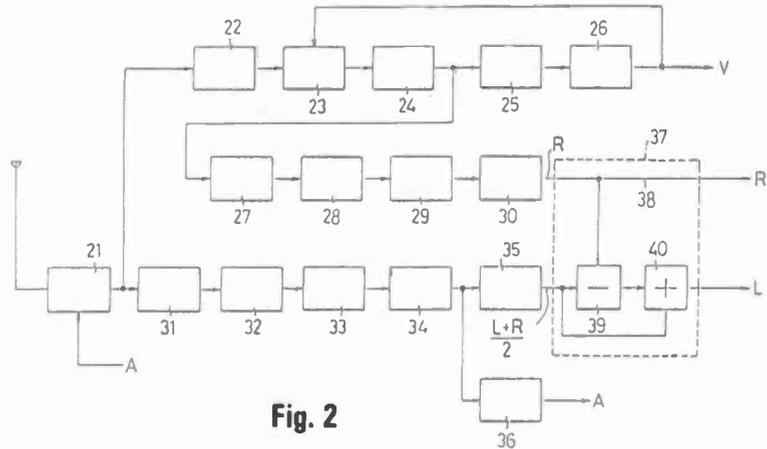


Fig. 2

ference). Fig. 1 shows the present circuit layout. Tuner 1 sends i.f. signal to amplifier 3 through filter 2. Detector 4 separates audio and video. Video is amplified at 5 and audio sent to bandpass filters 6 and 10. The main sound carrier is passed at 6, amplified at 7 and detected at 8. Auxiliary channel is passed at 10 to amplifier 13. Matrix 14 is

Sanyo, is buzz interference as caused by breakthrough from video into the audio circuits. This happens on most TV sets but becomes more noticeable in stereo if there is uneven buzz between channels.

Fig. 2 shows a new buzz balancing circuit and Fig. 3 shows the German stereo spectrum. (Note vision-sound carrier spacing is

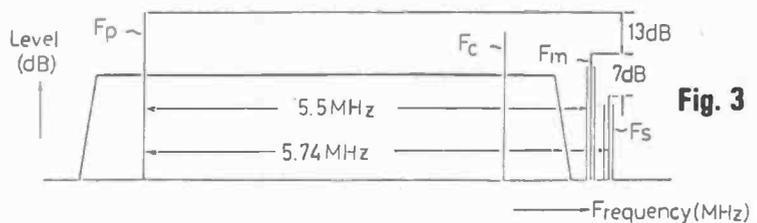


Fig. 3

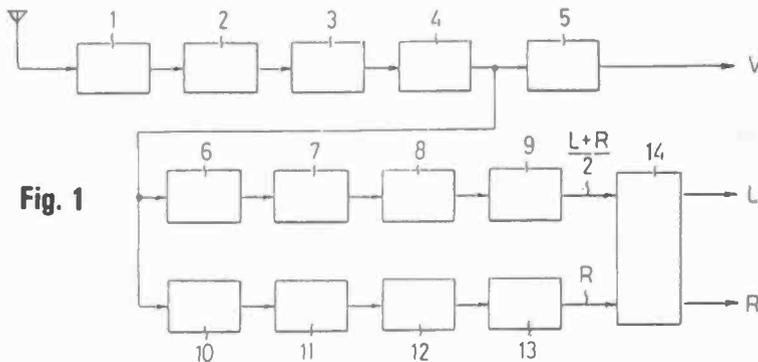


Fig. 1

different in the UK.)

Tuner 21 outputs to i.f. filters 22 and 31. Video detector 24 outputs the main sound carrier and auxiliary sound carrier to filter 27 which passes the auxiliary audio to detector 29 and matrix 37. Filter 31 passes both the main and auxiliary sound carriers to limiter 32 where the main carrier is separated at 34 and passed to matrix 37. The right channel signal, from the auxiliary carrier, contains buzz. The sum signal from the main carrier contains no buzz. So the matrix output contains equal, but reduced, buzz in each channel. For bilingual operation one channel contains more buzz than the other, but this does not matter because they are not heard together.

MONITORS... for Home Computers

MICHAEL TOOLEY BA DAVID WHITFIELD MA MSc CEng MIEE PART ONE

BRITAIN is a world-leader in terms of the number of home computers per head of population. So much so, in fact, that the accusation of being 'square-eyed' can now as easily refer to being a computer addict, as it can to being a television addict. A factor common to both of these conditions, however, is 'the box' itself. The growth of home computing would have been severely restricted but for widespread television ownership. After all, it is one thing to spend around £90 on a computer, which could turn out to be just a passing fancy, but quite a different matter to spend a further £200 to £300 for a special display unit just to be able to use it. Without a home television, therefore, many people would never even consider buying a home computer, or would rule it out as too expensive. The benefits of the computer have to become clear before adding a special-purpose display (known as a monitor) is usually even considered.

Part 1 of this article describes the various types of monitors which are now available for home computers at reasonable prices. If you are becoming dissatisfied with the quality of the display from your computer, or you are being forced to compute only during off-peak television time, then this article will help you to select a monitor to overcome these problems. Two current production monitors will be reviewed in Part 2 and a buying guide is included here to help in choosing a monitor which will suit both your needs and your pocket.

As a first step, however, we need to be able to make sense of the manufacturers' specifications, and of the facilities provided by monitors. It is useful, therefore, to start by looking at the ways in which computers generate their displays. We will then be in a position to appreciate what it is that a monitor must do with the signal from the computer.

COMPUTER DISPLAYS

In most medium and large computer systems, the tasks of working out the contents of a display, and of actually 'drawing' the image, are kept quite separate. For example, the main computer usually works out what is to be put onto the screen, outputs it to a display terminal (usually a VDU), and then forgets about it. The VDU, on the other hand, remembers the information from the computer, and looks after drawing the result onto the screen. Subsequent commands

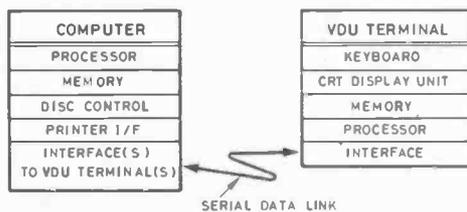


Fig. 1. Computer/VDU configuration

from the computer may cause changes to the information to be displayed, and this new information is again remembered in the VDU's memory, and displayed. Such VDUs must thus be able to communicate with the computer, must have a memory in which to hold the information to be displayed, and must be able to turn the memory's contents into a visual display. This usually means that there is a processor and some memory in both the computer and the terminal. Fig. 1 illustrates a typical arrangement.

A VDU of the type described above could be used in a small computer system, but it would probably cost two or three times as much as the computer itself. Most of the VDU functions are therefore usually performed by the computer,

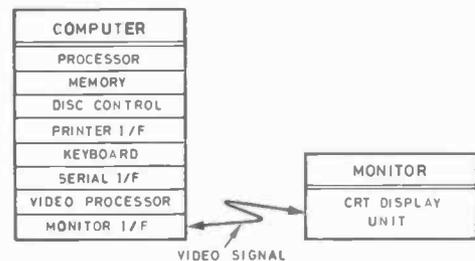


Fig. 2. Computer/monitor configuration

as shown in Fig. 2. The only function not then performed by the computer is actually 'drawing' the image onto the cathode ray tube; instead, a video signal is generated by the computer to drive a separate monitor. As we shall see, this video signal can take many different forms, but its essential purpose is to provide a convenient way of representing the final image. The most popular method, available on all small computers, is to generate a standard television signal suitable for driving a domestic television. However, this is not the only method, or even necessarily the best, but it is initially the most convenient approach.

GENERATING VIDEO SIGNALS

The majority of home computers now produce colour displays, and Fig. 3 shows a typical arrangement for the video section of such a computer. Basically, the same memory is shared by the programs and the display. Specific regions of this memory, however, are allocated exclusively for programs and for the display in any particular graphics/display mode. The memory area used for the display is often referred to as 'video RAM', while that reserved for programs is referred to as 'user RAM'.

This sharing of memory between the display and user programs allows very efficient utilisation of memory, and also minimises the hardware required to support the computing and display functions. A further benefit of this

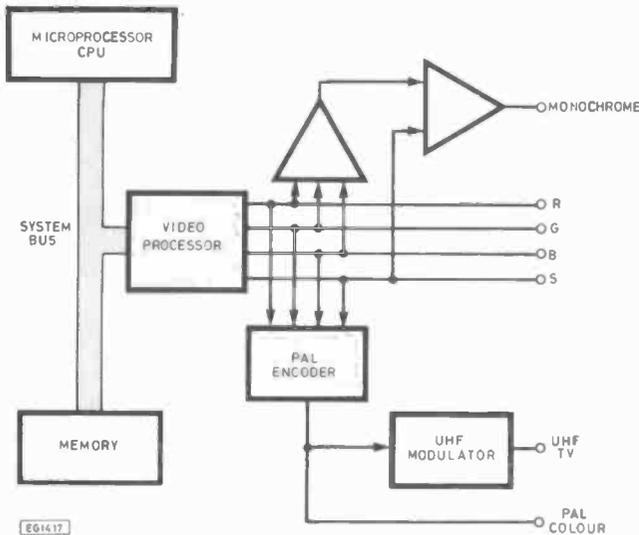


Fig. 3. Small computer video section

approach is that the division of memory between display and programs can be varied depending on the requirements of the selected graphics/display mode. The actual amount of video RAM required depends on the number of display colours, the maximum number of characters on a screen, and the resolution of any graphics. The remaining memory is then free for programs; large programs can thus be made to fit by judicious selection of the display mode used.

In such shared-memory systems, the CPU writes suitably coded information into the video RAM, either directly or via a language such as BASIC. This is usually done by running a program, but it can also be done directly from the keyboard. The video processor reads this display information, and converts it into a signal suitable for driving the display (monitor or television). Both of these operations appear to occur at the same time, although in fact the CPU and the video processor time-share the system bus and the memory. The exact details vary from one computer to another, but the general principles apply to most small computers. Having read the coded information from the video RAM, the next step is to look at how the various types of video signal are produced.

R-G-B-SYNC

The standard UK method of producing a colour picture uses 625 lines to build up each picture frame. In order to produce a stable picture, these frames are repeated at a rate of 25 per second: a technique known as raster scanning. In practice, each of the 625-line frames is usually drawn in two stages: the odd-numbered lines on the first scan, and the even-numbered lines on the second scan. This technique, known as interlacing, avoids visible flicker on the picture, and results in each scan lasting one-fiftieth of a second.

The video processor output must give a colour for every possible display position (pixel) in each picture line, even if this is only to indicate that there is no colour (black). The overall picture is thus represented by a 2-dimensional coloured matrix which is built up from lines of coloured pixels. The actual number of pixels in each line depends on the resolution of the computer; the more pixels, the finer the detail which can be displayed, but the greater the amount of video RAM required. The colours available are usually simple combinations of the primary colours, red, green and blue.

When any of these appears in a pixel, it is at maximum brightness, giving a total of eight possible colours; black (no colour), red, green, blue, yellow (red and green), magenta (red and blue), cyan (blue and green), and white (all colours), as illustrated in Fig. 4.

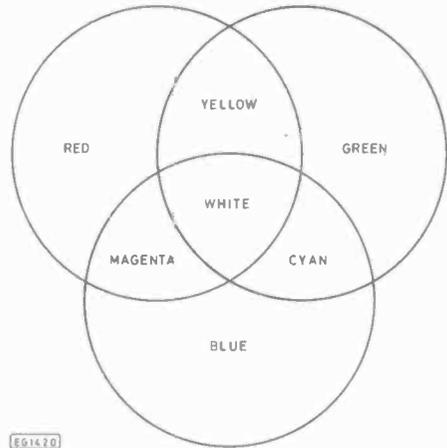


Fig. 4. Colour mixing chart

The pixel colour information on its own is not enough, however, to be able to recreate an image. Some additional control information is necessary to show where each line and frame starts. The signal for each line therefore starts with a line synchronisation pulse ('sync'), and is followed by the colour information for the pixels in that line; the whole line lasts 1/15625th of a second. In practice, not all of the 625 lines are actually used to display 'picture' information. A few lines in each frame are used to allow the picture spot to move from the bottom of the screen back up to the top during the frame sync pulse. This is similar to the way in which the spot moves back to the start of each line during the line sync pulse interval.

A typical display line is shown in Fig. 5 in terms of the four video processor outputs: red, green, blue and sync. On many computers this R-G-B-Sync signal is made available to drive

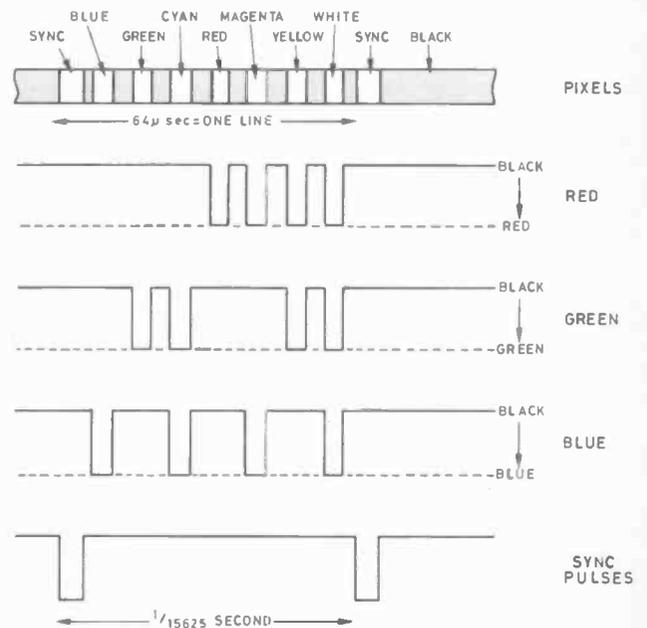


Fig. 5. R-G-B-Sync signals

a suitable monitor. However, even when not actually made available externally, the R-G-B-Sync signal is invariably produced internally by the computer.

Standard colour display tubes have a great deal in common with the R-G-B-Sync signal. Three electron 'guns' are used to produce the image on a colour tube, with each colour component (red, green, blue) being drawn by a separate gun. The electron beam from each gun is aligned to illuminate only the appropriately coloured phosphor dots on the screen, as illustrated in Fig. 6. Thus the image is built up

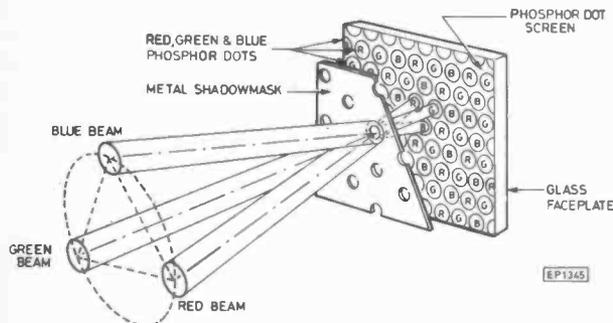


Fig. 6. Colour shadow mask tube

from numerous small clusters of the three primary colours.

The individual red, green, and blue signals from the computer are ideally suited to drive the colour guns, after appropriate amplification, and the sync signal provides the necessary information to control the positioning of the electron beams at any instant. All-in-all the R-G-B-Sync signal provides an ideal signal to drive a colour display tube, and monitors which accept such a signal are referred to as RGB monitors. Not all computer users will have an RGB monitor, so most colour computers also provide alternative video outputs.

PAL COLOUR

The next section of the video circuitry generates a composite colour signal by combining the information carried by the individual red, green, blue and sync signals. There are many different methods of combining red, green, blue, and sync to produce a single, composite colour signal. The method adopted in the UK uses the PAL coding system; France uses a system known as SECAM, while the NTSC system is used in the USA.

In the PAL system, an 8MHz bandwidth is allocated for a colour signal, as shown by Fig. 7. Different programmes are broadcast by modulating PAL signals onto suitable UHF carriers, using different carrier frequencies (a minimum of 8MHz apart) to separate the channels. The bottom part of the PAL bandwidth is used for luminance (brightness) information. Above this is a band centred on 4.43MHz which carries chrominance (colour) information. The sound information, if present (not on many computers), is then carried

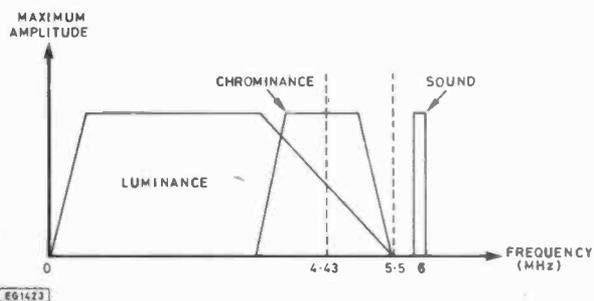


Fig. 7. PAL colour signal bandwidth

by a very narrow band centred on 6MHz, and the remaining bandwidth is used to provide separation from adjacent channels. Black-and-white sets are able to use PAL signals because they are only concerned with the luminance information.

The PAL encoder takes the computer's red, green, blue and sync signals, and combines them into a composite signal. This PAL signal is sometimes available as an output, and is particularly suitable for driving the VCR or CTV input provided on some colour television sets. The usual purpose of producing the PAL signal, however, is for modulating a suitable UHF carrier so that it can be used with a domestic television receiver.

UHF TELEVISION

The broadcasting services use sophisticated high power transmission equipment to modulate PAL signals onto UHF carriers, but more modest techniques suffice in small computers. A compact UHF modulator is used (invariably tuned at or around channel 36) which accepts a PAL input and produces a modulated low-power UHF signal which can be applied directly to the television's aerial socket.

The UHF modulator is designed to produce an output whose characteristics are as shown in Fig. 7. This implies that the luminance information must not exceed around 4MHz if interference with the chrominance information is to be avoided. With fine picture details, however, problems can arise because closely-spaced picture changes are represented by high luminance frequencies. This effect is demonstrated by clothing with close checks or stripes when seen on television; the fine patterns take on unexpected bursts of colour. An additional limitation on the maximum resolution (finest detail) of the UHF signal is imposed by the UHF modulator itself, which typically has a bandwidth of around 6MHz.

The final point to note about the modulators used in small computers is that their carrier frequency tends to drift slightly as they warm up. Depending on the television, this may necessitate adjustment of the (usually small) tuning controls to maintain the sharpest possible picture. Modern sets, however, are increasingly tolerant of such drift due to their automatic frequency control circuitry, but beware of the effect on older sets!

The UHF signal is probably the most useful output for the newcomer to home computing since it allows the computer to be used immediately with an unmodified television set. The use of this output does, however, bring with it some limitations in the achievable image quality. In many cases, however, these limitations will not be important, and a domestic television will provide a perfectly adequate level of performance.

MONOCHROME

There are many applications where a colour display is not really necessary or even desirable. Perhaps the best example of this is in word processing, where it is much more important that the display is as clear, sharp and stable as possible. In order for 80-column text to be easily readable, the monitor should have a high resolution. Typical 80-column text is composed of characters which are 8 pixels across. This gives 640 pixels on each line, and requires a monitor with a bandwidth of around 10-12MHz in order to produce a satisfactory picture. This performance is, however, usually well beyond the capabilities of a standard colour television, and for this reason a monochrome monitor (or a modified black-and-white television) is usually preferred for high resolution displays where colour is not essential.

Using the PAL signal to drive a monochrome monitor will

work, but it results in the loss of the very resolution which we are striving to retain. The best method of generating a suitable monochrome signal is to combine the red, green, and blue signals (rather than encode them as for PAL) to produce a monochrome signal which shows different colours as shades of grey, but which retains the highest possible resolution. The sync information is then added to what is by now a purely luminance signal, and a composite monochrome signal is then available.

CHOOSING A MONITOR

Having looked at the various ways in which a computer may output a signal representing the image to be displayed, which type of monitor do we choose? Before starting to decide, however, it is well worth looking at the image on your television, and deciding what you feel is wrong (or not quite right) with it. Then think carefully about the types of image that you would use a monitor to display, and decide on the performance improvements required.

Among the factors to consider next, price inevitably comes high on the list. Other considerations include whether colour is required, and whether a custom-designed monitor is required, or will a monitor/television suffice? The outputs available from the computer itself may also limit the choice somewhat, although it may be possible to obtain an additional interface to provide any missing outputs. Only when all of these factors have been considered will the necessary information be available to allow a start to be made in choosing a monitor.

When looking at a monitor, there are some general points worth noting. The first is to try out the monitor on the highest resolution display possible, and in particular see if text is readable at your expected viewing distance. Next, fill the whole screen with plus signs and look to see if they vary in shape or size across the height and width of the display; they shouldn't! With the same display, look for any signs of picture shimmer caused by poor power supply design. Next, try producing as white a display as possible (e.g. lines of white blocks), since this represents the most severe type of load on the power supply; the brightness should be constant across the screen. Finally, always try out any monitor on an image which is typical of your most exacting requirements, and then compare the results with at least one other monitor.

RGB MONITORS

An RGB monitor is without doubt the ideal type for colour displays since such a monitor makes the best possible use of the information provided by the computer. The major decisions to make in choosing an RGB monitor relate to the screen size and the bandwidth required. Choice of screen size is a matter of personal preference, and is usually limited by what is actually available; most RGB monitors have 14" screens. Choice of bandwidth is, however, a rather more involved matter.

A useful guide for good displays (colour or monochrome), is that a monitor should have a bandwidth which is approximately 1MHz for every 60 pixels in each display line. Thus, for 80-column text from a computer whose characters are each 10 pixels wide (i.e. 800 pixels per line), a bandwidth of 12-14MHz will produce a good picture. A lower bandwidth will produce quite acceptable results, but this will depend on the degree of image sharpness and resolution required. The minimum bandwidth to be able to distinguish between adjacent pixels, however, is around 1MHz for every 120 pixels in each line, and in the example above this represents a 6-7MHz bandwidth. Bandwidths below the minimum will cause adjacent pixels to merge into one another, and the picture will begin to noticeably lack

sharpness. By comparison, the usable bandwidth of a colour television is typically in the region of 5MHz maximum. As a guide, the finest lines on the test card are at 5-25MHz.

A point to note in relation to the bandwidth of RGB monitors is the size of the phosphor dots which make up the picture. Colour televisions are designed to be viewed from a distance, whereas many monitors are used less than a metre from the operator. When used for very high resolution work, the size of the phosphor dots becomes comparable with size of the pixels. The dots can actually be distinguished from very close-up on larger television tubes. Many monitors use tubes which are similar to those used in televisions, and it is advisable, therefore, to check that the spot size of the tube will allow the number of pixels required to be clearly displayed (often quoted in terms of pixels per line). This limitation does not apply to monochrome monitors (at least not as far as is visible to the naked eye), and for this reason monochrome monitors are usually preferred for word processing and similar applications.

In most literature, RGB monitors are referred to as medium/standard or high resolution; typically these have bandwidths of 10-12MHz, and 14MHz, respectively. RGB monitors of lower bandwidths are also available, typically around 7MHz. The bandwidth figure should, however, always be studied in conjunction with the horizontal resolution figure in order to determine the *usable* definition of the display.

The ultimate test as to whether a monitor has adequate bandwidth for your purpose is to try it out. Putting up 80-column text, for example, usually provides one of the most severe tests. The safest choice with colour monitors is to select a purpose-built RGB monitor with a bandwidth of 12-14MHz or more; this should cope with even the highest resolution displays currently available from small computers.

MONITOR/TELEVISIONS

Monitor/televisions represent an ideal compromise for many computer owners. Ideally such a set should have an R-G-B-Sync input, rather than the PAL colour input associated with video recorders. By choosing such a set, the problems associated with PAL encoding, limited modulator bandwidth, and the infuriating drift off channel caused by the modulator warming up, are avoided. The set is still also usable as a conventional television, although in some cases this may be considered a disadvantage! It should be borne in mind that such sets have usually been designed primarily as televisions, but the bandwidth is still usually adequate for all but the most exacting requirements.

MONOCHROME MONITORS

When selecting a monochrome monitor, there are a number of colours from which to choose. The usual phosphor colours are white (as in the conventional black-and-white television), green and amber. The colour chosen is purely a matter of personal taste, although green is considered to minimise the strain associated with long periods of use. Many people, however, still greatly prefer to see white text on a black background.

Most monochrome monitors have much higher bandwidths than comparable RGB monitors, with 24MHz models readily available at little or no extra cost. Finding a monochrome monitor with adequate bandwidth is therefore not usually a problem. Portable black-and-white televisions make quite acceptable monitors for many purposes, e.g. 40-column text is usually quite acceptable. For higher resolution work, however, a model with a direct video input is to be greatly preferred. In all cases the improvement provided by direct video input is quite dramatic.

Buyer's Guide

Two of the biggest problems often encountered after deciding to buy a product, especially in electronics, is finding out exactly what models are available in your price range and from where.

To help you overcome these problems when choosing a monitor we have listed 30 currently available models from a wide variety of manufacturers. Although it has not been possible to list all the models of every manufacturer we have tried to produce a balanced guide covering the six main specification areas.

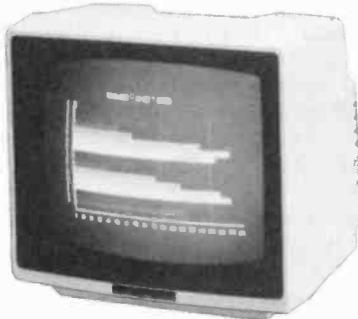
Most of the models given in our Table are dedicated monitors with the exception of the three marked †† which can also be used as television receivers.

The prices shown are intended only as a guide and current prices including VAT and carriage together with further details and specification sheets on the models listed can be obtained from the quoted suppliers.



The PTC 1202E from Philips

The Kaga Texan 12in monochrome monitor



The Bosch Blanpunkt range of monitors

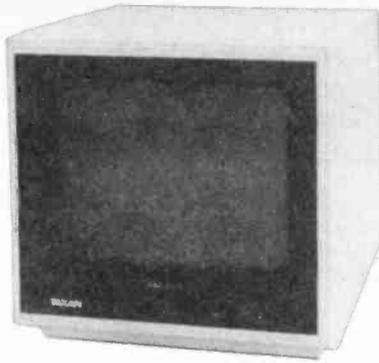


Fidelity's CM14 14in colour unit

MANUFACTURER	MODEL	SCREEN SIZE	INPUTS	BANDWIDTH
CABEL	CE370A	14in	RGB	10MHz
PRINCE SPA	PRINCE 12	12in	COMPOSITE	24MHz
NOVEX	NC-1414-CL	14in	COMPOSITE/ RGB	7MHz
FIDELITY	CM14	14in	COMPOSITE/ RGB	12MHz
PHILIPS	TP200	12in	COMPOSITE	18MHz
	PCT1201	12in	COMPOSITE	22MHz
	PCT1202	12in	COMPOSITE	22MHz
JVC	TM-90PSN	10in	RGB	•
SONY	PVM-1370	13in	RGB	10MHz
	PVM-91CE	9in	COMPOSITE	•
KAGA	K12G	12in	COMPOSITE	15MHz
	K12A	12in	COMPOSITE	15MHz
	K12R1	12in	RGB	15MHz
	K12R2	12in	RGB	15MHz
BOSCH	CDS37-121	14in	RGB	5MHz
	CM51-120	20in	COMPOSITE††	5MHz
SWORD	SCIMITAR	14in	RGB	18MHz
	SABRE	14in	RGB	18MHz
	RAPIER	14in	RGB	18MHz
ROLAND	CC-141	14in	RGB	18MHz
	CB-141	14in	COMPOSITE	•
	NB-121	12in	COMPOSITE	18MHz
CONRAC	ENA12/C	12in	COMPOSITE	10MHz
BARCO	DCD2240	22in	RGB	5MHz
BETER	BTV5000C	14in	RGB ††	10MHz
	BTV5001	14in	RGB ††	10MHz
SANYO	DM8112CX	12in	COMPOSITE	18MHz
	CD3115H	14in	RGB	•
	CD3117M	14in	RGB	•
	CD3125N	14in	RGB	•

†† Monitor/receiver model

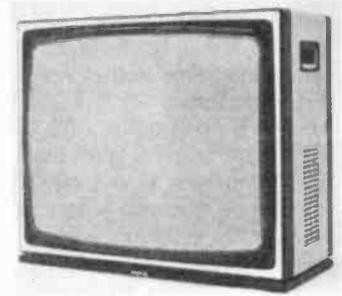
• Not known



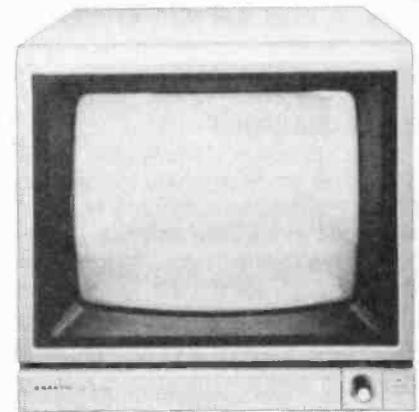
The Kaga Texan 12in colour unit



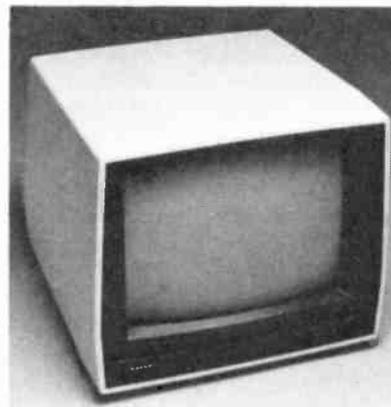
The JVC TM-90PSN 10in colour unit



The Barco 4000 series of receiver monitors



The Sanyo DM8112 green phosphor model



The Sanyo CD3115 14in colour monitor



The Sony PVM-1370 13in colour monitor

MONOCHROME COLOUR	PRICE GUIDE	AUDIO OUTPUT	SUPPLIER
COLOUR	£199.50	NO	CABEL ELECTRONIC, 19 High St., Tewkesbury, Glos (0684 298840)
MONO	£65	NO	DISPLAY DISTRIBUTION LTD., 35 Grosvenor Road, Twickenham, Middlesex (01-891 1923)
COLOUR	£199.95	YES	DISPLAY DISTRIBUTION LTD., 35 Grosvenor Road, Twickenham, Middlesex (01-891 1923)
COLOUR	£199	YES	MICRO PERIPHERALS LTD., 69 The Street, Basing, Basingstoke, Hants (0256 3232)
MONO	£88	NO	SWIFT SASCO LTD., Box 2000, Gatwick Road, Crawley, Sussex (0293 28700)
MONO	£118	NO	
MONO	£135	NO	
COLOUR	£350	YES	JVC, Eldonwall Trading Estate, Staples Corner, 6-8 Priestly Way, London (01-450 2621)
COLOUR	£805	YES	METRO VIDEO LTD., 5 Lansdowne Way, SW8 (01-582 2088)
MONO	£225	NO	
MONO	£109	NO	DATA EFFICIENCY LTD., Hemel Hempstead, Herts (0442 60155)
MONO	£119	NO	
COLOUR	£239	NO	
COLOUR	£285	NO	
COLOUR	£450	NO	TELETAPE LTD., 12 Tolden Square, London W1 (01-434 3311)
COLOUR	£560	YES	
COLOUR	£325	NO	COTRON ELECTRONICS LTD., Rockland Works, Eagle Street, Coventry (0203 21247)
COLOUR	£455	NO	
COLOUR	£550	NO	
COLOUR	£565	NO	ROLAND (UK) LTD., Great West Trading Estate, 983 Great West Road, Brentford (01-568 4578)
COLOUR	£299	YES	
MONO	£153	NO	
MONO	£620	NO	LINK ELECTRONICS LTD., North Way, Andover, Hants (0264 61345)
COLOUR	£505	YES	CAMERON COMMUNICATIONS, 3 Burnfield Road, Giffnock, Glasgow (041-633 0077)
COLOUR	£225.84	YES	BETER ELECTRONICS, 58 Mill Road Avenue, Angmering Village, Sussex (09062 72833)
COLOUR	£241	YES	
MONO	£109	NO	MICRO PERIPHERALS LTD., 69 The Street, Basing, Basingstoke, Hants (0256 3232)
COLOUR	£499	NO	
COLOUR	£349	NO	
COLOUR	£235	NO	

** All prices ex VAT and carriage

THIS Temperature Controller uses a single m.o.s. integrated circuit to make temperature measurements and provide a controlled output which may be used to switch on or off any appliance.

The operating range is -39.9 to $+39.9^{\circ}\text{C}$. The accuracy is better than $\pm 0.5^{\circ}\text{C}$ over the range 0 to $+39.9^{\circ}\text{C}$ when using a thermistor as the sensor; the response time when using this type of sensor is very fast indeed.

Two control outputs are provided, one which operates when the temperature is greater than that which has been set, and one which operates when the temperature is lower. Additionally, adjustable hysteresis can also be preset which then provides a margin either side of the critical temperature.

The i.c. used also features leading zero blanking, power failure detection, overrange indication and direct drive of either l.e.d. or l.c.d. displays.

BLOCK DIAGRAM

A block diagram of the system is shown in Fig. 2.

Consider the case where the temperature being measured is positive. The input circuitry within the dotted line can be considered as a bridge network designed to balance at 0°C . In this situation the output from the two comparators is zero (actually V_{ref}). When the temperature rises positively the output from the comparators changes, i.e. a voltage difference is produced. A non-linear ramp is produced by the system controller, the time taken for the ramp voltage to change from one comparator input voltage to the other gives the temperature. The measurement/read cycle diagram of Fig. 1 shows this more clearly. It can also be seen from the diagram how a temperature which is negative can also be measured in this way. The part shown as 'system cycles' allows the input to be auto-zeroed.

Connected to the system controller are the adjustable Set Temperature switches and the presettable hysteresis switches. Together these set the limits to the required temperature. Inside the system controller are further comparators which compare the measured temperature with the set temperature. Two switched outputs are provided, one which operates when the temperature is at the set point plus the hysteresis, and the other which operates when at set point minus the hysteresis. The appropriate output is selected by the mode switch and passed to the alarm and relay.

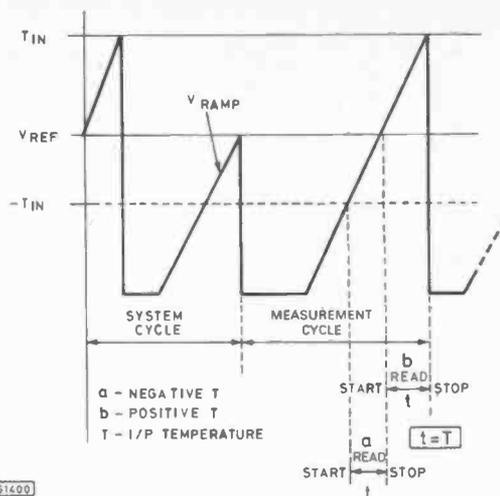


Fig. 1. Measurement/Read Cycle diagram

Both outputs switch off when the temperature returns to the set value. Thus the Temperature Controller provides either an overrange or underrange indication as required.

CIRCUIT DESCRIPTION

The full circuit diagram for the Temperature Controller is shown in Fig. 3.

The main i.c. is IC1, type AY-3-1270 and the pin-outs for this are shown in Fig. 5. The set temperature switches are three binary-coded decimal thumbwheel switches S6-S8. The ten's are set by S6, only the figures 0,1,2,3, should be set otherwise inaccurate readings will result. The unit's switch is S7 and is set to any number 0-9. Likewise with the 0.1's. The sign switch, S1 is used to set the sign of the temperature; in its normal position it is set to plus. The hysteresis set switches are S2-S4, S5 being the l.e.d. select switch and is normally in the off position. These four switches are contained in a single d.i.l. package mounted on the p.c.b. Consequently, the hysteresis must be decided on before final construction. The code for the hysteresis is not b.c.d.; the switch positions are given in Table 1.

There are 7 presettable hysteresis levels, ranging from $\pm 0.2^{\circ}\text{C}$ to $\pm 8^{\circ}\text{C}$. Additionally there is a 0.05° hysteresis

TEMPERATURE CONTROLLER

T. J. JOHNSON

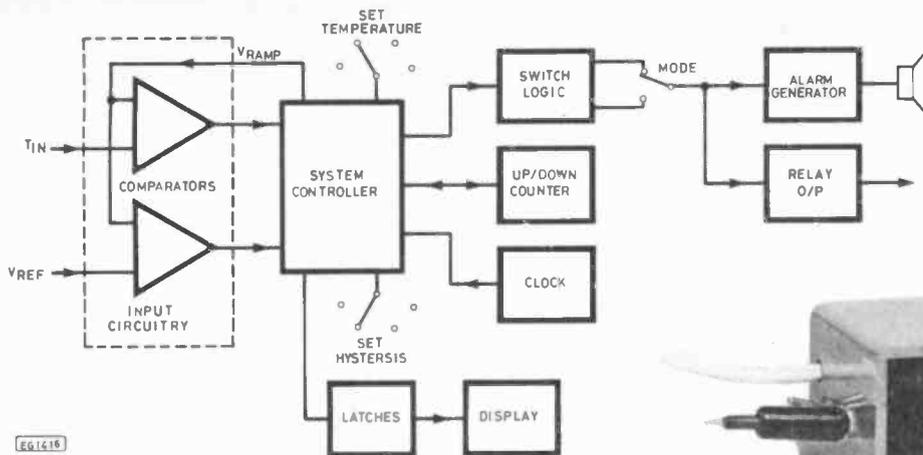


Fig. 2. Block diagram



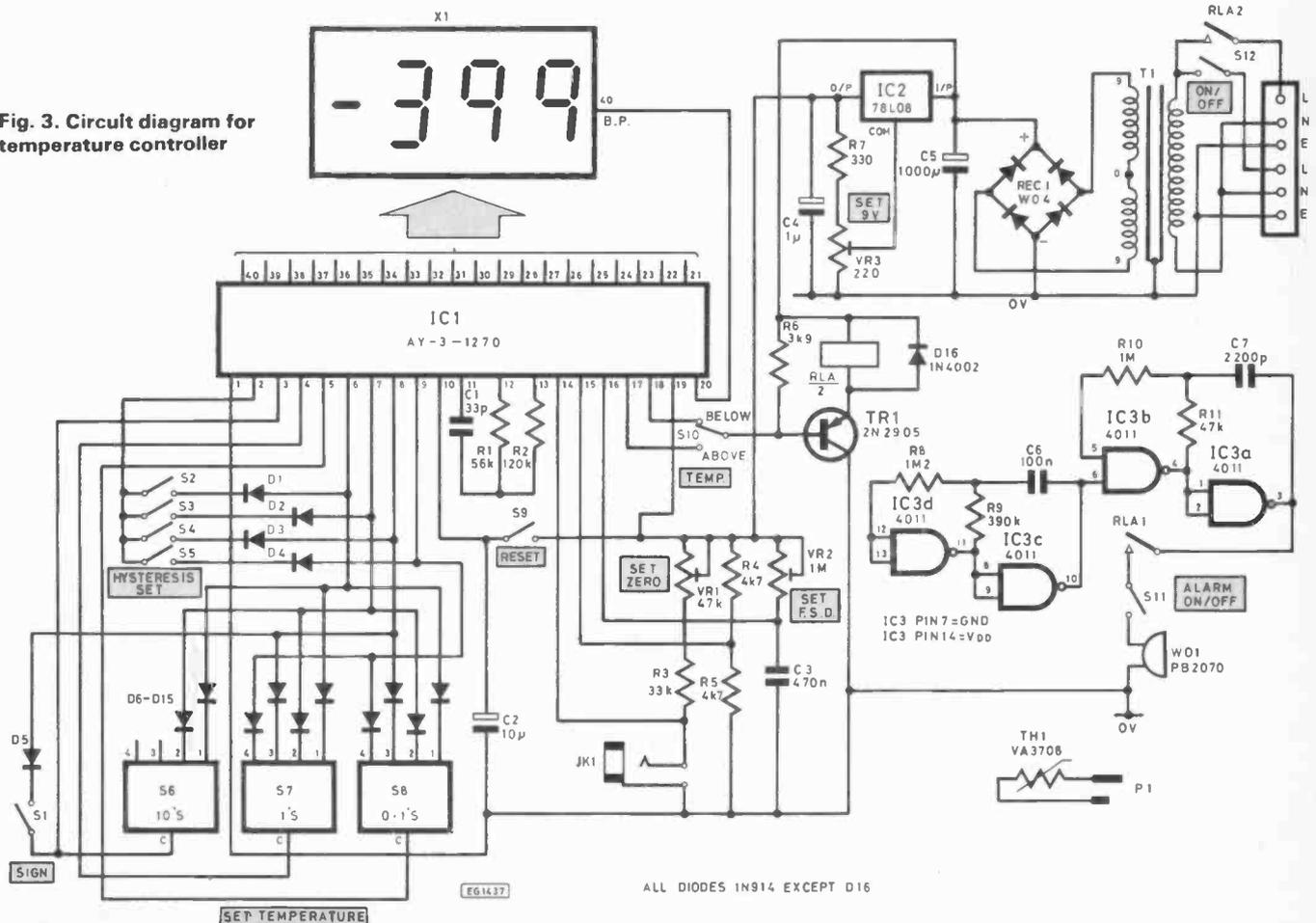
already set within the i.c. to prevent display and control output jitter. This figure should be borne in mind when setting the unit.

The clock components C1, R1 and R2 provide a clock frequency of about 560kHz. For most applications this type of R/C clock is quite suitable although minor variations may be noticed if the power supply voltage should drop by an appreciable amount. For this reason the clock is also designed to be used with a much more stable ceramic resonator. The

circuit for this is shown in Fig. 4. Ideally the resonator should be 560kHz, although any type within the range 300 to 800kHz should work.

The reset switch S9 together with C2 form the power failure detection circuit. Normally S9 is in the open position at switch on. When the unit is switched on, the circuit will operate normally, displaying the actual temperature for

Fig. 3. Circuit diagram for temperature controller



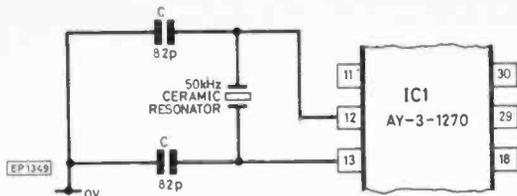


Fig. 4. Alternative clock circuit

about 2-3 seconds. After this time the circuit will store the last measurement and flash the display at about 1 flash every two seconds. In this condition the circuit will still operate normally, making real time measurements and switching the outputs as appropriate. Operation of the reset switch will restore the display to normal.

If there is a short power failure, of say two or three seconds' duration, the circuit will ignore it, and once power is restored will operate normally. If however, the power failure lasts longer, then on restoration of the power, the display will commence to flash as before. The display will also flash if an overrange situation occurs.

The bridge components are VR1, R3, TH1, R4 and R5. The preset is used to balance the bridge such that the display reads zero. The last components associated with the i.c. are C3 and VR2 and together they form the ramp. VR2 sets the f.s.d. of the unit.

The remaining parts of the circuit are the alarm generator and the power supply. The power supply is conventional, supplying a stabilised voltage of 9V to the i.c. and an unbalanced voltage of about 18V to the remainder of the circuit.

The mode switch S10 selects the required output. In the position shown in the diagram the relay will turn on and the alarm will sound when the temperature falls below the set temperature. In its second position, the relay will turn on when the output is above the set temperature.

The alarm circuit consists of IC2 and the ceramic buzzer to form a very effective pulsed output. The alarm may be turned off by S11 without affecting the normal operation of the controlled outputs.

COMPONENTS . . .

Resistors

R1	56k
R2	120k
R3	33k
R4,R5	4k7 (2 off)
R6	3k9
R7	330
R8	1M2
R9	390k
R10	1M
R11	47k
All 1/4W 5% carbon	

Potentiometers

VR1	47k horiz. preset
VR2	1M horiz. preset
VR3	220 horiz. preset

Capacitors

C1	33p polystyrene
C2	10µ 16V elect.
C3	470n polyester
C4	1µ 16V tant.
C5	1000µ 25V elect.
C6	100n
C7	2200p

Semiconductors

D1-15	1N914 (15 off)
D16	1N4002
TR1	2N2905
IC1	AY-3-1270
IC2	78L08
IC3	4011
REC1	W04
TH1	VA3708
X1	3 1/2 digit liquid crystal display

Switches

S1,S9	s.p.s.t. min toggle
S11,S12	
S2-S5	four way d.i.l. switch (s.p.s.t.)
S6-S8	b.c.d. thumbwheel switches (3 off)
S10	s.p.d.t. min toggle

Miscellaneous

T1	9-0-9 100mA transformer
WD1	PB2070 ceramic buzzer
RLA	12V 185 coil d.p.d.t. contacts (RS, 348-908)
JK1	3.5mm socket
PL1	3.5mm plug

Three p.c.b.s; ribbon cable; 6 way p.c.b. mounting, terminal block; 8BA hardware; display bezel (Vero); i.c. sockets; case ('clock case'—West Hyde Developments Ltd., Unit 9, Park Street Industrial Estate, Aylesbury, Bucks HP20 1ET).

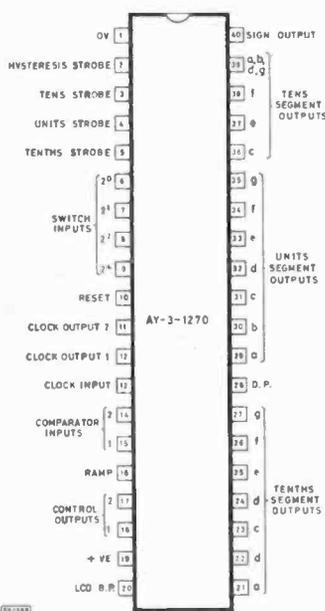


Fig. 5. Pin-out details for IC1

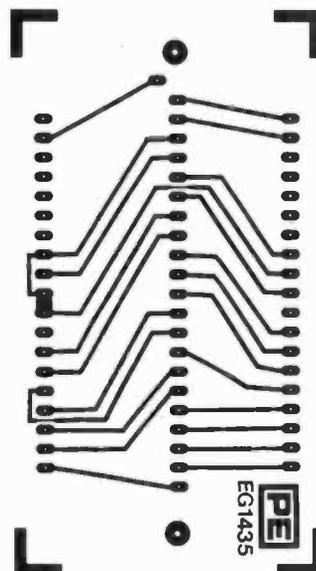


Fig. 6. P.c.b. design for Display board

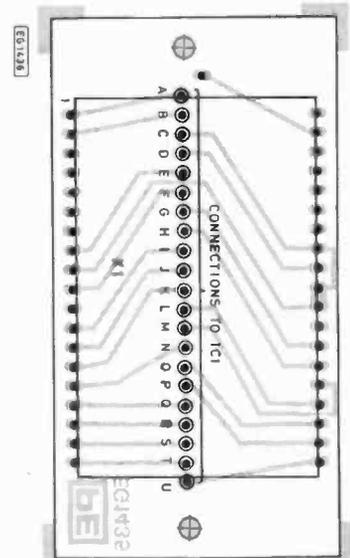


Fig. 7. Component layout for Display board

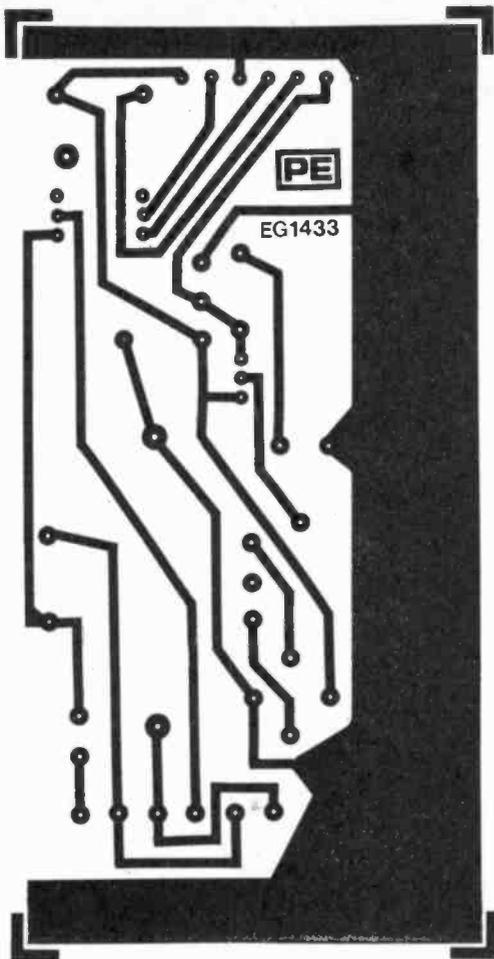


Fig. 8. P.c.b. design for Power board

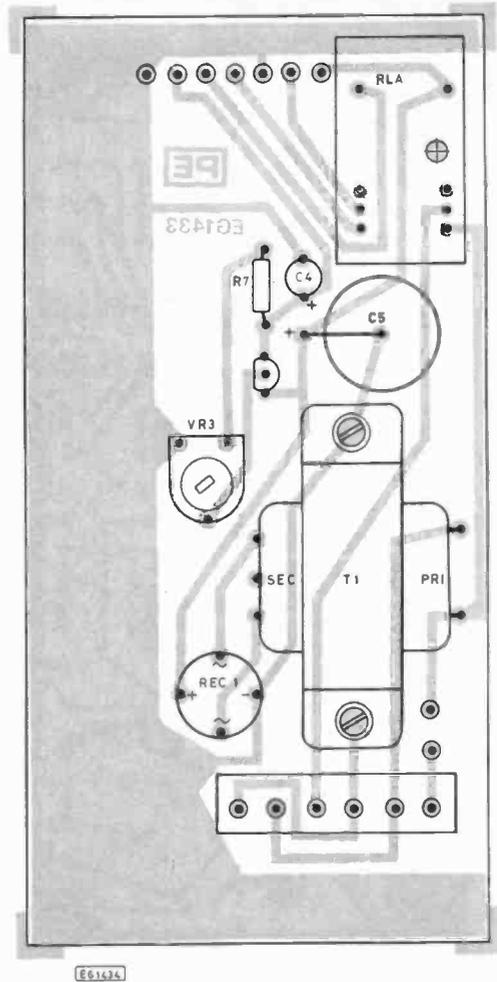


Fig. 9. Component layout for Power board

CONSTRUCTION

The Temperature Controller is built on three printed circuit boards designed to fit inside the recommended case. The fit inside the case is quite tight and some constructors may wish to mount the boards etc, in a larger case. For this reason no case drilling details have been given, besides which a great deal depends on the display bezel and b.c.d. switches used.

Figs. 6 and 7 show the display board details. The size given is appropriate for the type of bezel specified and should of course be varied if other types are used. The l.c.d. should be soldered direct to the board and not mounted in sockets.

The power supply board is shown in Figs. 8 and 9. The relay and transformer are very much standard items so changes in the layout should not be required. The final board is the main board and this is shown in Figs. 10 and 11. Here once again all the components are standard, except perhaps for the d.i.l. switch. It would be wise to check this component before finally drilling the board.

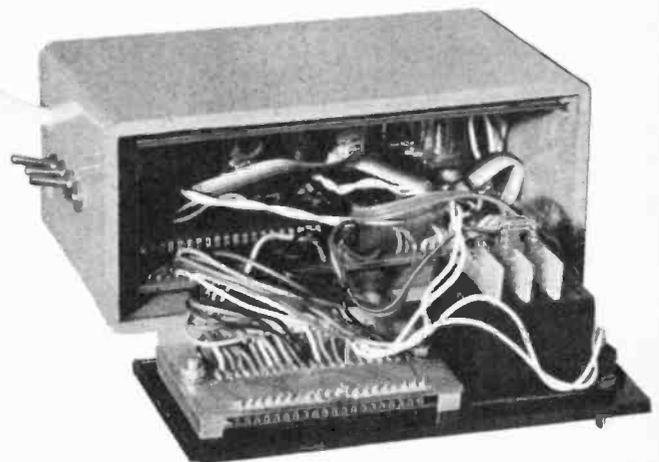
Because of the lack of space in the prototype, the ceramic buzzer (WD1) was mounted on the back-side of the Main board, as can be seen in Fig. 11.

FINAL WIRING

Fig. 12 shows the final wiring between the three p.c.b.s. The majority of the wiring was done with multi-coloured ribbon cable, with the exception of the mains switch, socket and the reset switch, for which a twisted-pair was used.

Connections to the display board are made direct to the pads on the copper side using single stranded wire. Note that the connections to the main board are in reverse order (see Fig. 12). Ribbon cable may be used here, but it would be an advantage if the wires are kept, say, to five per cable. This will make it easier when fitting the front panel.

Note carefully the correct orientation of the diodes D6-D15 which are mounted on the b.c.d. switches. Fig. 12 shows the sign switch (S1) where the spare tag is used to mount the diode (D5), as shown, the toggle of this switch



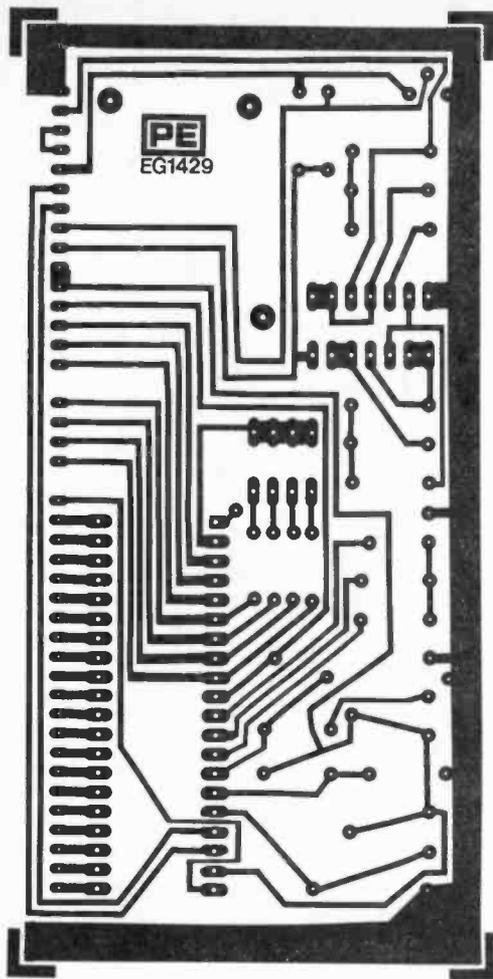


Fig. 10. P.c.b. design for Main board

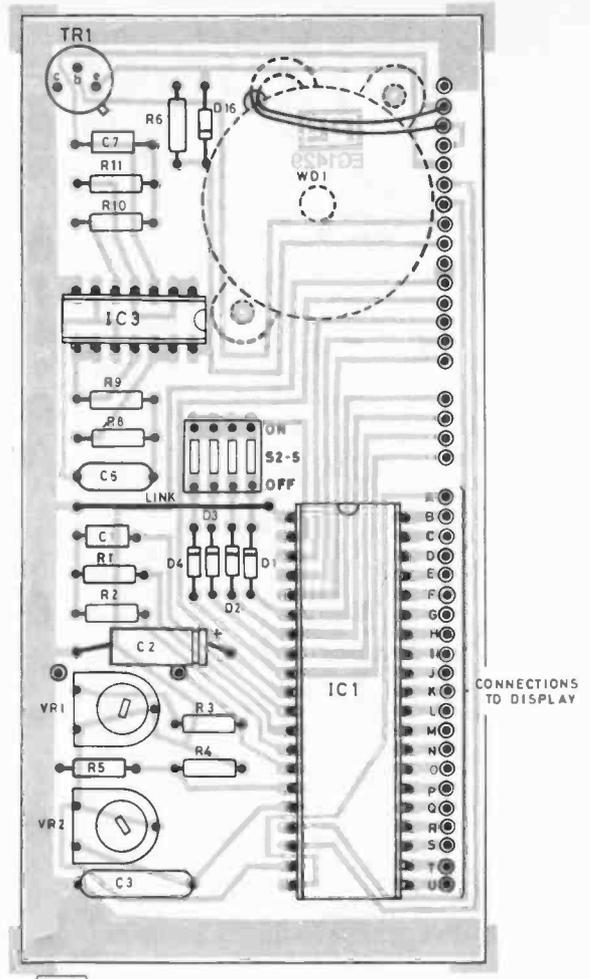


Fig. 11. Component layout for Main board

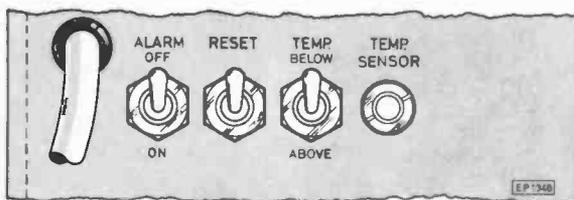
will normally be up when the sign required is positive.
Finally, remember to use sockets for IC1 and IC2.

ADJUSTMENT

There are only four adjustments to be made, the first is setting the power supply to 9V. This should be done with both i.c.s removed from their sockets, and checked again once the i.c.s are plugged in.

Before applying power, set VR1 and VR2 to about mid-position, connect the supply and observe the display. Using an accurate thermometer, adjust VR2 to give the same temperature in free air. This adjustment can conveniently be done at room temperature. Next the Set-Zero preset should be adjusted. This may be done by carefully placing the thermistor in a cube of ice, having previously prepared the ice cube with a suitable hollow, and adjusting the preset as the ice melts.

As a final check on the accuracy, the previous adjustment can be repeated until no further improvement can be made.



Switch function diagram

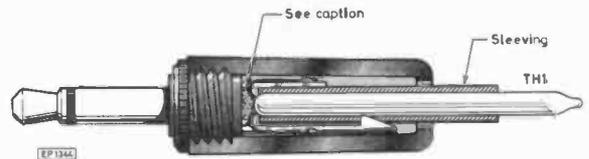


Fig. 13. Cross-sectional view of temperature sensor assembly. A small piece of insulating material should be fitted at the base of the thermistor (TH1) to ensure that no short-circuits occur when the sensor is assembled

Hysteresis	S2	S3	S4	
0				} NOTE
±0.2	X			
±0.4		X		
±0.8	X	X		
±2	X		X	
±4		X	X	
±8	X	X	X	

Table 1. (Hysteresis programming). X=switch to be on. If using an i.c.d. S5 must be 'off'. Note: These are nominal values, variations of ±0.1°C to ±0.9°C can be expected

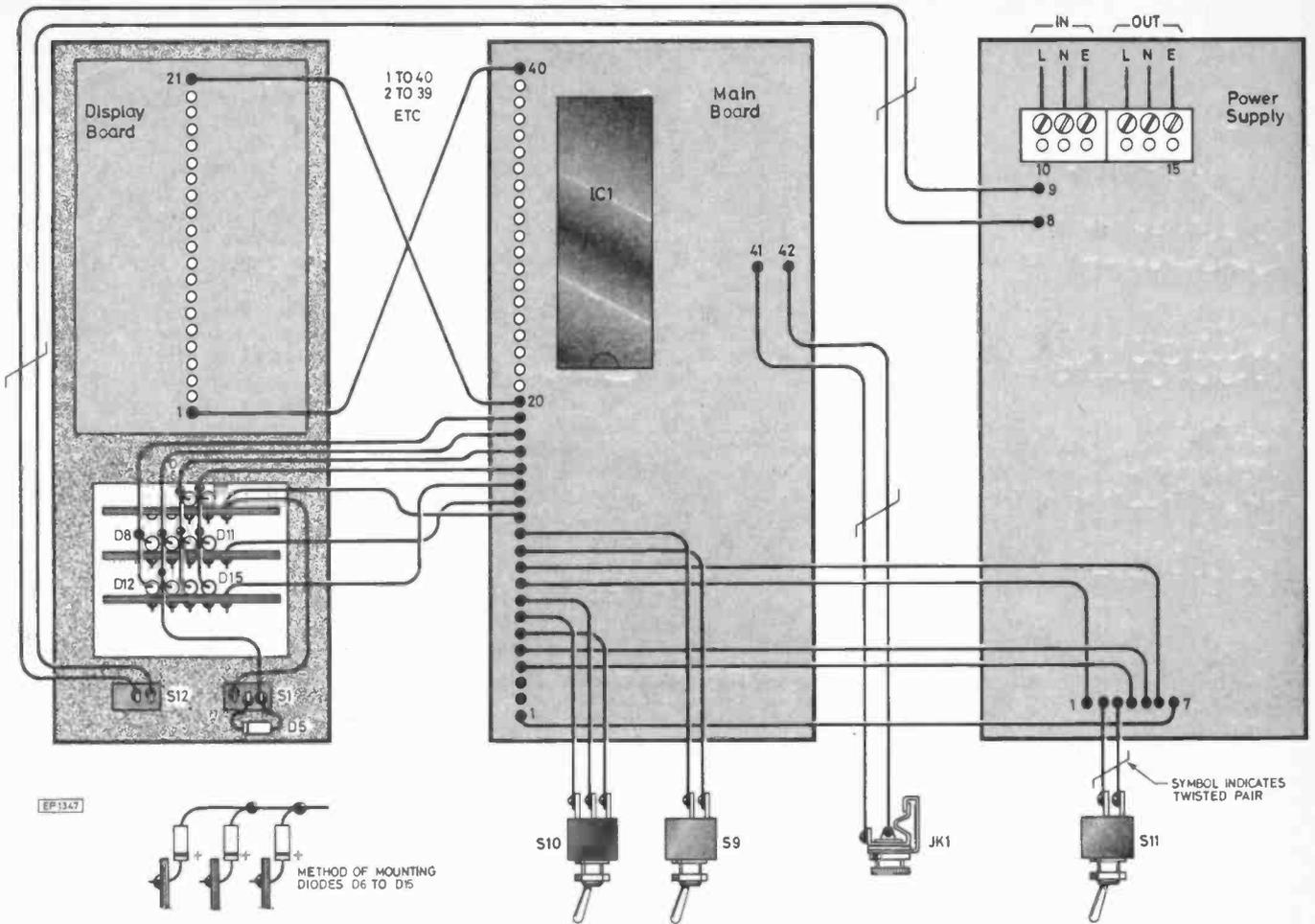


Fig. 12. Wiring details

The last adjustment is to set the required hysteresis, i.e. the margin allowable before the control outputs turn on. There are seven levels: 0, ± 0.2 , ± 0.4 , ± 0.8 , ± 2 , ± 4 and ± 8 , and one particular level should be decided on before the front panel is fitted. Table 1 gives the required switch settings. In the prototype the level was set at $\pm 0.4^\circ$ i.e. just S3 was on. Remember that S5 should always be turned off.

After the above adjustments have been made the unit is then ready for use.

Alternatively an l.e.d. display may be used. The display should of course not be multiplexed, and current limiting resistors should be inserted between all connections. If an l.e.d. display is used S5 should be switched on, inhibiting the l.c.d. back plane signal. ★

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My jumbo edition of Collins English Dictionary—which also does a fine job as a doorstop when not casting light on my etymological darkness, tells me that the word 'robot' means 'any automated machine, programmed to perform scientific mechanical functions in the manner of a man'.

So far so good. But old Collins, bless his heart (and those of his heirs and successors), was never one to do things by halves. Or to mask the complete truth from those who seek it. So he chucks in a bonus by explaining that 'robot' is derived from the old Slavonic 'robotas' which stands for 'servitude'. Which goes to prove that history, like the radish, is forever repeating itself.

But if you want to know more about robots in the modern sense, you should talk as I did to John Reekie, who, incidentally, must surely have some connections with Edinburgh, or 'Auld Reekie' as the locals are proud to call it. John's the founder and managing director of Colne Robotics, a young and lively enterprise based in somewhat cheerless premises (mind you, it was a lousy day) near the upper reaches of the Thames at Twickenham.

But don't be misled. The 18-plus people who work for John are far from cheerless characters. Their enthusiasm for and dedication to this comparatively new manifestation of electronics is complete. OK. So some of them may not show up for work until it's time for elevenses. But they'll stay on the job until midnight if the need arises. They may not be models of sartorial elegance—faded jeans and T-shirts abound. But that is of no consequence. *Haute couture* is not the business they're in. First names, from Reekie himself down to the newest recruit, are in common usage. John, a non-conformist if ever there was one, is adamant that this kind of informal and flexible attitude to working life produces the best creative results. I couldn't agree more.

John was trained as an economist (LSE and all that) and specialised in investment analysis. I didn't like to ask what that is. But I'm pretty sure that at no time in my life would I have required his services. My £12.50 in Nationwide doesn't call for much analysing. When the watershed of his late 30s loomed up he became disenchanting with the analysis lark. Maybe he'd read somewhere, as I did, that if all the economists in the world were laid end-to-end you could never expect them to arrive at a unanimous conclusion. Happily, he'd long been a keen electronics hobbyist and began to turn what had been a pastime into a living.

"I generated a number of products," he said. "Most of them were in the field of medicine—perception-speed devices for use in psychological research, for example. But it soon became clear to me that there was an enormous market potential in the educational

sector for products which would enable students and pupils to start *applying* their freshly-gained computing skills and growing awareness of the vast possibilities of information technology.

"I felt that the so-called 'computer literates' needed to be weaned away from the notion that computer skills are an end in themselves. A niche needed to be opened up for peripherals which could be seen to operate in real time in the environment." This marked the emergence of Colne Robotics.

As microcomputers began to arrive in increasing numbers in schools, Colne moved in to fill the gap with what John describes effectively as 'applied microprocessing'.

His Armdroid 1 microbotic arm quickly found its way into universities, colleges of further and higher education and secondary schools. Some of the bigger industrial concerns, too, rapidly caught on to it as a means of familiarising their workers with robotic technology. And a number of laboratories are now using it in such applications as the handling of hazardous materials.

"The only object of work is not to go on working"

During my visit to Twickenham I was officially introduced to Armdroid 1. Frankly, though I don't want to hurt his feelings, I didn't find him a handsome chap. A bit too Lost-World-ish for my liking. But he was, like the natives, friendly enough and left me in no doubt about his amazing versatility. I think I was fully accepted when he picked up a torch battery and deposited it in my outstretched palm in what I can only call a grand manner. If he has a fault, it's that he's a bit of a show-off.

Colne was well aware of the needs of primary schoolchildren. They were given the chance to acquire direct experience of keyboards and peripherals by the introduction of Zeaker, the Colne version of the Turtle mobile robot devised by Pappet in the USA.

"Zeaker," said John, "has brought a lively and entertaining form of robotics into schools operating on a low budget. Simple, robust construction and reasonable pricing have put this product within reach of the desired market. And of special significance is the fact that both Zeaker and Armdroid have helped to trigger research along the lines of robotic devices to help the disabled."

Other products coming out of the Thames-side stable are aimed at the higher end of the educational scale. Typical of these is the Colvis vision system which can be used to

teach the principles of image-processing and feedback. Much interest has been shown here by industry. One example is the recognition and orientation of items in confectionery production. One is almost tempted to say that sweet are the rewards of technological innovation.

Another Colne venture—described in detail in the January issue (*News and Market Place*)—is a computer numerically-controlled lathe. "We maintain," says John Reekie, "that the price, which includes tools, accessories and handbooks, is realistic and that the product itself meets the needs of those educational establishments which seek to teach tomorrow's engineers the skills required to gain maximum benefit from this extension to computer technology."

Getting down to sordid financial practicalities, Colne has been fortunate enough not to have operated in isolation. Prutec—the technology investment arm of Prudential Assurance—who are no slouches when it comes to recognising a winner, have consistently supported the company with encouragement, ideas and finance to the extent, to date, of £350,000.

It says something for Prutec's enlightened approach to the atmosphere of a modern undertaking that they have not been put off by the easy informality, the strictly non-City working hours and other contemporary and unconventional aspects of the Colne venture. In fact, the relationship has been eminently productive on a number of working fronts.

Looking at the social implications of the spread of robotics, John Reekie is honest and realistic. "Of course, there are going to be problems, serious problems. They're constantly being pointed out to us and we're all familiar with them. Widespread reductions in workforces, the need to share working time and all the rest of it.

"But in my view it would be utterly wrong to adopt the policy that because these problems exist—and they won't go away—we should opt out and abandon all our activity in the field of robotic advance. Believe me, others won't."

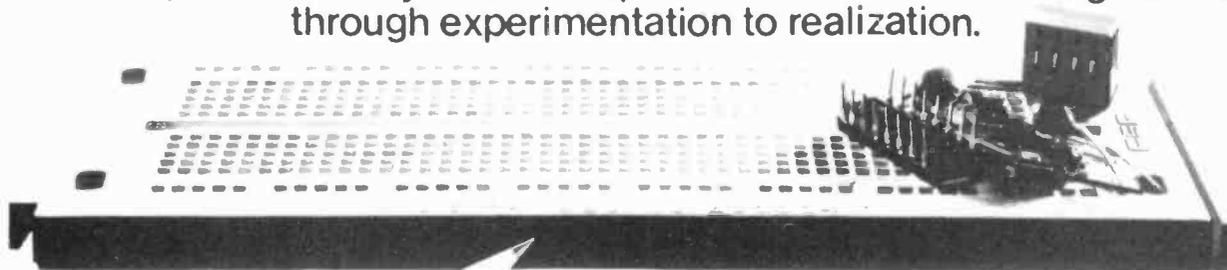
John Reekie is not the only one whose dreams revolve about a robotic future. Hoover, according to newspaper reports, is working on a remotely-controlled version of the vacuum cleaner invented more than 70 years ago. They claim it will whisk over the carpets while the housewife guzzles her coffee, operated by a joystick like a game of Star Wars. Eventually it could embody a programming facility, enabling the machine to find its way around all the rooms in the house, unaided by human hand. But that, at probably three times the cost of a hand-operated version, could be many years ahead.

There is someone else who shares John Reekie's philosophy. Indeed, his sentiments were echoed with an economy of words, rare in a Parliamentarian, by ex-Premier Harold Macmillan (justifiably dubbed Supermac) in a TV interview on the eve of the opening of his 90th year. A wily bird, as full of wit and wisdom as of years, he said: "We must realise that the only object of work is leisure," and added, "the only object of work is not to go on working."

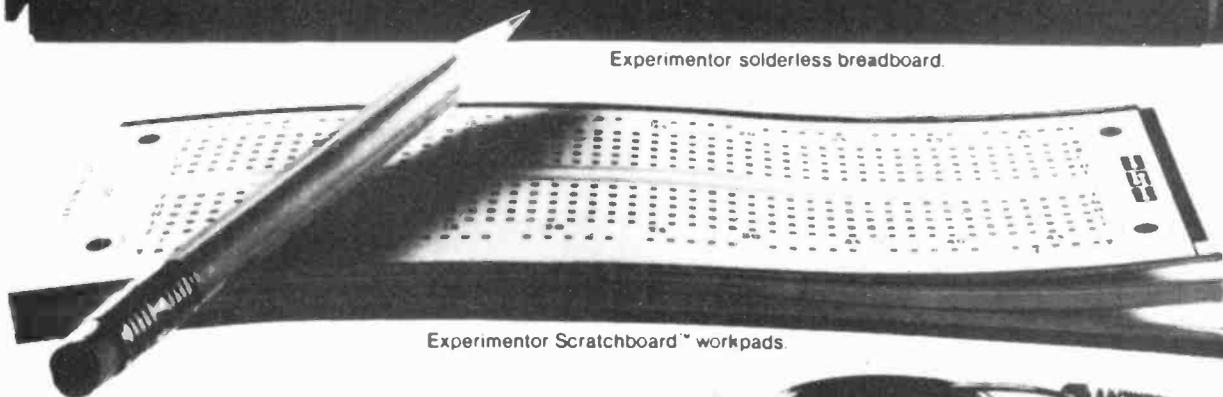
Those of us who would say Amen to that must be legion.

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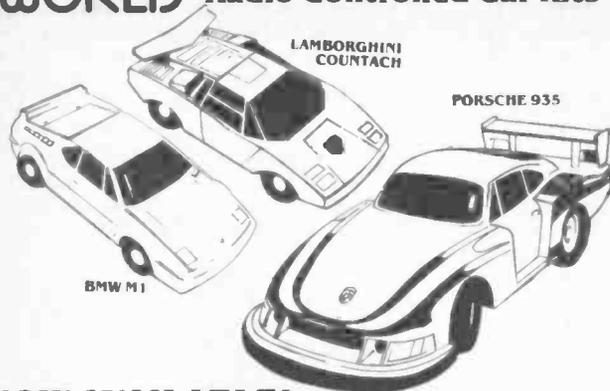
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Space Watch...

SHUTTLE 8

As part of its tests SHUTTLE 8 confirmed that the Tracking and Data Relay satellite (TDRS) could quite ably keep track of the vehicle. It showed that the overall performance of the TDRS system was well within its design specification. The Ku-band link using the Shuttle's dish aerial was quite successful and performed as scheduled. Some difficulties were encountered, the orbiter's S-band aerial was still causing some problems with communications through the geosynchronous-orbit relay satellite.

There are several S-band aerials aboard the shuttle and depending on the TDRS viewing angle those aerials have to be cycled. When using the S-band aerials for ground operation the decibel margin required is 40dB for 'lock'. The signals reaching TDRS are only 4-5dB. This of course means that S-band/TDRS locks are more difficult to achieve. Valuable experience was also gained in the operation concerning the interaction between the Johnson Space Flight Center, the Goddard Space Flight Center and the White Sands N.M. TDRS ground station. Robert O. Aller, the Director of TDRS for NASA, stated that the mandatory systems objectives had been achieved and successfully accomplished.

AT LAST THE BLACK HOLE

Some time ago because of false-alarms concerning Black Holes it was decided that until there was concrete evidence the subject would be kept in the background. Now the situation has changed. This *Spacewatch* contains the momentous scientific release from the Science and Engineering Research Council (SERC).

After studying ultra-violet emissions from a nearby galaxy an International research team with leading members from the Royal Greenwich Observatory 'weighed' a Black Hole. They came to the conclusion that the quasar like object NGC 4151 is powered by a black hole which is about 100 million times heavier than the Sun. The Sun though shedding its mass has a weight of 2×10^{27} tonnes. The relationship gives some idea of the magnitude of the matter involved.

This is the first time that astronomers have 'weighed' the centre of a quasar and the discovery now strengthens the theory that the immense and concentrated energy of a quasar is due to gas that is revolving round a black hole in the centre of a galaxy (Fig. 1). The team have been studying NGC 4151 since 1978. In

order to 'weigh' the centre they investigated the gas clouds very close to the Galaxy's core. In a crucial new step they obtained the distances of the clouds from the core. They found that the clouds were moving at speeds of up to 14 thousand km/second.

These figures were ascertained by finding the time taken for the core to 'light-up' the clouds. It was calculated that the slower moving clouds were those furthest from the core and were thus slowing in a way similar to the planets of our Sun. This means that the centre of the galaxy is a very massive object. Calculations show that the weight is 100 million times that of the Sun; only a Black Hole could have the mass and yet be as small as NGC 4151.

Professor D. Lyndon-Bell of the Institute of Astronomy at Cambridge proposed in 1969 that quasars were caused by black holes at the centres of galaxies—gas from the galaxy spirals inwards under the influence of the black hole's gravity, in the process the clouds become hot and produce radiation. The powerful quasars would have a black hole some 500 million times heavier than the Sun, these however being far away at the edge of the Universe. Many more galaxies would have smaller central black holes 50 to 100 times as massive as the Sun. There would thus arise mini-quasars at the centre of a small yet otherwise normal galaxy. NGC 4151 fits this description exactly. It is a spiral galaxy similar to our own but it has a centre mini-quasar. It is some 50 million light years from Earth in the direction of the constellation Canes Venatici. It is a Seyfert Galaxy, so called after the first astronomer to study them, Carl Seyfert.

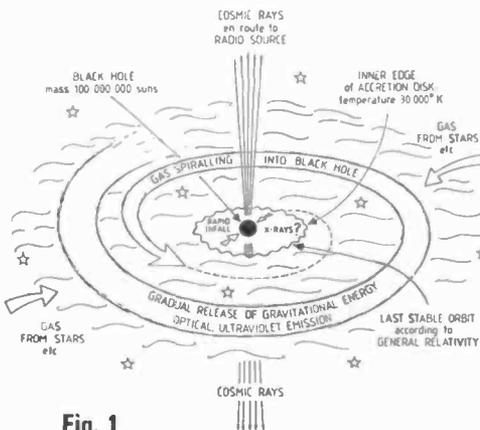


Fig. 1

The researchers from the UK, France, Italy, Sweden and Germany investigated the core using the 45cm telescope on board the IRAS satellite. This is the satellite whose quite startling successes have given it such publicity in the field of ultra-violet astronomy. The team discovered that there were other considerations. While the greater part of the core gives ultra-violet radiation there also arise spectral lines which come from the gas clouds outside the core. So far three different spectral lines have been discovered. These are first of all emissions characteristic of carbon atoms, secondly those of magnesium, the third being another carbon wavelength. Detailed studies reveal that they move at different speeds. Up to speeds of 14,000, 11,000 and 4,000km/se-

cond respectively. The core's radiation lights up the clouds, and the team noted that there was a delay between the flaring up of the core and the clouds becoming brighter. The delay is most likely to be due to the finite time that it takes the radiation to travel from the core to the clouds.

The delays from the three types of cloud are different. The highest speed cloud covers the distance in 13 days. This shows that the distance is 13 light days. The second fastest clouds take about 30 days, they must be therefore 30 light days distant. The other clouds must be about one light year or more away from the core. For each type of cloud the application of Newton's law of gravity can be applied, the speed and distance from the core gives the mass as being that of 100 million suns.

It is also true that this confirms the black hole theory in another way. As the gas spirals into the black hole it should form into a swirling 'accretion' disc and where the gas is close to the black hole it should have a temperature of 30,000°C and stretch to ten times the size of the black hole itself. The hottest point will be near to the edge of the disc producing most of the core's radiation. In the rest of the disc there should be the characteristic ultra-violet. The observations so far have borne this out. This must be another milestone in the unfolding of the mysteries of our Universe.

TWO NEW SERC MISSIONS

In Bonn, West Germany, Professor J. Kingsman FRS, Chairman of the Science and Engineering Research Council, and Dr. Hans-Hilger Haunschild, State Secretary of the Federal Ministry for Research and Technology, will sign agreements through which the UK scientists will participate with Germany and the USA in two space missions. One is called AMPTE and will investigate the space plasma surrounding the Earth at vast distances and the other is ROSAT which is for X-ray astronomy. Present at the signing ceremony will be Mr. Peter Brooke MP, Parliamentary Secretary of State for Education and Science.

These collaborations are well suited to the balanced programme of geophysics and astronomy supported by the SERC and will enable UK scientists to continue to carry out research in areas where they originally established international reputations through earlier UK satellites and through participation with European Space Agency missions.

The first mission AMPTE (Active Magnetospheric Particle Tracer Explorers), will study space plasma physics. Its purpose will be to investigate how solar energy, carried by the solar wind, is intercepted and stored as charged particles forming the Earth's radiation belts and the other parts of the comet-shaped magnetosphere. These belts surround the Earth out to distances of more than 100,000km. The stored energy eventually becomes deposited in the upper atmosphere where it produces heating, ionisation and the Aurora Borealis.

The second agreement concerns the German Röntgensatellit which will carry a German 0.8 metre X-ray telescope and a UK wide-field camera. The latter is of novel design optimised for the soft X-rays and the extreme ultra-violet band.

INTRODUCTION TO DIGITAL ELECTRONICS

MICHAEL TOOLEY BA DAVID WHITFIELD MA MSc CEng MIEE

O & A Level Part Five

IN ANY other than the most elementary of logic circuits, we sooner or later realise the need for a device which can remember a logic state. Such a device should possess the ability to remember a transitory logical condition and thus constitutes a simple form of electronic memory, the most fundamental form of which is the bistable. (The name simply indicates that the device has two stable states corresponding to outputs of either 1 or 0.) Another word synonymous with bistable is "latch". To explain the significance of this term let us consider the difference between two commonly available types of switch: "momentary" and "latching".

A momentary switch is one in which the switch contacts make (or break if it is a normally closed, rather than normally open, type) only when the switch is being operated. This is, for example, the case with a bell-push. We only want the bell to sound when the button is actually being pushed. It should not be possible for callers to walk away leaving the bell ringing!

A latching switch is one in which the contacts make (or changeover) whenever the switch is operated and, once operated, the mechanical design of the switch ensures that it remains biased in that state until operated again. A word sometimes used to describe this action is "toggle". In simple terms this means: operate once for 'on' and again for 'off'. An example of a switch with a mechanical latching action is that associated with a normal room light. Once the switch is operated, the room light must stay 'on' allowing one to move away from the switch!

In the previous example, sharp eyed readers might have noticed that we

were careful to use the term "mechanical latching". It is, of course, eminently possible for a momentary switch (such as a push-button) to be coupled with an electronic circuit such that the combination forms an "electrically latching" switch. Fortunately, we don't have to look very far for an example of such a device. Just such an arrangement is incorporated in the PE Logic Tutor!

At this point, and to make absolutely certain that we can distinguish between the two types of switch, it is recommended that readers take a brief look at the way in which the Logic Tutor switches operate. Press S1 (or S2) and notice that the associated l.e.d. lights only when the switch is actually depressed. Press S3 (or S4) and notice that its l.e.d. stays 'on' when the button is released, and remains 'on' until the switch is pressed for a second time. All this may appear to be labouring the point. It is, however, quite crucial since we must make a very clear distinction between logic devices which operate on a momentary basis, and those which operate on a latching basis.

BISTABLE LATCH USING INVERTERS

The simplest form of bistable arrangement uses two inverters, as shown in Fig. 5.1. We should, by now, be quite familiar with the way in which an inverter operates: a 1 input

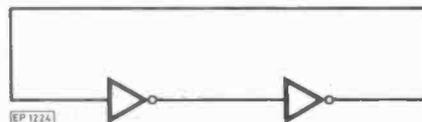


Fig. 5.1. Simple bistable latch using two inverters

produces a 0 output, and vice versa. The logical state of the outputs of the two gates in Fig. 5.1 must, therefore, always be complementary. If the first gate is producing a 1, the second gate must produce a 0. If the first gate produces a 0, this must result in a 1 from the second gate. If we were to assemble such a circuit the state of its outputs would, initially at least, be indeterminate. It would be impossible to say which of the outputs would assume a logic 1 state and which would assume a logic 0 state. Worse than that, there is no obvious method of changing the state other than by shorting one, or other, of the outputs to logic 0 in order to force the logical state at that particular point to become a 0. Such an arrangement is not considered good design practice but, don't worry, we shall show how this problem can be overcome later.

The time has now come to introduce a first practical example of the use of a bistable. Let's imagine that we require a logic system to control the operation of a pump. We wish to use two push-buttons to control the pump; one to switch it on (Pump On) and one to switch it off (Pump Off). The arrangement in Fig. 5.2 shows how these switches can be added to the simple bistable latch of Fig. 5.1. We simply pull-down the input of one, or other, gate to 0V momentarily whenever the

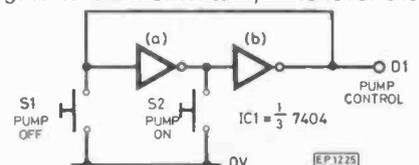


Fig. 5.2. Use of switches to control the operation of the simple bistable latch

appropriate switch is operated. If this all sounds too simple, check it out using the Logic Tutor as shown below!

Insert a 7404 hex-inverter into socket A of the Logic Tutor, checking as usual that pin 1 aligns correctly with the connection marked 'A1'. Now make the following links:

- A1 to S1 (S1 is the Pump Off switch)
- A2 to A3
- A3 to S2 (S2 is the Pump On switch)
- A4 to A1
- A4 to D1 (D1 indicates that the pump is running)
- A7 to 0V (0V)
- A16 to +5V (positive supply)

Note that, when the power is first applied, D1 may either be in the illuminated or extinguished state. Disconnecting the power supply and then reconnecting it again may sometimes effect a change of state but this cannot be relied upon. It will, therefore, be necessary to re-set the bistable latch into the inactive condition by first pressing S1 (Pump Off) as soon as the supply has been connected. (On real logic systems there are, of course, quite simple methods of achieving this automatically!) Then momentarily depress S2 (Pump On) and check that D1 becomes illuminated. Depressing S2 for a second time should have no further effect on the logical state of the circuit. Now momentarily depress S1 (Pump Off) and check that D1 is extinguished again.

By now, the perceptive reader may have counted three quite different logical input conditions. These may be summarised briefly as:

- (a) S1 'off' and S2 'off'.
- (b) S1 'on' momentarily whilst S2 remains 'off'.
- (c) S2 'on' momentarily whilst S1 remains 'off'.

There is, of course, one further possible input condition. This occurs when S1 and S2 are both 'on'. This condition would arise if we were foolhardy enough to operate both push-buttons at the same time (i.e. operating Pump On and Pump Off simultaneously). Such a condition is clearly one which should, if at all possible, be forbidden or prevented. But what happens if you actually try it?

SWITCH BOUNCE

Before continuing with a discussion of improved bistable arrangements, we shall digress a little to mention a topic which must, at some time or other,

have been or will be of concern to nearly every designer of digital logic circuits. This involves a gremlin known as "switch bounce". We mentioned, right at the start of Part One, that one of the pitfalls of overlooking the differences between 'perfect' paper devices and their real-life counterparts was that we sometimes produce circuits which should work, but don't. Switch bounce is a classic example of this. We all too often regard switches as perfect devices which are either 'on' or 'off'. What we overlook in this particular case is what happens at the instant of changing over from the 'off' to the 'on' state, and vice-versa. Most switches are far from perfect in this respect; they just don't change over cleanly. When the switch is operated, its contacts bounce and make repeated contact, 'on' and 'off', until they settle to their final condition. Admittedly, this takes a very short time. In TTL terms, however, this interval is quite considerable and thus the circuit reacts to each and every one of the bounces just as if the switch were being manually operated.

Fortunately, the problem of switch bounce can be very easily solved. The simple bistable latch which we met earlier changes its logical output condition whenever the relevant input connection is briefly taken to 0V. It then blissfully ignores any further changes on that particular input, only reverting back to its original state when the *other* input is taken to logic 0. Hence, all we need is a simple changeover switch arrangement, as shown in Fig. 5.3. This is all fairly straightforward;

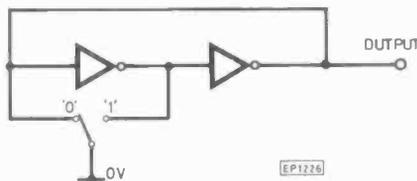


Fig. 5.3. Switch de-bouncing arrangement

however, we still have an arrangement which, although fairly harmless, is rather inelegant when one considers that triggering is achieved by shorting out the output of one, or other, of the two gates.

AN IMPROVED BISTABLE

The obvious solution to the problem of constructing a bistable is with the use of two-input gates rather than inverters. This eliminates the need to short the gate outputs in order to effect

a change of state. It should also be obvious that the gates we choose must be inverting; a non-inverting gate will not produce the complementary state that we require in order to latch the bistable. It thus remains to choose between two-input NOR or two-input NAND gates but, happily, we can use either and thus we shall describe bistables using both types. The bistable constructed from NOR gates is slightly easier to describe and we will therefore start with this type.

Fig. 5.4 shows how a bistable can be constructed from two two-input NOR gates. We have labelled the inputs

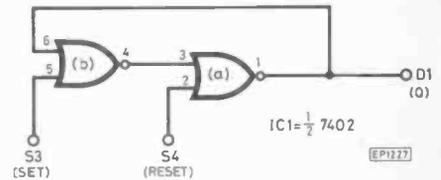


Fig. 5.4. Bistable using two-input NOR gates

'SET' and 'RESET'. The reason for the choice of these terms is that a 1 on the SET input produces a 1 at the output. We would say that it "sets the output" (to logic 1). Conversely, a 1 on the RESET input produces a 0 at the output. It can thus be said to "reset the output" (to logic 0). The output is labelled 'Q'. There is no particular significance in the choice of this letter other than that it satisfies the convention adopted for bistable elements generally.

Since the inputs are named RESET and SET, this simple form of bistable is called an 'R-S bistable'. We now continue with a practical investigation of an R-S bistable using two-input NOR gates.

R-S BISTABLE USING A 7402

The 7402 is a quad two-input NOR gate which we met in Part Three and thus only half the i.c. needs to be used in the R-S bistable investigation. As usual, the 7402 should be inserted into socket A of the Logic Tutor ensuring, of course, that pin 1 aligns with the connection marked 'A1'. The following links are required:

- A1 to D1 (D1 indicates the output state, Q)
- A2 to S4 (S4 is the RESET input)
- A3 to A4
- A5 to S3 (S3 is the SET input)
- A6 to A1
- A7 to 0V (0V)
- A16 to +5V (positive supply)

Set up S3 and S4 to produce logic 0 outputs. Ensure that D1 is 'off', i.e. the Q output is a logic 0. Now press S3 (leaving S4 at logic 0). This produces a logic 1 at the SET input. D1 should immediately come 'on' indicating that the Q output has changed state to logic 1. Press S3 again to produce a logic 0 (leaving S4 at logic 0). D1 should remain 'on' and no further change should be evident; the bistable has "remembered" that it has been set. Now press S4 (leaving S3 at logic 0). D1 should go 'off' and the Q output should immediately revert to logic 0. Pressing S4 again (leaving S3 unchanged at logic 0) should have no further effect; the bistable "remembers" that it has been reset.

In Part Two we learned how useful truth tables could be for describing the logical function of a gate. Let's now take a look at the truth table for the R-S bistable which is shown in Table 5.1. Note that we started the previous

RESET	SET	Q
0	0	0
0	1	1
1	0	0

Table 5.1. Partial truth table for the NOR gate R-S bistable

exercise with a Q output of logic 0 when both RESET and SET were also at logic 0. A 1 on the SET input made the Q output change to 1; a 1 on the RESET input made the Q output change to 0.

Another way of drawing the bistable arrangement using NOR gates is shown in Fig. 5.5. This symmetrical cir-

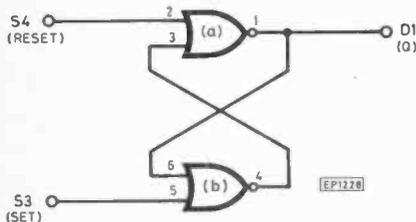


Fig. 5.5. Another way of drawing the NOR bistable

cuit shows clearly how the gate outputs are cross-coupled to the inputs. It also shows that we are only using one of two possible outputs. It would be a very simple matter to obtain a complementary, \bar{Q} , output from the gate, which may be useful in a more complex logic circuit. To adapt our earlier arrangement all we need is the following additional link on the Logic Tutor:

A4 to D2 (D2 indicates the \bar{Q} output state)

It is worthwhile repeating the previous exercise and noting the effect on the \bar{Q} output. The truth table should be the same as that obtained in Table 5.2. But, wait a minute, didn't we say

RESET	SET	Q	\bar{Q}
0	0	0	1
0	1	1	0
1	0	0	1
1	1	0	0

Table 5.2. Complete truth table for the NOR gate R-S bistable

earlier that the state of the Q and \bar{Q} outputs would always be complementary? This is obviously not the case for one particular combination of the inputs, i.e. SET = 1, RESET = 1. This is somewhat disconcerting since it clearly contravenes the rules which we have established. In future we shall refer to this particular input condition as "disallowed" and, whilst not wishing to pretend that such a condition cannot arise, we should take active steps to ensure that it is prevented. Or, at the very least, if it does occur we should be aware and not place any reliance on the output.

R-S BISTABLES USING NAND GATES

Simple R-S bistables can also be constructed using two-input NAND gates, such as the 7400. A typical arrangement is shown in Fig. 5.6. The

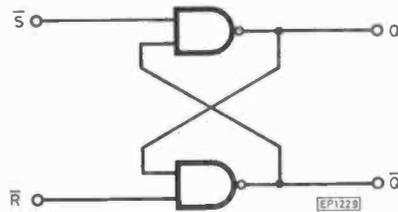


Fig. 5.6. R-S bistable using two-input NAND gates

important difference between this arrangement and that of the NOR gate equivalent is that the SET and RESET inputs are logically inverted, i.e. they are active when they are at logic 0 rather than when they are at logic 1. This is an important point and one which we shall come across later in Part Six. Sometimes these inputs are referred to as "active low" (on some logic diagrams a circle is used at the input of more complex logic gates to indicate this); however we shall simply refer to them as NOT SET, \bar{S} , and

NOT RESET, \bar{R} . If it is essential to have conventional SET and RESET inputs to the bistable it is, of course, a relatively simple matter to invert these signals prior to the bistable stage. With a 7400 quad two-input NAND we could, for example, achieve this by bringing into service the remaining two unused gates in an arrangement like that shown in Fig. 5.7. The operation of the bistable is then identical to that of the NOR gated bistable which we met earlier.

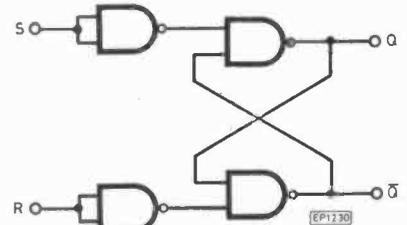


Fig. 5.7. NAND gate R-S bistable comparable with the NOR gate version

CLOCKED BISTABLES

Whilst the simple R-S bistable element is useful in a number of applications, it does have significant disadvantages when several such stages are to be incorporated in a complex logic system. The problems arise from the way in which changes of state occur in the system. Earlier, we demonstrated how the R-S bistable changed state immediately the correct SET and RESET inputs are received. At first this may sound quite acceptable; after all one of our chief aims with the design of most circuits is to produce the fastest possible speed of operation.

The difficulty with R-S bistables is that such rapid changes are not very predictable. In many cases we have what is known as a "race condition", in which the logical output from a system may well be determined by the speed at which individual gates operate rather than the logical rules which they should obey. What we really need is a system in which the changes occur in a controlled fashion. In such a system we can accurately predict the output states, and all we need is a means of synchronising the changes within the system. This leads us to the very important concept of "clocked logic"; a logic system which employs a clock signal to control the transfer of logical information from one stage to the next.

CLOCKING THE R-S BISTABLE

When we talk about clocked logic circuits, we always assume the

presence of a clock signal. At this stage it is useful to have some idea of the type of signal involved. The most common clock signal is one where the level varies between 0 and 1 at a constant rate, and spends an equal amount of time at each level before changing. This is a so-called square wave clock signal, and the rate at which the changes occur affects the speed at which information can pass through the system. Now for how such clock signals are used in logic circuits.

The simplest way of constructing a clocked bistable is to add two AND gates ahead of the bistable stage, as shown in Fig. 5.8. The CLOCK and

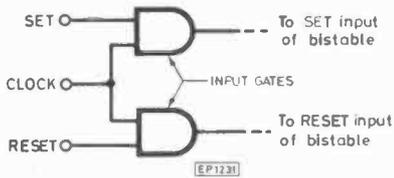


Fig. 5.8. Input gates of a clocked R-S bistable

SET signals are applied to one of these gates, and the resulting signal is then passed on to the bistable's SET input. Similarly, CLOCK and RESET signals are applied to the other AND gate, and the resultant output is passed on to the bistable's RESET input.

In this way, a logic 1 only appears at the SET and RESET inputs of the bistable stage when both input and clock are at a logic 1. In effect, this means that data, in the form of 1's and 0's, can only pass into the bistable when the clock is at a logic 1. When the clock signal is at a 0, no changes can occur on the SET and RESET inputs of the bistable stage. Each time the clock is at a 1, changes can occur.

We will now move on to combine the logic arrangements in Fig. 5.4 and Fig. 5.8 in order to construct a complete, clocked R-S bistable.

CLOCKED R-S BISTABLE USING 7402 AND 7408

A clocked R-S bistable can be made using 7408 quad two-input AND and 7402 quad two-input NOR gates, as shown in Fig. 5.9. Two gates of each device are employed: the 7408 providing the input gating, whilst the 7402 forms the bistable element. The 7408 should be placed in socket A of the Logic Tutor whilst the 7402 should be inserted in socket B. Care should be taken to ensure the correct orientation with pin 1 of both devices aligning with 'A1' and 'B1' respectively. The follow-

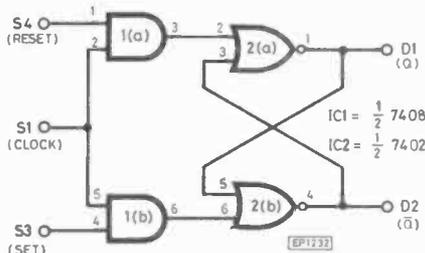


Fig. 5.9. Clocked R-S bistable using 7402 and 7408 gates

ing links are required on the Logic Tutor:

- A1 to S4 (S4 will act as the RESET input)
- A2 to A5
- A3 to B2
- A4 to S3 (S3 will act as the SET input)
- A5 to S1 (S1 will provide the CLOCK input)
- A6 to B6
- A7 to 0V (0V)
- A16 to +5V (positive supply)
- B1 to D1 (D1 indicates the Q output)
- B3 to B4
- B4 to D2 (D2 indicates the Q-bar output)
- B5 to B1
- B7 to 0V (0V)
- B16 to +5V (positive supply)

The procedure for testing the bistable is fairly complex and readers are advised to follow the stages carefully, repeating the whole exercise until they become thoroughly familiar with the way in which the circuit operates. The six stages are as follows:

Stage 1. Apply power to the Logic Tutor and note the output state of S3 and S4 by examining their respective l.e.d. indicators. If either, or both, of these l.e.d.s are illuminated this indicates a logic 1 output from the switch. We need to start the investigation with logic 0's on both the SET and RESET inputs. Thus S3 and S4 may need some initial adjustment to ensure that this is the case.

Stage 2. Having ensured that the SET and RESET inputs are both at logic 0, note down the state of the Q and Q-bar outputs by examining D1 and D2 respectively. Readers should be aware that it is not possible to predict the initial state of the Q and Q-bar outputs, other than that they should, of course, be complementary! In any event, we need

to know what their initial state is so that we can detect any subsequent change when we apply logic 1 to the SET and RESET inputs.

Stage 3. Press S1 in order to generate a momentary logic 1 at the CLOCK input. There should be no change in the state of the Q and Q-bar outputs; the circuit "ignores" the CLOCK input when SET and RESET are both at logic 0.

Stage 4. Now press S3 to produce a logic 1 at the SET input leaving S4 at logic 0. Check that the Q and Q-bar outputs are still the same as before, and then press S1 to produce another momentary logic 1 at the CLOCK input. The results of momentarily pressing S1 does not depend on the previous states of Q and Q-bar. When S1 produces the next clock input, Q goes to a logic 1, and Q-bar goes to a logic 0. The bistable has been SET.

Stage 5. Press S3 again in order to change its output state back to a logic 0. Press S4 to obtain a logic 1 on the RESET input. Check that the Q and Q-bar outputs have remained unchanged during this operation. Now press S1 to produce a further momentary logic 1 at the CLOCK input. The Q and Q-bar outputs should change state as soon as S1 is pressed and Q should become a logic 0 (and Q-bar a logic 1). The bistable has now been RESET.

Stage 6. Now press S3 to produce a logic 1 on the SET input whilst the RESET input remains at logic 1. Check that the bistable remains in its previous RESET condition. Press S1 to generate a further momentary logic 1 at the CLOCK input. Note what happens to the Q and Q-bar outputs, then press S3 again several times. The state of Q and Q-bar should appear to be somewhat random; they are affected by the clock but they change in an entirely unpredictable manner. This is, as you have probably guessed, a "disallowed" condition!

Pressing S1 repeatedly to generate a CLOCK "pulse" can be somewhat tedious and, since we have a built-in clock within the Logic Tutor, it seems sensible to use this instead of relying upon manual operation of the clock. The modification to the Logic Tutor wiring is simply that of removing the link from A5 to S1, and installing a link from 'A5' to 'CLOCK'. After a little further experimentation, it should become very obvious that "data", in the form of SET and RESET inputs, is transferred into the bistable whenever the clock input goes to logic 1.

TRUTH TABLE FOR THE CLOCKED R-S BISTABLE

Earlier we looked at the truth table for a simple R-S bistable. Now let's see what effect the CLOCK input has on this. Table 5.3 shows the truth table for a clocked R-S bistable. At first sight

SET	RESET	Q_{n+1}	\bar{Q}_{n+1}	COMMENTS
0	0	Q_n	\bar{Q}_n	NO CHANGE
1	0	1	0	Q OUTPUT SET TO LOGIC 1
0	1	0	1	Q OUTPUT RESET TO LOGIC 0
1	1	?	?	INDETERMINATE - DISALLOWED STATE

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Table 5.3. Truth table for a clocked R-S bistable

this may look very similar to that for the simple R-S bistable but note that the output states in the truth table all assume that a clock pulse has just been received, i.e. after the clock input changes from 0 to 1. The main points to note are:

(a) There are two inputs, SET and RESET, and two outputs, Q_{n+1} and \bar{Q}_{n+1} . An extra column has been incorporated for "comments" to explain what happens to the outputs after the clock input changes.

(b) A subscript notation has been adopted in conjunction with the Q and \bar{Q} outputs. This is simply a means of abbreviation: Q_n merely denotes the state of the Q output *before* the clock changes whereas Q_{n+1} denotes the state of the Q output *after* the clock transition.

(c) With SET and RESET inputs both at logic 0, the next Q output (Q_{n+1}) is the same as the previous output (Q_n). The same is true for the complementary output, \bar{Q} . There is thus no change in the state of the bistable outputs.

(d) With both SET and RESET inputs at logic 1 a disallowed state exists and the output state, after the clock pulse, is indeterminate.

(e) With SET at logic 1 and RESET at logic 0 the bistable is set after the clock pulse, i.e. $Q_{n+1} \rightarrow 1$.

(f) With RESET at logic 1 and SET at logic 0 the bistable is reset after the clock pulse, i.e. $Q_{n+1} \rightarrow 0$.

LEVEL VERSUS EDGE CLOCKING

In the clocked bistable which we have just considered, a logic level of 1 at the clock input caused the SET and RESET inputs to the bistable to become active. It may thus be referred to as a "level-clocked" bistable. This is

satisfactory for a number of applications, but is still far from ideal since, during the period in which the clock is at logic 1, changes which occur on the SET and RESET inputs will affect the state of the output. In practical logic systems this can cause problems. A much better bistable element would be one in which the condition on the SET and RESET inputs could be changed at any time with the certain knowledge that the bistable would only react at the instant of time when the clock next changed from a logic 0 to a logic 1 (or from logic 1 to logic 0). Such a bistable is referred to as an "edge-clocked" bistable and is ideal for use in logic systems where a number of bistables are connected in tandem. Data is then transferred, from one stage to the next, on each rising (or falling) clock transition.

D-TYPE BISTABLES

A further improvement on the R-S bistable can be obtained by adding an additional input which determines the state of the outputs at the instant the clock changes. This, edge-triggered, bistable is referred to as a "D-type". The "D" stands for "data" which is effectively loaded into the bistable stage when the clock transition occurs. The symbol for a D-type is shown in Fig. 5.10. This has four inputs and, as

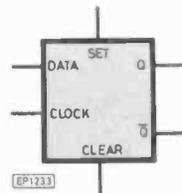


Fig. 5.10. Symbol for a D-type bistable

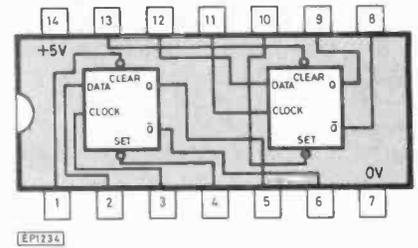
usual, two outputs. The inputs are: SET, CLEAR, CLOCK and D. The outputs are our old friends, Q and \bar{Q} .

The D-type is rather difficult to construct using individual logic gates (one can be constructed from no less than six three-input NAND gates!) and thus a purpose-designed integrated circuit version is preferred. We shall, therefore, not concern ourselves with the internal arrangement of the device which, for most applications, would be considered a purely academic exercise. Instead, we will concentrate on the characteristics and applications of the D-type.

7474 D-TYPE BISTABLE

The 7474 is a dual D-type bistable contained in a 14-pin d.i.l. package.

The internal arrangement and pin connections for the 7474 are shown in Fig. 5.11. As mentioned earlier, the small circles which appear on the SET and CLEAR inputs indicate that they are



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Fig. 5.11. Internal arrangement and pin connections for a dual D-type bistable

active low inputs. The following links are required in order to investigate the operation of the D-type in the circuit of Fig. 5.12:

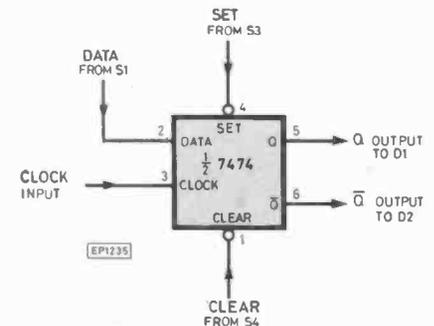


Fig. 5.12. 7474 D-type bistable circuit

- A1 to S4 (S4 is the CLEAR input)
- A2 to S1 (S1 will provide the DATA)
- A3 to CLOCK
- A4 to S3 (S3 is the SET input)
- A5 to D1 (D1 indicates the Q output)
- A6 to D2 (D2 indicates the \bar{Q} output)
- A7 to 0V (0V)
- A16 to +5V (positive supply)

The 7474 should be placed in socket A with pin 1 in position 'A1', as usual. The following steps should be followed in order to confirm that the D-type operates correctly:

Step 1. Adjust S3 and S4 to give logic 0 on both the SET and RESET inputs. (Remember that this device uses active low inputs and thus, in this condition, we are trying to SET and CLEAR the bistable at the same time!). Q and \bar{Q} will both go immediately to logic 1 in this normally disallowed state, although the behaviour is actually quite predictable for this particular bistable.

Step 2. Adjust S3 to produce a logic 0 on the SET input, and S4 to produce a

logic 1 on the CLEAR input. Q now immediately changes to (or remains at) logic 1 regardless of the state of the CLOCK input. The bistable is *set*.

Step 3. Adjust S3 and S4 to produce a logic 1 on the SET input and a logic 0 on the CLEAR input. Q now immediately changes to (or remains at) logic 0 regardless of the state of the CLOCK input. The bistable is *cleared*.

Step 4. (and this is the important one!) Adjust S3 and S4 so that both SET and CLEAR are at logic 1. Q should be at logic 0 initially whilst \bar{Q} is at logic 1 as a result of the previous step. Wait until the clock i.e.d. goes off, press S1 and hold the switch down. This places a logic 1 on the DATA input. Nothing should happen, however, until the clock goes to logic 1. When this happens, Q should change to logic 1 (whilst \bar{Q} changes to logic 0). When the clock i.e.d. goes off again, release S1 to place a logic 0 on the DATA input. Nothing should happen until the clock again goes to logic 1, at which point Q should revert to logic 0 (whilst \bar{Q} reverts to logic 1).

Readers should repeat the above exercise until they are absolutely familiar with the way in which the D-type operates. To summarise, you should have found that the SET and CLEAR inputs override the CLOCK (these are sometimes referred to as "direct" inputs since they act immediately), and the bistable is loaded with data when,

and only when, there is a positive-going (0 \rightarrow 1) clock transition. This is very important since it leads to numerous applications for the device.

TIMING DIAGRAMS

As we are now entering the world of clocked operation of bistables, it is important to have a simple and unambiguous means of describing the sequence of logical events in a circuit. This is achieved by constructing a "timing diagram". Such a diagram is simply a graph showing the logic states at various points in the circuit, plotted against a common scale of time. By referring to the diagram we can, not only accurately predict the logic states within the circuit at any instant of time, but we also identify the crucial times at which changes of state occur.

To demonstrate just how useful timing diagrams can be, let us consider the timing diagram for the previous circuit constructed around the 7474 D-type bistable. We have assumed that the SET and CLEAR inputs are both set to logic 1 and that we are following through 'Step 4' of the investigation. Readers may like to work through this step again whilst looking at the timing diagrams.

The timing diagram is shown in Fig. 5.13 and it illustrates the logic states at four points in the circuit; the CLOCK and DATA inputs, and the Q and \bar{Q} outputs. The most important

point on the clock waveform is the rising (positive-going) edge and you will notice that the changes at the Q and \bar{Q} outputs are always synchronised with this edge. The falling (negative-going) edge is unimportant, as is the precise moment at which the data input changes.

BINARY DIVIDERS

If the Q output of a D-type bistable is fed-back to its DATA input, the bistable can effectively be made to divide by two. To understand how this works, imagine that the Q and \bar{Q} outputs of the bistable are initially at logic 0 and logic 1 respectively. When the clock next changes from logic 0 to logic 1 (assuming that the device is positive edge triggered), the logic 1 at the \bar{Q} output will be transferred into the bistable such that the Q output changes to logic 1 whilst the \bar{Q} output becomes logic 0. The bistable remains in this state until the next positive clock edge occurs at which point the bistable again changes state with the Q output reverting to logic 0 whilst the \bar{Q} output becomes logic 1 again. Note that the Q output has changed from logic 0 to logic 1 and back to logic 0 in the same time that the clock has changed from logic 0 to logic 1 and back twice. It has taken two cycles of the clock to produce only one cycle at the output. This is binary division and we now have a device at our disposal which produces, in any given time interval, half as many output pulses as clock input pulses.

7474 BINARY DIVIDER

Fig. 5.14 shows how the 7474 D-type bistable can be connected to form a single stage binary divider. The

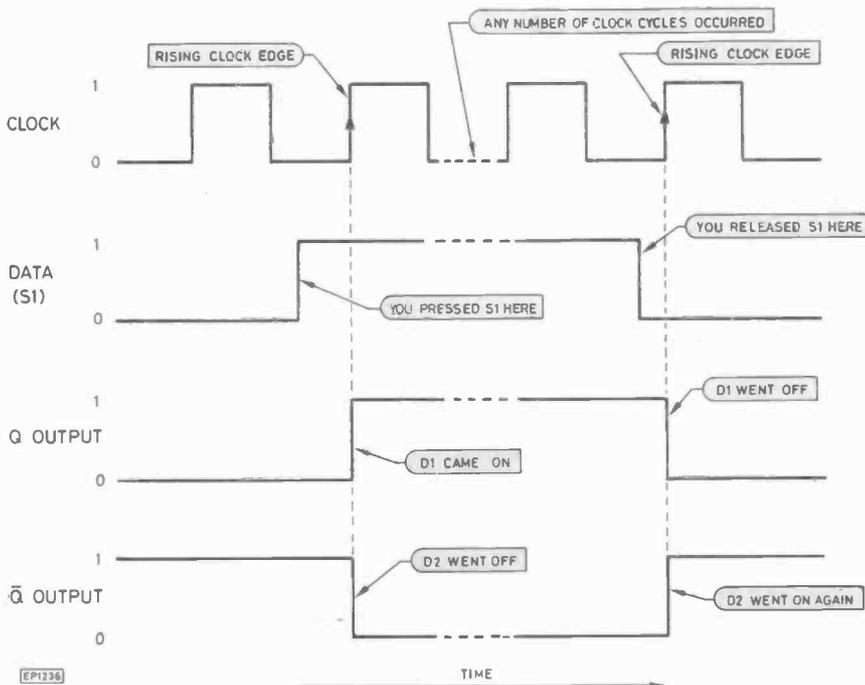
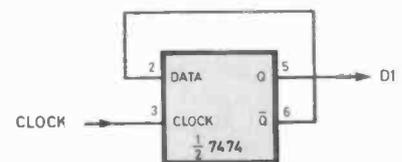


Fig. 5.13. Timing diagram for the 7474 D-type bistable



NOTE: CLEAR and SET (Pins 1 and 4 respectively) are both taken to logic 1

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Fig. 5.14. 7474 as a binary divider

following links are required with the 7474 again placed in socket A of the Logic Tutor:

- A1 to logic 1 (CLEAR input)
- A2 to A6 (DATA from \bar{Q})
- A3 to CLOCK (CLOCK input)
- A4 to logic 1 (SET input)
- A5 to D1 (D1 indicates the Q output)

A7 to 0V (0V)
A16 to +5V (positive supply)

D1 should flash at exactly half the rate at which the clock flashes and the timing diagram should look like that shown in Fig. 5.15.

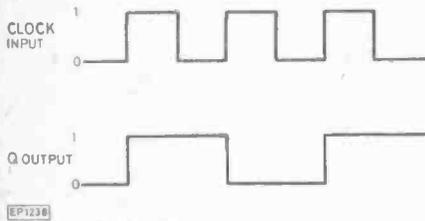


Fig. 5.15. Timing diagram for the binary divider

To conclude the exercise, readers may like to develop the foregoing circuit into a divide-by-four arrangement. The unused half of the 7474 can be brought into service and D2 used to indicate the new output.

BINARY NUMBERS

To conclude Part Five, we shall take a brief look at the binary number system. Digital logic circuits, however, operate with two states only, 0 and 1. Thus the arithmetic appropriate to logic circuits must have a base of two, and is known as the binary system.

Binary numbers consist of a combination of the digits, 0 and 1. The position of a particular digit within a number is an indication of its "weight" or magnitude of the power of two which it represents. The digits are arranged in descending order. Taking the binary number 1010, for example. This consists of four binary digits, or "bits" and can thus be referred to as a "four-bit number". The left-most bit carries the highest weight and is known as the "most significant bit" (MSB). The right-most bit carries the least weight and is known as the "least significant bit" (LSB). Thus, the number 1010 has an MSB of 1 and an LSB of 0.

At this point you are probably wondering what the decimal equivalent of 1010 is. Remember that we said that the position of each digit indicates its weight. The weighting of the LSB is $2^0 (=1)$, the next two bits have weightings of $2^1 (=2)$ and $2^2 (=4)$ respectively, and the MSB has a weighting of $2^3 (=8)$. We could, therefore, re-write the number in columns in a similar fashion to the "hundreds, tens, and units" of our primary school days. Let's compare two numbers: denary (i.e. decimal) 174 and binary 1010. Writing these using columns to indicate the weighting of each digit gives:

Denary 174		
$10^2 (= 100)$	$10^1 (= 10)$	$10^0 (= 1)$
(hundreds)	(tens)	(units)
1	7	4

Binary 1010			
$2^3 (= 8)$	$2^2 (= 4)$	$2^1 (= 2)$	$2^0 (= 1)$
1	0	1	0

The denary number 174 is the result of adding the individual weighted values, i.e. $(1 \times 100) + (7 \times 10) + (4 \times 1)$ or $(100 + 70 + 4)$. The binary number 1010 is, therefore, the result of adding its individual weighted values, i.e. $(1 \times 8) + (0 \times 4) + (1 \times 2) + (0 \times 1)$ or $(8 + 2)$ which is 10 on the denary scale. To reinforce the point, let's take another example. The eight bit binary number 01001011 is equivalent to $(0 \times 128) + (1 \times 64) + (0 \times 32) + (0 \times 16) + (1 \times 8) + (0 \times 4) + (1 \times 2) + (1 \times 1) = (64 + 8 + 2 + 1) = 75$.

So much for converting from binary to denary. Now let's consider the reverse process, i.e. converting from denary to binary. There are two commonly used methods, one involves finding the set of binary weighted values whose sum is equal to the denary number, and the other involves successive division of the number by two and noting down the remainders. We shall consider each of these methods in turn.

Starting with the decimal number we must first examine it to find the highest power of two contained in it. We then subtract that number, and examine the remainder, repeating the process until we are left with a 1 or a 0. In effect, we are determining a set of binary weighted values which, when added together, are the same as the number which we started with. This may all sound rather complex so, to show how easy it all is, let's take decimal 13 as an example:

$$13 = (8 + 4 + 1) = (2^3 + 2^2 + 2^0)$$

Now place a 1 in the appropriate weight positions and 0 in the remaining position, as shown below:

$2^3 (=8)$	$2^2 (=4)$	$2^1 (=2)$	$2^0 (=1)$
1	1	0	1

Thus decimal 13 is equivalent to binary 1101. Unfortunately, this method becomes somewhat cumbersome when we are dealing with very large numbers (say, greater than 64 or 2^6) and the alternative method may then be preferred. This method involves repeated division by 2, leaving whole numbers only, and noting down all the remainders produced. The values of the remainders (which will be either 0 or 1) are assembled, in reverse order, to give the binary number.

Again, taking decimal 13 as an example:

Step 1 $13/2 = 6$ remainder 1 (LSB)

Step 2 $6/2 = 3$ remainder 0

Step 3 $3/2 = 1$ remainder 1

Step 4 $1/2 = 0$ remainder 1 (MSB)

Assembling the remainders in reverse order gives 1101. Just to reinforce this method let's take one further example, decimal 60:

Step 1 $60/2 = 30$ remainder 0 (LSB)

Step 2 $30/2 = 15$ remainder 0

Step 3 $15/2 = 7$ remainder 1

Step 4 $7/2 = 3$ remainder 1

Step 5 $3/2 = 1$ remainder 1

Step 6 $1/2 = 0$ remainder 1 (MSB)

Thus decimal 60 is the same as binary 111100.

HEXADECIMAL NUMBERS

Many digital systems process groups of signals being used to represent numbers of one sort or another. Binary numbers are passed around as groups of digital signals, but continually referring to long numbers by strings of 0's and 1's becomes tedious to say the least! The hexadecimal (base 16) number system is a shorthand way of representing such numbers. The binary 0/1 string is split up into groups of 4 bits, starting with the least significant end. Each 'nibble' (as it is called) is then converted into a single hex digit according to Table 5.4. Thus 1010

DECIMAL	BINARY	HEXADECIMAL
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

Table 5.4. Hexadecimal numbers

0011 1111 is represented by A3F, while EF35 is shorthand for 1110 1111 0011 0101. The result is an economical representation which is easily remembered, and which is widely used.

NEXT MONTH: 3 and 4 input gates and JK flip-flops.

MICRO-BUS

and MICROPROMPT

Appearing every month, Micro-Bus now presents ideas, applications and programs for the most popular micro-computers and all micro-related projects so far published in PE. Ideas must be original, and payment will be made for any contribution featured.

THIS month's Micro-Bus features a 6809 Call Utility, submitted by R. G. Strange of Loughborough.

6809 CALL UTILITY

The 6809 processor offers two forms of subroutine call. JSR jumps to a direct address, resulting in programs which are easy to code and read, but which are position dependent. BSR produces position independent code, but requires relative jump calculations, and results in code which is difficult to read.

Often programs do not need to be relocated by an arbitrary number of bytes, but are simply shifted by a whole number of K, for example, when transferring a RAM based program to EPROM.

The CALL routine listed in Fig. 1 utilises the 6809 software—interrupt SWI (op code 3F) to create an alternative instruction which

```

F800 AE 6A CALL LDX 10,S
F802 A6 6A LDA 10,S
F804 84 F8 ANDA # $F8
F806 5F CLR B

F807 E3 81 ADDDX++

F809 ED 68 STD 8,S

F80B AF 6A STX 10,S
F80D 35 BF PULs CC, A, B,
           DP, X, Y, PC
    
```

branches relative to the next lowest 2K boundary (since the writer's programs are currently based in 2K EPROMs). This results in a relocatable program in which each subroutine has a unique and meaningful jump vector. For example, in the 2K block \$9800-\$9FFF, a routine at \$9950 has jump vector \$0150 and is CALLED by the instruction

```
3F 01 50
```

The routine can reside anywhere in memory, and the SWI vector at \$FFFA, \$FFFB must point to it.

There is an inherent time penalty of 70 cycles, but in programs where execution time is not critical the CALL routine can speed program development considerably.

SWI automatically stacks all registers, and the operation of the routine can be understood with the help of Fig. 2, the 6809 stacking order.

X = Stacked PC (Jump Vector address)

A = Stacked PC high byte

Round down to 2K

D contains the 2K boundary

(D is the concatenation of A & B)

Add jump vector to boundary

X = New Return address

Put subroutine address on stack

in place of the User Stack Pointer

Update the stacked PC

Restore original values of all

registers, jump to subroutine

Return vector is left on the

stack for termination of subroutine

by RTS.

Fig. 1. CALL routine

9A00 3F 01 50	CALL \$9950		
Stack after interrupt	Stack before PULs	Stack after PULs	
High memory			
PCL = 01	PCL = 03	PCL = 03	
10,S PCH = 9A	10,S PCH = 9A	0,S PCH = 9A	
UL	PCL = 50		
8,S UH	8,S PCH = 99		
YL	YL		
YH	YH		
XL	XL		
XH	XH		
DP	DP		
B	B		
A	A		
0,S CC	0,S CC		

Fig. 2. 6809 stack during execution of CALL \$9950

USING USR WITH THE PSG

Sir—Currently to set up a register and its contents on the PSG, it is necessary to use two POKEs, i.e. POKE R, REG : POKE C, CON, where R and C are the register and content addresses on the PSG and REG and CON is the register number and its value. This method is rather long winded and cumbersome especially where large numbers of registers need to be set up. However, with the machine code routine shown below, and having first set the USR address to \$0222 (POKE 11, 34:POKE 12,2), $X = USR(REG*256+CON)$ gives register number REG the value of CON. Furthermore, to set up a number of registers use:— $X = USR(R1*256+C1) = USR(R2*256 + C2) = USR(R3*256+C3) = \dots$

The values inside the brackets can, of course, be calculated before-hand, for instance $X = USR(255) = USR(1039) = USR(1022)$ outputs a single tone, and is far shorter and more convenient than its equivalent POKEs.

```

; PSG routine
; ORG $0222 relocatable
0222 20 01 AE JSR $AE01
0225 A5 AE LDA $AE
0227 8D 70 F1 STA $F170
022A A5 AF LDA $AF
022C 8D 71 F1 STA $F171
022F 60 RTS
    
```

A. D. Love,
Swansea

ALTERNATIVE KEYBOARD

Sir—The key action on my UK 101 is not perfect having unequal weight and occasional "stuttering" and having now come into possession of a nice professional keyboard which provides ASCII output and which is not easily rewired for matrix operation, I am seeking advice or hints on how to adopt it for the 101. A WEMON monitor is fitted and to my very inexperienced eye, this seems to do some "sorting out" before turning the character into ASCII. Can anyone help?

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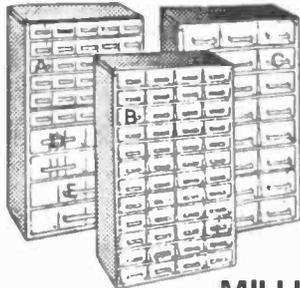
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INDEX TO ADVERTISERS

A.D. Electronics	68
Audio Electronics	8
Bensham Recordings	42
Bimsales	69
Bi-Pak	7
British National Radio & Electronics School ..	12
Clef Products	69
Cricklewood	Cover 3
C.R. Supply Co	70
Display Distribution	42
M. Dziubas	69
Electronic Mailorder	70
Electronics Brokers	4
Electrovalue	68
Flight Electronics	41
G.C.H.Q.	71
G.S.C.	57
Greenweld	6
ICS Intertext	6
ILP Electronics	10 & 11
Maplin	11 & Cover 4
Marshalls	42
Midwich	8
Millhill	69
Modern Book Co	71
Parndon	68
Phonosonics	58
P.K.G. Electronics	71
Powertran	Cover 2
Proto Design	71
Radio Component Specialists	68
R.T.V.C.	4
Scientific Wire Co	71
Service Trading	58
Simpsons Electronic Alarms	70
Sparkrite	9
Swanley	72
Tandy	23
T.K. Electronics	5
Tomorrows World	58
Watford Electronics	2 & 3
Williamson Amplification	71

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ORIC AND SINCLAIR COMPUTERS



Oric 1 computer 48K £143 (£141) £151. Oric Colour Printer £134 (£123) £140. Sinclair Spectrum 48K £131 (£131) £143. Spectrum 16K £101 (£105) £117. 32K memory upgrade kit for 16K Spectrum (Issue 2 only) £31 (£28) £30. Fuller Master Unit for the spectrum including speech unit, sound synthesizer, amplifier and joystick port £56 (£56) £62. Fuller full sized FDS keyboard for the spectrum with proper space bar £52 (£52) £62. ZX printer with 5 free rolls paper £41. ZX printer alone £36 (£38) £50. 5 printer rolls £13 (£16) £21. ZX81 £37 (£37) £47. Special offer pack ZX81 computer + 16K ram pack + game tape £49 (£55) £65. ZX81 16K ram packs £31 (£28) £30.

COMMODORE COMPUTERS

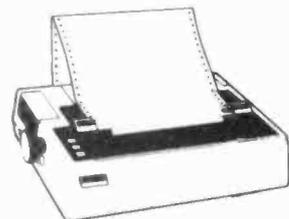
Commodore 64 £204 (£184) £204. Vic 20 £104 (£97) £117. Converter to allow most ordinary mono cassette recorders to be used with the Vic 20 and Commodore 64: built £9.78 (£9) £11, kit £7.47 (£7) £9. Commodore cassette recorder £43 (£44) £50. 1541 Disc drive £233 (£209) £234. 1525 Printer £235 (£220) £245. 1526 Printer £350 (£330) £360.

ACORN COMPUTERS

Electron £203 (£209) £229. BBC Model B £424 (£388) £408. Kenda double density disk interface system for beeb £139

(£125) £135. We stock the whole range of Cumana disc drives for the beeb e.g. 100K single £230 (£220) £240, Double 2 x 400K £625 (£560) £580.

PRINTERS



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 Case included in both prices

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Full construction details in Projects Book 9.

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