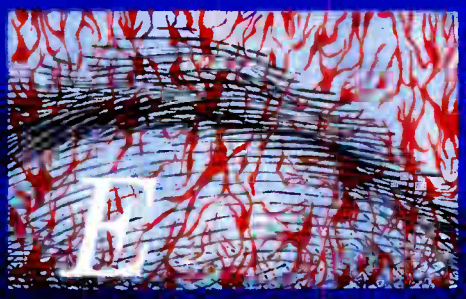
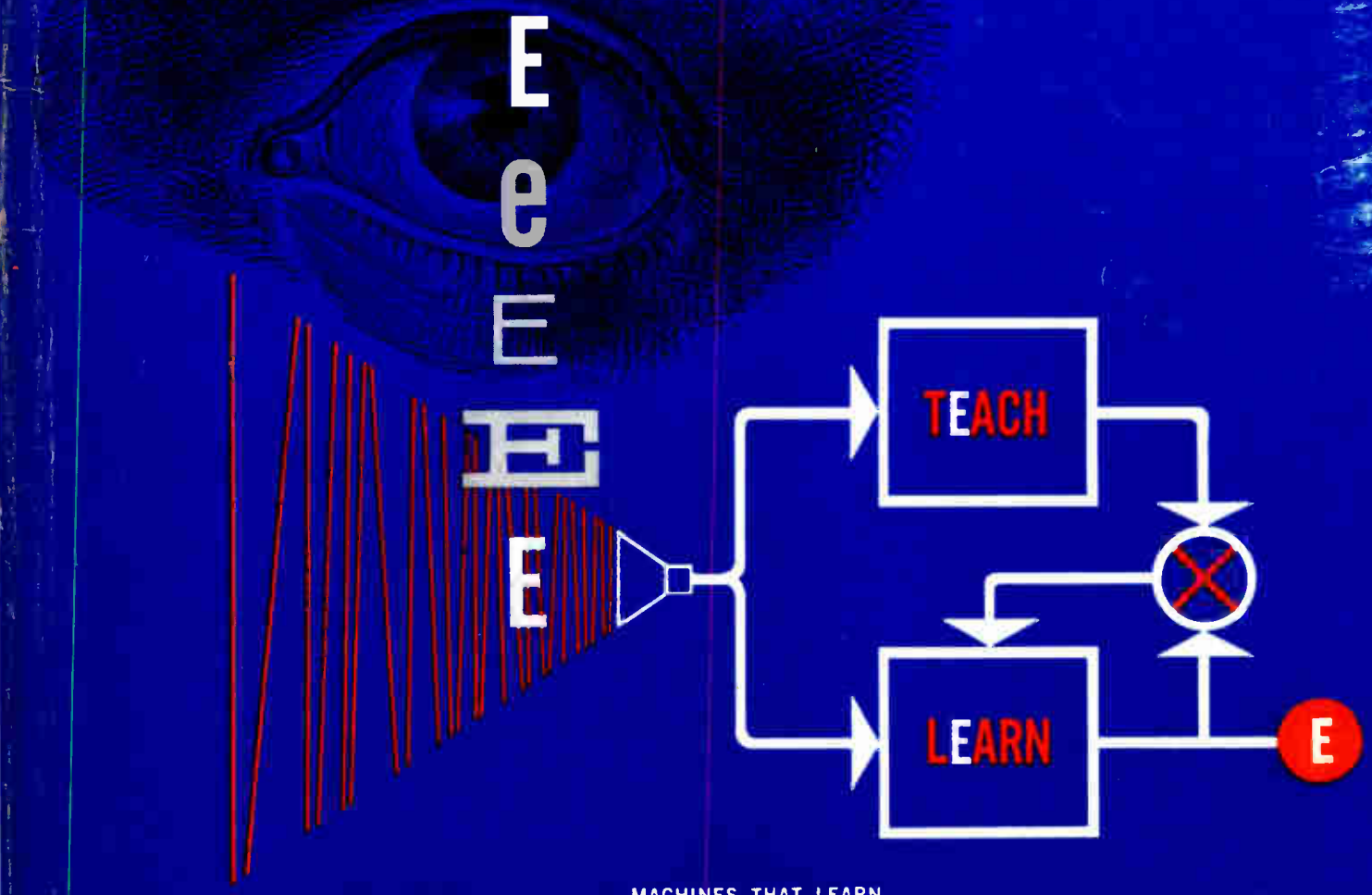
january 1961
the
institute
of
radio
engineers

Proceedings of the IRE

SPECIAL ISSUE ON COMPUTERS





MACHINES THAT LEARN

NEW* Revolutionary† DO-T and DI-T TRANSISTOR TRANSFORMERS

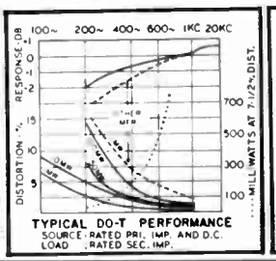
FROM STOCK—Hermetically Sealed to MIL-T-27A Specs.

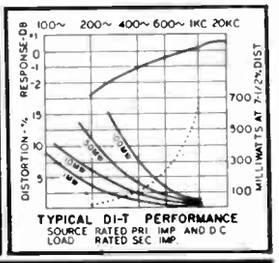
There is no transformer even twice the size of the DO-T and DI-T series which has as much as 1/10th the power handling ability . . . which can equal the efficiency . . . or equal the response range. And none to approach the reliability of the DO-T and DI-T units (proved to, but exceeding MIL-T-27A grade 4).

High Power Rating	up to 10 times greater.
Excellent Response	twice as good at low end.
Low Distortion	reduced 80%.
High Efficiency	up to 30% better . . . compare DCR
Moisture Proof	hermetically sealed to MIL-T-27A.
Rugged	completely metal cased.
Anchored Leads	will withstand 10 pound pull test.
Printed Circuit Use	(solder melting) plastic insulated leads.
Suited to Clip Mounting	use Augat #6009-8A clip.

TRANSFORMERS PICTURED ACTUAL SIZE
DO-T: 5/16 Dia. x 13/32", 1/10 Oz.; DI-T: 3/16 Dia. x 1/4", 1/20 Oz.

Typical Printed Circuit Positioning





DO-T No.	Pri. Imp.	D.C. Ma.‡ in Pri.	Sec. Imp.	Pri. Res. DO-T	Pri. Res. DI-T	Mw. Level	DI-T No.
DO-T1	20,000 30,000	.5 .5	800 1200	850	815	50	DI-T1
DO-T2	500 600	3 3	50 60	60	65	100	DI-T2
DO-T3	1000 1200	3 3	50 60	115	110	100	DI-T3
DO-T4	600	3	3.2	60		100	
DO-T5	1200	2	3.2	115	110	100	DI-T5
DO-T6	10,000	1	3.2	790		100	
DO-T7	200,000 500	0 0	1000 100,000	8500 —		25	
	Reactor 2.5 Hys./2 Ma., .9 Hy./4 Ma				630		DI-T8
DO-T8	" 3.5 Hys./2 Ma., 1 Hy./5 Ma.			630			
DO-T9	10,000 12,000	1 1	500 CT 600 CT	800	870	100	DI-T9
DO-T10	10,000 12,500	1 1	1200 CT 1500 CT	800	870	100	DI-T10
DO-T11	10,000 12,500	1 1	2000 CT 2500 CT	800	870	100	DI-T11
DO-T12	150 CT 200 CT	10 10	12 16	11		500	
DO-T13	300 CT 400 CT	7 7	12 16	20		500	
DO-T14	600 CT 800 CT	5 5	12 16	43		500	
DO-T15	800 CT 1070 CT	4 4	12 16	51		500	
DO-T16	1000 CT 1330 CT	3.5 3.5	12 16	71		500	
DO-T17	1500 CT 2000 CT	3 3	12 16	108		500	
DO-T18	7500 CT 10,000 CT	1 1	12 16	505		500	
DO-T19	300 CT	7	600	19	20	500	DI-T19
DO-T20	500 CT	5.5	600	31	32	500	DI-T20
DO-T21	900 CT	4	600	53	53	500	DI-T21
DO-T22	1500 CT 600	3 5	600 1500 CT	86 —	87	500	DI-T22
DO-T23	20,000 CT 30,000 CT	.5 .5	800 CT 1200 CT	850	815	100	DI-T23
DO-T24	200,000 CT 500 CT	0 0	1000 CT 100,000 CT	8500 —		25	
DO-T25	10,000 CT 12,000 CT	1 1	1500 CT 1800 CT	800	870	100	DI-T25

DO-T No.	Pri. Imp.	D.C. Ma.‡ in Pri.	Sec. Imp.	Pri. Res. DO-T	Pri. Res. DI-T	Mw. Level	DI-T No.
	Reactor 4.5 Hys./2 Ma., 1.2 Hys./4 Ma.				2300		DI-T26
DO-T26	" 6 Hys./2 Ma., 1.5 Hys./5 Ma.			2100			
	Reactor .9 Hy./2 Ma., .5 Hy./6 Ma.				105		DI-T27
DO-T27	" 1.25 Hys./2 Ma., .5 Hy./11 Ma.			100			
	Reactor .1 Hy./4 Ma., .08 Hy./10 Ma.				25		DI-T28
DO-T28	" .3 Hy./4 Ma., .15 Hys./20 Ma.			25			
DO-T29	120 CT 150 CT	10 10	3.2 4	10		500	
DO-T30	320 CT 400 CT	7 7	3.2 4	20		500	
DO-T31	640 CT 800 CT	5 5	3.2 4	43		500	
DO-T32	800 CT 1000 CT	4 4	3.2 4	51		500	
DO-T33	1060 CT 1330 CT	3.5 3.5	3.2 4	71		500	
DO-T34	1600 CT 2000 CT	3 3	3.2 4	109		500	
DO-T35	8000 CT 10,000 CT	1 1	3.2 4	505		100	
DO-T36	10,000 CT 12,000 CT	1 1	10,000 CT 12,000 CT	950	970	100	DI-T36
*DO-T37	2000 CT 2500 CT	3 3	8000 Split 10,000 Split	195		100	
*DO-T38	10,000 CT 12,000 CT	1 1	2000 Split 2400 Split	560		100	
*DO-T39	20,000 CT 30,000 CT	.5 .5	1000 Split 1500 Split	800		100	
*DO-T40	40,000 CT 50,000 CT	.25 .25	400 Split 500 Split	1700		50	
*DO-T41	400 CT 500 CT	8 6	400 Split 500 Split	46		500	
*DO-T42	400 CT 500 CT	8 6	120 Split 150 Split	46		500	
*DOT-43	400 CT 500 CT	8 6	40 Split 50 Split	46		500	
*DO-T44	80 CT 100 CT	12 10	32 Split 40 Split	9.8		500	
DO-TSH	Drawn Hipermalloy shield and cover 20/30 db						DI-TSH

‡ DCMA shown is for single ended useage (under 5% distortion—100MW—1KC) . . . for push pull, DCMA can be any balanced value taken by .5W transistors (under 5% distortion—500MW—1KC)

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Proceedings of the IRE®

contents

COVER

The cover suggests the major facets of current research in "self-organizing" machines, a subset of the research applied to developing some form of "artificial intelligence." The block diagram suggests a machine that is learning the alphabet. The letter E is presented to both the teacher fixed network (TEACH) and the pupil variable network (LEARN). The teacher's output E is compared with the pupil's output by a comparison network (X), and lack of equality excites trials of other possible pupil outputs until equality is attained. Success strengthens "synaptic" connections in the learning network. The illustration of a neural net suggests the type of network researchers are using as a partial guide. The eye represents the type of sensor most often provided the machine in current research.

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Proceedings of the IRE®

continued

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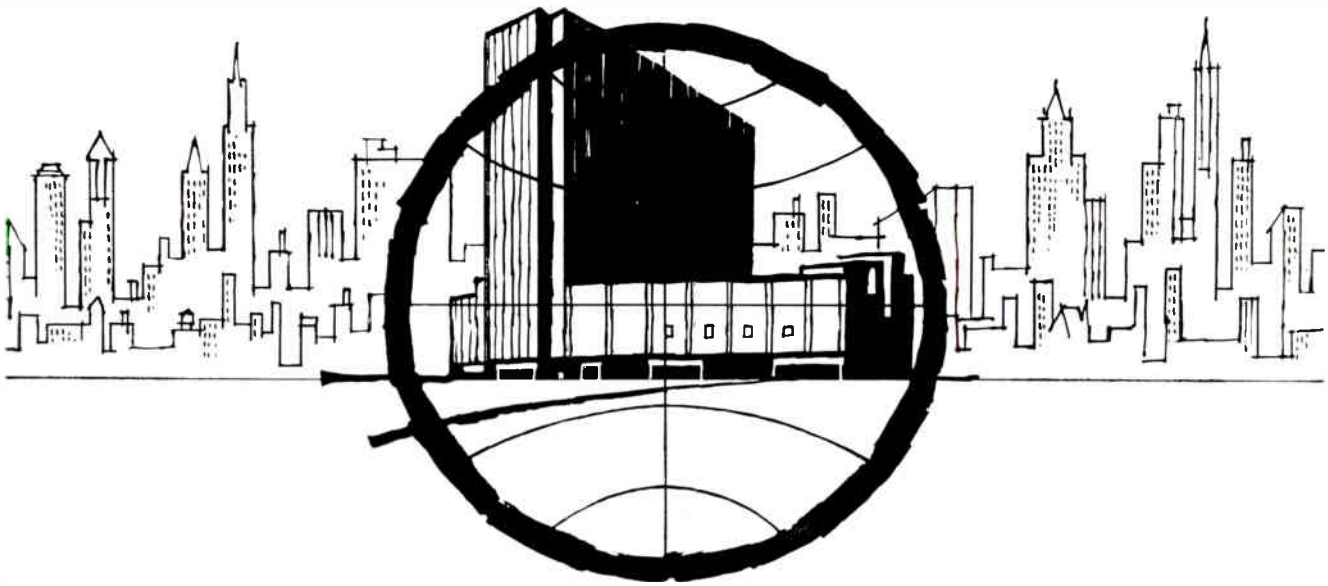
JANUARY

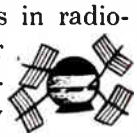
NEW YORK • WORLD CENTER FOR RADIO-ELECTRONICS • 1961



INTERNATIONAL CONVENTION AND IRE SHOW

MARCH 20-23

Visitors from all over the world will converge on the Coliseum, March 20-23, for IRE's big Show and International Convention. Join the more than 65,000 radio-electronics engineers who will attend! On the Coliseum's **4** gigantic floors you'll see the latest production items, systems, instruments and components in radio-electronics; in radar; in complex air traffic control; in space communications — in any and every field of radio-engineering you care to name. At the convention, you'll trade ideas with brilliant delegates from the world of radio-electronics, and choose from amongst scores of papers to be read by experts in their field. Like the IRE show, the convention is both a summing-up and a look into the future!



Registration: IRE members $1.00—non-members $3.00
No one under 18 years of age will be admitted.

Remember the occasion, the time, the place:

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MARCH 20-23 1961

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REMEMBERS THE MAN

IRE

On a recent development program for the Hallicrafters Company, Dick Domchick and Bob Sleven of our Department of Applied Electronics faced the old problem of chanellizing a wide-frequency band with minimum adjacent channel interaction. In spite of extreme skirt selectivity requirements, a reasonably compact and inexpensive solution was found.

Waveguide Channelizing Filters

We have recently developed an X-band channel separation filter array. The performance and the approach used proved to have many interesting aspects. The array consists of 40 waveguide bandpass filters and associated crystal detectors in the 8.5 to 11 Kmc range. The nominal 3 db bandwidth of each bandpass filter is 63 Mc with cross-overs that are 3 db or better. Performance (cross-over characteristics and filter insertion loss) obtained was superior to that previously realized with TEM structures such as coaxial or strip transmission lines. This is due to the inherently higher resonator Q's and the ability to hold closer tolerances. Although 8-section maximally flat filters were used, the design and fabrication techniques are applicable to a wide range of multi-channel systems requiring different numbers of channels and different filter responses. Waveguide branching filters can be made lightweight and can, with careful design, be of reasonable size. This article will describe design, fabrication and performance of the X-band filter assembly and will then indicate the procedure by which other frequency channelization requirements can be realized.

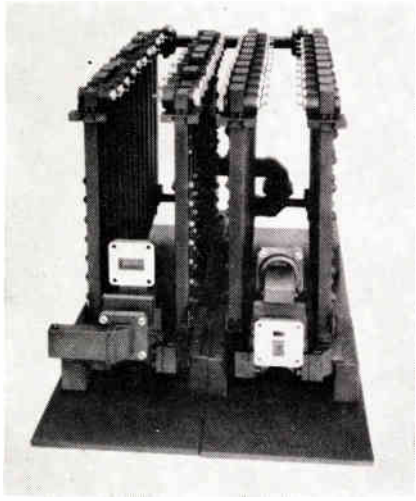

Figure 1.

A photograph of the complete 40 channel filter assembly is shown in Fig. 1. Each filter consists of eight direct coupled waveguide resonators. The length of the resonator is approximately one-half guide wavelength (about 1") at the filter center frequency. Coupling between resonators is obtained by means of circular irises except that the input and output couplings require inductive slits. The couplings are chosen to give a maximally flat amplitude-frequency response. The couplings in most cases are calculated from formulas in reference 1. Slight corrections were made from design data available at AIL. The input coupling is specially tailored in order to give a good feedline characteristic. To obtain a good feedline characteristic, it was necessary to isolate adjacent frequency filters from each other. Since it was possible to accept an additional 3 db insertion loss, advantage was taken of this fact by utilizing a waveguide hybrid. Feedlines were attached to the coupled arm of the hybrid and isolation was obtained by alternating adjacent frequency filters on the two lines. This arrangement makes it possible for filter n not to see the cross-over impedance of filters $n \pm 1$ reflected into it. It was therefore possible to obtain at the cross-overs a characteristic which was essentially independent of adjacent filters. All filters were coupled off the H-plane of the waveguide feedline. The response of the feedline was checked by measuring the SWR of each filter at the frequency of the next one on the particular feedline. This was found to be reasonably low; approximately 1.5 to 1 or better. A plot was made of all filter channels. Except for some ripple, which in all cases was well under 3 db, we find that the cross-overs were also 3 db or better. The hybrid therefore serves the purpose of giving true passband characteristics for each filter and simplifies both the feedline design and the tuning of the filters. The results obtained in this filter assembly indicate that it is capable of extension to a greater number of channels. In particular, if the channel separations were narrower it would also be possible by using looser input coupling to each filter to have an even smoother feedline characteristic. The design of this filter assembly is, in most instances, based on calculated couplings and involves a minimum amount of experimental work.

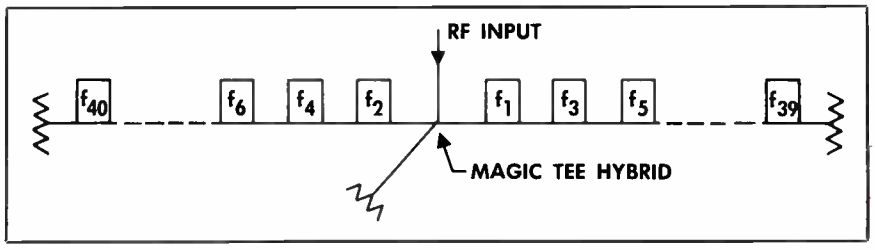

Figure 2. Channelizing Filters Using a Hybrid Junction

Tuning of each filter was provided by means of screws placed on the E-plane of each waveguide resonator. The filters were tuned using the Dishal procedure (reference 2). The filters were connected to waveguide feedlines which had H-plane openings and mounting holes placed at each filter position. We have found that with the hybrid feedline technique the spacing of one filter relative to the next is not critical. It is therefore possible to tailor a filter array to suit a variety of packaging considerations. In addition to achieving good feedline characteristics, the insertion loss of each filter was low. Loss due to each filter was approximately 2 db. The loss of the overall channel was, however, in the vicinity of 8 db. The additional 6 db is due to power splits in the hybrid and the feedline termination. This loss has not been a disadvantage in this application.

Waveguide filter assemblies offer a means of obtaining excellent cross-over characteristics; low insertion loss, and reliable, accurate, inexpensive fabrication. In X-band, and above, size is usually no problem. In waveguide sizes below X-band it would be necessary, if size were important, to use non-standard waveguide for the filters. Significant volume savings can be made using, for example, half or quarter height waveguide. This would make waveguide filter assemblies competitive in size to TEM structures for frequencies above 4 Kmc. In S-band, the assemblies are useful if space is not the major consideration. The techniques described are perfectly general, involve a minimum of experimentation and sufficiently suited for other frequency channelization requirements. Minimum development and production time allow for quick delivery. It is felt that many systems now in operation can be significantly improved in both performance and reliability by switching over to filters of this type.

REFERENCES

1. N. Marcuvitz, "Waveguide Handbook," MIT Radiation Lab Series, Vol. 10, McGraw-Hill, 1950.
2. M. Dishal, "Alignment and Adjustment of Synchronously Tuned Multiple-Resonant-Circuit Filters," Milton Dishal, Proc. IRE, Nov. 1951, p. 1448 to 1455.

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μF	Diameter in Inches	μF	Diameter in Inches
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.22	.275	.1	.400
.47	.400	.22	.595
1.0	.595	.47	.840
2.2	.840		

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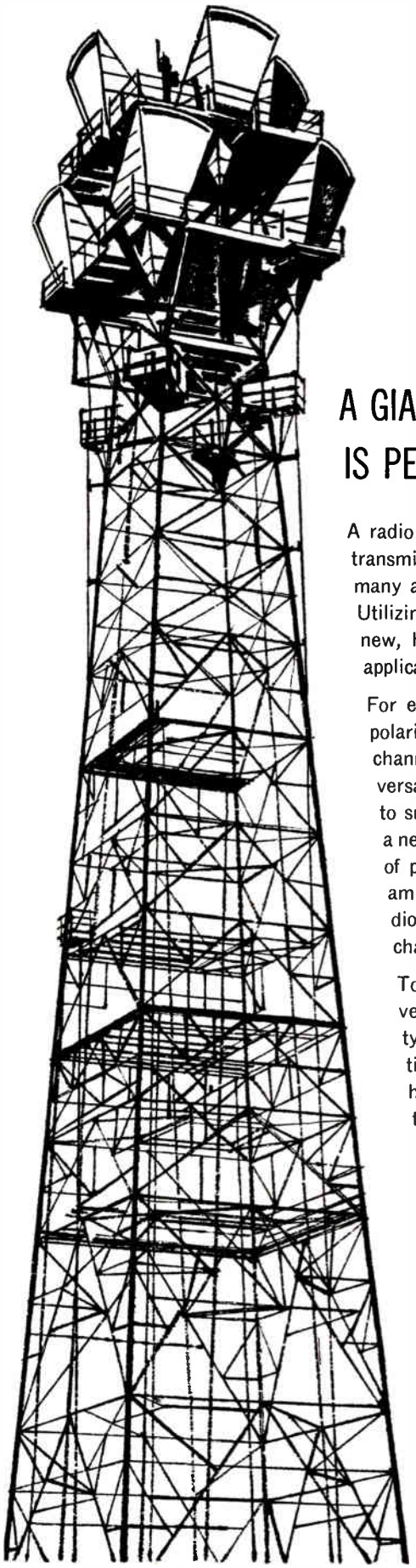

A GIANT RADIO HIGHWAY IS PERFECTED FOR TELEPHONY

A radio relay system operating at 6 billion cycles per second and able to transmit 11,000 voices on a single beam of microwaves—several times as many as any previous system—has been developed at Bell Laboratories. Utilizing the assigned frequency band with unprecedented efficiency, this new, heavy-traffic system was made possible by the development and application of new technology by Bell Laboratories engineers and scientists.

For example, they arranged for the waves in adjacent channels to be polarized 90 degrees apart, thus cutting down interference between channels and permitting the transmission of many more telephone conversations in the same frequency space. They developed ferrite isolators to suppress interfering wave reflections in the waveguide circuits; and a new traveling wave tube that has ten times the power handling capacity of previous amplifiers and provides uniform and almost distortionless amplification of FM signals. They devised and applied a new high-speed diode switching system which instantly switches service to a protection channel when trouble threatens.

To transmit and receive the waves, the engineers applied their invention, the horn-reflector antenna. Elsewhere, this versatile antenna type is brilliantly aiding space communication research in the reception of radio signals from satellites. For radio relay, a single horn-reflector antenna can efficiently handle both polarizations of the 6000 megacycle waves of the new system; at the same time it can handle 4000 and 11,000 megacycle waves used for existing radio relay systems. Thus it enables all three systems to share economically the same radio towers and routes.

Produced by the Bell System's manufacturing unit, Western Electric, the new system is now in operation between Denver and Salt Lake City, and will gradually be extended from coast to coast. This new advance in radio technology is another example of how Bell Telephone Laboratories works to improve your Bell communication services.

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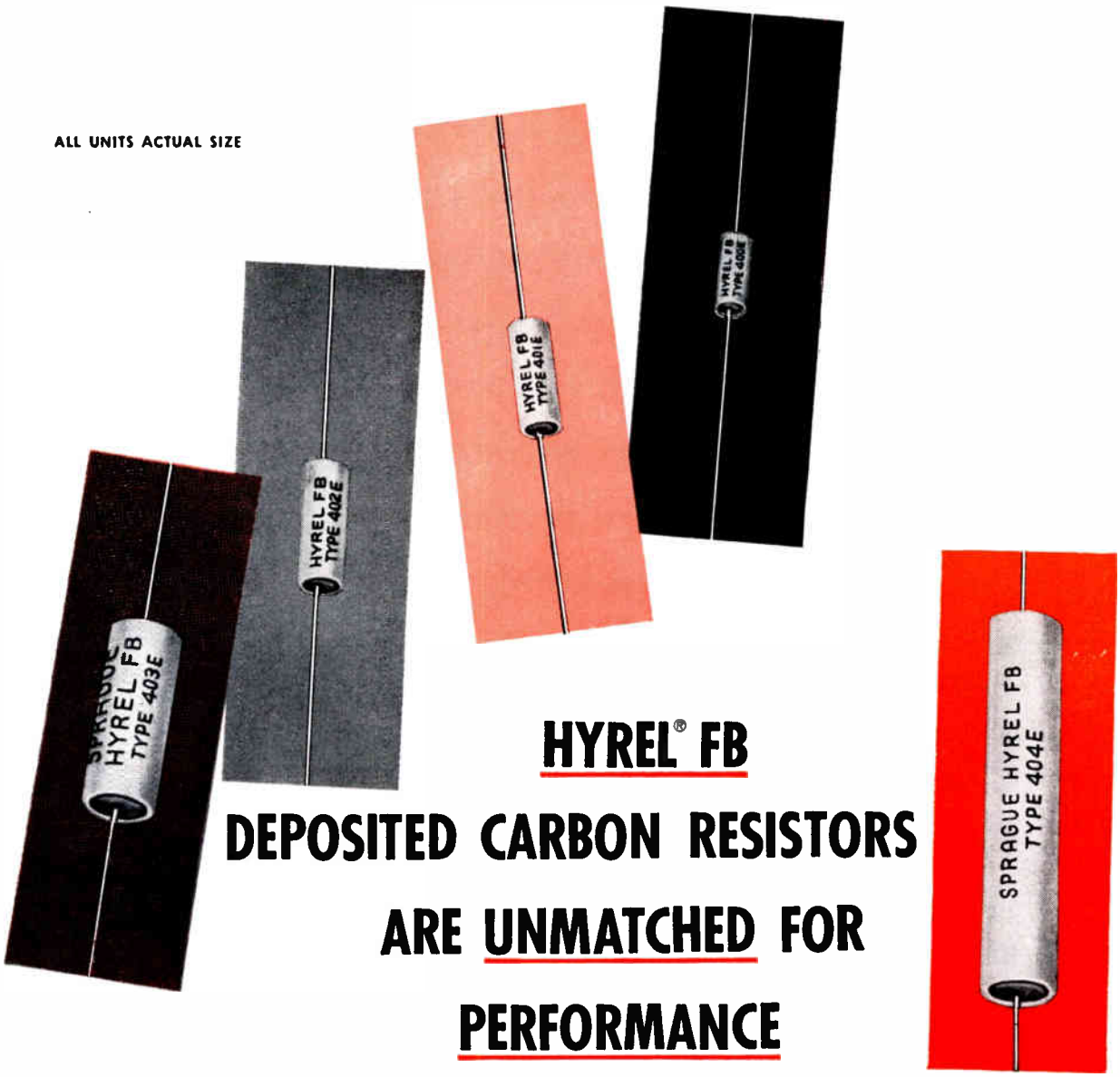
ALL UNITS ACTUAL SIZE



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Meetings with Exhibits

● As a service both to Members and the industry, we will endeavor to record in this column each month those meetings of IRE, its sections and professional groups which include exhibits.

Δ

February 1-3, 1961

Second Winter Convention on Military Electronics, Biltmore Hotel, Los Angeles, Calif.

Exhibits: Mr. John Francis O'Halloran, O'Halloran & Associates, 11636 Ventura Blvd., North Hollywood, Calif.

March 20-23, 1961

International Radio and Electronics Show and IRE International Convention, Waldorf-Astoria Hotel and New York Coliseum, New York, N.Y.

Exhibits: Mr. William C. Copp, Institute of Radio Engineers, 72 West 45th Street, New York 36, N.Y.

April 19-21, 1961

SWIRECO, South West IRE Regional Conference & Electronics Show, Dallas, Tex.

Exhibits: Mr. R. W. Olson, Texas Instruments, Inc., 6000 Lemmon Ave., Dallas 9, Tex.

April 26-28, 1961

Seventh Region Technical Conference and Trade Show, Westward Ho Hotel, Phoenix, Ariz.

Exhibits: Mr. G. J. Royden, 912 W. Linger Lane, Phoenix, Ariz.

May 8-10, 1961

National Aerospace Electronics Conference (NAECON), Miami & Biltmore Hotels, Dayton, Ohio

Exhibits: Mr. Edwin P. Turner, Wright Patterson Air Force Base, Dayton, Ohio

May 9-11, 1961

Western Joint Computer Conference, Ambassador Hotel, Los Angeles, Calif.

Exhibits: John H. Whitlock Associates, 253 Waples Mills Road, Oakton, Va.

May 22-24, 1961

Fifth National Symposium on Global Communications (GLOBECOM V), Sherman Hotel, Chicago, Ill.

Exhibits: Mr. Robert Hajek, Commtronix Engineering, Box 62, Riverside, Ill.

May 22-24, 1961

National Telemetering Conference, Sheraton Towers Hotel, Chicago, Ill.

Exhibits: Mr. Frank Finch, 795 Gladys Ave., Long Beach 4, Calif.

June 6-8, 1961

Armed Forces Communications & Electronics Show, Sheraton Park and Shoreham Hotels, Washington, D.C.

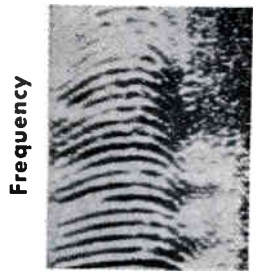
Exhibits: Mr. William C. Copp, 72 W. 45th St., New York 36, N.Y.

(Continued on page 11A)

KAY AUDIO SPECTRUM ANALYZERS

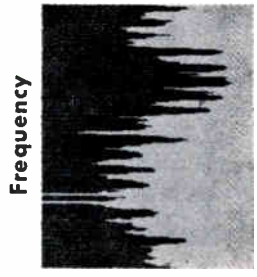
PERMANENT RECORDS

DISPLAY NO. 1



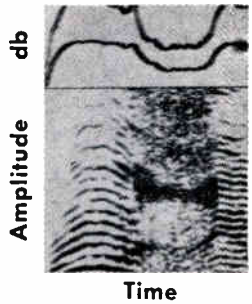
Frequency & Amplitude vs Time. —4" × 12" record on facsimile paper.

DISPLAY NO. 2

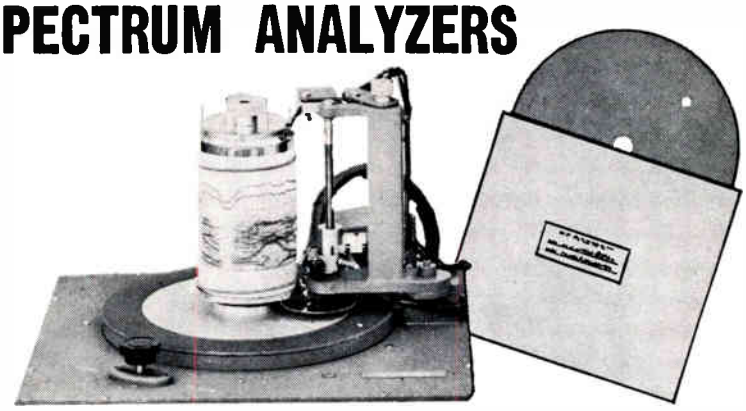


Intensity vs Frequency at Selected Time. Range: 35 db.

DISPLAY NO. 3



Average Amplitude vs Time. Logarithmic scale. 24 and 34 db ranges.



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- **85–12,000 cps**
- **Easily stored, permanent or re-usable magnetic disc recording**

The *Sona-Graph Model Recorder* is a new audio spectrograph for sound and vibration analysis. This instrument provides *four* permanent, storable records of any sample of audio energy in the 85–12,000 cps range . . . the three visual displays made by the *Sona-Graph 661-A* plus an aural record made on a 12" plastic-base magnetic disc which can be stored with the visual records.

SPECIFICATIONS

Frequency Range: 85 cps to 12 kc in two switched bands; 85 cps to 6 kc and 6 kc to 12 kc.

Frequency Response: ± 2 db over entire frequency range. Flat or 15 db high-frequency pre-emphasis in lower range.

Recording Medium: Plastic-base magnetic disc that can be removed and stored, or erased and re-used.

Analyzing Filter Bandwidths: 45 and 300 cps.

Recording Time: Any selected 2.4 second interval of any audio signal within frequency range.

Price: $2950.00 f.o.b. factory. $3245.00 f.a.s., New York.

NEW KAY *Missilyzer*®

5–15,000 cps

Catalog No. 675

- **Two separate channels for simultaneous recording of two signals.**
- **Remote control of recording and reproducing channel selectors.**

The Missilyzer is a wider range spectrum analyzer providing two identical channels for the simultaneous recording of two related signals. Built-in fast acting relays permit rapid automatic remote control.

SPECIFICATIONS

Frequency Range: Standard models, 5–15,000 cps, in bands listed below.

	Analyzing Filter Band		*Duration Recorded*
Freq. Range	*Narrow*	*Wide*	*Sample*
5-500 cps	2 cps	20 cps	24 seconds
15-1500 cps	6 cps	60 cps	8.0 seconds
50-5000 cps	20 cps	200 cps	2.4 seconds
150-15,000 cps	60 cps	600 cps	0.8 seconds

Record-Reproduce Amplifier Characteristics: Frequency response switchable to provide FLAT or (for transducer usage) either 44-db or 60-db falling characteristic.

Frequency Calibration: Calibration markers at 30 cps or 240 cps intervals may be recorded on analysis paper.

Input Impedances, Selectable: High, 1.8 Megohms for low level and microphone input. Low, for high level signals, such as from tape recorders.

Price: $2950.00 f.o.b. factory $3245.00 f.a.s., New York.

KAY *Sona-Graph*® Catalog No. 661-A

An audio spectrograph in the 85–8000 cps range makes three permanent visual records.

SPECIFICATIONS

Frequency Range: 85–8000 cps.
Analyzing Filter Bandwidths: 45 and 300 cps.
Recording Time: Any selected 2.4 sec. interval of any audio signal within frequency range.
Record-Reproduce Amplifier Characteristics: Flat or 15 db high-frequency pre-emphasis for voice studies.
Microphone: Altec-Lansing 633A dynamic.
Input Impedance: 30 ohms.
Price: $2,450.00 f.o.b. factory. $2.695.00 f.a.s., New York.

KAY *Vibralyzer*® Catalog No. 651-A

An audio and sub-audio spectrograph in the 5–4400 cps range makes three permanent visual records.

SPECIFICATIONS

Frequency Range: 5–4400 cps in 3 bands.
Frequency Calibration: Markers at 30 cps or 240 cps intervals may be recorded on analysis paper.
Record-Reproduce Amplifier Characteristics: Frequency response switchable to provide FLAT (or for transducer usage) 44 or 60 db falling characteristic.
Pickup Devices: Vibration pickups: microphones or other properly matched devices may be used.
Input Impedance: High, 1.8 megohms.
Input Signal Sensitivity: Approx. 3 mv rms for full scale operation.
Price: $2495.00 f.o.b. factory. $2745.00 f.a.s., New York.

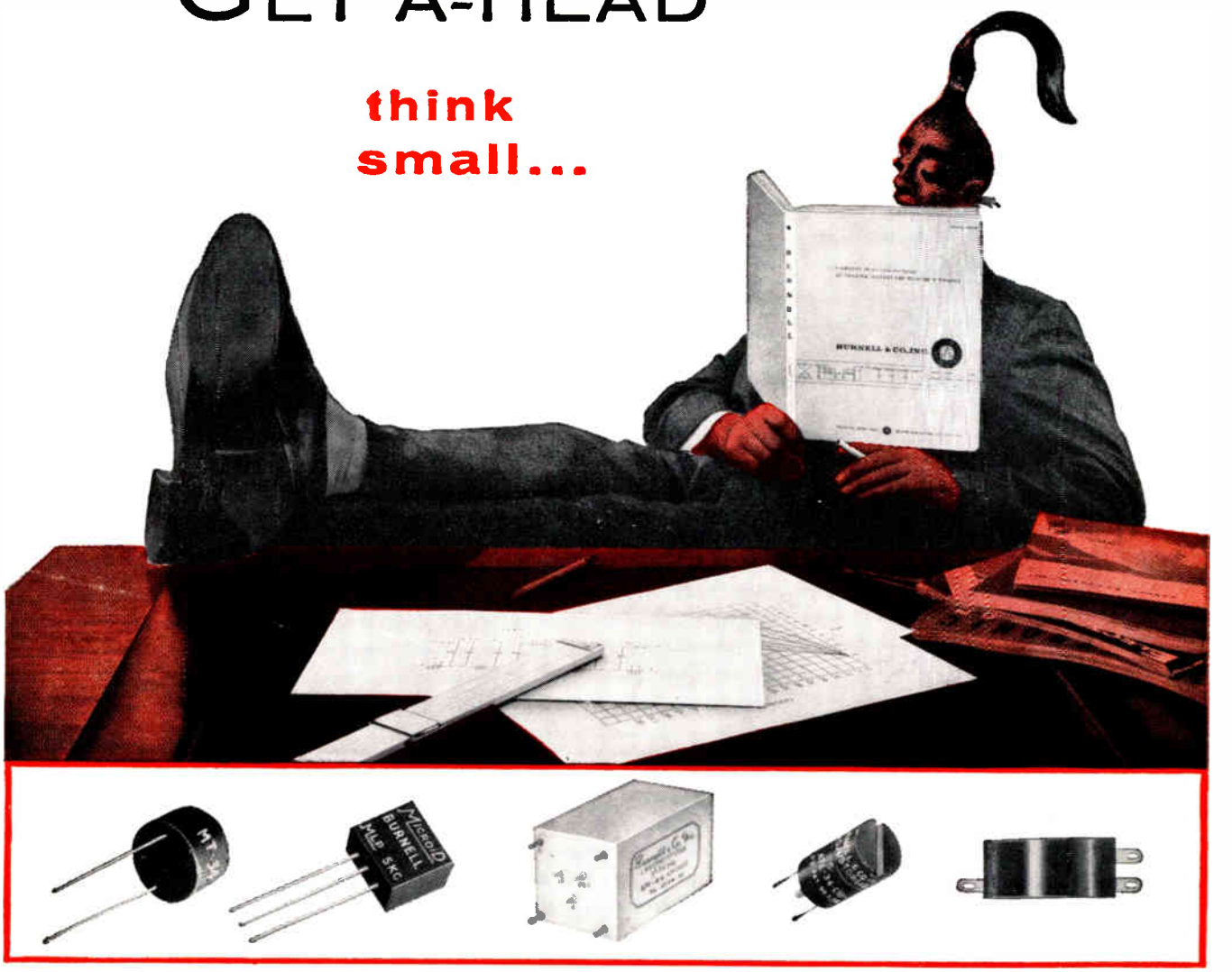
Write For Complete Catalog Information

KAY ELECTRIC COMPANY

Dept. I-1, Maple Avenue, Pine Brook, N.J., CApital 6-4000

GET A-HEAD

think small...



At Burnell & Co., our engineers devote a big part of their thinking to shrinking—reducing the size (and cost) of components to the least common denominator consistent with high performance standards. From this staff have come such components as:

The Kernel ATE Adjustoroid®—This variable toroid contains an actual complete toroid with all the excellent characteristics of the non-adjustable type. Valuable in oscillators, discriminators, variable tuned circuits, etc.

MLP and *MHP* *MICROID* ® Filters —Microminature counterparts of the popular Burnell TCL and TCH low pass and high pass filters, they range from .5 kc to 100 kc with a standard impedance of 10k ohms. Cascading the *MLP* with the *MHP* produces excellent response band pass characteristics.

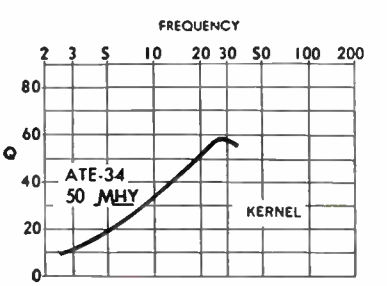
"Cheerio" Toroids — Subminiature high Q coils in a range of frequencies that make them ideal for transistorized equipment.

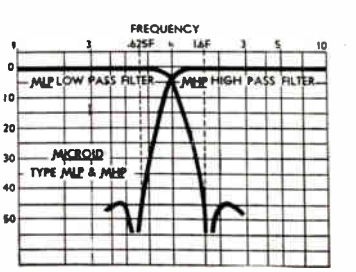
Crystal Filters—Advanced engineering techniques enable Burnell to offer at nominal cost, high selectivity, high attenuation crystal filters covering the extraordinary range of 1 kc to 30 mcs with considerable latitude in impedance.

Pulse networks, interference filters, active networks and magnetic amplifiers are among the newer additions to our product line.

Write for latest catalog.

Burnell & Co., Inc., has a number of positions available for engineers capable of thinking big and shrinking small. Inquiries are invited.





If you haven't already done so—send for your free membership in the Space Shrinkers Club.

Meetings with Exhibits

(Continued from page 8A)

June 19-20, 1961

Chicago Spring Conference on Broadcast and Television Receivers, O'Hare Inn, DesPlaines, Ill.

Exhibits: Mr. Roy Lee, Philco Corp., 6957 West North Ave., Oak Park, Ill.

June 26-28, 1961

Fifth National Convention on Military Electronics, Shoreham Hotel, Washington, D.C.

Exhibits: Mr. L. David Whitelock, 5614 Greentree Road, Bethesda 14, Md.

July 16-22, 1961

Fourth International Conference on Medical Electronics & Fourteenth Conference on Electrical Techniques in Medicine & Biology, Waldorf-Astoria Hotel, New York, N.Y.

Exhibits: Mr. Lewis Winner, 152 W. 42nd St., New York 36, N.Y.

August 22-25, 1961

Western Electronic Show and Convention (WESCON), Cow Palace and Fairmont Hotel, San Francisco, Calif.

Exhibits: Mr. Don Larson, WESCON, 1435 LaCienega Blvd., Los Angeles, Calif.

October 4-6, 1961

IRE Canadian Convention, Exhibition Park, Toronto, Canada

Exhibits: Business Manager, IRE Canadian Convention, 1819 Yonge St., Toronto 7, Ontario, Canada

October 9-11, 1961

National Electronics Conference, Hotel Sherman, Chicago, Ill.

Exhibits: Mr. Arthur H. Streich, National Electronics Conference, 228 N. LaSalle St., Chicago 1, Ill.

October 23-25, 1961

East Coast Conference on Aeronautical & Navigational Electronics, Lord Baltimore Hotel, Baltimore, Md.

Exhibits: Dr. Harold Schutz, Westinghouse Electric Corp., Air Arm Div., P.O. Box 746, Baltimore, Md.

November 14-16, 1961

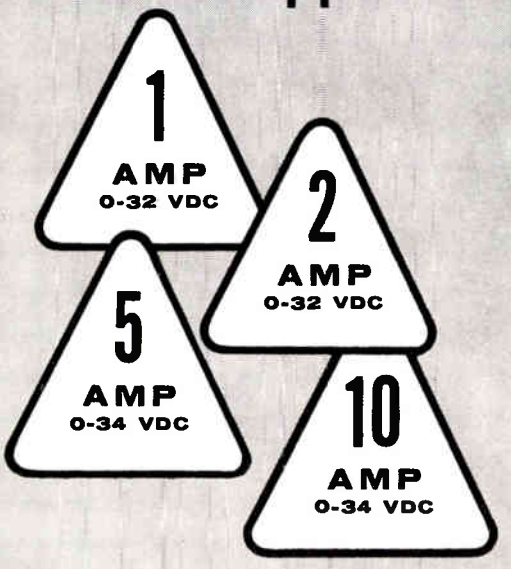
Northeast Electronics Research and Engineering Meeting (NEREM), Boston Commonwealth Armory, Boston, Mass.

Exhibits: NEREM, 313 Washington St., Newton, Mass.

Δ

Note on Professional Group Meetings: Some of the Professional Groups conduct meetings at which there are exhibits. Working committeemen on these groups are asked to send advance data to this column for publicity information. You may address these notices to the Advertising Department and of course listings are free to IRE Professional Groups.

LAMBDA
Transistorized Regulated Power Supplies



- **Convection cooled—no internal blowers to wear out.**
- **Guaranteed for a full 5 years.**
- **Compact. 1, 2, and 5 Amp only 3½" high, 10 Amp 7" high.**

- Ambient temperature 50°C.
- Excess ambient thermal protection.
- Special, high purity foil, hermetically sealed long-life electrolytic capacitors.
- Hermetically sealed transformer designed to MIL-T-27A.
- Remote sensing and DC vernier.

CONDENSED DATA ON LT SERIES

LT 1095M	(with meters)	0-32 VDC, 0-1 AMP	$315
LT 2095M	(with meters)	0-32 VDC, 0-2 AMP	395
LT 1095	(without meters)	0-32 VDC, 0-1 AMP	285
LT 2095	(without meters)	0-32 VDC, 0-2 AMP	365

MODEL	VOLTAGE BANDS
LT 1095, LT 1095M	0-8, 8-16, 16-24, 24-32
LT 2095, LT 2095M	0-8, 8-16, 16-24, 24-32

Regulation: Line: Better than 0.15 per cent or 20 millivolts (whichever is greater). For input variations from 105-125 VAC. **Load:** Better than 0.15 per cent or 20 millivolts (whichever is greater). For load variations from 0 to full load.

AC Input: 105-125 VAC, 50-400 CPS.

Ripple and Noise: Less than 1 millivolt rms.

Ambient Temperature: 50°C—continuous duty.

Remote DC Vernier: Provision for remote operation of DC Vernier.

Remote Sensing: Provision is made for remote sensing to minimize effect of power output leads on DC regulation, output impedance and transient response.

Size:
LT 1095 3½" H x 19" W x 14⅜" D
LT 2095 3½" H x 19" W x 14⅜" D

CONDENSED DATA ON LA SERIES

LA 50-03AM	(with meters)	0-34 VDC, 0- 5 AMP	$425
LA100-03AM	(with meters)	0-34 VDC, 0-10 AMP	540
LA 50-03A	(without meters)	0-34 VDC, 0- 5 AMP	395
LA100-03A	(without meters)	0-34 VDC, 0-10 AMP	510

MODEL	VOLTAGE STEPS
LA 50-03A, LA 50-03AM	— 2, 4, 8, 16 and 0-4 volt vernier
LA100-03A, LA100-03AM	— 2, 4, 8, 16 and 0-4 volt vernier

Regulation: Line: Better than 0.15 per cent or 20 millivolts (whichever is greater). For input variations from 100-130 VAC. **Load:** Better than 0.15 per cent or 20 millivolts (whichever is greater). For load variations from 0 to full load.

AC Input: 100-130 VAC, 60 ± 0.3 cycle. This frequency band amply covers standard commercial power lines in the United States and Canada.

Ripple and Noise: Less than 1 millivolt rms.

Ambient Temperature: 50°C—continuous duty.

Remote DC Vernier: Provision for remote operation of DC Vernier.

Remote Sensing: Provision is made for remote sensing to minimize effect of power output leads on DC regulation, output impedance and transient response.

Size:
LA 50-03A 3½"H x 19" W x 14⅜" D
LA100-03A 7" H x 19" W x 14⅜" D

LA 115

SEND TODAY FOR COMPLETE DATA.

LAMBDA ELECTRONICS CORP.
11-11 131 STREET • DEPT. 3 • COLLEGE POINT 56, N. Y. • INDEPENDENCE 1-8500

Now...12-Nanosecond Total Switching Time with CBS MADT* Transistors

Total switching time for typical CBS 2N501 and 2N501A transistors in this circuit is less than 12 nanoseconds. The basic circuit can readily be cascaded to form fast-switching ON and OFF stages for computers. Since the transistors have a high gain-bandwidth product at only -3 collector volts, the size and cost of your power supply can be substantially reduced.

The economical CBS 2N501 and 2N501A also offer a wide choice of design possibilities in other fast-switching circuits. Consult the table for high switching rates permitted in the variety of circuits shown.

Order engineering samples for your prototype design. Call or write for technical data and delivery information, today, from your local sales office or Manufacturer's Warehousing Distributor.

Wide Choice of Fast Switching Circuits
With CBS 2N501 and 2N501A

Logic Circuits	*Switching Rate*
Special non-saturating	140 mc
Emitter follower coupled	140 mc
Base gating	140 mc
Transformer coupled pulse	140 mc
Diode transistor logic (DTL)	20 mc
Resistor capacitor transistor logic (RCTL)	20 mc
Direct coupled transistor logic (DCTL)	7 mc
Resistor transistor logic (RTL)	1 mc
Pulse Generators & Shaping Circuits	
Blocking oscillators	10 mc
Regenerative amplifiers	10 mc
Schmidt trigger circuits	10 mc
Monostable multivibrators	5 mc
High Current Pulse Amplifiers†	
Line drivers	10 mc
Core drivers	10 mc
Read-write amplifiers	10 mc

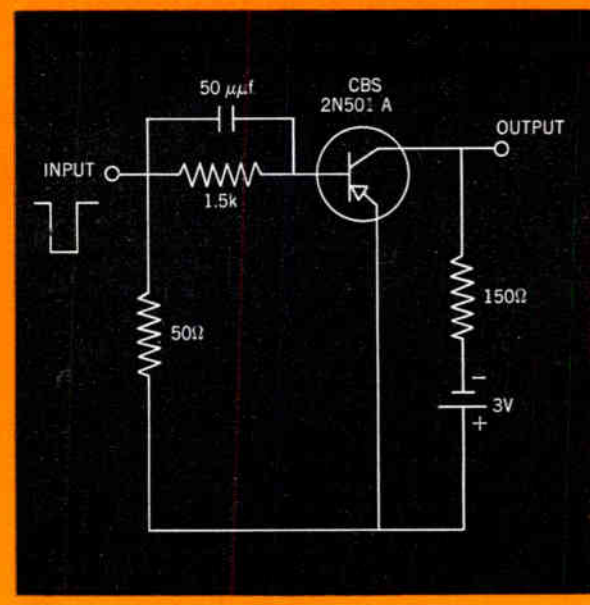
†Switching current, 35 ma.

*Micro Alloy Diffused-base Transistor, trade-mark, Philco Corp.

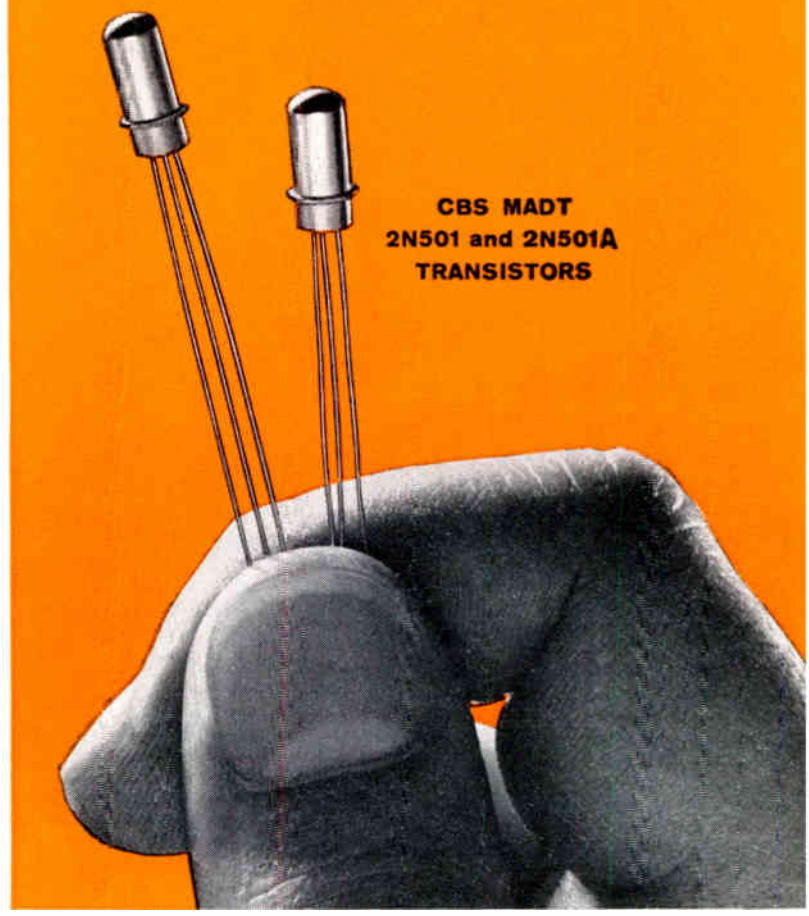
CBS semiconductors®

More Reliable Products through Advanced Engineering

Semiconductors for Computer Circuitry



IN THIS NEW CIRCUIT, CBS 2N501 and 2N501A transistors achieve delay, rise, storage and fall times of 2.0, 3.7, 3.2, and 2.3 ns respectively.



CBS ELECTRONICS, Semiconductor Operations, Lowell, Mass. • A Division of Columbia Broadcasting System, Inc.
Semiconductors • tubes • audio components • microelectronics

Sales Offices: Lowell, Mass., 900 Chelmsford St., GLenview 2-8961 • Newark, N. J., 231 Johnson Ave., TAlbert 4-2450 • Melrose Park, Ill., 1990 N. Mannheim Rd., EStebrook 9-2100 • Los Angeles, Calif., 2120 S. Garfield Ave., RAymond 3-9081 • Minneapolis, Minn., The Heimann Co., 1711 Hawthorne Ave., FEderal 2-5457 • Washington, D. C., 1735 Desales St., N.W., EMerson 2-9300 • Dayton, Ohio, 39 North Torrence St., CLearwater 2-1972 • Toronto, Ont., Canadian General Electric Co., Ltd., LEnnox 4-6311.

IRE News and Radio Notes

Current IRE Statistics

(As of November 30, 1960)
Membership—87,124
Section*—108
Subsections*—28
Professional Groups*—28
Professional Group Chapters—275
Student Branches†—195

* See November, 1960 for a list.
† See October, 1960 for a list.

Calendar of Coming Events and Authors' Deadlines*

1961

Symp. on Thermoelectric Energy Conversion, Statler Hotel, Dallas, Tex., Jan. 8–12. (DL*: Oct. 10, 1960, P. Klein, GE Co., Syracuse, N. Y.)
7th Natl. Symp. on Reliability and Quality Control, Bellevue-Stratford Hotel, Philadelphia, Pa., Jan. 9–11.
Symp. on Space Instrumentation, Washington, D. C., Jan. 16–17.
Conf. on Magnetic & Dielectric Devices, LMSD, Palo Alto, Calif., Jan.
2nd PGMIL Conf., Biltmore Hotel, Los Angeles, Calif., Feb. 1–3. (DL*: Nov. 15, 1960, Dr. J. J. Meyers, Hoffman Electronic Corp., Military Products Div., 3717 S. Grand Ave., Los Angeles, Calif.)
Int'l. Solid State Circuits Conf., University of Pennsylvania and Sheraton Hotel, Philadelphia, Pa., Feb. 15–17. (DL*: Oct. 14, 1960, J. J. Suran, Bldg. 3, Rm. 115, GE Co., Electronics Park, Syracuse, N. Y.)
Int'l. Symp. on Semiconductor Devices, UNESCO, 2 Place Fontenoy, Paris, February 20–25.
Symp. on Engrg. Aspects of Magnetohydrodynamics, Univ. of Pa., University Park, Mar. 9–10.
IRE Int'l. Conv., N. Y. Coliseum and Waldorf-Astoria Hotel, New York, N. Y., Mar. 20–23.
PIB Int'l. Symp. on Electromagnetics and Fluid Dynamics of Gaseous Plasma, N. Y., N. Y., April 4–6. (DL*: Dec. 20, 1960, Symp. Committee, Polytechnic Inst. of Brooklyn, 55 Johnson St., Brooklyn 1, N. Y.)
SWIRECO, Dallas, Tex., April 19–21.
7th Region Tech. Conf. & Trade Show, Westward Ho Hotel, Phoenix, Ariz., April 26–28.
Conf. Electro-Optical & Radiation Devices, IBM, San Jose, Calif., Apr.
Joint Automatic Techniques Conf., Cincinnati, Ohio, Apr.
Electronic Comp. Conf., Jack Tar Hotel, San Francisco, Calif., May 2–4.
Workshop in Graph Theory, University of Illinois, Urbana, May 6.

* DL = Deadline for submitting abstracts.

(Continued on page 15A)

IRE Elects Officers for 1961

Lloyd V. Berkner (A'26–M'34–SM'43–F'47), president of Graduate Research Center, Inc., Dallas, Tex., has been elected president for 1961 of the Institute of Radio Engineers. He succeeds Ronald L. McFarlan (SM'51), consultant to the DATAmatic Corporation and the Raytheon Manufacturing Company.

In accordance with a policy established last year, the IRE now has two vice presidents, one residing in North America and the other abroad. The vice president representing overseas countries for 1961 will be Franz Ollendorff (SM'52), research professor at the Technion-Israel Institute of Technology, Haifa, Israel. He succeeds J. A. Ratcliffe (M'29–A'32–F'53), head of radio research at the Cavendish Laboratory, Cambridge, England. The vice president representing North America will be J. F. Byrne (SM'45–F'50), manager of the Riverside Lab., Motorola, Inc., Riverside, Calif. He succeeds J. N. Dyer (J'30–A'32–SM'45–F'49), vice president of the Research and Engineering Division of Airborne Instruments Lab., Melville, N. Y.

Elected as directors for the 1961–1963 term are E. F. Carter (A'23–F'36), director and member o the Board of Directors, Stanford Research Institute, Menlo Park, Calif., and L. C. Van Atta (M'42–SM'43–F'52), Director of Technical Information and Education, Hughes Aircraft Co., Culver City, Calif.

Regional Directors elected for 1961–1962 are as follows: Region 2—A. B. Giordano (SM'46–F'59), Associate Dean in charge of the Graduate School and professor of electrical Engineering, Polytechnic Institute of Brooklyn, Brooklyn, N. Y.; Region 4—A. B. Bereskin (A'41–M'44–SM'46–F'59), professor of electrical engineering, University of Cincinnati, Cincinnati, Ohio; Region 6—M. W. Bullock (S'33–A'37–M'45–SM'54), Engineering Manager, Continental Electronics Manufacturing Co., Dallas, Texas; Region 8—B. R. Tupper (A'36–SM'36–F'54), Chief Engineer of the British Columbia Telephone Co., Vancouver, Canada.

1961 IRE International Convention Set for March

March 20 through 23 have been selected as the dates for the 1961 IRE International Convention, which will again be held at the Waldorf-Astoria Hotel and New York Coliseum in New York City. More than 70,000 engineers and scientists from 40 countries are expected to attend what has become the world's largest technical meeting and exhibition.

A comprehensive program of 275 papers, covering the most recent developments in the fields of all 28 IRE Professional Groups, will be presented in 54 sessions at the Waldorf-Astoria and the Coliseum. The high point of the program will be a special symposium on new energy sources to be held Tuesday evening, March 21. The complete program will be announced in the March issue of PROCEEDINGS.

The IRE Show, filling all four floors of the Coliseum, will accommodate approximately 850 exhibitors. Some $15,000,000 worth of the latest electronic equipment will be on display, most of it for the first time.

The social events will include a "get-together" cocktail party Monday evening and the annual IRE banquet Wednesday evening, both in the Grand Ballroom of the Waldorf. The banquet will feature the presentation of IRE Awards for 1961.

An entertaining program of tours, fashion shows and matinees is being arranged for wives of visitors.

Dr. George W. Bailey (*center*) (W2KH), Executive Secretary of the IRE and former President of the ARRL, accepts a citation from Edwin Piller (*left*) (W2KPQ), President of the Single Sideband Amateur Radio Association, during the annual dinner of the Quarter Century Wireless Association on October 14, 1960. The dinner, which was a testimonial for Dr. Bailey, was cosponsored by the Single Sideband Amateur Radio Association. John Di Blasi (*right*) (W2FX), President of the Quarter Century Wireless Association, later presented Dr. Bailey with a life membership in this organization.

German Electrotechnicians To Hold Convention

The Nachrichtentechnische Gesellschaft im VDE (Society of German Electrotechnicians) is holding the following meetings during its Convention, April 11–14, 1961, in Karlsruhe, Germany:

"Receiving and Processing of Information," and
"Learning Machines."

More than 30 experts from Germany and other countries will participate, and will present papers on the above-mentioned topics.

Final programs are available beginning January, 1961, without charge, from: Nachrichtentechnische Gesellschaft im VDE, Frankfurt a. M. S 10, Stresemann Allee 21, Germany.

Air Force MARS Announces Schedule

The January schedule for the Air Force MARS Eastern Technical Net, operating Sundays from 2 to 4 P.M. EDT, on 3295, 7540, and 15,715 kc, has been announced as follows:

January 1	No broadcast on this date.
January 8	"Exotic Applications of Semiconductors," R. R. Darden, American Bosch-Arma Corp.
January 15	"Passive Satellite Communications," H. Hoffman, Jr., Rome Air Development Center, USAF.
January 22	"Some Aspects of Extraterrestrial Communications," A. Feiner, Rome Air Development Center, USAF.
January 29	"Plasma Physics," Capt. Dr. P. Larsen, Rome Air Development Center, USAF.
February 5	"Titration with HF Radiation," Dr. Cefola, Fordham Univ.
February 12	"The Electron Emission Microscope," Fr. Schubert, S.J., Fordham Univ.

Telecommunications Exhibit To Be Held in Lisbon

The State Department advises that the Second International Exhibition of Telecommunications Photograph Art for professionals will take place in Lisbon in March, 1961. The exhibition is sponsored by the Portuguese Permanent Commission to commemorate the feast of the Archangel St. Gabriel.

The Salon is open only for telecommunications professionals. Two groups of prints are admitted: 1) Black and white prints and 2) Color Transparencies (slides) with the following sections: a) Artistic (free subject, artistic nude excluded) and b) Telecommunications.

Not more than four prints and/or four transparencies in *each section* may be sent in by each contributor. The size of the prints must be as follows: 1) Black and white—from a minimum of 18×24 cm to a maximum of 40×50 cm; 2) Color Transparencies —24×36 mm or 6×6 cm. Black and white prints must be sent unmounted, and color transparencies must be sent mounted in glass or cardboard and correctly spotted (in the lower left corner when viewed as appearing on the screen). The black and white prints must be sent separately from the color transparencies and all are to be forwarded by mail, as *registered* printed matter to: II Salão Internacional de Arte Fotográfica das Telecomunicações, Companhia Portuguesa Rádio Marconi, Estação Emissora de Alfragide, Amadora, Portugal, or against receipt when delivered personally.

Each print or transparency must bear on the back in block letters: a) section; b) name and address of the contributor; and c) number and title of the print or transparency corresponding with that on the entry form.

A jury, whose decisions will be final, will select the prints and transparencies and will distribute the prizes, awarding cups and medals to each group and section.

The right to reproduce any of the accepted prints, either in the catalogue or in the press, will be assumed unless otherwise mentioned in the entry form.

Among those who attended the PGED Meeting in Washington, D. C., October 27–28, 1960, were (*left to right*) J.A. Hornbeck, Bell Telephone Laboratories, Conference Chairman; H.W. Welch, Jr., Motorola, Inc., Technical Program; and A. K. Wing, Jr., Hughes Aircraft Co., Chairman, Professional Group on Electron Devices.

Calendar of Coming Events and Authors' Deadlines*

(Continued from page 14A)

5th Midwest Symp. on Circuit Theory, Allerton Park & Urbana Campus, Univ. of Ill., Urbana, May 7-8.

NAECON, Miami & Biltmore Hotels, Dayton O., May 8–10. (DL*: Abstracts, Jan 1; Papers, March 7, A. J. Wilde, 4136 Lotz Rd., Dayton 29, Ohio.)

Western Joint Computer Conf., Ambassador Hotel, Los Angeles, Calif., May 9–11. (DL*: Dec. 12, 1960, Dr. W. F. Bauer, Ramo-Wooldridge Co., 8433 Fallbrook Ave., Canoga Park, Calif.)

Microwave Theory and Tech. Nat'l. Symp., Sheraton Park Hotel, Washington, D. C., May 15–17.

GLOBCOM V, Sherman Hotel, Chicago, Ill., May 22–24. (DL*: Nov. 31, 1960, D. C. Campbell, I. T. T.-Kellogg, 5959 S. Harlem Ave., Chicago 38, Ill.)

Nat'l. Telemetering Conf., Chicago, Ill., May 22–24. (DL*: Dec. 15, 1960, J. Becker, AC Spark Plug Div., G.M. Corp., Milwaukee 1, Wis.)

3rd Nat'l. Symp. on Radio Frequency Interference, Washington, D. C., June 12–13.

5th Nat'l. Symp. on Product Engrg. and Production, Philadelphia, Pa., June 13–14.

Chicago Spring Conf. on Broadcast and Television Receivers, O'Hare Inn, DesPlaines, Ill., June 15–16. (DL*: Feb. 15, 1961, N. Frihardt, Motorola Inc., 4545 W. Augusta Blvd., Chicago, Ill.)

MIL-E-CON 1961, Shoreham Hotel, Washington, D. C., June 26–28. (DL*: Feb. 1, 1961, H. Davis, SAFRD, The Pentagon, Washington 25, D.C.)

JACC, Univ. of Colorado, Boulder, June 28–30. (DL*: Abstracts, Nov. 15, 1960; Papers, Dec. 15, 1960, R. Kramer, 1961 JACC Program Committee, Bldg. 32, M.I.T., Cambridge, Mass.)

4th Int'l. Conf. On Medical Electronics & 14th Conf. on Elec. Techniques in Medicine & Biology, Waldorf-Astoria, Hotel, N. Y., N. Y., July 16–22. (DL*: April 1, 1961, H. P. Schwan, Moore School of E.E., Philadelphia 4, Pa.)

WESCON, San Francisco, Calif., Aug. 22–25.

1961 Symp. on Transmission & Processing of Information, M.I.T., Cambridge, Mass., Sept. 6–8. (DL*: Abstracts, Jan. 1, 1961; Papers, April 1, 1961, P. Elias, M.I.T., Cambridge, Mass.)

1961 Nat'l. Symp. on Space Electronics and Telemetry, Albuquerque, N. M., Sept. 6–8.

Joint Nuclear Instrumentation Symp., North Carolina State College, Raleigh, N. C., Sept. 6–8.

9th Ann. Engrg. Management Conf., New York, N. Y., Sept. 14–16.

10th Ann. Industrial Electronics Symp., Boston, Mass., Sept. 20–21.

1960 Radio Fall Mtg., Syracuse Hotel, Syracuse, N. Y., Oct. 30–31, Nov. 1.

IRE Canadian Conv., Exhibition Park, Toronto, Can., Oct. 4–6.

* DL = Deadline for submitting abstracts.

Eta Kappa Nu Honors Young Engineers

Kenneth H. Olsen (S'48-A'53) of Bedford, Mass., has been named Outstanding Young Electrical Engineer of 1960 by Eta Kappa Nu Association, national electrical engineering society. Among the honorable mentions in this national competition were Dr. Robert R. Johnson (S'50–M'56) of Phoenix, Ariz., and Thomas H. Thompson (S'50–A'53–M'57) of Basking Ridge, N. J.

The 1960 award is the twenty-fourth since 1936. Formal presentation of the awards will be made at a banquet on January 30, 1961, during the Winter General Meeting of the American Institute of Electrical Engineers. The banquet will be held in the Governor Room, Hotel Govenor Clinton, Seventh Avenue at 31 Street, New York, N. Y. The cocktail hour will start at six P.M., and the dinner promptly at seven P.M. All electrical engineers, whether members of Eta Kappa Nu or not, are invited to the traditional and important event. Ladies are cordially invited.

Reservations for the banquet should be mailed to: W. Levidow, Rm. 3B-154, Bell Telephone Labs., Inc., Whippany, N. J. Reservations postmarked on or before January 25, 1961, will be honored at $6.50 per person. Later reservations, or those made at AIEE Registration Headquarters during the Winter General Meeting, will cost $7.50 per person. Checks or money orders should be made payable to New York Alumni Chapter, Eta Kappa Nu. Attendance at the banquet is limited and reservations will be honored in the order received up to the limit of space available.

An informal, yet dignified, program has been arranged to honor these truly outstanding young men. The principal address, "Why We Need Engineers as Well as Scientists," will be delivered by Dr. J. R. Pierce, Director of Research, Bell Telephone Labs., Inc. Dr. Pierce was an award recipient himself in 1942.

Mr. Olsen, a native of Bridgeport, Conn., is 34 years old and received the B.S. and M.S. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1950 and 1952. As a graduate student, he invented a magnetic matrix switch for use with coincident current magnetic memories. Following graduation, he became a staff member of the Digital Computer Laboratory of M.I.T., and supervised the group responsible for the first digital computer to use magnetic core random-process memory. He was one of the leaders in the design of computers for the Sage air defense system. Later, he was one of the first to build a high-performance digital computer using transistors. In 1957, he founded and became president of Digital Equipment Corporation, a concern that has created and marketed transistorized building blocks for the computer industry.

Dr. Johnson is 32 years old and a graduate of the University of Wisconsin, Madison, in 1950. He received the M.S. degree from Yale University, New Haven, Conn., in 1951 and the Ph.D. degree from the California Institute of Technology, Pasadena, in 1956. He is presently with the General Electric Company as Manager of Engineering in the Computer Department.

He discovered a new dynamic relationship in sequential logic which is used to simplify the static Boolean equations used in digital computers.

He has made numerous contributions to the computer field, and has half a dozen patents for his inventions.

Mr. Thompson is 32 years old and a graduate of the University of Texas, Austin, in 1951. He received the M.S. degree in 1952 from the same university. Since graduation, he has been employed by Bell Telephone Laboratories in Whippany, N. J., and has been directly concerned with the development of Command Guidance Systems for the Titan ICBM and for Thor-Able, Tiros, and Delta Space Vehicles.

OBITUARIES

Harry H. Goode (SM'52), Professor of Electrical Engineering at the University of Michigan, Ann Arbor, and a leader in the activities of the IRE Professional Group on Electronic Computers, died in an automobile accident on October 30, 1960.

H. H. Goode

He was born in New York, N. Y., on July 1, 1909. He received the B.S. degree in history from New York University, New York, N. Y., in 1931, the Bachelor of Chemical Engineering degree from Cooper Union, New York, N. Y., in 1940, and the M.A. degree in mathematics from Columbia University, New York, N. Y., in 1945. His early professional work was in statistics, and in 1941, he became Statistician-in-Charge for the New York City Department of Health. During the war years, he was a research associate at Tufts College, Medford, Mass., and worked on applications of probability to war problems and also on the acoustic torpedo problem. From 1946 through 1949, he was on the staff of the Office of Naval Research at the Special Devices Center, Sands Point, L. I. Here he progressed through successive responsibilities to be head of the Special Projects Branch.

In 1950, he joined the Willow Run Research Center of the University of Michigan, serving there as head of the Systems Analysis and Simulation Group, as Chief Project Engineer, and finally as Director of the Center.

In 1954, he was appointed Professor of Electrical Enginering at the University of Michigan, and in 1956 received a dual appointment as Professor of Electrical Engineering and also Professor of Industrial Engineering. In 1958 he served for a year as Technical Director of the Systems Division of the Bendix Corporation, maintaining a fractional appointment in the University so that he could continue to teach his newly-introduced course on system design. In 1959, he returned to full-time teaching and research in the Department of Electrical Engineering.

Professor Goode also served as a consultant to industry and government and was active in professional society affairs. Among the firms for which he consulted were the United Aircraft Corporation, the Bendix Corporation, the Auerbach Electronics Corporation, the Du Pont Corporation, the Ford Motor Company, the Burroughs Corporation, the Texas Company, and the Franklin Institute. He served the government as a consultant to the National Bureau of Standards, the Post Office Department, the Air Force, and the House of Representatives Appropriations Committee. For the Air Force, he was chairman of the W-117L Committee on Advanced Reconnaissance; and for the House Committee, he served as a member of the Study Group on Missile Reliability.

He served his profession as a member of the Administrative Committee of the Professional Group on Electronic Computers from 1953–1956, as a member of the Computer Advisory Committee of the Society of Automotive Engineers, and as a member of a subcommittee of the AIEE Committee on Feedback Controls. He served as chairman of the National Joint Computer Committee of the IRE, AIEE, and ACM.

Professor Goode was a member of the Association for Computing Machinery, the American Mathematical Society, the Mathematical Association of America, and the Institute for Mathematical Statistics. He was also a Fellow of the American Association for the Advancement of Science, and a member of Sigma Xi, Eta Kappa Nu, and Mu Alpha Omicron.

His many published papers touched upon statistics, simulation and modeling, vehicular traffic control, and system design. His major published work is the book, "System Engineering," of which he was senior author with R. E. Machol.

His broad experience with computers and his participation in national computer functions led to his participation as one of the group of eight Americans who visited Soviet computer establishments in 1959.

Professor Goode contributed substantially to this special Computer Issue of the PROCEEDINGS by assisting in the review of papers for this issue.

Dr. E. Vernon Potter (SM'59), Director of the Physics and Electronics Division of the U. S. Naval Civil Engineering Laboratory, Port Hueneme, Calif., died suddenly, October 6, 1960. Born in Baltimore, Md., in 1908, he was educated at The Johns Hopkins University, Baltimore, receiving the B.E. degree in 1928 and the Doctorate of Engineering degree in 1932.

His professional career was spent in Government Research Laboratories in the Bureau of Mines, Bureau of Ships, and Bureau of Yards and Docks, where he was recognized as an authority in the fields of Underwater Acoustics and electromagnetic radiation. He was a frequent contributor to the literature relating to his special fields. He was listed in "American Men of Science" and "Who's Who in Engineering."

Dr. Potter was a member of Tau Beta Pi, the American Institute of Electrical Engineers, American Geophysical Union, American Society of Metals, Sigma Xi, Research Society of America, and was a Registered Professional Engineer in Utah.

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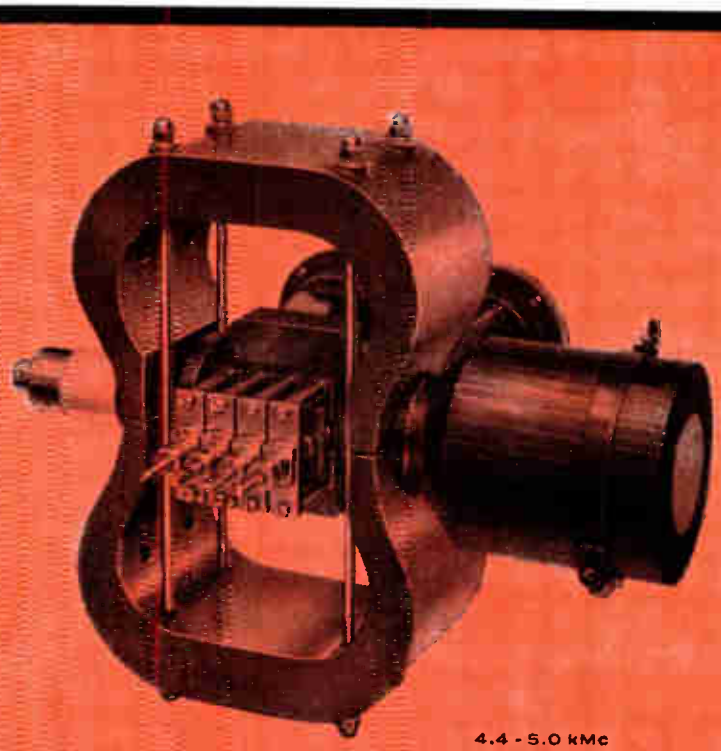

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Call for Papers Issued by Annual NAECON

The Thirteenth Annual National Aerospace Electronics Conference (NAECON) now invites submission of papers for the 1961 Conference, which will be held at the Miami and Biltmore Hotels, Dayton, Ohio, May 8–10, 1961. The theme of the Conference is "Electronic Technology in the Aerospace Age."

The technical papers program will continue the practice of scheduling only four concurrent sessions during each conference period, with topics selected and balanced to minimize conflicts of audience interest. Discussion or critique periods will be conducted immediately following the formal papers in each session. These arrangements should enhance the quality and real value of the NAECON technical program. As of this date, the following subjects have been suggested as session topics:

Energy Conversion Systems
Solid State Devices
Radio Astronomy
Ground Support Equipment
Aerospace Reconnaissance Systems
Molecular Electronics
Magnetohydrodynamics
Aerospace Systems Integration
Bionics
Aerospace Communications
Antennas and Propagation
Aerospace Environment
Vehicle-Borne Computers
Guidance and Control Systems
Telemetry
Systems Management
Microwave Tubes and Circuits
Scientific Education
Audio Technique
Electromagnetic Interference
Electric Propulsion

Workers in this field are urged to submit papers for presentation by January 15, 1961, to R. G. Stimmel, 809 Larriwood Avenue, Dayton 25, Ohio.

Microelectronics and Systems Call for Papers

The July, 1961, issue of the IRE Transactions on Military Electronics will be devoted entirely to the subject of microelectronics and systems.

The aim will be not so much to present a review of the state of the art as it exists today, as to project the ten- or twelve-year future, with the hope of stimulating the thinking of military systems people in the potentiality that will be created by those revolutionary changes now visible on the horizon of circuit design.

The issue will contain one or two invited papers summarizing current thought in the field, but the rest of the issue will be devoted to reports of original investigation.

Topics which should be covered include:

1) New solid-state device techniques and assembly methods, including functional devices and integrated electronics.

2) Problems which the microminiature systems designer will need to overcome; for example, the compounded unreliability problem and systems having many thousand parts.

3) The heat dissipation problem and factors related to it, such as: a) means for removing heat; b) methods for calculation of temperature distribution in a microminiature assembly; c) systems size and dimensional limitation imposed by heat generation; d) the inter-relationship among circuit speed, component precision, and minimum heat generation.

4) Critical appraisal of methods for interconnection of components and circuits.

5) Entirely new type of electronic systems either made possible or necessary by microminiaturization.

6) Specification for nonexistent, but needed devices to make microelectronics possible.

7) Critical review of typical military electronics problems and the influence microelectronics can have on their solution.

Detailed abstracts should be submitted by February 8, 1961, to: Dr. J. E. Thomas, Jr., Sylvania Electric Products, Inc., 100 Sylvan Rd., Woburn, Mass. The abstracts will be reviewed and the authors of the papers selected will be notified by February 20, 1961. April 15, 1961, is the deadline for submission of finished manuscripts.

Standard IRE practice should be followed in preparation of the manuscripts. All illustrations should either be originals or glossy prints thereof. Each author should submit a photograph and biography of himself for inclusion in the contributor section.

Call for Papers

5th National Convention on Military Electronics
(MIL-E-CON 1961)

June 26-28, 1961

Shoreham Hotel, Washington, D. C.

The 5th National Convention on Military Electronics (MIL-E-CON 1961) will be held at the Shoreham Hotel, Washington, D. C., on June 26–28, 1961, under the sponsorship of the Professional Group on Military Electronics of The Institute of Radio Engineers. Major General F. L. Ankenbradt, USAF (Ret.), member of the Technical Staff of Defense Electronic Products, RCA, Camden, New Jersey, is Convention President for MIL-E-CON 1961.

Papers presenting original work in military electronics are invited for this meeting. Suggested topics include, but are not limited to, the following:

Current Problems of Space Technology
Space Electronics
Ranging and Tracking
Electronic Propulsion
Data Handling Systems
Guidance and Control
Inertial Systems
Reconnaissance Systems
Communication Systems
Operational Analysis
Reliability

The technical program will include both classified (limited to Confidential) and unclassified sessions, with the Air Research and Development Command sponsoring the classified sessions. An unclassified and bound *Proceedings* of the convention will be available at the meeting.

Prospective authors are requested to furnish the following information, *not later than February 1, 1961:*

Three copies of a 750-word unclassified abstract of the proposed paper, plus the name and position of the author and the name and address of his company or organization.

Three copies of a biographic sketch of the author(s), including education, experience, memberships in professional societies, honors, publications.

Each author must obtain the appropriate military and company clearances for his abstract.

Send abstracts to: H. Davis, SAFRD, The Pentagon, Washington 25, D. C.

New ideas for MIL-E-CON 1961, to be held in Washington, D. C., June 26–28, 1961, are discussed by members of the planning committee. Committee chairmen (*left* to *right*): L. D. Whitelock, Exhibits; C. De Vore; Public Relations; Maj. Gen. F. L. Ankenbrandt, USAF (Ret.), Convention President; B. J. Goldfarb, Proceedings, H. Davis, Technical Program; and W. Hulse, Arrangements. Attendance at MIL-E-CON 1960 was nearly 5000; an even larger attendance is seen for MIL-E-CON 1961.

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The Model Thach can be used independently as a true RMS measuring instrument powered by any appropriate source. It checks its own accuracy against an internal standard cell, and is furnished completely self contained with a high sensitivity galvanometer. General specifications are as follows: Accuracy ± .2% F.S. (.1% at self-check points). Ranges 10/20/50/100/200/500 ma; 1/2/5 amps; 1/2/5/10/20/50/100/200/500/1000 v. Frequency range DC and 7 cps. to 4 kc. Sensitivity 100 ohms volt. Thermocouple D'Arsonval type. 100 division 6.3" hand drawn mirrored scale. Temperature compensated from 20°C. — 30°C. 1000% manually operated overload protection system. Independent of influence of stray magnetic fields. Diamond Pivoted with sapphire shock mounted jewels. Furnished with 1 or 2 thermocouples. Available in two combinations: 1x is self checking at full scale only: 3x is self checking at 5 cardinal points including full scale. Size 16⅜" x 10½" x 8¾" deep. Weight approx. 21 lbs.

Model THACH AND THACH-PS

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SPECIFICATIONS:

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WAVEFORM: 60 cps distortion 2.5% total harmonic content plus line distortion.

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Harold Stout (*left*), Chairman of the Kansas City Section, presents the Kansas City Section Award to Dr. C. N. Kimball (*right*), President of the Midwest Research Institute, for his outstanding contributions to the advancement of science and technology. The presentation was made during the 12th Annual Mid-America Electronics Conference (MAECON), November 15–16, 1960, which had an attendance of over 1000 people.

Call for Papers

1961 Western Electronic Show and Convention (WESCON)

August 22-25, 1961

Cow Palace, San Francisco, Calif.

The 1961 Western Electronic Show and Convention now issues a call for papers for its 1961 meeting, which is to be held August 22–25, at the Cow Palace in San Francisco, Calif.

Prospective authors are required to submit 100- to 200-word abstracts and 500- to 1000-word detailed summaries of their papers by May 1, 1961, in order to be considered for inclusion in the program. They will be notified by June 1, 1961, of acceptance or rejection of their papers.

Submissions should be sent to: E. W. Herold, c/o WESCON's Northern California Office, 701 Welch Road, Palo Alto, Calif.

Twenty-five instrument manufacturers, institutions and government agencies had exhibits at the 13th Annual Conference on Electrical Techniques in Medicine and Biology, October 31-November 1-2, 1960, which was sponsored by the IRE, the AIEE, and the ISA.

1961 Winter Convention On Military Electronics To Be Held In Los Angeles

An attendance of 3000 is expected for the 2nd Winter Convention on Military Electronics, which will be held from February 1–3, 1961. Again this year, the conference will be held in the Biltmore Hotel, Los Angeles, Calif. A program of approximately 100 technical papers as well as 60 exhibits is planned.

A. N. Curtiss

Arthur N. Curtiss (*left*) is this year's Convention Chairman, and Dr. John Meyers is Program Chairman. Vice Admiral John T. Hayward, Chief of Naval Research, will be the speaker at the banquet which will be held February 2.

The Professional Group on Military Electronics is sponsoring the Convention, and the Los Angeles Section is the host.

A tentative list of the technical program sessions is as follows:

Wednesday Morning, February 1

1) Panel Discussion—"Improving Research Effectiveness in Military Electronics"

Wednesday Afternoon

2) Reconnaissance (Confidential)
3) Inertial Guidance (Confidential)
4) Location Devices and Techniques
5) Data Memories
6) Telemetry
7) Reliability I

Thursday Morning, February 2

8) Antennas (Confidential)
9) VLF Communications (Confidential)
10) Microwave Tubes
11) Machine Decision Making
12) Extreme Environments
13) Reliability II

Thursday Afternoon

14) Electronic Warfare (Confidential)
15) Data Processing (Confidential)
16) Communications
17) System Planning, Analysis, and Use
18) System Test and Support Equipment
19) Refrigeration and Low Noise Design

Friday Morning, February 3

20) Propagation (Confidential)
21) Spacecraft Instrumentation
22) Power Conversion
23) Data Displays
24) Radar
25) Multiplexing and Switching

Friday Afternoon

26) Sonar and Displays (Confidential)
27) Spacecraft Communications and Control (Confidential)
28) Microwave Components and Optical Pumping
29) Solid State Device Applications

IRE Announces 1961 Awards

Ralph Bown (M'22–F'25)(L), renowned former Bell Telephone Laboratories scientist, and Ernst A. Guillemin (A'41–SM'48–F'49), Webster Professor of Electrical Engineering at Massachusetts Institute of Technology, Cambridge, were among those named by the Institute of Radio Engineers to receive IRE awards in 1961. Presentations of the awards will take place at the 1961 IRE International Convention banquet on March 22 at the Waldorf-Astoria Hotel, New York, N. Y.

Mr. Bown has been named to receive the 1961 Founders Award, "For outstanding service to the IRE and for outstanding contributions to the radio engineering profession through wise and courageous leadership in the planning and administration of technical developments which have greatly increased the impact of electronics on the public welfare." This is one of the two highest IRE awards and is bestowed only on special occasions.

Dr. Guillemin will receive the 1961 Medal of Honor, the highest annual technical award in the field of electronics. He will be given the award "for outstanding scientific and engineering achievements."

Five additional awards will be given as follows:

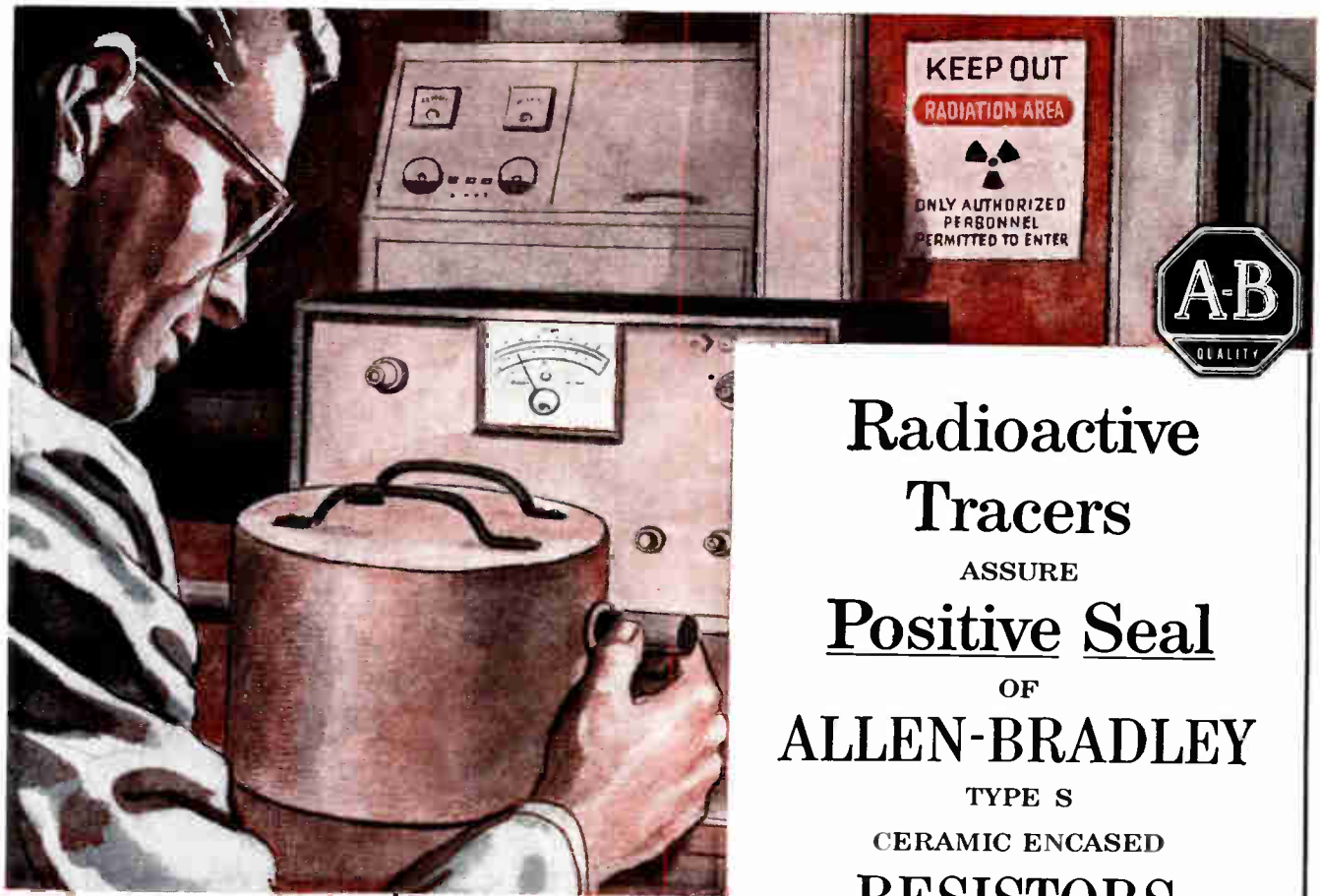
1961 Morris N. Liebmann Memorial Prize. (Awarded to a member of the IRE for a recent contribution to the radio art.) To Leo Esaki (SM'60), consultant at IBM Research Lab., Poughkeepsie, N. Y. (on leave from Sony Corp., Japan) "for important contributions to the theory and technology of solid state devices, particularly as embodied in the tunnel diode."

1961 Browder J. Thompson Memorial Prize Award. (Awarded for an IRE paper combining the best technical contribution and presentation which has been written by an author under thirty.) To Eiichi Goto, University of Tokyo, Tokyo, Japan, for his paper entitled, "The Parametron, a Digital Computing Element which Utilizes Parametric Oscillation," which appeared in the August, 1959, issue of Proceedings of the IRE.

1961 Harry Diamond Memorial Prize Award. (Awarded to a person in government service for outstanding contributions in the field of radio or electronics as evidenced by publication in professional journals.) To Helmut L. Brueckmann (SM'49–F'58), U. S. Army Signal Research and Development Laboratories, Fort Monmouth, N. J. "for outstanding contributions to the theory and technology of antennas."

1961 W. R. G. Baker Award. (Awarded to the author of the best paper published in the IRE Transactions of the Professional Groups.) To Manfred Clynes (SM'49), Rockland State Hospital, Orangeburg, N. Y. for his paper entitled, "Respiratory Control of Heart Rate: Laws Derived from Analog

Continued on page 22.



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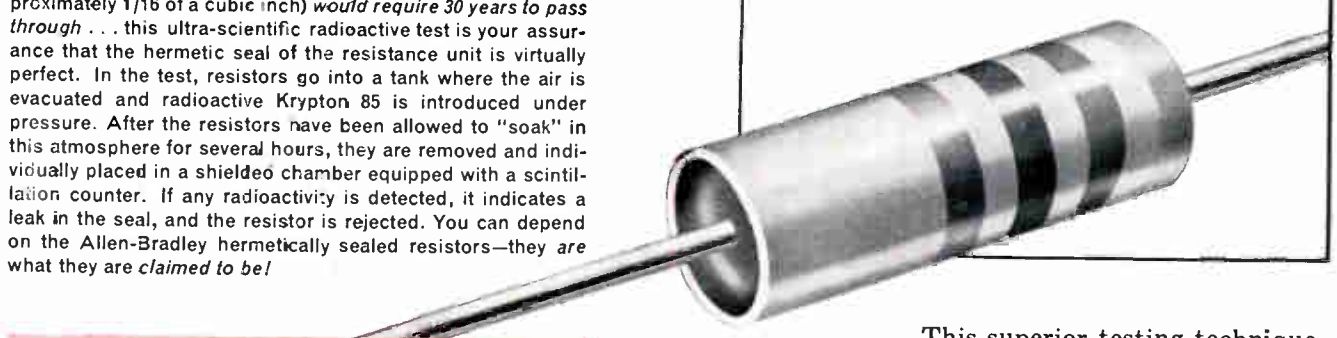

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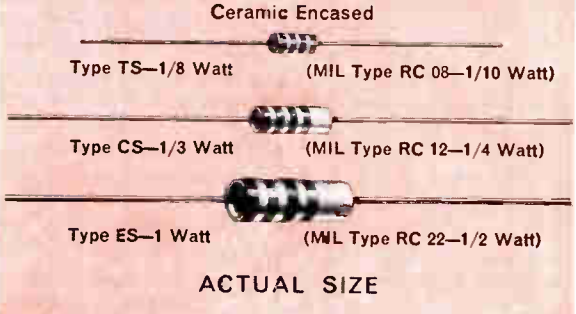

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Computer Simulation," which appeared in the January, 1960, issue of IRE TRANSACTIONS ON MEDICAL ELECTRONICS.

1961 Vladimir K. Zworykin Prize Award. (Awarded to a member of the IRE for important technical contributions to electronic television.) To Peter C. Goldmark (A'36–M'38–F'43), CBS Laboratories, Stamford, Conn., "for important contributions to the development and utilization of electronic television in military reconnaissance and in medical education."

1961 William J. Morlock Professional Group on Bio-Medical Electronics Prize Award. (Awarded for important contributions in the field of Bio-Medical Electronics and given for the first time this year.) To Britton Chance (M'46–SM'46–F'54), Professor and Director, Johnson Research Foundation, University of Pennsylvania, Philadelphia, Pa., "for the application of a variety of advanced electronic techniques in a long-term program of fundamental biological research."

PROFESSIONAL GROUP NEWS

At its meeting on November 14, 1960, the IRE Executive Committee approved the following new Chapters: PG on **Bio-Medical Electronics**—Cleveland Chapter, PG on **Electronic Computers**—Joint New York and Northern New Jersey Chapter, and PG on **Radio Frequency Interference**—San Francisco Chapter.

International Solid State Circuits Conference

UNIVERSITY OF PENNSYLVANIA AND SHERATON HOTEL, PHILADELPHIA, PA., FEBRUARY 15–17, 1961

The 1961 International Solid State Circuits Conference will be held February 15–17, at the University of Pennsylvania and the Sheraton Hotel, Philadelphia, Pa. Sponsoring bodies are the IRE Professional Group on Circuit Theory, the AIEE, and the University of Pennsylvania. The formal opening of the Conference will be Wesdnesday afternoon, February 15. T. R. Finch, Bell Telephone Labs., Inc., Chairman of the Conference, will deliver the introductory comments. Also, G. P. Harnwell, President of the University of Pennsylvania, will give a welcoming address. A. P. Stern, Electronics, Lab., G. E. Co., Chairman of the 1960 Conference, will present the 1960 Conference Awards. J. G. Linvill, of Stanford Electronics Labs., Stanford University, will speak on the subject, "How Can Solid-State Electronics Mature Without Losing Its Youth?"

The program of the conference will be as follows:

Wednesday Morning, February 15

Session 1—New Device Characteristics

Chairman: *E. O. Johnson, RCA, Somerville, N. J.*

"A Survey of Tunnel Diode Equivalent Circuits," *E. Baldinger, Univ. of Basel, Basel, Switzerland.*

"Efficiency and Linearity of Multi-Contact Hall Plates," *G. Arlt, Philips Zentrallaboratorium, Eindhoven, Holland.*

"An Analysis of a Nonlinear Transmission Line," *R. B. Riley, Hewlett-Packard Co., Palo Alto, Calif.*

"A Comparison of the Diffusion-Limited Semiconductor Diode and the Space-Charge-Limited Dielectric Diode," *G. T. Wright, Univ. of Birmingham, Birmingham, England.*

"Superconducting Tunneling Devices," *I. Gaever, Res. Lab., G. E. Co., Schenectady, N. Y.*

Session 2—Microwave Amplifiers

Chairman: *E. W. Sard, Airborne Instruments Lab., Melville, N. Y.*

"The Characteristics of an Esaki-Diode at Microwave Frequencies," *H. Fukui, Sony Corp., Tokyo, Japan.*

"Some X-Band Microwave Tunnel-Diode Circuits," *R. Trambarulo, Bell Telephone Labs., Inc., Holmdel, N. J.*

"Parametric Excitation and Amplification Using Esaki Diodes," *T. Yamamoto and A. Kishimoto, Res. and Dev. Center, Japan Defense Agency, Japan.*

"High-Frequency and High-Power Operation of Tunnel Diodes," *C. S. Kim and J. B. Hopkins, Electronics Lab., G. E. Co., Syracuse, N. Y.*

"Waveguide Parametric Amplifiers," *B. C. DeLoach, Jr., Bell Telephone Labs., Inc., Holmdel, N. J.*

Wednesday Afternoon

Session 3—Logic I

Chairman: *J. J. Suran, Electronics Lab., G. E. Co., Syracuse, N. Y.*

"Parametron and Tunnel Diode Progress in Japan," *E. Goto, Univ. of Tokyo, Tokyo, Japan.*

"The Neuristor," *H. D. Crane, Stanford Res. Inst., Menlo Park, Calif.*

"Gain and Geometrical Considerations in Planar Optoelectronic Circuits," *T. E. Bray, Electronics Lab., G. E. Co., Syracuse, N. Y.*

"Flow Table Logic," *J. A. O'Connell, E. J. Skiko, and P. Low, IBM Corp., Poughkeepsie, N. Y.*

"Hydraulic Counterparts of Electronic Logic Components as Possible New Elements for Control," *H. H. Glaettli, IBM Corp., Zurich, Switzerland.*

Session 4—Power and Control

Chairman: *P. F. Pittman, Westinghouse Electric Corp., Pittsburgh, Pa.*

"Calculation of Offset Voltage in Saturated Switches," *J. Gibbons, Stanford Univ., Stanford, Calif.*

"A New DC Differential Transistor Amplifier," *D. Hilbiber, Fairchild Semiconductor Corp., Palo Alto, Calif.*

"Improved Magnetic Voltage Stabilizer Employing Silicon-Controlled Rectifiers," *E. W. Manteuffel, Advanced Systems Lab., G. E. Co., Ithaca, N. Y.*

"A Control Circuit for *PNPN* Regulated Rectifiers," *R. J. Healey, Bell Telephone Labs., Inc., N. Y., N. Y.*

"Redundancy Techniques in Reliable Power Supply Design," *D. A. Paynter and V. P. Mathis, Electronics Lab., G. E. Co., Syracuse, N. Y.*

Wednesday Evening

Informal Discussion Sessions

1—High-Frequency Measurements and Characterization of Transistors

Moderator: *A. K. Rapp, Philco Corp., Philadelphia, Pa.*

Panel Members: *M. M. McWhorter, Stanford Univ., Stanford, Calif.; V. H. Grinich, Fairchild Semiconductor Corp., Palo Alto, Calif.; V. R. Saari, Bell Telephone Labs., Inc., Murray Hill, N. J.; Y. C. Hwang, Electronics Lab., G. E. Co., Syracuse, N. Y.; R. P. Abraham, Texas Instruments Inc., Dallas, Tex.; E. J. Rymaszewski, IBM Corp., Poughkeepsie, N. Y.*

2—Microwave Applications

Moderator: *R. M. Ryder, Bell Telephone Labs., Inc., Murray Hill, N. J.*

Panel Members: *M. E. Hines, Microwave Associates, Inc., Burlington, Mass.; B. C. DeLoach, Bell Telephone Labs., Inc., Holmdel, N. J.; F. R. Arams, Airborne Instruments Labs., Melville, N. Y.; E. Baldinger, Univ. of Basel, Basel, Switzerland; J. H. Forster, Bell Telephone Labs., Inc., Murray Hill, N. J.; E. Stern, Electronics Lab., G. E. Co., Syracuse, N. Y.; K. K. N. Chang, RCA, Princeton, N. J.*

3—Micro-Power Circuit Operation

Moderator: *R. L. Trent, Fairchild Semiconductor Corp., Mountain View, Calif.*

Panel Members: *C. D. Simmons, Philco Corp., Lansdale, Pa.; R. D. Lohman, RCA, Somerville, N. J.; G. Saltus, Bell Telephone Labs., Inc., Whippany, N. J.; R. Schultz, Fairchild Semiconductor Corp., Mountain View, Calif.; R. H. Baker, MIT Lincoln Labs., Lexington, Mass.; R. A. Henle, IBM Corp., Poughkeepsie, N. Y.*

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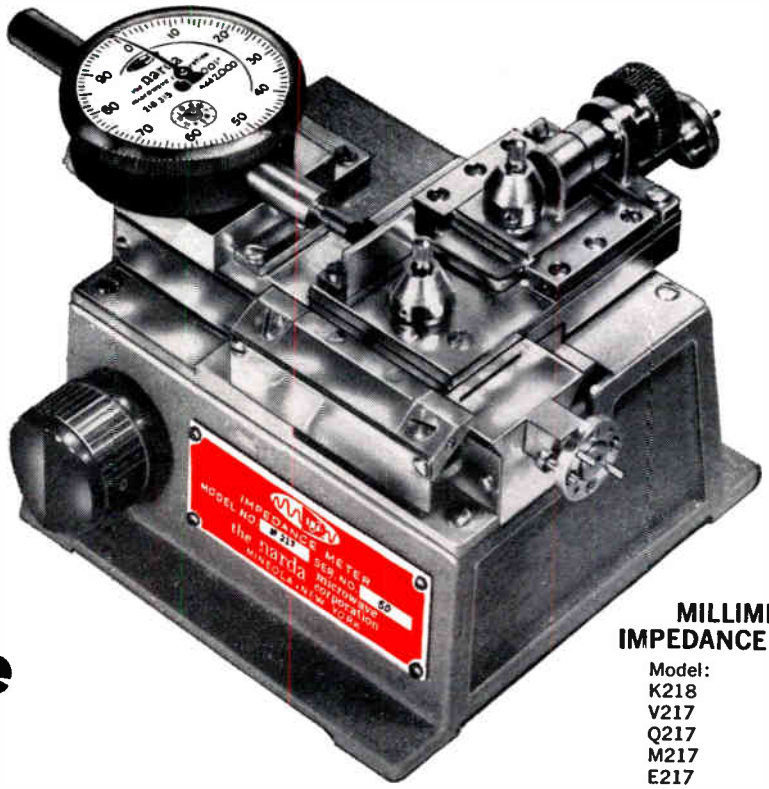

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4—New Logic Techniques

Moderator: *E. Stabler, Electronics Lab., G. E. Co., Syracuse, N. Y.*

Panel Members: *H. D. Crane, Stanford Res. Inst., Menlo Park, Calif.; U. F. Gianola, Bell Telephone Labs., Inc., Murray Hill, N. J.; W. W. Davis, Remington Rand Univac, St. Paul, Minn.; S. Einhorn, Burroughs Corp., Paoli, Pa.; M. H. Lewin, RCA Labs., Princeton, M. J.; E. Goto, Univ. of Tokyo, Tokyo, Japan; M. K. Haynes, IBM Corp., N. Y., N. Y.; G. B. Chaplin, Plessey Co., Ltd., Hants, England; J. A. O'Connell, IBM Corp., Poughkeepsie, N. Y.*

5—Reliability

Moderator: *B. T. Howard, Bell Telephone Labs., Inc., N. Y., N. Y.*

Panel Members: *E. R. Kretzmer, Bell Telephone Labs., Inc., Murray Hill, N. J.; R. R. Painter, RCA, Somerville, N. J.; J. W. Tarzwell, Autonetics Div., North American Aviation, Inc., Downey, Calif.; K. G. Ashar, IBM Corp., Poughkeepsie, N. Y.; C. H. Zierdt, G. E. Co., Syracuse, N. Y.*

6—Power Conversion and Control

Moderator: *L. Bright, Westinghouse Electric Corp., Cheswick, Pa.*

Panel Members: *D. Paynter, Electronics Lab., G. E. Co., Syracuse, N. Y.; R. P. Putkovich, Westinghouse Electric Corp., Cheswick, Pa; H. Storm, General Engrg. Lab., G. E. Co., Schenectady, N. Y.; A. Walker, Westinghouse Mfg. Co., Ltd., London, England.*

Thursday Morning, February 16

Session 5—New Technologies

Chairman: *J. M. Early, Bell Telephone Labs., Inc., Murray Hill, N. J.*

"Problems of Microminiaturization," *G. Mollenstedt and R. Speidel, Univ. of Tübingen, Tübingen, West Germany.*

"Progress Report on Thin Film Circuitry," *R. G. Counihan, IBM Corp., Federal Systems Div., Kingston, N. Y.*

"Investigation of a Thin-Film Thermal Transducer," *J. G. Gottling, MIT, Cambridge.*

"Properties and Applications of Diffused Silicon Transistors Using Epitaxial Techniques," *W. B. Cagle, H. J. Patterson, and H. E. Talley, Bell Telephone Labs., Inc., Whippany, N. J., and Allentown, Pa.*

"KMC Planar Transistors in Microwatt Logic Circuitry," *D. F. Allison, R. H. Beeson and R. M. Shultz, Fairchild Semiconductor Corp., Palo Alto, Calif.*

Session 6—Computer Magnetics

Chairman: *R. H. Baker, MIT Lincoln Lab., Lexington.*

"The Application of Domain Wall Motion to Storage Devices," *H. Rubinstein, T. L. McCormack and H. W. Fuller, Lab. for Electronics, Inc., Boston, Mass.*

"A Study of Switching in Thin Magnetic Films," *W. Dietrich and W. E. Proebster, IBM Corp., Zurich, Switzerland.*

"AC and Impulse Switching Techniques for Fixed Random Access and Analog Memory Use," *R. E. McMahon, MIT Lincoln Lab., Lexington.*

"A Word-Organized Memory Which Builds Address Decoding Into the Topology of the Ferrite Sheet," *E. E. Newhall, Bell Telephone Labs., Inc., Murray Hill, N. J.*

"Circuit Approach for an All-Magnetic Computing System," *H. D. Crane and E. Van De Riet, Stanford Res. Inst., Menlo Park, Calif.*

Thursday Afternoon

Session 7—Logic II

Chairman: *G. B. Chaplin, Plessey Co., Ltd., Hants, England.*

"100-Mc Nonsychronous Computer Circuitry Using Esaki Diodes," *J. R. Turnbull, Jr., IBM Corp., Poughkeepsie, N. Y.*

"High Speed Switching Circuitry Using Tunnel Diodes," *W. V. Harrison and R. S. Foots, Texas Instruments, Inc., Dallas, Tex.*

"Rapid-Transfer Principles for Transistor Switching Circuits," *A. K. Rapp and J. L. Robinson, Res. Div., Philco Corp., Philadelphia, Pa.*

"Determination of the Switching Speeds of Transistors by Stored Charge and Effective Life Time," *Y. C. Hwang, D. S. Cleverley, and D. J. Monsour, Semiconductor Products Dept., G. E. Co., Syracuse, N. Y.*

"Continuous Phase Regenerative Logic," *W. F. Chow, Sperry-Rand Corp., Philadelphia, Pa.; W. Peil, H. Raillard, and R. Marolf, Electronics Lab., G. E. Co., Syracuse, N. Y.*

Session 8—Microwave Applications

Chairman: *A. Uhlir, Jr., Microwave Associates, Inc., Burlington, Mass.*

"PIN Diodes for Protective Limiter Applications," *D. Leenov and J. H. Forster, Bell Telephone Labs., Inc., Murray Hill, N. J.; N. G. Cranna, CBS Electronics, Stamford, Conn.*

"Low-Level Garnet Limiters," *M. Grace, F. R. Arams, and S. Okwit, Airborne Instruments Lab., Melville, N. Y.*

"Microwave Tunnel Diode Autodyne Receiver," *F. Sterzer, A. Presser, and A. H. Solomon, Electron Tube Div., RCA, Princeton, N. J.*

"A New Broadband Absorption Modulator for Rapid Switching of Microwave Power," *F. Reggia, Diamond Ordnance Fuze Labs., Washington, D. C.*

"Fast One-Kilomegacycle Ferrite Switch," *E. Stern and R. E. Cole, Electronics Lab., G. E. Co., Syracuse, N. Y.*

Thursday Evening

Informal Discussion Sessions

7—Low-Frequency, Low-Level Signal Amplification

Moderator: *W. Moore, Jr., Brown Instrument Div., Minneapolis-Honeywell Regular Co., Philadelphia, Pa.*

Panel Members: *D. B. Bell, Texas Instruments Inc., Dallas, Tex.; J. S. MacDougall, Raytheon Co., Needham, Mass.; D. A. Robinson, Airpax Electronics, Inc., Ft. Lauderdale, Fla; E. G. Nielson, Electronics Lab., G. E. Co., Syracuse, N. Y.; D. Hilbiber, Fairchild Semiconductor Corp., Palo Alto, Calif.; M. W. P. Strandberg, Cambridge Electronics Corp., Newton Lower Falls, Mass.*

8—A Second Look at Microelectronics

Moderator: *E. Fletcher, MIT, Cambridge.*

Panel Members: *A. P. Stern, Electronics Lab., G. E. Co., Syracuse, N. Y.; J. Nall, Fairchild Semiconductor Corp., Palo. Alto, Calif.,; R. Alberts, WADD, Dayton, Ohio; T. Stanley, RCA Labs., Princeton, N. J.; S. J. Angello, Westinghouse Electric Corp., Pittsburgh, Pa.; V. J. Kublian, Engrg. Lab., U. S. Army Signal Corps, Fort Monmouth, N. J.; R. G. Counihan, IBM Corp., Poughkeepsie, N. Y.; W. Gaertner, CBS Labs., Inc., Stamford, Conn.; E. Keonjian, American Bosch Arma Corp., Garden City, N. Y.; G. Mollenstedt, Univ. of Tübingen, Tübingen, West Germany.*

9—Tunnel Diodes

Moderator: *E. O. Johnson, RCA, Camden, N. J.*

Panel Members: *L. Cuccia, RCA, Harrison, N. J.; J. Tiemann Res. Lab., G. E. Co., Schenectady, N. Y.; S. Sharpe, Bell Telephone Labs., Inc., Murray Hill, N. J.; J. A. Walsh, IBM Corp., Poughkeepsie, N. Y.; J. R. Biard Texas Instruments, Inc., Dallas, Tex.*

10—Access and Storage Techniques

Moderator: *A. Lo, IBM Corp., Poughkeepsie, N. Y.*

Panel Members: *J. E. Mack, Bell Telephone Labs., Inc., Whippany, N. J.; S. M. Rubens, Sperry-Rand Univac, St. Paul, Minn.; M. Rosenberg, Telemeter Magnetics, Los Angeles, Calif.; E. A. Fisch, Electronics Lab., G. E. Co., Syracuse, N. Y.; R. McMahon, MIT Lincoln Lab., Lexington; J. Rajchmann, RCA Labs., Princeton, N. J.; Q. W. Simkins, IBM Corp., Poughkeepsie, N. Y.*

11—Optical Masers

Chairman: *A. L. Schawlow, Bell Telephone Labs., Inc., Murray Hill, N. J.*

Panel Members: *R. T. Daly, Technical Res. Group, Inc., Syosset, L. I., N. Y.; G. C. Dacey, Bell Telephone Labs., Inc., Murray Hill, N. J.; M. Stevenson, IBM Corp., Yorktown, N. Y.; G. Wessel, Electronic Lab., G. E. Co., Syracuse, N. Y.; G. Bernbaum, Hughes Res. Lab., Malibu, Calif.*

Friday Morning, February 17

Session 9—Storage

Chairman: *R. A. Henle, IBM Corp., Poughkeepsie, N. Y.*

"A New Load-Sharing Matrix Switch," *N. G. Vogl, Jr., IBM Corp., Poughkeepsie, N. Y.*

"A 12-Kilobit, 5-Microsecond Twistor Variable Store," *W. B. Gaunt and D. C. Weller, Bell Telephone Labs., Inc., Murray Hill, N. J.*

"An Evaporated Film 135—Cryotron Memory Plane," *J. P. Beesley, Federal Systems Div., IBM Corp., Kingston, N. Y.*

"Coincident Current Superconductive Memory," *L. L. Burns, G. A. Alphonse, and G. W. Leck, RCA Labs., Princeton, N. J.*

"High-Speed Tunnel-Diode Memory," *D. L. Berry and E. A. Fisch, Electronics Lab., G. E. Co., Syracuse, N. Y.*

Session 10—Communication Circuits and Techniques

Chairman: *R. L. Pritchard, Texas Instruments, Inc., Dallas, Tex.*

"Optical Masers," *G. C. Dacey, Bell Telephone Labs., Inc., Murray Hill, N. J.*

"Wide-Band Esaki Diode Amplifiers," *G. E. Sharpe, Bell Telephone Labs., Inc., Murray Hill, N. J.*

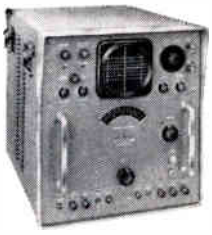
"High Speed Analog-to-Digital Converter Utilizing Tunnel Diodes," *R. A. Kaenel, Bell Telephone Labs., Inc., Murray Hill, N. J.*

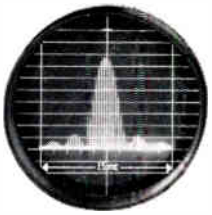
"Superregenerative Circuits Using Tunnel Diodes," *J. F. Bogusz and H. H. Schaffer, Res. Div., Philco Corp., Philadelphia, Pa.*

VISUAL MICROWAVE ANALYSIS 10 to 44,000 mc

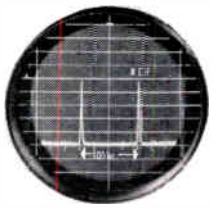
MODEL TSA
DIRECT-READING SPECTRUM ANALYZER

10 to 44,000 mc with five plug-in tuning units

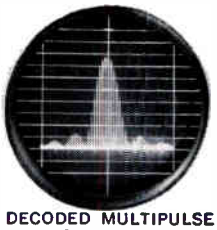




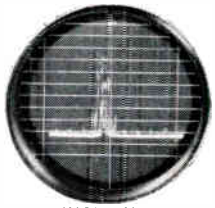
0.4 μSEC PULSE



STANDARD SIGNAL



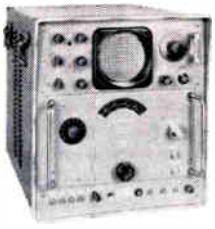
DECODED MULTIPULSE SPECTRUM

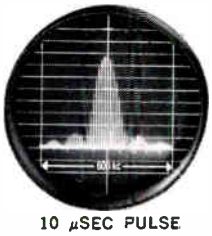


INCIDENTAL FM ANALYSIS

MODEL TSA-S
COMBINATION SYNCHROSCOPE-SPECTRUM ANALYZER

10 to 44,000 mc with five plug-in tuning units





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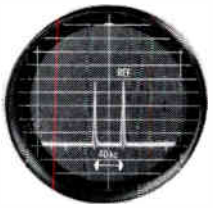

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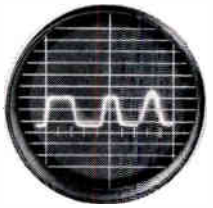
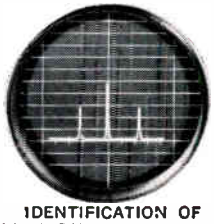


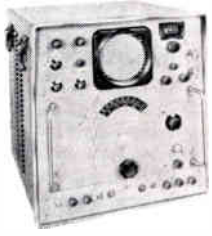
ANALYSIS AS A FUNCTION OF TIME

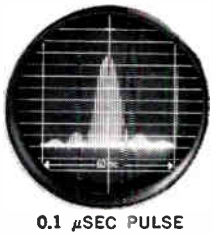


IDENTIFICATION OF AMPLITUDE MODULATION

MODEL TSA-W
WIDE DISPERSION SPECTRUM ANALYZER

10 to 44,000 mc with five plug-in tuning units—70 mc dispersion





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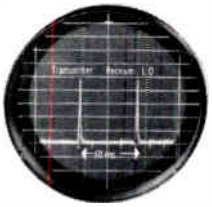
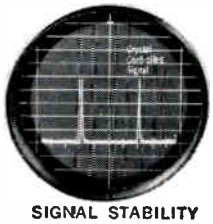


AFC ACTION

LOG DISPLAY



SIGNAL STABILITY MEASUREMENT

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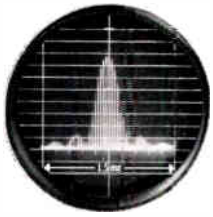
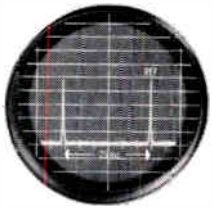
UNIVERSAL SPECTRUM ANALYZER

10 to 44,000 mc in one integrated self-contained unit



4 μSEC PULSE



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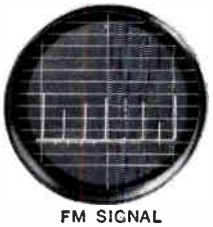
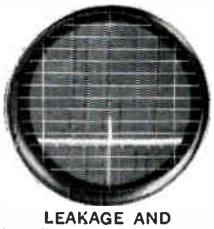


FM SIGNAL ANALYSIS

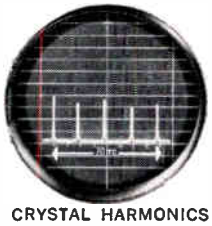


LEAKAGE AND RADIATION MEASUREMENT

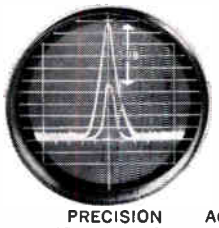
MODEL SA-84W
WIDE DISPERSION UNIVERSAL SPECTRUM ANALYZER

10 to 44,000 mc in one integrated self-contained unit—features over 80 mc dispersion

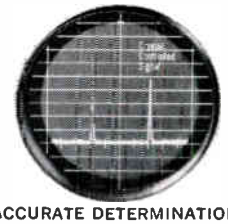
0.08 μSEC PULSE



CRYSTAL HARMONICS



PRECISION ATTENUATION



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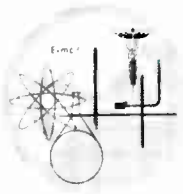

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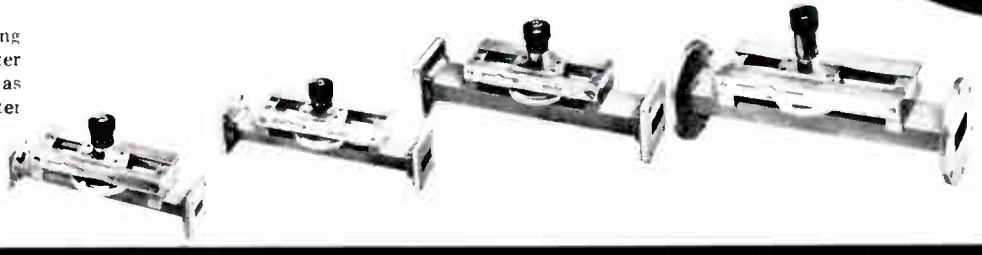

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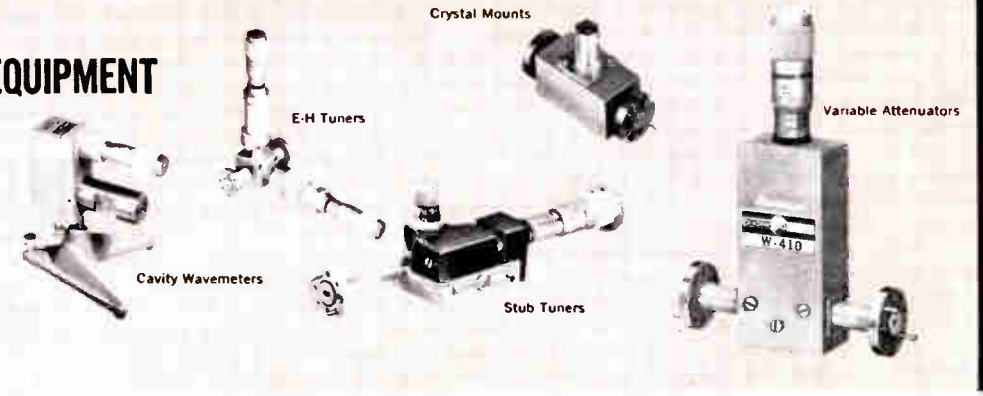

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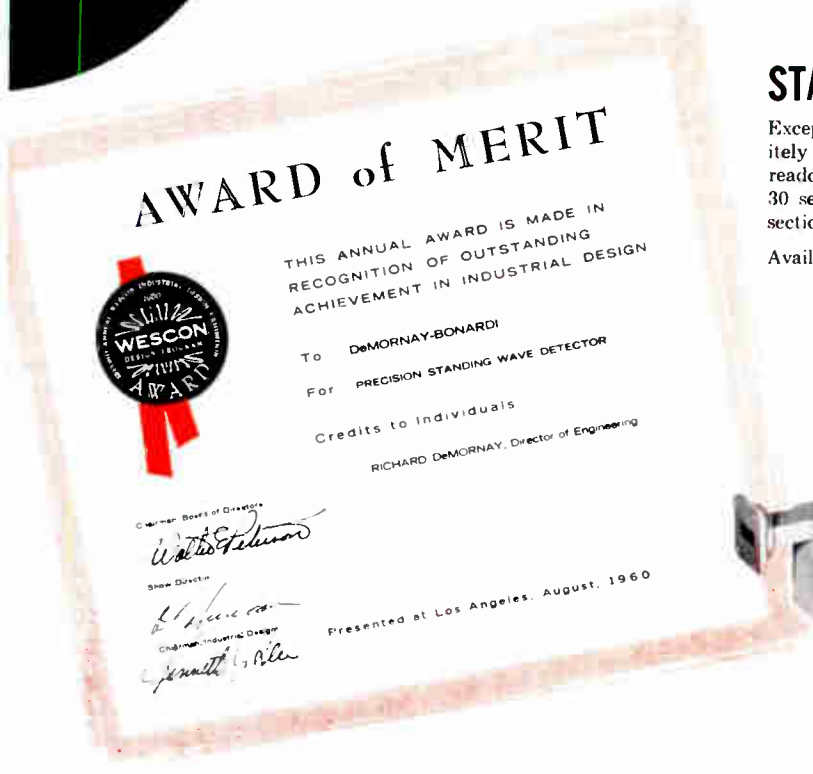

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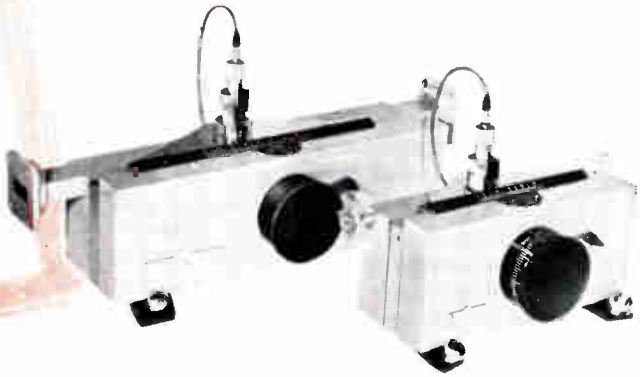

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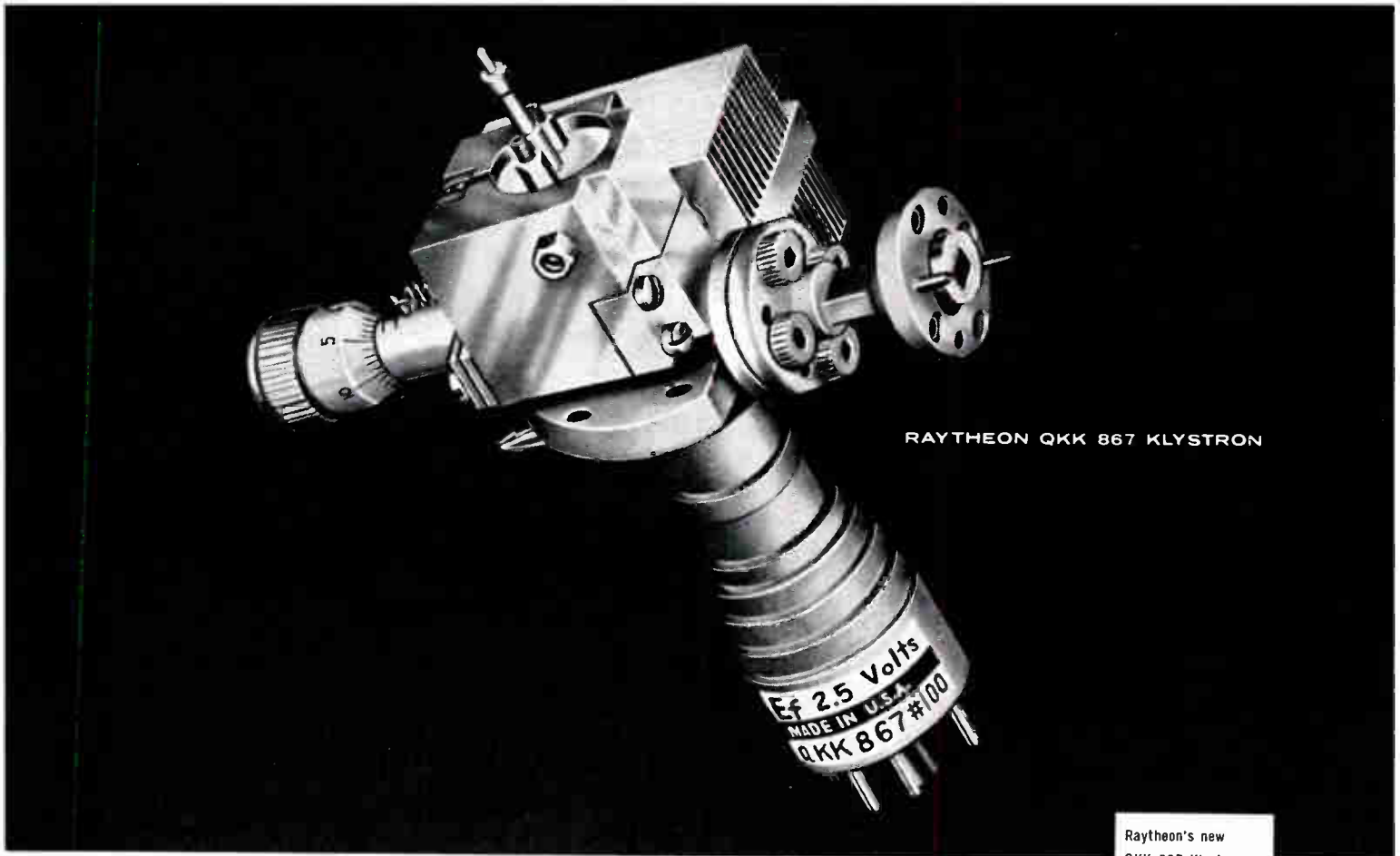

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Focus voltage	-150V	
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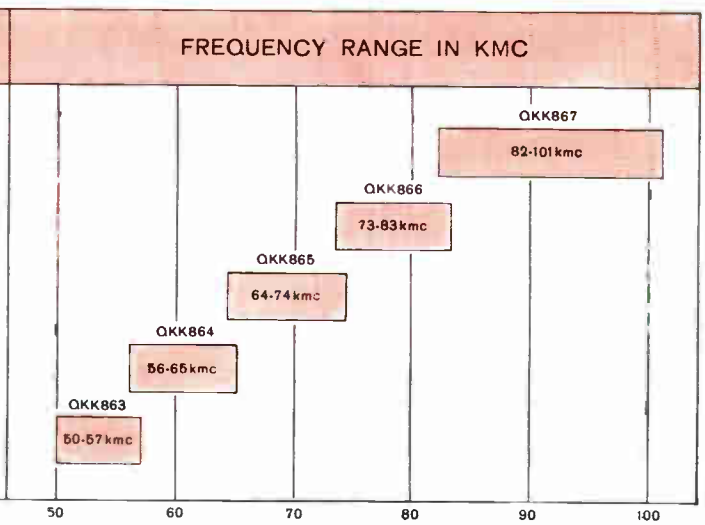
Heater current	1.5A	
Tuner turns	10	
Power output (min)	25 mW	10 mW



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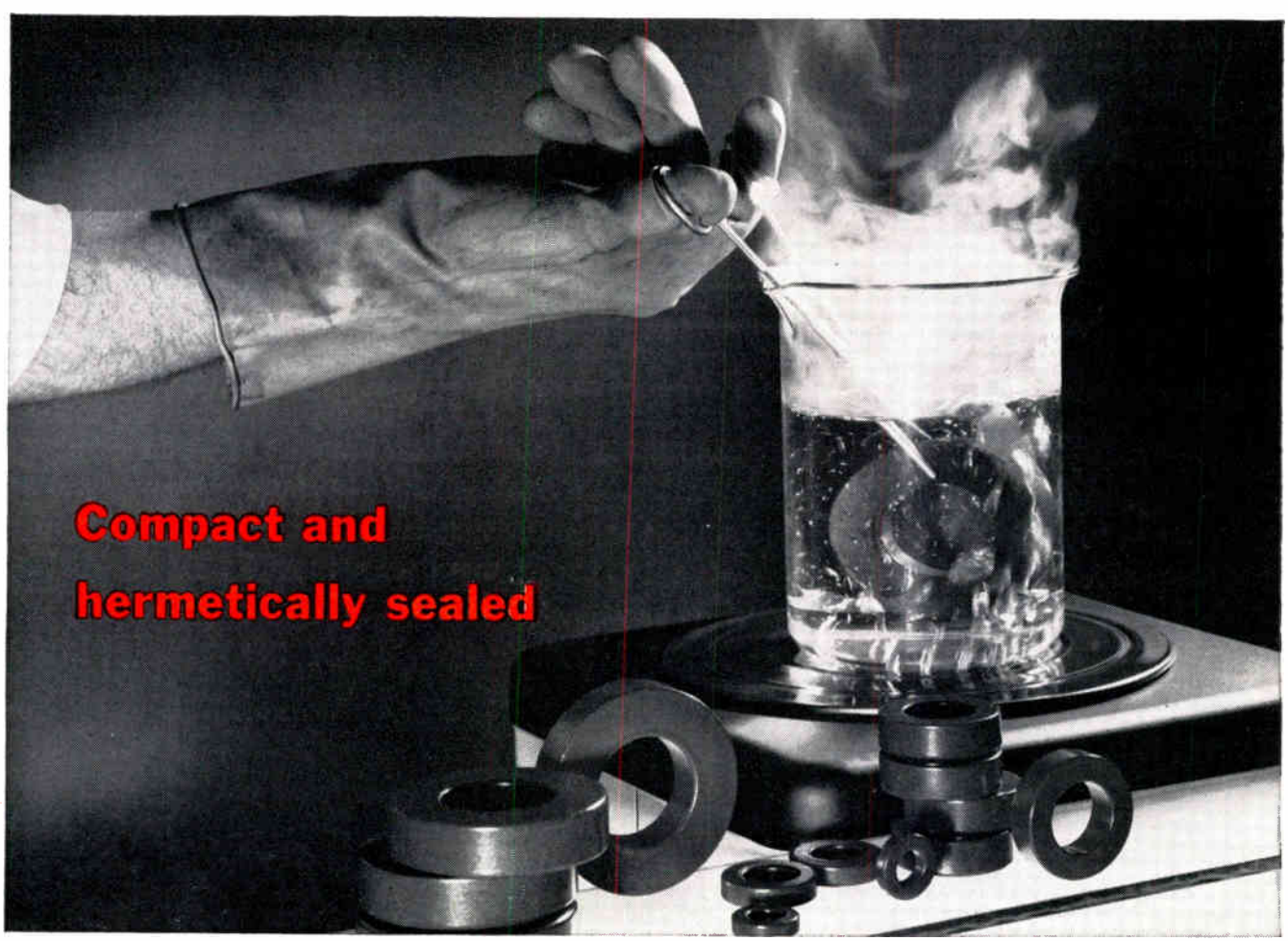


Rio de Janeiro—J. A. Wiltgen, Caixa Postal 450, Rio de Janeiro, D.F., Brazil; L. C. Bahiana, Rua Bogari 70, Apt. 102, Lagoa, Rio de Janeiro, Brazil.

Rochester (1)—H. F. Hicks, Jr., 120 Lynnwood Dr., Rochester 18, N. Y.; D. Y. Keim, 55 Council Rock Ave., Rochester 10, N. Y.

Rome-Utica (1)—M. P. Forte, 904 DeWitt Lane, Rome, N. Y.; D. L. Dakan, 102 Victory Dr., Rome, N. Y.

Sacramento (7)—F. C. Jacob, Dept. of Agricultural Engrg., Univ. of Calif., Davis, Calif.; J. R. Kowalczyk, 3730 Las Pasas Way, Sacramento 25, Calif.

St. Louis (6)—R. D. Hill, Jr., 363 Gray Ave., Webster Groves 19, Mo.; G. E. Barnard, 639 N. 69 St., East St. Louis, Ill.

Salt Lake City (7)—C. L. Alley, Elec. Engrg. Dept., Univ. of Utah, Salt Lake City, Utah; J. E. Dalley, 3920 S. 1380 E., Salt Lake City 17, Utah.

San Antonio-Austin (6)—G. E. White, Box 9006, Allandale Station, Austin 17, Tex.; F. X. Bostick, 5002 Beverly Hills Dr., Austin 3, Tex.

San Diego (7)—R. E. Honer, 5462 Mary Lane Dr., San Diego 15, Calif.; E. W. Carlson, 3154 Bremerton Pl., La Jolla, Calif.

San Francisco (7)—D. A. Dunn, Stanford Electronics Labs., Stanford Univ., Stanford, Calif.; P. D. Lacy, 324 Lakeview Way, Redwood City, Calif.

Schenectady (1)—R. P. Wellinger, 309 Riverside Ave., Scotia, N. Y.; B. J. Shinn, 2000 Baker Ave., Schenectady 9, N. Y.

Seattle (7)—D. K. Reynolds, Dept. of Elec. Engrg., Univ. of Washington, Seattle 5, Wash.; R. M. Lundberg, 9115 N.E. 21 St., Bellevue, Wash.

Shreveport (6)—D. L. Johnson, Louisiana Polytech. Inst., Elec. Engrg. Dept., Ruston, La.; R. M. Steere, 406 West Florida Ave., Ruston, La.

South Bend-Mishwaka (5)—C. H. Hoffman, 52663 Lynnewood Ave., South Bend, Ind.; D. L. Cunningham, 16269 Shamrock Dr. Mishawaka, Ind.

South Carolina (3)—P. A. McMasters, 5809 Moore St., N. Charleston, S. C.; H. L. Hunter, 49 Fort Dr., Rte. 6, Box 423, North Charleston, S. C.

Southern Alberta (8)—A. P. Davis, 47 Wildwood Dr., Calgary, Alberta, Canada; G. L. Sadler, 2520-32 Ave., S.W., Calgary, Alberta, Canada.

Syracuse (1)—R. N. Lothes, G.E. Co., DeWitt Engrg. Office, 3711 Erie Blvd., E., De Witt, N. Y.; R. E. Gildersleeve, 110 S. Burdick St., Fayetteville, N. Y.

Tokyo—I. Koga, 254 8-Chome, Kami-Meguro, Tokyo, Japan; F. Minozuma, 16 Ohara-Machi, Meguro-Ku, Tokyo, Japan.

Toledo (4)—R. N. Hanna, 1924 Glencairn Ave., Toledo 14, Ohio; H. K. Seike, 2920 Kendale Dr., Toledo 6, Ohio.

Toronto (8)—K. MacKenzie, McCurdy Radio Ind., Ltd., 22 Front St., W., Toronto 1, Ont., Canada; W. H. Anderson, 321 Shelbourne St., Apt. 110, Toronto 2, Ont., Canada.

Tucson (7)—E. L. Morrison, Jr., 4549 E. Eastland St., Tucson, Ariz.; W. Bastian, 7132 E. 31 St., Tucson, Ariz.

Tulsa (6)—H. B. Ferguson, 4530 E. 32 Place, Tulsa, Okla.; J. M. Bushnell, KVOO-TV, Box 1349, Tulsa, Okla.

Twin Cities (5)—J. Kahnke, 1541 Edgewater Ave., St. Paul 13, Minn.; C. G. Compton, 1011 Fairmount Ave., St. Paul 5, Minn.

Vancouver (8)—W. H. Thompson, 2958 West 28 Ave., Vancouver 8, B. C., Canada; D. H. J. Kay, 4539 Imperial St., Burnaby, B. C., Canada.

Virginia (3)—R. W. Morton, Box 96, Denbigh, Va.; J. B. Spratley, Ellerson, Va.

Washington (3)—D. C. Ports, Jansky & Bailey, 1339 Wisconsin Ave., N.W., Washington 7, D. C.; C. R. Busch, 2000 N. Vermont St., Arlington 7, Va.

Western Massachusetts (1)—J. J. Allen, 29 Sunnyside Dr., Dalton, Mass.; J. E. Mulford, Sprague Elec. Co., Marshall St., North Adams, Mass.

Western Michigan (4)—F. E. Castenholz, Police Headquarters, Jefferson & Walton Sta., Muskegon, Mich.; J. F. Giardina, 1528 Ball, N.E., R. 4, Grand Rapids 5, Mich.

Wichita (6)—M. E. Dunlap, 548 S. Lorraine Ave., Wichita 16, Kans.; N. J. Damaskos, 7803 East Indianapolis, Wichita 7, Kans.

Williamsport (4)—D. M. Jewart, 1400 Faxon Pkwy., Williamsport, Pa.; G. W. Deming, 1891 East 3rd Williamsport, Pa.

Winnipeg (8)—P. F. Windrick, 669 Oxford St., Winnipeg 9, Man., Canada; R. I. Punshon, Canadian Broadcasting Corp., 540 Portage Ave., Winnipeg, Man., Canada.

Subsections

Buenaventura (7)—T. A. Solferino, 533 East Guava St., Oxnard, Calif.; J. A. Frederick, 455 Corsicana Dr., Oxnard, Calif.

Burlington (5)—P. D. Keser, Box 123, Burlington, Iowa; C. D. Cherryholmes, 2072 Highland, Burlington, Iowa.

Catskill (2)—E. L. Johnson, 10 Kiersted Ave., Kingston, N. Y.; C. R. Eickhorn, Jr., 10 Park Circle, Mount Marion, N. Y.

East Bay (7)—A. J. Stripeika, 2759 Miranda Ave., Alamo, Calif.; J. T. Lavrischeff, 7029 Cutting Blvd., El Cerrito, Calif.

Eastern North Carolina (3)—W. J. Barclay, Dept. of Elec. Engrg., North Carolina State College, Raleigh, N. C.; W. J. Speed, 2718 E. Rothgeb Dr., Raleigh, N. C

Fairfield County (1)—J. M. Hollywood, Box 355, Greenwich, Conn.; R. Townsend, 60 Du Bois St., Darien, Conn.

Lancaster (3)—W. N Parker, 1493 Hollywood Dr., Lancaster, Pa.; J. Evans, 2109 Lyndell Dr. Lancaster, Pa.

Las Cruces-White Sands Proving Ground (6)—H. Coleman, Box 1238, Las Cruces, N. M.; Secretary to be advised.

Lehigh Valley (3)—H. A. Tooker, 2524 Fairview St., Allentown, Pa.; M. C. Waltz, Bell Telephone Labs., 555 Union Blvd., Allentown, Pa.

Memphis (3)—J. J. Freymuth, 3205 Guernsey Ave., Memphis 12, Tenn.; Brother I. John Haas, Christian Brothers College, Memphis 4, Tenn.

Merrimac Valley (1)—C. E. White, 16 Dale St., West Peabody, Mass.; D. Christiansen, 12 Hay St., Newbury, Mass.

Mid-Hudson (2)—W. D. Reiner, IBM Corp., Dept. 553, Bldg. 703, Poughkeepsie, N. Y.; B. Augusta, 53 Colburn Drive, Poughkeepsie, N. Y.

Monmouth (2)—J. A. Young, Jr., 34 Kemp Ave., Fairhaven, N. J.; O. E. DeLange, Bell Telephone Labs., Holmdel, N. J.

Nashville (3)—P. E. Dicker, 4208 Wallace Lane, Nashville 12, Tenn.; R. L. Hucaby, 945 Caldwell Lane, Nashville 4, Tenn.

New Hampshire (1)—R. Baer, 134 Mayflower Dr., Manchester, N. H.; F. J. Safford, 71 Concord St., Nashua, N. H.

Northern Vermont (1)—F. J. M. Sichel, 35 Henderson Terrace, Burlington, Vt.; W. C. Chase, WDEV, 9 Stowe St., Waterbury, Vt.

Orange Belt (7)—J. R. Mickelson, Convair, Zone 6-87, P. O. Box 1011, Pomona, Calif.; G. E. Kinzer, 2856 Ronald St., Riverside, Calif.

Panama City (3)—S. B. Marley, 1912 Calhoun Ave., Panama City, Fla.; R. C. Lowry, 2342 Pretty Bayou Dr., Panama City, Fla.

Pasadena (7)—J. W. Thatcher, 936 Winston Ave., San Marino, Calif.; R. L. Heacock, 2532 Hanning Ave., Altadena, Calif.

Pikes Peak (6)—A. O. Behnke, 1445 North Foote, Colorado Springs, Colo; Secretary to be advised.

Reading (3)—W. I. Huyett, 1020 Wyomissing Blvd., Wyomissing, Pa.; R. H. Lundberg, 3312 Harrison Ave., Reading, Pa.

Richland (7)—P. R. Kelly, 220 Delafield, Richland, Wash.; G. L. Erickson, 213 Armistead, Richland, Wash.

San Fernando Valley (7)—J. D. Wills, 6606 Lindley, Reseda, Calif.; C. Z. Becker, RCA, 8500 Balboa Ave., Van Nuys, Calif.

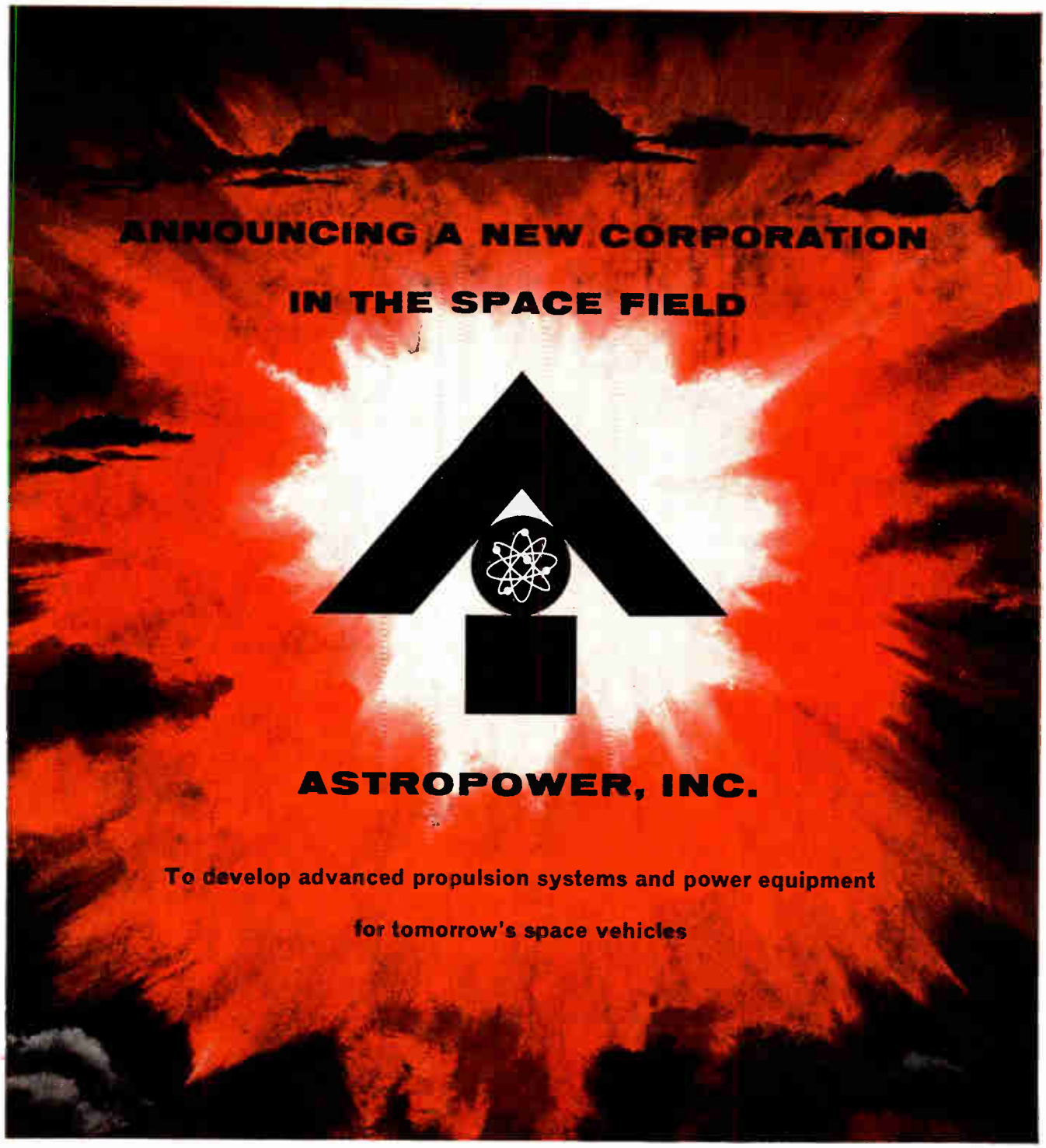
Santa Ana (7)—D. R. Proctor, 1601 East Chestnut Ave., Santa Ana, Calif.; J. C. Hathaway, Collins Radio Co., 3324 W. Delhi Rd., Santa Ana, Calif.

Santa Barbara (7)—S. D. Crane, 590 Barker Pass Rd., Santa Barbara, Calif.; D. L. Herr, 24 E. Pedregosa St., Santa Barbara, Calif.

South Western Ontario (8)—W. A. Ruse, Bell Telephone Co., 1149 Goyeau St., Windsor, Ont., Canada; G. L. Virtue, 619 Lounsborough Rd., Sandwich-South, Windsor, Ont., Canada.

Westchester County (2)—S. Sherr, 35 Byway, Hartsdale, N. Y.; S. K. Benjamin, 59 Cooper Dr., New Rochelle, N. Y.

Western North Carolina (3)—L. L. Caudle, Jr., Box 2536, 1901-25 N. Tryon St., Charlotte, N. C.; J. I. Barron, Southern Bell T&T Co., Box 240, Charlotte, N. C.



Astropower, Inc. has been formed as a subsidiary of Douglas Aircraft Company with Mr. Y. C. Lee, internationally noted propulsion expert, as president.

In offering its services for research and development of advanced space propulsion systems to system contractors and government agencies, Astropower will operate as an independent company. The proprietary interests of major systems and sub-systems contractors will be respected and protected by both Douglas and Astropower.

A balanced engineering and research program is now being formulated to advance the state of the art in—

- Ultra-high energy propulsion systems in the nuclear, chemical and electrical fields
- Solid state devices and energy conversion equipment

Mr. Lee is now staffing key positions in Astropower, Inc. and will welcome inquiries from qualified engineers and scientists having advanced degrees in the areas of nuclear physics, plasma physics, solid state physics, thermodynamics and high temperature materials.

Astropower's permanent scientific and engineering center will be located in one of Southern California's ideally situated research communities.

ASTROPOWER, INC.

Temporary headquarters: 3801 Lakewood Boulevard, Long Beach, California

NEWS New Products

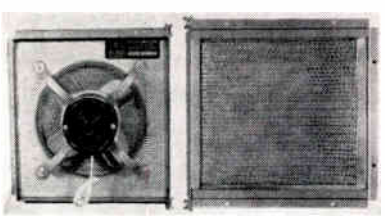
Super-Temp Expands R&D

American Super-Temperature Wires, Inc., Winooski, Vt., a subsidiary of **Haveg Industries, Inc.,** a supplier of Teflon and silicone rubber insulated wire and cable, has completed the expansion of its research and development department. The section now occupies almost 4000 square feet, virtually doubling the previous facilities. The new equipment is now in operation and not only permits the company to run all necessary qualification tests, but provides facilities to develop a larger product line.

Of particular interest to purchasers of high-temperature wire is the installation of a new corona tester and high voltage dielectric tester. The ratings of the equipment are as follows: 15,000 volts ac maximum corona and 30,000 volts ac maximum dielectric.

Panel-Mounted Fan

McLean Engineering Laboratories, P.O. Box 228, Princeton, N. J., has announced the production of a new panel-mounted fan to be installed on the outside of electronic racks. The fan is designed to pressurize the cabinet with air filtered through a permanent, washable-type filter.



Designated as Model 1PB65W, it is installed from outside the rack and uses a minimum of cabinet area. The filter is also accessible from the outside of rack and may be serviced without removing the fan mounting bolts. The fan has a shallow depth which makes it adaptable for use in densely packed racks.

Model 1PB65W moves 295 cfm, and is equipped with a ball bearing motor which meets Specifications CC-M-636A. The lubricant is a MIL-G-3278 having a temperature range of −62°C to +93°C. Shipment can be made from stock.

For specifications, prices and other information contact the firm.

Connector Catalog

Complete technical data on the Foamflex series of coaxial connectors manufactured by **Kings Electronics Co., Inc.,** 38 Marbledale Rd., Tuckahoe, N. Y., are contained in their new 8-page catalog just issued. These connectors are designed for use with Phelps Dodge Copper Products Corporation's Foamflex Cable.

Also featured in this 2-color bulletin are connectors which are specifically designed for applications involving Phelps Dodge's Spirafil and Styroflex Cables.

A copy of the Foamflex catalog may be secured by writing the manufacturer.

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your IRE affiliation.

Cardon Appointed By Servo Corp.

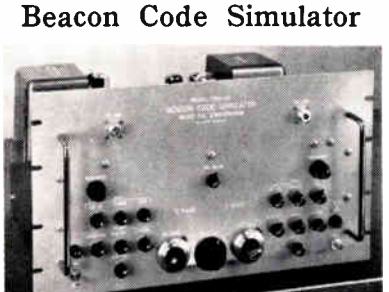
In line with the Government's latest trend toward total project supervision, with more direct interest being shown in sub-contracts as well as primes, **Servo Corporation of America,** Hicksville L. I., N. Y., named Jules Cardon manager of Government Sales.

In a simultaneous move Servo acted to integrate all its government contract and subcontract activities under the direction of the new unified marketing group to be headed by Cardon.

The organizational change merges the two distinct sales groups which formerly marketed Servo capabilities, facilities, and products to the government and prime defense contractors separately. In effect, the former Government Sales and Weapons and Sub-System Sales Divisions are now merged into a single Government Sales group.

The move also completes re-organization of Servo's sales department according to the company's over-all marketing plan, a Servo spokesman stated.

Beacon Code Simulator



Micro-Tel Corp., 2127 Maryland Ave., Baltimore 19, Md., announces the availability of Model PSG-10A Beacon Code Simulator. The instrument is a double-pulsed microwave signal source covering 2.7 to 2.9 kmc and 5.1 to 5.9 kmc. Pulse width can be adjusted from 0.3 to 10 μsec, pulse spacing from 0 to 100 μsec, and PRF from 10 to 2000 pps. An additional feature is that parallel sets of pulse controls can be used to pre-set all pulse parameters in either "C" or "S" band. 100 milliwatts of pulse or cw power is available in both bands through 40 db variable attenuators for sensitivity measurements. The entire instrument is housed in a 19×10½×15″ cabinet and will operate from 60 to 400 cps power source. Primary purpose of the instrument is to check sensitivity and pulse decoding circuitry of radar beacons. For further information, contact the firm.

Hines Appointed by Microwave Associates

Microwave Associates, Inc., Burlington, Mass., announces the appointment of Marion E. Hines to the newly created position of Senior Scientist. Hines will coordinate the company's extensive research activities in solid state circuits and will initiate two new programs which will lead to the company's entry into microwave oscillators and microwave amplifier-down converters both using Esaki (tunnel) diode techniques.

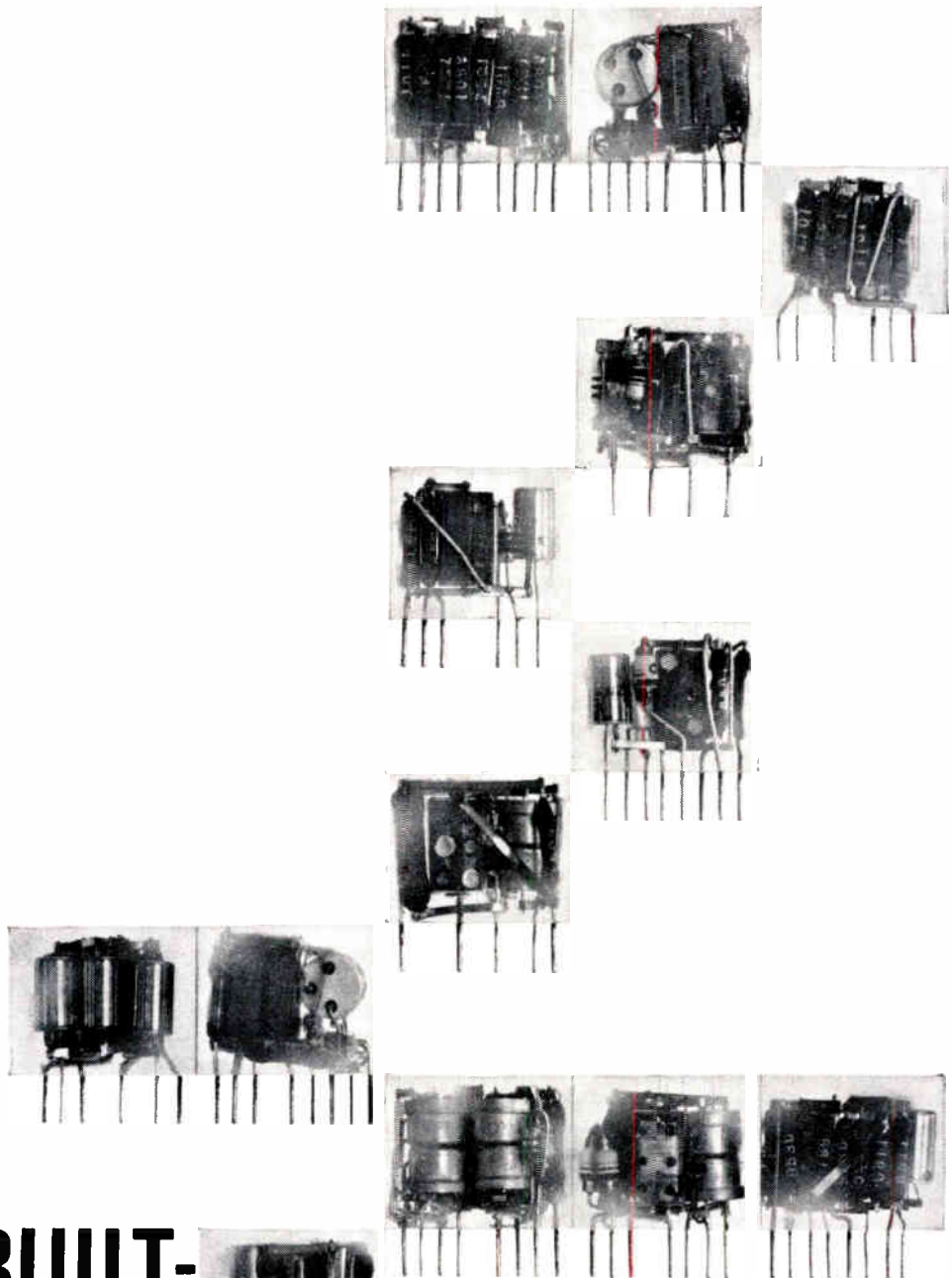
Hines was previously associated with the Bell Telephone Laboratories, Inc., at their New York City, Allentown, Pa., and Murray Hill, N. J. laboratories. He has been active in the development of microwave electron tubes, development of telephone transmission systems and in research on solid state electron devices. His most recent work has been involved with research on Esaki (tunnel) diodes for application as microwave oscillators and amplifiers.

At the Bell Laboratories, Hines was an instructor in electron tubes for the Communications Development Training program and has recently been a visiting lecturer at the University of Pennsylvania.

Hines is a graduate of the California Institute of Technology where he obtained a Bachelor's degree in 1940 and a Master's degree in Electronic Engineering in 1946. He served as a weather officer in the Air Force during World War II.

He holds numerous patents in the fields of electron tubes, electronic circuits, and semiconductor devices.

(Continued on page 157A)



BUILT-TO-ORDER COMPUTERS

...with off-the-shelf components

Delco Radio can design, develop and deliver digital computers with the speed you need, for airborne guidance and control as well as a wide variety of other special applications. ■ With off-the-shelf Delco transistorized digital circuits, we have, for example, built a computer for a military application in less than three months. ■ These miniature modules contain standard components. They satisfy all MIL-E-5272D (ASG) requirements, which assures extremely rugged, reliable computers. Continuing life tests on these computer circuits now exceed four and one-half million transistor hours *without a failure*. And where space is no problem, you can have these same, reliable digital circuits packaged on plug-in circuit cards. ■ Delco Radio has six sections of highly experienced people with the necessary capabilities to produce complete computer systems: Application Analysis, Systems, Logic, Memory, Circuit Design and Advanced Development. May we review your requirements? Just contact our Sales Department. ■ *Physicists and Electronics Engineers: Join Delco Radio's search for new and better products through Solid State Physics.*

PIONEERING ELECTRONIC PRODUCTS THROUGH SOLID STATE PHYSICS

DELCO RADIO

Division of General Motors • Kokomo, Indiana

Industrial Engineering Notes*

Association Activities

Electronic component sales will rise from their present level of $3 billion a year to $5 billion within the next 10 years, L. Berkely Davis, President of the Electronic Industries Association and Vice President of the General Electric Co., predicted in a speech before the Washington Society of Financial Analysts.

Mr. Davis warned, however, that any company which intends to compete seriously in the component business must be able to invest "substantially" in research and possess the technological capabilities for volume production at mass-production prices.

"Despite the aura of glamour and the still-glowing prospects for a continued rapid growth, electronic components right now is a tough business, and it is rapidly getting tougher," Mr. Davis said.

Developments in components provide the key to growth in all electronics markets, Mr. Davis said. As examples of how new components have extended the range and capability of electronics, he called attention to the introduction of solid-state devices in one of the new model automobiles, the dependence of dial telephones upon new components, and the use of electronic control circuits in the baking and steel industries.

Since components are basic to all kinds of electronic equipment, growth in this segment of the electronics industry will follow expansion patterns for the industry as a whole, Mr. Davis observed. In 1970, he said, the military market will still be the largest, "but industrial sales will be challenging for the lead and the consumer market will have grown significantly, largely through the introduction of a host of exciting and entirely new kinds of equipment."

Governmental and Legislative

It may take up to six months for the Federal Communications Commission to reach a decision on whether to permit the Hartford Phonovision Co. to run tests of subscription television in Hartford, Conn., it was reported.

A lengthy study was indicated by the massive collection of testimony recorded during the Commission's five days of hearings on pay-TV.

A delay on a decision past January 3, when the 87th Congress convenes, would permit Congressional intervention in the pay-TV action. Rep. Emanual Celler (D., N. Y.) stated in a letter sent to the FCC during the hearings that "many members of Congress" are opposed to subscription TV. He urged that the Commission delay authorization until Congress is back in session.

Meanwhile, the National Association of Broadcasters joined the Connecticut Committee Against Pay-TV in opposing the proposed tests. In testimony given during the closing sessions of the hearings, Charles H. Tower, NAB Vice President for Television, said the broadcasting would be in direct competition with other commercial TV stations.

Mr. Tower was not permitted to read an NAB statement after protests by the Phonovision attorney. He appeared as a public witness and his testimony was elicited through questioning and cross-examination.

A system which utilized an electronic reader and printer for one-second transmission of letters from city to city was demonstrated by the Post Office Department in Washington.

The new Speed Mail system sped letters from Washington to Battle Creek, Mich., and Chicago at a rate of 400 times faster than facilities used by the major press associations for transmission of photographs. The system transmits by microwave and uses facsimile reproduction equipment to convert the impulses into the printed letters. The letters are read only by the sender and the recipient.

The "brain" of the system, the Post Office Department said, is a complex electronic scanner which operates by sweeping a tiny spot of light across the face of a cathode ray tube 360 times a second. The spot is focused on the letter being transmitted as it moves along a conveyor belt. The light is picked up by a photomultiplier tube, which puts out a voltage proportional to the reflections from light and dark areas of the paper. The varied impulses are shaped into levels denoting either black or white and these are transmitted to the printer.

A cathode-ray tube in the printer at the receiving end of the system is synchronized with the scanner. Since the spot of light emitted by this tube is modulated by the voltage output from the photomultiplier, the varying light source is used to produce the transmitted image on a light-sensitive, electrostatically charged surface of a rotating xerographic drum. A powder process transfers the printed material to the paper.

Postal engineers have recommended a nation-wide network of Speed Mail stations in 71 large post offices located to provide links between major population centers.

Prime contractor for the system was the International Telephone and Telegraph Corp. Other contractors were the Stromberg-Carlson Division of General Dynam-

(Continued on page 38A)

* The data on which these NOTES are based were selected by permission from *Weekly Report* issues of October 31 and November 7, 1960, published by the Electronic Industries Association, whose helpfulness is gratefully acknowledged.

NEW!

DIRECT READING FREQUENCY METER

a full octave and beyond

3.95 to 11.0 KMc

DELIVERY FROM STOCK

Model No. N414A **Price: $495.00**

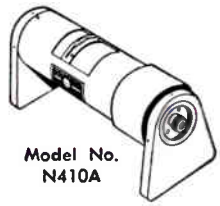
- Direct reading from 3.95 to 11.0 KMc
- Covers a full octave and beyond
- Reaction type with 0.1% absolute accuracy
- Non-contacting choke for long life and high Q
- Standard Type N Connectors for universal utilization

Meet the newest member of the FXR "family" of direct reading frequency meters. This coaxial type, Model No. N414A, has a range from 3.95 KMc to 11.0 KMc and by use of FXR Series 601 coax to waveguide adapters converts to waveguide set-ups. The unit covers "a full octave and beyond" with an absolute accuracy of 0.1% throughout its range. It is a perfect companion for the FXR Models No. C772 and X772 signal sources.

This newest direct reading frequency meter augments FXR's existing line, recognized as the largest in the industry. Direct reading, reaction type units are available for use up to 39.5 KMc while micrometer types extend FXR's coverage up to 220 KMc.

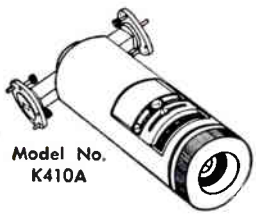
Write or call now for data sheets on Model No. N414A and other units in the integrated FXR family of precision frequency meters.

FXR "FAMILY" OF DIRECT READING REACTION TYPE FREQUENCY METERS



Model No. N410A

Model No. X410B



Model No. K410A

Model No. C402A

Model No.	Frequency Range (KMc)	Absolute Accuracy (%)	Approx. Q	Waveguide Type RG-( )/U	Flange Type UG-( )/U	Price (F.O.B. Woodside)
COAXIAL TYPES						
N410A	1.00- 4.00	0.10	3000	(⅜" Coax Type N)		$495.00
N414A	3.95-11.0	0.10	500 to 1500	(⅜" Coax Type N)		495.00
WAVEGUIDE TYPES						
*H410B	3.95- 5.85	0.08	8000	49	149A	250.00
*C410B	5.85- 8.20	0.08	8000	50	344	180.00
*W410B	7.05-10.00	0.08	8000	51	51	165.00
*X410B	8.20-12.40	0.08	8000	52	39	150.00
Y410A	12.40-18.00	0.10	4500	91	419	210.00
K410A	18.00-26.50	0.10	4000	53	425	230.00
U410A	26.50-39.50	0.10	3000	96	381	250.00
C402A	5.85- 8.20	0.03	8000	50	344	1275.00
X402A	8.20-12.40	0.03	8000	52	39	1275.00

* With transmission coupling probe.

DELIVERY FROM STOCK

FXR M.M. TYPES (Micrometer Reading)

Model No.	Frequency Range KMc	Price (F.O.B. Woodside)
Q410X	33-50	$325.00
M410X	50-75	300.00
E410X	60-90	500.00
F412A	90-140	750.00
G412A	140-220	750.00

DELIVERY FROM STOCK

FXR, Inc.

Design • Development • Manufacture

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PRECISION MICROWAVE EQUIPMENT • HIGH-POWER PULSE MODULATORS • HIGH-VOLTAGE POWER SUPPLIES • ELECTRONIC TEST EQUIPMENT

Industrial Engineering Notes

(Continued from page 36A)

ics Corp., Bell and Howell Co., Haloid-Xerox, Inc., Pitney-Bowes Co., and Baum Folder Co.

A new U. S. Department of Commerce publication, Directory of National Associations of Businessmen: 1960, containing data on over 2,000 national associations, was placed on sale by the Government Printing Office, Washington 25, D. C. Price 50 cents a copy.

By the year 1965, the number of television sets in Russia will have increased from the now more than 3 million to over 15 million, there will be 160 TV stations as compared to about 70 now, and the relay system will be greatly expanded, according to a Russian writer in the Soviet magazine Literature and Life.

The article, written by a Professor P. Shmakov in December 1959, has been translated by a U. S. Government agency and printed for public sale by the Office of Technical Services, U. S. Department of Commerce. It also forecasts an expansion of the network of relay posts and other facilities for broader coverage of the Russian land area with TV broadcasts.

Industry Marketing Data

The Japanese Ministry of International Trade and Industry (MITI) has revised upward its recent estimates of Japanese electronics output during the five-year period 1960–1964, the Electronics Division, Business and Defense Services Administration, U. S. Department of Commerce reported.

MITI's revised Five-Year Plan shows a projected estimate of overall production for the year 1964 at a level 82 per cent above actual production in 1959; a tentative estimate announced by MITI in May of this year called for an increase of 32 per cent. Significant upward revisions were made in estimated production of industrial electronic equipment, tape recorders and other acoustic apparatus, receiving tubes and transistors.

Projected estimates show a decrease in output of monochrome television receivers and a very sharp increase in color television receivers. It is expected that emphasis will be placed on television receivers using transistors.

The plan assumes an annual rise in transistor radio exports amounting to 27 per cent from 1960 to 1961, 10 per cent in 1961 and 1962, and 5 per cent in 1963 and 1964.

Japanese electronic industries continued to expand their output during the first half of 1960, with total production amounting to $565 million—40 per cent higher than during the first half of 1959—the Electronics Division of the Commerce Department's Business and Defense Services Administration reported.

Production of consumer items, which still accounts for the major portion of total Japanese electronics output, increased

(Continued on page 42A)

A SUMMIT
in storage tube development

EXCLUSIVE COAXIAL GUN DESIGN A NEW HIGH POINT IN ITT IATRON* PROGRAM

Latest additions to the ever-increasing line of ITT Iatron storage tubes are several new models in which both the writing and the flooding guns are symmetrically disposed about the axis of the cathode-ray display tube. This imaginative solution to a difficult packaging problem in radar indicator design eliminates at the same time all possibility of trapezoidal distortion.

Added to the full line of ITT Iatrons with the more conventional off-axis writing gun arrangement, the new coaxial gun models make it possible to specify an ITT Iatron for virtually any storage tube application—in any diameter from 2½ to 7 inches, to satisfy any requirement with regard to weight, size and desired brilliance under high ambient light conditions.

New and further improved ITT Iatrons, in an even wider range of types, are scheduled for release in the near future. ITT's unlimited access to world-wide research, development and production facilities turns a new design concept into a production model at record pace—in Iatrons as well as other electron tube types.

Write for information on the complete line of ITT Iatrons. Application assistance is available for your specific requirements.

ITT IATRON STORAGE TUBES

TYPE	DIAMETER (in.)	SPECIAL FEATURES	FOCUS†	DEFLECTION†
7172	2½	Coaxial gun	ES	ES
FW-211	2½	Coaxial gun	ES	ES
7173	4	—	EM	EM
7174	4	—	EM	EM
FW-227	4	2 writing guns	ES	ES
7423	5	—	ES	ES
FW-204	5	Coaxial gun	EM	EM
D-3001	5	—	ES	ES
FW-212	5	Coaxial gun	EM	ES
FW-217	5	Coaxial gun	ES	EM
FW-208	7	—	EM	EM

†EM = Electromagnetic ES = Electrostatic

*IATRON IS A TRADEMARK OF INTERNATIONAL TELEPHONE AND TELEGRAPH CORPORATION

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OPTIMIZE ANY MODEL at 100 CYCLES PER-SECOND

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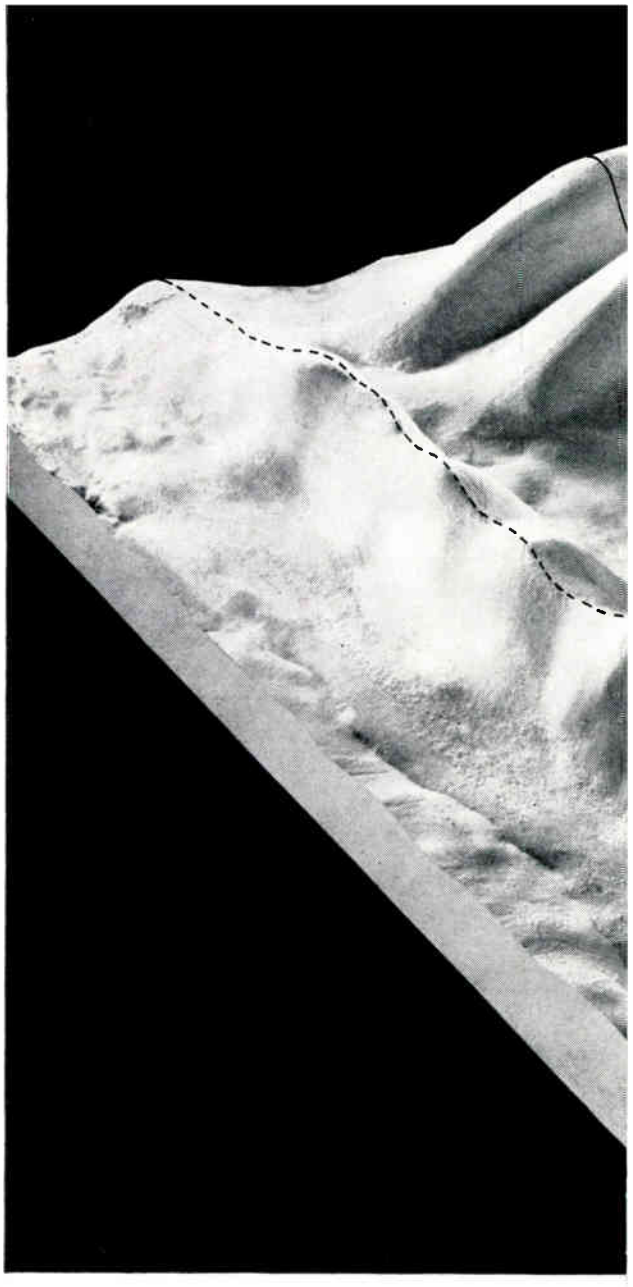

Whether your problems are dynamic or static, covering costs, design, or production control in: Operations Research, Chemical Kinetics, Aerodynamics, Structures, Astrophysics, or Hydrodynamics, DYSTAC computers can solve them faster, more accurately, and more economically than any other computer.

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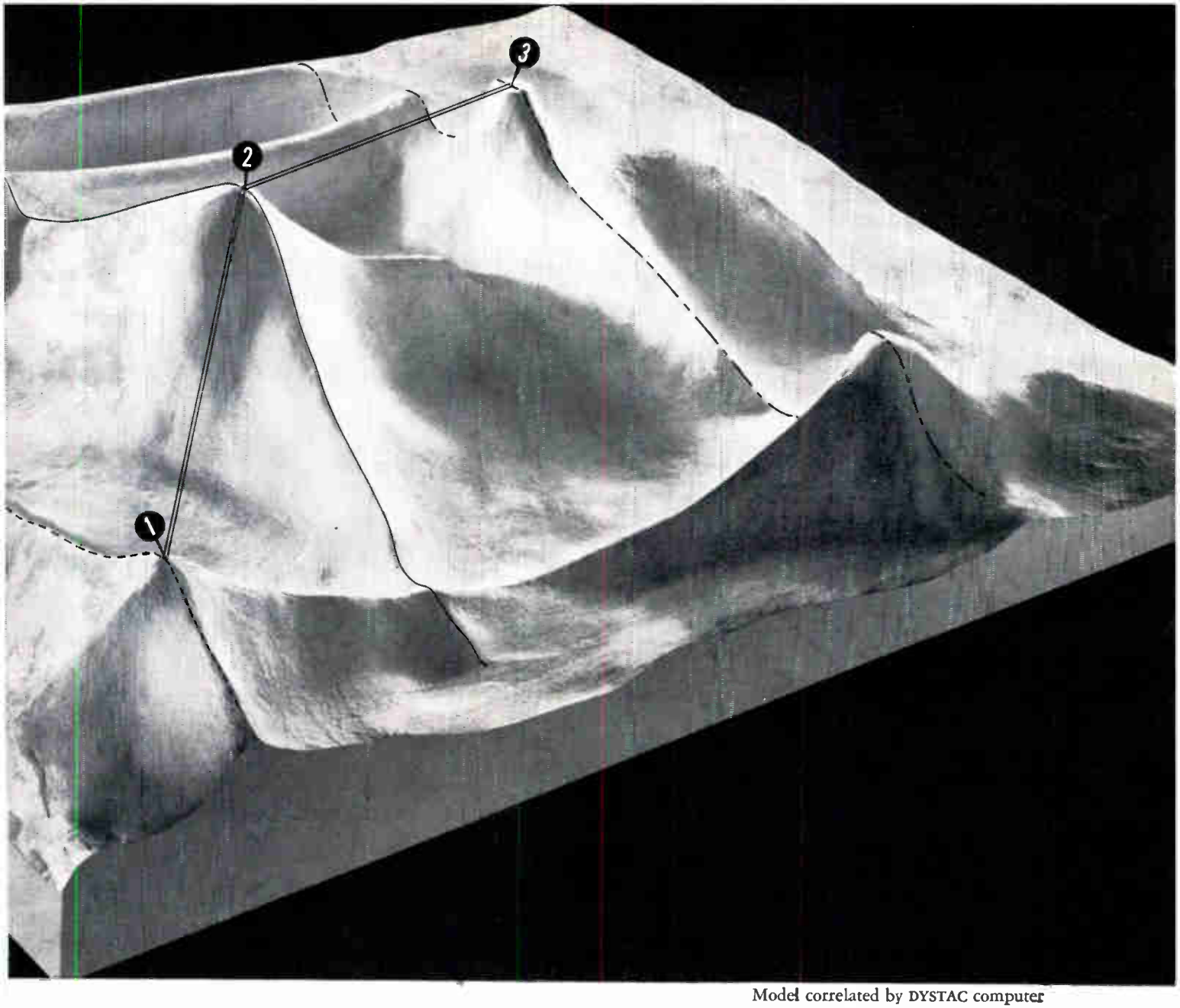
DYSTAC provides unique time-sharing of computer components and high speed reiterations. These features make possible economic and rapid solution of complex problems that have required too many computer components, or too long a solution time, to be considered practical for either digital or analog machines. And you can expand the number of operational amplifiers by a flick of a switch which converts the precision Dynamic Memory units into Fixed and Summing Integrators.

$\left(\frac{\delta a}{\delta t}\right)$ – – – – – –	This curve describes the design parameters for the entire process, with the maximum design factor occurring at point (1).
$\left(\frac{\delta b}{\delta t}\right)$ ———	This curve describes the profitability of the process. Note peak (2), where maximum profitability occurs.
$\left(\frac{\delta c}{\delta t}\right)$ – — – — –	This curve shows the product quality variation. Maximum quality plateaus at point (3).
❶ ❷ ❸ ———	Optimization for the entire process is achieved by operating along points (1), (2), (3).



Model correlated by DYSTAC computer

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The problem of optimizing feed stocks and operating conditions in chemical kinetics problems has always defied continuous automatic solution. With any computer, other than DYSTAC, solutions require invalid oversimplifications. DYSTAC computers solve these problems by least mean square procedures at *high speed* and with a *minimum of components*. Accuracies are held to ±0.05%. Send for complete 26-page report entitled *"Correlation and Optimization of Chemical Kinetics Models"*.

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Industrial Engineering Notes

(Continued from page 38A)

from $224 million in the first half of 1959 to $320 million in the first half of 1960—an increase of 43 per cent. Production of television receivers during the first half of this year was valued at $196 million, 36 per cent higher than the first half of 1959; production of radio receivers with three or more transistors, valued at $80 million, was up 80 per cent; radio-phonographs, valued at $10 million, up 139 per cent.

Production of receiving tubes during January–June of this year increased by 63 per cent over the same period last year and transistors showed a gain of 48 per cent.

Total value of Japanese electronics production during the second quarter 1960 increased only slightly—$1 million—over that of the first quarter.

The U. S. Embassy in Tokyo reports that expansion in Japan's production of electronic products during the first half of 1960 can be attributed in part to the increase in exports but more basically to the high level of investments in Japanese industries and the continued rise in consumption levels of the Japanese people. Within the electronic industries, also, there was a significant increase in the number of technological agreements to improve production processes. The Japanese Ministry of International Trade and Industry

(Continued on page 44A)

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Type 9001-03 Size 9 28VDC permanent magnet timer motor or motor tach

- Withstands 8000 G axial shock; 500 G transverse shock.
- Up to 500 oz. in. peak load can be handled.
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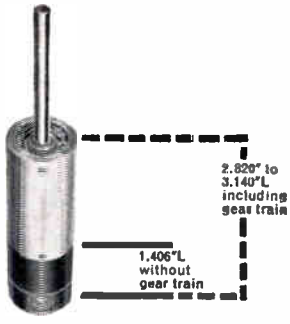
- 1.406"L without gear train; 2.820" to 3.140"L including gear train.
- 6:1 to 46,656:1 gear ratios available.

GEAR RATIO	OUTPUT RPM	LOAD	AMPS AT 25°C	UNIT LENGTH	OSTER TYPE NO.
46,656 to 1	0.25	100 oz. in.	0.075 max.	3.140	E149
4536 to 1	2.68	100 oz. in.	0.100 max.	2.980	E169
756 to 1	12	100 oz. in.	0.175 max.	2.820	E170
7776 to 1	1.5	100 oz. in.	0.090 max.	2.980	E171
9168 to 1	1.25	100 oz. in.	0.085 max.	3.140	E179
4056 to 1	2.75	100 oz. in.	0.100 max.	2.980	E215
2923 to 1	4.00	100 oz. in.	0.120 max.	2.980	9001-05
393.7 to 1	33	32 oz. in.	0.200 max.	2.725	9001-02*

Max. shaft dia. .263"; .250" on Type 9001-02. *Not a hi-shock unit. Output 27.5VDC.



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Engineers For Advanced Projects: Interesting varied work on designing transistor circuits and servo mechanisms. Contact Mr. Dallas Nielsen, Personnel Manager, in confidence.

Industrial Engineering Notes

(Continued from page 42A)

(MITI) estimates that expenditures for research in the electronic industries more than doubled between 1957 and 1959.

The relatively favorable production and export conditions in the electronic industries prompted MITI to revise sharply upward its estimates of Japan's electronic equipment production during the next five years.

Professional Group Meetings

Aeronautical and Navigational Electronics

Boston—September 27

"The Ground Stations and Satellite Systems of Project Transit," Dr. G. C. Weiffenbach, APL Johns Hopkins University, Silver Spring, Md.

Metropolitan New York—April 14

"Project Transit, A Navigation Satellite," Cmdr. R. F. Freitag, U. S. Navy.

Metropolitan New York—June 9

"Field Trip—Newark Airport Control Tower and IFR Room," Various FAA Personnel.

Antennas and Propagation

Boston—October 26

"A Different Approach to the Analysis of Antenna Arrays," J. R. Allen, MIT Lincoln Lab.

"Transoceanic Radio Ducts," R. W. Corkum, Air Force Cambridge Research Center.

Chicago—October 14

"A Survey of Frequency Independent Antennas," R. L. Carrel, P. E. Mayes, and J. D. Dyson, University of Illinois.

San Francisco—October 12

"Meteorological Factors in the Refraction of Microwave Energy," R. Nagle, Stanford Research Institute.

Antennas and Propagation Microwave Theory and Techniques

Orange Belt—October 12

"Recent Developments in the Parametric Amplifier," A. Uhlir, Microwave Associates.

"Theory and Construction of a Microwave Coupled Cavity Traveling Wave Parametric Amplifier," K. Grabowski.

(Continued on page 50A)

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The foreshortened radiator employs a bifilar helical element which is encased in Fiberglass for strength, durability and corrosion resistance. One helix is grounded, providing a static drain path. The other is fed. Ground rods employ single helix conductors which also are embedded in Fiberglass. Size reduction is shown by comparing the 57 inch radiator of Type 902 with 101 inches of a conventional antenna at 30 mc. Ground rods are also shortened by a proportionate amount.

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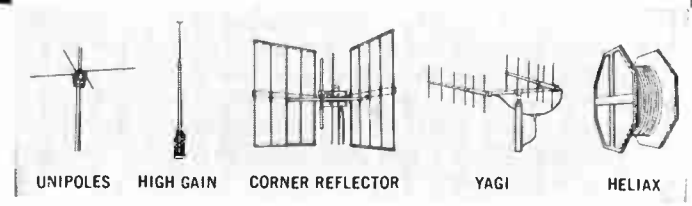
Economically priced ANDREW Type 902 is the best performing, corrosion resistant high wind load antenna on the market.

Write or call your ANDREW sales engineer for complete information or request Bulletin 8467.

*TRADEMARK



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28 Fields of Special Interest-

The 28 Professional Groups are listed below, together with a brief definition of each, the name of

Aeronautical and Navigational Electronics

Annual fee: $2.

The application of electronics to operation and traffic control of aircraft and to navigation of all craft.

Mr. William P. McNally, Chairman, 35 Laurel St., Floral Park, L.I., N.Y.

36 Transactions, *6, & *9, and Vol. 2, No. 1-3; Vol. 3, No. 2; Vol. 4, No. 1, 2, 3; Vol. 5, No. 2, 3, 4; Vol. 6, No. 1, 3, 4; Vol. 7, No. 1, 2.

Antennas and Propagation

Annual fee: $4.

Technical advances in antennas and wave propagation theory and the utilization of techniques or products of this field.

Prof. Edward C. Jordan, Chairman, Electrical Engineering Dept., University of Illinois, Urbana, Ill.

32 Transactions, *Vol. AP-2, No. 2; AP-4, No. 4; AP-5, No. 1-4; AP-6, No. 1, 2, 3, 4; AP-7, No. 1, 2, 3, 4; AP-8, No. 1, 2, 3, 4, 5.

Audio

Annual fee: $2.

Technology of communication at audio frequencies and of the audio portion of radio frequency systems, including acoustic terminations, recording and reproduction.

Mr. H-S. Knowles, Chairman, Knowles Electronics, 9400 Belmont Ave., Franklin Park, Ill.

54 Transactions, *Vol. AU-1, No. 6; *Vol. AU-2, No. 4; Vol. AU-3, No. 1, 3, 5; Vol. AU-4, No. 1, 5-6; Vol. AU-5, No. 1, 2, 3, 4, 5, 6; AU-6, No. 1, 2, 3, 4, 5, 6; AU-7, No. 1, 2, 3, 4, 5, 6; AU-8, No. 1, 2, 3, 4.

Automatic Control

Annual fee: $3.

The theory and application of automatic control techniques including feedback control systems.

Mr. John M. Salzer, Chairman, 909 Berkeley St., Santa Monica, Calif.

10 Transactions, PGAC-3-4-5-6, AC-4, No. 1, 2, 3; AC-5, No. 1, 2, 3.

Bio-Medical Electronics

Annual fee: $3.

The use of electronic theory and techniques in problems of medicine and biology.

Dr. Herman P. Schwan, Chairman, University of Pennsylvania, School of Elec. Engrg., Philadelphia 4, Pa.

17 Transactions, 8, 9, 11, 12; ME-6, No. 1, 2, 3, 4; ME-7, No. 2, 3.

Broadcast & Television Receivers

Annual fee: $4.

The design and manufacture of broadcast and television receivers and components and activities related thereto.

Mr. Robert R. Thalner, Chairman, Sylvania Home Electronics, Batavia, N.Y.

26 Transactions, *7, 8; BTR-1, No. 1-3, BTR-2, No. 1-2-3; BTR-3, No. 1-2; BTR-4, No. 2, 3-4; BTR-5, No. 1, 2, 3; BTR-6, No. 1, 2.

Broadcasting

Annual fee: $2.

Broadcast transmission systems engineering, including the design and utilization of broadcast equipment.

Mr. George E. Hagerty, Chairman, Westinghouse, 122 E. 42nd St., New York 17, N.Y.

17 Transactions, No. 2, 6, 7, 10, 11, 12, 13, 14; BC-6, No. 1, 2, 3.

Circuit Theory

Annual fee: $3.

Design and theory of operation of circuits for use in radio and electronic equipment.

Mr. Sidney Darlington, Chairman, Bell Tel. Labs., Murray Hill, N.J.

27 Transactions, CT-3, No. 2; CT-4, No. 3-4; CT-5, No. 1, 2, 3, 4; CT-6, No. 1, 2, 3, 4; CT-7, No. 1, 2.

Communications Systems

Annual fee: $2.

Radio and wire telephone, telegraph and facsimile in marine, aeronautical, radio-relay, coaxial cable and fixed station services.

Capt. C. L. Engleman, Chairman, Engleman & Co., Inc., 2480 16th St., N.W., Washington 9, D.C.

18 Transactions, CS-5, No. 2, 3; CS-6, No. 1, 2; CS-7, No. 1, 3, 4; CS-8, No. 1, 2.

Component Parts

Annual fee: $3.

The characteristics, limitation, applications, development, performance and reliability of component parts.

Mr. Floyd E. Wenger, Chairman, Headquarters ARDC, Andrews AFB, Washington 25, D.C.

20 Transactions, CP-4, No. 1, 2, 3-4; CP-5, No. 1, 2, 3, 4; CP-6, No. 1, 2, 3, 4; CP-7, No. 1, 2.

Education

Annual fee: $3.

To foster improved relations between the electronic and affiliated industries and schools, colleges, and universities.

Dr. John G. Truxal, Chairman, Dept. of EE, PIB, Brooklyn, N.Y.

11 Transactions, Vol. E-1, No. 3, 4; E-2, No. 1, 2, 3, 4; E-3, No. 1, 2, 3.

Electron Devices

Annual fee: $3.

Electron devices, including particularly electron tubes and solid state devices.

Mr. A. Kyle Wing, Jr., Chairman, Fed. Telecommunication Labs., 500 Washington Ave., Nutley 10, N.J.

29 Transactions, *Vol. ED-1, No. 3-4; ED-3, No. 2-4; ED-4, No. 2-3, 4; ED-5, No. 2, 3, 4; ED-6, No. 1, 3; ED-7, No. 1, 2, 3.

Electronic Computers

Annual fee: $4.

Design and operation of electronic computers.

Dr. A. A. Cohen, Chairman, Remington-Rand Univac, St. Paul 16, Minn.

35 Transactions, EC-6, No. 2, 3; EC-7, No. 1, 2, 3, 4; EC-8, No. 1, 2, 3, 4; EC-9, No. 1, 2, 3.

Engineering Management

Annual fee: $3.

Engineering management and administration as applied to technical, industrial and educational activities in the field of electronics.

Dr. Henry M. O'Bryan, General Tel. & Elec. Lab., 730 3rd Ave., New York 17, N.Y.

18 Transactions, EM-3, No. 2, 3; EM-4, No. 1, 3, 4; EM-5, No. 1-4; EM-6, No. 1, 2, 3; EM-7, No. 1, 2.

Engineering Writing and Speech

Annual fee: $2.

The promotion, study, development, and improvement of the techniques of preparation, organization, processing, editing, and delivery of any form of information in the electronic-engineering and related fields by and to individuals and groups by means of direct or derived methods of communication.

John M. Kinn, Jr., Chairman, IBM Journal, 545 Madison Ave., New York, N.Y.

7 Transactions, Vol. EWS-1, No. 2, EWS-2, No. 1, 2, 3; EWS-3, No. 1, 2.

THE INSTITUTE OF RADIO

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the group chairman, and publications to date.

*** Indicates publications still available**

Human Factors in Electronics

Annual fee: $2.

Development and application of human factors and knowledge germane to the design of electronic equipment.

Mr. Robert R. Riesz, Chairman, Bell Tel. Labs, Murray Hill, N.J.

1 Transaction, HFE-1, No. 1.

Industrial Electronics

Annual fee: $3.

Electronics pertaining to control, treatment and measurement, specifically, in industrial processes.

Mr. J. E. Eiselein, Chairman, RCA Victor Div., Camden, N.J.

13 Transactions, *PGIE 1, 3, 5, 6, 7, 8, 9, 10, 11; IE-7, No. 1, 2.

Information Theory

Annual fee: $4.

The theoretical and experimental aspects of information transmission, processing and utilization.

Mr. Paul E. Green, Jr., Chairman, 14 Bradford Rd., Weston 93, Mass.

22 Transactions, PGIT-4, IT-1, No. 3; IT-2, No. 3; IT-3, No. 1, 2, 3, 4; IT-4, No. 1, 2, 3, 4; IT-5, No. 1, 2, 3, 4; IT-6, No. 1, 2, 3.

Instrumentation

Annual fee: $2.

Measurements and instrumentation utilizing electronic techniques.

Mr. C. W. Little, Jr., Chairman, C-Stellerator Assoc., Princeton, N.J.

17 Transactions, PGI-4, Vol. 1-6, No. 2, 3, 4; Vol 1-7, No. 1, 2; Vol. 1-8, No. 1, 2; Vol. 1-9, No. 1.

Microwave Theory and Techniques

Annual fee: $3.

Microwave theory, microwave circuitry and techniques, microwave measurements and the generation and amplification of microwaves.

Dr. Kiyo Tomiyasu, Chairman, General Electric Gen. Eng. Lab., Schenectady, N.Y.

31 Transactions, MTT-4, No. 3; MTT-5, No. 3, 4; MTT-6, No. 1, 2, 3, 4; MTT-7, No. 2, 3, 4; MTT-8, No. 1, 2, 3, 4.

Military Electronics

Annual fee: $2.

The electronics sciences, systems, activities and services germane to the requirements of the military. Aids other Professional Groups in liaison with the military.

Dr. Edward G. Witting, Chairman, 3700 N. Albemarle St., Arlington 7, Va.

9 Transactions, MIL-1, No. 1; MIL-2, No. 1; MIL-3, No. 2, 3, 4; MIL-4, No. 2-3.

Nuclear Science

Annual fee: $3.

Application of electronic techniques and devices to the nuclear field.

Mr. Louis Costrell, Chairman, 10614 Cavalier Dr., Silver Spring, Md.

17 Transactions, NS-1, No. 1; NS-4, No. 2; NS-5, No. 1, 2, 3; NS-6, No. 1, 2, 3, 4; NS-7, No. 1, 2-3.

Product Engineering & Production

Annual fee: $2.

New advances and materials applications for the improvement of production techniques, including automation techniques.

Mr. W. D. Novak, Chairman, 325 Douglas Road, Chappaqua, N.Y.

6 Transactions, No. 2-3, 4, 5, 6.

Radio Frequency Interference

Annual fee: $2.

Origin, effect, control and measurement of radio frequency interference.

Professor Ralph M. Showers, Chairman, Moore School of Elec. Eng., 200 S. 33rd St., Philadelphia 4, Pa.

2 Transactions, RFI-1, No. 1, RFI-2, No. 1.

Reliability and Quality Control

Annual fee: $3.

Techniques of determining and controlling the quality of electronic parts and equipment during their manufacture.

Mr. P. K. McElroy, Chairman, General Radio Co., West Concord, Mass.

18 Transactions, *3, 5, 10, 11, 12, 13, 14, 15; RQC-9, No. 1, 2.

Space Electronics and Telemetry

Annual fee: $2.

The control of devices and the measurement and recording of data from a remote point by radio.

Mr. Robert V. Werner, Chairman, 5575 Kearney Road, San Diego 10, Calif.

15 Transactions, TRC-1, No. 2-3; TRC-2, No. 1; TRC-3, No. 2, 3; TRC-4, No. 1; SET-5, No. 1, 2, 3, 4; SET-6, No. 1, 2.

Ultrasonics Engineering

Annual fee: $2.

Ultrasonic measurements and communications, including underwater sound, ultrasonic delay lines, and various chemical and industrial ultrasonic devices.

Mr. David L. Arenberg, Chairman, Arenberg Ultrasonic Lab., Inc., 94 Green St., Jamaica Plains, Mass.

9 Transactions, PGUE, 5, 6, 7; UE-7, No. 1, 2.

Vehicular Communications

Annual fee: $2.

Communications problems in the field of land and mobile radio services, such as public safety, public utilities, railroads, commercial and transportation, etc.

Mr. Richard P. Gifford, Chairman, 2719 Hurdle Hill Rd., Lynchburg, Va.

15 Transactions, 5, 8, 9, 10, 11, 12, 13; Vol. VC-9, No. 1, 2.

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Professional Group Meetings

(Continued from page 44A)

Audio

San Francisco—October 4

"What's New at Ampex," G. Behklau, C. Wilkins, J. Bennett, Ampex Professional Products Co.

Washington, D. C.—September 12

"Electrical Methods of Tone Generation and Control," R. White, Kitt Music Company.

Washington, D. C.—October 18

"Sound in the Theater," H. Burris-Meyer.

Automatic Control

Los Angeles—October 11

"Introduction to Space Guidance," J. M. Slater, Autonetics.

Bio-Medical Electronics

Boston—October 18

"Instrumentation for the Study of the Physiology of Whales and Porpoises," Dr. J. W. Kanwisher, Woods Hole Oceanographic Institute, Mass.

Los Angeles—October 20

"Monitoring Autonomic Nervous System Activity in Emotion and Psychological Disorders," M. A. Wenger, UCLA.

New York—April 14

"The Use of Computers as Aids in the Diagnosis of Heart Disease," W. J. Carbery, Airborne Instruments Lab.; C. A. Steinberg, Airborne Instruments Lab.

New York—May 19

"New Instrumentation Concepts for Manned Flight," L. J. Fogel, Convair, San Diego, Calif.

New York—June 16

"The Effect of Percutaneous Medication on Muscle Tissue Using Electromyographic Control," B. Post, St. John's Episcopal Hospital.

San Francisco—October 24

"Exobiology—Experimental Approaches to Life Beyond the Earth," J. Lederberg, Stanford Medical School.

Circuit Theory

Los Angeles—October 19

"Is Circuit Theory Useful at Microwave Frequencies?" S. B. Cohn, Rantec Corp., Calabasas, Calif.

"Some Unsolved Problems in Microwave Tube Research," D. G. Dow, Calif. Inst. of Technology.

(Continued on page 54A)

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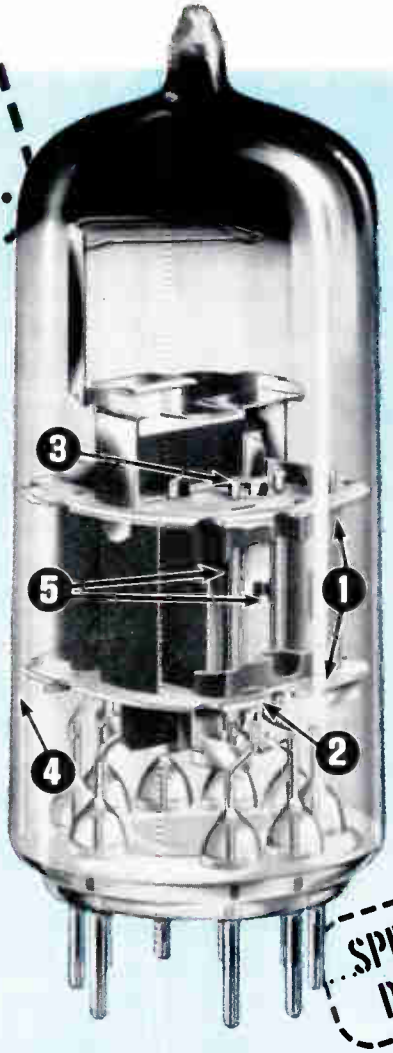
America's Largest Manufacturer of Frame Grid Tubes... Announces

2 NEW RUGGEDIZED AMPLIFRAME* TUBES... 7737 and 7308

SPECIFICALLY DEVELOPED...



1 Heavy, square mica supports — eliminate mica chipping and flaking as well as loosening of mount when subjected to shock and vibration

2 Special mica holes anchor the anode firmly

3 Tongue mica dampens cathode movement allows normal expansion and contraction...prevents cathode bowing

4 Calibrated, tapered bulb rigidly holds mount...will not allow any movement

5 'Ampliframe' grid — rigid frame with fine grid wire under tension accurately maintains close grid-to-cathode spacing

Several years ago, when AMPEREX announced the new 6922 and 6688 frame grid tubes for military and industrial applications, they were received with immediate and overwhelming acceptance. However, our applications work in these areas subsequently revealed that there was still room for improvement — as, for example, in the case of video amplifiers which must carry signals from DC to UHF... without microphonics, under extreme shock and vibration conditions. Today, with the new 7737 and 7308 AMPEREX Ampliframes (now in mass production in our Hicksville, Long Island plant), we believe that we have arrived at the ultimate in tube reliability.

***AMPLIFRAME** a new concept in electron tube construction, designed and mass produced exclusively by Amperex, incorporates the unique Frame Grid...the closest approach to the "ideal Physicists' grid" —electrical characteristics but no physical dimensions. Outstanding features of Amperex Frame Grid Tubes include: ■ higher transconductance per milliampere ■ tighter Gm and plate current tolerance ■ low transit time ■ low capacitances ■ lower microphonics

SPECIFICATIONS

	7737	7308
Swept Frequency Vibration (50-2000 cps).	10 G	10 G
Noise & Microphonics Output	190 millivolts	10 millivolts
Plate Supply Voltage	190 volts	100 volts
Grid Supply Voltage	9 volts	9 volts
Cathode Bias Resistor	630 ohms	680 ohms
Plate Current	13 mA	15 mA
Transconductance	16,500 μ mhos	12,500 μ mhos
Amplification Factor	53	33

SPECIFICALLY DEVELOPED...

for ultra-critical military and industrial applications in high shock and vibration environments

New

Amperex AMPLIFRAME 7737

Premium Quality

BROADBAND AMPLIFIER PENTODE

Extra-rugged, low-microphonic version of the 6688... for critical airborne applications, coaxial cable amplifiers, video and broadband IF amplifiers in communication links and TV equipment.

New

Amperex AMPLIFRAME 7308

Premium Quality

HIGH-GAIN TWIN TRIODE

Extra-rugged, low-microphonic version of the 6922... for use in radar, oscilloscopes, computers, broadband amplifiers and critical airborne applications.

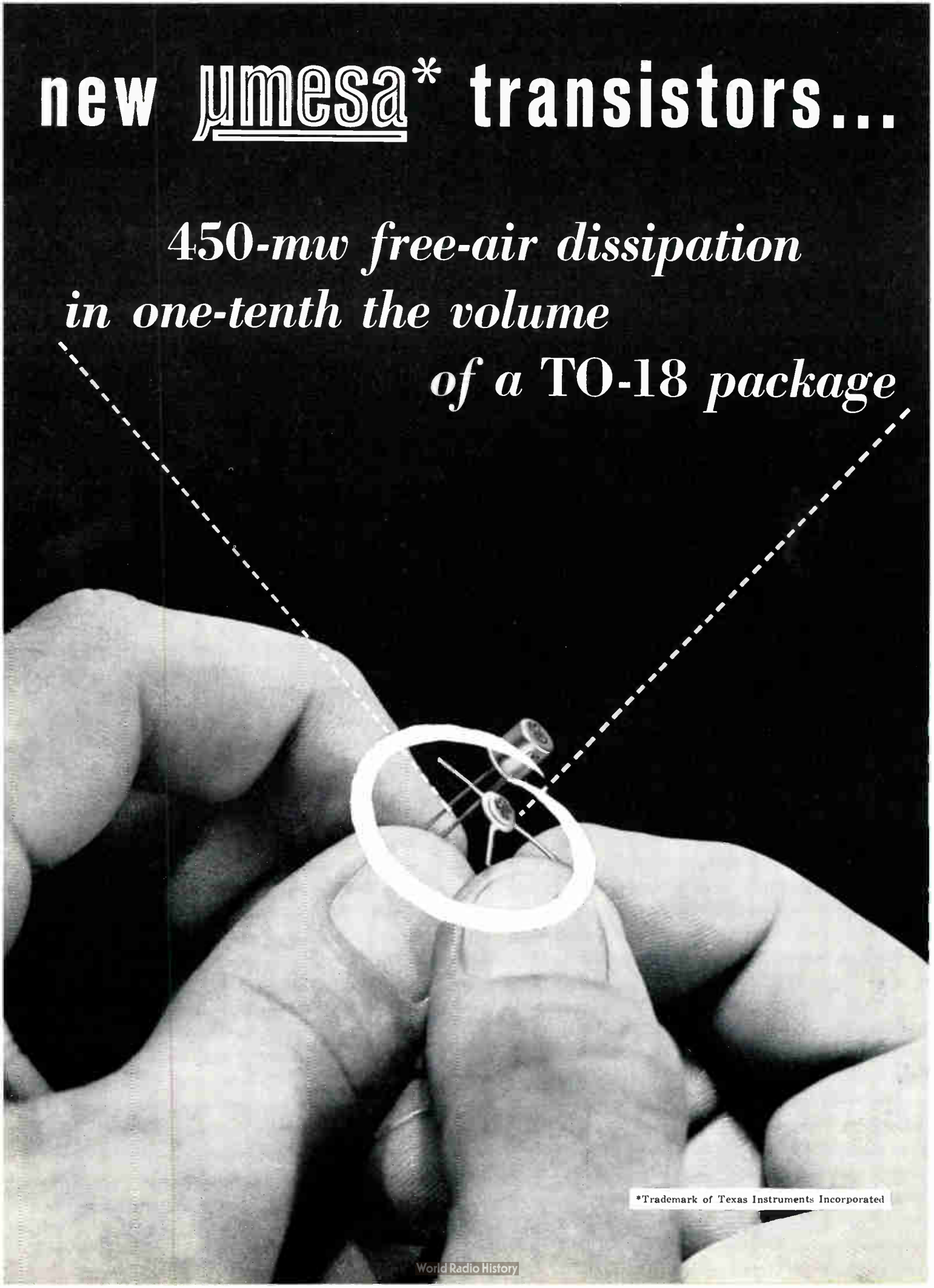
ask Amperex

about Ampliframe tubes for ultra-critical military and industrial applications

AMPEREX ELECTRONIC CORPORATION
230 Duffy Ave., Hicksville, Long Island, N.Y.
In Canada: Rogers Electronic Tubes & Components, 116 Vanderhoof Ave., Toronto 17, Ont.

new µmesa* transistors...

450-mw free-air dissipation in one-tenth the volume of a TO-18 *package*



*Trademark of Texas Instruments Incorporated

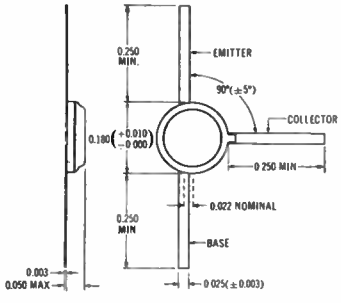
TI 450/451

silicon transistors give you more power per package volume than any other silicon transistor

Use these TI *second generation* transistors to complement your *second generation* high-speed computers.

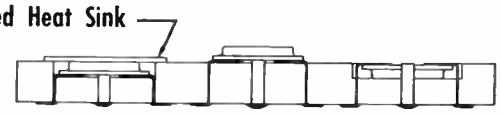
Check the outstanding advantages of the TI 450 and TI 451 . . .

- ☑ 1/10 the volume of a TO-18 package
- ☑ 450-mw free air dissipation @ 25°C
- ☑ hermetically-sealed-in reliability
- ☑ backed by a full year's warranty
- ☑ electrically the same as 2N706A and 2N753
- ☑ ribbon leads for "two-dimensional" mounting
- ☑ 1/5 the weight of a TO-18 package — only 0.07 gms
- ☑ heat sinking simplified by electrically isolated case



SUGGESTED MOUNTING METHODS

Copper-etched Heat Sink



Conventional mounting for dip soldering.

Heat Sink

Alternate mounting technique for welded connections or silk-screened wiring connections.

Electrical characteristics @ 25°C ambient

Symbol	Parameter	Test Conditions	Type	Min	Max	Units
t_{on}	Turn-On Time	I_{B1} = 3 ma, I_{B2} = 1 ma V_{CC} = 3 v, R_L = 270 Ω			40	nsec
t_{off}	Turn-Off Time	P. W. ≥ 400 nsec, less than 2% duty cycle			75	nsec
$V_{CE\ (sat)}$	Collector-Emitter Saturation Voltage	I_C = 10 ma, I_B = 1 ma (Pulse Test)			0.6	v
h_{FE}	DC Forward Current Transfer Ratio	V_{CE} = 1 v, I_C = 10 ma	TI 450	20	60	
			TI 451	40	120	

Specify TI for all your silicon transistor requirements—small signal • switching • medium power • power

IN TI DISTRIBUTOR STOCKS 3D DEPTH - DELIVERY - DEPENDABILITY

SEMICONDUCTOR-COMPONENTS DIVISION

TEXAS INSTRUMENTS

LIMITED — DALLAS ROAD • BEDFORD, ENGLAND

INCORPORATED — 13500 NORTH CENTRAL EXPRESSWAY • DALLAS, TEXAS

Professional Group Meetings

(Continued from page 50A)

Syracuse—September 20

"Analysis of Nonlinear Systems," Dr. A. A. Wolfe, Stromberg-Carlson, Rochester, N. Y.

Communication Systems

Oklahoma City—September 27

"Limpander Amplifiers," J. B. Daniel, Electronic Systems Engrg. Co., Oklahoma City, Okla.

Syracuse—October 27

"Advanced Satellite and Space Probe Telemetry Systems," H. N. Putschi, General Electric, Syracuse.

Toronto—November 3

"Use of Microwave to Support a High Altitude Platform," R. L. McFarlan, President, IRE.

Communication Systems
Vehicular Communications

Omaha-Lincoln—October 28

"The Strategic Air Command 'Short Order' Single Sideband System," G. King, USAF, Offutt AFB.

"The SAC 'Short Order' SSB System Controls," K. Glorfield, Alpha Corp., Offutt AFB.

Component Parts

Los Angeles—October 17

"Gyro Applications in Ballistic Missiles and Space Vehicles," P. Ott, Gyro Applications Eng., Nortronics.

Component Parts
Product Engineering and Production

Metropolitan New York—April 20

"Capacitors in Europe," L. Kahn, Aerovox Corp., New Bedford, Mass.

Component Parts
Reliability and Quality Control

Metropolitan New York—June 8

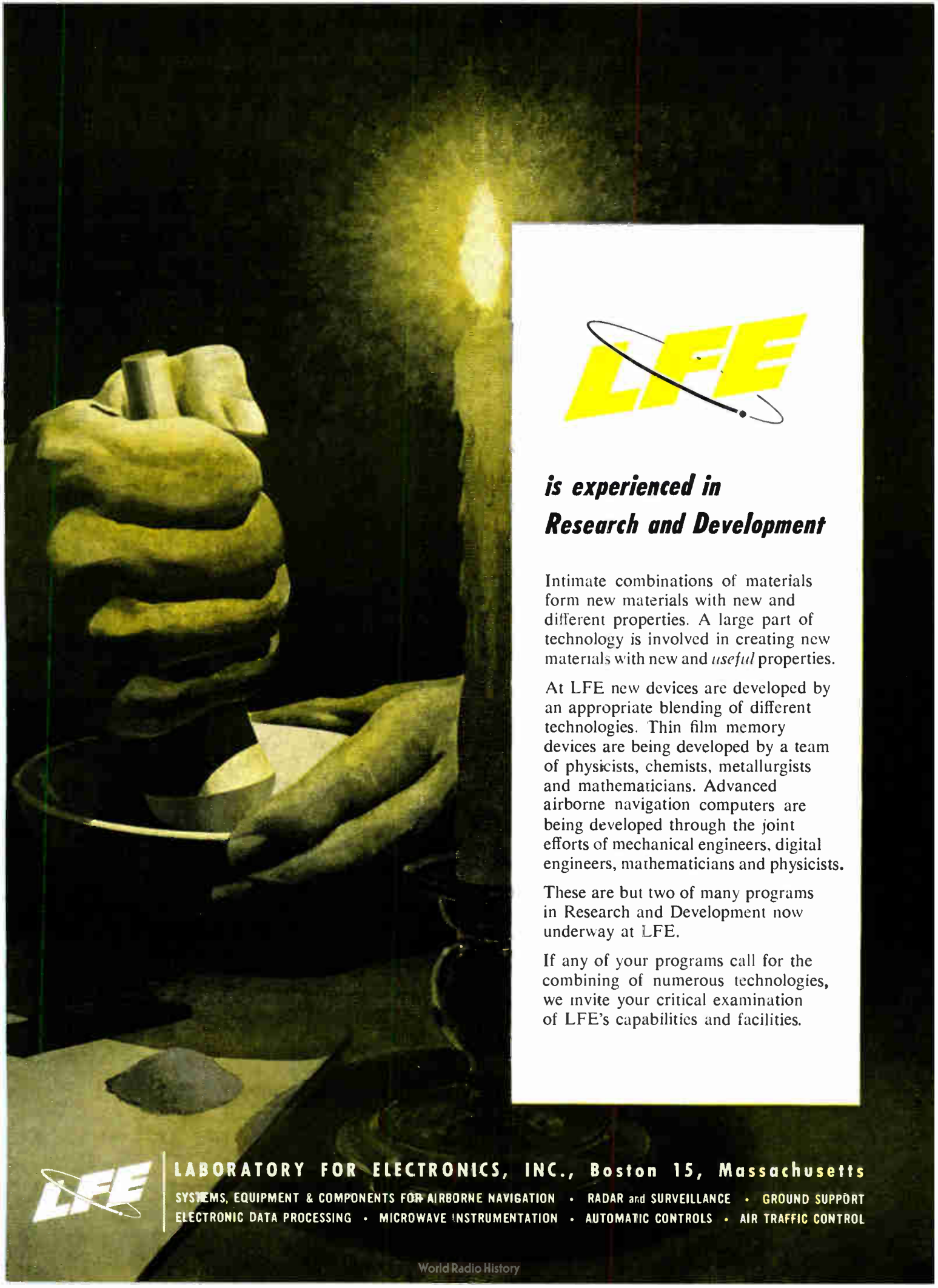
"Specifying and Assuring the Reliability of Component Parts," G. Neuschaefer, Brooklyn Navy Yard.

Electron Devices

Los Angeles—October 10

"Thermoelectrics," Buckman, Johnson, Tang, Airesearch Corp., Los Angeles.

(Continued on page 58A)



LFE

is experienced in Research and Development

Intimate combinations of materials form new materials with new and different properties. A large part of technology is involved in creating new materials with new and *useful* properties.

At LFE new devices are developed by an appropriate blending of different technologies. Thin film memory devices are being developed by a team of physicists, chemists, metallurgists and mathematicians. Advanced airborne navigation computers are being developed through the joint efforts of mechanical engineers, digital engineers, mathematicians and physicists.

These are but two of many programs in Research and Development now underway at LFE.

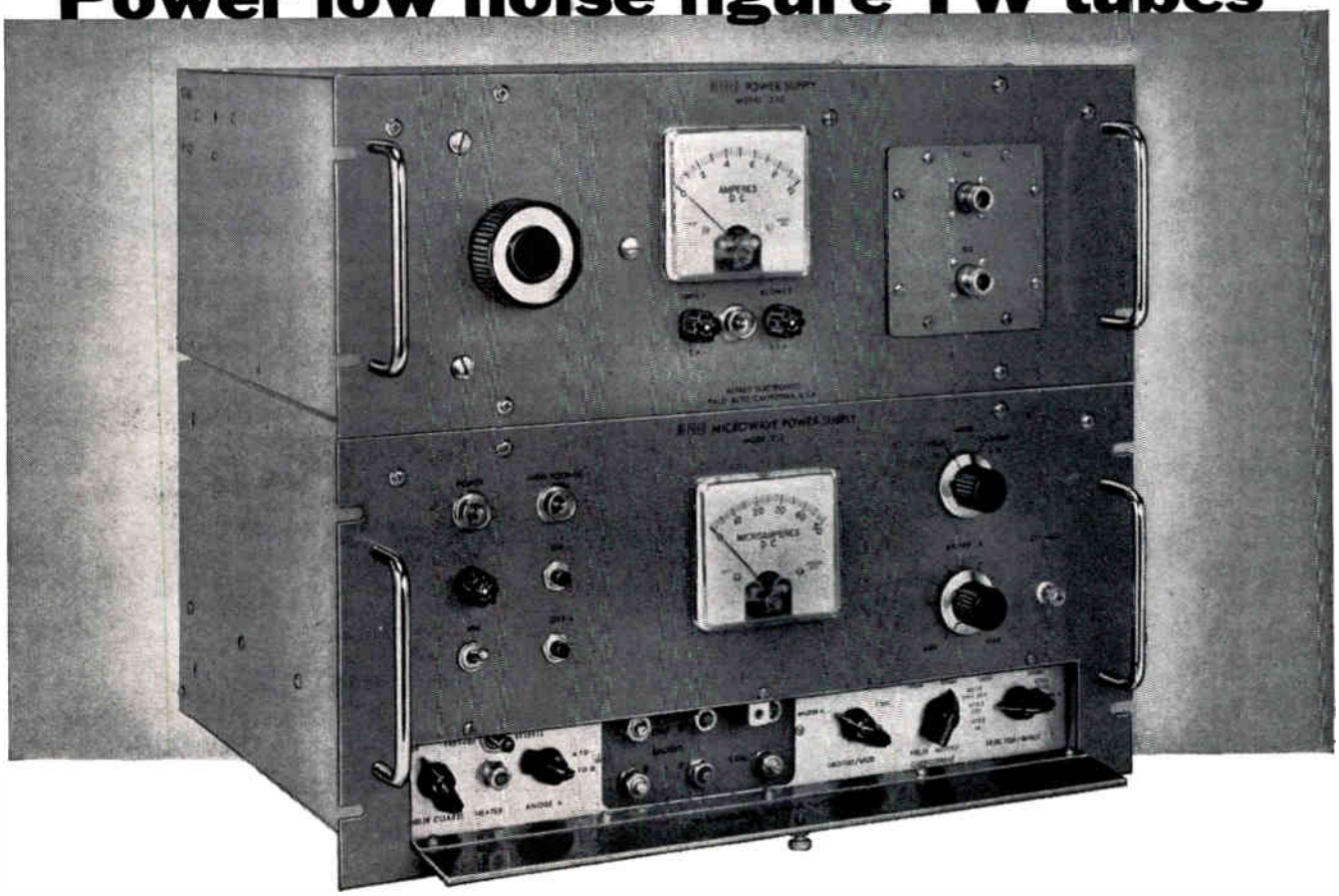
If any of your programs call for the combining of numerous technologies, we invite your critical examination of LFE's capabilities and facilities.

LFE

LABORATORY FOR ELECTRONICS, INC., Boston 15, Massachusetts

SYSTEMS, EQUIPMENT & COMPONENTS FOR AIRBORNE NAVIGATION • RADAR and SURVEILLANCE • GROUND SUPPORT
ELECTRONIC DATA PROCESSING • MICROWAVE INSTRUMENTATION • AUTOMATIC CONTROLS • AIR TRAFFIC CONTROL

Power low noise figure TW tubes



with one ALFRED *supply!*

This compact ALFRED ELECTRONICS microwave power supply provides electrode voltages for nearly all medium and low noise figure TW tubes. Companion solenoid supplies for electromagnet focused TW tubes are available. Here are the major advantages of this precision ALFRED supply:

☆ FLEXIBILITY

One electrode supply operates most presently known tubes. It will operate new tubes as they become available. Cover present and future needs with *same* supply.

☆ INTERCHANGEABILITY

Build all your low noise amplifiers around standard unit. Simplify servicing. Stock parts for only one type of supply.

☆ LOCAL OR REMOTE OPERATION

Model 252 design permits remote operation of TW tube as may be required with broad-band preamplifiers. Heater supply has extra wide voltage range to compensate for cable IR drop.

☆ SIMPLE OPERATION

Only two controls on front panel for day-to-day operation. Set-up controls are on recessed subpanel. All voltages and currents are internally measured using front panel meter and recessed selector switch.

☆ STABILITY

Electrode supplies are well-regulated and designed for minimum drift. Use of dc heater power reduces spurious amplitude modulation.

☆ 50 TO 450 CPS INPUT

Wide band power input permits use with almost any available power source.

☆ ECONOMY

Separate solenoid supplies are available. Purchase only the supply you need when you need it.

KEY SPECIFICATIONS FOR MODEL 252
Helix: Voltage, 75 to 1400 v; Ripple, less than 20 mv pk-to-pk; Regulation, ±.03% line. **Collector:** 0 to +300 v relative to helix. Four Anodes, ranging from −100 v to +900 v relative to cathode. Heater, 0 to 11 v DC at 0 to 1 amp with 2% regulation. All electrode supplies internally metered.

Two low ripple Solenoid Supplies are available. Both are adjustable over a wide range providing adequate power for most TW tube focusing magnets. Model 253 is unregulated; Model 254 is current regulated.

KEY SPECIFICATIONS FOR MODEL 253
0 to 105 v DC at 0 to 7.5 amp or 0 to 110 v at 6 amp. Ripple, .5% pk-to-pk.

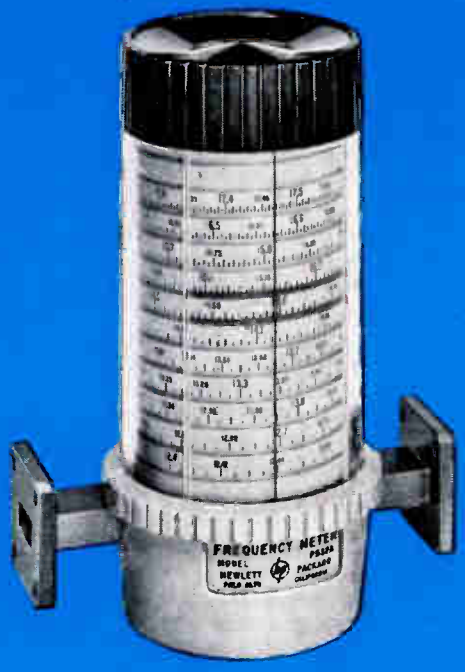
KEY SPECIFICATIONS FOR MODEL 254
0 to 100 v DC at 0 to 7.5 amp or 0 to 105 v at 6 amps. Ripple, .5% Regulation, ±1% for ±10% line change or 30% load change.

PRICES: Model 252, $890; Model 253, $200; Model 254, $350.

WRITE FOR MORE DATA—*Contact your* ALFRED *engineering representative for more details, or write us directly at Dept. 86.*

ALFRED ELECTRONICS
897 Commercial Street • Palo Alto, California
DAvenport 6-6496

8



COMPLETE FREQUENCY COVERAGE

Highly accurate, direct reading wide band

FREQUENCY METERS

3.95 to 40 KMC!

Now hp offers you high quality, moderately priced precision Frequency Meters covering eight important microwave bands.

Frequency is read directly in KMC on the large, precisely calibrated spiral scale. No charts or interpolation are required. Accuracy is high—up to 0.06% including 0 to 100% relative humidity change, 20° C temperature variation and dial accuracy (See Specifications).

Model 532 Frequency Meters comprise a special waveguide section mounting a high Q resonant cavity tuned by a choke plunger. A 1 db or greater dip in output indicates resonance. There are no spurious modes or resonances. Tuning is by a precision lead screw, spring loaded to eliminate backlash. Minimum calibration spacing is 1/32" to provide good resolution.

SPECIFICATIONS

Model No.	Overall Accuracy (%)	Frequency Range KMC	Dial Calib Accuracy (%)	Calibration Increment (MC)	Max. Temp. Coefficient % per ° C	Price
G532A	0.065	3.95 - 5.85	0.033	1	0.0012	$325.00
J532A	0.065	5.30 - 8.20*	0.033	2	0.0012	300.00
H532A	0.075	7.00 - 10.0	0.040	2	0.0015	195.00
X532B	0.080	8.20 - 12.4	0.050	5	0.0010	150.00
M532A	0.085	10.0 - 15.0	0.053	5	0.0012	275.00
P532A	0.100	12.4 - 18.0	0.068	5	0.0012	210.00
K532A	0.110	18.0 - 26.5	0.077	10	0.0013	230.00
R532A	0.120	26.5 - 40.0	0.083	10	0.0017	250.00

K and R band models available with circular flange adapters; specify K532AC and R532AC respectively.

*When used between 5.3 to 7.5 KMC, or 5.7 to 8.2 KMC, single mode resonance is achieved.

Data subject to change without notice. Prices f.o.b. factory.

For complete details, call your hp representative or write direct

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hp complete instrumentation for microwave measurements

Professional Group Meetings

(Continued from page 54A)

New York—May 12

"Military Applications of Infra-Red Devices," Dr. D. K. Coles, ITT Labs., Ft. Wayne, Ind.

Metropolitan New York—September 29

"Ferroelectric Energy Converters," S. R. Hoh, ITT Labs., Nutley, N. J.

Electron Devices Microwave Theory and Techniques

San Francisco—September 21

"Paramagnetic Resonance," G. E. Pake, Stanford Univ., Stanford, Calif.

San Francisco—October 13

"Tube Trends for the Space Age," H. I. Ewen, Ewen-Knight Corp.

Electronic Computers

Detroit—October 31

"The Application of Tunnel Diodes to Digital Computers," F. K. Buelow, IBM, Poughkeepsie.

Fort Worth—November 1

"Digital and Pulse Circuits," H. Cragon, Texas Instruments Inc.

Houston—October 20

"The 1620 IBM," D.Williamson, IBM, Houston.

New York—September 29

"Unique Features of Republic Aviation Airborne Digital Computer," N. Nessenoff and M. Modschein, Republic Aviation Corp., Mineola, L. I.

San Francisco—September 27

"New Systems' Concepts in Control," G. M. Amdahl, IBM, San Jose.

Washington, D. C.—October 5

"The Perceptron," A. E. Murray, Cornell Aeronautical Lab.

Washington D. C.—November 2

"A Review of Cryoelectric Computer Elements," W. B. Ittner, III, IBM, Yorktown.

Engineering Management

Boston—October 20

"Profit Improvement through Organization Planning," J. G. Hendricks, Raytheon Co., Watertown, Mass.

Metropolitan New York—February 18

"The Computer as an Aid to Engineering Management," Dr. T. C. Fry and C. F. Crichton, Remington Rand.

(Continued on page 60A)

Mercury-wetted contact relays, steel-enclosed and ready for mounting on your own assembly line, give you Clare reliability in operation, combined with new ease of application and handling. Clare HG and HGS relays have test records of over 10 billion operations, without maintenance or change in characteristics. In these new modular cases, they're sturdy, magnetically shielded, easily replaceable.

Choose either the standard Clare HG relay, or the HGS—super-fast and super-sensitive. You'll gain extra convenience and increased component-density with these Clare Relay modules.

Now you can mount CLARE BILLION-OPERATION RELAYS on your own printed circuit board

Typical Clare mercury-wetted relay steel-enclosed modules for circuit-board mounting. From top: HGSM Relay Module, HGM Relay Module, HGPM Relay Module. Epoxy molded Relay Modules are also available.

Each relay contains one or more of these magnetic switches. Mercury-wetted contact surfaces are continually wetted by capillary action; they never bounce, never get dirty, never weld, and never wear out.

Get Bulletin CPC-8 for detailed specifications, characteristics, dimensions: Ask your Clare representative, or address C. P. Clare & Co., 3101 Pratt Blvd., Chicago 45, Illinois. In Canada: C. P. Clare Canada Ltd., 840 Caledonia Road, Toronto 19, Ontario. Cable address: CLARELAY.

C. P. CLARE & CO.

Relays and Related Control Components

Professional Group Meetings

(Continued from page 58A)

Metropolitan New York—April 21

"Briefing for Executive Action," Dr. O. G. Haywood, F. Huyck & Son, New York, N. Y.

San Francisco—October 12

"Can Managers Remain Creative," J. E. Arnold, Stanford University, Stanford, Calif.

Syracuse—October 6

"PERT (Program Evaluation & Review Technique) in the Polaris Program," W. Fazar, USN Special Projects Office, Washington, D. C.

"PERT in Industry," J. Pearlman, General Electric Co., Utica, N. Y.

A film following the Polaris (Fleet Ballistic Missile) through Development.

Engineering Writing and Speech

San Francisco—October 18

"Motion Pictures as another Tool for the Engineering Writer," T. Brickley, Palmer Films, Inc., San Francisco.

"How the 'Writer Producer' Can Use Motion Picture Services," W. A. Palmer, Palmer Films, Inc., San Francisco.

Industrial Electronics

Chicago—October 14

"Radiation Gaging in Industry," R. L. Carver, Nuclear-Chicago Corp.

Instrumentation

San Francisco—October 4

"Progress in Development of Electronic Standards," C. Sheehan, Ampex Corp., Redwood City; T. Whittimore, Philco Corp., Palo Alto; L. Burlingame, Lenkurt Electric Co., San Carlos; P. Hand, Hewlett-Packard, Palo Alto.

Microwave Theory and Techniques

Boston—October 13

"Low Noise Microwave Amplification," Dr. G. Wade, Raytheon Spencer Lab., Burlington, Mass.

Denver—June 6

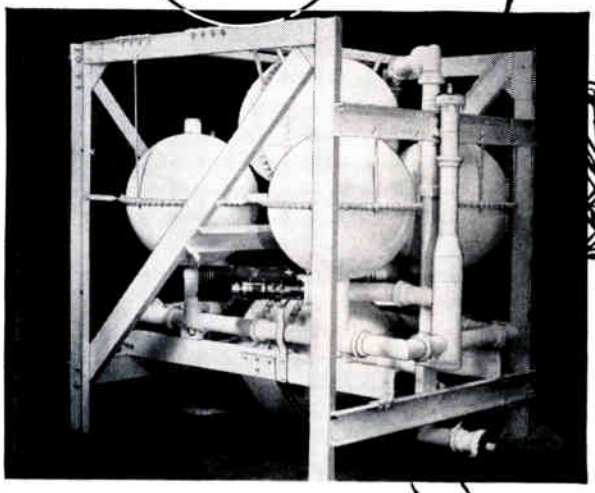
"Flow Graphs for Analysis of Electronic Systems," C. S. Lorens, Jet Propulsion Lab., Calif. Inst. of Technology.

Denver—June 28

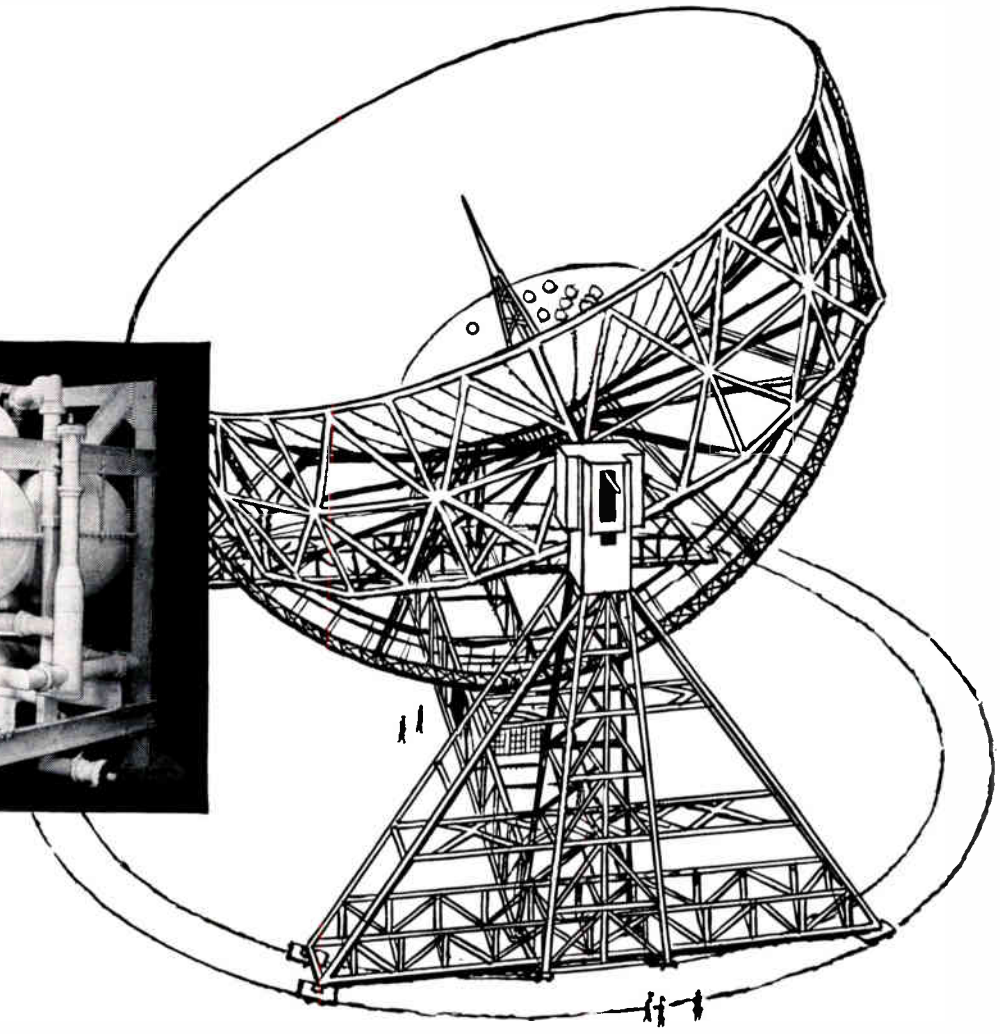
"Properties of the H'guide at Microwave and Millimeter Waves," F. J. Tischer, Ohio State University.

(Continued on page 64A)

ANOTHER MEASURE OF DIELECTRIC'S CAPABILITY



THIS UHF DIPLEXER NETWORK was built by **DIELECTRIC** Products Engineering Company, Inc., under contract from Space Technology Laboratories, Inc. It is now installed in the tower of the single giant antenna of "SpaN Net's" Jodrell Bank radio telescope at Manchester, England Its function is . . .



isolating simultaneous signals to and from deep-space payloads

Commanding and monitoring space vehicles is the responsibility of "SpaN Net" . . . a global network of radio telescopes set up and operated by Space Technology Laboratories for U.S.A.F.

To fulfill its mission, "SpaN Net" had to meet challenges far beyond the state of the communications art. Never before had powerful command signals and faint telemetered deep-space data been simultaneously handled by a single antenna. How could transmit and receive channels with a differential of more than 200 decibels be isolated? Conventional diplexer technology was not the answer.

Teamwork solved the isolation problem! "SpaN Net" assigned the task to Space Technology Laboratories, Inc., who added DIELECTRIC of Maine to its research, development and production team. Result? An ultra-high-frequency diplexer network that allows the Jodrell Bank radio telescope's single antenna to transmit 20 kw commands and receive 0.002 microvolt signals . . . simultaneously.

This contribution to SpaN Net's break-through is typical of product advances by DIELECTRIC If you have similar problems in communications . . . from design to delivery . . . it pays to contact DIELECTRIC. Capabilities, facilities and accomplishments are described in our brochure. Write for it today.

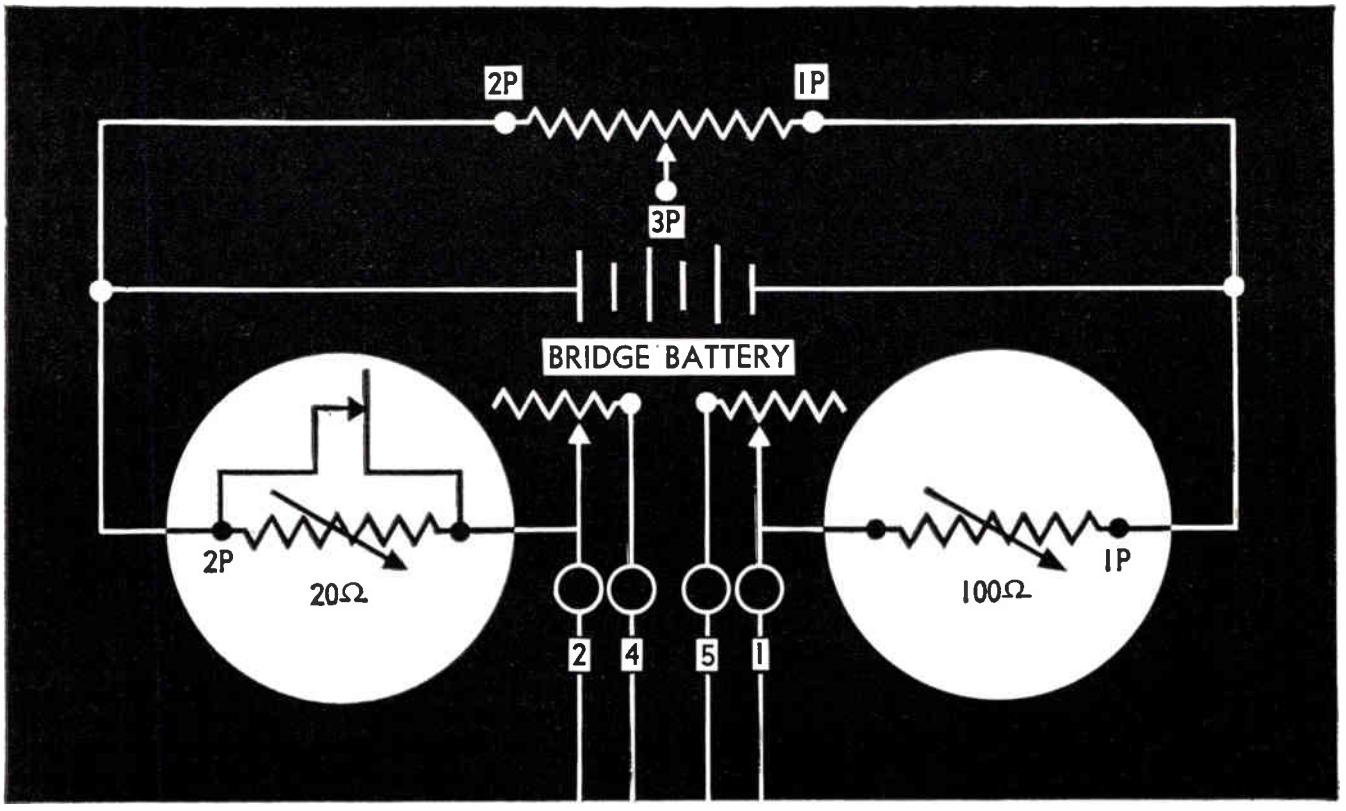
Other areas of **DIELECTRIC** capability in coaxial, waveguide and open wire techniques . . .

TRANSMISSION LINE & COMPONENTS • NETWORKS • SWITCHES • ANTENNAS & FEEDS
TEST EQUIPMENT • R&D ENGINEERING

dial DIELECTRIC for solutions to communications problems.

DIELECTRIC PRODUCTS ENGINEERING CO., INC.

RAYMOND, MAINE



Eliminate Trimming Resistor Problems with Borg Absolute-Linearity Micropots

The above schematic illustrates how many original equipment manufacturers are eliminating trimming networks from circuits by replacing conventional potentiometers with Borg 900 Series *Absolute Linearity* Micropots. The Borg 900 Series eliminates electrical overhang . . . trimming becomes unnecessary. A further advantage is accomplished by setting the 900 Series mechanical stop to a phasing point. Field replacement of the primary potentiometer now becomes a simple mechanical process of attaching leads and phasing from the preset stop. This means you do not have to replace trimmers or resistors each time you replace the primary potentiometer. The design advantages and cost savings brought about by the *absolute linearity* of the Borg 900 Series can now be fully appreciated. With 900 Micropots, your equipment will afford greater accuracy, reliability and practicality because trimming and adjustments with auxiliary resistors are no longer required. Trained assembly personnel can now be concentrated on more profitable areas of production. Many other 900 Series advantages can help solve your potentiometer problems as they are now doing in all types of industry. The 900 Series is available in ten and three turn models with several optional features. Contact your Borg technical representative or let us put him in touch with you. *Ask for data sheets BED-A128 and BED-A129.*

BORG®

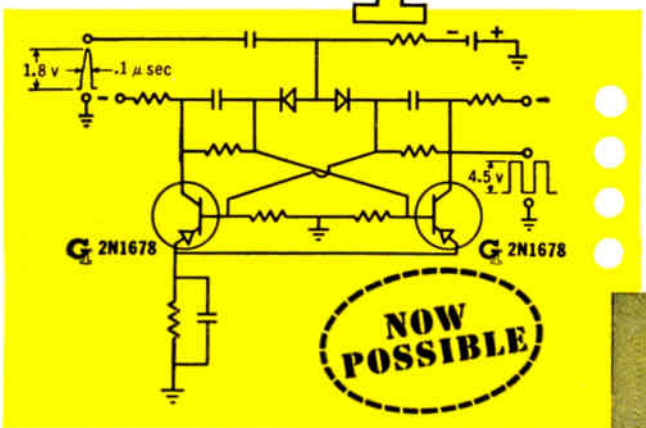
BORG EQUIPMENT DIVISION

Amphenol-Borg Electronics Corporation
Janesville, Wisconsin • Phone Pleasant 4-6616

Micropot Potentiometers • Turns-Counting Microdials • Sub-Fractional Horsepower Motors • Frequency and Time Standards

General Instrument Semiconductor . . . Design Breakthrough

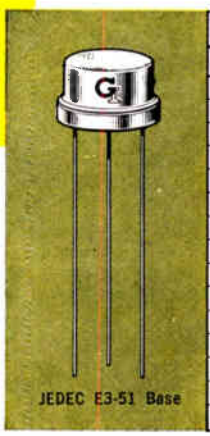
NEW G 2N1678 "DYNAMIC DRIFT"



High Voltage
High Speed
Saturated Circuitry
At Low Cost

General Instrument proudly presents the 2N1678 "Dynamic Drift". . . ideally suited for high speed, high voltage saturated circuit applications. The 1 Mc bistable multivibrator, above, is only one example of the multitude of applications for this attractively-priced transistor family.

Life test data proves reliability of the new General Instrument 2N1678 "Dynamic Drift". Close quality control guarantees extremely high electrical uniformity, shipment to shipment.



2N1678 PNP Germanium "Dynamic Drift"

Parameter	Conditions	Min.	Typ.	Max.
T_s		−65°C		+85°C
P_c	$T_a = 25°C$			120 mw
V_{CES}	$I_c = 100\ \mu a$	60 v		
V_{CBO}	$I_{CBO} = 25\ \mu a$	60 v		
V_{EBO}	$I_{EBO} = 100\ \mu a$	4 v		
h_{FE}	$I_c = 20$ ma; $V_{CE} = 0.25$ v	25	40	
I_{CBO}	$V_{CB} = 10$ v			5 μa
V_{BE}	$I_c = 20$ ma; $V_{CE} = 0.25$ v			0.6 v
$f_{\alpha fb}$	$I_E = 1$ ma; $V_{CE} = 5$ v	25 Mc	35 Mc	
$f_{\alpha fb}$	$I_E = 1$ ma; $V_{CE} = 10$ v		50 Mc	
h_{ib}	$I_E = 1$ ma; $V_{CE} = 5$ v; $f = 1$ kc		30 Ω	
h_{ob}	$V_{CB} = 5$ v; $I_e = 1$ ma; $f = 1$ kc		0.5 μ mho	2 μ mho
C_{ob}	$V_{CB} = 5$ v; $I_e = 1$ ma; $f = 5$ Mc		3.5 pf	5 pf
$t_r + t_d$	$I_c = 20$ ma; $I_{B1} = I_{B2}$		0.4 μ sec	
$t_s + t_f$	$= 1$ ma; $R_L = 1$K		0.4 μ sec	

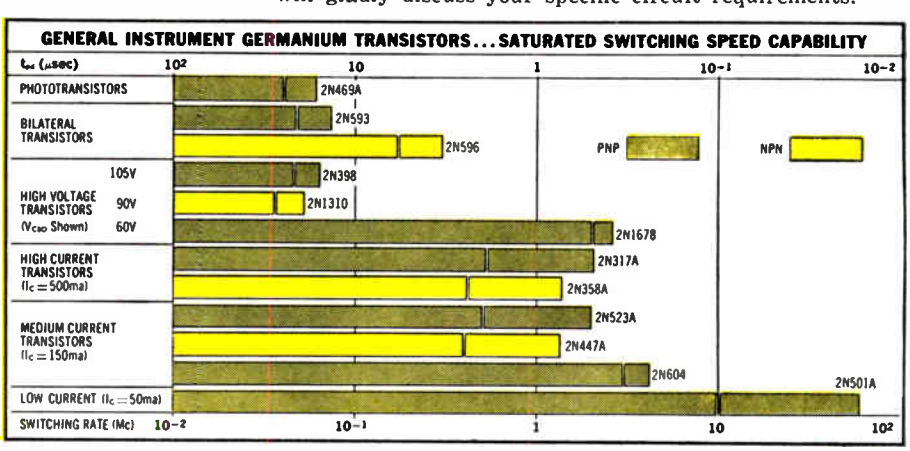
FULL LINE OF QUALITY G COMPUTER SEMICONDUCTORS

General Instrument is your major source for high quality computer semiconductors . . . *transistors*, as well as *companion diodes*, *rectifiers* and *logic encapsulations* for every type of circuit application. The transistor families shown below indicate the broad range of superior quality units offered by General Instrument.

Write General Instrument for complete engineering and life test data, design curves, and typical circuitry which takes advantage of the unique combination of characteristics offered by the new G 2N1678. Data is available, of course, on our full line of computer semiconductors. Our engineers will gladly discuss your specific circuit requirements.

All speeds shown have been attained with conventional saturated circuitry. Total bar length represents rate (period) using speed-up capacitors; broken bar indicates maximum speed without capacitor.

Representative transistors shown are alloyed-junction devices. Types 2N501A, 2N604, and 2N1678 are MADT, Drift, and High-Voltage Drift, respectively.



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TRANSISTORS, DIODES, RECTIFIERS

G SEMICONDUCTOR
DIVISION OF GENERAL INSTRUMENT CORPORATION
65 Gouverneur Street, Newark 4, New Jersey

For immediate delivery of G Semiconductors, call your local authorized stocking distributor.

IN CANADA: General Instrument—F. W. Sickles of Canada Ltd., P.O. Box 408, 151 S. Weber Street, Waterloo, Ontario, Canada. Sherwood 4-8101.

Professional Group Meetings

(Continued from page 60A)

New York—January 14

"Fundamentals of Antennas," Dr. H. Jasik, Jasik Labs., Inc., Westbury, L. I.

New York—January 21

"Principles of Traveling Wave Antennas," A. A. Oliner, Microwave Research Institute, Brooklyn.

New York—January 28

"Reflectors as Antennas," R. L. Mattingly, Bell Telephone Labs.

New York—February 4

"Lens Structures and Artificial Dielectrics," K. S. Kelleher, AGA Corp., Alexandria, Va.

New York—February 11

"Microwave Measurement Techniques," Dr. T. E. Tice, Ohio State University.

New York—April 7

"The Role of Plasmas in Microwave Engineering—Panel Meeting," Dr. N. Marcuvitz, Microwave Research Institute; Dr. Gould, Microwave Associates; Prof. L. Smullen, MIT; O. T. Fandingsland, Raytheon Mfg. Co.

New York—May 19

"Practical Utilization of Power Transmission by Electromagnetic Beams," W. C. Brown, Raytheon Mfg.

Military Electronics

Long Island—October 25

"Reconnaissance Photography," J. Zilko, Fairchild Camera & Instrument Corp.

Nuclear Science

Los Angeles—October 18

"The Use of Semiconductor Junction Devices as Nuclear Particle Detectors," J. W. Mayer, Hughes Aircraft Co.

Oak Ridge (Atlanta)—September 15

"Clinical Gamma Ray Detectors and Their Problems," D. A. Ross, Oak Ridge Inst. of Nuclear Science Medical Division.

Product Engineering and Production

New York—October 3

"Economical Design of Military Electronic Equipment," P. D. Belz, Westinghouse Electric, Baltimore, Md.

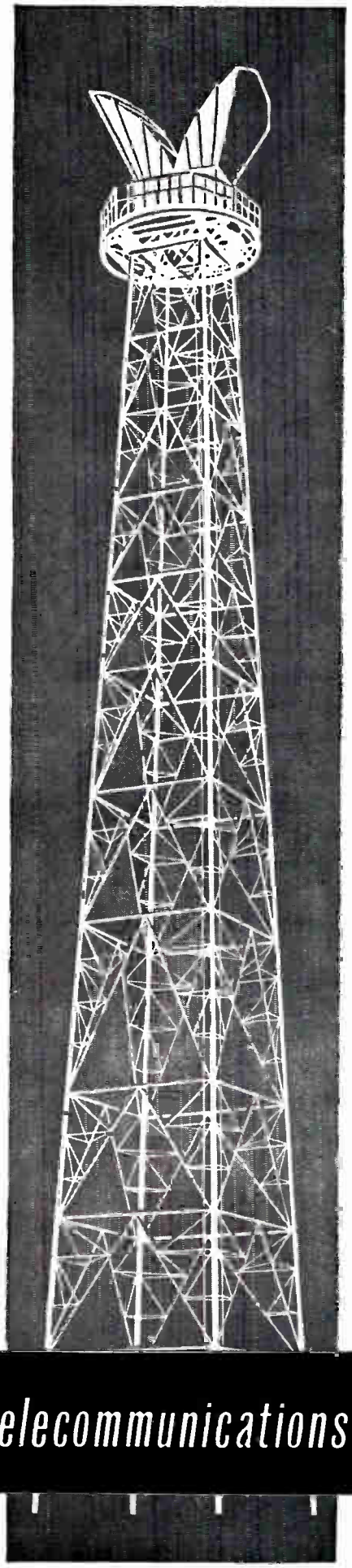
San Francisco—September 27

"Movie on Manufacture of High Density Electronic Packages," Lockheed Sunnyvale Plant.

(Continued on page 68A)

G.E.C.

SHF Broadband Radio Equipment carries 960 speech circuits or 1 television circuit on Trans-Continental routes



The latest GEC triumph in the field of telecommunications is their new ***SHF Broadband Radio Equipment*** which operates in the 6000 Mc/s band and carries 960 speech circuits or a television circuit.

Choice of a band in the SHF range was due to GEC engineers, who foresaw that the design objectives could not economically be achieved in the 2000 Mc/s band, and because of their firm belief that within the next few years the 4000 Mc/s band would become increasingly congested.

It is significant that this new equipment has already been chosen for the new British television link between Carlisle and Kirk o' Shotts.

Please write for further information to:

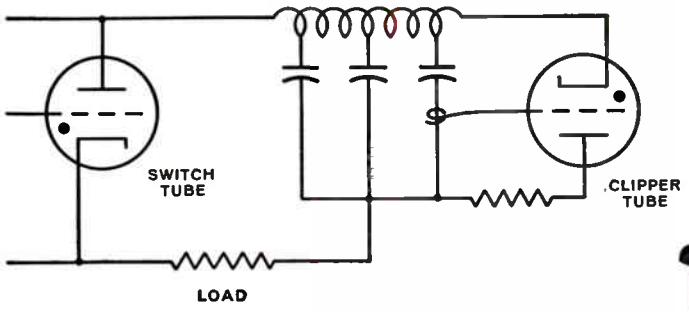
Everything for Telecommunications G.E.C.

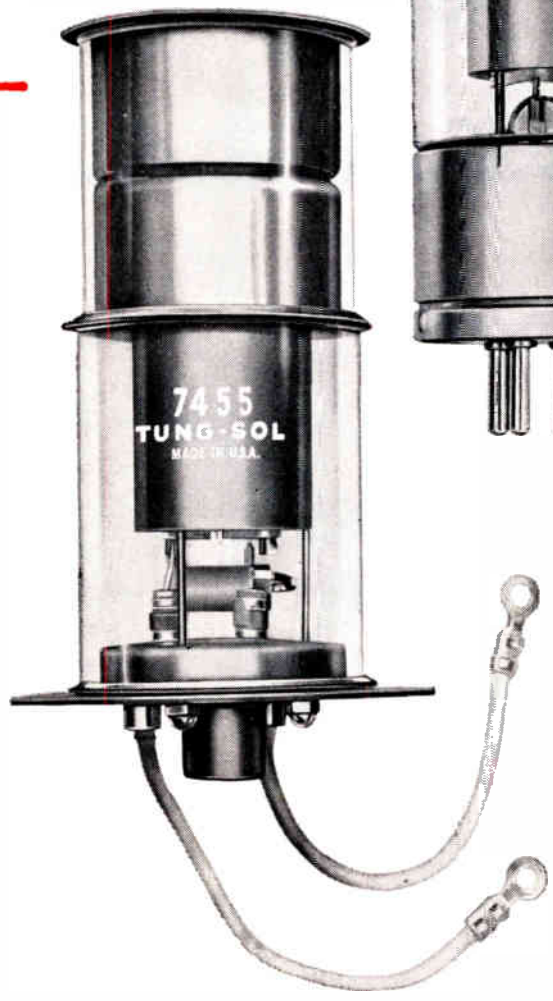
THE GENERAL ELECTRIC COMPANY LIMITED
OF ENGLAND
Telephone Works, Coventry, England.
Works at Coventry, London, Middlesbrough, Portsmouth.

Smee's GEC 66

End-of-line clipper

Clipper tube is connected across the far end of the pulse-forming network in series with a resistive load whose value approximates the network impedance. When the clipper tube is triggered, the pulse-forming network terminates in its characteristic impedance thereby reducing the inverse voltage to zero.





Positive protection against destructive voltages with Tung-Sol Clipper Thyratrons

Line-type radar modulators require clipper protection against excess inverse voltages, which can destroy costly components and increase equipment downtime. Clippers also perform valuable circuit service by regulating pulse amplitudes and reducing switch tube loading.

But until Tung-Sol developed these high-reliability hydrogen-filled clipper triodes previously used clipping devices brought some serious disadvantages to the job.

Now, however, you can be sure of *perfect* clipping action when you design Tung-Sol clippers into your equipment. More rugged and less costly than solid state devices, more efficient with a much lower dynamic impedance than vacuum clippers, and faster acting and more resistant to arc-back than gas diodes, the new Tung-Sol thyratron clippers are designed and built to deliver uncompromised performance.

The low "firing" voltage and the ability to carry large peak currents make these hydrogen clipper thyratrons ideal for this application. These tubes also feature hydrogen reservoirs which promote long life by providing an automatic mechanism for replenishing hydrogen lost by "cleanup".

Circuit requirements are simple whether the Tung-Sol thyratrons are used as "end of the line" clippers, "across switch" clippers or "tail biters".

Write for complete technical details on the new 7454 and 7455 Clipper Thyratrons. Tung-Sol Electric Inc., Newark 4, N. J. TWX:NK193.

TUNG-SOL®

Technical information available through ATLANTA, GA.; COLUMBUS, OHIO; CULVER CITY, CALIF.; DALLAS, TEXAS; DENVER, COLO.; DETROIT, MICH.; IRVINGTON, N. J.; MELROSE PARK, ILL.; NEWARK, N. J.; PHILADELPHIA, PA.; SEATTLE, WASH. IN CANADA: ABBEY ELECTRONICS, TORONTO, ONT.

Professional Group Meetings

(Continued from page 64A)

San Francisco—October 25

"Theory and Practice of Impurity Concentration and Control in Silicon Mono Crystals," H. Kramer, Knapic Electrophysics Inc., Palo Alto.

Radio Frequency Interference

Fort Worth—October 11

"System Cabling: The Weakest Link in the Chain of Interference Control," M. B. Tomme, Convair Division General Dynamics.

Space Electronics and Telemetry

Los Angeles—October 18

"Synchronization Methods for PCM Telemetry," M. C. Pawley; U. S. Naval Ordnance Lab.

Vehicular Communications

Detroit—October 26

"Mobile Installation Headaches, Batteries, Antenna Location, Ignition Noise," E. Denstaedt, City of Detroit (Moderator); S. Estes, Hallett Mfg. Co.; E. Bivek, Ford Motor Co.; P. Skeels, General Motors; R. Batts, Motorola Inc.; R. Stinson, Chrysler Corp.

Metropolitan New York—November 17, 1959

"Universal Mobile Communications," A. F. Cilbertson, Lenkurt Electric Co., San Carlos, Calif.

Metropolitan New York—February 16

"Design Considerations of ITT Mobile Telephone Equipment for Common Carrier Service," K. Haase, ITT Indl. Products Div., San Fernando, Calif.

Metropolitan New York—March 23

Dinner and entertainment for all PGVC members and guests attending IRE International Convention.

Metropolitan New York—May 3

"Report on Joint SAE, IRE and EIA Cooperative Test of Ignition Noise in Mobile Radio Systems," S. Mayer, Allen B. DuMont Labs., Clifton, N. J.

Metropolitan New York—October 4

"A New Amplitude Modulation System Employing Hybrid Tubes," W. L. Smith, DuMont Labs., Clifton, N. J.

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	PERIPHERAL EQUIPMENT	LOGIC	MEMORY	POWER SUPPLY
GERMANIUM TRANSISTORS	2N1038 Series, 2N1046 Series — Driver 2N1302 Series — Logic and Medium Power Driver 2N250 Series, 2N511 Series — Electromechanical Driver	2N797 — Very High Speed 2N705, 2N710, 2N711, 2N1385 — High Speed N100, N101 — Medium Speed 2N1302 Series	2N1046 Series — Driver	2N1038 Series, 2N1042 Series — Medium 2N250 Series, 2N456 Series, 2N1038 Series — High 2N1046 Series — Power
SILICON TRANSISTORS	2N332 Series, 2N497 Series, 2N734 Series, 2N738 Series, 2N1564 Series, 2N1572 Series, 2N1586 Series — Logic and Medium Power Driver 2N389 Series, 2N1714 Series, 2N1717 Series, 2N1722 Series — Electromechanical Driver	TI 450, TI 451 — High-Speed Transistors 2N706A Series, 2N753 Series, 2N1252 Series — High Speed 2N726 — PNP High Speed 2N696 Series, 2N702 Series — Medium Speed J-460 Series, 2N337 Series — Low Speed	2N696 Series, 2N1252 Series, 2N1508 Series — Driver	2N337 Series —A 2N342B Series—D 2N389 Series —P 2N497 Series —D 2N726 —A 2N734 Series —A 2N738 Series —A 2N1047 Series—P 2N1564 Series—A 2N1572 Series—A 2N1714 Series—P 2N1718 Series—P 2N1722 —P A—Amplifier P—Power D—Driver or Medium Power
SOLID CIRCUIT* **Semiconductor Networks**		Type 502 bistable multivibrator and custom designs for logic circuits	Type 502 Set-reset Flip-Flop	
SILICON DIODES	1N2175 (Photo) LS-222 (Photovoltaic), LS-223 (Photovoltaic) — Readout Devices	C 01 — Low Cost 1N650, 1N651, 1N652, 1N653 — Gallium Arsenide Tunnel Diodes 1N914 Series — High Speed	C 01 — Low Cost 1N650, 1N651, 1N652, 1N653 — Gallium Arsenide Tunnel Diodes 1N914 Series — High Speed	1N746 Series — Reference 1N1816 Series — Power Regulators
SILICON RECTIFIERS	TI-010, TI-025, TI-050 — Controlled Rectifiers			1N253 Series, 1N538 Series, 1N1124 Series, 1N1614 Series — General Purpose Rectifiers 2N1595 to 2N1604 — Controlled Rectifiers
CAPACITORS	*tan-TI-cap** Solid tantalum electrolytic capacitors—type SCM—203 standard ratings—6v to 35v—1 µf to 330 µf			
RESISTORS	CG ⅛ Hard Glass Hermetic—Precision Film—Standard Resistance Values from 24.9 ohms to 18.2 K CG ¼ Hard Glass Hermetic—Precision Film—Standard Resistance Values from 24.9 ohms to 82.5 K ⅛ watt to 2 watt—MIL-Line—Precision Film—Standard Resistance Values from 10 ohms to 50 meg Ω ⅛ watt to 2 watt—Molded—Precision Film—Standard Resistance Values from 10 ohms to 45 meg Ω			

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IRE People

Tore N. Anderson (S'47–A'49–SM'55), executive vice president of FXR, Inc., Woodside, N. Y., has been named president of the firm. He succeeds Henry Feldman, the founder, who moves into the newly created post of board chairman.

T. N. Anderson

Formerly Vice President and Director of engineering at Airtron, Inc., a division of Litton Industries, he came to FXR last January as assistant to the president. He became executive vice president and general manager in April, and was elected to the board of directors in July.

He is Chairman of the Waveguide Standardization Committee of the Electronic Industries Association, and is a consultant to the Defense Department's Advisory Group on Electron Parts. He recently participated in the Ulm, Germany, meeting which was preparing international standards for waveguides and waveguide connectors. As a result of this meeting, he became head of the secretariat of the waveguide committee for the International Electrotechnical Commission.

Mr. Anderson was Chairman of the Northern New Jersey Section and organized the Chapter's Professional Group on Microwave Theory and Techniques. He is now a member of the Administrative Committee and Vice Chairman of the Group. He is also a member of the American Physical Society and the American Institute of Electrical Engineering, and a member of the Tau Beta Pi and Mu Alpha Omicron honor societies. He received the B.S. degree from Cooper Union, New York, N. Y.

❖

The appointment of **Edward J. Bacon** (M'53), as Head of the Electronics Department at Washington Technological Associates, Rockville, Md., was recently announced.

E. J. Bacon

He comes to WTA directly from Emerson Research Laboratories, and was earlier employed at Diamond Ordnance Fuze Laboratories and Radio Corporation of America. He earned both the B.S. (1946) and M.S. (1947) degrees in Electrical Engineering at Massachusetts Institute of Technology, Cambridge.

He has specialized in FM-CW and short range pulse radar systems. For the U. S. Signal Engineering Laboratories, he created and developed the AN/APN-100 Radar Altimeter, a significant innovation in the field of accurate airborne altimetry. He was also responsible for the development of a radar altimeter required by the Federal Aviation Administration for an instrumented landing system, and contributed to the design of altitude sensing devices for the "Hound Dog" missile and a proximity fuze for the "Corvus" missile needed by the U. S. Navy Bureau of Ordnance.

While Chief of the Air-Target Fuzing Section at Diamond Ordnance Fuze Laboratories, he guided the development and fabrication of proximity fuzing systems for the "Terrier," "Sparrow" and "Tartar" missiles, and was successful in improving fuze performance for increased reliability, immunity to countermeasures and absolute range cut-off.

❖

John Brinda, Jr. (A'48–M'55), has joined the Remington Rand Univac Military Division, St. Paul, Minn., as supervisor of a new reliability training program.

J. Brinda, Jr.

He was formerly a research engineer at the American Institute for Research, Pittsburgh, Pa. He received the master's degree in electrical engineering from the University of Pittsburgh in 1952, and was an assistant professor of electrical engineering there from 1952–1959. In his new job, Mr. Brinda is setting up a training program to show Univac engineers how to improve the reliability of their designs.

❖

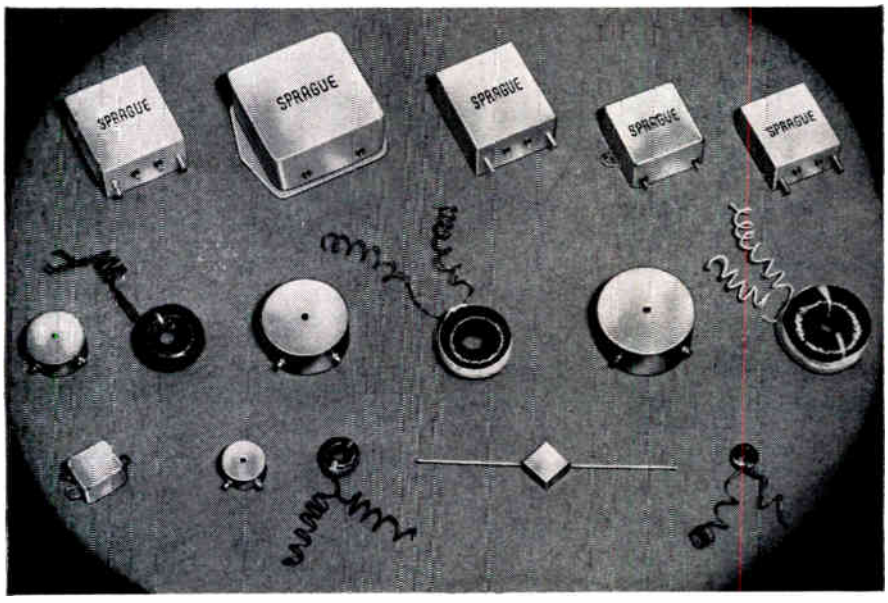
John Basarab, Jr., (S'50–A'52–M'57), who joined Lockheed Electronics Company four years ago as a design engineer, has been named supervisory engineer in that company's Shipboard Electronics Department, Military Systems Division.

He assumes engineering responsibility for some of the division's major Navy contracts, including those concerned with the Regulus Guidance System, Gunfire Control Systems, and various radar equipments.

As senior engineer and project engineer in the Shipboard Electronics Department (the positions he held previous to his present promotion) his work has been concerned primarily with design and develop-

(Continued on page 72A)

Broadness of Sprague's Line of Precision Toroidal Inductors Offers Standard Units for Practically Every Application



DESIGNED FOR USE in commercial, industrial, and military apparatus, Sprague Precision Toroidal Inductors are customarily supplied to the close inductance tolerance of ±1%. The broad line of Sprague Precision Toroidal Inductors includes such styles as open coil, plastic-dipped, rigid encapsulated inductors with tapped or through-hole mounting, and hermetically-sealed inductors.

All styles, with the exception of the open coil type construction, meet the appropriate requirements of Military Specification MIL-T-27A.

Sprague Precision Inductors are manufactured in modern plants which are equipped with the most up-to-date facilities for winding, processing, and testing the cores. Production instruments used in the manufacture of Sprague inductors are calibrated periodically to assure desired levels of accuracy. Quality control and inspection departments, which function independently of each other, maintain close surveillance over all production operations.

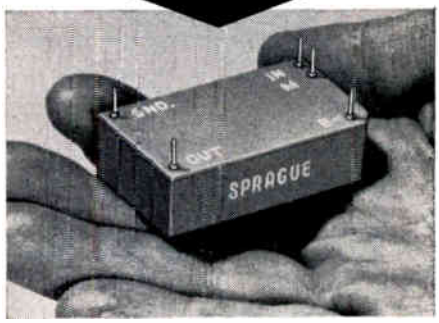
Several core permeabilities may be obtained in each of the five basic sizes of Sprague inductors to give the circuit designer the optimum selection of desired Q and current carrying abilities. Further, each of the core sizes is available with several degrees of stabilization. Inductors made with cores which have not been subjected to the stabilization process exhibit low inductance drift with time and have a low temperature coefficient of inductance. Where a greater degree of permanence of characteristics is required, cores with two different stabilization treatments can be used for most types of inductors.

All standard inductors by Sprague may be operated over the temperature range of −55 C to +125 C. Temperature cycling of finished inductors is a standard production procedure in order to equalize internal stresses and insure permanence of electrical characteristics.

In those cases where the extensive line of Sprague standard inductors is unsuitable for a particular application, the Special Products Division of the Sprague Electric Company will be glad to work with you to custom-tailor designs to meet specific customer requirements.

For detailed information on standard ratings, package sizes, Q, current carrying abilities, properties, etc., write on company letterhead for portfolio of engineering data sheets on precision toroidal inductors to Technical Literature Section, Sprague Electric Company, 235 Marshall Street, North Adams, Massachusetts.

Something NEW in counting techniques!



Sprague type 73Z1 core-transistor DECADE COUNTERS

Here is a simple yet versatile, low-cost yet reliable component for counter applications. Counting to speeds of 10 kc, the 73Z1 decade counter provides an output signal for every 10 input pulses, then resets in preparation for the next cycle. For higher counting, two or more counters may be cascaded. Typical characteristics are shown below.

CHARACTERISTIC	INPUT	OUTPUT
Amplitude	1.5 to 8 volts	6.5 volts min.
Pulse Width	1 μsec min.	50 μsec nom.
Impedonce	100 ohms	20 ohms

Utilizing two rectangular hysteresis loop magnetic cores and two junction transistors to perform the counting operation, the 73Z1 counter is encapsulated in epoxy resin for protection against adverse environmental conditions. It has five terminals −B+ (12v ±10%), input, output, ground, and manual reset.

The 73Z1 counter is available as a standard item. However, "customer engineered" designs can be supplied when other counting cycles, speeds, and package configurations are required for special applications.

For complete technical data or application assistance on the 73Z1 counter or other Sprague components, write to Special Products Division, Sprague Electric Co., 235 Marshall St., North Adams, Mass.

SPRAGUE®
THE MARK OF RELIABILITY

IRE People

(Continued from page 70A)

ment of components and subsystems for missile guidance.

Before joining Lockheed Electronics, he served as an electrical engineer at Chatham Electronics in Livingston, where he was involved in testing components and systems.

He is a native of Rahway, N. J., holds the B.S. and M.S. degrees in electrical engineering from Newark College of Engineering, Newark, N. J. He served as an aerial engineer in the Air Force during World War II and was assigned to troop carrier duty in the China-Burma-India theater.

Mr. Basarab is a member of the Alumni Association of Newark College of Engineering.

❖

Gerald M. Clarke (M'59), has been appointed Assistant to the Product Manager of the Amplifier Division of Magnetico, Inc., L. I., N. Y.

G. M. Clarke

A graduate of Manhattan College, New York, N. Y., he was a former Product Engineer at the Sperry Gyroscope Company, Great Neck, N. Y.

He will concentrate on Magnetico's advanced design of solid state devices for precise system control, particularly in the transistorized servo amplifier area.

❖

Paul C. Constant, Jr. (M'48–SM 54), has been promoted to Head of the Systems Engineering Section, Midwest Research Institute, Kansas City, Mo. according to a recent announcement.

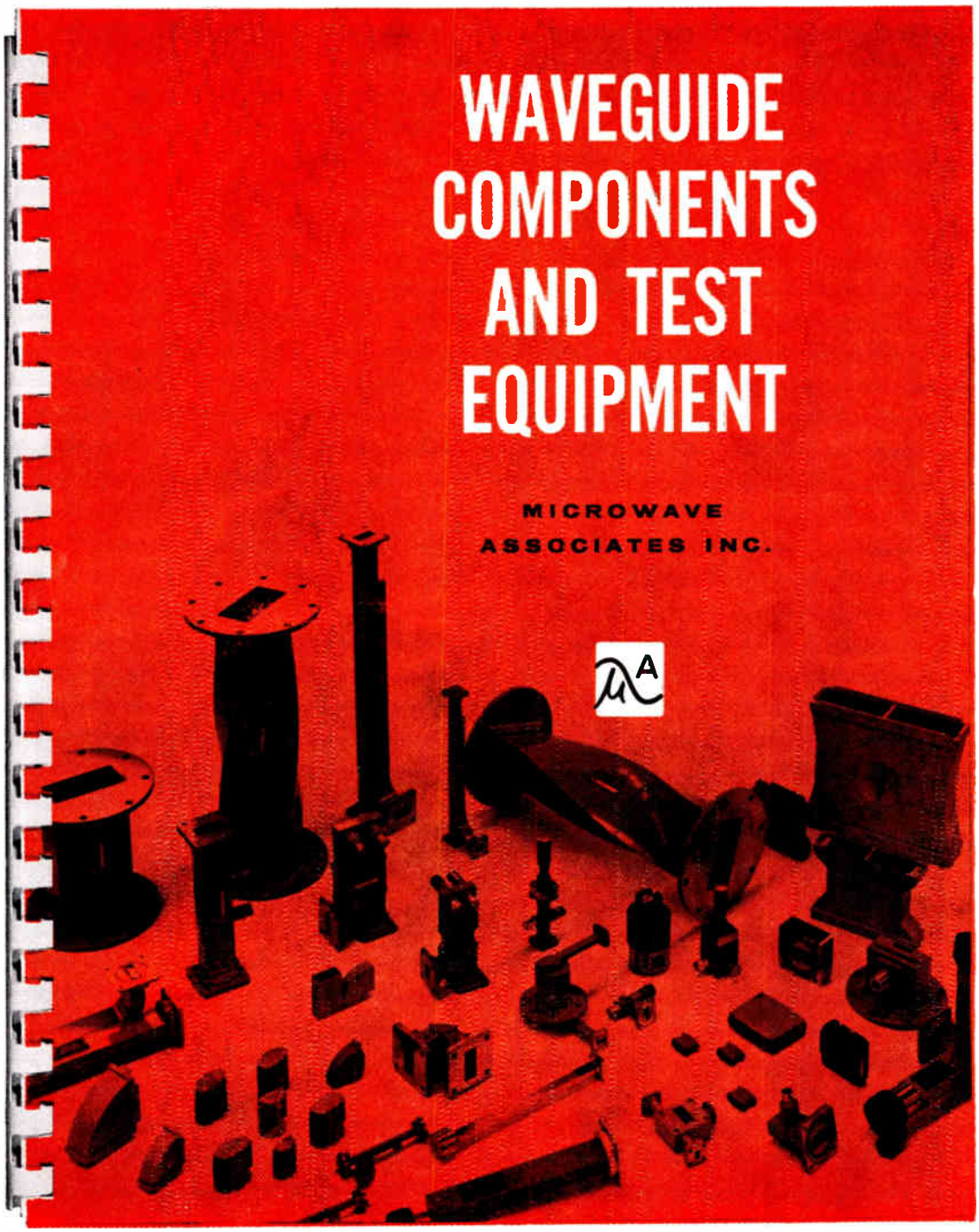
P. C. Constant, Jr.

He has been on the MRI staff since 1948 and has been a Senior Engineer since 1958. He received the B.E.E. degree in 1943 from the University of Minnesota, Minneapolis, and in addition to graduate studies there, he received the M.A. degree in 1956 from the University of Kansas City. He also is an instructor in mathematics at the latter school.

From 1943 to 1946, he was a communications officer in the Army. He was an assistant instructor at the University of Minnesota from 1946–1947, and a filter design engineer, Railway Radio Telephone Telegraph Co., Kansas City, from 1947–1948.

Mr. Constant is the author of nine recent technical articles. He has served as

(Continued on page 76A)



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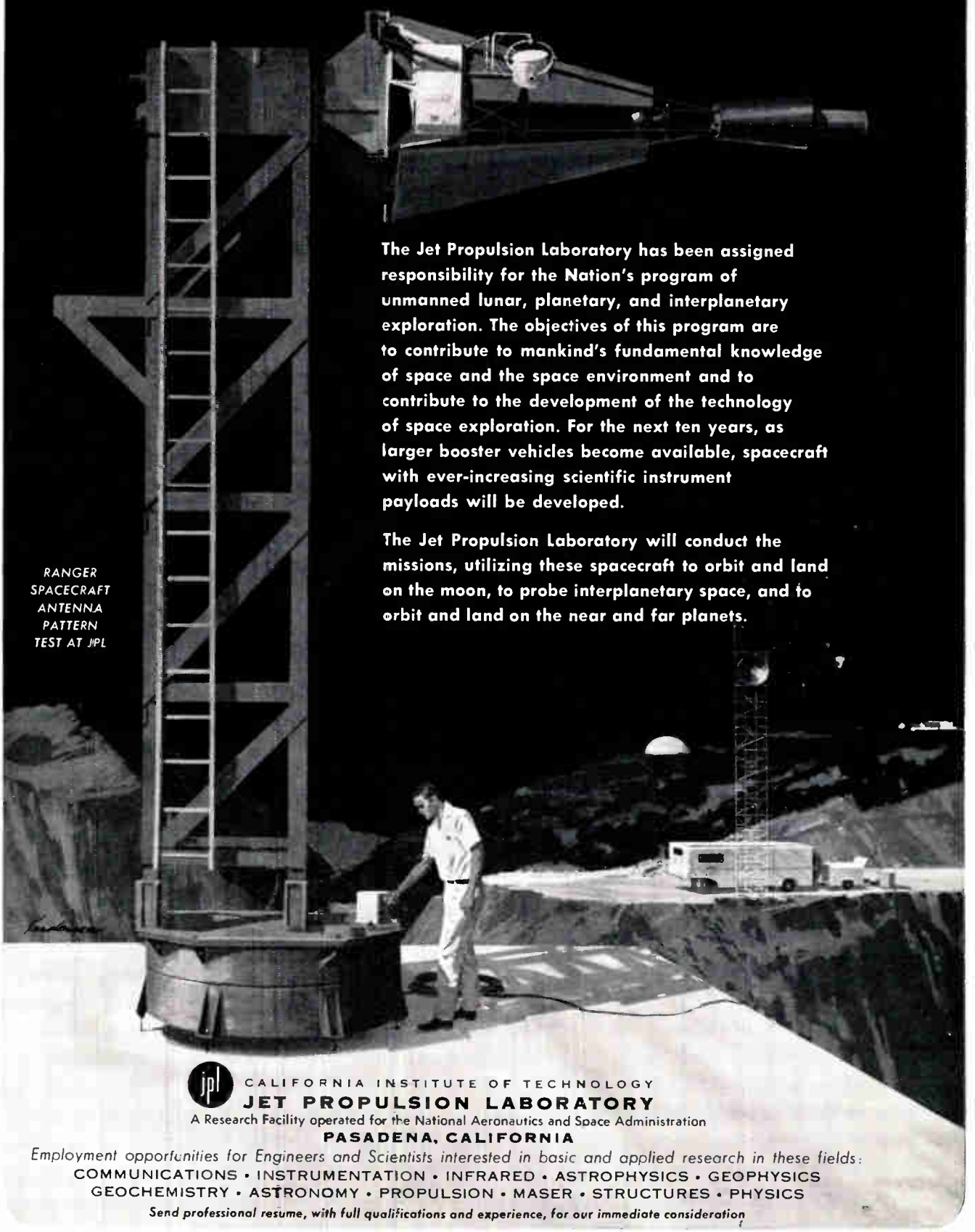

RANGER SPACECRAFT ANTENNA PATTERN TEST AT JPL

The Jet Propulsion Laboratory has been assigned responsibility for the Nation's program of unmanned lunar, planetary, and interplanetary exploration. The objectives of this program are to contribute to mankind's fundamental knowledge of space and the space environment and to contribute to the development of the technology of space exploration. For the next ten years, as larger booster vehicles become available, spacecraft with ever-increasing scientific instrument payloads will be developed.

The Jet Propulsion Laboratory will conduct the missions, utilizing these spacecraft to orbit and land on the moon, to probe interplanetary space, and to orbit and land on the near and far planets.

jpl

CALIFORNIA INSTITUTE OF TECHNOLOGY

JET PROPULSION LABORATORY

A Research Facility operated for the National Aeronautics and Space Administration

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Employment opportunities for Engineers and Scientists interested in basic and applied research in these fields:

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Send professional resume, with full qualifications and experience, for our immediate consideration

look into Panoramic's new SPA-4a exclusive features for more reliable spectrum analysis 10 mc to 44,000 mc

2 to 4 TIMES THE USABLE SENSITIVITY

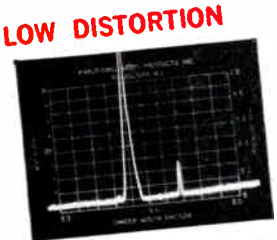
Lower internal noise enables analysis of even smaller signals than before (see chart)... accurate measurement of more highly dispersed energies, as typified by extremely narrow pulsed signals.

BAND	RF SENSITIVITY*
1- 10 — 420 MC	−100 to −110 dbm
2- 350 — 1000 MC	— 95 to −105 dbm
3- 910 — 2200 MC	−100 to −110 dbm
4- 1980 — 4500 MC	— 90 to −100 dbm
5- 4.5 — 10.88 KMC	— 90 to −100 dbm
6-10.88 — 18.0 KMC	— 85 to −100 dbm
7- 18.0 — 26.4 KMC	— 70 to — 90 dbm
8- 26.4 — 44.0 KMC	— 60 to — 85 dbm

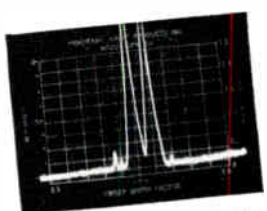
*measured when signal and noise equal 2x noise

EXCEPTIONALLY LOW DISTORTION

Reduced threshold allows SPA-4a to operate at smaller input signal levels (and attenuated larger ones). Unretouched screen photos show how this permits virtually spurious-free measurement—over a wide dynamic range—of harmonics, in-band distortion, and other weak signals in the presence of strong ones.



Extended dynamic range comparison of 2 signals on SPA-4a. Larger is + 15 db over full scale log. Smaller is at −28 db on scale or −43 db from larger. Note exceptional freedom from spurious. (Photo not retouched)

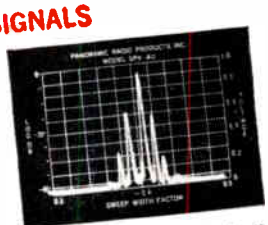


Distortion analysis illustrates SPA-4a wide range linearity. Odd-order distortion here is measured more than 50 db below level of 2 main tones (deflected 20 db above full scale). Photo unretouched.

RESOLVES MORE CLOSELY SPACED SIGNALS

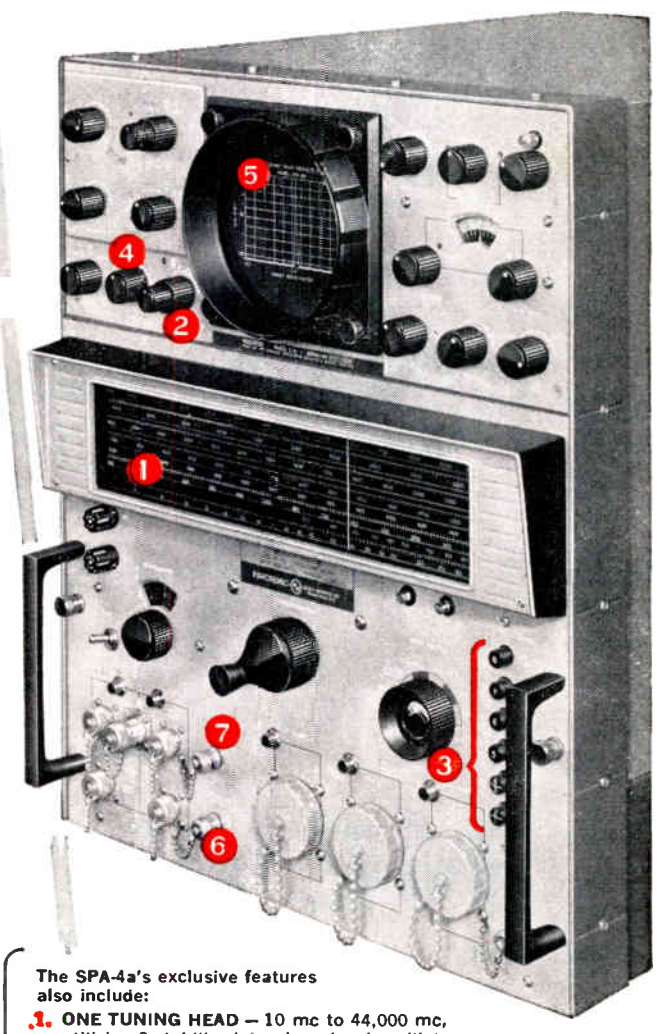
Lower hum means improved repeatability for narrow band analysis of closely spaced signals, enables more highly magnified analyses with improved minimum useful dispersions. Unretouched screen photos illustrate SPA-4a's exceptional stability and resolution capability.

Narrow band 20 kc dispersion analysis shows unique resolution capability. Here, a 1000 mc FM signal with 2 kc modulation is seen near first carrier null. Photo unretouched.



Highly resolved analysis in X band. Carrier frequency = 10.8 kmc. Sidebands due to modulation at 20 kc. (Unretouched)

dependable CERTIFIED SPECIFICATIONS for accurate data



The SPA-4a's exclusive features also include:

1. **ONE TUNING HEAD** — 10 mc to 44,000 mc, utilizing 3 stabilized, low hum local oscillators (1 HF triode and 2 klystrons). Fundamentals to 11 kmc. Direct reading with ± 1% accuracy.
2. **TWO INDEPENDENT FREQUENCY DISPERSION RANGES:** Continuously adjustable; 0-70 mc with exceptional flatness, stable 0-5 mc for narrow band analysis. Both swept local oscillators operate on fundamentals only for spurious-free analysis.
3. **PUSH-BUTTON FREQUENCY RANGE SELECTOR.**
4. **ADJUSTABLE IF BANDWIDTH 1 KC to 80 KC.**
5. **3 CALIBRATED AMPLITUDE SCALES** — 40 db log, 20 db lin, 10 db power.
6. **SYNCHROSCOPE OUTPUT WITH 40 DB GAIN.**
7. **ACCURATE MEASUREMENT OF SMALL FREQUENCY DIFFERENCES:** Self-contained marker oscillator, modulated by a calibrated external generator, provides accurate differential marker pips as close as 10 kc.

Important as these advantages are, there are many more.

Easy to use, too... human engineered for simple operation, component accessibility.

The advanced new SPA-4a is unmatched for visually analyzing FM, AM and pulsed signal systems —instabilities of oscillators —noise spectra—for detection of parasitics—studies of harmonic outputs, radar systems and other signal sources.

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IRE People

(Continued from page 72A)

chairman of the Kansas City Section, 1957–1958; as chairman of the Mid-America Electronics Conference, 1959; and as a member of the National Committee on Electronic Computers since 1959. He is a registered professional engineer in Missouri and Kansas, and he also belongs to the Missouri Society of Professional Engineers, the National Society of Professional Engineers, Society of Industrial and Applied Mathematics, Kansas City Applied Mathematical Society, and the Central Simulation Council.

❖

Murray G. Crosby (A'25–M'38–SM'43–F'43), president of Crosby-Teletronics Corporation, and a leading authority in the communications field, has been appointed to the government's Patent Advisory Committee, it was announced in Washington by Secretary of Commerce F. H. Mueller.


M. G. CROSBY

Members of the committee, who advise the Secretary on measures affecting the operation of the United States patent system, include representatives of the legal profession, and leading figures from industry and science.

Mr. Crosby holds more than 180 patents in the field of communications and his system for transmitting stereophonic broadcasts by FM stations is presently under consideration by the Federal Communications Commission for permanent broadcast licensing.

❖

Roger M. Daugherty (A'42–M'45–SM'48), has been appointed general manager of the new Farmingdale, N. J., plant of Reeves Instrument Corporation.


R. M. DAUGHERTY

Before joining Reeves, he had been vice president of engineering of The Hammarlund Manufacturing Company, Inc., vice president and general manager of the Boonton Molding Company, and executive vice president and general manager of J. H. Bunnell and Company.

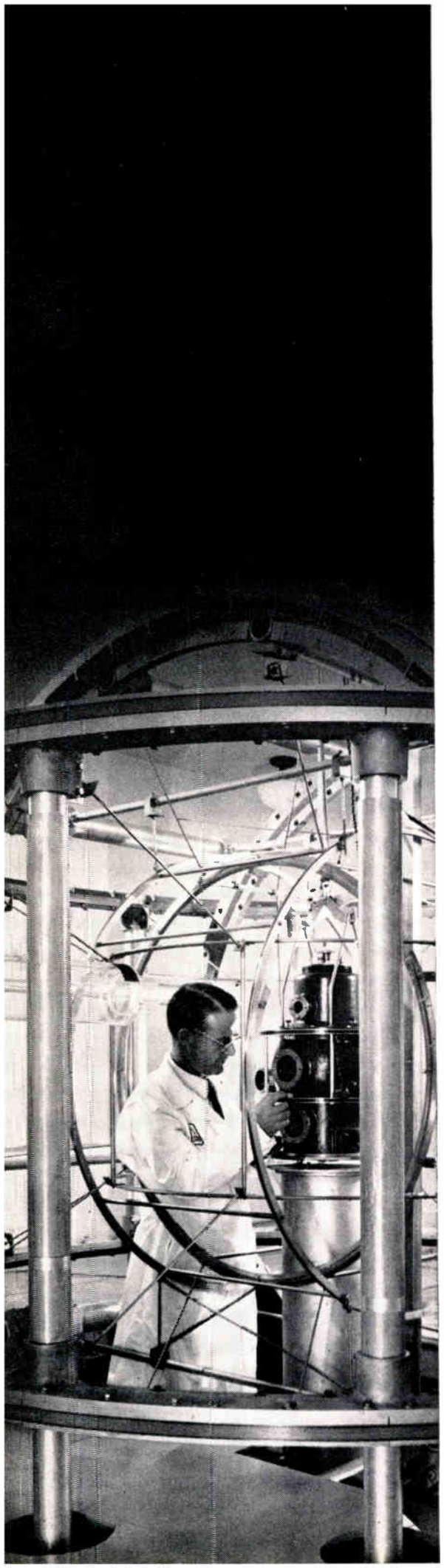
Mr. Daugherty is a member of the Professional Groups on Engineering Management and on Vehicular Communication.

❖

Leon D. Findley (M'57), has joined the Remington Rand Univac Military Department, St. Paul, Minn., as staff con-

(Continued on page 79A)

One of a series.



Why we eliminated the earth's magnetic field... almost

In an isolated laboratory in southwestern Ohio, GM Research scientists have reduced the earth's magnetic field to one ten-thousandth of its usual strength. This is about as weak as the interplanetary field detected by the Pioneer V solar satellite.

Why neutralize the earth's field? To perform with precision one of the more fundamental experiments in magnetism — measuring the Einstein-DeHaas effect. The measurement is simple in concept, experimentally difficult because of the tiny forces involved. It is made by suspending a ferromagnetic rod in a nearly field-free environment . . . magnetizing the rod . . . then measuring the effect (how much the rod rotates) when this known magnetization is reversed.

The beauty of the experiment is that the resulting values can be related directly to the motions of electrons in the rod. The values indicate the large portion of magnetization due to the *spin* of electrons . . . and the slight, but theoretically important, remaining portion due to *orbital* motion of electrons.

These measured values are helping scientists form a better understanding of the perplexing phenomenon — ferromagnetism. Currently being pursued in cooperation with the Charles F. Kettering Foundation, this long-standing project is one of the ventures in basic research of the General Motors Research Laboratories.

General Motors Research Laboratories

Warren, Michigan

Gyromagnetic Ratios		
Iron	***a*** *1.92*	***b*** *1.90*
Cobalt	*1.85*	*1.83*
Nickel	*1.84*	*1.83*
Supermalloy	*1.91*	*1.91*

Comparison of (a) gyromagnetic ratios measured in the new Kettering Magnetics Laboratory with (b) corresponding ferromagnetic resonance measurements. These ratios would equal 2 if magnetization were due only to electron spin, or 1 if due only to orbital electron motion.

System of Helmholtz coils used to neutralize earth's magnetic field.

IRE People

(Continued from page 76A)

L. D. FINDLEY

sultant to the manager of the NTDS (Naval Tactical Data System) department.

He was formerly head of the systems engineering section at the Midwest Research Institute, Kansas City, Mo. From 1948–50, he was employed by Engineering Research Associates, St. Paul, Minn., as a development engineer, and later as a project engineer.

Mr. Findley holds the B.S. and M.S. degrees in electrical engineering from Kansas State University, Manhattan, Kans.

❖

E. I. GREEN

Estill I. Green (A'27–M'36–SM'43–F'55), executive vice president of Bell Telephone Laboratories, retired on November 30, 1960, after a distinguished career of 39 years with the Bell System.

He has won nationwide professional recognition not only for his engineering achievements, but also for his contributions in the field of engineering management and administration. He has been granted more than 70 patents for his inventions and is the author of many authoritative articles on scientific subjects and on the management and evaluation of technical personnel.

He began his telephone career in 1921 with the American Telephone and Telegraph Company's development and research department. There he engaged in transmission studies and the planning of new transmission developments, especially the carrier telephone and telegraph systems which were just then getting started. He took a leading part in the planning of the coaxial system, which now provides a major part of the Bell System long distance telephone and television network. He also made important contributions to the standardization of carrier system frequency allocations which through the years afforded much economy in development and manufacturing effort.

After the merger of the A.T. and T.'s development and research department with Bell Telephone Laboratories in 1934, he continued his transmission planning activities at the Laboratories.

As the U. S. moved into World War II, he took over broad responsibilities for the development of apparatus, mostly in the microwave range, for the testing of radar

(Continued on page 80A)

IRE People

(Continued from page 79A)

systems. Under his general direction, some 250 designs of radar test gear were developed, representing about half of the designs required for the entire U. S. war effort.

Following the war, he returned to transmission work for the Bell System and served successively as assistant director of transmission development and as director of transmission apparatus development. In the latter post, he was responsible for the development of a wide variety of system components and parts, including miniaturized electronic components compatible in size and performance with the newly-invented transistor.

In 1953, he was appointed director of military communications systems, with broad responsibilities for both planning and development work in that area. He became vice president—systems engineering in 1955 and for the next three and a half years headed that part of the Laboratories organization engaged in the systematic analysis and planning for future developments.

Mr. Green assumed the post of executive vice president in January, 1959.

A native of St. Louis, Mo., Mr. Green attended grammar and high schools in that city. He received the A.B. degree from Westminster College, Fulton, Mo., in 1915. After a year of graduate study in mathematics, English and languages at the University of Chicago, Chicago, Ill., he returned to Westminster College as professor of Greek. Simultaneously he taught a course in Greek at William Woods College, also in Fulton.

In May, 1917, he enrolled in an officer's training course at Fort Riley, Kans., and was commissioned as Second Lieutenant. He served overseas with the 89th Division and took part in the St. Mihiel Drive and the Meuse-Argonne Offensive. He was commissioned a Captain in October, 1918 and saw six months of occupation duty in Germany following the armistice.

After his discharge in 1919, he entered Harvard Engineering School, Cambridge, Mass. and was graduated with the B.S. in E.E. degree (summa cum laude) in 1921. He joined the A.T. & T. Company immediately after graduation.

Mr. Green is a Fellow and Director of the American Institute of Electrical Engineers and a Fellow of the Acoustical Society of America, and the American Association for the Advancement of Science. He has served as a member or chairman of many AIEE and IRE committees. He is also a member of the American Physical Society, the Operations Research Society of America, the Harvard Engineering Society, the Newcomen Society in North America, and the Research and Development Planning Council of the American Management Association. For a number of years he was a member of the Engineering Foundation Board.

He has been active on Department of Defense committees, including Technical Advisory Panel on Electronics, Ad Hoc Committee on Military Electronics Research, and Advisory Group on Electronic Parts.

From 1946 to 1958, he was chairman of a subcommittee of the American Standards Association which produced a new glossary comprising definitions of about 1780 technical terms used in communications.

In 1956, he was awarded the honorary Doctor of Science degree by Westminster College, and delivered the commencement address on "Science and Liberal Education."

He is a director of the United-Carr Fastener Corporation of Cambridge, Mass.

Mr. Green is presently engaged in consultation on engineering management, as well as other professional activities.

❖

Charles P. Ginsburg (A'48–M'55–SM'59), of Ampex Corporation, who led the development of the Videotape television recorder, has received the coveted "Valdemar Poulsen Gold Medal" from the Danish Academy of Technical Sciences, it was recently announced.

He is the first native-born American to receive the award, which has been given only six times since its inception in 1939. The Gold Medal was presented to Mr. Ginsburg by Carl Schroder of Copenhagen, vice president of the Danish Academy of Technical Sciences, in special ceremonies

(Continued on page 85A)

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with continuously variable current limiter...

These new Regatrans are sparing only of space . . . delivering super-regulated, virtually ripple-free d-c power with the instant start-up and very high reliability of solid-state circuitry . . . and offering a group of features hitherto unprecedented in d-c power supplies of this size.

REGULATION, LINE OR LOAD, 0.1% OR 0.01 V

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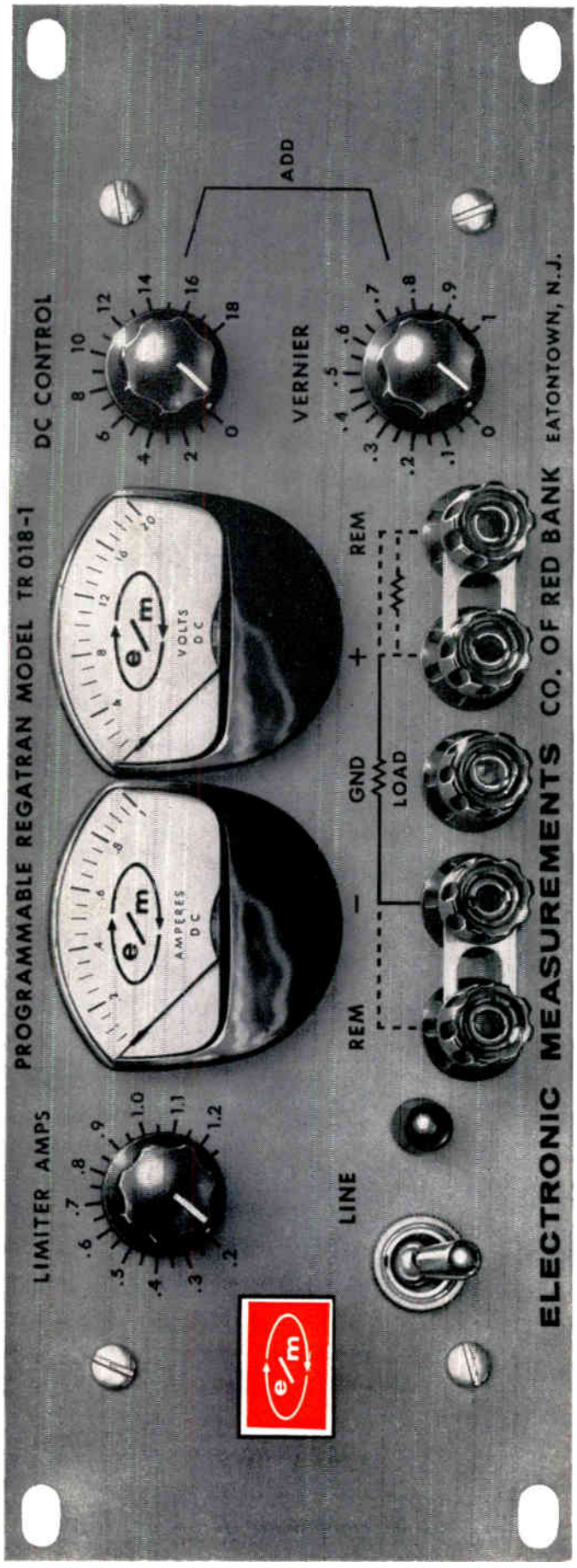
	VOLTS	AMPS	
TR212A	0-100	0-100 MA	250 μv
TR018-1	0-18	0-1 AMP	150 μv
TR036-0.2	0-36	0-200 MA	150 μv

For a closer look, ask your local Electronic Measurements representative for a copy of Specification Sheet 5000 . . . or write direct.



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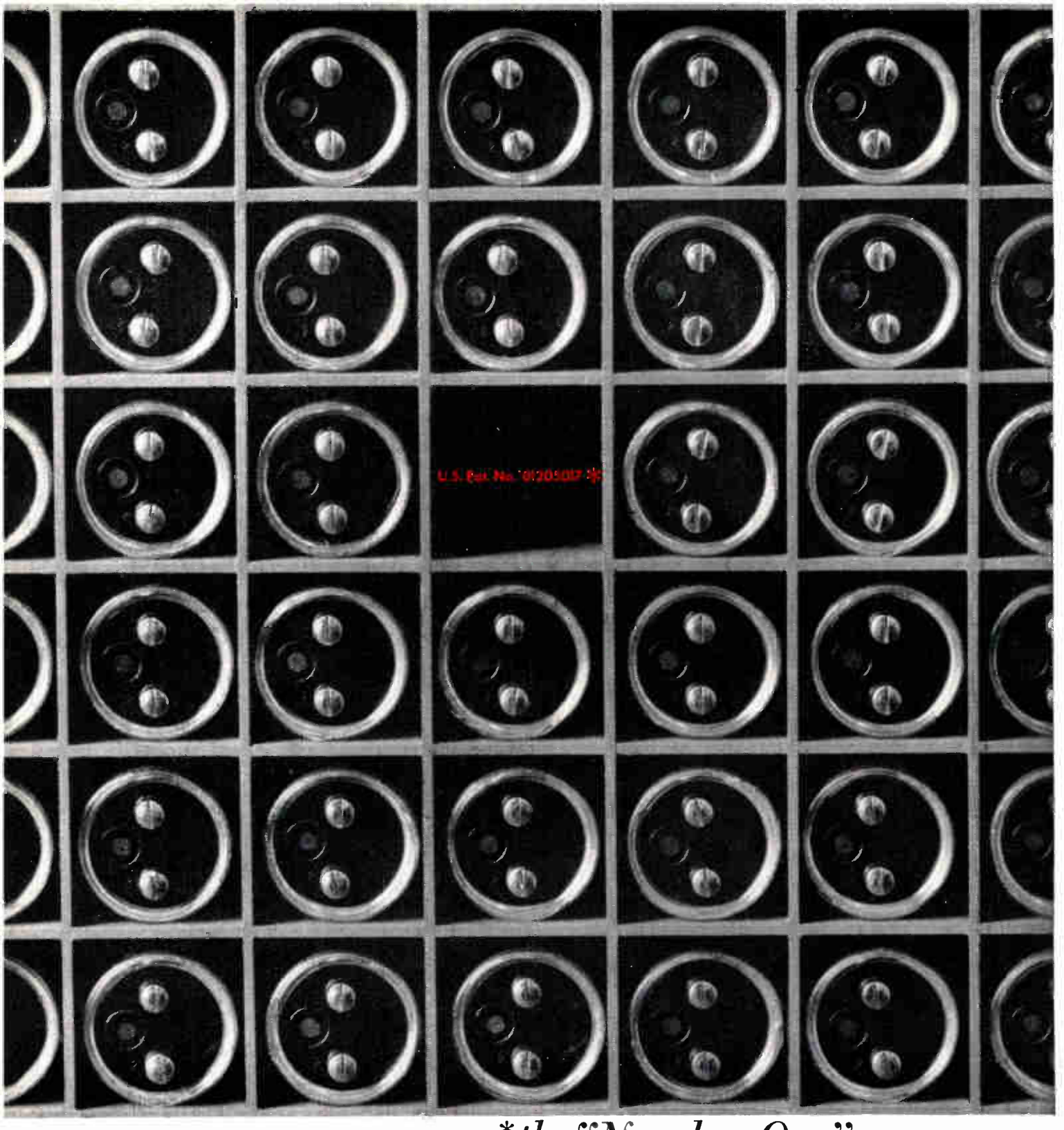

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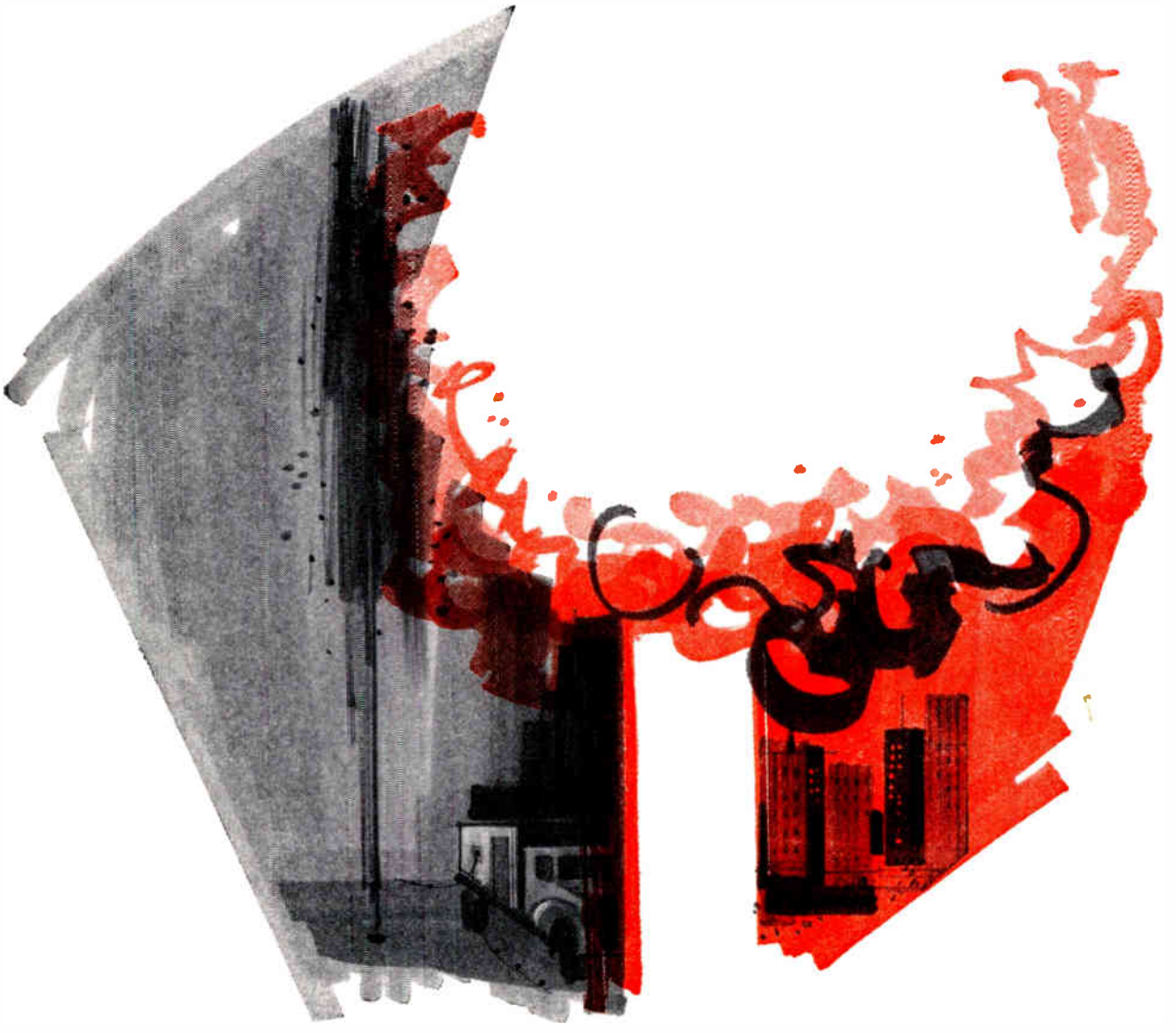

DOODLEBUGS AND BOMBS

As far as the earth is concerned, one explosion is much like another. Geophysical oil-exploration "shots" and bomb blasts both involve common seismic shock detection and assessment techniques. Since 1951 more Dresser Electronics' "doodlebugging" instruments have been in use around the world than all competitive equipment combined.

For the Department of Interior Dresser Electronics is now proud to supply seismic refraction amplifier systems for the Major Crustal Studies Program.

Dresser Electronics systems engineering is also at work in airborne telemetry . . . civil defense . . . process control . . . anti-submarine warfare . . . mobile hospitals—projects throughout military, industrial and defense areas.

The unique approach of this systems-oriented company may solve your problem.

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DRESSER ELECTRONICS

SIE DIVISION / ONE OF THE DRESSER INDUSTRIES

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IRE People

(Continued from page 80A)

on November 23, 1960, in San Francisco, Calif.

He was cited by the academy for his "guiding spirit and principal participation in the development of the 'video tape' recorder by Ampex Corporation—an outstanding achievement . . . which is well known to magnetic recording and television engineers all over the world." The academy, which administers the "Valdemar Poulsen Gold Medal Foundation," noted that its decision is supported by the IRE and the Society of Motion Picture and Television Engineers.

Mr. Ginsburg received the Gold Medal, officially, November 23, the birthday of Valdemar Poulsen, discoverer of magnetic recording.

The Valdemar Poulsen Gold Medal Award was established in Denmark in 1939 to be awarded each year on the birthday of Valdemar Poulsen to a radio engineer or scientist in recognition of important contributions to the development of the science or art of radio communications or magnetic registration. Winners of the renowned science medal are selected on the basis of recommendations from competent institutions in Denmark and abroad.

The first Gold Medal was presented to Valdemar Poulsen, himself, on the occasion of his 70th birthday, November 23, 1939. Since that time, the academy points out, it has not been possible to award the medal each year as planned, due to the war and related circumstances.

Mr. Ginsburg joined Ampex in 1952, after serving in various engineering capacities with professional sound services and radio stations in the San Francisco Bay Area. He was graduated in 1948 from San Jose State College, San Jose, Calif., with the B.A. degree in mathematics. He was named a vice president of Ampex Corporation in 1960, and serves as Manager of Advanced Video Development.

In 1957, he was awarded the David Sarnoff Gold Medal by the Society of Motion Picture and Television Engineers. That same year, he also received an Academy of Television Arts and Sciences "Emmy" awarded Ampex for outstanding technical achievement. In 1958, he received the Vladimir K. Zworykin Television Prize, awarded by the IRE.

❖

Curtis R. Hammond (A'47–M'55) has been appointed Commerical Vice President-Market Development for Raytheon Company, it was recently announced.

He has been director of commercial sales development and will continue to work with the firm's manufacturing divisions in maintaining liaison with executives in customer and prospect companies and coordinating joint divisional sales activities.

He was named director of regional commercial administration in 1958 and super-

(Continued on page 86A)

IRE People

(Continued from page 85A)

vised the company's marketing centers across the nation until May, 1960, when he was named director of commercial sales development.

A well-known figure in the industry, he was educated as an electrical engineer at the University of Kentucky, Lexington. He worked with Ken-Rad Tube and Lamp Co., and the General Electric Company from 1933 to 1945 in production and sales engineering capacities. He joined Raytheon's Receiving Tube Division in 1945. From 1950 to 1958, he served as general sales manager for receiving tubes, industrial tubes, cathode ray tubes, and semiconductor products.

An amateur radio operator since 1931, Mr. Hammond is an active broadcaster under the call sign K1JTC.

❖

General Instrument Corporation has announced the appointment of **John L. Herre** (M'57) as Government Sales Manager of its Semiconductor Division. He will direct the sale of General Instrument's semiconductor products—transistors, diodes and rectifiers—to government agencies, and will be responsible for sales of research, development and industrial preparedness programs for the Semiconductor Division.

Prior to joining General Instrument Corporation, he was Sales Manager, Government and Special Accounts, for the Semiconductor Division of the Raytheon Company for two years. Previously, he had been a technical representative to the United States Armed Forces and Manager of Government Sales and eastern industrial sales activities for Philco Corporation.

During World War II, he served in various technical capacities with the United States Air Force. He is a member of the Professional Group on Electron Devices, and the Armed Forces Communications and Electronics Association.

Mr. Heere was educated at the University of Pennsylvania, and University of Chicago, Chicago, Ill.

❖

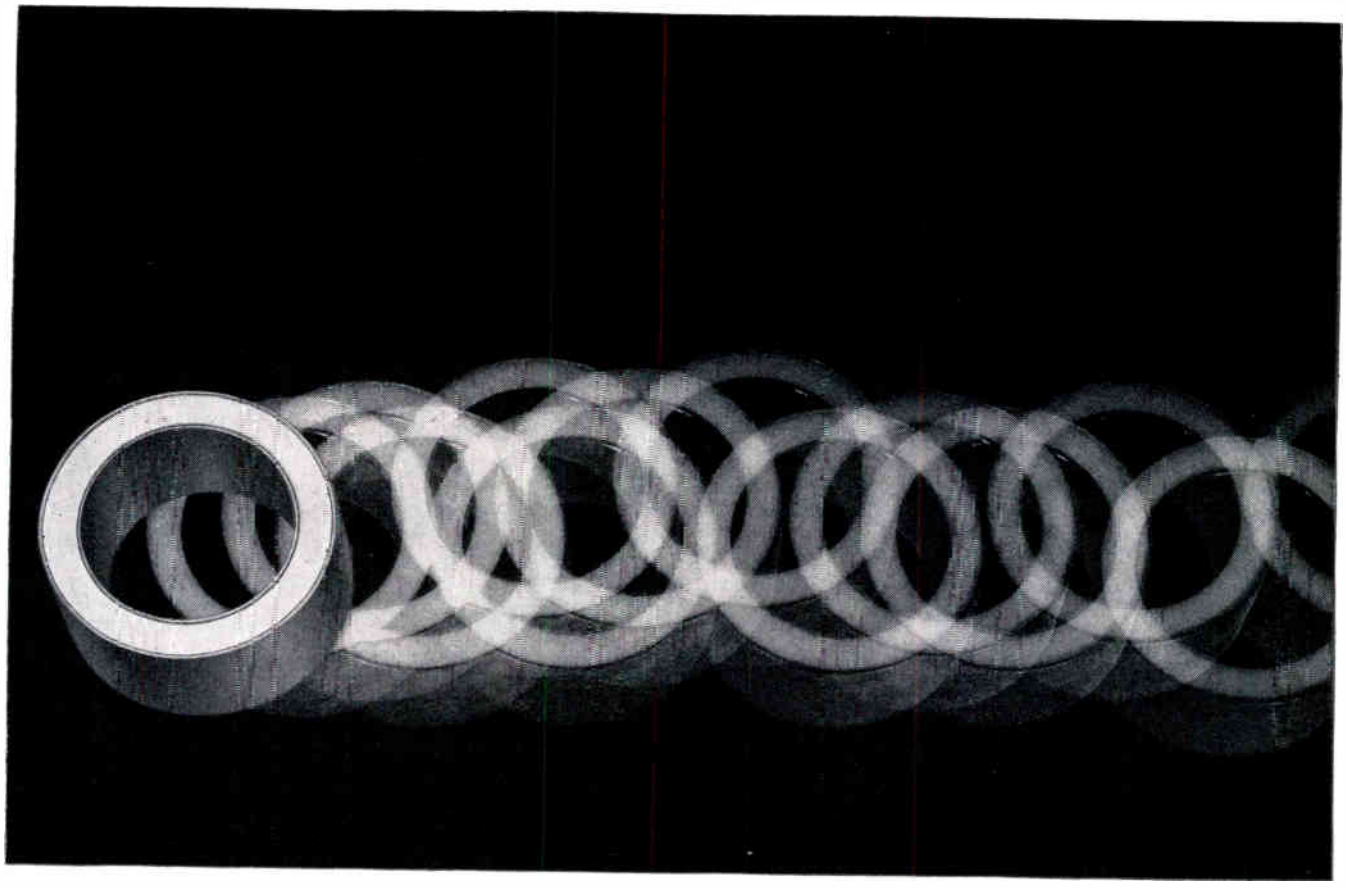
The appointment of **Edmundo Gonzalez-Correa** (M'55) to the newly-created position of manager, microwave department, Special Products Operations, Lansdale Division, Philco Corporation, was recently announced.

E. GONZALEZ-CORREA

In his new position, he assumes over-all responsibility for activities in microwave device and circuit development, engineering, production, testing, and materials development.

He joins the Lansdale Division follow-

(Continued on page 88A)



the strong case for Centricores®

When you're considering magnetic cores it pays to get down to cases. The sturdy aluminum case for Centricores assumes special importance where impact, vibration, heat or mechanical pressure could cause trouble in a control loop you're designing, or where you want to miniaturize an inductive component.

The case is ruggedly rigid, so that you can apply your circuit windings without danger of distorting the core's magnetic properties. And the case is absolutely leakproof. You can vacuum-impregnate Centricores without danger of their damping oil leaking out or foreign matter leaking in. The tightly sealed case also guards against leakage in applications where high ambient temperatures are present, or where Centricores are used in rotating equipment.

Here's a tip on miniaturization. The rugged design of the Centricore case permits use of a thinner gage aluminum that shaves fractions of an inch off their size—fractions that can add up to precious inches where you want to scale down component dimensions. *Centricores are the slimmest magnetic cores on the market.*

Centricores are the most uniform. They give the exact performance you want, from core to core and lot to lot. Their remarkable consistency in insulation, dimensions, squareness, thermal stability and gain is the product of unique quality controls that begin with the very selection of raw materials and extend through final testing.

Write for complete data. Centricores are available from stock from our East and West Coast plants in all standard sizes and magnetic qualities, and in both aluminum and phenolic cases. We will match them within 5 per cent over the entire voltage-current loop, in sets, units or in multiples up to twelve. Write for detailed specifications today.

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IRE People

(Continued from page 86A)

ing four years of service in the Philco Research Division, first as manager of solid state research planning and more recently as executive coordinator of technical programs of the Research Division Staff.

He has been active in the field of solid state devices since 1952. As chief of the Circuit Research Units, Frequency Control Branch, U. S. Army Signal Corps, he directed a group which initiated a study program at the Ft. Monmouth, N. J., Engineering Laboratories, aimed at the application of semiconductor devices in frequency control and switching circuitry. Subsequently, he was placed in charge of the section of the Signal Corps Engineering Laboratories responsible for the device and application engineering aspects of that facility's transistor and diode program.

Prior to 1952, he was engaged in a variety of assignments in education, industry, and overseas government service. As acting director of research and development for the U. S. Civil Communications Section in Japan after World War II, he received a citation for his contributions to the reorganization of the Laboratories of the Ministry of Communications into the largest modern research and development center in the Orient.

Mr. Gonzalez received his undergraduate training at the University of Puerto Rico, Rio Piedras, and holds the M.S. degree in physics from the University of Chicago, Chicago, Ill., and the M.S. degree in electrical engineering from Rutgers University, New Brunswick, N. J. He is a member of Sigma Xi, and the IRE Solid State Circuits Committee.

✣

Philip W. Jackson (A'52–M'57) has been promoted to manager of East Coast laboratories in IBM's Advanced Systems Development Division, it was recently announced.

P. W. Jackson

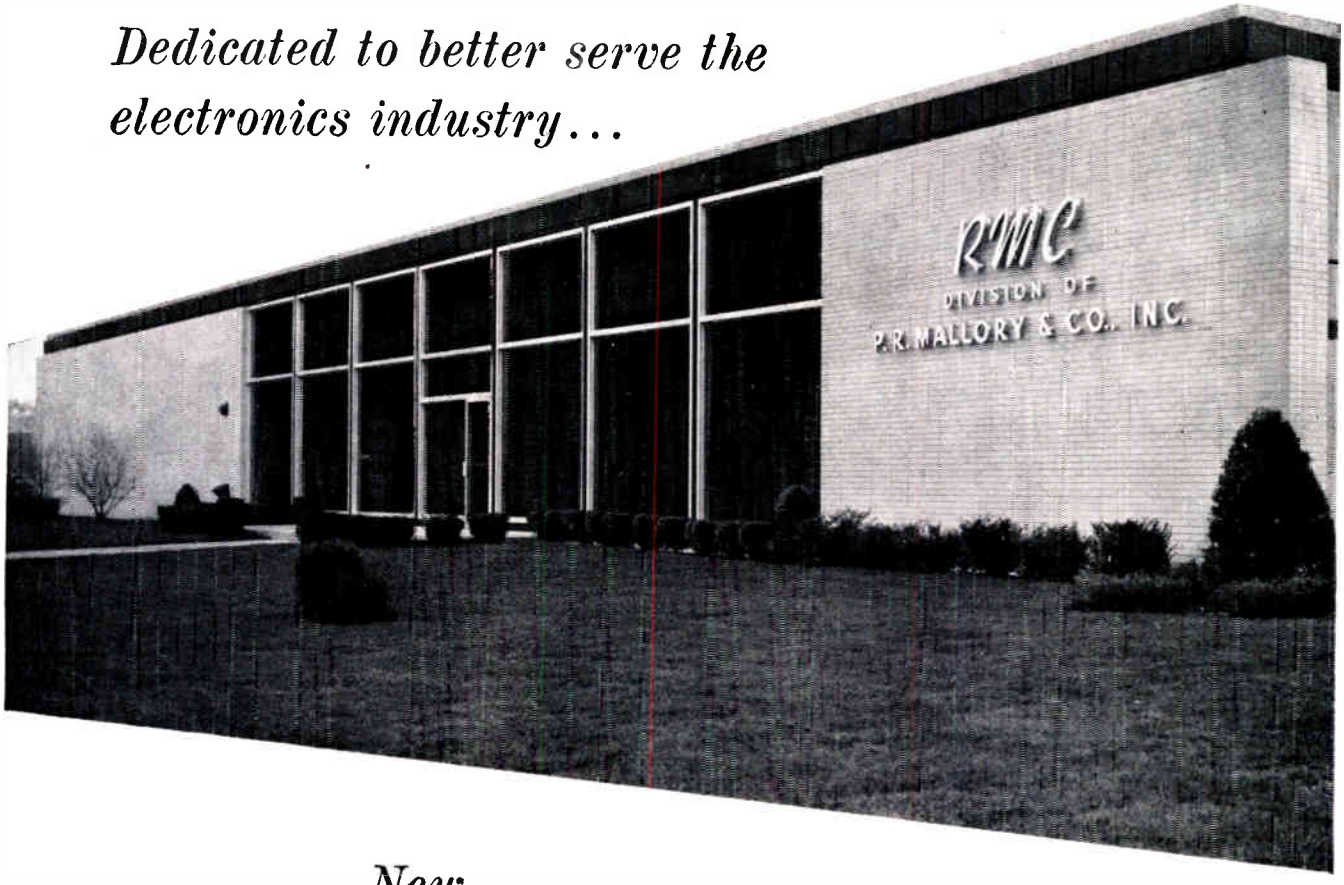
He has been with IBM since 1949, previously was executive assistant to IBM Vice President and Group Executive T. V. Learson at Corporate Headquarters in New York, N. Y.

In his new position, he will manage engineering and scientific development work at ASDD's East Coast locations including Yorktown, Peekskill and Ossining. The division has responsibility for identifying technical and commercial feasibility of advanced information handling computer systems.

Throughout his IBM career, he has held important technical assignments. He was previously manager of product development for ASDD at Poughkeepsie and prior to that was manager of engineering

(Continued on page 91A)

Dedicated to better serve the electronics industry...



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RADIO MATERIALS COMPANY

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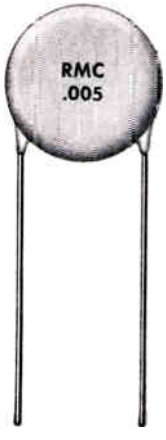
This new factory, office and research center in Chicago will enable RMC to expand its service to the growing electronic industry. The modern facility incorporates extensive manufacturing space to provide the fastest shipments of RMC DISCAPS with up to the minute research laboratories where technicians are engaged in capacitor development and improvement.



The combination of this new facility with RMC's modern plant in Attica, Indiana, enables Radio Materials Company, now, more than ever, to better serve your ceramic capacitor requirements efficiently and economically.

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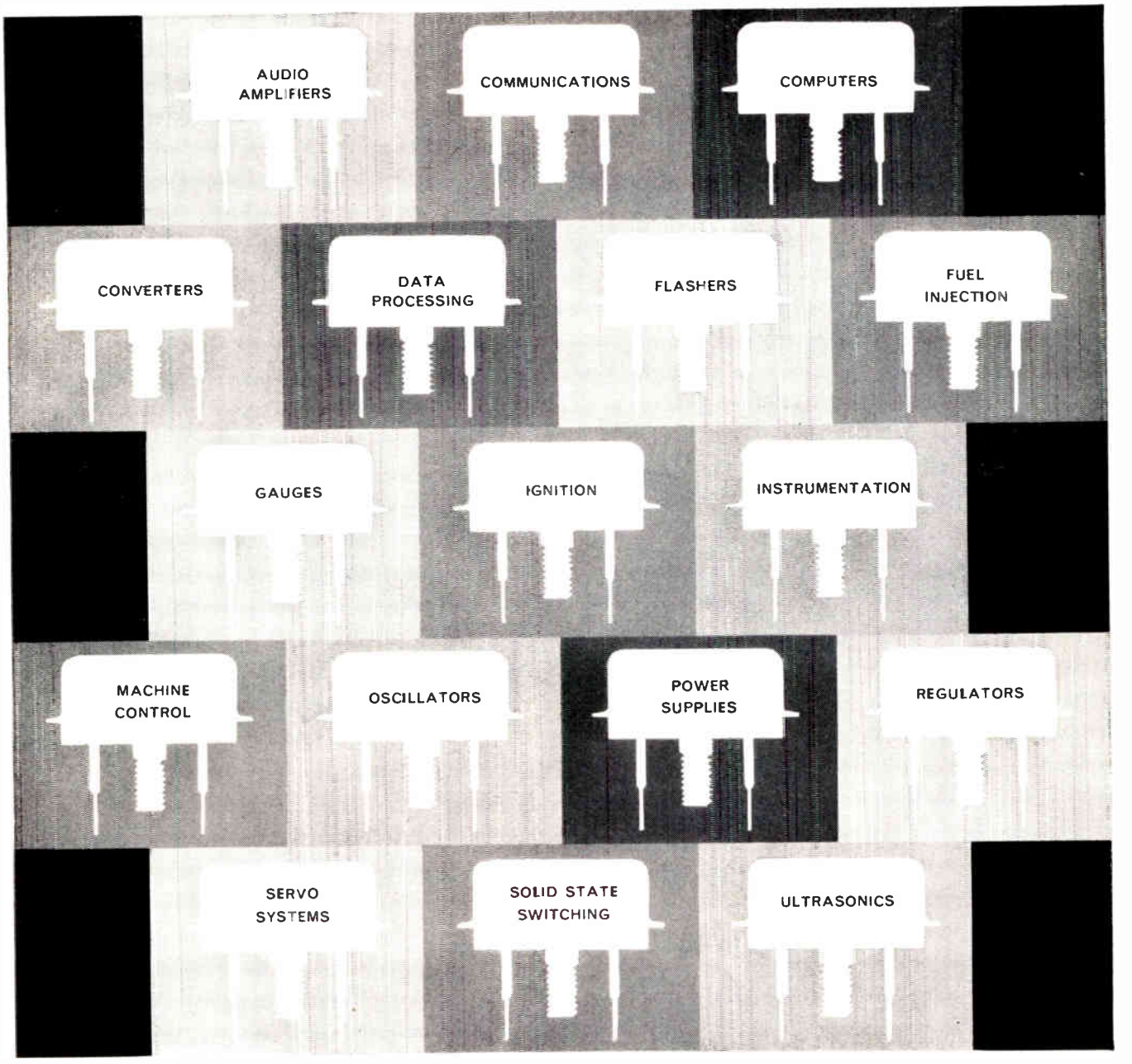

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TRinity 3-6560

Division of General Motors · Kokomo, Indiana

IRE People

(Continued from page 88A)

for the Special Engineering Products Division, a predecessor of ASDD.

He was also assistant manager of computer development at the IBM Poughkeepsie Laboratory. He designed input/output systems for tape processing machines and the IBM 702 computer.

Mr. Jackson holds the B.S. degree in electrical engineering from Duke University, Durham, N. C., and is a member of the American Institute of Electrical Engineers.

❖

Leslie C. Jesty (M'54–SM'55–F'56), B.Sc., M.I.E.E., has been appointed Manager of Sylvania-Thorn Colour Television Laboratories Ltd., London, in succession to **Brian C. Fleming-Williams** (SM'55), B.Sc., A.M.I.E.E., who has resigned his position with the company.

Mr. Jesty joined the Laboratories in 1957 and has been mainly responsible for the research and development program on color television and cathode-ray tubes.

Following recent reorganization, the work of the Laboratories is now directed toward serving various long-term interests of the parent companies, including work on color television.

❖

The appointment of **Richard M. Johnson** (M'51) to the post of Sales Manager has been announced by Markite Corporation, New York, N. Y., manufacturers of conductive plastic precision potentiometers for use in electro-mechanical controls and instrumentation for the industrial, commercial, aircraft and military fields.

R. M. Johnson

He has a background of more than 22 years of sales management and developing engineering experience in the electro-mechanical and electronic components industry. Prior to joining Markite, he had been associated with International Resistance Co., Philadelphia, Pa., serving as District Sales Manager for 8 years and Chief Product Development Engineer for 4 years previously. Other firms where he has held design engineering posts include Brown Instrument Co. and United Specialties Co., both of Philadelphia.

Mr. Johnson holds the B.S.E.E. degree, Tri-State College, Angola, Ind., and his memberships include the American Management Association.

❖

Louis H. Kellogg (SM'58) has been named Director of the Bell Telephone Laboratories' White Sands, N. M., in-

(Continued on page 92A)

IRE People

(Continued from page 91A)

L. H. KELLOGG

stallation. He was previously Missile Systems Development Engineer at the Whippany, N. J., location of Bell Laboratories. His new appointment became effective October 1, 1960. He will be responsible for continued NIKE-HERCULES tests at White Sands and for the expanding NIKE-ZEUS test program at White Sands and at Pt. Mugu, Calif.

He is a native of Madison, Ohio, and received the Bachelor of Electrical Engineering degree from The Ohio State University, Columbus, in 1939 and completed a year of graduate study before entering the Armed Services in 1941.

As an officer in the Signal Corps, he was involved in the development of microwave radar. During the latter part of World War II, he was a project officer for the Army Air Forces Board, Orlando, Fla., concerned with tactical operation tests of new ground and airborne radar equipment.

He joined Bell Laboratories in 1945 and was first engaged in the development of missile electronics for the NIKE anti-aircraft guided missile project. He was appointed a supervisor in charge of development of the missile electronics for NIKE-AJAX in 1951. Later, his responsibilities were increased to include the missile electronics as well as system engineering for NIKE-HERCULES. He next added responsibility for radar engineering and computer development on NIKE-HERCULES, including the recently announced improved NIKE-HERCULES system.

Mr. Kellogg is a member of the American Rocket Society, American Ordnance Association, and Tau Beta Pi, Eta Kappa Nu and Sigma Pi Sigma honorary fraternities.

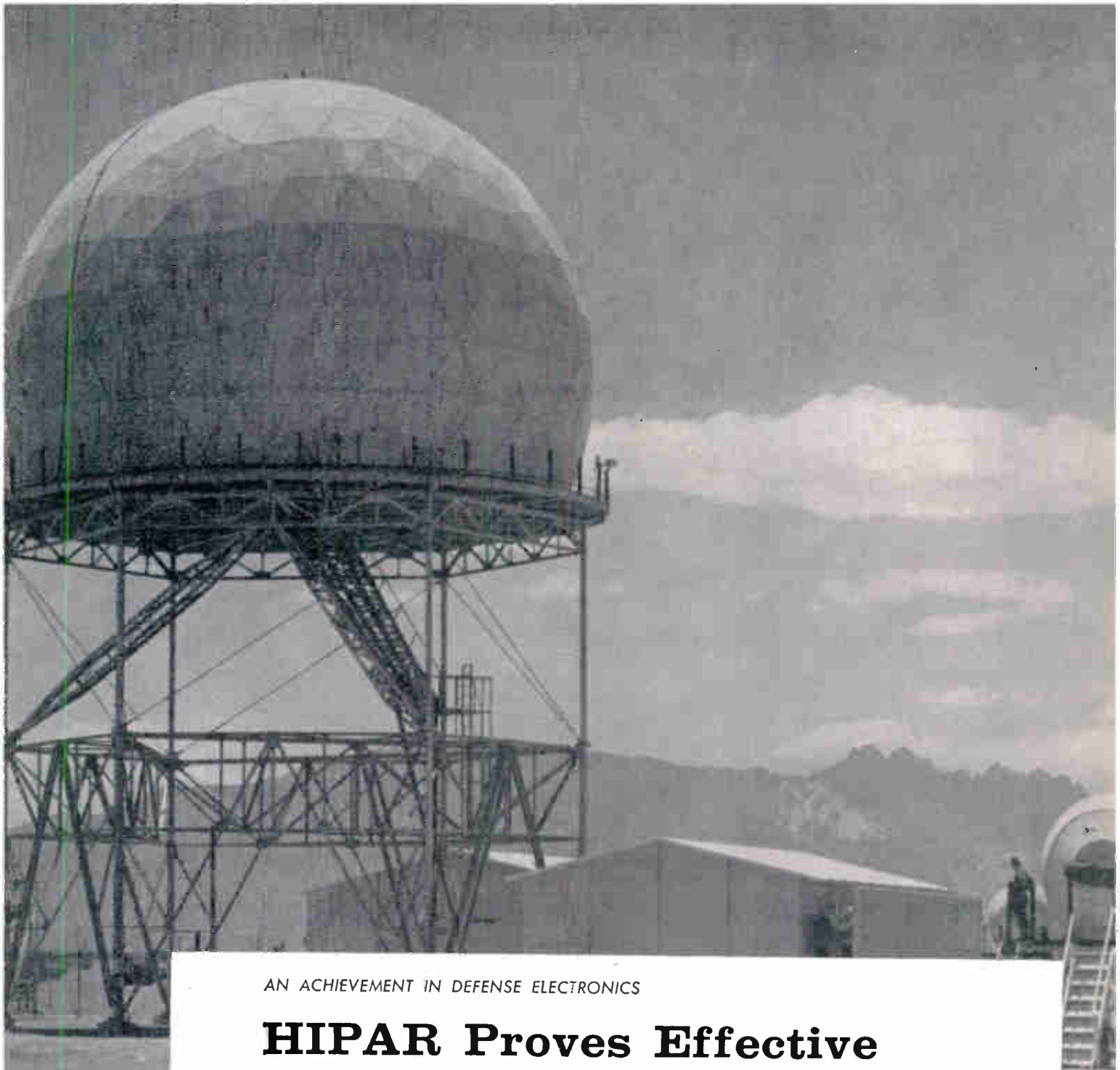
❖

George N. Krassner (M'59) has been appointed product manager for astronautics equipment in the Electronics Division of Stromberg-Carlson, it was recently announced. Stromberg-Carlson is a division of General Dynamics Corporation.

G. N. KRASSNER

He comes to Stromberg-Carlson from the U.S. Army Signal Research and Development Laboratory at Fort Monmouth, N. J., where he was chief of the satellite equipment section, Radio Relay Branch, and later chief of the technical staff, Astro-Electronics Division. He performed much

(Continued on page 102A)



AN ACHIEVEMENT IN DEFENSE ELECTRONICS

HIPAR Proves Effective In Hercules Anti-Missile Test

This new General Electric *High Power Acquisition Radar* (HIPAR) more than triples the detection capability of the U. S. Army's Nike-Hercules System. Produced for Western Electric, Nike-Hercules System Prime Contractor, this General Electric radar provides high resolution target data at long range and high altitudes on bomber and fighter aircraft, air-launched missiles and tactical ballistic missiles. The effectiveness of this Improved System was demonstrated at the White Sands Missile Range on June 3, 1960, with the successful intercept and destruction of a Corporal Missile, and in August and September, 1960, when target Nike-Hercules Missiles were destroyed by their defending counterparts at altitudes to almost 100,000 feet and closing speeds near Mach 7. 176-06

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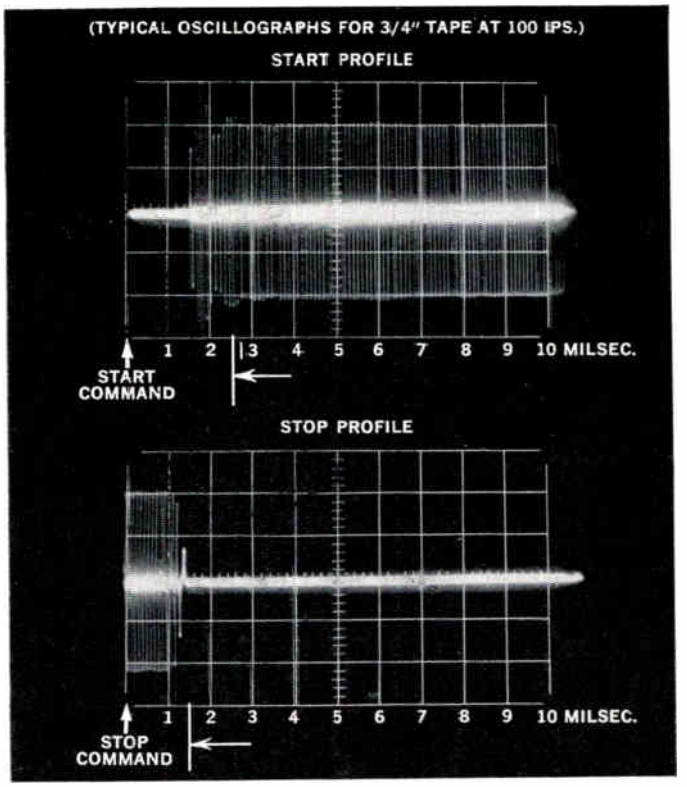

The Potter 906 II gives you the highest performance and reliability at savings up to 1/3 the cost of ordinary tape handlers. Potter has been given complete responsibility for tape sub-systems in some of the most widely sold computers. Potter's many years of concentrated specialization in tape system designs assures computer manufacturers of performance and dependability at costs that give them a competitive advantage in today's market. Computer users, too, are specifying Potter tape systems for lower rental costs, fewer service problems, and less down time. The Potter 906 II Tape Handler is being specified by more and more manufacturers and computer users because of the kind of performance proven by the clean Start-Stop profiles above and because the 906 II offers such other advantages as: ● Full forward-reverse cycling with 1" tape at 120 ips. ● Low skew tape guide. ● High density: 450,000 8-bit characters per second can be recorded on 1" tape by using the 906 II with the Potter Contiguous Double Transition System. ● Transistorized control of all functions. ● Simplified packaging for easy maintenance. Write for detailed specifications, prices and delivery information on the 906 II and see proof that you get higher performance and greater economy from a tape system specialist.

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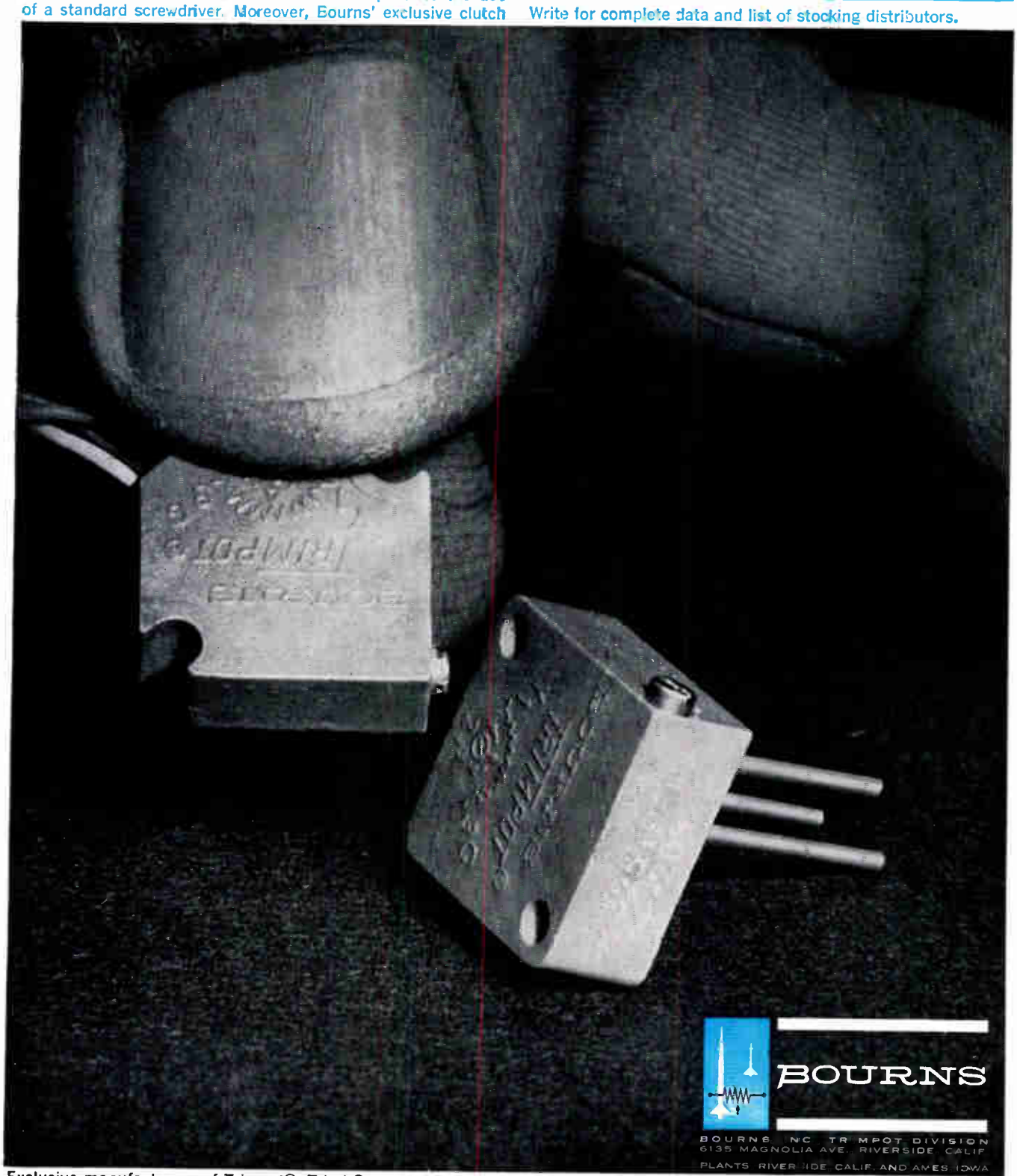

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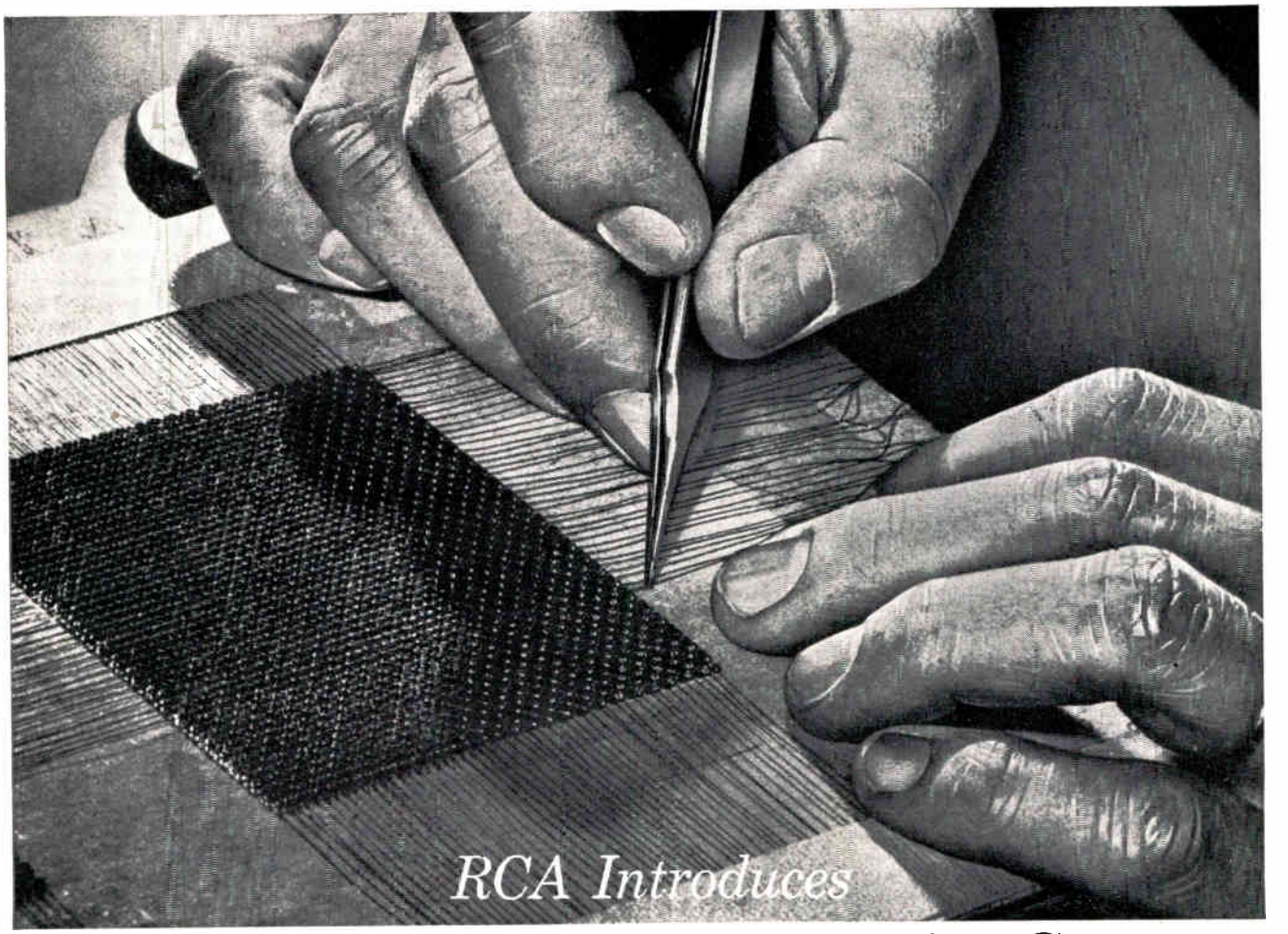

New Ultra-High-Speed Ferrite Core For Simplified Memory Plane Construction

Now RCA Offers TWO Memory Cores for Impulse Switching to 0.2 Microsecond

New RCA memory core XF4930 joins the RCA 400M1 in adding new flexibility to memory system design. Specifically developed for operation under impulse switching conditions in magnetic memory systems, XF4930 switches in 0.25 microsecond and provides excellent discrimination at relatively low driving currents.

The larger size of the XF4930, providing more than twice the effective aperture size of the RCA 400M1, permits simpler and more economical fabrication of memory planes.

Systems Engineering Service: Your local RCA field representative is prepared to furnish a completely coordinated application service, covering transistors and other semiconductor devices, ferrites, and memory systems. Call him today.

Nominal Operating Characteristics At 25°C	Type XF4930	Type 400M1	Units
Read Driving Current (I_R)	570	380	ma
Full Write Current (I_{FW})	255	280	ma
Impulse Write Current (I_{IW})	130	180	ma
Digit Write Current (I_{DW})	125	100	ma
Read Pulse Rise Time (t_r)	0.1	0.1	μsec
Full and Impulse Write Current Rise Time (t_r)	0.1	0.08	μsec
Digit Write Pulse Rise Time	0.1	0.15	μsec
Switching Time (t_s)	0.25	0.2	μsec
Response: "Undisturbed Read-1" (uV_{R1})	100	50	mv
"Disturbed 0" (dV_z)	15	8	mv
Size	.050x.030x.015	.080x.018x.010	inch

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Walter R. G. Baker

1892–1960

"It is with a sense of profound loss that we record the death on October 30, 1960 of Walter R. G. Baker, treasurer and past president of The Institute of Radio Engineers.

"In the decade and a half that he sat in the high councils of IRE, he left in those vibrant and vital years an indelible mark on the thoughts and practices of the Institute.

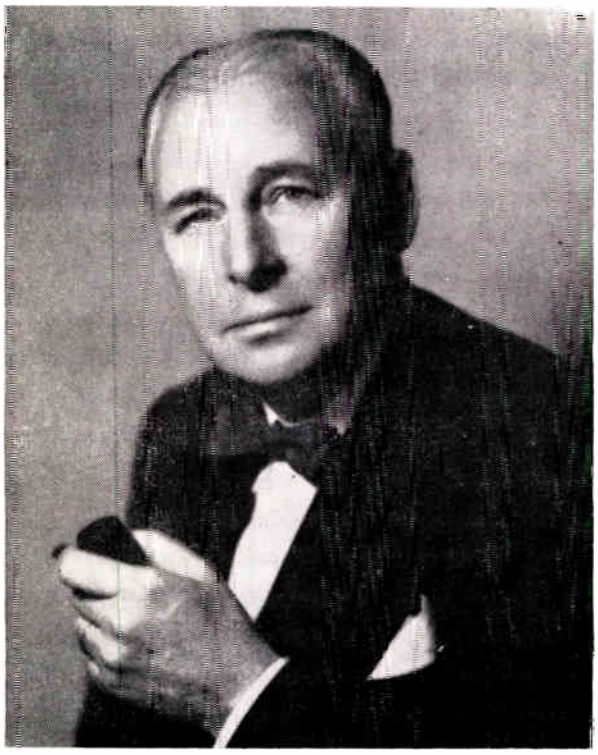
"As a member of the Board of Directors (1946–60), as a member of the Executive Committee (1947–60), as President (1947), as chairman of the Finance Committee (1948–60), and as Treasurer (1951–60), he brought to The Institute of Radio Engineers the firmness so necessary in a period of exponential growth, a foresight that anticipated our tremendous development, and the wisdom and fairness required to govern a multi-faceted organization.

"To him more than any single individual is owed our economic well being.

"The wise organization of our Professional Group system, expressing so well our unity through diversity, is due in great measure to his untiring efforts and ardent support.

"Resourceful, imaginative, totally dedicated, W. R. G. Baker will be remembered long and well in the annals of The Institute of Radio Engineers."

The foregoing testimonial to Dr. Baker was adopted by the IRE Board of Directors at its meeting on November 15, 1960, with the instruction that it be transmitted to his family and that it be spread upon the minutes of the meeting as lasting tribute to a great man.



Lloyd V. Berkner

President, 1960

Lloyd V. Berkner (A'26–M'34–SM'43–F'47) was born February 1, 1905, in Milwaukee, Wis. He received the B.S.E.E. degree in 1927 from the University of Minnesota, Minneapolis, which in 1952 honored him with the Distinguished Alumni Award, and from 1933–1935, he studied physics at the George Washington University, Washington, D. C. He holds honorary Doctorate degrees from Brooklyn Polytechnic Institute, Brooklyn, N. Y., Uppsala University in Sweden, University of Calcutta in India, Dartmouth College, Hanover, N. H., University of Notre Dame, Notre Dame, Ind., Columbia University, New York, N. Y., University of Rochester, Rochester, N. Y., and the University of Edinburgh in Scotland.

While still an undergraduate, he was engineer-in-charge at radio station WLB-WGMS in Minnesota. For a year after graduation, he worked as an electrical engineer for the Airways Division, U. S. Bureau of Lighthouses. He was an engineer with the first Byrd Expedition to the Antarctic in 1928–1930, and was awarded the U. S. Special Congressional Gold Medal, the Silver Medal of the Aeronautical Institute, and the Gold Medal of the City of New York for his services. For three years thereafter, he was on the staff of the National Bureau of Standards. From 1933–1941, he was a physicist with the Department of Terrestrial Magnetism of the Carnegie Institution of Washington, bringing the first Air Waves Radio Range System to fruition. During 1940–1941, he was a consultant to the National Defense Committee.

An aviator in the Naval Reserve since 1926, Dr. Berkner was called to active duty as head of the Radar Section, Bureau of Aeronautics, in 1941. He directed the Bureau's Electronics Materiel Branch from 1943–1945, and served on the *U.S.S. Enterprise* in 1945, in the Battle of Okinawa. He has held the rank of Rear Admiral, USNR, since 1955.

During 1946–1947, he was Executive Secretary of the Research and Development Board and remained a consultant to the Board until 1951. He was head of the Section on Exploratory Geophysics of the Atmosphere, Department of Terrestrial Magnetism, Carnegie Institution, from 1947–1951. From 1951 to 1960, he was President of Associated Universities, Inc., New York, N. Y., an educational institution which operates research facilities such as the Brookhaven National Laboratory, under contract with the Atomic Energy Commission, and the National Radio Astronomy Observatory, under contract with the National Science Foundation. He has recently become president of the Graduate Research Center, Dallas, Tex.

Dr. Berkner has held numerous offices and advisory positions in government, industry, and education. In the State Department, he served as Special Assistant to the Secretary of State, and Director of the Foreign Military Assistance Program in 1949, and Chairman of the International Science Steering Committee which produced the report "Science and Foreign Relations." Recently, he was a leader on national and international committees for the International Geophysical Year. He is presently a member of the Board of several industrial and research organizations. He was formerly a member of the President's Science Advisory Committee, and at the expiration of this term became consultant to the Committee.

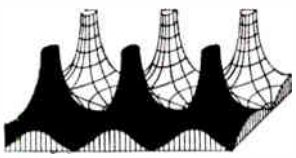
He received the Science Award of the Washington Academy of Sciences in 1941; Commendation Ribbon of the Secretary of the Navy in 1944; Honorary Officer, Order of the British Empire in 1945; U. S. Legion of Merit in 1946; and Alumni Recognition Award of Acacia Fraternity in 1954.

He is Chairman of the Space Science Board of the National Academy of Sciences, Past President of the International Scientific Radio Union, Retiring President of the International Council of Scientific Unions, and a former member of the Executive Committee of the International Union of Geodosy and Geophysics. He is Treasurer of the National Academy of Sciences, a member of the American Philosophical Society, President of the American Geophysical Union, and a Fellow of the American Academy of Arts and Sciences, the American Institute of Electrical Engineers, the American Physical Society, the Arctic Institute of North America, and the New York Academy of Sciences. Also he is a Foreign Fellow of the Royal Swedish Academy of Sciences and holds membership in numerous other professional and honorary societies in the U. S. and abroad.

January, 1961
Vol. 49 No. 1

Proceedings of the IRE

Poles and Zeros



Second Round. This issue of the PROCEEDINGS, being the second Special Issue devoted to Computers, is so excellently described in the Introduction (page 4) that Scanning the Issue has been omitted this month. Poles and Zeros can also use the comprehensiveness of the Introduction as an excuse to devote its attention, and that of its readers, to the work represented in the successful assembling of this volume.

A Guest Editorial Board, comprised of Harry T. Larson as Guest Editor, L. C. Hobbs, and K. W. Uncapher, undertook the preparation of this issue. C. W. Rosenthal stood by to assist in special situations. This group has produced an issue of the PROCEEDINGS about which the Managing Editor has stated, "This issue represents more work on the part of more people than any IRE publication to date." The members of the Guest Editorial Board were responsible for the procurement and selection of the 11 invited review papers, the 17 selected papers, and the one reprinted paper that make up this imposing issue.

The Guest Editorial Board established a special review committee of 63 experts from all over the country. These experts handled the 140 submitted papers in a very short period of time. This was only the beginning of the task since the initial reviews left about half of the total papers as possible prospects for the issue. The guest editors worked far beyond the call of duty, literally night and day, in re-reviewing, revising, and selecting the final group of papers.

It is difficult to appropriately express appreciation for the superb job turned in by the editors of, and contributors to, this issue. Their satisfaction and thanks will come from their knowledge that they have produced an outstanding contribution to the progress of the computer art.

Membership. A review of back copies of the PROCEEDINGS reveals that Poles and Zeros first made mention of IRE membership statistics in August, 1956. At that time Editor Fink reported that the IRE membership roster had just passed the 50,000 mark. He went on to predict that if growth continued to be compounded as it had since 1952, we could expect to pass the 100,000 mark in 1962. The August, 1957 Poles and Zeros reported that in May of that year the membership had passed 60,000. Then in July, 1958, Editor Ryder devoted the entire Poles and Zeros page to the subject of IRE growth and in typical engineering fashion demonstrated by a semi-logarithmic plot that "barring cataclysms, catastrophes, or controvertible calculations" a simple extrapolation confirmed the earlier prediction of 100,000 members in 1962. The present Editor is pleased to report that, having inserted the latest statistics (see box on page 14A) on the same semilogarithmic plot, the extrapolation still appears valid.

This is all a rather lengthy prelude to calling to your attention the availability to all IRE members of an application form for prospective members. It is as close as your copy of the IRE Directory. The new 1961 Directory which you received a short time ago contains a convenient tear-out application following page 20. Of course, if you need more than one they are readily available through your Section Membership Committee.

IRE Dictionary. During the past 18 years, The Institute of Radio Engineers, through its Technical Committees and its Standards Committee, has formulated and published 37 IRE Standards dealing with terminology and symbology. Prior to 1949 these Standards were published as separate pamphlets; since that time they have appeared singly in issues of the PROCEEDINGS. Gathering these Standards and combining them between one pair of covers has now been accomplished, and the IRE Dictionary thus brings together all the definitions and symbols published and still valid through December, 1959.

The Dictionary provides a convenient and ready reference to approximately 3700 technical terms and their IRE Standard definitions. It also includes reprints of five IRE Standards containing letter and graphical symbols. It is anticipated that the Dictionary will serve an important need, and it should save much searching among PROCEEDINGS files. It may be purchased by IRE members for $5.20; by non-members for $10.40. Orders may be directed to Headquarters.

Reminder. Chairmen, and Secretaries of Sections, Subsections, and Professional Groups have received from the Executive Secretary instructions as to the new procedure for nominations for IRE Fellow grade. These instructions called attention to the necessity for submitting Fellow nominations on or before March 31, 1961 for a candidate to be eligible for consideration for advancement to the grade of Fellow as of January 1, 1962. Adherence to the deadline will assure consideration of your candidates. Do not deprive your candidate of consideration for advancement by your carelessness.

Miscellany. By action of the Board of Directors, at its meeting in October, 1960, the bylaws were amended to require the signatures of 100 members to petition for the formation of a new Professional Group. This is certainly a minimal requirement for an organization comprising over 87,000 members. At the same meeting the Board approved the formation of an IRE Technical Committee on Reliability. There are now 26 Standing Technical Committees.—F. H., Jr.

The Computer Issue*

HARRY T. LARSON†, GUEST EDITOR

Introduction

THIS IS the second special Computer Issue of the IRE Proceedings; the first was dated October, 1953. Since computers continue to be a subject of widespread interest and have become a factor in the lives of most electronic engineers, this issue has been designed to be useful to the nonspecialist as well as computer specialists. The papers herein review useful developments in the intervening seven years, report the "state of the art" in important aspects of current computer design and application, describe significant new developments, and indicate the trends of this multifaceted technology.

As in 1953, activity in the computer field continues to expand at an astonishing rate, whether measured in terms of numbers of computers in use, types of functions computers perform, number of people employed in the industry, or number of inventions and new components introduced. Basic (non-mutually-exclusive) forces behind this advance include the following:

1) Computer equipment can perform some of the functions classed as "mental processes." Thus, this equipment is a candidate for a broad range of activities that have, in the past, been performed entirely by humans. Computers have proven to be capable of matching or outperforming men in many information processing activities, in terms of speed, cost, or capacity to integrate a multitude of factors. Also, computers can perform such functions in environments unsuited for humans.
2) The value of the computer in the sciences and engineering is solidly established. This acceptance, in the fields that stimulated the creation of the equipment, has accounted for a large fraction of the expansion to date.
3) The general information processing capability of the computer is a major addition to the array of tools available for the "industrial revolution." This evolution has been primarily characterized in the past by the introduction of machines that replace or augment man's *muscular* activity. Computers, on the other hand, can undertake some of the *control* function performed by man. The powerful economic forces behind the ever continuing industrial revolution are coming into play here, and the arrival of the computer and its descendents may well introduce a truly "revolutionary" note to this evolution.
4) The impatient designers and builders of computing equipment, aware of the breadth of its general applicability, are vigorously sponsoring invasions into new areas. While these attacks are based primarily on economic forces, an independent force not unlike enthusiastic missionary zeal is a measurable factor.

These and other interrelated forces have resulted in a rapidly growing military and commercial demand for computer equipment, in turn producing an economic environment that is supporting an extraordinary range of engineering activities. Some of the new research and engineering activities within this field arise from an independent source: the computer, having characteristics that cause it to perform in some ways like what is believed to be the human thinking process, and having a complexity that may exceed that of any other thing built by man, has intrigue, excitement, and challenge that attract the mind of many an engineer and scientist, causing them to direct their efforts to this area.

From the resulting myriad of current developments, the editors have identified significant facets of computer evolution since 1953, and have selected a representative set of papers describing advanced developments. Several informative and hopefully stimulating introductory and survey papers have been included for the nonspecialist. Relatively elementary information has been included where judged necessary to properly introduce subjects. For the computer specialist, state-of-the-art papers are provided that summarize and compare the many activities in certain specialized areas, and reports are included on advanced developments and examples of areas of current research.

Contents of This Issue

Artificial Intelligence

Possibly the most stimulating advanced developments in computer design and application are those devoted to improving the capabilities of the computer to perform increasingly higher level information-processing functions; "higher" in this context means moving toward the processes human intelligence can perform. The issue starts with two invited articles on this subject. The first paper (Minsky) is a thorough and intensely interesting review of the first halting steps toward "artificial intelligence." This paper speaks primarily to a class of activities in which a general purpose computer, complete with a library of basic programs, is further programmed to perform functions which lead to learning, problem solving, etc. A second group of ac-

* Received by the IRE, November 10, 1960.
† Aeronutronic Div., Ford Motor Co., Newport Beach, Calif.

tivities is devoted to "self-organizing" machines (Hawkins), which include a variable network, the elements of which are to be organized by the equipment itself to meet criteria of success in the environment in which it operates. Hawkins' thoroughgoing paper is followed by a description of an element that can be used to construct networks that simulate neural networks (Brain), indicating a hardware mechanization which may be useful in self-organizing machines. A third class of developments, "self adaptive" systems, may be associated with the approaches to artificial intelligence. These adaptive systems are usually employed in feedback control systems, being capable of automatically modifying internal network parameters to optimize, stabilize, or otherwise improve the control system as a function of variations in its environment. A description of an advanced form of such a system appears later in the issue, in an article on control system use of computers (Truxal).

The nature of the attack on this matter of artificial intelligence contains ingredients of a recurring phenomenon of considerable significance in the spread of computer application: when computers are applied to a field of activity outside the fields that primarily employ mathematics and logic in their theories, *that field undergoes greater formalization*. Once serious effort is initiated to apply the computing machine in such a field, often a chaotic condition is soon reached wherein it is recognized that the problem cannot be fully stated with the information and understanding at hand, so the machine cannot be fully instructed. Rather than turn away from the problem, the team attempting to apply the computer usually has sufficient motivation to create the required formalization. Useful standardization of terminology is usually fostered, as indicated in current efforts to apply computers to medical diagnosis. Successful computer application may require initiation of a new theory for the field, as in Minsky's start on a theory of intelligence. Language translation (see Bauer, Gerlough, and Granholm) has initiated exciting work on the theory of the structure of language; the grammar rules taught in English classes are inadequate and inexact. *Thus, perhaps one of the most important impacts computers are producing in our society is through serving as a catalyst for channeling the attention of scientific and disciplined minds into relatively unformalized areas.* When the channel is established, when the practitioner has overcome his fear of the machine, and when the scientist and practitioner are communicating, the attack is relentless. The scientific mind has found an unformalized field, and it cannot rest until it identifies, understands, and organizes basic elements of the field; the practitioner has found a powerful new tool to advance his capabilities.

Computer Organization and Components

The next set of papers is devoted to the computer proper. It is introduced by an invited article discussing the evolution in the over-all organization of the arithmetic and control elements (Beckman, Brooks, and Lawless). The internal organization of today's machines is appreciably more complex than in the computers reported upon in 1953. The design has been influenced by the desires of computer programmers, as evidenced by such things as an increasing number of index registers, and a larger repertoire of instructions in some machines. Several operations may be performed concurrently. The sharply increased use of input/output and auxiliary storage devices has reflected requirements into the internal computer design. Also, the boundaries between arithmetic, control, and storage units have become indistinct in some of the more sophisticated designs.

The internal operating speeds of computers have increased two or three orders of magnitude since 1953. This has been accomplished in part by advances in the methods of performing the basic operations (MacSorley) of addition, multiplication, and division. This thorough paper classifies and compares many methods of obtaining high speed in these operations in parallel binary computers, and reports original work in this field. The arithmetic operation of division is often bothersome to the system designer, usually taking longer to perform than the other basic arithmetic operations. An analysis of several division techniques is presented (Freiman).

The computer field continues to be characterized by the appearance of new components capable of performing the basic functions of storage or logic. A few such components are reported upon here.

An important factor in determining over-all computer performance is the internal memory or storage. The electronic, random-access class of internal memories is reviewed in an invited paper (Rajchman), describing the functions fulfilled by such storage units, and explaining the principles of present advanced components and techniques. The thin film memory (Raffel, Crowther, Anderson and Herndon) is a promising development in storage devices. The development of a disk device that may serve either as a central storage or in the hierarchy of stores backing up the central store is reported (Pearson), in an unusual type of paper that describes a research and development program of mature caliber. Design information of value in magnetic digital recording on tapes, disks, or drums is also presented (Hoagland and Bacon).

Tunnel diodes hold promise of becoming a useful element, performing both logic and memory functions, and extending the speed of computers. The status of the varied activity is surveyed (Sims, Beck, and Kamm), to put the many isolated contributions into perspective. The tunnel-diode locked-pair circuit is subjected to an introductory analysis (Kaupp and Crosby) that makes it possible to estimate the maximum operating frequency of such a pair; this paper also serves as an example of the use of a digital computer to solve nonlinear circuit design problems.

This issue would not be complete without a report on the exciting work on use of radio high-frequency circuits to attain ultra high speed computation (Abeyta, Bor-

gini, and Crosby). Significant work in phase-locked subharmonic oscillator operation in the kilomegacycle region is described.

Input, Output and Communication

In 1953, computers were generally large machines dominated by the computer proper, augmented by a relatively moderate amount of "auxiliary" on-line equipment for storage and input/output functions. In the last seven years, the proliferation of equipment has produced systems of all sizes, ranging from desk size to four-story blockhouse size. In many of these, especially the medium and large size equipments, the computer proper is a moderate part of what is often now termed the "computer system"; extensive arrays of on-line storage, input, and output equipments surround the central "main frame" or computer proper, and special processing equipment has evolved for managing the activities of these parts of the system.

A small group of papers has been included to reflect properly the "computer system" nature of current developments. Many of the peripheral devices are aimed at improving the communication between man and computing machines. The considerable body of work in developing a visual input sensor for computers is indicated by reporting an example of current research in character recognition (Horwitz and Shelton). This work is particularly pertinent to the self-organizing systems work (Hawkins). On the output end, communication of computer-generated data to people has been markedly improved by the development of new display devices. An invited paper (Loewe, Sisson and Horowitz) summarizes the user requirements and functions to be fulfilled by displays, and surveys many of the newer devices and techniques available or under development in this surprisingly varied and active field.

Computing systems today are often found to be but a part of a larger system, sometimes directly linked to inputs and outputs distributed over substantial geographical areas. In such systems, digital communication has become a significant problem. Many of the advanced developments in this area remain under military classification. Considerable commercial and domestic digital communication work exists, and this has been surveyed in an introductory invited paper (Wier).

Design Techniques

The importance of logical design and the continuing progress in this discipline require that an example or two of current developments be incorporated in this issue. A considerable body of advanced activity exists in techniques for use with threshold devices (Stram) and for majority (or vote-taking) logic. Logical and systems designers who find the flow table useful will be interested in a logical design approach (Low and Maley) which starts with a new set of design criteria appropriate for the coming microminiature systems employing a massive number of elements packed at high density. An example of the variety of error-detecting codes now in use or development is the class of codes for detecting bursts of errors (Brown and Peterson), especially useful in digital communication (Weir).

"Worst-case" design of computer circuits continues, but some reaction to this approach has occurred. There is evidence that worst-case design results in so many components in a system that its over-all reliability is not maximized. Statistical analysis is now being applied (Nussbaum, Irland and Young) to seek a compromise that produces greater over-all reliability and contributes to improved performance in other ways.

Design techniques for nonlinear dynamical systems (Haynes), applied to cryotron circuits, are applicable in many aspects of engineering, and should prove interesting to the nonspecialist; the computer specialist will be interested in this paper's application to cryotron networks. A useful example of a design technique applicable to magnetic digital recording (Hoagland and Bacon) is given in a paper considered to be one of the outstanding reports in the TRANSACTIONS of the Professional Group on Electronic Computers within the last year. Both of these papers are good examples of the use of computers in engineering design.

Analog

Readers interested in the solution of a class of partial differential equations representing transient field problems will be interested in an analog network simulator (Karplus) which is useful particularly in those differential equations in which the dependent variable varies nonperiodically with time.

Clever mathematical analogs have been applied for many years in analog equipments that allow the measurement of the magnitude and angle of functions of the complex variable; these have usually taken the form of electrolytic tanks in which appropriate measurements are taken in the fields between the singularities. Automatic control engineers will be interested in a novel approach (Morgan) which permits the measurement of magnitude and angle by taking measurements at the poles and zeros. This will be of interest to those who find themselves evaluating the inverse Laplace transform.

Programming

Computer programming developments qualify for a report in this issue because of the fundamental and extremely important role programming plays in the use of any stored program computer, because of the role programming plays in the design of a computer, and because of the major progress being made. An invited paper (Orchard-Hays), starting from the Hopper and Mauchly paper in the 1953 Computer issue, identifies the techniques, languages, and systems that have

evolved as programmers move to higher and higher levels of sophistication and abstraction in their employment of computing machinery.

Applications

A useful simple listing or even a simple classification of the range of uses of computers is a task of considerable magnitude. A few representative new applications have been summarized in an invited paper (Bauer, Gerlough, and Granholm), which will be of considerable interest to the nonspecialist. One class of computer applications of rapidly growing importance is the use of computers in control systems, discussed in an interesting invited review paper (Truxal). A recently declassified paper on the use of a digital system in a multiple control task (Lewis) is of considerable interest to the specialist and nonspecialist alike, describing the application itself and blocking out the computer and its characteristics. This system contains two computers, a smaller lower capability computer taking over if the main computer malfunctions.

For the purposes of most PROCEEDINGS readers, probably the most useful type of application to report upon is that which shows the computer as a tool in circuit design. A number of earlier papers in the issue do just this (Kaupp and Crosby) (Nussbaum, Irland, and Young) (Haynes) (Hoagland and Bacon) (Morgan). An excellent example of the rapidly growing use of computers in simulation roles is given (David), showing the aid provided by this tool in engineering research.

European Situation

The explosive growth in types and numbers of computer equipments in the United States militates against any satisfactory selection of machines to report upon. Also, current interest in computers and excellent publication channels have provided adequate coverage for nearly all recent developments which are free of military security. Although many existing machines are mentioned in the articles in this issue, only one article has been assigned to a machine description (Lewis). Attention has been turned to the extensive developments in Europe (Auerbach). In this invited paper, the author has selected and described the most significant developments there, and has summarized the characteristics of the many computers in operation and under development.

ACKNOWLEDGMENT

The guest editorial board gratefully acknowledges the assistance of the large staff of reviewers assembled to assist in judging the merits of the flood of papers submitted for this issue, including the many men around the country asked to make special reviews. The guest editor especially acknowledges the valuable and untiring efforts of L. C. Hobbs and K. W. Uncapher, who served on the guest editorial board. These men cheerfully assigned an extraordinary amount of personal time to this work, superimposed upon unusually heavy work loads. Theirs is a major contribution to the development of this issue.

Steps Toward Artificial Intelligence*

MARVIN MINSKY†, MEMBER, IRE

The work toward attaining "artificial intelligence" is the center of considerable computer research, design, and application. The field is in its starting transient, characterized by many varied and independent efforts. Marvin Minsky has been requested to draw this work together into a coherent summary, supplement it with appropriate explanatory or theoretical noncomputer information, and introduce his assessment of the state-of-the-art. This paper emphasizes the class of activities in which a general purpose computer, complete with a library of basic programs, is further programmed to perform operations leading to ever higher-level information processing functions such as learning and problem solving. This informative article will be of real interest to both the general PROCEEDINGS reader and the computer specialist.—*The Guest Editor*

Summary—**The problems of heuristic programming—of making computers solve really difficult problems—are divided into five main areas: Search, Pattern-Recognition, Learning, Planning, and Induction.**

A computer can do, in a sense, only what it is told to do. But even when we do not know how to solve a certain problem, we may program a machine (computer) to *Search* through some large space of solution attempts. Unfortunately, this usually leads to an enormously inefficient process. With *Pattern-Recognition* techniques, efficiency can often be improved, by restricting the application of the machine's methods to appropriate problems. Pattern-Recognition, together with *Learning*, can be used to exploit generalizations based on accumulated experience, further reducing search. By analyzing the situation, using *Planning* methods, we may obtain a fundamental improvement by replacing the given search with a much smaller, more appropriate exploration. To manage broad classes of problems, machines will need to construct models of their environments, using some scheme for *Induction*.

Wherever appropriate, the discussion is supported by extensive citation of the literature and by descriptions of a few of the most successful heuristic (problem-solving) programs constructed to date.

INTRODUCTION

A VISITOR to our planet might be puzzled about the role of computers in our technology. On the one hand, he would read and hear all about wonderful "mechanical brains" baffling their creators with prodigious intellectual performance. And he (or it) would be warned that these machines must be restrained, lest they overwhelm us by might, persuasion, or even by the revelation of truths too terrible to be borne. On the other hand, our visitor would find the machines being denounced, on all sides, for their slavish obedience, unimaginative literal interpretations, and incapacity for innovation or initiative; in short, for their inhuman dullness.

Our visitor might remain puzzled if he set out to find, and judge for himself, these monsters. For he would find only a few machines (mostly "general-purpose" computers, programmed for the moment to behave according to some specification) doing things that might claim any real intellectual status. Some would be proving mathematical theorems of rather undistinguished character. A few machines might be playing certain games, occasionally defeating their designers. Some might be distinguishing between hand-printed letters. Is this enough to justify so much interest, let alone deep concern? I believe that it is; that we are on the threshold of an era that will be strongly influenced, and quite possibly dominated, by intelligent problem-solving machines. But our purpose is not to guess about what the future may bring; it is only to try to describe and explain what seem now to be our first steps toward the construction of "artificial intelligence."

Along with the development of general-purpose computers, the past few years have seen an increase in effort toward the discovery and mechanization of problem-solving processes. Quite a number of papers have appeared describing theories or actual computer programs concerned with game-playing, theorem-proving, pattern-recognition, and other domains which would seem to require some intelligence. The literature does not include any general discussion of the outstanding problems of this field.

In this article, an attempt will be made to separate out, analyze, and find the relations between some of these problems. Analysis will be supported with enough examples from the literature to serve the introductory function of a review article, but there remains much relevant work not described here. This paper is highly compressed, and therefore, cannot begin to discuss all these matters in the available space.

There is, of course, no generally accepted theory of "intelligence"; the analysis is our own and may be controversial. We regret that we cannot give full personal acknowledgments here—suffice it to say that we have discussed these matters with almost every one of the cited authors.

It is convenient to divide the problems into five main areas: Search, Pattern-Recognition, Learning, Planning, and Induction; these comprise the main divisions

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of the paper. Let us summarize the entire argument very briefly:

A computer can do, in a sense, only what it is told to do. But even when we do not know exactly how to solve a certain problem, we may program a machine to *Search* through some large space of solution attempts. Unfortunately, when we write a straightforward program for such a search, we usually find the resulting process to be enormously inefficient. With *Pattern-Recognition* techniques, efficiency can be greatly improved by restricting the machine to use its methods only on the kind of attempts for which they are appropriate. And with *Learning*, efficiency is further improved by directing Search in accord with earlier experiences. By actually analyzing the situation, using what we call *Planning* methods, the machine may obtain a really fundamental improvement by replacing the originally given Search by a much smaller, more appropriate exploration. Finally, in the section on *Induction*, we consider some rather more global concepts of how one might obtain intelligent machine behavior.

I. The Problem of Search[1]

***Summary*—If, for a given problem, we have a means for checking a proposed solution, then we can solve the problem by testing all possible answers. But this always takes much too long to be of practical interest. Any device that can reduce this search may be of value. If we can detect relative improvement, then "hill-climbing" (Section I-B) may be feasible, but its use requires some structural knowledge of the search space. And unless this structure meets certain conditions, hill-climbing may do more harm than good.**

When we talk of problem-solving in what follows we will usually suppose that all the problems to be solved are initially *well defined* [1]. By this we mean that with each problem we are given some systematic way to decide when a proposed solution is acceptable. Most of the experimental work discussed here is concerned with such well-defined problems as are met in theorem-proving, or in games with precise rules for play and scoring.

In one sense all such problems are trivial. For if there exists a solution to such a problem, that solution can be found eventually by any blind exhaustive process which searches through all possibilities. And it is usually not difficult to mechanize or program such a search.

But for any problem worthy of the name, the search through all possibilities will be too inefficient for practical use. And on the other hand, systems like chess, or nontrivial parts of mathematics, are too complicated for complete analysis. Without complete analysis, there must always remain some core of search, or "trial and error." So we need to find techniques through which the results of *incomplete analysis* can be used to make the search more efficient. The necessity for this is simply overwhelming: a search of all the paths through the game of checkers involves some 10^{40} move choices [2]; in chess, some 10^{120} [3]. If we organized all the particles in our galaxy into some kind of parallel computer operating at the frequency of hard cosmic rays, the latter computation would still take impossibly long; we cannot expect improvements in "hardware" alone to solve all our problems! Certainly we must use whatever we know in advance to guide the trial generator. And we must also be able to make use of results obtained along the way.[2,3]

A. Relative Improvement, Hill-Climbing, and Heuristic Connections

A problem can hardly come to interest us if we have no background of information about it. We usually have some basis, however flimsy, for detecting *improvement*; some trials will be judged more successful than others. Suppose, for example, that we have a *comparator* which selects as the better, one from any pair of trial outcomes. Now the comparator cannot, alone, serve to make a problem well-defined. No goal is defined. But if the comparator-defined relation between trials is "transitive" (*i.e.*, if *A dominates B* and *B dominates C* implies that *A dominates C*), then we can at least define "progress," and ask our machine, given a time limit, to do the best it can.

But it is essential to observe that a comparator by itself, however shrewd, cannot alone give any improvement over exhaustive search. The comparator gives us information about partial success, to be sure. But we need also some way of using this information to direct the pattern of search in promising directions; to select new trial points which are in some sense "like," or "similar to," or "in the same direction as" those which have given the best previous results. To do this we need some additional structure on the search space. This structure need not bear much resemblance to the ordinary spatial notion of direction, or that of distance, but it must somehow tie together points which are heuristically related.

We will call such a structure a *heuristic connection*. We introduce this term for informal use only—that is why our definition is itself so informal. But we need it. Many publications have been marred by the misuse,

[1] The adjective "heuristic," as used here and widely in the literature, means *related to improving problem-solving performance;* as a noun it is also used in regard to any method or trick used to improve the efficiency of a problem-solving system. A "heuristic program," to be considered successful, must work well on a variety of problems, and may often be excused if it fails on some. We often find it worthwhile to introduce a heuristic method which happens to cause occasional failures, if there is an over-all improvement in performance. But imperfect methods are not necessarily heuristic, nor vice versa. Hence "heuristic" should not be regarded as opposite to "foolproof"; this has caused some confusion in the literature.

[2] McCarthy [1] has discussed the enumeration problem from a recursive-function theory point of view. This incomplete but suggestive paper proposes, among other things, that "the enumeration of partial recursive functions should give an early place to compositions of functions that have already appeared."

I regard this as an important notion, especially in the light of Shannon's results [4] on two-terminal switching circuits—that the "average" n-variable switching function requires about $2^n/n$ contacts. This disaster does not usually strike when we construct "interesting" large machines, presumably because they are based on composition of functions already found useful.

[3] In [5] and especially in [6] Ashby has an excellent discussion of the search problem. (However, I am not convinced of the usefulness of his notion of "ultrastability," which seems to be little more than the property of a machine to search until something stops it.)

for this purpose, of precise mathematical terms, *e.g.*, *metric* and *topological*. The term "connection," with its variety of dictionary meanings, seems just the word to designate a relation without commitment as to the exact nature of the relation.

An important and simple kind of heuristic connection is that defined when a space has coordinates (or parameters) and there is also defined a numerical "success-function" E which is a reasonably smooth function of the coordinates. Here we can use local optimization or *hill-climbing* methods.

B. Hill-Climbing

Suppose that we are given a black-box machine with inputs $\lambda_1, \cdots, \lambda_n$ and an output $E(\lambda_1, \cdots, \lambda_n)$. We wish to maximize E by adjusting the input values. But we are not given any mathematical description of the function E: hence we cannot use differentiation or related methods. The obvious approach is to explore locally about a point, finding the direction of steepest ascent. One moves a certain distance in that direction and repeats the process until improvement ceases. If the hill is smooth this may be done, approximately, by estimating the gradient component $\partial E/\partial \lambda_i$ separately for each coordinate λ_i. There are more sophisticated approaches (one may use noise added to each variable, and correlate the output with each input, see Fig. 1), but this is the general idea. It is a fundamental technique, and we see it always in the background of far more complex systems. Heuristically, its great virtue is this: the sampling effort (for determining the direction of the gradient) grows, in a sense, only linearly with the number of parameters. So if we can solve, by such a method, a certain kind of problem involving many parameters, then the addition of more parameters of the same kind ought not cause an inordinate increase in difficulty. We are particularly interested in problem-solving methods which can be so extended to more difficult problems. Alas, most interesting systems which involve combinational operations usually grow exponentially more difficult as we add variables.

A great variety of hill-climbing systems have been studied under the names of "adaptive" or "self-optimizing" servomechanisms.

C. Troubles with Hill-Climbing

Obviously, the gradient-following hill-climber would be trapped if it should reach a *local peak* which is not a true or satisfactory optimum. It must then be forced to try larger steps or changes.

It is often supposed that this false-peak problem is the chief obstacle to machine learning by this method. This certainly can be troublesome. But for really difficult problems, it seems to us that usually the more fundamental problem lies in finding any significant peak at all. Unfortunately the known E functions for difficult problems often exhibit what we have called [7] the "*Mesa Phenomenon*" in which a small change in a parameter usually leads to either no change in performance or to a large change in performance. The space is thus composed primarily of flat regions or "mesas." Any tendency of the trial generator to make small steps then results in much aimless wandering without compensating information gains. A profitable search in such a space requires steps so large that hill-climbing is essentially ruled out. The problem-solver must find other methods; hill-climbing might still be feasible with a different heuristic connection.

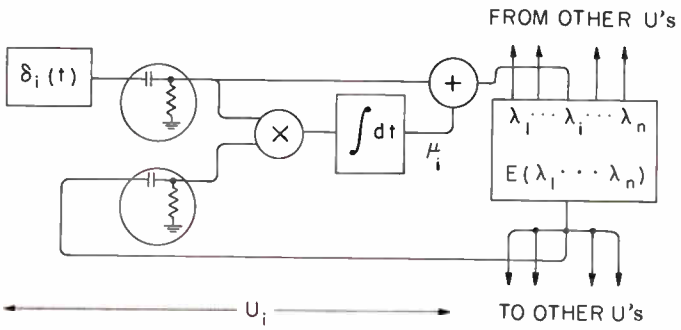

Fig. 1—"Multiple simultaneous optimizers" search for a (local) maximum value of some function $E(\lambda_1, \cdots, \lambda_n)$ of several parameters. Each unit U_i independently "jitters" its parameter λ_i, perhaps randomly, by adding a variation $\delta_i(t)$ to a current mean value μ_i. The changes in the quantities δ_i and E are correlated, and the result is used to (slowly) change μ_i. The filters are to remove dc components. This simultaneous technique, really a form of coherent detection, usually has an advantage over methods dealing separately and sequentially with each parameter. (Cf. the discussion of "informative feedback" in Wiener [11], p. 133 ff.)

Certainly, in our own intellectual behavior we rarely solve a tricky problem by a steady climb toward success. I doubt that in any one simple mechanism, *e.g.*, hill-climbing, will we find the means to build an efficient and general problem-solving machine. Probably, an intelligent machine will require a variety of different mechanisms. These will be arranged in hierarchies, and in even more complex, perhaps recursive, structures. And perhaps what amounts to straightforward hill-climbing on one level may sometimes appear (on a lower level) as the sudden jumps of "insight."

II. The Problem of Pattern Recognition

***Summary*—In order not to try all possibilities, a resourceful machine must classify problem situations into categories associated with the domains of effectiveness of the machine's different methods. These pattern-recognition methods must extract the heuristically significant features of the objects in question. The simplest methods simply match the objects against standards or prototypes. More powerful "property-list" methods subject each object to a sequence of tests, each detecting some *property* of heuristic importance. These properties have to be invariant under commonly encountered forms of distortion. Two important problems arise here—inventing new useful properties, and combining many properties to form a recognition system. For complex problems, such methods will have to be augmented by facilities for subdividing complex objects and describing the complex relations between their parts.**

Any powerful heuristic program is bound to contain a variety of different methods and techniques. At each step of the problem-solving process the machine will have to decide what aspect of the problem to work on,

and then which method to use. A choice must be made, for we usually cannot afford to try all the possibilities. In order to deal with a goal or a problem, that is, to choose an appropriate method, we have to recognize what kind of thing it is. Thus the need to choose among actions compels us to provide the machine with classification techniques, or means of evolving them. It is of overwhelming importance that the machine have classification techniques which are realistic. But "realistic" can be defined only with respect to the environments to be encountered by the machine, and with respect to the methods available to it. Distinctions which cannot be exploited are not worth recognizing. And methods are usually worthless without classification schemes which can help decide when they are applicable.

A. Teleological Requirements of Classification

The useful classifications are those which match the goals and methods of the machine. The objects grouped together in the classifications should have something of heuristic value in common; they should be "similar" in a useful sense; they should depend on relevant or essential features. We should not be surprised, then, to find ourselves using inverse or teleological expressions to define the classes. We really do want to have a grip on "the class of objects which can be transformed into a result of form Y," that is, the class of objects which will satisfy some goal. One should be wary of the familiar injunction against using teleological language in science. While it is true that talking of goals in some contexts may dispose us towards certain kinds of animistic explanations, this need not be a bad thing in the field of problem-solving; it is hard to see how one can solve problems without thoughts of purposes. The real difficulty with teleological definitions is technical, not philosophical, and arises when they have to be used and not just mentioned. One obviously cannot afford to use for classification a method which actually requires waiting for some remote outcome, if one needs the classification precisely for deciding whether to try out that method. So, in practice, the ideal teleological definitions often have to be replaced by practical approximations, usually with some risk of error; that is, the definitions have to be made *heuristically effective*, or economically usable. This is of great importance. (We can think of "heuristic effectiveness" as contrasted to the ordinary mathematical notion of "effectiveness" which distinguishes those definitions which can be realized at all by machine, regardless of efficiency.)

B. Patterns and Descriptions

It is usually necessary to have ways of assigning *names*—symbolic expressions—to the defined classes. The structure of the names will have a crucial influence on the mental world of the machine, for it determines what kinds of things can be conveniently thought about. There are a variety of ways to assign names. The simplest schemes use what we will call *conventional* (or *proper*) names; here, arbitrary symbols are assigned to classes. But we will also want to use complex *descriptions* or *computed names;* these are constructed for classes by processes which *depend on the class definitions.* To be useful, these should reflect some of the structure of the things they designate, abstracted in a manner relevant to the problem area. The notion of description merges smoothly into the more complex notion of *model;* as we think of it, a model is a sort of active description. It is a thing whose form reflects some of the structure of the thing represented, but which also has some of the character of a working machine.

In Section III we will consider "learning" systems. The behavior of those systems can be made to change in reasonable ways depending on what happened to them in the past. But by themselves, the simple learning systems are useful only in recurrent situations; they cannot cope with any significant novelty. Nontrivial performance is obtained only when learning systems are supplemented with classification or pattern-recognition methods of some inductive ability. For the variety of objects encountered in a nontrivial search is so enormous that we cannot depend on recurrence, and the mere accumulation of records of past experience can have only limited value. Pattern-Recognition, by providing a heuristic connection which links the old to the new, can make learning broadly useful.

What is a "pattern"? We often use the term teleologically to mean a set of objects which can in some (useful) way be treated alike. For each problem area we must ask, "What patterns would be useful for a machine working on such problems?"

The problems of *visual* pattern-recognition have received much attention in recent years and most of our examples are from this area.

1) Prototype-Derived Patterns: The problem of reading *printed* characters is a clear-cut instance of a situation in which the classification is based ultimately on a fixed set of "prototypes"—*e.g.*, the dies from which the

C. Prototype-Derived Patterns

The problem of reading *printed* characters is a clear-cut instance of a situation in which the classification is based ultimately on a fixed set of "prototypes"—*e.g.*, the dies from which the type font was made. The individual marks on the printed page may show the results of many distortions. Some distortions are rather systematic: change in size, position, orientation. Some are of the nature of noise: blurring, grain, low contrast, etc.

If the noise is not too severe, we may be able to manage the identification by what we call a *normalization and template-matching* process. We first remove the differences related to size and position—that is, we *normalize* the input figure. One may do this, for example, by constructing a similar figure inscribed in a certain fixed triangle (see Fig. 2); or one may transform the figure to obtain a certain fixed center of gravity and a unit second central moment. (There is an additional problem

with rotational equivalence where it is not easy to avoid all ambiguities. One does not want to equate "6" and "9". For that matter, one does not want to equate (0, *o*), or (*X*, x) or the *o*'s in x_o and x^o, so that there may be context-dependency involved.) Once normalized, the unknown figure can be compared with *templates* for the prototypes and, by means of some measure of *matching*, choose the best fitting template. Each "matching criterion" will be sensitive to particular forms of noise and distortion, and so will each normalization procedure. The inscribing or boxing method may be sensitive to small specks, while the moment method will be especially sensitive to smearing, at least for thin-line figures, etc. The choice of a matching criterion must depend on the kinds of noise and transformations commonly encountered. Still, for many problems we may get acceptable results by using straightforward correlation methods.

When the class of equivalence transformations is very large, *e.g.*, when local stretching and distortion are present, there will be difficulty in finding a uniform normalization method. Instead, one may have to consider a process of adjusting locally for best fit to the template. (While measuring the matching, one could "jitter" the figure locally; if an improvement were found the process could be repeated using a slightly different change, etc.) There is usually no practical possibility of applying to the figure *all* of the admissible transformations. And to recognize the *topological* equivalence of pairs such as those in Fig. 3 is likely beyond any practical kind of iterative local-improvement or hill-climbing matching procedure. (Such recognitions can be mechanized, though, by methods which follow lines, detect vertices, and build up a *description* in the form, say, of a vertex-connection table.)

The template matching scheme, with its normalization and direct comparison and matching criterion, is just too limited in conception to be of much use in more difficult problems. If the transformation set is large, normalization, or "fitting," may be impractical, especially if there is no adequate heuristic connection on the space of transformations. Furthermore, for each defined pattern, the system has to be presented with a prototype. But if one has in mind a fairly abstract class, one may simply be unable to represent its essential features with one or a very few concrete examples. How could one represent with a single prototype the class of figures which have an even number of disconnected parts? Clearly, the template system has negligible descriptive power. The property-list system frees us from some of these limitations.

D. Property Lists and "Characters"

We define a *property* to be a two-valued function which divides figures into two classes; a figure is said to have or not have the property according to whether the function's value is 1 or 0. Given a number N of distinction properties, we could define as many as 2^n subclasses by their set intersections and, hence, as many as 2^{2^n} *patterns* by combining the properties with AND's and OR's. Thus, if we have three properties, *rectilinear*, *connected*, and *cyclic*, there are eight subclasses (and 256 patterns) defined by their intersections (see Fig. 4).

If the given properties are placed in a fixed order then we can represent any of these elementary regions by a vector, or string of digits. The vector so assigned to each figure will be called the *Character* of that figure (with respect to the sequence of properties in question). (In [9] we use the term *characteristic* for a property without restriction to 2 values.) Thus a square has the Character (1, 1, 1) and a circle the Character (0, 1, 1) for the given sequence of properties.

For many problems one can use such Characters as names for categories and as primitive elements with

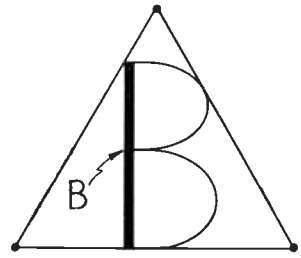

Fig. 2—A simple normalization technique. If an object is expanded uniformly, without rotation, until it touches all three sides of a triangle, the resulting figure will be unique, and pattern-recognition can proceed without concern about relative size and position.

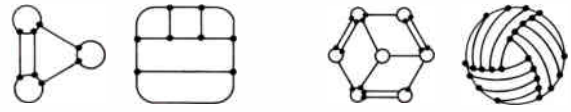

Fig. 3—The figures *A*, *A'* and *B*, *B'* are topologically equivalent pairs. Lengths have been distorted in an arbitrary manner, but the connectivity relations between corresponding points have been preserved. In Sherman [8] and Haller [39] we find computer programs which can deal with such equivalences.

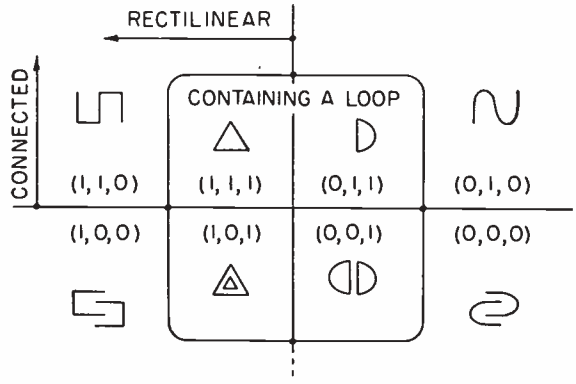

Fig. 4—The eight regions represent all the possible configurations of values of the three properties "rectilinear," "connected," "containing a loop." Each region contains a representative figure, and its associated binary "Character" sequence.

which to define an adequate set of patterns. Characters are more than conventional names. They are instead very rudimentary forms of *description* (having the form of the simplest symbolic expression—the *list*) whose structure provides some information about the designated classes. This is a step, albeit a small one, beyond the template method; the Characters are not simple instances of the patterns, and the properties may themselves be very abstract. Finding a good set of properties is the major concern of many heuristic programs.

E. Invariant Properties

One of the prime requirements of a good property is that it be invariant under the commonly encountered equivalence transformations. Thus for visual Pattern-Recognition we would usually want the object identification to be independent of uniform changes in size and position. In their pioneering paper Pitts and McCulloch [10] describe a general technique for forming invariant properties from noninvariant ones, assuming that the transformation space has a certain (group) structure. The idea behind their mathematical argument is this: suppose that we have a function P of figures, and suppose that for a given figure F we define $[F] = \{F_1, F_2, \cdots\}$ to be the set of all figures equivalent to F under the given set of transformations; further, define $P[F]$ to be the set $\{P(F_1), P(F_2), \cdots\}$ of values of P on those figures. Finally, define $P^*[F]$ to be AVERAGE $(P[F])$. Then we have a new property P^* whose values are independent of the selection of F from an equivalence class defined by the transformations. We have to be sure that when different representatives are chosen from a class the collection $[F]$ will always be the same in each case. In the case of continuous transformation spaces, there will have to be a *measure* or the equivalent associated with the set $[F]$ with respect to which the operation AVERAGE is defined, say, as an integration.[4]

This method is proposed [10] as a neurophysiological model for pitch-invariant hearing and size-invariant visual recognition (supplemented with visual centering mechanisms). This model is discussed also by Wiener.[5] Practical application is probably limited to one-dimensional groups and analog scanning devices.

In much recent work this problem is avoided by using properties already invariant under these transformations. Thus a property might count the number of connected components in a picture—this is invariant under size and position. Or a property may count the number of vertical lines in a picture—this is invariant under size and position (but not rotation).

F. Generating Properties

The problem of generating useful properties has been discussed by Selfridge [12]; we shall summarize his approach. The machine is given, at the start, a few basic transformations $A_1, \cdots, A_n$, each of which transforms,

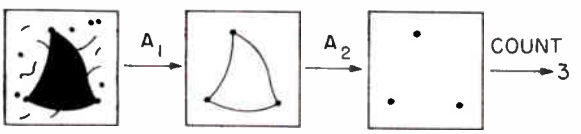

Fig. 5—An arbitrary sequence of picture-transformations, followed by a numerical-valued function, can be used as a *property* function for pictures. A_1 removes all points which are not at the edge of a solid region. A_2 leaves only vertex points—at which an arc suddenly changes direction. The function C simply counts the number of points remaining in the picture. All remarks in the text could be generalized to apply to properties, like A_1A_2C, which can have more than two values.

in some significant way, each figure into another figure. A_1 might, for example, remove all points *not on a boundary* of a solid region; A_2 might leave only *vertex* points; A_3 might *fill up hollow regions*, etc. (see Fig. 5). Each sequence $A_{i_1}A_{i_2}\cdots A_{i_k}$ of these forms a new transformation, so that there is available an infinite variety. We provide the machine also with one or more "terminal" operations which convert a picture into a number, so that any sequence of the elementary transformations, followed by a terminal operation, defines a property. (Dineen [13] describes how these processes were programmed in a digital computer.) We can start with a few short sequences, perhaps chosen randomly. Selfridge describes how the machine might learn new useful properties.

We now feed the machine A's and O's telling the machine each time which letter it is. Beside each sequence under the two letters, the machine builds up distribution functions from the results of applying the sequences to the image. Now, since the sequences were chosen completely randomly, it may well be that most of the sequences have very flat distribution functions; that is, they [provide] no information, and the sequences are therefore [by definition] not significant. Let it discard these and pick some others. Sooner or later, however, some sequences will prove significant; that is, their distribution functions will peak up somewhere. What the machine does now is to build up new sequences *like* the significant ones. This is the important point. If it merely chose sequences at random it might take a very long while indeed to find the best sequences. But with some successful sequences, or partly successful ones, to guide it, we hope that the process will be much quicker. The crucial question remains: how do we build up sequences "like" other sequences, but not identical? As of now we think we shall merely build sequences from the transition frequencies of the significant sequences. We shall build up a matrix of transition frequencies from the significant ones, and use those as transition probabilities with which to choose new sequences.

We do not claim that this method is necessarily a very good way of choosing sequences—only that it should do better than not using

[4] In the case studied in [10] the transformation space is a *group* with a uniquely defined measure: the set $[F]$ can be computed without repetitions by *scanning* through the application of all the transforms T_α to the given figure so that the invariant property can be defined by

$$P^*(F) = \int_{\alpha \in G} P(T_\alpha(F))d\mu$$

where G is the group and μ the measure. By substituting $T_\beta(F)$ for F in this, one can see that the result is independent of choice of β since we obtain the same integral over $G\beta^{-1} = G$.

[5] See p. 160 ff. of [11].

at all the knowledge of what kind of sequences has worked. It has seemed to us that this is the crucial point of learning.[6]

It would indeed be remarkable if this failed to yield properties more useful than would be obtained from completely random sequence selection. The generating problem is discussed further in Minsky [14]. Newell, Shaw, and Simon [15] describe more deliberate, less statistical, techniques that might be used to discover sets of properties appropriate to a given problem area. One may think of the Selfridge proposal as a system which uses a finite-state language to describe its properties. Solomonoff [55], [18] proposes some techniques for discovering common features of a set of expressions, *e.g.*, of the descriptions of those properties of already established utility; the methods can then be applied to generate new properties with the same common features. I consider the lines of attack in [12], [15], [18] and [55], although still incomplete, to be of the greatest importance.

G. Combining Properties

One cannot expect easily to find a *small* set of properties which will be just right for a problem area. It is usually much easier to find a large set of properties each of which provides a little useful information. Then one is faced with the problem of finding a way to combine them to make the desired distinctions. The simplest method is to choose, for each class, a typical character (a particular sequence of property values) and then to use some matching procedure, *e.g.*, counting the numbers of agreements and disagreements, to compare an unknown with these chosen "Character prototypes." The linear weighting scheme described just below is a slight generalization on this. Such methods treat the properties as more or less independent evidence for and against propositions; more general procedures (about which we have yet little practical information) must account also for nonlinear relations between properties, *i.e.*, must contain weighting terms for joint subsets of property values.

1) *"Bayes nets" for combining independent properties:* We consider a single experiment in which an object is placed in front of a property-list machine. Each property E_i will have a value, 0 or 1. Suppose that there has been defined some set of "object classes" F_j, and that we want to use the outcome of this experiment to decide in which of these classes the object belongs.

Assume that the situation is basically probabilistic, and that we know the probability p_{ij} that, if the object is in class F_j then the ith property E_i will have value 1. Assume further that these properties are independent; that is, even given F_j, knowledge of the value of E_i tells us nothing more about the value of a different E_k in the same experiment. (This is a strong condition—see below.) Let ϕ_j be the absolute probability that an object is in class F_j. Finally, for this experiment define V to be the particular set of i's for which the E_i's are 1. Then this V represents the Character of the object. From the definition of conditional probability, we have

$$\Pr(F_j, V) = \Pr(V) \cdot \Pr(F_j \mid V) = \Pr(F_j) \cdot \Pr(V \mid F_j).$$

Given the Character V, we want to guess which F_j has occurred (with the least chance of being wrong—the so-called *maximum likelihood* estimate); that is, for which j is $\Pr(F_j \mid V)$ the largest? Since in the above $\Pr(V)$ does not depend on j, we have only to calculate for which j is $\Pr(F_j) \cdot \Pr(V \mid F_j) = \phi_j \Pr(V \mid F_j)$ the largest. Hence, by our independence hypothesis, we have to maximize

$$\phi \cdot \prod_{i \in V} p_{ij} \cdot \prod_{i \in \bar{V}} q_{ij} = \phi_j \prod_{i \in V} \frac{p_{ij}}{q_{ij}} \cdot \prod_{\text{all } i} q_{ij}. \qquad (1)$$

These "maximum likelihood" decisions can be made (Fig. 6) by a simple network device.[7]

These nets resemble the general schematic diagrams proposed in the "Pandemonium" model of Selfridge [19] (see his Fig. 3). It is proposed there that some intellectual processes might be carried out by a hierarchy of simultaneously functioning submachines suggestively called "demons." Each unit is set to detect certain pat-

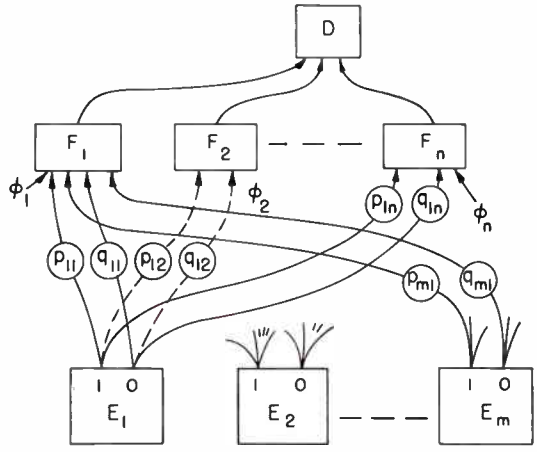

Fig. 6—"Net" model for maximum-likelihood decisions based on linear weightings of property values. The input data are examined by each "property filter" E_i. Each E_i has "0" and "1" output channels, one of which is excited by each input. These outputs are weighted by the corresponding p_{ij}'s, as shown in the text. The resulting signals are multiplied in the F_j units, each of which "collects evidence" for a particular figure class. (We could have used here $\log(p_{ij})$, and *added* at the F_j units.) The final decision is made by the topmost unit D, who merely chooses that F_j with the largest score. Note that the logarithm of the coefficient p_{ij}/q_{ij} in the second expression of (1) can be construed as the "weight of the evidence" of E_i in favor of F_j. (See also [21] and [22].)

[6] See p. 93 of [12].

[7] At the cost of an additional network layer, we may also account for the possible cost g_{jk} that would be incurred if we were to assign to F_k a figure really in class F_j: in this case the minimum cost decision is given by the k for which

$$\sum_j g_{jk}\phi_j \prod_{i \in V} p_{ij} \prod_{i \in \bar{V}} q_{ij}$$

is the least. $\bar{V}$ is the complement set to V; q_{ij} is $(1 - p_{ij})$.

terns in the activity of others and the output of each unit announces the degree of confidence of that unit that it sees what it is looking for. Our E_i units are Selfridge's "data demons." Our units F_j are his "cognitive demons"; each collects from the abstracted data evidence for a specific proposition. The topmost "decision demon" D responds to that one in the multitude below it whose shriek is the loudest.[8]

It is quite easy to add to this "Bayes network model" a mechanism which will enable it to *learn* the optimal connection weightings. Imagine that, after each event, the machine is told which F_j has occurred; we could implement this by sending back a signal along the connections leading to that F_j unit. Suppose that the connection for p_{ij} (or q_{ij}) contains a two-terminal device (or "synapse") which stores a number w_{ij}. Whenever the joint event $(F_j, E_i=1)$ occurs, we modify w_{ij} by replacing it by $(w_{ij}+1)\theta$, where θ is a factor slightly less than unity. And when the joint event $(F_j, E_i=0)$ occurs, we decrement w_{ij} by replacing it with $(w_{ij})\theta$. It is not difficult to show that the expected values of the w_{ij}'s will become proportional to the p_{ij}'s [and, in fact, approach $p_{ij}[\theta/(1-\theta)]$. Hence, the machine tends to learn the optimal weighting on the basis of experience. (One must put in a similar mechanism for estimating the ϕ_j's.) The variance of the normalized weight $w_{ij}[(1-\theta)/\theta]$ approaches $[(1-\theta)/(1+\theta)]p_{ij}q_{ij}$. Thus a small value for θ means rapid learning but is associated with a large variance, hence, with low reliability. Choosing θ close to unity means slow, but reliable, learning. θ is really a sort of memory decay constant, and its choice must be determined by the noise and stability of the environment—much noise requires long averaging times, while a changing environment requires fast adaptation. The two requirements are, of course, incompatible and the decision has to be based on an economic compromise.[9]

2) Possibilities of using random nets for Bayes decisions: The nets of Fig. 6 are very orderly in structure. Is all this structure necessary? Certainly if there were a great many properties, *each of which provided very little marginal information*, some of them would not be missed. Then one might expect good results with a mere sampling of all the possible connection paths w_{ij}. And one might thus, *in this special situation*, use a random connection net.

The two-layer nets here resemble those of the "perceptron" proposal of Rosenblatt [22]. In the latter, there is an additional level of connections coming directly from randomly selected points of a "retina." Here the properties, the devices which abstract the visual input data, are simple functions which add some inputs, subtract others, and detect whether the result exceeds a threshold. Eq. (1), we think, illustrates what is of value in this scheme. It does seem clear that a maximum-likelihood type of analysis of the output of the property functions can be handled by such nets. But these nets, with their simple, randomly generated, connections can probably never achieve recognition of such patterns as "the class of figures having two separated parts," and they cannot even achieve the effect of template recognition without size and position normalization (unless sample figures have been presented previously in essentially all sizes and positions). For the chances are extremely small of finding, by random methods, enough properties usefully correlated with patterns appreciably more abstract than those of the prototype-derived kind. And these networks can really only separate out (by weighting) information in the individual input properties; they cannot extract further information present in nonadditive form. The "perceptron" class of machines have facilities neither for obtaining better-than-chance properties nor for assembling better-than-additive combinations of those it gets from random construction.[10]

For recognizing *normalized* printed or hand-printed characters, single-point properties do surprisingly well [23]; this amounts to just "averaging" many samples. Bledsoe and Browning [24] claim good results with point-pair properties. Roberts [25] describes a series of experiments in this general area. Doyle [26] without normalization but with quite sophisticated properties obtains excellent results; his properties are already substantially size- and position-invariant. A general review of Doyle's work and other pattern-recognition experiments will be found in Selfridge and Neisser [20].

For the complex discrimination, *e.g.*, between one and two connected objects, the property problem is very serious, especially for long wiggly objects such as are handled by Kirsch [27]. Here some kind of recursive processing is required and combinations of simple properties would almost certainly fail even with large nets and long training.

We should not leave the discussion of some decision net models without noting their important limitations. The hypothesis that, for given j, the p_{ij} represent independent events, is a very strong condition indeed. Without this hypothesis we could still construct maximum-likelihood nets, but we would need an additional layer of cells to represent all of the joint events V; that is, we would need to know all the Pr $(F_j|\ V)$. This gives a general (but trivial) solution, but requires 2^n cells for n properties, which is completely impractical for large systems. What is required is a system which computes some sampling of all the joint conditional probabilities, and uses these to estimate others when needed. The work of Uttley [28], [29], bears on this problem, but his proposed and experimental devices do not yet clearly show how to avoid exponential growth.[11]

[8] See also the report in [20].
[9] See also [7] and [21].
[10] See also Roberts [25], Papert [21], and Hawkins [22]. We can find nothing resembling an analysis [see (1) abve] in [22] or subsequent publications of Rosenblatt.
[11] See also Papert [21].

H. Articulation and Attention—Limitations of the Property-List Method

Because of its fixed size, the property-list scheme is limited (for any given set of properties) in the detail of the distinctions it can make. Its ability to deal with a compound scene containing several objects is critically weak, and its direct extensions are unwieldy and unnatural. If a machine can recognize a chair and a table, it surely should be able to tell us that "there is a chair and a table." To an extent, we can invent properties which allow some capacity for superposition of object Characters.[12] But there is no way to escape the information limit.

What is required is clearly 1) a *list* (*of whatever length is necessary*) of the primitive objects in the scene and 2) a statement about the relations among them. Thus we say of Fig. 7(a), "A rectangle (1) contains two subfigures disposed horizontally. The part on the left is a rectangle (2) which contains two subfigures disposed vertically; the upper a circle (3) and the lower a triangle (4). The part on the right . . . etc." Such a description entails an ability to separate or "articulate" the scene into parts. (Note that in this example the articulation is essentially *recursive;* the figure is first divided into two parts; then each part is described using the same machinery.) We can formalize this kind of description in an expression language whose fundamental grammatical form is a pair (R, L) whose first member R names a *relation* and whose second member L is an *ordered list* $(x_1, x_2, \cdots, x_n)$ of the objects or subfigures which bear that relation to one another. We obtain the required flexibility by allowing the members of the list L to contain not only the names of "elementary" figures but also "subexpressions" of the form (R, L) designating complex subfigures. Then our scene above may be described by the expression

$$[\odot, (\square, (\rightarrow, \{(\odot, (\square, (\downarrow, (\bigcirc, \triangle)))), (\odot, (\bigcirc, (\triangledown, (\bigcirc, \bigcirc, \bigcirc))))\}))]$$

(a) (b) (c)

Fig. 7—The picture 4(a) is first described verbally in the text. Then, by introducing notation for the relations "inside of," "to the left of" and "above," we construct a symbolic description. Such descriptions can be formed and manipulated by machines. By abstracting out the complex relation between the parts of the figure we can use the same formula to describe the related pictures 4(b) and 4(c), changing only the list of primitive parts. It is up to the programmer to decide at just what level of complexity a part of a picture should be considered "primitive"; this will depend on what the description is to be used for. We could further divide the drawings into vertices, lines, and arcs. Obviously, for some applications the relations would need more metrical information, *e.g.*, specification of lengths or angles.

[12] Cf. Mooers' technique of Zatocoding [30], [31].

where $(\odot, (x, y))$ means that y is contained in x; $(\rightarrow, (x, y))$ means that y is to the right of x; $(\downarrow, (x, y))$ means that y is below x, and $(\triangledown, (x, y, z))$ means that y is to the right of x and z is underneath and between them. The symbols $\square$, $\bigcirc$, and $\triangle$ represent the indicated kinds of primitive geometric objects. This expression-pair description language may be regarded as a simple kind of "list-structure" language. Powerful computer techniques have been developed, originally by Newell, Shaw and Simon, for manipulating symbolic expressions in such languages for purposes of heuristic programming. (See the remarks at the end of Section IV. If some of the members of a list are themselves lists, they must be surrounded by exterior parentheses, and this accounts for the accumulation of parentheses.)

It may be desirable to construct descriptions in which the complex relation is extracted, *e.g.*, so that we have an expression of the form FG where F is an expression which at once denotes the composite relation between all the primitive parts listed in G. A complication arises in connection with the "binding" of variables, *i.e.*, in specifying the manner in which the elements of G participate in the relation F. This can be handled in general by the "λ" notation [32] but here we can just use integers to order the variables.

For the given example, we could describe the relational part F by an expression

$$\odot(1, \rightarrow(\odot(2, \downarrow(3, 4)), \odot(5, \triangledown(6, 7, 8))))$$

in which we now use a "functional notation"; "$(\odot, (x, y))$" is replaced by "$\odot(x, y)$," etc., making for better readability. To obtain the desired description, this expression has to be applied to an ordered list of primitive objects, which in this case is $(\square, \square, \bigcirc, \triangle, \bigcirc, \bigcirc, \bigcirc, \bigcirc)$. This composite functional form allows us to abstract the composite relation. By changing only the object list we can obtain descriptions also of the objects in Fig. 7(b) and 7(c).

The important thing about such "articular" descriptions is that they can be obtained by *repeated application of a fixed set of pattern-recognition techniques.* Thus we can obtain *arbitrarily complex* descriptions from a fixed complexity classification-mechanism. The new element required in the mechanism (beside the capacity to manipulate the list-structures) is the ability to articulate—to "attend fully" to a selected part of the picture and bring all one's resources to bear on that part. In efficient problem-solving programs, we will not usually complete such a description in a single operation. Instead, the depth or detail of description will be under the control of other processes. These will reach deeper, or look more carefully, only when they have to, *e.g.*, when the presently available description is inadequate for a current goal. The author, together with L. Hodes, is working on pattern-recognition schemes using articular descriptions. By manipulating the formal descrip-

tions we can deal with overlapping and incomplete figures, and several other problems of the "Gestalt" type.

It seems likely that as machines are turned toward more difficult problem areas, *passive* classification systems will become less adequate, and we may have to turn toward schemes which are based more on internally-generated hypotheses, perhaps "error-controlled" along the lines proposed by MacKay [89].

Space requires us to terminate this discussion of pattern-recognition and description. Among the important works not reviewed here should be mentioned those of Bomba [33] and Grimsdale, *et al.* [34], which involve elements of description, Unger [35] and Holland [36] for parallel processing schemes, Hebb [37] who is concerned with physiological description models, and the work of the Gestalt psychologists, notably Kohler [38] who have certainly raised, if not solved, a number of important questions. Sherman [8], Haller [39] and others have completed programs using line-tracing operations for topological classification. The papers of Selfridge [12], [43], have been a major influence on work in this general area.

See also Kirsch, *et al.* [27], for discussion of a number of interesting computer image-processing techniques, and see Minot [40] and Stevens [41] for reviews of the reading machine and related problems. One should also examine some biological work, *e.g.*, Tinbergen [42] to see instances in which some discriminations which seem, at first glance very complicated are explained on the basis of a few apparently simple properties arranged in simple decision trees.

III. Learning Systems

***Summary*—In order to solve a new problem, one should first try using methods similar to those that have worked on similar problems. To implement this "basic learning heuristic" one must generalize on past experience, and one way to do this is to use success-reinforced decision models. These learning systems are shown to be averaging devices. Using devices which learn also which events are associated with reinforcement, *i.e.*, reward, we can build more autonomous "secondary reinforcement" systems. In applying such methods to complex problems, one encounters a serious difficulty—in distributing credit for success of a complex strategy among the many decisions that were involved. This problem can be managed by arranging for local reinforcement of partial goals within a hierarchy, and by grading the training sequence of problems to parallel a process of maturation of the machine's resources.**

In order to solve a new problem one uses what might be called the basic learning heuristic—first try using methods similar to those which have worked, in the past, on similar problems. We want our machines, too, to benefit from their past experience. Since we cannot expect new situations to be precisely the same as old ones, any useful learning will have to involve generalization techniques. There are too many notions associated with "learning" to justify defining the term precisely. But we may be sure that any useful learning system will have to use records of the past as *evidence for more general propositions*; it must thus entail some commitment or other about "inductive inference." (See Section V-B.) Perhaps the simplest way of generalizing about a set of entities is through constructing a new one which is an "ideal," or rather, a typical member of that set; the usual way to do this is to smooth away variation by some sort of averaging technique. And indeed we find that most of the *simple* learning devices do incorporate some averaging technique—often that of averaging some sort of product, thus obtaining a sort of correlation. We shall discuss this family of devices here, and some more abstract schemes in Section V.

A. Reinforcement

A reinforcement process is one in which some aspects of the behavior of a system are caused to become more (or less) prominent in the future as a consequence of the application of a "reinforcement operator" Z. This operator is required to affect only those aspects of behavior for which instances have actually occurred recently.

The analogy is with "reward" or "extinction" (not punishment) in animal behavior. The important thing about this kind of process is that it is "operant" (a term of Skinner [44]); the reinforcement operator does not initiate behavior, but merely selects that which the Trainer likes from that which has occurred. Such a system must then contain a device M which generates a variety of behavior (say, in interacting with some environment) and a Trainer who makes critical judgments in applying the available reinforcement operators. (See Fig. 8.)

Let us consider a very simple reinforcement model. Suppose that on each presentation of a stimulus S an animal has to make a choice, *e.g.*, to turn left or right, and that its probability of turning right, at the nth trial, is p_n. Suppose that *we* want it to turn right. Whenever it does this we might "reward" it by applying the operator Z_+;

$$p_{n+1} = Z_+(p_n) = \theta p_n + (1 - \theta) \qquad 0 < \theta < 1$$

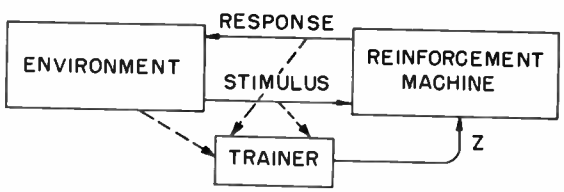

Fig. 8—Parts of an "operant reinforcement" learning system. In response to a stimulus from the environment, the machine makes one of several possible responses. It remembers what decisions were made in choosing this response. Shortly thereafter, the Trainer sends to the machine positive or negative reinforcement (reward) signal; this increases or decreases the tendency to make the same decisions in the future. Note that the Trainer need not know how to solve problems, but only how to detect success or failure, or relative improvement; his function is selective. The Trainer might be connected to observe the actual stimulus-response activity or, in a more interesting kind of system, just some function of the state of the environment.

which moves p a fraction $(1-\theta)$ of the way towards unity.[13] If we dislike what it does we apply negative reinforcement.

$$p_{n+1} = Z_{-}(p_n) = \theta p_n$$

moving p the same fraction of the way toward 0. Some theory of such "linear" learning operators, generalized to several stimuli and responses, will be found in Bush and Mosteller [45]. We can show that the learning result is an average weighted by an exponentially-decaying time factor: Let Z_n be ± 1 according to whether the nth event is rewarded or extinguished and replace p_n by $c_n = 2p_n - 1$ so that $-1 \leq c_n \leq 1$, as for a correlation coefficient. Then (with $c_0 = 0$) we obtain by induction

$$c_{n+1} = (1 - \theta) \sum_{i=0}^{n} \theta^{n-i} Z_i,$$

and since

$$1/(1 - \theta) \approx \sum_{0}^{n} \theta^{n-i},$$

we can write this as

$$c_{n+1} \approx \frac{\sum \theta^{n-i} Z_i}{\sum \theta^{n-i}}. \tag{1}$$

If the term Z_i is regarded as a product of i) how the creature responded and ii) which kind of reinforcement was given, then c_n is a kind of correlation function (with the decay weighting) of the joint behavior of these quantities. The ordinary, uniformly-weighted average has the same general form but with time-dependent θ:

$$c_{n+1} = \left(1 - \frac{1}{N}\right) c_n + \frac{1}{N} Z_n. \tag{2}$$

In (1) we have again the situation described in Section II-G, 1; a small value of θ gives fast learning, and the possibility of quick adaptation to a changing environment. A near-unity value of θ gives slow learning, but also smooths away uncertainties due to noise. As noted in Section II-G, 1, the response distribution comes to approximate the probabilities of rewards of the alternative responses. (The importance of this phenomenon has, I think, been overrated; it is certainly not an especially rational strategy. One reasonable alternative is that of computing the numbers p_{ij} as indicated, but actually playing at each trial the "most likely" choice. Except in the presence of a hostile opponent, there is usually no reason to play a "mixed" strategy.[14])

In Samuel's coefficient-optimizing program [2] [see Section III-C, 1)], there is a most ingenious compromise between the exponential and the uniform averaging methods: the value of N in (2) above begins at 16 and so remains until $n = 16$, then N is 32 until $n = 32$, and so on until $n = 256$. Thereafter N remains fixed at 256. This nicely prevents violent fluctuations in c_n at the start, approaches the uniform weighting for a while, and finally approaches the exponentially-weighted correlation, all in a manner that requires very little computation effort! Samuel's program is at present the outstanding example of a game-playing program which matches average human ability, and its success (in real time) is attributed to a wealth of such elegancies, both in heuristics and in programming.

The problem of extinction or "unlearning" is especially critical for complex, hierarchical, learning. For, once a generalization about the past has been made, one is likely to build upon it. Thus, one may come to select certain properties as important and begin to use them in the characterization of experience, perhaps storing one's memories in terms of them. If later it is discovered that some other properties would serve better, then one must face the problem of translating, or abandoning, the records based on the older system. This may be a very high price to pay. One does not easily give up an old way of looking at things, if the better one demands much effort and experience to be useful. Thus the *training sequences* on which our machines will spend their infancies, so to speak, must be chosen very shrewdly to insure that early abstractions will provide a good foundation for later difficult problems.

Incidentally, in spite of the space given here for their exposition, I am not convinced that such "incremental" or "statistical" learning schemes should play a central role in our models. They will certainly continue to appear as components of our programs but, I think, mainly by default. The more intelligent one is, the more often he should be able to learn from an experience something rather definite; *e.g.*, to reject or accept a hypothesis, or to change a goal. (The obvious exception is that of a truly statistical environment in which averaging is inescapable. But the heart of problem-solving is always, we think, the combinatorial part that gives rise to searches, and we should usually be able to regard the complexities caused by "noise" as mere annoyances, however irritating they may be.) In this connection we can refer to the discussion of memory in Miller, Galanter and Pribram [46].[15] This seems to be the first major work in Psychology to show the influence of work in the artificial intelligence area, and its programme is generally quite sophisticated.

B. Secondary Reinforcement and Expectation Models

The simple reinforcement system is limited by its dependence on the Trainer. If the Trainer can detect only

[13] Properly, the reinforcenent functions should depend both on the p's and on the previous reaction—reward should *decrease* p if our animal has just turned to the left. The notation in the literature is also somewhat confusing in this regard.

[14] The question of just how often one should play a strategy different from the estimated optimum, in order to gain information, is an underlying problem in many fields. See, *e.g.*, [85].

[15] See especially ch. 10.

the *solution* of a problem, then we may encounter "mesa" phenomena which will limit performance on difficult problems. (See Section I-C.) One way to escape this is to have the machine learn to generalize on what the Trainer does. Then, in difficult problems, it may be able to give itself partial reinforcements along the way, *e.g.*, upon the solution of relevant subproblems. The machine in Fig. 9 has some such ability. The new unit

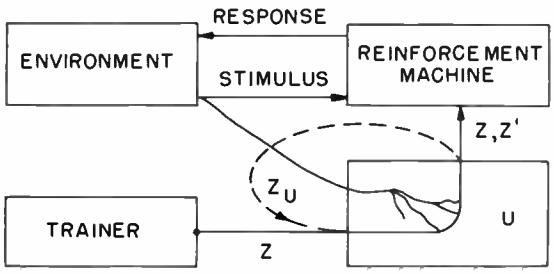

Fig. 9—An additional device U gives the machine of Fig. 8 the ability to learn which signals from the environment have been associated with reinforcement. The primary reinforcement signals Z are routed through U. By a Pavlovian conditioning process (not described here), external signals come to produce reinforcement signals like those that have frequently succeeded them in the past. Such signals might be abstract, *e.g.*, verbal encouragement. If the "secondary reinforcement" signals are allowed, in turn, to acquire further external associations (through, *e.g.*, a channel Z_U as shown) the machine might come to be able to handle chains of subproblems. But something must be done to stabilize the system against the positive symbolic feedback loop formed by the path Z_U. The profound difficulty presented by this stabilization problem may be reflected in the fact that, in lower animals, it is very difficult to demonstrate such chaining effects.

U is a device that learns which external stimuli are strongly correlated with the various reinforcement signals, and responds to such stimuli by reproducing the corresponding reinforcement signals. (The device U is *not* itself a reinforcement learning device; it is more like a "Pavlovian" conditioning device, treating the Z signals as "unconditioned" stimuli and the S signals as conditioned stimuli.) The heuristic idea is that any signal from the environment which in the past has been well correlated with (say) positive reinforcement is likely to be an indication that something good has just happened. If the training on early problems was such that this is realistic, then the system eventually should be able to detach itself from the Trainer, and become autonomous. If we further permit "chaining" of the "secondary reinforcers," *e.g.*, by admitting the connection shown as a dotted line in Fig. 9, the scheme becomes quite powerful, in principle. There are obvious pitfalls in admitting such a degree of autonomy; the values of the system may drift to a "nonadaptive" condition.

C. Prediction and Expectation

The evaluation unit U is supposed to acquire an ability to tell whether a situation is good or bad. This evaluation could be applied to *imaginary* situations as well as to real ones. If we could estimate the consequences of a proposed action (without its actual execution), we could use U to evaluate the (estimated) resulting situation. This could help in reducing the effort in search, and we would have in effect a machine with some ability to look ahead, or *plan*. In order to do this we need an additional device P which, given the descriptions of a situation and an action, will predict a description of the likely result. (We will discuss schemes for doing this in Section IV-C.) The device P might be constructed along the lines of a reinforcement learning device. In such a system the required reinforcement signals would have a very attractive character. For the machine must reinforce P positively when the *actual outcome resembles that which was predicted*—accurate expectations are rewarded. If we could further add a premium to reinforcement of those predictions which have a novel aspect, we might expect to discern behavior motivated by a sort of curiosity. In the reinforcement of mechanisms for confirmed novel expectations (or new explanations) we may find the key to simulation of intellectual motivation.[16]

Samuel's Program for Checkers: In Samuel's "generalization learning" program for the game of checkers [2] we find a novel heuristic technique which could be regarded as a simple example of the "expectation reinforcement" notion. Let us review very briefly the situation in playing two-person board games of this kind. As noted by Shannon [3] such games are in principle finite, and a best strategy can be found by following out all possible continuations—if he goes there I can go there, or there, etc.—and then "backing-up" or "minimaxing" from the terminal positions, won, lost, or drawn. But in practice the full exploration of the resulting colossal "move-tree" is out of the question. No doubt, some exploration will always be necessary for such games. But the tree must be pruned. We might simply put a limit on depth of exploration—the number of moves and replies. We might also limit the number of alternatives explored from each position—this requires some heuristics for selection of "plausible moves."[17] Now, if the backing-up technique is still to be used (with the incomplete move-tree) one has to substitute for the absolute "win, lose, or draw" criterion some other "static" way of evaluating nonterminal positions.[18] (See Fig. 10.) Perhaps the simplest scheme is to use a weighted sum of some selected set of "property" functions of the positions—mobility, advancement, center control, and the like. This is done in Samuel's program, and in most of its predecessors. Associated with this is a multiple-simultaneous-optimizer method

[16] See also ch. 6 of [47].

[17] See the discussion of Bernstein [48] and the more extensive review and discussion in the very suggestive paper of Newell, Shaw, and Simon [49]; one should not overlook the pioneering paper of Newell [50], and Samuel's discussion of the minimaxing process in [2].

[18] In some problems the backing-up process can be handled in closed analytic form so that one may be able to use such methods as Bellman's "Dynamic Programming" [51]. Freimer [52] gives some examples for which limited "look-ahead" doesn't work.

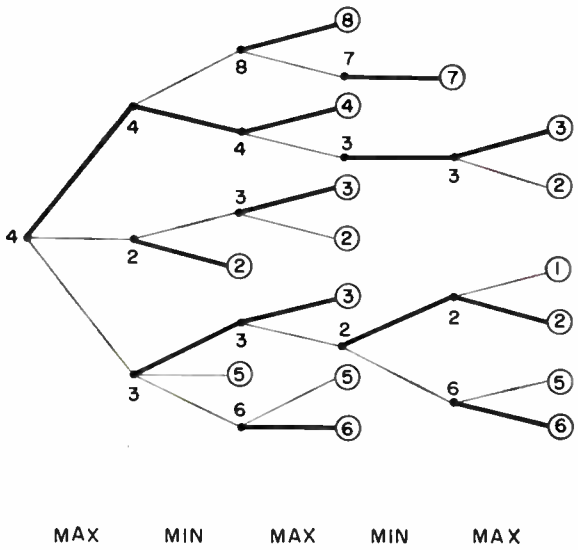

Fig. 10—"Backing-up" the static evaluations of proposed moves in a game-tree. From the vertex at the left, representing the present position in a board game, radiate three branches, representing the *player's* proposed moves. Each of these might be countered by a variety of *opponent* moves, and so on. According to some program, a finite tree is generated. Then the worth to the player of each terminal board position is estimated. (See text.) If the opponent has the same values, he will choose to minimize the score, while the player will always try to maximize. The heavy lines show how this minimaxing process backs up until a choice is determined for the present position.

The full tree for chess has the order of 10^{120} branches—beyond the reach of any man or computer. There is a fundamental heuristic exchange between the effectiveness of the evaluation function and the extent of the tree. A very weak evaluation (*e.g.*, one which just compares the players' values of pieces) would yield a devastating game if the machine could explore all continuations out to, say, 20 levels. But only 6 levels, roughly within range of our presently largest computers, would probably not give a brilliant game; less exhaustive strategies, perhaps along the lines of [49], would be more profitable.

for discovering a good coefficient assignment (using the correlation technique noted in Section III-A). But the source of reinforcement signals in [2] is novel. One cannot afford to play out one or more entire games for each single learning step. Samuel measures instead *for each move* the difference between what the evaluation function yields *directly* of a position and what it *predicts* on the basis of an extensive continuation exploration, *i.e.*, backing-up. The sign of this error, "Delta," is used for reinforcement; thus the system may learn something at *each move*.[19]

D) The Basic Credit-Assignment Problem for Complex Reinforcement Learning Systems

In playing a complex game such as chess or checkers, or in writing a computer program, one has a definite success criterion—the game is won or lost. But in the course of play, each ultimate success (or failure) is associated with a vast number of internal decisions. If the run is successful, how can we assign credit for the success among the multitude of decisions? As Newell noted,

> It is extremely doubtful whether there is enough information in "win, lose, or draw" when referred to the whole play of the game to permit any learning at all over available time scales. . . . For learning to take place, each play of the game must yield much more information. This is . . . achieved by breaking the problem into components. The unit of success is the goal. If a goal is achieved, its subgoals are reinforced; if not they are inhibited. (Actually, what is reinforced is the transformation rule that provided the subgoal.) . . . This also is true of the other kinds of structure: every tactic that is created provides information about the success or failure of tactic search rules; every opponent's action provides information about success or failure of likelihood inferences; and so on. The amount of information relevant to learning increases directly with the number of mechanisms in the chess-playing machine.[20]

We are in complete agreement with Newell on this approach to the problem.[21]

It is my impression that many workers in the area of "self-organizing" systems and "random neural nets" do not feel the urgency of this problem. Suppose that one million decisions are involved in a complex task (such as winning a chess game). Could we assign to each decision element one-millionth of the credit for the completed task? In certain special situations we can do just this—*e.g.*, in the machines of [22], [25] and [92], etc., where the connections being reinforced are to a sufficient degree independent. But the problem-solving ability is correspondingly weak.

For more complex problems, with decisions in hierarchies (rather than summed on the same level) and with increments small enough to assure probable convergence, the running times would become fantastic. For complex problems we will have to define "success" in some rich local sense. Some of the difficulty may be evaded by using carefully graded "training sequences" as described in the following section.

Friedberg's Program-Writing Program: An important example of comparative failure in this credit-assignment matter is provided by the program of Friedberg [53], [54] to solve program-writing problems. The problem here is to write programs for a (simulated) very simple digital computer. A simple problem is assigned, *e.g.*, "compute the AND of two bits in storage and put the result in an assigned location." A generating device produces a random (64-instruction) program. The program is run and its success or failure is noted. The success information is used to reinforce *individual instructions* (in fixed locations) so that each success tends to increase the chance that the instructions of successful programs will appear in later trials. (We lack space for details of how this is done.) Thus the program tries

[19] It should be noted that [2] describes also a rather successful checker-playing program based on recording and retrieving information about positions encountered in the past, a less abstract way of exploiting past experience. Samuel's work is notable in the variety of experiments that were performed, with and without various heuristics. This gives an unusual opportunity to really find out how different heuristic methods compare. More workers should choose (other things being equal) problems for which such variations are practicable.

[20] See p. 108 of [50].

[21] See also the discussion in Samuel (p. 22 of [2]) on assigning credit for a change in "Delta."

to find "good" instructions, more or less independently, for each location in program memory. The machine did learn to solve some extremely simple problems. But it took of the order of 1000 times longer than pure chance would expect. In part II of [54], this failure is discussed, and attributed in part to what we called (Section I-C) the "Mesa phenomena." In changing just one instruction at a time the machine had not taken large enough steps in its search through program space.

The second paper goes on to discuss a sequence of modifications in the program generator and its reinforcement operators. With these, and with some "priming" (starting the machine off on the right track with some useful instructions), the system came to be only a little worse than chance. The authors of [54] conclude that with these improvements "the generally superior performance of those machines with a success-number reinforcement mechanism over those without does serve to indicate that such a mechanism can provide a basis for constructing a learning machine." I disagree with this conclusion. It seems to me that each of the "improvements" can be interpreted as serving only to increase the step size of the search, that is, the randomness of the mechanism; this helps to avoid the Mesa phenomenon and thus approach chance behavior. But it certainly does not show that the "learning mechanism" is working—one would want at least to see some better-than-chance results before arguing this point. The trouble, it seems, is with credit-assignment. The credit for a working program can only be assigned to functional groups of instructions, *e.g.*, subroutines, and as these operate in hierarchies we should not expect individual instruction reinforcement to work well.[22] It seems surprising that it was not recognized in [54] that the doubts raised earlier were probably justified! In the last section of [54] we see some real success obtained by breaking the problem into parts and solving them sequentially. (This successful demonstration using division into subproblems does not use any reinforcement mechanism at all.) Some experiments of similar nature are reported in [94].

It is my conviction that no scheme for learning, or for pattern-recognition, can have very general utility unless there are provisions for recursive, or at least hierarchical, use of previous results. We cannot expect a learning system to come to handle very hard problems without preparing it with a reasonably graded sequence of problems of growing difficulty. The first problem must be one which can be solved in reasonable time with the initial resources. The next must be capable of solution in reasonable time by using reasonably simple and accessible combinations of methods developed in the first, and so on. The only alternatives to this use of an adequate "training sequence" are 1) advanced resources, given initially, or 2) the fantastic exploratory processes found perhaps only in the history of organic evolution.[23] And even there, if we accept the general view of Darlington [56] who emphasizes the heuristic aspects of genetic systems, we must have developed early (in, *e.g.*, the phenomena of meiosis and crossing-over) quite highly specialized mechanisms providing for the segregation of groupings related to solutions of subproblems. Recently, much effort has been devoted to the construction of training sequences in connection with programming "teaching machines." Naturally, the psychological literature abounds with theories of how complex behavior is built up from simpler. In our own area, perhaps the work of Solomonoff [55], while overly cryptic, shows the most thorough consideration of this dependency on *training sequences*.

[22] See the introduction to [53] for a thoughtful discussion of the plausibility of the scheme.

IV. Problem-Solving and Planning

***Summary*—The solution, by machine, of really complex problems will require a variety of administration facilities. During the course of solving a problem, one becomes involved with a large assembly of interrelated subproblems. From these, at each stage, a very few must be chosen for investigation. This decision must be based on 1) estimates of relative difficulties and 2) estimates of centrality of the different candidates for attention. Following subproblem selection (for which several heuristic methods are proposed), one must choose methods appropriate to the selected problems. But for really difficult problems, even these step-by-step heuristics for reducing search will fail, and the machine must have resources for analyzing the problem structure in the large—in short, for "planning." A number of schemes for planning are discussed, among them the use of models—analogous, semantic, and abstract. Certain abstract models, "Character Algebras," can be constructed by the machine itself, on the basis of experience or analysis. For concreteness, the discussion begins with a description of a simple but significant system (LT) which encounters some of these problems.**

A. The "Logic Theory" Program of Newell, Shaw and Simon

It is not surprising that the testing grounds for early work on mechanical problem-solving have usually been areas of mathematics, or games, in which the rules are defined with absolute clarity. The "Logic Theory" machine of [57], [58], called "LT" below, was a first attempt to prove theorems in logic, by frankly heuristic methods. Although the program was not by human standards a brilliant success (and did not surpass its designers), it stands as a landmark both in heuristic programming and also in the development of modern automatic programming.

The problem domain here is that of discovering proofs in the Russell-Whitehead system for the propositional calculus. That system is given as a set of (five) axioms and (three) rules of inference; the latter specify how

[23] It should, however, be possible to construct learning mechanisms which can select for themselves reasonably good training sequences (from an always complex environment) by pre-arranging a relatively slow development (or "maturation") of the system's facilities. This might be done by pre-arranging that the sequence of goals attempted by the primary Trainer match reasonably well, at each stage, the complexity of performance mechanically available to the pattern-recognition and other parts of the system. One might be able to do much of this by simply limiting the depth of hierarchical activity, perhaps only later permitting limited recursive activity.

certain transformations can be applied to produce new theorems from old theorems and axioms.

The LT program is centered around the idea of "working backwards" to find a proof. Given a theorem T to be proved, LT searches among the axioms and previously established theorems for one from which T can be deduced by a single application of one of three simple "Methods" (which embody the given rules of inference). If one is found, the problem is solved. Or the search might fail completely. But finally, the search may yield one or more "problems" which are usually propositions from which T may be deduced directly. If one of these can, in turn, be proved a theorem the main problem will be solved. (The situation is actually slightly more complex.) Each such subproblem is adjoined to the "subproblem list" (after a limited preliminary attempt) and LT works around to it later. The full power of LT, such as it is, can be applied to each subproblem, for LT can use itself as a subroutine in a recursive fashion.

The heuristic technique of working backwards yields something of a teleological process, and LT is a forerunner of more complex systems which construct hierarchies of goals and subgoals. Even so, the basic administrative structure of the program is no more than a nested set of searches through lists in memory. We shall first outline this structure and then mention a few heuristics that were used in attempts to improve performance.

1) Take the next problem from problem list.
   (If there are no more problems, EXIT with total failure.)
2) Choose the next of the three basic Methods.
   (If no more methods, go to 1.)
3) Choose the next member of the list of axioms and previous theorems.
   (If no more, go to 2.)
   Then apply the Method to the problem, using the chosen theorem or axiom.
   If problem is solved, EXIT with complete proof.
   If no result, go to 3.
   If new subproblem arises, go to 4.
4) Try the special (substitution) Method on the subproblem.
   If problem is solved, EXIT with complete proof.
   If no result, put the subproblem *at the end* of the problem list and go to 3.

Among the heuristics that were studied were 1) a *similarity test* to reduce the work in step 4 (which includes another search through the theorem list), 2) a *simplicity test* to select apparently easier problems from the problem list, and 3) a *strong nonprovability test* to remove from the problem list expressions which are probably false and hence not provable. In a series of experiments "learning" was used to find which earlier theorems had been most useful and should be given priority in step 3. We cannot review the effects of these changes in detail. Of interest was the balance between the extra cost for administration of certain heuristics and the resultant search reduction; this balance was quite delicate in some cases when computer memory became saturated. The system seemed to be quite sensitive to the training sequence—the order in which problems were given. And some heuristics which gave no significant over-all improvement did nevertheless affect the class of solvable problems. Curiously enough, the general efficiency of LT was not greatly improved by any or all of these devices. But all this practical experience is reflected in the design of the much more sophisticated "GPS" system described briefly in Section IV-D, 2).

Wang [59] has criticized the LT project on the grounds that there exist, as he and others have shown, mechanized proof methods which, for the particular run of problems considered, use far less machine effort than does LT and which have the advantage that they will ultimately find a proof for any provable proposition. (LT does not have this exhaustive "decision procedure" character and can fail ever to find proofs for some theorems.) The authors of [58], perhaps unaware of the existence of even moderately efficient exhaustive methods, supported their arguments by comparison with a particularly inefficient exhaustive procedure. Nevertheless, I feel that some of Wang's criticisms are misdirected. He does not seem to recognize that the authors of LT are not so much interested in proving these theorems as they are in the general problem of solving difficult problems. The combinatorial system of Russell and Whitehead (with which LT deals) is far less simple and elegant than the system used by Wang.[24] (Note, *e.g.*, the emphasis in [49] and [60].) Wang's problems, while *logically* equivalent, are *formally* much simpler. His methods do not include any facilities for using previous results (hence they are sure to degrade rapidly at a certain level of problem complexity), while LT is fundamentally oriented around this problem. Finally, because of the very effectiveness of Wang's method on the *particular* set of theorems in question, he simply did not have to face the fundamental heuristic problem of *when to decide to give up on a line of attack*. Thus the formidable performance of his program [59] perhaps diverted his attention from heuristic problems that must again spring up when real mathematics is ultimately encountered.

This is not meant as a rejection of the importance of Wang's work and discussion. He and others working on "mechanical mathematics" have discovered that there are proof procedures which are much more efficient than has been suspected. Such work will unquestionably help in constructing intelligent machines, and

[24] Wang's procedure [59] too, works backwards, and can be regarded as a generalization of the method of "falsification" for deciding truth-functional tautology. In [93] and its unpublished sequel, Wang introduces more powerful methods (for much more difficult problems).

these procedures will certainly be preferred, when available, to "unreliable heuristic methods." Wang, Davis and Putnam, and several others are now pushing these new techniques into the far more challenging domain of theorem-proving in the predicate calculus (for which exhaustive decision procedures are no longer available). We have no space to discuss this area,[25] but it seems clear that a program to solve real mathematical problems will have to combine the mathematical sophistication of Wang with the heuristic sophistication of Newell, Shaw and Simon.[26]

B. Heuristics for Subproblem Selection

In designing a problem-solving system, the programmer often comes equipped with a set of more or less distinct "Methods"—his real task is to find an efficient way for the program to decide where and when the different methods are to be used.

Methods which do not dispose of a problem may still transform it to create new problems or subproblems. Hence, during the course of solving one problem we may become involved with a large assembly of interrelated subproblems. A "parallel" computer, yet to be conceived, might work on many at a time. But even the parallel machine must have procedures to allocate its resources because it cannot simultaneously apply all its methods to all the problems. We shall divide this administrative problem into two parts: the selection of those subproblem(s) which seem most critical, attractive, or otherwise immediate, and, in the next section, the choice of which method to apply to the selected problem.

In the basic program for LT (Section IV-A), subproblem selection is very simple. New problems are examined briefly and (if not solved at once) are placed at the end of the (linear) problem list. The main program proceeds along this list (step 1), attacking the problems in the order of their generation. More powerful systems will have to be more judicious (both in generation and selection of problems) for only thus can excessive branching be restrained.[27] In more complex systems we can expect to consider for each subproblem, at least these two aspects: 1) its apparent "centrality"—how will its solution promote the main goal, and 2) its apparent "difficulty"—how much effort is it liable to consume. We need heuristic methods to estimate each of these quantities and, further, to select accordingly one of the problems and allocate to it some reasonable quantity of effort.[28] Little enough is known about these matters, and so it is not entirely for lack of space that the following remarks are somewhat cryptic.

Imagine that the problems and their relations are arranged to form some kind of directed-graph structure [14], [57], [62]. The main problem is to establish a "valid" path between two initially distinguished nodes. Generation of new problems is represented by the addition of new, not-yet-valid paths, or by the insertion of new nodes in old paths. Then problems are represented by not-yet-valid paths, and "centrality" by location in the structure. Associate with each connection, quantities describing its current validity state (solved, plausible, doubtful, etc.) and its current estimated difficulty.

1) Global Methods: The most general problem-selection methods are "global"—at each step they look over the entire structure. There is one such simple scheme which works well on at least one rather degenerate interpretation of our problem graph. This is based on an electrical analogy suggested to us by a machine designed by Shannon (related to one described in [63] which describes quite a variety of interesting game-playing and learning machines) to play a variant of the game marketed as "Hex" (and known among mathematicians as "Nash"). The initial board position can be represented as a certain network of resistors. (See Fig. 11.) One player's goal is to construct a *short-circuit* path between two given boundaries; the opponent tries to open the circuit between them. Each move consists of shorting (or opening), irreversibly, one of the remaining resistors. Shannon's machine applies a potential between the boundaries and selects that resistor which carries the largest current. Very roughly speaking, this resistor is likely to be most critical because changing it will have the largest effect on the re-

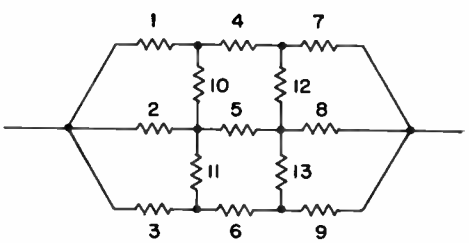

Fig. 11—This board game (due to C. E. Shannon) is played on a network of equal resistors. The first player's goal is to open the circuit between the endpoints; the second player's goal is to short the circuit. A move consists of opening or shorting a resistor. If the first player begins by opening resistor 1, the second player might counter by shorting resistor 4, following the strategy described in the text. The remaining move pairs (if *both* players use that strategy) would be (5, 8) (9, 13) (6, 3) (12, 10 or 2) (2 or 10 *win*). In this game the first player should be able to force a win, and the maximum-current strategy seems always to do so, even on larger networks.

[25] See [61] and [93].

[26] All these efforts are directed toward the reduction of search effort. In that sense they are all heuristic programs. Since practically no one still uses "heuristic" in a sense opposed to "algorithmic," serious workers might do well to avoid pointless argument on this score. The real problem is to find methods which significantly delay the apparently inevitable exponential growth of search trees.

[27] Note that the simple scheme of LT has the property that each generated problem will eventually get attention, even if several are created in a step 3. If one were to turn *full* attention to each problem, as generated, one might never return to alternate branches.

[28] One will want to see if the considered problem is the same as one already considered, or very similar. See the discussion in [62]. This problem might be handled more generally by simply *remembering* the (Characters of) problems that have been attacked, and checking new ones against this memory, *e.g.*, by methods of [31], looking more closely if there seems to be a match.

sistance of the net and, hence, in the goal direction of shorting (or opening) the circuit. And although this argument is not perfect, nor is this a perfect model of the real combinatorial situation, the machine does play extremely well. (It can make unsound moves in certain artificial situations, but no one seems to have been able to force this during a game.)

The use of such a global method for problem-selection requires that the available "difficulty estimates" for related subproblems be arranged to combine in roughly the manner of resistance values. Also, we could regard this machine as using an "analog model" for "planning." (See Section IV-D.)[29]

2) Local, and "Hereditary," Methods: The prospect of having to study at each step the whole problem structure is discouraging, especially since the structure usually changes only slightly after each attempt. One naturally looks for methods which merely *update* or modify a small fragment of the stored record. Between the extremes of the "first-come-first-served" problem-list method and the full global-survey methods, lie a variety of compromise techniques. Perhaps the most attractive of these are what we will call the *Inheritance* methods —essentially recursive devices.

In an Inheritance method, the effort assigned to a subproblem is determined only by its immediate ancestry; at the time each problem is created it is assigned a certain total quantity Q of time or effort. When a problem is later split into subproblems, such quantities are assigned to them by some local process which *depends only on their relative merits and on what remains of* Q. Thus the centrality problem is managed implicitly. Such schemes are quite easy to program, especially with the new programming systems such as IPL [64] and LISP [32] (which are themselves based on certain hereditary or recursive operations). Special cases of the inheritance method arise when one can get along with a simple all-or-none Q, *e.g.*, a "stop condition"—this yields the exploratory method called "back-tracking" by Golumb [65]. The decoding procedure of Wozencraft [66] is another important variety of Inheritance method.

In the complex exploration process proposed for chess by Newell, Shaw, and Simon [49] we have a form of Inheritance method with a *non-numerical stop-condition*. Here, the subproblems inherit *sets of goals to be achieved*. This teleological control has to be administered by an additional goal-selection system and is further complicated by a global (but reasonably simple) stop rule of the backing-up variety [Section III-C]. (Note: we are identifying here the move-tree-limitation problem with that of problem-selection.) Even though extensive experimental results are not yet available, we feel that the scheme of [49] deserves careful study by anyone planning serious work in this area. It shows only the beginning of the complexity sure to come in our development of intelligent machines.[30]

C. "Character-Method" Machines

Once a problem is selected, we must decide which method to try first. This depends on our ability to classify or characterize problems. We first compute the Character of our problem (by using some pattern recognition technique) and then consult a "Character-Method" table or other device which is supposed to tell us which method(s) are most effective on problems of that Character. This information might be built up from experience, given initially by the programmer, deduced from "advice" [70], or obtained as the solution to some other problem, as suggested in the GPS proposal [68]. In any case, this part of the machine's behavior, regarded from the outside, can be treated as a sort of stimulus-response, or "table look-up," activity.

If the Characters (or descriptions) have too wide a variety of values, there will be a serious problem of filling a Character-Method table. One might then have to reduce the detail of information, *e.g.*, by using only a few important properties. Thus the *Differences* of GPS [see Section IV-D, 2)] describe no more than is necessary to define a single goal, and a priority scheme selects just one of these to characterize the situation. Gelernter and Rochester [62] suggest using a property-weighting scheme, a special case of the "Bayes net" described in Section II-G.

D. Planning

Ordinarily one can solve a complicated problem only by dividing it into a number of parts, each of which can be attacked by a smaller search (or be further divided). Generally speaking, a successful division will reduce the search time not by a mere fraction, but by a *fractional exponent*. In a graph with 10 branches descending from each node, a 20-step search might involve 10^{20} trials, which is out of the question, while the insertion of just four *lemmas* or *sequential subgoals* might reduce the search to only 5.10^4 trials, which is within reason for machine exploration. Thus it will be worth a relatively enormous effort to find such "islands" in the solution of complex problems.[31] Note that even if one encountered, say, 10^6 failures of such procedures before success, one would still have gained a factor of perhaps 10^{10} in overall trial reduction! *Thus practically any ability at all to "plan," or "analyze," a problem will be profitable*, if the problem is difficult. It is safe to say that all simple, unitary, notions of how to build an intelligent machine will fail, rather sharply, for some modest level of problem difficulty. Only schemes which actively pursue an analysis toward obtaining a set of *sequential goals* can be

[29] A variety of combinatorial methods will be matched against the network-analogy opponent in a program being completed by R. Silver, Lincoln Lab., M.I.T., Lexington, Mass.

[30] Some further discussion of this question may be found in Slagle [67].

[31] See section 10 of [6].

expected to extend smoothly into increasingly complex problem domains.

Perhaps the most straightforward concept of planning is that of using a *simplified model* of the problem situation. Suppose that there is available, for a given problem, some other problem of "essentially the same character" but with less detail and complexity. Then we could proceed first to solve the simpler problem. Suppose, also, that this is done using a second set of methods, which are also simpler, but in some correspondence with those for the original. *The solution to the simpler problem can then be used as a "plan" for the harder one.* Perhaps each step will have to be expanded in detail. But the multiple searches will *add, not multiply*, in the total search time. The situation would be ideal if the model were, mathematically, a *homomorphism* of the original. But even without such perfection the model solution should be a valuable guide. In mathematics one's proof procedures usually run along these lines: one first assumes, *e.g.*, that integrals and limits always converge, in the planning stage. Once the outline is completed, in this simple-minded model of mathematics, then one goes back to try to "make rigorous" the steps of the proof, *i.e.*, to replace them by chains of argument using genuine rules of inference. And even if the plan fails, it may be possible to patch it by replacing just a few of its steps.

Another aid to planning is the *semantic*, as opposed to the homomorphic, model [14], [9]. Here we may have an *interpretation* of the current problem within another system, not necessarily simpler, but with which we are more familiar and have already more powerful methods. Thus, in connection with a plan for the proof of a theorem, we will want to know whether the proposed lemmas, or islands in the proof, are actually *true*; if not, the plan will surely fail. We can often easily tell if a proposition is true by looking at an interpretation. Thus the truth of a proposition from plane geometry can be supposed, at least with great reliability, by actual measurement of a few constructed drawings (or the analytic geometry equivalent). The geometry machine of Gelernter and Rochester [62], [69] uses such a semantic model with excellent results; it follows closely the lines proposed in [14].

1) The "Character-Algebra" Model: Planning with the aid of a model is of the greatest value in reducing search. Can we construct machines which find their own models? I believe the following will provide a general, straightforward way to construct certain kinds of useful, abstract models. The critical requirement is that we be able to compile a "Character-Method Matrix" (in addition to the simple Character-Method table in Section IV-C). *The CM matrix is an array of entries which predict with some reliability what will happen when methods are applied to problems.* Both of the matrix dimensions are indexed by problem Characters; if there is a method *which usually transforms problems of character C_i into problems of character C_j* then let the matrix entry C_{ij} be the name of that method (or a list of such methods). If there is no such method the corresponding entry is null.

Now suppose that there is no entry for C_{ij}—meaning that we have no *direct* way to transform a problem of type C_i into one of type C_j. Multiply the matrix by itself. If the new matrix has a non-null (i, j) entry then there must be a sequence of *two* methods which effects the desired transformation. If that fails, we may try higher powers. Note that [if we put unity for the (i, i) terms] we can reach the 2^n matrix power with just n multiplications. We don't need to define the symbolic multiplication operation; one may instead use arithmetic entries—putting *unity for any non-null entry* and zero for any null entry in the original matrix. This yields a simple connection, or flow diagram, matrix, and its nth power tells us something about its set of paths of length 2^n.[32] (Once a non-null entry is discovered, there exist efficient ways to find the corresponding sequences of methods. The problem is really just that of finding paths through a maze, and the method of Moore [71] would be quite efficient. Almost any problem can be converted into a problem of finding a chain between two terminal expressions in some formal system.) If the Characters are taken to be abstract representations of the problem expressions, this "Character-Algebra" model can be as abstract as are the available pattern-recognition facilities. See [14] and [9].

The critical problem in using the Character-Algebra model for planning is, of course, the *prediction-reliability of the matrix entries*. One cannot expect the Character of a result to be strictly determined by the Character of the original and the method used. And the reliability of the predictions will, in any case, deteriorate rapidly as the matrix power is raised. But, as we have noted, any plan at all is so much better than none that the system should do very much better than exhaustive search, even with quite poor prediction quality.

This matrix formulation is obviously only a special case of the character planning idea. More generally, one will have descriptions, rather than fixed characters, and one must then have more general methods to calculate from a description what is likely to happen when a method is applied.

2) Characters and Differences: In the GPS (General Problem Solver) proposal of Newell, Shaw, and Simon [68], [15], we find a slightly different framework: they use a notion of Difference between two problems (or expressions) where we speak of the Character of a single problem. These views are equivalent if we take our problems to be links or connections between expressions. But this notion of Difference (as the Character of a pair) does lend itself more smoothly to teleological reasoning. For what is the goal defined by a problem but to *reduce the "difference" between the present state and the*

[32] See, *e.g.*, [88].

desired state? The underlying structure of GPS is precisely what we have called a "Character-Method Machine" in which each kind of Difference is associated in a table with one or more methods which are known to "reduce" that Difference. Since the characterization here depends always on 1) the current problem expression and 2) the desired end result, it is reasonable to think, as its authors suggest, of GPS as using "means-end" analysis.

To illustrate the use of Differences, we shall review an example [15]. The problem, in elementary propositional calculus, is to prove that from $S \wedge (-P \supset Q)$ we can deduce $(Q \vee P) \wedge S$. The program looks at both of these expressions with a recursive *matching* process which branches out from the main connectives. The first Difference it encounters is that S occurs on different sides of the main connective "$\wedge$". It therefore looks in the Difference-Method table under the heading "change position." It discovers there a method which uses the theorem $(A \wedge B) \equiv (B \wedge A)$ which is obviously useful for removing, or "reducing," differences of position. GPS applies this method, obtaining $(-P \supset Q) \wedge S$. GPS now asks what is the Difference between this new expression and the goal. This time the matching procedure gets down into the connectives inside the left-hand members and finds a Difference between the connectives "$\supset$" and "$\vee$". It now looks in the CM table under the heading "Change Connective" and discovers the appropriate method using $(-A \supset B) \equiv (A \vee B)$. It applies this method, obtaining $(P \vee Q) \wedge S$. In the final cycle, the difference-evaluating procedure discovers the need for a "change position" inside the left member, and applies a method using $(A \vee B) \equiv (B \vee A)$. This completes the solution of the problem.[33]

Evidently, the success of this "means-end" analysis in reducing general search will depend on the degree of specificity that can be written into the Difference-Method table—basically the same requirement for an effective Character-Algebra.

It may be possible to *plan* using Differences, as well.[33] One might imagine a "Difference-Algebra" in which the predictions have the form $D = D'D''$. One must construct accordingly a difference-factorization algebra for discovering longer chains $D = D_1 \cdots D_n$ and corresponding method plans. We should note that one *cannot* expect to use such planning methods with such primitive Differences as are discussed in [15]; for these cannot form an adequate Difference-Algebra (or Character Algebra). Unless the characterizing expressions have many levels of descriptive detail, the matrix powers will too swiftly become degenerate. This degeneracy will ultimately limit the capacity of any formal planning device.

One may think of the general planning heuristic as embodied in a recursive process of the following form. Suppose we have a problem P:

1) Form a plan for problem P.
2) Select first (next) step of the plan.
   (If no more steps, exit with "success.")
3) Try the suggested method(s):
   Success: return to b), *i.e.*, try next step in the plan.
   Failure: return to a), *i.e.*, form new plan, or perhaps change current plan to avoid this step.
   Problem judged too difficult: *Apply this entire procedure to the problem of the current step.*

Observe that such a program schema is essentially recursive; it uses itself as a subroutine (explicitly, in the last step) in such a way that its current state has to be stored, and restored when it returns control to itself.[34]

Miller, Galanter and Pribram[35] discuss possible analogies between human problem-solving and some heuristic planning schemes. It seems certain that, for at least a few years, there will be a close association between theories of human behavior and attempts to increase the intellectual capacities of machines. But, in the long run, we must be prepared to discover profitable lines of heuristic programming which do not deliberately imitate human characteristics.[36]

[33] Compare this with the "matching" process described in [57]. The notions of "Character," "Character-Algebra," etc., originate in [14] but seem useful in describing parts of the "GPS" system of [57] and [15]. Reference [15] contains much additional material we cannot survey here. Essentially, GPS is to be self-applied to the problem of discovering sets of Differences appropriate for given problem areas. This notion of "bootstrapping"—applying a problem-solving system to the task of improving some of its own methods—is old and familiar, but in [15] we find perhaps the first specific proposal about how such an advance might be realized.

[34] This violates, for example, the restrictions on "DO loops" in programming systems such as FORTRAN. Convenient techniques for programming such processes were developed by Newell, Shaw, and Simon [64]; the program state-variables are stored in "push-down lists" and both the program and the data are stored in the form of "list-structures." Gelernter [69] extended FORTRAN to manage some of this. McCarthy has extended these notions in LISP [32] to permit *explicit* recursive definitions of programs in a language based on recursive functions of symbolic expressions; here the management of program-state variables is fully automatic. See also Orchard-Hays' article in this issue.

[35] See chs. 12 and 13 of [46].

[36] Limitations of space preclude detailed discussion here of theories of self-organizing neural nets, and other models based on brain analogies. (Several of these are described or cited in [C] and [D].) This omission is not too serious, I feel, in connection with the subject of heuristic programming, because the motivation and methods of the two areas seem so different. Up to the present time, at least, research on neural-net models has been concerned mainly with the attempt to show that certain rather simple heuristic processes, *e.g.*, reinforcement learning, or property-list pattern-recognition, can be realized or evolved by collections of simple elements without very highly organized interconnections. Work on heuristic programming is characterized quite differently by the search for new, more powerful heuristics for solving very complex problems, and by very little concern for what hardware (neuronal or otherwise) would minimally suffice for its realization. In short, the work on "nets" is concerned with how far one can get with a small initial endowment; the work on "artificial intelligence" is concerned with using all we know to build the most powerful systems that we can. It is my expectation that, in problem-solving power, the (allegedly brain-like) minimal-structure systems will never threaten to compete with their more deliberately designed contemporaries; nevertheless, their study should prove profitable in the development of component elements and subsystems to be used in the construction of the more systematically conceived machines.

V. Induction and Models

A. Intelligence

In all of this discussion we have not come to grips with anything we can isolate as "intelligence." We have discussed only heuristics, shortcuts, and classification techniques. Is there something missing? I am confident that sooner or later we will be able to assemble programs of great problem-solving ability from complex combinations of heuristic devices—multiple optimizers, pattern-recognition tricks, planning algebras, recursive administration procedures, and the like. In no one of these will we find the seat of intelligence. Should we ask what intelligence "really is"? My own view is that this is more of an esthetic question, or one of sense of dignity, than a technical matter! To me "intelligence" seems to denote little more than the complex of performances which we happen to respect, but do not understand. So it is, usually, with the question of "depth" in mathematics. Once the proof of a theorem is really understood its content seems to become trivial. (Still, there may remain a sense of wonder about how the proof was discovered.)

Programmers, too, know that there is never any "heart" in a program. There are high-level routines in each program, but all they do is dictate that "if such-and-such, then transfer to such-and-such a subroutine." And when we look at the low-level subroutines, which "actually do the work," we find senseless loops and sequences of trivial operations, merely carrying out the dictates of their superiors. The intelligence in such a system seems to be as intangible as becomes the meaning of a single common word when it is thoughtfully pronounced over and over again.

But we should not let our inability to discern a locus of intelligence lead us to conclude that programmed computers therefore cannot think. For it may be so with *man*, as with *machine*, that, when we understand finally the structure and program, the feeling of mystery (and self-approbation) will weaken.[37] We find similar views concerning "creativity" in [60]. The view expressed by Rosenbloom [73] that minds (or brains) can transcend machines is based, apparently, on an erroneous interpretation of the meaning of the "unsolvability theorems" of Godel.[38]

B. Inductive Inference

Let us pose now for our machines, a variety of problems more challenging than any ordinary game or mathematical puzzle. Suppose that we want a machine which, when embedded for a time in a complex environment or "universe," will essay to produce a description of that world—to discover its regularities or laws of nature. We might ask it to predict what will happen next. We might ask it to predict what would be the likely consequences of a certain action or experiment. Or we might ask it to formulate the laws governing some class of events. In any case, our task is to equip our machine with *inductive* ability—with methods which it can use to construct general statements about events beyond its recorded experience. Now, there can be no system for inductive inference that will work well in all possible universes. But given a universe, or an ensemble of universes, and a criterion of success, this (epistemological) problem for machines becomes technical rather than philosophical. There is quite a literature concerning this subject, but we shall discuss only one approach which currently seems to us the most promising; this is what we might call the "grammatical induction" schemes of Solomonoff [55], [16], [17], based partly on work of Chomsky and Miller [80], [81].

We will take *language* to mean the set of expressions formed from some given set of primitive symbols or expressions, by the repeated application of some given set of rules; the primitive expressions plus the rules is the *grammar* of the language. Most induction problems can be framed as problems in the *discovery of grammars*. Suppose, for instance, that a machine's prior experience is summarized by a large collection of statements, some labelled "good" and some "bad" by some critical device. How could we generate selectively more good statements? The trick is to find some relatively simple (formal) language in which the good statements are grammatical, and in which the bad ones are not. Given such a language, we can use it to generate more statements, and presumably these will tend to be more like the good ones. The heuristic argument is that if we can find a relatively simple way to separate the two sets, the discovered rule is likely to be useful beyond the immediate experience. If the extension fails to be consistent with new data, one might be able to make small changes in the rules and, generally, one may be able to use many ordinary problem-solving methods for this task.

The problem of finding an efficient grammar is much the same as that of finding efficient *encodings*, or pro-

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[37] See [14] and [9].

[38] On problems of volition we are in general agreement with McCulloch [75] that our *freedom of will* "presumably means no more than that we can distinguish between what we intend [*i.e.*, our *plan*], and some intervention in our action." See also MacKay ([76] and its references); we are, however, unconvinced by his eulogization of "analogue" devices. Concerning the "mind-brain" problem, one should consider the arguments of Craik [77], Hayek [78] and Pask [79]. Among the active leaders in modern heuristic programming, perhaps only Samuel [91] has taken a strong position against the idea of machines thinking. His argument, based on the fact that reliable computers do only that which they are instructed to do, has a basic flaw; it does not follow that the programmer therefore has full knowledge (and therefore full responsibility and credit for) what will ensue. For certainly the programmer may set up an evolutionary system whose limitations are for him unclear and possibly incomprehensible. No better does the mathematician know all the consequences of a proposed set of axioms. Surely a machine has to *be* in order to perform. But we cannot assign all the credit to its programmer if the operation of a system comes to reveal structures not recognizable or anticipated by the programmer. While we have not yet seen much in the way of intelligent activity in machines, Samuel's arguments in [91] (circular in that they are based on the presumption that machines do not have minds) do not assure us against this. Turing [72] gives a very knowledgeable discussion of such matters.

grams, for machines; in each case, one needs to discover the important regularities in the data, and exploit the regularities by making shrewd *abbreviations*. The possible importance of Solomonoff's work [18] is that, despite some obvious defects, it may point the way toward systematic mathematical ways to explore this discovery problem. He considers the class of all programs (for a given general-purpose computer) which will produce a certain given output (the body of data in question). Most such programs, if allowed to continue, will add to that body of data. By properly weighting these programs, perhaps by length, we can obtain corresponding weights for the different possible continuations, and thus a basis for prediction. If this prediction is to be of any interest, it will be necessary to show some independence of the given computer; it is not yet clear precisely what form such a result will take.

C. Models of Oneself

If a creature can answer a question about a hypothetical experiment, without actually performing that experiment, then the answer must have been obtained from some submachine inside the creature. The output of that submachine (representing a correct answer) as well as the input (representing the question) must be coded descriptions of the corresponding external events or event classes. Seen through this pair of encoding and decoding channels, the internal submachine acts like the environment, and so it has the character of a "model." The inductive inference problem may then be regarded as the problem of constructing such a model.

To the extent that the creature's actions affect the environment, this internal model of the world will need to include some representation of the creature itself. If one asks the creature "why did you decide to do such and such" (or if it asks this of itself), any answer must come from the internal model. Thus the evidence of introspection itself is liable to be based ultimately on the processes used in constructing one's image of one's self. Speculation on the form of such a model leads to the amusing prediction that intelligent machines may be reluctant to believe that they are *just* machines. The argument is this: our own self-models have a substantially "dual" character; there is a part concerned with the physical or mechanical environment—with the behavior of inanimate objects—and there is a part concerned with social and psychological matters. It is precisely because we have not yet developed a satisfactory mechanical theory of mental activity that we have to keep these areas apart. We could not give up this division even if we wished to—until we find a unified model to replace it. Now, when we ask such a creature what sort of being it is, it cannot simply answer "directly;" it must inspect its model(s). And it must answer by saying that it seems to be a dual thing—which appears to have two parts—a "mind" and a "body." Thus, even the robot, unless equipped with a satisfactory theory of artificial intelligence, would have to maintain a dualistic opinion on this matter.[39]

Conclusion

In attempting to combine a survey of work on "artificial intelligence" with a summary of our own views, we could not mention every relevant project and publication. Some important omissions are in the area of "brain models"; the early work of Farley and Clark [92] (also Farley's paper in [D], often unknowingly duplicated, and the work of Rochester [82] and Milner [D].) The work of Lettvin, *et al.* [83] is related to the theories in [19]. We did not touch at all on the problems of logic and language, and of information retrieval, which must be faced when action is to be based on the contents of large memories; see, *e.g.*, McCarthy [70]. We have not discussed the basic results in mathematical logic which bear on the question of what can be done by machines. There are entire literatures we have hardly even sampled—the bold pioneering of Rashevsky (c. 1929) and his later co-workers [95]; Theories of Learning, *e.g.*, Gorn [84]; Theory of Games, *e.g.*, Shubik [85]; and Psychology, *e.g.*, Bruner, *et al.* [86]. And everyone should know the work of Polya [87] on how to solve problems. We can hope only to have transmitted the flavor of some of the more ambitious projects *directly* concerned with getting machines to take over a larger portion of problem-solving tasks.

One last remark: we have discussed here only work concerned with more or less self-contained problem-solving programs. But as this is written, we are at last beginning to see vigorous activity in the direction of constructing usable *time-sharing* or *multiprogramming* computing systems. With these systems, it will at last become economical to match human beings in real time with really large machines. This means that we can work toward programming what will be, in effect, "thinking aids." In the years to come, we expect that these man-machine systems will share, and perhaps for a time be dominant, in our advance toward the development of "artificial intelligence."

[39] There is a certain problem of infinite regression in the notion of a machine having a *good* model of itself: of course, the nested models must lose detail and finally vanish. But the argument, *e.g.*, of Hayek (See 8.69 and 8.79 of [78]) that we cannot "fully comprehend the unitary order" (of our own minds) ignores the power of recursive description as well as Turing's demonstration that (with sufficient external writing space) a "general-purpose" machine can answer any question about a description of itself that any larger machine could answer.

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Self-Organizing Systems—A Review and Commentary*

J. K. HAWKINS†, MEMBER, IRE

Within the general area of activity groping toward "artificial intelligence," a considerable body of work is being devoted to the development of theory and mechanizations to produce self-organizing machines. Such machines may be loosely characterized as containing a variable network in which the elements are organized by the machine itself, without external intervention, to meet criteria of successful operation. J. K. Hawkins has been requested to direct his attention to this class of machines, to summarize significant work, to generalize upon it, and to evaluate its status.—*The Guest Editor*

Summary—**The class of self-organizing systems represented by networks which learn to recognize patterns is reviewed from an historical standpoint, and some of the behavioral similarities between such nets and biological nervous systems are discussed. Examples and results of several experimental models for alphanumeric character recognition are presented. The network synthesis problem is then recast in terms of redundant information removal, multivariable curve-fitting and expansion in orthonormal functions. Recognition network structures and the learning process are described from these points of view. The potential component and behavioral advantages to be gained from sequential feedback networks are discussed briefly.**

I. Introduction

THE TERM self-organizing system has been employed loosely to describe any system which modifies its behavior according to a set of inputs representing the environment within which it operates. The environment commonly includes a signal or energy source which is interpreted as an error indicator, causing the system to be unstable or to change its input-output relationship in some manner. Behavioral modification is generally taken to be accomplished by the system itself, without external intervention in its detailed inner workings. The result, if the system is successful, is that its behavior improves according to one or more criteria. The criteria are usually related to reduction of errors or to increased system stability.

The term has been applied to so many different phenomena, however, that it has lost any precise meaning. It has been taken as a point of view in describing business organizations, biological cell conglomerates, digital computer programs, feedback control systems, and electronic networks. For example, the self-organization of a collection of geometrical shapes which lock together to form complex structures under the influence of noise (mechanical vibration) has been considered by Penrose [1]. Biological self-organization at the cellular level has been pointed out by Auerbach [2] in describing the reaggregation of embryonic cells. Beer [3] has discussed business activity from a self-organizing viewpoint; and the game strategy of electro-chemical systems has been considered by Pask [4].

While these widely dispersed subjects are certainly of interest to the present discussion, appraisal of the entire spectrum is virtually impossible. In this review, therefore, the viewpoint will be largely that of the digital computer engineer, and consideration will be confined primarily to network models. They will be referred to as self-organizing machines, as opposed to systems which can be constructed of less machine-like components. The types of machines to be considered can best be described as networks capable of performing certain functions usually associated with animal nervous systems, including recognition and learning, and whose detailed construction is more or less consciously modeled after the known physical characteristics of nervous tissue. Two major categories of such networks will be distinguished:

1) *Recognition* networks, defined as fixed-parameter networks which tend to produce an arbitrarily assigned (generally coded) output upon the occurrence of any member of a set of pre-assigned input events. Examples of events of interest include spatial patterns (*e.g.*, printed alphanumeric characters) and temporal patterns (*e.g.*, spoken words).
2) *Learning* machines, defined as variable-parameter networks which improve in recognition in the above sense, solely as a result of the repeated joint occurrence of input and desired output events. As will appear in later sections, it does not seem necessary at this time to draw a distinction between the process of learning and the combined process of calculation and storage of results, as in a digital computer.

Some comments, brief and incomplete, are also made upon the problem of generalization, and upon the possi-

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bility of networks to whose behavior the term reasoning might be applied.

Specifically excluded from consideration in this review are some interesting self-organizing or learning systems which deal primarily with higher-level abstractions [5]. Systems of this type include computer programs oriented toward learning to solve problems such as geometry proofs and checker games, and are not generally associated with the handling of raw sensory data such as visible or audible events. Also excluded from this review is a significant body of work on adaptive control systems [6] which is concerned with the maintenance of stability in a feedback control system. It is perhaps useful in bounding the self-organizing systems field to point out the analogy between the above approaches and levels of human system functions. The programmed problem-solving approach can be likened to abstract cortical activity and thought, adaptive control systems to the autonomic nervous system controlling the body's internal environment necessary for survival, and the recognition network to peripheral sensory processing and early cortical association nets.

This review will be oriented primarily toward networks which exist as hardware models, as mathematical models, or as digital computer programs which could, reasonably, be reduced to hardware models. Emphasis is therefore placed upon the network synthesis problem. The networks to be considered will have a large number of input points, corresponding conceptually to a visual raster, or to the outputs of a tapped delay line which display a time varying signal (*e.g.*, audible sequence) upon some spatial coordinate. Networks will also possess outputs, generally fewer in number than the inputs, which will assume specific configurations of values corresponding to coded forms of some feature or features of the input configurations.

The significance of learning (or self-organization) in specific network applications has been debated at length. The question is whether or not an adaptive network possesses any inherent advantage over a fixed network, suitably designed for some recognition task. While the question is variously answered in specific cases, it is clear that, provided the statistical nature of the environment does not change with time, any equipment built into a network for the purposes of learning becomes useless once the machine has successfully learned the necessary responses. A machine which learns to read the English alphabet and thereafter is required to perform no other task, for example, might well be replaced by an equivalent fixed-parameter network. If the network is in time required to perform additional tasks, such as reading another language, then a built-in learning mechanism may be justified.

In later sections it will be seen that what has been described as learning can be readily accomplished by a network, provided it possesses certain arithmetic ability and storage capacity. The importance of network learning—the choice of fixed-parameter networks with precalculated values vs variable-parameter learning networks—depends largely upon the requirements and economics of practical applications. Since a frequently useful criterion of network performance is its error rate, appropriately adjusted for the cost of errors, it seems reasonable to measure the value of network learning capability in terms of the expected cost reduction vs the cost of incorporating hardware required to perform the necessary arithmetic and storage operations.

This review takes the viewpoint that the problem of generalization is primarily a corollary of the recognition network synthesis problem. That is, the structure of a recognition network must in some sense reflect the structure of the environment with which it must deal. Since it is generally not practical to consider or perform calculations based upon all possible input configurations, some sampling procedure is indicated. If the sample is representative of the whole environment, and the signal and noise variations are treated on a gross basis, then a well-designed recognition network can be expected to generalize within the limitations of the sample and the sophistication of its statistical treatment. It seems unreasonable, on the other hand, to expect a network to identify correctly some input pattern which does not correspond to anything contained in or implied by its previous history. Thus, it is possible to construct a network which will correctly identify a variety of capital *A*'s, based only upon the learning of a few sample *A*'s. There does not appear to be any reasonable logical relationship between capital *A*'s and lower-case *a*'s, however, upon which basis a network could be expected to recognize the latter in the absence of learned samples.

The importance of generalization also depends largely upon the application. It may be measured by the degree to which an application justifies a network which can form elaborate conjectures in the form of logical relationships, based upon meager data, as opposed to an application in which environmental samples are plentiful and input-output relationships simple.

Since one of the major justifications for considering recognition and learning machines consists of the biological evidence before us, and since some of the description is couched in physiological terms, a brief survey of the pertinent features of nerve tissue and of the human nervous system is presented below. At the risk of lack of physiological precision, nerve properties are considerably abstracted and simplified, based upon the usage of various workers in the field.

II. Biological Background

The neuron, basic nervous system building block, is a specialized body cell notable for its ability to amplify and conduct an electrical impulse. The neuron may be briefly described as consisting of a main cell body, from which runs an *axon*, a long fiber which may be regarded as a lossless transmission line. The axon terminates in a series of small *dendritic* branches, the ends of which lie

on or near the cell bodies of other neurons. The point of near-contact between the dendritic endings and the succeeding cell body is termed the *synapse* or synaptic junction. The synapse is capable of transmitting, with some attenuation, an electrical impulse between one neuron and another.

Operation of the neuron is as follows. If a sufficient number (about 10) of nearly simultaneous impulses arrive at a set of nearby synaptic junctions, the potential of the cell body is raised above what is called the *threshold* potential, and the neuron fires. Firing consists of a complex ion-exchange process, the details of which need not concern us, equivalent to the discharge of an energy storage device such as a transmission line. The resulting fixed-amplitude impulse travels over the cell body and down its axon, eventually finding its way to synaptic junctions terminating on other neurons, and so on.

The properties of neurons which have been most commonly abstracted are as follows:

1) Synchronous operation: This abstraction is required primarily by the mathematical necessity for treating discrete time intervals. It can be partially justified, however, by the fact that long neurons tend to transmit at a higher speed than short ones, with the result that the delay time per neuron in any given region tends toward a constant on the order of one millisecond.
2) Binary operation, or all-or-none firing: This can be experimentally observed, and in fact a neuron at any instant is either emitting a pulse or not. Many sensory neurons, however, behave more nearly like pulse rate modulation devices, with pulse rate continuously variable over some range of intensity of the sensory stimulus.
3) Linear, weighted summation of inputs: This again is primarily a simplifying assumption for mathematical convenience. It says that inputs (binary valued) are weighted according to the value of the corresponding synaptic strength, and summed linearly at the cell body. If the sum is greater than the threshold, the cell fires, otherwise not. The fact that the threshold value is known to vary (it goes effectively to infinity for a brief period immediately following firing) is sometimes taken into account. A distinction is sometimes drawn between excitatory and inhibitory types of synaptic weighting, since it is known that the firing of one neuron will in some cases tend to prevent rather than augment the firing of another. Inhibition is indicated either by a special symbol or simply by a negative synaptic weight having an equivalent effect under the assumption of linear input summation.

For purposes of early work in the field, in which variable synaptic weighting was not specifically considered, the simplified nerve net diagrams of Fig. 1(a) served to illustrate neuron properties. With variable synaptic weighting considered, nerve net diagrams tend to resemble that of Fig. 1(b) in which all synapses are represented in a similar fashion, and the functions of cell body and axon have been combined into a single unit. Both representations will be used in this review.

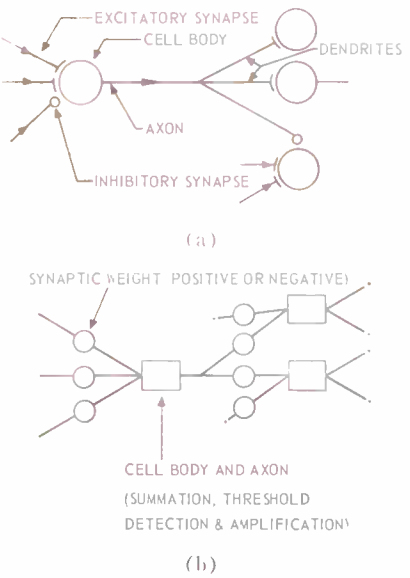


Fig. 1—Neuron representations. (a) Biological analog with fixed synaptic functions. (b) Network analog with variable synapse.

The number of neurons in the human nervous system is on the order of 10^{10}. Each neuron exhibits dendritic branching properties connecting it with on the order of 10^2 to 10^3 other neurons. If synaptic weighting is considered to be variable within some degree of precision or significance, say for discussion 0.1 per cent (*i.e.*, 1,024 significant levels), then the information storage capacity of the nervous system can be placed in the neighborhood of 10^{14} bits (10^{13} synapses, 10 bits per synapse). At any instant, the system can conceivably assume any one of $2^{10^{10}}$ different states, under the abstraction of binary neuron operation. If the simple nerve-net diagrams of Fig. 1 give the impression that an analysis of the nervous system is nearly within each, then the reader is referred to Sholl [7] for a compact but revealing survey of the known structure of the cortex.

III. Historical Review

Although Pavlov's work [8] provided an early conceptual framework for the study of nerve net action, it appeared prior to widespread knowledge of other disciplines which seem to be necessary for useful formulation of his concepts. Pavlov's experiments on the conditioned reflex will therefore be referred to later in this section in conjunction with more recent terminology.

The first major worker to attempt a mathematical description of biological processes was Rashevsky [9], who in 1938 discussed not only nerve net action but also a wide variety of physiological phenomena from basic cell chemistry to the behavior of populations of organisms. Although Rashevsky appeared unaware of Boolean algebra in his first edition, in effect he pointed out

how certain logical operations might be carried out by simple nerve arrangements. His point of view is illustrated, in simplified form, in Fig. 2(a), in which it can be seen that the exclusive-or function is mechanized by an arrangement of excitatory and inhibitory connections. Rashevsky also suggested an explanation of short-term memory by means of recirculating neuron loops, in which an impulse, once initiated, would continue to cycle indefinitely or until terminated by a specific inhibitory impulse. The simplest form of such a loop is illustrated in Fig. 2(b). Rashevsky's early conjecture regarding nerve net operations has been experimentally verified by Lettvin and others [10], who cataloged two specific logical functions carried out in the frog's optic nerve, plus three other neuron functions related to light intensity changes. Recirculation of signal sequences in the cortex has been observed by Verzeano [11], although the loop is considerably more involved than the simple illustration given.

In 1943, McCulloch and Pitts [12] published an important contribution to the field pointing out the possibility of applying Boolean algebra to nerve net behavior. This had the effect of bringing to bear on the problem a large body of techniques associated with the design of digital computers, then just coming into widespread use. McCulloch and Pitts have subsequently extended this concept [13]. A second contribution [14] consisted of suggesting how it might be possible for nerve nets to perform certain transformations upon input signals. The idea is illustrated in highly simplified form in Fig. 3 for linear translation of an input pattern. Providing the first two layers of neurons fire only under the condition of two inputs active, while the last layer fires upon any input active, control lines A and B act as multipole switches. If A is active, the input is displayed directly upon the output neurons; if B is active, the input shifted by one bit position is displayed. This technique can be extended to translation in two dimensions, as well as to other transformations, by appropriate spatial arrangement of the network. By successively energizing various control lines, it is therefore possible, in principle, to generate any desired transformation of the input pattern and thereby bring it into coincidence with some stored standard pattern. While repetitive structures are certainly found in the nervous system, and the alpha-rhythm is sometimes regarded as a scanning mechanism, there has been no experimental evidence that animal nerve nets perform specific linear transformations such as that illustrated.

In 1949, Hebb [15] advanced two hypotheses which have become the basis of many nerve net models. Hebb postulated that the synaptic junction is the site of permanent memory, memory consisting of the value of the attenuation (strength) of the junction, and that memory of any event is a distributed phenomenon residing in the small changes in strength which occur as the result of the event impinging upon a large number of synapses. Hebb suggested the following qualitative rule for the change in strength of a junction as the result of activity: "When an axon of cell A is near enough to excite a cell B and repeatedly or persistently takes part in firing it, some growth process or metabolic change takes place in one or both such that A's efficiency, as one of the cells firing B, is increased." Hebb's postulates are in agreement with many observable psychological phenomena, especially Pavlov's conditioned reflex. His distributed memory concept is supported by the results of certain experiments in which behavior and memory can be tested following the removal of various major portions of the cortex. Hebb also suggested that some thought processes might be described in terms of assemblies of cells acting in unison in various time sequences. Farley and Clark formalized this qualitative concept by means of a digital computer simulation [16], [17] and indeed observed the spontaneous development of cell assemblies as well as growth in the program's ability to recognize simple patterns and generalize to some extent.

A more formal nerve net model possessing some of the features of Hebb's variable synaptic junction was proposed independently by Sholl and Uttley [18], [19]. The network was assumed to calculate the conditional probability of an input event, given the occurrence of one or more other inputs, based upon past experience. A simplified version of the Uttley model

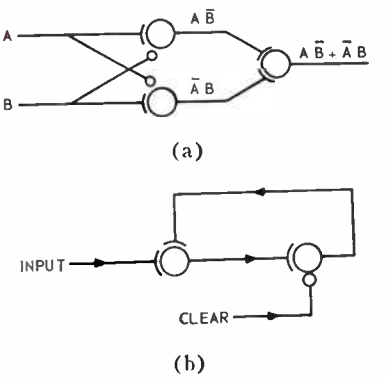


Fig. 2—Simple nerve nets. (a) Logical operation. (b) Short-term memory loop.

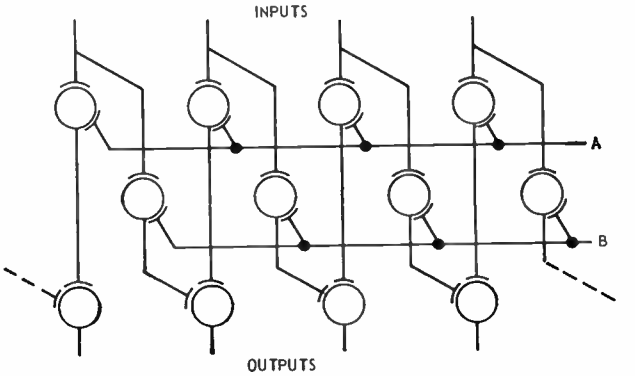
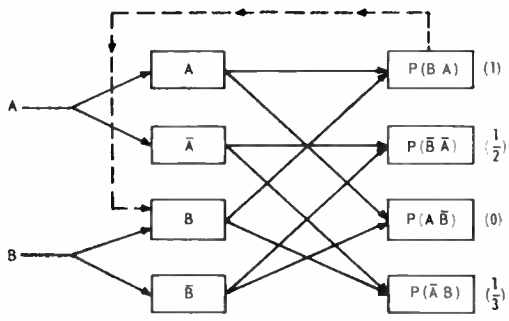


Fig. 3—Linear translation network.

for two inputs is illustrated in Fig. 4. Considering all-or-none occurrences of events, and using the notation $P(x=1|y=1)=P(x|y)$, then four independent boxes are required to calculate the possible conditional probabilities, since $P(x|y)=1-P(\bar{x}|y)$. For the assumed experience table shown, the four conditional probability boxes will store the quantities in parentheses. The Uttley model further assumes feedback connections from the storage units to the inputs (only one shown for illustration). If a storage unit is excited by its corresponding input, it feeds back a quantity proportional to the stored value, thus tending to cause the controlled input to assume the state which past experience indicates. In the illustration, if A alone is active the $P(B|A)$ storage unit delivers full output, 1, to the input of the B unit, causing it to assume the state 1 since all previous occurrences of A were accompanied by B. Note that if A is considered the input neuron, B the output and $P(B|A)$ the synaptic junction, the Uttley and Hebb models may be described in terms of one another. The Uttley model involves an extravagant number of storage elements, when biological systems are considered, since an element must be supplied for each of the possible combinations of inputs taken one at a time, two at a time, etc., up to N at a time for N inputs. This is 2^N-1, a quantity which would exceed the supply of human neurons, given the optic system alone, since N is approximately 10^8 at the retina.

A somewhat different approach employing probabilistic principles was taken by von Neumann [20], who considered the use of simple automata for the contruction of fixed logical propositions as well as crude learning networks. He also demonstrated the potential reliability which can be achieved by multiplexing unreliable elements.



(a)

EXPERIENCE TABLE

A	B	NUMBER OF OCCURRENCES
0	0	25
0	1	25
1	0	0
1	1	50

(b)

Fig. 4—Conditional probability model. (a) Network representation. (b) Sample table of binary event occurrences.

Networks based to some degree upon physiological evidence have been studied by Taylor [21], [22]. A simplified version of his model is illustrated in Fig. 5, in which the transformed inputs are weighted by the storage units and the resulting signals summed at the response units. The largest signal determines which response unit will fire. Learning consists of changing the values contained in the storage units according to the relative agreement between the transformed input and the output, when the latter is being driven externally by the experimenter. Values increase if input and output activity agree; otherwise, they decrease. Experiments were conducted on a nine-input, two-output system. Illustrative of the network transformations employed by Taylor is the detail filter illustrated in Fig. 6(a). It consists of a bank of summing amplifiers, the output of each being fed back with appropriate attenua-

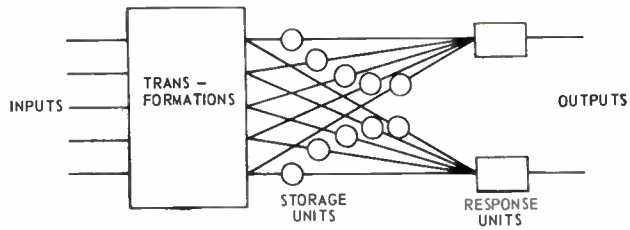
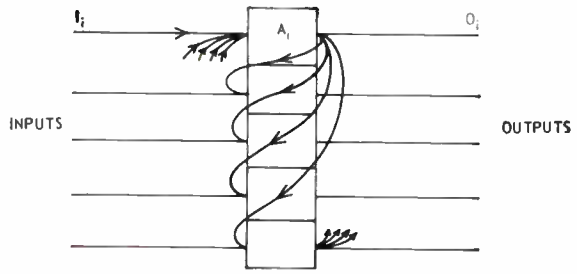
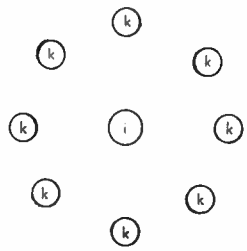


Fig. 5—General learning and recognition network structure.



(a)



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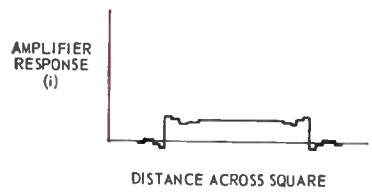

(c)

Fig. 6—Detail filter. (a) Network. (b) Spatial arrangement of inputs. (c) Example of filter output.

tion to the inputs of all others (only one set is illustrated), together with the external input. If the inputs are wired to a spatial arrangement of sensory cells as in Fig. 6(b), and if the feedback coefficient from all radial sensors k to the central sensor i are negative, then the amplifier associated with the central sensor tends to emphasize edges, corners or spots which illuminate the central sensor but few of the peripheral sensors. Amplifier output for a scan across a solid square is illustrated in Fig. 6(c). Such a network has some of the properties of the frog's eye "bug detector," reported by Lettvin and others [10].

In 1958, Rosenblatt reported on the Perceptron [23], a model which takes into account much of the foregoing work, and which represents a major attempt to place the complete learning sequence of an artificial nervenet on a rigorous mathematical basis. At the risk of grossly oversimplifying a voluminous amount of material, what Rosenblatt succeeded in proving in the original and subsequent reports [24]–[26] was that learning of an input-output relationship will indeed occur in a linear-summation network under very general conditions of repeated presentation of input and desired output patterns. It is necessary that synaptic strengths or weighting elements follow certain rules of growth, and that a solution exists for the set of values of the weighting elements required to realize the given output function. The Perceptron model is illustrated in simplified form in Fig. 7. It is assumed that sensory in-

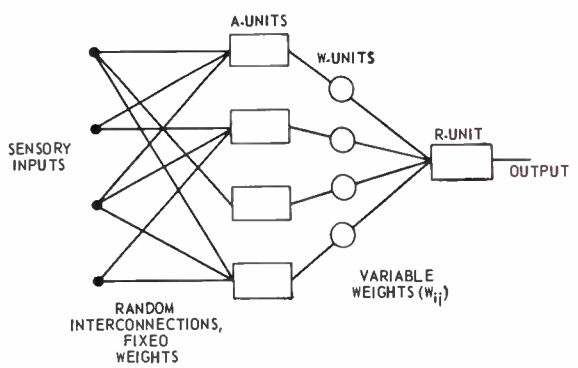

Fig. 7—Perceptron model.

puts are mapped by means of random connections with fixed synaptic strengths upon a series of neurons termed A-units. Since no learning occurs in this stage of the network, it may be considered that an input pattern S is replaced by some transformed pattern S' displayed directly upon the A-units. The transformed inputs are then mapped through variable connections to a set of response-units (R-units) which determine the outputs (only one shown). Binary neuron operation and linear input summation may be formalized as follows:

$$\begin{aligned} R_j = 1 \quad &\text{if} \quad \sum_i x_i W_{ij} - \theta_j \geq 0 \\ R_j = 0 \quad &\text{if} \quad \sum_i x_i W_{ij} - \theta_j < 0 \end{aligned} \tag{1}$$

where

x_i = transformed binary input signal corresponding to activity of unit A_i (*e.g.*, 0 and 1, or -1 and $+1$),

W_{ij} = weight of unit connecting A_i to R_j,

θ_j = threshold of R_j.

During the learning process, the values stored in the W-units are changed whenever the state of R_j does not correspond to some arbitrary *desired* response D_j for the given input pattern. This process is termed error-correcting "forced" learning, in that a correction is forced upon the network only if an erroneous response is made. Whenever it is necessary to correct a response, the strengths of all synaptic junctions (W-units) connected to that output change simultaneously according to some simple rule. A number of rules for changing values have been tried, most of them with some success, and it is perhaps simplest to express the possibilities [27] as shown in Table I,

TABLE I
SYNAPTIC GROWTH LOGIC

x_i	D_j	R_j	ΔW_{ij}
0	0	0	0
0	1	1	0
1	0	0	0
1	1	1	0
0	0	1	a_1
0	1	0	a_2
1	0	1	a_3
1	1	0	a_4

where the a's are some set of numbers and D_j is the desired response. These storage increments are usually selected so that weights increase algebraically if $x_i = D_j$ and decrease if $x_i \neq D_j$. Whether or not $x_i = 1$ is also considered in some schemes.

Verification of network learning has been obtained both by means of digital computer simulations and by experiments on a hardware model of the Perceptron system [28]. The latter possesses 400 inputs in a 20-by-20 array, approximately 400 A-units, and 8 R-units. It has successfully learned to recognize the letters of the English alphabet, in fixed position and font, performing the recognition by means of an 8-bit output code.

Rosenblatt's mathematical proof of network convergence, as amended by Joseph [29], rests upon the existence of a set of weighting functions W_{ij} which satisfy the response equations (1) and the arbitrarily specified dichotomy D_j, such that $R_j = D_j$ for all input patterns. Such a solution in fact exists only for a limited number of logical functions. For more than a few input variables, these constitute only a small fraction of the possible 2^M different logical functions (sets of dichotomies D_j) which might be specified for a set of M patterns. The percentage of correct responses to which the network will converge and the conditions under which convergence occurs when a solution does not exist remain to be analyzed.

More advanced versions of the simple Perceptron model have been postulated in which interconnections are permitted among A-units. Such an arrangement, termed a cross-coupled system, is clearly a time-dependent feedback system, since both the sequence of input patterns and internal activity determine network response. In this sense, the cross-coupled Perceptron can be described in somewhat the same terms as a sequential transducer, upon which subject a considerable body of literature exists [30]–[32], although analog and digital operations are mixed. The purpose of the cross-coupled system is to learn not only recognition of isolated patterns but also any linear transformation (*e.g.*, translation, rotation, etc.) of patterns which occur in close time sequence. The problem may be posed as follows: If the machine is shown and forced to give the correct response to a sequence of patterns P_i ,each followed by some transformation of the same pattern $T(P_i)$, will it tend to give the correct response to the presentation of $T(P_j)$ following learning of P_j alone, where P_j is not one of the patterns in the sequence P_i? For example, will the machine correctly identify a square presented in some location on the input raster in which a square has never previously occurred, if the machine is presented and taught a sequence of circles followed by their transformations and then taught to recognize a square presented in a single location on the raster? An affirmative answer is supported to some degree by computer simulation and by an analysis which is as yet incomplete.

It is apparent that the nature of the network transformations between raw input signals and association or learning areas is crucial. The recent work of Greene [33], [34] in which some of the mathematical properties of transformations are related to psychological evidence, especially Gestalt phenomena, is therefore significant. Highly simplified, Greene's suggestions may be interpreted in the following manner. Label input variables $x_1, x_2, \cdots, x_N$ (corresponding to points on an input raster), then any pattern $f(x_1, x_2, \cdots, x_N)$ may be represented by an expansion in orthonormal functions $\phi(x_1, x_2, \cdots, x_N)$ as

$$f(x_1, x_2 \cdots x_N) = \sum_{i=1}^{k} a_i \phi_i(x_1, x_2 \cdots x_N) \ldots \qquad (2)$$

Greene then points out the similarity of quantum mechanical mathematics to certain psychological data, and suggests that the concept "point of view" can be expressed by expanding a given input in terms of different sets of orthonormal functions $\{\phi_i\}$, $\{\psi_i\}$, etc. Gestalt phenomena are related to large values of the coefficients a_i of the expansions. Greene's efforts have been largely directed toward obtaining criteria on the basis of which sets of functions which are useful in describing the environment can be specified. Usefulness can be measured in terms of the degree to which member functions of a given set represent structures commonly encountered. This may be interpreted as a search for redundancy in the environment, that is, for sets of data which can be described (or coded) in simple ways. Given that a complex environmental configuration can be simply coded, however, there still remains the problem of associating or learning an arbitrary output code or response which is appropriate to the environmental event. In the simple terms of Fig. 5, Greene has tackled the first half of the system, the transformation box, while workers oriented toward learning devices have concentrated primarily on rules governing storage.

The properties of a simple linear expansion of the input variables with quantized output effectively equivalent to (1) have been considered by Mattson [35], who points out that the coefficients (weights) and threshold define a plane in N-dimensional space. The success of such an element in realizing a given dichotomy depends upon its ability to place the plane in space between those points (corresponding to combinations of the input variables) for which a 1 output and those for which a 0 output is desired. An example of a three-variable case for $R_j = x_3 \cdot (x_2 + x_1)$ in Boolean notation is illustrated in Fig. 8. Mattson then defines a

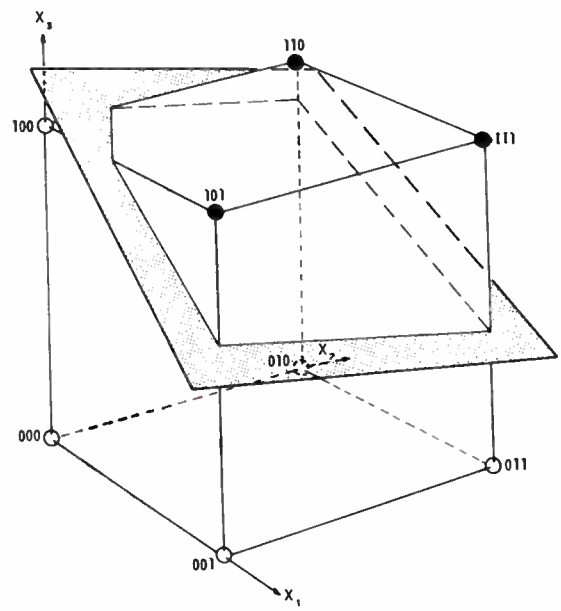

Fig. 8—Three-variable pattern space.

performance criterion in terms of the number of agreements between the element's actual responses and those desired, measured over-all patterns. He shows that, provided the performance as a function of any one of the input variables including the threshold possesses a single peak, the best possible performance is obtained with the threshold and coefficients W_{ij} set at the peak. A simple adjustment procedure for reaching the peak is to change each of the weights in turn, and measure whether or not performance improves. This process can be visualized in Fig. 8 by noting that a threshold change corresponds to displacement of the plane from the ori-

gin, while coefficient changes rotate the plane. The number of peaks on the performance curve is equal to the number of groups of +1 points in the pattern space separated from one another by groups of 0 (or −1) points. It can be seen that a single plane cannot separate more than one group of points in a pattern space. In order to realize the most general logical functions it is therefore necessary to provide either multiple planes, corresponding to cascaded linear-summation elements, or nonplanar surfaces, equivalent to nonlinear functions of the input variables.

Learning in terms of quantized outputs has been discarded by Widrow [36], [37], who considers the learning process from the point of view of minimizing the mean-square-error between the analog sum and desired output over the set of patterns. In terms of (2), letting the functions simply equal the input variables $\phi_i = x_i$, the error of a two-input summing device with respect to the mth pattern is

$$e(m) = f(m) - a_1 x_1(m) - a_2 x_2(m). \tag{3}$$

The mean square error over the set of patterns is

$$\overline{e^2} = \overline{f^2} - 2a_1\overline{f \cdot x_1} - 2a_2\overline{f \cdot x_2} + a_1^2\overline{x_1^2} - 2a_1a_2\overline{x_1 \cdot x_2} + a_2^2\overline{x_2^2} \tag{4}$$

in which the bar denotes average value. Providing the statistical properties of the sample patterns do not change during the learning process, the quantities $\overline{f^2}$, $\overline{x^2}$, $\overline{f \cdot x}$ and $\overline{x_1 \cdot x_2}$ are constants. They may be regarded as the mean square values of the function and the inputs, and the various cross correlations between function and inputs, respectively. Setting the partial derivatives of $\overline{e^2}$ with respect to the coefficients equal to zero, one obtains a parabolic equation defining an error surface. Widrow describes the search for a minimum on this surface in terms of hill-climbing techniques, and defines a standard "time-constant" corresponding to a change in coefficients which would result in a decrease in the error by a factor of $1/\epsilon$ per increment. Widrow also points out that there will exist errors over and above the minimum, due to 1) the fact that a small sample of patterns may not represent the same error surface as a large sample and 2) the noise introduced by finite adjustment steps. Formulas are derived for these errors under various assumptions. Although the use of a minimum mean square error criterion for network learning is attractive, especially because of familiarity, it should be noted that it is not the same as the minimum error rate when the output is binary quantized, equivalent to the algebraic sign of the analog sum, as in (1). The distinction is pointed out again in Section IV in connection with other learning models.

Minsky and Selfridge [38] have observed the need for variable sized "strides" in surface-searching techniques. Their comments also bear upon optimum-choice criteria in pattern recognition and are considered later in this section.

It is worthwhile at this point to recast the simple Perceptron and other models in terms of basic psychological observations, as made by Pavlov and recounted by Hebb, in order to see just what features of human behavior are being represented. For this purpose, Pavlov's famous conditioned reflex experiment on dogs is particularly pertinent. The experiment is as follows. When presented with food, a dog salivates. Prior to conditioning, the same dog makes no response to the ringing of a bell. If, now, a bell is rung simultaneously with the presentation of food for a number of times, the dog will salivate upon the ringing of the bell alone. The implication is that learning consists of the time association (simultaneity of occurrence) of two or more complex stimuli. The network representation of the conditioned reflex is shown in Fig. 9. In Rosenblatt's terms, the transformed "food" signals are the forcing functions and are, during the training sequence, indistinguishable from the desired output since food and salivation always occur together via the large fixed synaptic junction. The transformed "bell" signal represents the input as mapped on the A-units. As the desired response, salivation, and the bell signal occur repeatedly, the strength of the corresponding synapse increases in accordance with Hebb's postulate. When the synapse is sufficiently strong, the bell alone can induce salivation. The variable synaptic junction is therefore considered to be computing something akin to Uttley's conditional probability, or simply some quantity, as in Rosenblatt's W-unit, resembling the correlation coefficient between input and output. It is worth noting that Hebb's theory of positive synaptic reinforcement has been challenged [39] in favor of a viewpoint which regards learning as a process of inhibiting extraneous responses. While the distinction may be of considerable importance physiologically, there does not appear to be any conceptual network problem in computing a negative quantity equivalent to the absence of correlation rather than a positive quantity representing its presence.

It is generally assumed, although not explicitly, that the above basic structure can be extended to more subtle situations. Consider the case in which no built-in mechanism exists, as in the food-salivation circuit,

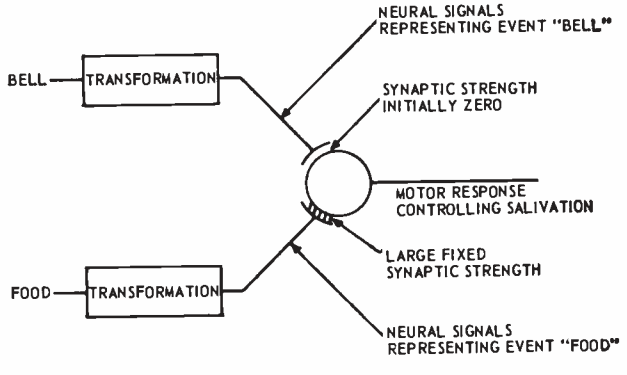

Fig. 9—Conditioned reflex network representation.

for forcing the desired response. In this case, how can the network be made to produce some arbitrarily desired output? It is generally implied that the over-all network must contain some mechanism for stimulating outputs to occur, more or less at random, in the presence of certain inputs (*e.g.*, punishment). This corresponds to trial-and-error learning. Thus, the network will continue trying various outputs until the desired one occurs, at which point the random forcing ceases and the network dwells in the desired-response condition long enough for the strength of the synapse between arbitrary input pattern and response to increase. If this is indeed a valid model, then it does not seem necessary to draw a distinction between the forced and the reward-punishment forms of learning, except for the niceties of psychological parallels, since the forcing connection is replaced by a random signal generator which eventually causes the desired output and therefore produces effectively the same result.

In this light, consider the problem of learning to produce the sound "*aaa* · · · " in response to the visual input pattern *A*. The network may be represented as in Fig. 10(a) in which the same pattern is presented to both teacher (fixed network) and pupil (learning network). The comparison between the teacher's output sound "*aaa* · · · " and that of the pupil is made either by the pupil or the teacher. In either case, lack of comparison excites trials of other possible outputs via some forcing process such as motivation on the part of the pupil or reward and punishment by the teacher. Somewhere within the learning network must exist a connection represented by Fig. 10(b), in which a synaptic strength is increased when trials ultimately result in the correct "*aaa* · · · " response and the machine dwells for a time in this state.

While the above network models considerably stretch the psychological analogies, it is believed that they represent the implications of much of the current work in the field of learning machines. Some consequences of the model are also significant. It is apparent, for example, that a simple learning device (human or otherwise) is no panacea for those applications in which survival is not possible under conditions of a single error. The alternative in such cases appears to be a device which can perform the trial-and-error process symbolically, and "think" about the possible results of a response to an input which in fact has never occurred. The learning machine networks under consideration in this review are far from such a level of sophistication, although programmed models reported elsewhere in this issue [5] are more nearly approaching such behavior.

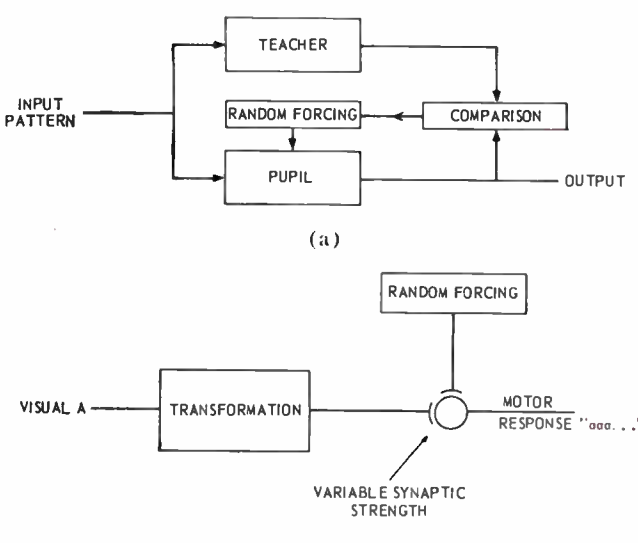

Fig. 10—Trial and error learning. (a) Block diagram of system functions. (b) Site of learning.

A. Character Recognition Networks

One of the tasks to which human and some animal nervous systems are notably suited is the learning of arbitrary responses to various sets of complex visual images. In particular, the ability to learn a language of some sort is a fairly definitive feature of such systems. As a design goal for learning machines, therefore, alphanumeric character recognition has frequently been selected as having sufficient complexity to be interesting while being capable of solution at various levels of difficulty.

A number of character readers have been designed and tested with varying degrees of success. While not nerve-net models in any sense, these networks have structures which bear closely upon the proposed models for learning machines, and in addition provide some objective measure of performance. The salient features of several such designs are therefore reviewed in the following paragraphs.

A rigorous general treatment of character recognition systems has been published by Chow [40]. Although dealing with sequential reading of magnetic ink characters, Chow considered system inputs to be obtained from a tapped delay line, and therefore his development is equally applicable to spatial patterns. The problem is regarded as one of testing multiple hypotheses in statistical inference, that is, testing for each character the hypothesis that the observed pattern is indeed the given character against the hypothesis that it is not. Consider the multiple signal inputs to the system $v_1, v_2, \cdots, v_s$, as making up a vector v. The possible characters which may appear are labelled $a_1, a_2, \cdots, a_c$. Chow derives a formula for the magnitude of the expected risk in making a given decision in terms of: $F(v|a_i)$, the conditional probability of the vector v occurring if the pattern is in fact the ith character; p_i, the *a priori* probability that the ith character occurs; w_{ij}, the (arbitrary) weight assigned to misreading the ith character as the jth one; and the optimum decision rule δ^* (Bayes strategy). Based upon the formula, a network can be derived whose form is given in Fig. 11. In the first level, the conditional probabilities $F(v|a_i)$ are cal-

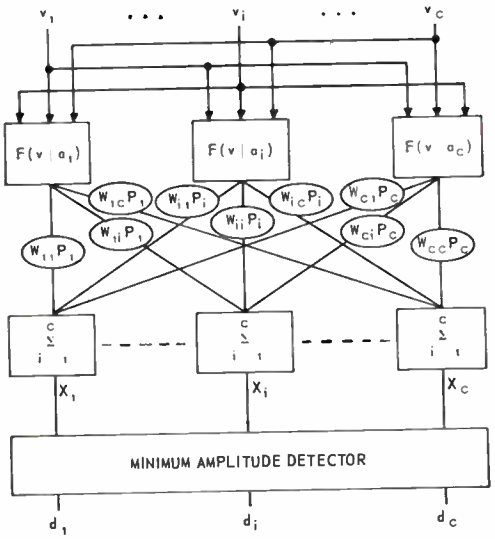

Fig. 11—Optimum recognition system.

culated for each of the c characters. The risk assigned to each decision is then calculated in the second level as the weighted sum

$$X_j = \sum_{i=1}^{c} (w_{ij}p_i)F(v|a_i). \tag{5}$$

In the final layer, the minimum-risk signal is selected (one decision signal 1, all others 0). If a minimum error rate rather than a minimum risk criterion is chosen, the network reduces simply to weighting each $F(v|a_i)$ with its corresponding p_i, and selecting the maximum signal (in both cases, the rejection channel has been omitted from this discussion for simplicity). Chow's work thus provides a conceptual framework for designing recognition systems, and furnishes an objective measure of performance, but leaves open the technique for network synthesis of the conditional probability functions.

The effects of specific transformations upon raw input data consisting of alphabetic characters have been reported by Selfridge [41] and Dineen [42]. They studied such operations as edging (similar to Taylor's detail filter) and averaging in local regions, performed by means of computer simulation, but they did not construct a full-scale alphabetic recognition system.

A network which crudely approximates Chow's conditional probability calculation has been simulated by Bledsoe and Browning [43]. The input consisted of a 10 by 15 raster, with illumination levels binary quantized. Pairs of points were selected at random over the raster and transformed into one of four signals per pair, corresponding to the possible combinations 00 through 11. During something akin to a learning process, binary weights (0 or 1) were stored in cells corresponding to active transformed inputs *and* the known character, over a reasonably large sample of characters. During testing, the transformed binary inputs weighted by the corresponding stored value were summed for each character and the largest quantity was selected. A simplified representation of the system is shown in Fig. 12. Bledsoe and Browning's results were: 100 per cent correct recognition of typewritten numerals, up to 92 per cent of hand-block print with character positioning and rotation simulated, and a total of 104 sample characters (four alphabets) used both for learning and for subsequent recognition.

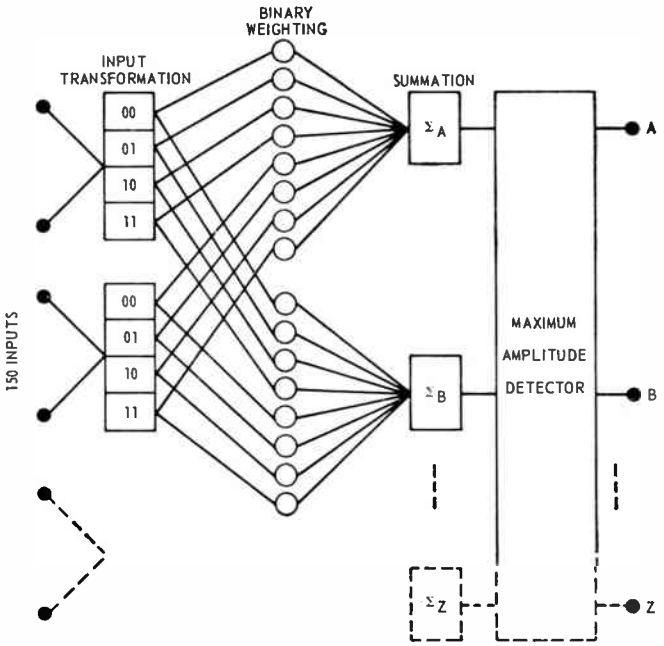

Fig. 12—Model of character reading program.

A computer specifically designed for carrying out spatial data processing has been proposed by Unger [44]. It consists of a large number of limited capacity arithmetic and memory elements, each connected with its neighbors and programmed from a central control. Unger showed how pattern features such as oriented corners and concavity could be detected by the system, which has been simulated on a computer.

A network modeled directly after the Perceptron has been simulated by Roberts [45] in studies of hand-printed character recognition. The network was modified, however, by selecting S to A-unit connections from neighborhoods rather than at random over the raster, and by allowing A-unit activity to be continuously variable rather than binary. On a 36-by-36 raster, Roberts obtained up to 94 per cent correct recognition on samples of hand-printed characters.

A more sophisticated set of input transformations has been simulated by Doyle [46]. The system consisted of a series of tests performed upon the input pattern, such as counts of horizontal-line intersections, convexities in various directions, etc. During storage, results were used to determine a value associated with each test for each of a set of sample characters. During trials, test results were weighted according to the value of the test for each character, the results summed, and the character having the largest score was selected. Doyle's results were approximately 88 per cent recognition on a

set of badly distorted hand-printed samples of ten different alphabetic characters displayed on a 32-by-32 array. It should be noted that human recognition of hand-printed characters, in the absence of context, tends to be in the neighborhood of 95 per cent [45].

Approaching pattern recognition from the viewpoint of multiple hypothesis testing, Minsky and Selfridge [38] consider the *a priori* and conditional probabilities associated with a series of tests performed upon the patterns. Based upon an admittedly restrictive assumption that the test results are statistically independent, they derive an optimization formula and network realization in which binary test results are weighted according to the conditional probability of the ith test being successful (e.g., 1), given the jth class of characters. The network has structure similar to Fig. 11. Minsky and Selfridge then show that quantities w_{ij} proportional to the conditional probabilities p_{ij} can be learned according to the simple rule

$$w_{ij}' = k(w_{ij} + 1), \; i\text{th test} = 1$$
$$w_{ij}' = kw_{ij}, \; i\text{th test} = 0. \tag{6}$$

They point out that the analysis and resulting networks apply directly to Perceptron-type models, but emphasize the highly organized as opposed to random arrangement of the optimum net.

It is tempting to draw a parallel between the foregoing spatial recognition approaches and more formal analyses of the detection or recognition of temporal signals in noise, particularly as represented by the matched filter concept. An excellent introduction to the latter has been published by Turin [47]. Briefly, a matched filter is a network whose transfer function is the complex conjugate of the spectrum of the signal to which it is matched. Another way of stating this is that the transfer function of a matched filter is the complex conjugate of a filter whose impulse response is identical to the signal to be detected. This is illustrated (from Turin) in Fig. 13(a). The matched filter response characteristic can be derived from the criterion of maximizing instantaneous output signal power (signal value squared) relative to noise power, or alternatively, from the criterion of maximizing the probability of accepting the correct hypothesis. Both approaches lead to the same complex-conjugate filter for the case in which the signal is distorted by additive, Gaussian noise. A generic realization of the matched filter is a tapped delay line with the outputs of the taps weighted by the values of $s(-\tau)$ within the range $-T<t<0$, and summed to form an approximation to the output signal $y(t)$, given ideally by

$$y(t) = \int_{-T}^{0} s(-\tau)x(t-\tau)d\tau. \tag{7}$$

Such a network is illustrated in Fig. 13(b). It is clear that if $x(t)$ is the result of temporal scanning of a spatial pattern raster, and if the $s(i)$ are weighted according to

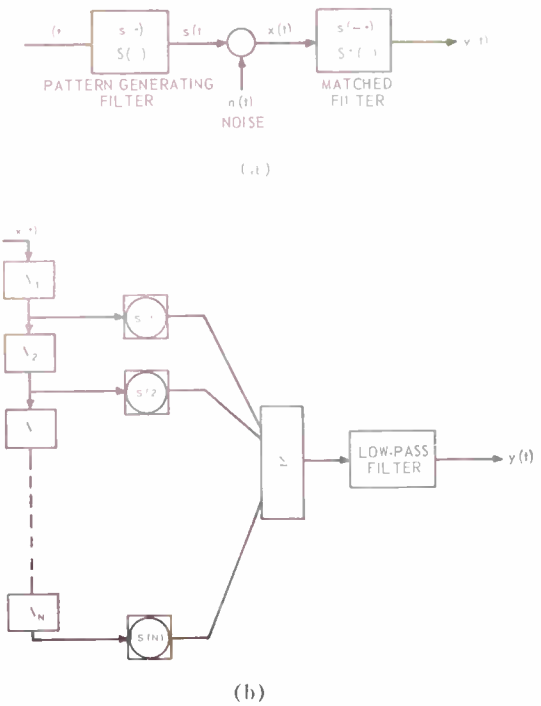

Fig. 13—Matched filters. (a) Model of signal generation and detection system. (b) Realization of filter requirements.

the value of the ideal pattern at the ith scanning point, then $y(t)$ will contain an impulse whose relative magnitude is dependent upon the amount of noise (random spots) superimposed upon the pattern, and whose occurrence in time depends upon pattern location.

IV. Problems of Recognition and Learning

In this section, an attempt is made to restate the recognition network synthesis and network learning problems in terms of several different disciplines, and to single out those features of the problem to which the works reviewed above represent common approaches. Some of the areas in most urgent need of further investigation are discussed.

Consider a network with N input variables $x_1, x_2, \cdots, x_N$ and Q output lines $y_1, y_2, \cdots, y_Q$. Each input and output is quantized at r discrete levels. Let $r=2$ for simplicity. While some significant work on multivalued logic is currently in progress [48], the problem statement justifies binary logic at this stage on the basis of familiarity to the reader and ease of representation. Let the structure of the network be constrained, for the time being, by forbidding feedback connections. That is, the network interconnections are directional, and are arranged such that from any point there is no path through the network returning to that point.

Of the 2^N input configurations possible, assume that the environment is so arranged that only a relatively small number in fact can occur. Such an assumption is certainly not valid when the environment is that of a digital computer in which all possible configurations are

very likely to occur in a given register. In the world around us, however, events are considerably constrained by natural laws, with the result that we seldom see purple cows, or random black-and-white spots, or any of a number of potentially see-able events. Of the relatively small number of environmental configurations which can occur, we must necessarily design the network on the basis of an even more limited number M of samples of these configurations. Additional information may be available regarding known transformations T (*e.g.*, translation and rotation) which enable us to specify an additional set of input configurations $T_1(M)$, $T_2(M)$, $\cdots$, which can be expected to occur. Alternatively, it may be necessary to extract this information from the properties of the M samples.

It is desired to produce some unique configuration $y(s)$ of output signals in response to any member of one of C different sets ($s=1, 2, \cdots, C$) of input configurations. The sets may, of course, be coded in any arbitrary way, but it is necessary that $Q \geq \log_2 C$. It may be argued that the selection of a code cannot be arbitrary but rather must be specified by the environment. Thus, the manner in which the visual configuration A is coded by the vocal chords depends upon which language we wish to speak. Since we have scant data on either visual or vocal coding, however, it seems simpler to break the problem into a two-part network design. In the first network the input configuration is reduced to some simple code representing the class s, and in the second network the class is recoded in some redundant form compatible with the environment (*e.g.*, as in speech synthesis) [49], [50].

Reasonable physiological arguments have been advanced [51] for the use of one-out-of-C coding schemes, in which a separate line is provided for each character or set. Such coding arrangements are attractive from the standpoint of compatibility with mathematical models of multiple hypothesis testing, as in Figs. 11 and 12, and in the models of Doyle, Minsky and Selfridge, and in matched filters. They suffer from at least two serious drawbacks, however. Some thought will show that all of these recognition schemes depend upon a template-matching point of view, in which the actual pattern is matched, statistically, against a single ideal pattern. If two or more rather different patterns are to be coded into the same set, it becomes difficult to define an ideal against which to compare, and subsets must usually be established. For example, there is a strong tendency to regard as "different" the patterns A, **A** and a, even though their vocal coding is identical. This leads to a proliferation of templates and code bits. It is, of course, possible to follow a one-out-of-C coding network with OR circuits to recombine subclasses. In the extreme, template stages become equivalent to the AND stage of a canonical AND-OR realization, in which a separate template (AND circuit) is provided for every possible minterm (pattern). The second disadvantage of one-out-of-C coding is its relatively inefficient use of the available code bits, only C different sets being represented compared to a potential of 2^C. If the patterns in a class differ from one another by well-defined noise processes and the number of classes is reasonably limited, however, it is likely that this choice of code will continue to be useful simply because mathematical tools exist for specifying optimum network structure in such terms. In any case, having selected a suitable code, a complete list of available data might conceivably be constructed in truth-table form as in Table II, in which the sets consist of various forms of English alphabetic characters for illustrative purposes.

TABLE II
DATA TRUTH TABLE

Sample	Character	Inputs					Outputs				
		x_1	x_2	$\cdots$	x_i	x_N	y_1	y_2	$\cdots$ y_j	$\cdots$	y_Q
1	A	0	1	$\cdots$		1	0	0			1
2	B	1	0	$\cdots$		1	0	0			0
.	.										
.	.										
.	.										
26	Z	0	1	$\cdots$		0	1	1			0
27	a	1	0	$\cdots$		0	0	0			1
28	b	0	0	$\cdots$		1	0	0			0
.	.										
.	.										
.	.										
52	z	0	1	$\cdots$		0	1	1			0
53	**A**	1	1	$\cdots$		1	0	0			1
54	**B**	0	0	$\cdots$		1	0	0			0
.	.										
.	.										
.	.										
k		x_{1k}	x_{2k}	$\cdots$	x_{ik}	x_{Nk}	y_{1k}	y_{2k}	$\cdots$ y_{jk}	$\cdots$	y_{Qk}
.											
.											
.											
M		x_{1M}	x_{2M}	$\cdots$	x_{iM}	x_{NM}	y_{1M}	y_{2M}	$\cdots$ y_{jM}	$\cdots$	y_{QM}

Consider now, a single output bit y_j which performs some arbitrary dichotomy upon the input patterns. From the standpoint of y_j, all of the information contained in the input signals is expressed by either 0 or 1. The network synthesis problem therefore consists of determining the redundant structure contained in the input signals, and designing a practical network which removes that structure with respect to y_j. The learning problem consists of determining simple, readily mechanized operations which can be incorporated into the network to permit it to calculate the parameters required for synthesis.

It is standard practice to represent structure by means of mathematical functions which describe the relationships among as many variables or points in one variable as possible. For example, a sine function describing a waveform may be regarded as representing in simple notation a large number of relationships which could otherwise be specified only by a long listing of function values vs time. The problem in recognition network synthesis is therefore one of selecting easily mechanized operations which also represent structures commonly encountered in the environment. If a group of operations is chosen which constitutes a complete, linearly independent set, then any function can be precisely represented in terms of their weighted sum, a simple and therefore attractive mechanization. For the N-dimensional input and M patterns with which we are dealing, an output code bit can be expressed in these terms as

$$y_{jk}(x_1, x_2 \cdots x_N) = \sum_i a_{ij}\phi_{ik}(x_1, x_2, \cdots, x_N) \qquad (8)$$

in which y_{jk} is the value assumed by the jth output line for the kth pattern (configuration of the inputs x_1, x_2, $\cdots$, x_N), and ϕ_{ik} is the value of the ith function of the kth input ($k=1, 2, \cdots, M$). For a complete set of linearly independent functions, $i=1, 2, \cdots, M$. That is, the value of the output for each pattern is given by the weighted sum of the values assumed by the set of functions of the input variables for that pattern. The selected functions ϕ_i may possess the additional useful property of being orthonormal, that is, of satisfying the relation

$$\frac{1}{M}\sum_{k=1}^{M} \phi_{ik}\cdot\phi_{jk} = 0, \qquad i \neq j$$
$$= 1, \qquad i = j. \qquad (9)$$

In this special case, the coefficients of the expansion are given by

$$a_{ij} = \frac{1}{M}\sum_{k=1}^{M} y_{jk}\cdot\phi_{ik}. \qquad (10)$$

If the selected functions ϕ_i are orthogonal but do not constitute a complete set, then the expansion will not, in general, exactly represent the desired function. An approximation to the desired output y_j may be expressed as

$$y_{jk}^* = \sum_i a_{ij}\phi_{ik} \qquad (11)$$

in which the index i ranges over a set of functions ϕ_i fewer in number than M. The values of the coefficients given by (10) will result in the minimum mean square error between y_j^* and y_j for the given ϕ_i and desired function y_j, where the error is calculated over the $k=1, 2, \cdots, M$ input patterns.

If the selected functions ϕ_i are not orthogonal but are linearly independent and constitute a complete set, then the calculation of the coefficients a_{ij} may be performed by a matrix inversion. Eq. 8 can be expressed in matrix notation as

$$[\phi][A] = [Y] \qquad (12)$$

in which $[\phi]$ represents the square matrix of the network inputs or functions of the inputs over the M sample patterns, $[A]$ the column of the coefficients $a_{1j}, a_{2j}, \cdots, a_{Mj}$, and $[Y]$ the (jth) column of desired responses for the M patterns $y_{j1}, y_{j2}, \cdots, y_{jM}$. The solution for the coefficients is given by

$$[A] = [\phi]^{-1}[Y] \qquad (13)$$

where the -1 superscript denotes an inverse matrix. Straightforward calculation of the coefficients a_{ij} from (13) may involve the evaluation of determinants; for example, by Cramer's Rule,

$$a_{ij} = \frac{|\phi|_{ij}}{|\phi|} \qquad (14)$$

where $|\phi|_{ij}$ is the determinant formed by replacing the ith column of $[\phi]$ by $[Y]$. Eq. (14) is clearly a difficult operation to mechanize in a simple network. While a large number of alternative methods exist for evaluating an inverse matrix, their direct network mechanizations may be described as involving either a substantial number of parallel arithmetic units (multiplication and addition) or iterative networks, together with storage elements for intermediate results. Neither of these levels of complexity is achieved by present learning network models.

If the selected functions ϕ_i do not form a complete set, then in general it is not possible to obtain a solution for the coefficients a_{ij}.

The problem of an exact solution for network parameters is relieved somewhat in the case of digital, as opposed to analog, networks. That is, in most cases we do not insist that a linear combination of functions of the input patterns represent the desired output exactly, $y_{jk}^* = y_{jk}$ for all $k=1, 2, \cdots, M$ input patterns. Rather, it is only required that the resultant be above or below some level according to whether the code bit is 1 or 0. If binary levels are taken to be $+1$ and -1 rather than 1 and 0, this requirement can be expressed as sgn $[y_{jk}^*] = y_{jk}$. It is apparent that quantization re-

moves a large degree of constraint on the network, since for a given input it is only necessary that y_{jk}^* lie in some region (*e.g.*, from 0 to $+\infty$) rather than at some point (*e.g.*, $+1.0$). Optimization criteria must also be appropriately modified. In the quantized case, it is reasonable to minimize $(y_{jk}-\text{sgn}\ [y_{jk}^*])^2$ averaged over the M input patterns, rather than $(y_{jk}-y_{jk}^*)^2$. Just what effect these changed requirements have upon the calculation of the expansion coefficients a_{ij} and upon the choice of a set of suitable functions ϕ_i is not known except in special cases.

We may now describe some of the nerve-net models reviewed in Section III in terms of the above representations. In the Perceptron, for example, considering only A to R-unit connections $\phi_i(x_1, x_2, \cdots, x_N)=x_i$ and

$$y_{jk}^* = \sum_{i=0}^{N} a_{ij}x_i(k) \tag{15}$$

where $x_i(k)=$activity of ith A-unit in response to kth pattern, $a_{ij}=W_{ij}$, and $y_{jk}^*=$input summation to jth R-unit. The output signal is quantized by $y_{jk}=\text{sgn}[y_{jk}^*]$. In general, the functions x_i do not form a complete set since there are only N inputs and there can be as many as 2^N different patterns. It is not clear whether the functions x_i have any tendency to be either independent or orthogonal since S-to-A-unit mapping is performed at random, with S-units furnishing equal positive and negative excitation. The learning process therefore cannot be described in the simple terms of either (10) or (14). A restricted version of the Perceptron, however, yields some insight into the relationship between (10) and the learning process specified by Table I. Suppose that only complete truth tables are presented; that is, $M=2^N$ with all possible input configurations represented. In this special case, with binary values -1 and $+1$, the input functions are orthonormal since

$$\frac{1}{2^N}\sum_{k=1}^{2^N} x_{ik}\cdot x_{pk} = \begin{cases} 0, & i \neq p \\ 1, & i = p \end{cases} \tag{16}$$

where k represents the row (pattern), and i and p the columns (inputs). If the patterns occur with equal frequency and value change occurs over all patterns (as if $R_j \neq D_j$), and if the increments are taken to be $a_1=a_4=-a_2=-a_3=1$, (10) is mechanized except for a scale factor of 2^N. The result can be expressed as a simple count of the number of agreements minus the number of disagreements between the input bit and desired output. In an incomplete truth table (*e.g.*, Table II), a simple count of this type is in general inadequate, since orthogonality can no longer be guaranteed. It is worth noting that the above procedure and Widrow's surface-searching technique are equivalent in the case of orthogonal inputs. The latter is more powerful in the general case, since it results in a minimum mean-square error regardless of input function properties.

In the Perceptron model, coefficient calculation is based neither on a minimum mean square error criterion nor upon an assumed independence or orthogonality. Rosenblatt and Joseph's proof of learning convergence—given the existence of a set of coefficients which satisfy sgn $[y_{jk}^*]=y_{jk}$ over all $k=1, 2, \cdots, M$ patterns—is therefore of considerable interest. The proof is rather tortuous, however, and does not furnish much insight into the process. The work of Stafford and Deschamps, described by Kelly [52] in a recent discussion of the learning problem, provides a somewhat clearer means of visualization, particularly in simple cases. They note that the requirement sgn $[y_{jk}^*]=y_{jk}$ over the set of M patterns may be expressed by

$$y_{jk}^*\cdot y_{jk} = [P_k][A_{ij}]\cdot y_{jk} > 0, \quad k = 1, 2, \cdots, M, \tag{17}$$

where $[P_k]$ is the kth row vector of the input functions ϕ_{ik}, corresponding to the kth pattern, $[A_{ij}]$ is the coefficient column vector, and y_{jk} is the desired output (± 1) for the kth pattern. Eq. 17 may be written $[P_{jk}]\cdot[A_{ij}]>0$, in which

$$[P_{jk}] = [P_k]\cdot y_{jk} = [\phi_{1k}\cdot y_{jk}, \phi_{2k}\cdot y_{jk}, \cdots, \phi_{ik}\cdot y_{jk}, \cdots].$$

This says that the desired function can be realized if the coefficient vector $[A_{ij}]$ possesses a positive projection upon all pattern vectors, when the latter are multiplied by the sign of the desired output. A vector representation of the OR function in terms of the $[P_{jk}]$ vectors is illustrated in Fig. 14(a). It is apparent that a vector exists which has a positive component upon the $[P_{jk}]$ vectors (*e.g.*, $[A_{ij}]=[+1, +1, +1]$). Stafford and Deschamps have demonstrated that the error-correcting learning procedure has the effect of increas-

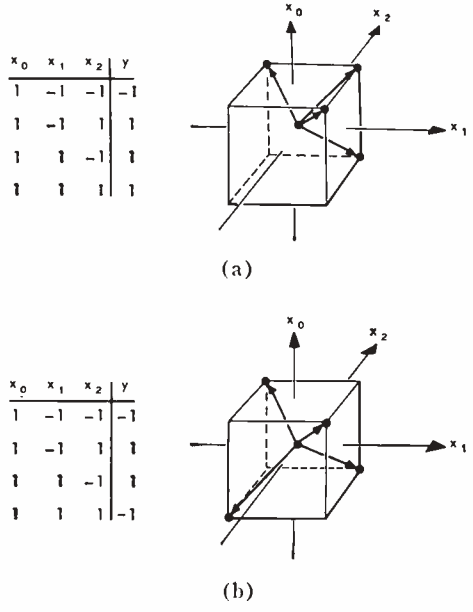

Fig. 14—Pattern vector representations. (a) Logical OR function. (b) Exclusive-or function.

ing algebraically the component of the coefficient vector $[A_{ij}]$ along the $[P_{jk}]$ vectors, and that if a solution exists the procedure will converge. A case in which no solution exists, the exclusive-or function, is illustrated in Fig. 14(b).

A qualitative comparison between the minimum-mean-square error and the error-correcting learning procedures is now possible. The former effectively calculates the center of gravity of the $[P_{jk}]$ vectors, while the latter locates a plane (or N-1 dimensional space) relative to which the P_{jk} vectors all lie to one side. In many simple cases, the two procedures are equivalent, for all practical purposes. As the vector space increases in dimension, however, it becomes possible for the center of gravity to fail to locate a solution space which indeed exists.

Returning now to other recognition and learning network models, in the case of Fig. 12, the expansion is in terms of Boolean product pairs $x_i\bar{x}_k$, $\bar{x}_ix_k$, x_ix_k and $\bar{x}_i\bar{x}_k$. The coefficients are calculated in something like a step-function version of (10), with $a_{ij}=1$ if $\phi_{ik}\cdot y_{jk}=1$ occurs anywhere in the set of patterns. In the case of Taylor's model (Fig. 5), the functions represented by the series of input transformations are specified in detail, but their mathematical properties with respect to a set of spatial patterns have not been determined. His coefficient calculator is equivalent to an integral form of (10), being mechanized by an analog multiplying and integrating device.

Chow's optimum decision network can be regarded as calculating an expansion in terms of the function $F(v|a_i)$, whose form remains unspecified. Doyle's calculations involve functions (tests) which could conceivably be mechanized in a network, but there is no assurance that they represent anything approaching an optimum selection. Since the value of a test is determined by the statistical agreement of its result with the members of a set of sample patterns, the network may be described as a conditional probability calculator based upon assumed test independence. Minsky and Selfridge specifically note the assumption of statistical independence of tests in their development of a more formal optimum recognition and learning model. Learning is accomplished by incremental calculation of conditional probabilities by (6). It is useful to assume that the conditional probability of the ith test ($\phi_{ik}=1$), given that the jth class occurs ($y_{jk}=1$), is equal to the conditional probability $\phi_{ik}=0$, given $y_{jk}=0$. In this case, the conditional probability is $p_{ij}=\frac{1}{2}\cdot(a_{ij}+1)$, where a_{ij} is given by (10). The network weight w_{ij} can therefore be described as proportional to a_{ij} plus an additive constant bias term. Minsky and Selfridge discuss the assumption of independence and state that, in its absence, the only alternative appears to be the calculation of higher-order joint probabilities.

The last remark serves to point up what is probably the central problem in recognition and learning network synthesis. This is the selection and analysis of suitable nonlinear functions of the input variables. It is apparent that the simple linear expansion of (15) will frequently be inadequate to approximate an arbitrary output function. However, general criteria do not exist for the selection of more complex functions of the inputs which ideally should be as few in number as possible, readily mechanized, and capable of modification in such a way that over-all network learning will occur. Consideration of two types of such functions will illustrate the point.

The importance of nonlinear operations upon the inputs suggests the use of product terms in a functional expansion. The work of Huffman [53] and that of van Heerden [54] make use of the modulo-two sum of k variables. This is the algebraic product $x_1x_2\cdots x_k$ (k odd) or its negative (k even), if the binary values ± 1 are used rather than 0 and 1. Their work can be extended in the following manner. Since all possible products of N binary variables taken 1, 2, $\cdots$, N at a time makes up a complete set of 2^N orthogonal functions, any arbitrary output code bit can be represented by

$$y(x_1, x_2, \cdots, x_N) = \sum_{i=1}^{N} a_ix_i + \sum_{i=1}^{N}\sum_{j=1}^{N} a_{ij}(x_ix_j) + \cdots + \sum_{i=1}^{N}\sum_{j=1}^{N}\cdots\sum_{k=1}^{N} a_{ij\ldots k}(x_ix_j\cdots x_k) + a_{12\ldots N}(x_1x_2\cdots x_N) \tag{18}$$

with $i\neq j\neq k\cdots$, in which the coefficients are given by

$$\begin{aligned} a_i &= \frac{1}{2^N}\sum y\cdot x_i \\ a_{ij} &= \frac{1}{2^N}\sum y\cdot(x_i\ x_j) \\ &\vdots \qquad\qquad \vdots \\ a_{12\ldots N} &= \frac{1}{2^N}\sum y\cdot(x_1\ x_2\cdots x_N). \end{aligned} \tag{19}$$

Network learning of correct coefficient values can be readily mechanized along the lines indicated in Table I. Convergence is assured by the existence of a solution. As a synthesis technique such an expansion is obviously impractical, however, since the network must contain 2^N elements.

A similar product-term functional expansion which will be familiar can be expressed as

$$\begin{aligned} y(x_1, x_2\cdots x_N) = {} & a_1\bar{x}_1\bar{x}_2\cdots\bar{x}_N \\ & + a_2\bar{x}_1\bar{x}_2\cdots x_N \\ & + \cdots \\ & + a_{2^N}x_1x_2\cdots x_N \end{aligned} \tag{20}$$

in which the bar denotes the complement (algebraically,

$1-x$, for binary levels 0 and 1). This is simply the cannonical-form Boolean representation with the coefficients a equal to 0 or 1. Again, synthesis is impractical because no economic simplification techniques exist for large values of N. If the term "learning" is still applicable to such a network, then mechanization becomes particularly simple, since it is only necessary to make $a_k = y_k$ the desired output for the kth input pattern.

The foregoing serves to illustrate some of the difficulties encountered when cascade or multistage logical networks are considered. It is apparent that complex functions employed in a linear expansion can themselves be mechanized by means of summation and threshold circuits. For example, the AND terms of (20) can be realized with the linear-logic circuit of Fig. 15(a), while the exclusive-or terms of (18) require a cascade linear-logic arrangement, illustrated for the case of two input variables in Fig. 15(b). As the complexity of such built-in functions of the raw inputs is allowed to increase, the circuits can be regarded as property filters [55]. This term usually refers to networks which detect the presence of some geometrical property of spatial patterns, such as corners, edges, convexities, number of separate objects in the field. The detection and counting of particular features of patterns has been employed in a number of character reading schemes, of which Doyle's work is representative. Although the property filter point of view is intuitively attractive, no general practical procedures exist for making an optimum selection of suitable filters based upon sample patterns and desired output data.

As an alternative to selection and fixed installation of complex functions of the inputs, the possibility of components or networks which can learn to realize suitable functions is attractive. The term suitable means, qualitatively, that the filter should learn to match or detect some feature or features of the environment, and that its output should be useful in realizing the desired network output function. Since complex operations can be mechanized by components identical with those known to be capable of learning, as described previously, multilevel network learning appears to be feasible, at least in principle. Except in special cases, however, present techniques for incorporating such sophistication into network behavior have little advantage over purely random searching among the functions realizable with a given network structure.

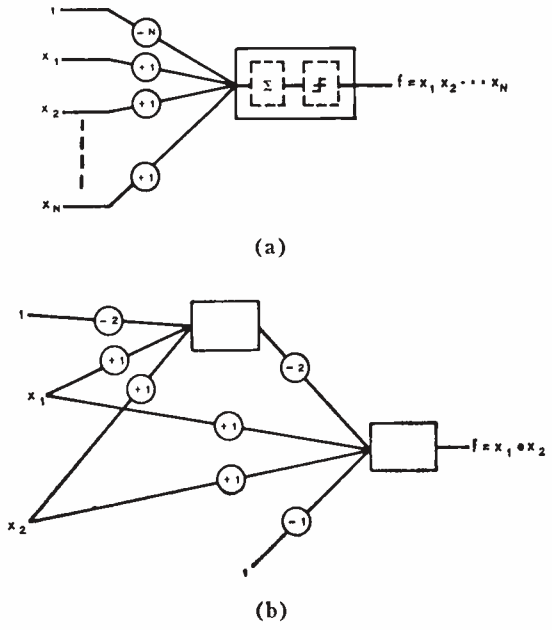

Fig. 15—Linear-logic mechanizations. (a) AND circuit. (b) Exclusive-or network.

V. Sequential Networks

The recognition networks discussed so far have contained no feedback paths, and consequently it has not been necessary to give any particular consideration to the time sequence of events. With feedback permitted, however, a considerable increase in the sophistication of machine behavior can be anticipated, as well as an increasing dependence upon specific time sequences. A number of potential advantages can be listed in qualitative terms. It should be possible, for example, to perform complex transformations upon the input patterns by means of iterative operations employing a very limited number of active components and some amount of storage. In the limit, of course, such a network becomes simply a Turing machine. It is also clearly possible for a network with feedback to compare or perform other operations upon patterns separated in time, an important consideration for contextual aid in recognition. Comparing the results of a series of transformations with new sensory data, or directing the re-examination of portions of sensory data based upon the outcome of a calculation, are obviously included in the above. Such network operations begin to resemble what is called reasoning, and border upon the programmed problem-solving approaches reviewed elsewhere in this issue [5]. At this time, the possibility of synthesizing networks, as opposed to computer programs, which operate at so-called higher levels of abstraction, can only be speculated upon.

The language which is probably most appropriate for the discussion of quantized feedback networks is that of sequential machines, although there is a close relationship to sampled-data control system theory as well. It is difficult to comment intelligently upon the potential application of these disciplines to recognition and reasoning problems for two reasons. First, it is safe to say that no practical general synthesis procedures exist for designing sequential networks to deal with the complex sensory events which are under discussion in this review. Second, no major effort has yet been made to couch the psychological or physiological language of human and animal behavior in terms amenable to these disciplines, or vice versa. In view of these difficulties, and the tentative nature of this aspect of self-organizing

machines, the interested reader is encouraged, and directed to [32] and [56] for sequential machine theory, and to the treatment by Truxal [57] for sampled-data control systems.

In the foregoing discussions of networks with and without feedback, it is almost universally assumed that the topology of network interconnections remains fixed, while storage may or may not occur. A rather interesting and specialized subclass of sequential machines is therefore represented by an evolutionary point of view. Broadly speaking, the concept is that a machine must seek to make those network connections which are most useful, based upon some criteria, and to discard unused connections. An experimental model which evolves a structure representing an arbitrary time sequence has been simulated by Foulkes [58], who considered a machine capable of splitting its state (generating new network elements) if a given state (set of component states) does not provide useful information. For example, if the machine state 00 provides only a 50-50 prediction of the next bit in a time sequence, two new states 100 and 000 are generated. The model continues to collect prediction data corresponding to joint conditional probabilities, and to split states as required, until a sufficiently high level of over-all performance is achieved. Some of the mathematical limitations of an evolutionary process have been investigated by Friedman [59], who considers the problem of searching a multivariable survival space. A comparison is made between the times required for random versus hill-climbing search techniques.

It is still too early to say whether there is any fundamental network difference between the evolutionary concept and simple calculation and storage of results based upon past experience. The interested reader is directed to Sperry [60] for an illuminating account of the role played by inheritance in specifying complex biological neural networks.

Conclusion

Network learning in the very simple case of single-layer, linear-summing elements with weighted inputs and nonlinear output characteristics has been discussed at some length. With the learning process restricted to changes in input weighting, it is clear that improved performance can be obtained by means of a number of learning criteria. Some of these, such as the minimum error rate (error-correcting), are more powerful than others since they can be guaranteed to reach the ultimate limitations of the element's logical properties.

These limitations are extremely severe, however, since the percentage of realizable logical functions becomes vanishingly small as the number of input variables increases. The chances of obtaining an arbitrarily specified response are correspondingly reduced. More sophisticated approaches must therefore be undertaken if networks are to be capable of handling the most general learning problems.

A number of alternatives are possible, such as input weighting according to the product of variables, or multiple-threshold decision elements. The most attractive, however, appears to be multiple-layer logical circuit arrangements, since it is known that any function can thereby be realized. Multistage realization of logical functions by means of fixed weight summation-logic elements can of course be derived. However, no general criteria on the basis of which intermediate logical layers can be taught functions required for over-all network realization of the desired input-output relationship have been discovered. While a number of workers have pointed out this basic problem, few inroads have been made upon it to date.

Somewhat the same problem is approached from the recognition network point of view, and the results of workers exploring the usefulness of various complex operations upon input pattern variables have been described. Although a number of interesting devices have been studied or observed, particularly in biological investigations, there exists no adequate measure of the utility of a given logical operation in terms of environmental properties and required network behavior.

Finally, the possibility exists that networks possessing feedback may be useful for the economic realization of complex logical functions. Understanding of the learning process in such networks, however, is still in a rudimentary state.

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The Simulation of Neural Elements by Electrical Networks Based on Multi-Aperture Magnetic Cores*

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Summary—**Multilevel storage, gating, controlling threshold-level, and summation are basic functional operations common to several systems for the simulation of neural behavior by electrical networks. It is shown how these may be realized very efficiently in terms of multi-apertured magnetic cores; in a typical example, only two cores of the type described by Crane are required for a circuit with threshold control of three simultaneous gates and non-destructive analog read-out. A logic element equivalent to a self-holding relay exhibits dc current gain and has compatible input-output connections.**

I. Introduction

IN THE many schemes that have been suggested for the simulation of neural elements by electrical networks,[1–4] the following characteristic electrical operations recur with considerable regularity and form the building blocks from which comprehensive simulations may be devised:

A. Multi-Level Storage

The strength of an output signal is to be dependent on the previous history of the neural element. In the simulation, this appears as a "weight" or "stored value." Since the weight is to receive increments and decrements at intervals throughout the period of operation of the system, it is desirable that readout should be nondestructive. In some systems, it is necessary to generate a signal level proportional to the product of two or more weights.

B. Gating Function

A signal may or may not be present, depending on the presence of controlling signals. This implies a relay, commonly a normally off, make-and-break relay, which closes when part of a system becomes "active," and, for example, allows a signal to be read out from a multilevel store.

C. A Controlling Threshold Level

A signal is gated either on or off, depending on whether the signal level at some point exceeds a controlling threshold level θ. The threshold may control several circuits simultaneously.

D. Summation

A set of signals is added together to form an input, which may, for example, be compared with a gating level θ.

One possible arrangement based on the work of Rosenblatt[1] is shown in Fig. 1. The inputs from the sensors S_1, S_2, S_3 · · · are summed to generate an input signal; $\sum S_1 \cdot \sum S_1$ is compared with the threshold θ; and if $\sum S_1 > \theta$, the three normally open make-and-break contacts are closed. The unit is said to be active. A signal level proportional to the stored weight, of value V, is read out from the analog store of the active unit and processed by subsequent logical elements in the system. On the basis of this processing, the analog store may receive either an increment or a decrement to its store; both possibilities are available since the threshold has been exceeded and the switches in the increment and decrement lines were closed at the time of read-out. It is required that inactive units are isolated from the active system and do not have their stored weights changed so long as they are inactive.

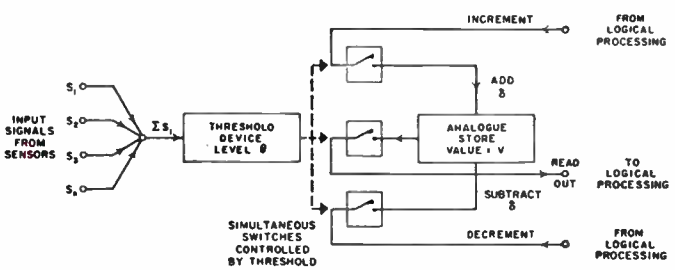

Fig. 1—Simulation circuit for neural element.

II. Analog Storage in Apertured Cores

The preliminary investigation of analog storage in apertured cores has been carried out using ferrite cores of the type described by Crane[5,6] (Fig. 2). The dimensions

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of the core are characterized by the fact that the cross-sectional area of A is equal to the sum of areas B and C, and also that B and C are equal. Thus, when A is saturated by winding a, both B and C are saturated also in either a clockwise or a counter-clockwise direction. However, if there is a winding b as shown, carrying a bias current, it is possible to hold the core material within the dotted circle saturated in a particular direction and to reverse some or all of the material outside it.

Since the material most easily switched is that with the shortest path length, assuming the core to be homogeneous, when the saturated core of Fig. 2 is partially switched, the flux distribution changes from that shown in Fig. 3(a) to the situation in Fig. 3(b).

If a high-frequency carrier is fed into a winding c in the side hole, and a second winding c' is put on the same leg (Fig. 2), a signal appears in c' which has a level proportional to the amount of flux which has been switched around the large aperture. Several cycles of carrier may be required before a reversible flux system is reached, since the initial situation shown in Fig. 3(b) is unstable and reverts to Fig. 3(c). Once this equilibrium condition is reached, in order to change the output signal level, it is necessary to switch some of the flux around the large aperture; flux trapped around the hole may therefore be sensed nondestructively with relatively high carrier drive without risk of degrading the stored level.

The extent to which the core is switched can be varied incrementally by the use of a very small core ("bucket"), shown in Fig. 4. However, it is essential that the switching should always occur at a constant reference phase with respect to the carrier drive unless this is removed, since the size of the increment depends on the vector sum of the switching pulse and the carrier. In the practical realization of Fig. 1, using two similar multi-aperture cores, the bucket core is, in fact, one of the side holes. Typical measurements are shown in Fig. 5.

III. Gate and Threshold Functions

The gate and threshold functions may be performed in a core of the same type as that used for analog storage. A typical configuration is Fig. 6. A winding a has a steady current passing through it which is greater than the minimum necessary to hold the main leg saturated.

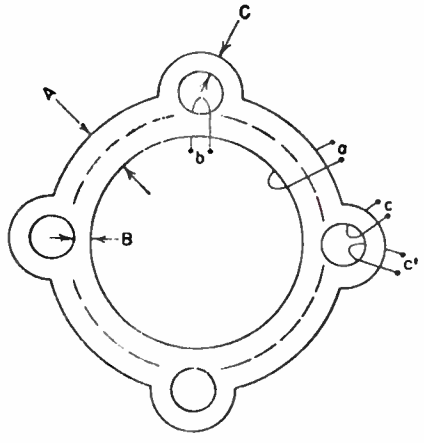

Fig. 2—Configuration of MAD ferrite core of Bennion and Crane.

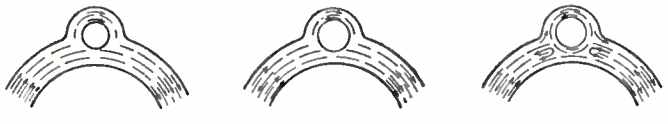

Fig. 3—Partial switching of flux around an aperture.

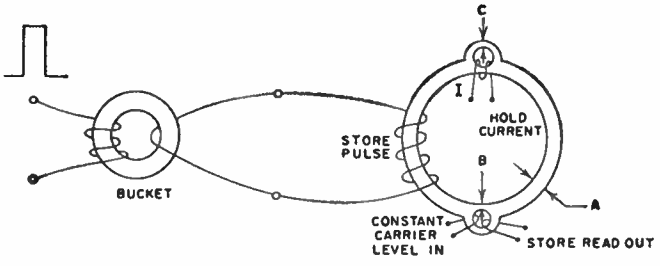

Fig. 4—Multi-aperture core used for analog storage.

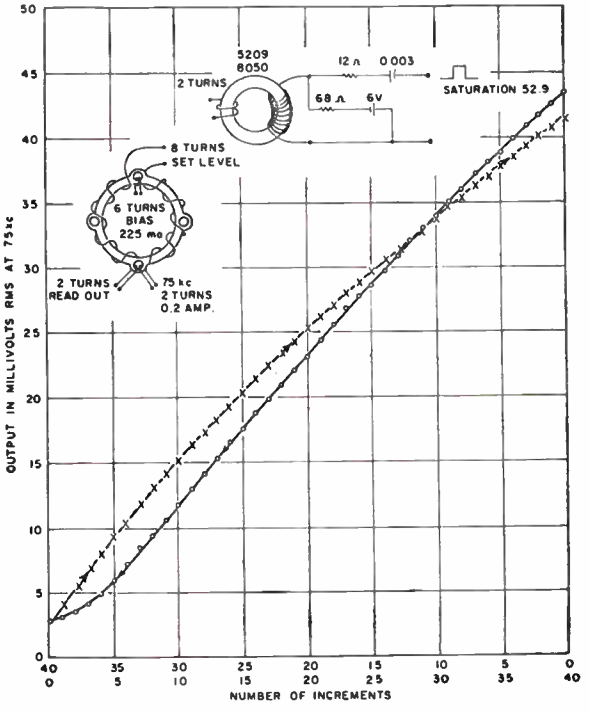

Fig. 5—Storage characteristic for multi-aperture core.

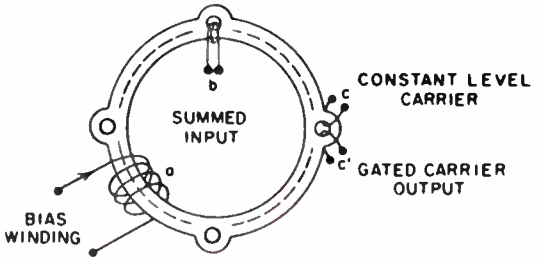

Fig. 6—Multi-aperture core used for gate and threshold functions.

There is also a winding *b* inside one of four similar side holes which receives the current due to the summation of inputs from the sensors. If the current in *b* is sufficiently large, it will be able to reverse the flux around the center hole within the dotted line shown, in opposition to the field provided by winding *a*. The winding *b* therefore behaves as a control winding for a switch, since windings such as *c* and *c'* are virtually uncoupled when both annuli of the core are magnetized in parallel, but tightly coupled if anti-parallel. The current in winding *a* provides the variable threshold control. The three available holes may be used for carrier switching and the increment and decrement control shown in Fig. 1. It happens that the small side holes are of a suitable magnitude to act as a "bucket" for the increments. An over-all characteristic through a gating core is shown in Fig. 7.

However, there is a practical difficulty associated with Fig. 6 which severely limits the application of this arrangement. The side holes are only 20 mil in diameter, and the drive required in winding *b* is of the order of two ampere turns, so that the choice typically lies between supplying one ampere into two turns of 33-gauge wire, or winding 10 turns of 40 gauge in a 20-mil hole and supplying 200 ma. Either way it is not a very attractive situation. Fortunately, there is a relatively simple way around this difficulty. The input winding, *b*, is replaced by a winding through the main aperture, which receives the controlling signal, plus a blocking winding on the inner leg of the side hole. The input winding may now consist of 200 turns of 38-gauge wire and is conveniently wound in the large central aperture by a standard toroid winder. The sense of the windings is opposed so that the gating characteristic takes the form of Fig. 8. The operating current is 10 ma. It is necessary to provide a holding current in the blocking winding to produce a flat top to the gate characteristic of sufficient width to meet the application. The arrangement of Fig. 6 permits the input signal to be increased arbitrarily, but in Fig. 8 the allowable range is approximately equal to the ampere turns in the blocking winding.

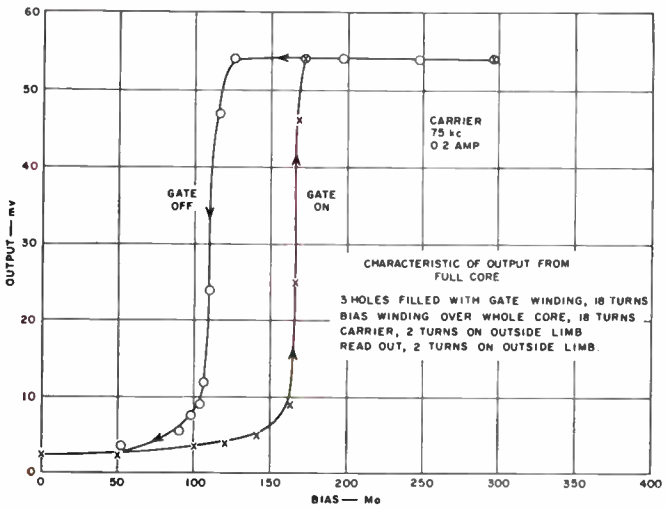

Fig. 7—Gating characteristic for multi-aperture core (simple arrangement).

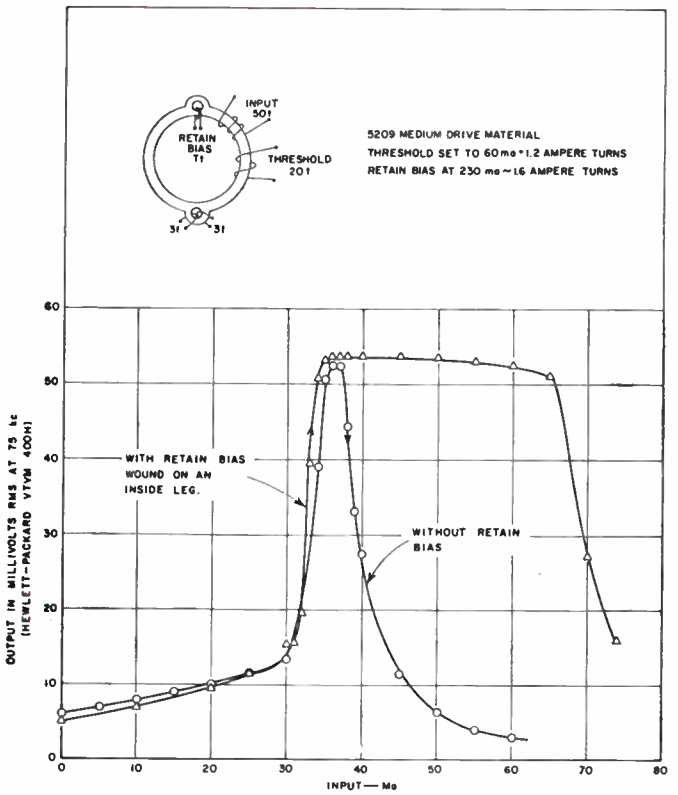

Fig. 8—Gating characteristic for multi-aperture core (modified arrangement).

IV. A Simulation Circuit for a Neural Element

Now that the individual functions of the simulation circuit have been achieved in terms of equivalent magnetic circuitry, it remains to combine them into a mutually compatible system. The completed circuit analogous to Fig. 1 is shown in Fig. 9, and makes use of two multi-aperture cores and wire only. It will be appreciated that the design of the flux transfer circuit between the gate and analog cores presents some difficulty, since the flux configuration in the analog core varies from fully saturated to 50 per cent reversed. In addition, the side hole which is acting as a bucket drives the analog core in series with its inoperative twin, while there is considerable back-coupling through the carrier loop as well. In the circumstances, it is perhaps remarkable that the arrangement can exhibit linearity of the quality

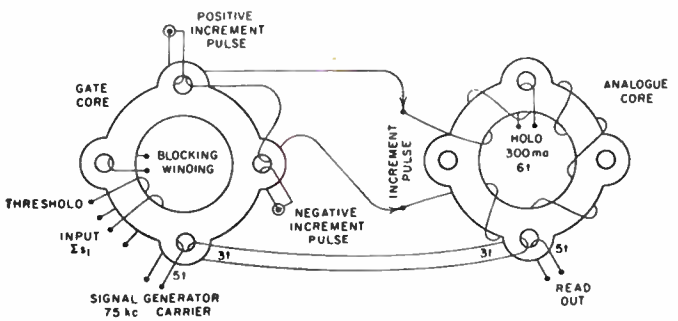

Fig. 9—Magnetic circuit equivalent to Fig. 1.

shown in Fig. 10; an attempt was made to equalize the increments over a greater range by the use of small resistors in series with the pulse generator. The ordinate is a measure of the mean signal level rather than the rms; this being a characteristic of the circuit of the vacuum tube voltmeter (Hewlett-Packard 400 H). If the simulation behavior demands that the output should increase more rapidly than linearly, a peak-reading circuit rather than an average-reading arrangement should be used. Multiplication of weights may be effected by use of the carrier output from one storage core as the drive for a second core, since both circuits are of low impedance and compatible.

V. A Logic Element

If has been found possible to extract more dc current from a winding through a minor aperture than is necessary to operate the control winding of the same gate core. Such an arrangement exhibits two stable states and corresponds in function to a self-holding relay; the remainder of the minor apertures are available for other functions if needed in the manner of independent relay contacts. The measured characteristics of the circuit shown in Fig. 11 are given in Fig. 12. If the carrier drive is gated, the circuit will reset to the off condition; a typical ratio for the steady currents in the two stable states is 20:1. It should be noted that the threshold current and the extent of the flat top are independently controllable, and in some applications the additional reset to zero at high currents may be employed to advantage.

Since this arrangement exhibits power gain and controlled switching states, and is compatible not only with itself but also with the gate and multilevel storage circuits, if forms an ideal coupling element for use in multilayer logic systems of neuron simulation.

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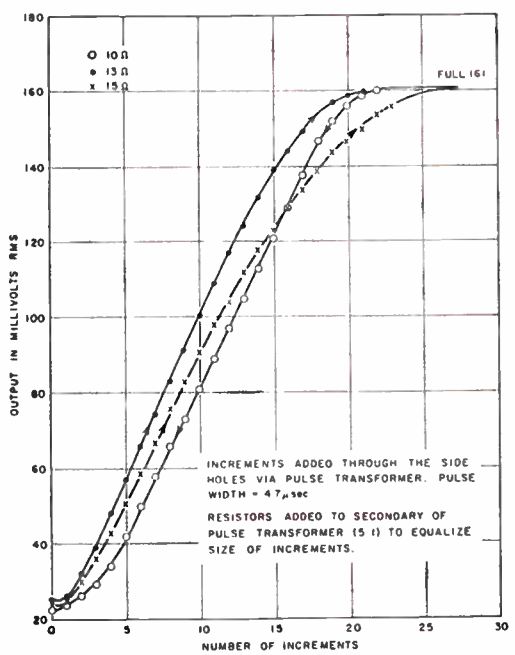

Fig. 10—Storage characteristic for neuron simulation circuit based on Fig. 9.

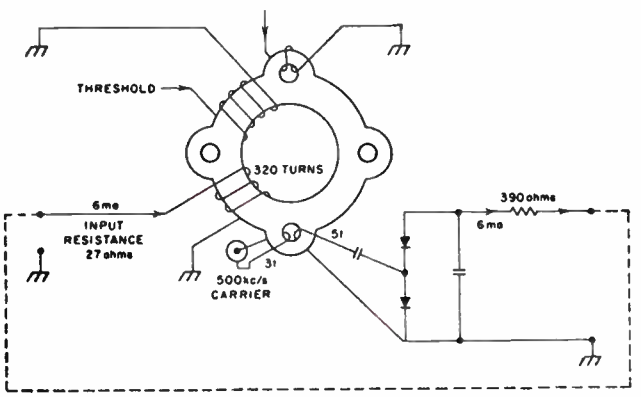

Fig. 11—A logic element with two stable dc states.

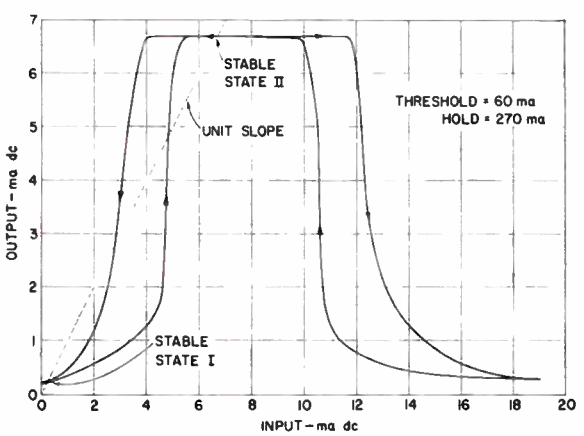

Fig. 12—Characteristic of the logic element shown in Fig. 11.

Developments in the Logical Organization of Computer Arithmetic and Control Units*

F. S. BECKMAN†, F. P. BROOKS, JR.‡, MEMBER, IRE, AND W. J. LAWLESS, JR.§

Considerable attention has been given to the organization of the arithmetic and control functions of computers. W. J. Lawless, Jr., and his associates have been requested to identify the major branches of the evolution of the mechanization of these functions since the first generation of computers, and to indicate current trends. The interested student of computers with a moderate understanding of computer terminology and functioning will find this a useful discourse, and the computer specialist should find it to be a helpful summary.
—The *Guest Editor*

I. Introduction

DURING the last seven years there has been a remarkable increase in the power and speed of the general purpose digital computer. The fastest digital computers that are now coming into use have, individually, more computational capability than the collective powers of all the approximately fifty large general purpose digital computers which were in use in the world at the end of 1953. Comparable improvements in machine reliability have been achieved.

There has been great progress in the development of memory and switching devices which function at ten or more times the speed of the older physical devices and clever schemes have been developed to increase the speed of the arithmetic operations for a given circuit speed. Considerable attention has been given in recent years to machine organization which permits the handling of concurrent operations. This simultaneous execution of processing operations takes several different forms. In addition to overlapping input-output operations and data processing operations, it is possible to overlap the execution of one instruction with the interpretation and obtaining of operands for succeeding instructions. In some modern computers the presence of more than one arithmetic unit and instruction register permits the parallel execution of several programs.

In this paper we shall not consider those characteristics of the physical devices used in a computer which influence the speed and the design of circuitry. Rather, we shall concern ourselves with the organization of the basic components into "packages" that perform the arithmetic and control functions and shall not deal with the "micro-level" of logical organization.

II. Addressing and Address Modification

A. Addressing Techniques

The conventional method of addressing words in a computer instruction is by use of the assigned unique numeric address.

Other addressing techniques [1] are:

Geometric Addressing: A few storage cells, for example, index or ALU registers, can each be addressed by a unique bit position in an instruction. This technique makes inefficient use of instruction bit positions, but sometimes is justified when multiple registers are used in a single instruction. (A related case is the use of a specific manual or automatic sense switch to address a register.)

Implicit Addressing: Storage cells may be addressed implicitly; *e.g.*, reading in or out of a memory unit is normally through a memory register. Thus, any instruction which includes reading in or out of a memory unit is implicitly addressing that unit's memory register.

In some computers certain registers are addressed both conventionally and implicitly. An ALU (arithmetic and logic unit) register may be addressable conventionally in certain instructions in a set and be addressed implicitly in other instructions in the same set. For example, in an "add" type instruction in the IBM-705[1] the sum is stored in one of several ALU registers according to the address specified. The product of a multiplication instruction is always stored in one specific register (or pair of registers), and thus the address is implied, not stated. The same cell might be addressed both conventionally and implicitly in one instruction.

Addressing by Content: A storage cell can be specified by its contents; *i.e.*, "the cell whose content is X" or "is closest to X" or "falls between X and Y," etc. This type of addressing usually requires a subroutine to locate the cell. Special instructions (*e.g.*, search and compare instructions in the RCA 301) are often provided to simplify these subroutines. Recently developed *associative* memories permit cells to be directly addressed by content.

Immediate Addressing: In several recent machines an actual operand can be stored in an instruction word, in lieu of the address for that operand. This is a special case of implicit addressing. The register that contains the instruction word at the time the instruction opera-

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† IBM Systems Res. Inst., New York, N. Y.
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[1] In the text when citing some computer manufacturers' machines, the manufacturer is referred to in abbreviated form; *e.g.*, IBM for International Business Machines, SR for Sperry Rand, MH for Minneapolis-Honeywell, etc.

tion code is interpreted is implicitly addressed for part of its contents. The operand in the instruction word is available "immediately" rather than after a memory reference.

Direct and Indirect Addressing: In a computer instruction a *direct address* is the address of a cell containing an operand; an *indirect address* is the address of a cell containing the address of an operand. The second address might also be indirect so that the process can continue through an essentially unlimited number of indirect addresses before arriving at a direct address.

Indirect addressing has many uses. An important one is to reduce data transmission in internal memory. In sorting, for example, short records can be generated which contain the *key* plus the address in memory of the corresponding long record. The short records are sorted into sequence in memory and are then referred to sequentially by indirect addressing to write out the long records in sequence on tape.

Indirect addressing may also be used in lieu of index registers for address modification. The indirect address in an instruction is to a cell which contains the modified address. Instruction modification routines perform the necessary arithmetic on the pseudo-index register.

This approach, although considerably less elegant than index registers and special index adders, is simpler to use than the routines necessary when neither indexing nor indirect addressing is provided.

Abbreviated or Truncated Addressing: Some cells are addressed partly implicitly, partly conventionally [2]. An operation code may imply that an address in the instruction refers to one of a limited number of cells. An abbreviated address specifies which cell. An abbreviated operand address can be incremented by an unabbreviated index value to obtain the unabbreviated *effective* address.

Abbreviated addressing is useful primarily as a means of packing more content into an instruction word. A special case of abbreviated addressing is used in the RCA 601. Some operand addresses can be specified by a character in the instruction which designates one of several ALU registers presently containing the operand address. This technique is used to take advantage of situations in which one of the operand addresses was used in the previous operation and still sits in the ALU register. It should be noted that this is also a special case of indirect addressing.

Relative Addressing: A cell may be addressed by stating its location relative to another address; *e.g.*, by stating the interval from some established base address. This, of course, implies an address modification to arrive at the effective address. Relative addressing has been used in several machines to save instruction bits or to simplify program relocation. In the CDC-160, for example, a combination of relative and indirect addressing has been used to reduce substantially the instruction size. The operand address in the instruction is stated as ± 0 to 63 relative to the *present* instruction address, or it may be any memory location by indirect addressing.

B. Addressing Systems

General: The various single, double, triple, etc., addressing systems used in early computers have been perpetuated and extended in recent machines. The most common extension has been provision for addressing one or more of a limited number of index registers in addition to the basic addressing system.

In all of these systems it must be kept in mind that specific instructions in a set may use the address fields unconventionally, *e.g.*, to specify the number of shifts in a shift instruction, or the location of the next instruction in a transfer instruction, or an immediate address.

Single address systems provide one basic address field in an instruction, normally the address of one operand. Typical variations are an additional index register address or provision for one or more additional abbreviated auxiliary accumulator addresses as in the Sperry Rand LARC [34] and the Soviet LEM 1 [3]. This latter feature converts single address systems to limited two or more address systems.

Multiple address systems provide more than one full address field in an instruction. The use of the multiple address fields may vary within one instruction set. In two-address machines, the two addresses may specify the two operand addresses required in most arithmetic operations. Many machines use the second address to specify the location of the next instruction.

A conventional three-address system provides for two operand addresses and the address for storing the result, or the next instruction. The four-address system provides for two operand addresses, a result address, and next instruction address. Because so many instructions in a set do not require four addresses, the few four-address computers (*e.g.*, SEAC) provide many variations to the basic format.

Variable address systems have been used in some recent computers since it is obvious that no fixed address system is optimum. These machines provide some degree of variability in the number of addresses that can be specified in one instruction. In some cases, this variability is provided within a fixed length instruction. In others, the instruction length varies, sometimes in a very limited fashion, sometimes with few restraints.

Variable instruction length obviously introduces design complications, especially in parallel machines. One relatively uncomplicated technique is to vary between one and two instructions per fixed size memory word. The full word instruction provides additional control data including, usually, address fields.

Variable addressing from no addresses to two or three addresses is perhaps the next stage in flexibility, *e.g.*, the IBM 1401. This permits the programming and execution time economies of multiple operand instructions where needed, while retaining the memory storage space economy of no-address and one-address instructions where appropriate.

Such variable length instruction systems are relatively less complicated in serial machines as compared to parallel large-word machines.

Obviously, the most flexible addressing system provides unlimited variability in the number of addresses contained in an instruction. Both the RCA 601 and the Bull Gamma 60 [4] permit any number of addresses in an instruction. This is accomplished in both machines by chaining as many fixed length words together as needed to provide the variable length instruction.

In the Gamma 60, the considerable variability in instruction length is required by the organization of the machine. Instructions set up the several independent ALU's, which then operate essentially autonomously until the tasks set up are completed. The different ALU's use varying amounts of set-up data.

This listing by no means exhausts the possible addressing systems, or even the special deviations from conventional systems. For example, some thought has been given to entirely relative addressing; *i.e.*, storage cells not assigned any permanent address. Instead any available cell is arbitrarily established as a base and all other cells in an available block of cells in memory are designated relative to that base for a given program. Other programs could work independently in another available block of cells. This would, theoretically, eliminate certain assembly and memory location assignment problems; but would certainly introduce numerous other problems, including a major one of design.

Address Modification: Certainly the most important single advance in the development of computers was the concept, credited primarily to John von Neumann [6], of operating upon instructions as data to perform address modification.

Address modification permits different data to be operated upon with the same sequence of instructions. In all early computers, and many present-day computers, data address modification was accomplished entirely by programming; no special hardware was provided to simplify or expedite the process. Since the invention of the "B-tube" in the 1949 Manchester Computer [7], increasingly elaborate hardware systems have been developed to facilitate address modification [1].

Address modification can be considered in two parts: 1) modifying an address by adding (or subtracting) an index value to an address; 2) modifying the index value, testing to determine if the required number of index value modifications have been completed, and similar bookkeeping functions on the indexing operation—all often called "index arithmetic." Hardware has been added to facilitate each in different machines.

The primary aid to incrementing the address has been automatic incrementing (without additional instructions) using special adders. In some cases, no special adder is provided but incrementing is done automatically using the main ALU adder. In either case, designers normally attempt to overlap the process as much as possible with other processes in the basic machine cycle.

There is a great deal of variation in the manner of accomplishing index arithmetic in computers. The *minimum* built-in hardware consists of one or more index registers for storing index values. When called for in an instruction, the index register value is added to the specified address field in the instruction to arrive at the effective address. All modifications of the index values and testing for terminating the process are accomplished by normal programmed operations.

Since the index arithmetic operations should be quite independent of the use of the index values in modifying addresses, it is essentially necessary that at least one programmed operation be involved in index arithmetic. The instruction set frequently includes at least one special index arithmetic instruction. If the instruction word is large enough, the instruction might be to increment the index value in a specified index register by the increment value contained in the instruction word, test the resultant index value for zero or negative value, and transfer to an address also contained in the instruction if the test is not met. Two instructions are more common: an increment instruction, and a test and transfer instruction.

The increment to the index value need not be in the instruction word. It could be in a storage cell addressed by the instruction, or it might be in the index register together with the index value. This latter technique requires more hardware but may be a more general solution. Ideally, all storage registers should be accessible fast enough so that any storage cell could be used as an index register. In some machines (*e.g.*, Pegasus [8]), a small set of registers may be used as arithmetic, index or storage registers. In other machines (*e.g.*, IBM STRETCH), any memory register may be used as an index register (in addition to any special index registers), *but* an extra memory access is required.

In addition to tests for a zero or negative index value, limits and counts have been used for determining when to terminate an indexing loop. In the limit test, a limit value is compared with the index value after it has been incremented. Actually the zero test is a limit test with a fixed, implied limit. In testing by counting, a variable is reduced by one and tested for zero (or a limit).

Counting has the advantage of making the termination point completely independent of the index value. In particular, it is possible to keep an index value constant. Both the limit test and counting require storing an additional value, either in the instruction word, the index register or general storage.

One additional step necessary in index arithmetic is setting up or "initializing" the index register with initial values prior to use and re-initializing for each reuse. Normally this is handled by routine programming.

Multiple Indexing: An obvious extension of indexing is called "multiple indexing," *i.e.*, adding more than one index value to the base operand address. Multiple indexing is especially useful in multicoordinate systems where it is necessary to maintain two or more separate indices in computing the location of operands in an array.

The process can be facilitated by built-in hardware, but is normally programmed. In STRETCH, a special instruction permits specifying multiple index registers, whose index values are automatically added together

and stored as the index value of another index register.

Computing of operand addresses is a significant computing task, one that has not been provided for properly in comparison with its importance in most machines. There are at least four activities in computers where relatively independent computing is required: 1) basic operational computing as conventionally supplied by an ALU; 2) input-output control computing, as provided by the input-output processor in the LARC, for example; 3) instruction sequencing; and 4) operand addressing and address modification. There might well be some advantages in generality in a computer design which provided general purpose computing capability, under program control, for each of these four activities.

Addresses Formed by Data: A very important addressing (and address modification) technique is that of forming an address or, more often, the index value to a base address, from data itself. That is, the bits that represent some unit of data are added to a base address to arrive at an effective address. The base address would be to the general location of a table in memory; the data index value would locate the specific entry in the table.

The use of data for table-lookup is obviously useful in any input or output code conversion process. Tables may also be used for editing, "looking-up" rather than executing arithmetic processes, and a variety of logical and statistical operations.

Until recently, few computers made any provision for simplifying forming addresses from data. In fact, address registers were frequently not addressable. In some recent machines, provisions for table-lookups of varying degrees of complexity have been made. The IBM HARVEST Computer [9] has probably the most elaborate and powerful table-lookup capability built to date. It provides a direct path, through a separate indexing unit to memory address registers. In addition, it provides for automatic multiple table-lookups; *i.e.*, the data found in one table-lookup is used as a partial address, usually together with a new data unit, to a second table, etc. Multiple table-lookup is an extremely powerful logical tool which permits such complex transformations as binary to decimal, etc., with a minimum of instructions.

III. Sequencing and Control

A. Specification of Instruction Sequences

Normal Sequencing: Early computers specified the normal succession of instructions by a counter, as in the IAS [6] computer or the SR UNIVAC I [10], or by the physical adjacency of the next instruction on a self-indexing tape, as in the Harvard Mark I [11] or the IBM SSEC [12]. The instruction counter method of sequencing is most widely used on modern machines. Some computers with serial storage have used one of the addresses in the instruction to specify the location of the next instruction, as in the 3+1 address instruction on the SEAC [13] or the 1+1 address instruction of the IBM 650 [14] and the SR Solid State 80.

Branching: Decision operations, classically performed by conditionally altering the instruction counter, have been elaborated to include a wide variety of tests and alternative conditions, which have been described and classified by Stevens [15]. A few developments are noteworthy.

One has been the use of implied addresses, both relative, as in the IBM 704 Compare Accumulator and Storage operation, and absolute, as in the RCA BIZMAC Verify with Rollback operation, or the SR UNIVAC Scientific 1103A Repeat operation. This has become necessary as programming experience has shown the desirability of more complex decision operations whose addresses did not suffice to specify all operands, or whose execution has required the instruction counter hardware.

Another development has been the systematization of decision operations in STRETCH where all machine conditions that can be tested are collected together in a single addressable indicator register and an instruction for testing and resetting these is provided.

A particularly powerful development is the combination of branching instructions and a general instruction repeating facility introduced in the SR UNIVAC SCIENTIFIC and widely imitated. Iterated branching is also incorporated in the IBM 650 Table Look-up operation to serve the same function in a somewhat more complex and rigid way.

Upon branching to a closed subroutine, one must store the instruction counter contents, or an equivalent, for use in the return branch. Classically, brute force programming techniques related to the original Wheeler linkage [16] have been used. The frequency of this operation has led to the development of a variety of mechanizations. The most straightforward of these is a counter-storing operation, as the return jump in the Royal-McBee LGP-30 [17]. This stores the counter contents, plus an appropriate constant, in the addressed location. A pathfinder register, as in the Los Alamos MANIAC II, automatically retains the value of the counter as it was immediately before the last branch. This is useful in program debugging as well as in subroutine work. The Harvard Mark IV [18] incorporates a more elaborate version of the pathfinder, which can store the most recent four locations branched to. Perhaps the most useful development has been the concept of storing the appropriately modified counter contents in an index register, as in the IBM 704. The index value can be used not only to modify the return branch address, but also to modify all addresses that refer to the calling sequence for operands, etc.

A particularly interesting development has been the use of multiple instruction counters, so that subroutines, etc., could be executed without changing the original counter. This development was foreshadowed in the Harvard Mark I, which has four paper tapes and ten relay subsequence units among which control can be switched. The use of subsequence counters was introduced in the Datamatic 1000. Both the MH 800 [19] and the Lincoln Labs TX-2 [20] go a step beyond

and include a multiplicity of similar and coordinate instruction counters.

Interruption: Three trends have stimulated the development of program interruption systems. First has been the drive toward greater efficiency, which has made undesirable the use of conditional branching for testing very rare events (such as overflow). Second has been the trend toward real-time operation, which necessitates immediate response to external signals which may be infrequent and arbitrarily timed. The third is the increasing independence of I/O (Input/Output) operations, whose completions or difficulties are infrequent and arbitrarily timed relative to internal operations, and must be signaled to the main program.

Program interruption is a general technique in which sequence changes are specified in advance of, and effected immediately upon the occurrence of, one or more exceptional conditions, which are monitored continuously. The UNIVAC I contains a rudimentary form of interruption in which occurrence of overflow causes a pair of instructions to be taken from a fixed location. A similar facility in the IBM 650 can only be actuated by failure of mechanical checks. In the Datamatic 1000, a variety of conditions can each cause automatic entry into an appropriate subsequence. The UNIVAC SCIENTIFIC 1103A seems to have been the first machine to incorporate an interruption system which would respond to external signals [21].

Interruption techniques have developed rapidly, and more recent computers have systems which are more universal in type of condition monitored, and more flexible in the way in which sequence changes and conditions can be prespecified. In the TX 2, for example, the programmer of any sequence specifies when a higher-priority sequence may interrupt and when program control should descend to a lower-priority sequence. Each condition causes actuation of a separate instruction counter. In STRETCH, a mask register permits the programmer to select specifically that set of conditions for which interruption is permitted [22]. Each condition causes a branch to a unique address, which is itself relative to a program-set interruption base address. Priorities can thus be very generally specified.

Execute: In a variety of circumstances it is convenient to execute a single instruction detached from its normal sequence. The execute operations developed for several recent computers permit this by addressing an instruction which is brought into the decoding circuits without the counter being changed. The successor instruction is thus normally that of the execute instruction rather than that of the object instruction. In effect, an execute operation calls a one-instruction subroutine and specifies an immediate return to the main routine. This is closely akin to indirect addressing, except that the whole instruction, not just the address, is selected from the specified location.

In the IBM 709 the execute operation facilitates modification of instructions which permit neither indexing nor indirect addressing, such as those for input-output. In the Soviet LEM 1 [5], programs are normally executed directly from a large read-only storage, and the execute operation permits isolated instructions to be placed in the small data store, where they can be modified.

In STRETCH execute operation, two further developments facilitate monitor programs [23]. During execution of the object instruction, neither branching nor program interruption is permitted. An attempted branch is suppressed and a particular interruption indicator is set. Thus, an object program cannot seize control from the monitor. A second execute operation specifies a pseudo-instruction counter, which in turn specifies the object instruction. The pseudo-instruction counter is automatically incremented according to the length of the object instruction.

B. Control of Instruction Execution

Operation Phase Control: The classical synchronous techniques for sequencing the phases of an operation use a latch ring or counter-decoder for distributing a sequence of timed pulses from an oscillator or other clock along appropriate gating lines. These techniques are still very widely used.

As old, and also widely used today, are the asynchronous techniques by which the completion of each operation phase causes generation of a pulse which initiates the next phase. In a widely-used variant of asynchronous technique, each operation is independently timed, and each signals the initiation of the next.

The most important trend in conventional operation phasing has been the increase in complexity of operations. In early computers, the most complex operation was usually divide, and it was composed of iterated short cycles of elementary steps. In contrast, modern computers abound with such operations as floating-point add, edit for print, table look-up, and repeat, each of which requires many steps, often all different.

Microprogramming: A principal innovation in the control of operation execution has been *microprogramming*, in which gating is directly controlled by programmer-set-up bits [24]. In pure *horizontal* microprogramming, each bit in the instruction format directly controls a gate or set of gates in the data path. (The bits may be scanned sequentially.) In *vertical* microprogramming, each operation phase and all gating involved in it is specified (perhaps in coded form) by a separate instruction.

Pure horizontal microprogramming suffers from low information density in instructions, since only a small fraction of all gating combinations are meaningful. This is sometimes remedied, at the expense of performance, by using ordinary operation codes in each instruction and deriving the fully expanded operation designation by table look-up upon execution. Clearly, a small fast memory is quite helpful here, and since it need not be written into, read-only memories have been used for this purpose.

Similarly, instruction density in vertical microprogramming can be improved by using macro operations

in programs and decoding them into sequences of micro operations upon execution. A small, fast, and cheaper read-only memory is also advantageously used here in, for example, Ferranti's ATLAS.

Microprogramming offers two advantages and has been sometimes used for one, and sometimes for the other. When memory components are relatively cheap and logical components relatively dear, microprogramming often affords cheaper control than conventional techniques. Microprogramming also permits the user to adjust his instruction repertoire to suit the problem. This flexibility is of less importance when computers are mass-produced and programs widely shared, but even then it permits designer's oversights to be readily remedied.

C. Time-Sharing and Concurrent Operation

Concepts: When units which work together are widely disparate in speed, so that the faster must often be idle while waiting for the slower, efficiency can be increased by *time-sharing* the faster unit among several slower ones, which operate *concurrently*. Time-sharing and concurrency are thus the two sides of the same coin.

Probably no trend has so affected recent computer development as the trend to greater concurrency. Early computers generally did one thing at a time, for this is the arrangement that minimizes total equipment, even if at the expense of efficiency. As work loads and willingness to invest have increased, however, ever greater concurrency has been used.

Speed disparities and consequent opportunity for concurrency have been exploited on several levels in computer systems. Fast computing systems are time-shared among slow I/O devices; and fast elements within a processor are time-shared among slow ones.

Concurrent operation of I/O devices is almost universal today. Consideration of the developments in techniques will be deferred until a later section, but it should be remarked that the method selected for control of I/O concurrency often has been extended to other areas of concurrent operation.

Intra-processor Concurrency: Many contemporary computers are of conventional organization. All others, however, embody one form or another of concurrency among the elements of the processor itself. In the NBS Pilot [25] for example, a separate stored-program-controlled element does address modification for and concurrently with the main arithmetic processor. The SR LARC [34] provides two computing units and an I/O processor unit sharing a common memory. The Bull Gamma 60 [4] carries this concept further, with a sizeable number of independent processing units sharing a common memory. Each executes instructions as specified by its queue.

This kind of processing concurrency, in which several units are at once at work on instructions of many sequences, has been called horizontal concurrency. It is distinguished from vertical concurrency in which several units operate in assembly-line fashion upon the successive instructions of a single sequence. This mode of operation has been carried to a high degree of development in STRETCH, where an index arithmetic unit, a four-level instruction lookahead, and a main processor may be simultaneously in the various stages of executing up to six instructions [26]. This is possible because the fast processing units can service many concurrently operating memory boxes.

Inter-computer Concurrency and Coupling: Some of the larger systems incorporate multiple similar processors which operate concurrently on a common problem. The problems of computer coupling were explored by Leiner and others at NBS, and the NBS DYSEAC [28] was designed to be used coupled with the SEAC for such experiments. The principal problems are the interlocking of shared memories, signaling a desired action (usually solved by interruption), and the maintenance of synchronization.

The Thompson Ramo Wooldridge 400 system permits a number of conventionally organized computers to be variously linked with each other and with I/O buffer memories. A cross-bar switching system under program control from one of the computers is used to establish the necessary connections.

Multiprogramming: A most significant recent development is the technique of multiprogramming by which a fast computer is shared among slow users or slow I/O devices, each of which has a different program. This technique is important because I/O times are often relatively quite long, so that input for one problem must be overlapped with calculation on a second and output on a third. The greatest promise of multiprogramming lies not in more efficient I/O operation, but rather in permitting closer collaboration of user and machine.

As computers have gotten faster, the higher cost of idle seconds has forced the user into a more and more remote relationship with the computer. The intimate familiarity with intermediate results that so aided the user of a desk calculator is long gone, but the problems essayed today are more, not less, complex and may be less well understood by the sponsor. The results of this separation of user and machine are more unnecessary printing of voluminous memory dumps and voluminous worthless results, more lengthy calculation whose uselessness would have been obvious to an observer from the first, and lengthier program and mathematical model debugging, because of the enforced infrequency of debugging attempts.

Multiprogramming promises to permit the user to halt his problem at will without idling an expensive machine. When this economic breakthrough is achieved, the advantages of closer man-machine coupling can easily be derived.

The implications of multiprogramming for computer organization are relatively few. The required hardware elements seem to be: 1) a program interruption system, 2) a program-controlled memory or address protection system, 3) a multiplicity of displays, consoles, or inquiry stations for direct man-computer interaction, and 4) adequate memory for one program and a supervisory routine and a high-data-rate, few-millisecond-access,

external storage for the programs whose executions are interlaced. Provision for automatic relocation of programs is extremely desirable, if not mandatory. Multiprogramming is being attempted on computers such as the IBM 7090 and the SR 1103A (which have only one or two of the facilities listed above) [29]. STRETCH contains the first four facilities, and appears to be well-suited to multiprogramming, but no experience has yet been accumulated.

The principal problems in multiprogramming lie in the construction of adequate supervisory routines. Development of such programs is being pursued by several groups [30], [31].

IV. Arithmetic and Logical Operations

A. General Considerations

In recent years, the order codes for the large digital computers have been considerably expanded. The repertoire of operations for the new machines is often six or more times as long as the instruction lists for the first large digital computers. These are sometimes used with certain "modifiers" appearing in the instruction word giving thousands of different combinations resulting in different operations. To a large extent these expanded order lists reflect the desire on the part of the professional programmer for additional conveniences in the order code. With the greatly expanded use of automatic programming facilities, however, many of the users of modern computers never become familiar with the entire machine order code list. Their knowledge of programming languages is frequently confined to the "source language" of problem oriented programming systems. It is usually the programmer who works on the preparation of large automatic programming systems or on frequently recurring applications programmed in machine language who benefits most from these increased facilities of the machine order code.

There has been considerable emphasis placed in recent years on the development of such automatic programming systems for scientific and commercial data processing. Therefore, the inclusion of instructions to permit more efficient compilers is often considered in designing the order code. For this purpose alone, field manipulation and other data processing abilities are desirable in a computer designed primarily for scientific work—although no extensive commercial data processing applications may be performed on the machine.

Arithmetic and logical instructions have been added in order to

1) Facilitate data manipulation and input-output conversion in binary machines,
2) Permit the more efficient handling of double precision arithmetic operations,
3) Facilitate logical decisions based upon information received from external units, and
4) Provide automatic floating point operations.

Built-in floating point arithmetic operations have become standard features on all the large scientific computers and on many of the smaller machines. The Boolean operations which are usually available in large binary computers are used principally for field manipulation and the making of logical decisions. The fastest machine available today is perhaps several hundred times as fast as its predecessor of seven years ago. This increase in speed is explained both by faster hardware and improved design. The use of concurrent operations is responsible for some of this improvement and the application of considerable ingenuity has resulted in some significant savings in the execution time of the arithmetic operations.

As faster computers have become available, word length has in general increased in the larger machines. This is reasonable because the faster machines, when used for scientific calculations, are used often in solving bigger problems and, when these are mathematical, a larger growth of round-off error is, in general, to be expected in the course of these more extended calculations. Thus, more precision and a larger word size for operands are required. Another reason for larger words in the bigger and faster computers is that the larger size of high speed storage requires a bigger address field in the instruction word format. A somewhat bigger operation field may also be needed to represent a larger set of operation codes.

No precise relationship between the word length and speed of a computer seems to be possible. However, for one class of scientific problems, namely those in which the round-off error behaves as it does during matrix inversion, we can apply some heuristic reasoning to derive a relationship between speed and word length which seems to be plausible. Von Neumann and Goldstine [35] have shown that one can expect to be able to obtain the inverse of a matrix (*i.e.*, a better, in some sense, approximation to the inverse than the identity matrix) of order n using a computer with radix β and word length s if $n < 0.04\,\beta^{s/3}$. Since the order of a matrix that can be inverted on a given machine in a given time interval will vary approximately with the cube root of the "speed" (suitably defined) of the machine, it seems reasonable to infer that the word length should vary logarithmically with the speed (S) in accordance with the following relationships: $s = \text{constant} + \log_\beta S$. The experience of some large computing centers seems to indicate that this relationship, although based on matrix inversion alone, is a reasonable one. It would imply that the fastest digital computers of the present, which are 200 or more times as fast as their predecessors of 1953, should properly have word lengths in excess of those of the earlier machines by at least eight binary bits or a little more than two decimal digits (assuming that the earlier machines were "well balanced" with respect to speed and word length). Another reason for larger words in the bigger and faster computers is that the larger size of high-speed storage requires a bigger address field in the instruction word format. A somewhat bigger operational field may also be needed to represent a larger set of operation codes.

An opposite trend has appeared in a few smaller machines. Higher component speeds have permitted

word sizes in the order of 20 bits to be utilized with programmed subroutines used to handle larger data words.

The basic operation facilities in binary and decimal machines are usually the same. While floating point operations are sometimes omitted from the repertoire of instructions in decimal computers, they appear in the order list of most new binary computers. Differences appear, however, in those instructions which are useful in a binary machine for performing input-output editing. In some cases special instructions have been provided to facilitate the conversion between binary and decimal information. Also, it is natural to include in a binary machine the ability to perform Boolean operations. In these cases the binary bits may be thought of as independent true-false indications.

B. *Arithmetic Operations*

Most of the early work in the logical design of the arithmetic operations, as well as many of the other functions of a digital computer, was reported by Burks, Goldstine and von Neumann in their 1946 report on "The Logical Design of an Electronic Computing Instument" [6]. The fundamental ideas for the execution of the arithmetic operations appeared in this work. In recent years, some clever artifices have been devised to cause a substantial speed-up of arithmetic operations. For example, the ratio between fixed point multiplication and addition time in some modern computers is substantially less than in the earlier machines. Floating point addition time has always been significant by comparison to floating point multiplication time and it is no longer as meaningful to tally only the number of multications in a computational procedure in order to assess its length. For the sake of simplicity, we shall assume in what follows that the computer being discussed is a binary machine. The same principles will also usually apply to a decimal machine, where binary encoding is used.

The most serious deterrent in speeding up the process of addition in a computer is the time that is required for the propagation of carries. In their 1946 report, Goldstine and von Neumann proved that the expected value of the length of a carry sequence in the addition of two n-bit numbers does not exceed $\log_2 n$. More precisely, the expected length of a carry sequence in the addition of forty bit words is 4.6 (rather than $\log_2 40$) [36]. However, the schemes used for addition in the early computers involved waiting a fixed length of time for each addition to make sure that the carries had all been propagated to the end of the "carry chains." This meant that this time interval had to be long enough to permit the propagation of a chain of as many as forty carries, for forty bit operands, even though the probability of this happening is extremely small. Today, circuits are sometimes designed so that a signal terminates the addition operation when all the carries have been completed [37]. This means that the average length of an addition time need only provide for, in the case of forty bit words, 4.6 carries, rather than the possible maximum of forty. Actually, the implementation of this scheme involves "no-carry sequences" as well, increasing the expected length to 5.6 carries. This technique is only possible of course on a machine that takes advantage of variable length operation times.

The increase in addition speed also, of course, improves multiplication time because multiplication on digital computers is usually accomplished by performing a series of additions. Partial products are formed using the successive digits of the multiplier and the total of these is obtained to give the product. Devices have been contrived to improve further the multiplication speed. In some machines [38] the digits of the multiplier are taken in pairs or even larger groups for the formation of the partial products.

An especially fruitful idea in multiplication is due apparently to several authors [39], [40], [41], [42], and is based on the fact that a binary number consisting of a string of ones can be written in a much more compact form; that is

$$\sum_{i=0}^{n} 2^i = 2^{n+1} - 1.$$

If we assume that binary notation is generalized so as to permit the use of negative digits defined in the obvious way—then we see that any complete string of consecutive ones in a binary integer can be replaced by a plus one in the first position preceding the string and a minus one in the last or least significant position in the string. We may, by doing this, lengthen other strings in the representation of the binary number. We assume that the process is continued until the original number contains only strings of zeros and isolated plus ones and minus ones in its representation. It is easily seen that this rewriting of the binary number must result in one that does not have more nonzero digits and will, in general, have substantially fewer nonzero digits. Since the usual method of multiplication involves the formation of a partial product for every nonzero digit in the multiplier, it is seen that this process will be shortened if the multiplier is so transformed. We assume here that the subtractions which are necessary to handle the negative ones in the representation of the multiplier can be as easily accomplished as the additions. The average saving in the number of additions (or subtractions) which have to be performed during a multiplication by using this technique, has been computed to be more than 17 per cent, and the average number of shifts required during multiplication is reduced by 30 per cent. An algorithm for multiplication can be defined which is based upon this equivalent representation for the multiplier but does not actually require that the multiplier first be so transformed [42].

Another device which has recently been widely used to decrease multiplication time is one which is independent of the method just described, and which therefore can be used in conjunction with it. This consists of using a separate accumulating register during multiplication to "save the carries." The use of this register makes it

unnecessary to wait for the carries to "ripple" through the word during the accumulation of every partial sum. In the normal addition process, two corresponding bits in the two summands are added to the carry resulting from the addition of the preceding pair of bits. The result then consists of a sum bit and a carry bit which is added to the next pair of bits in the summands as we proceed from right to left. The Boolean operations which produce the two outputs (the sum bit and the carry-out bit) from the three inputs (the two summand bits and the carry-in bit) are well known and form the basis of operation of most adders. Note that in this operation the origin of one of the inputs as a carry bit is not relevant to the process and the procedure can be applied to any three independent bits. The additional "carry save" register is used to take advantage of this fact. When the first two partial sums are added during the multiplication process, the result appears in two registers in "unassimilated" form; *i.e.*, the sum digit for each pair of corresponding digits appears in one register and the carry digit appears in the corresponding position in another. When the next number in the continuing sum leading to the product is added, two corresponding digits in the "sum" register and addend are added to the corresponding carry digit in the "carry save" register to produce, again, two results. After all partial products have been accumulated in this manner, the two "unassimilated" results (in the sum register and "carry save" register) are combined to produce the sum in its normal form [43], [44], [45]. An additional refinement in this method has been developed [44] to simplify the "assimilation" at the last step of the multiplication process.

In a serial computer other devices may be used. In the decimal machine, IBM NORC [46], the multiplicand flows from a register into a "product generator" which provides simultaneously the nine multiples of this operand. These multiples are conducted to a set of selector switches. The setting of each of these corresponds to a digit of the multiplier. Through these switches the appropriate multiples are added, properly shifted by means of a set of adder boxes and a delay unit. In this machine, multiplication time is only twice the addition time.

Another approach used in reducing the number of carries in addition has been described [47]. This method is based on the feasibility of simplifying substantially the Boolean equations which describe the digits in the four bit sum and carry resulting from the addition of two four bit numbers and a carry. The Boolean expressions for the sum bits of binary numbers of any length can of course always be written, but the implementation of this logical expression in hardware will be intolerably unwieldy for numbers with many bits. It is still economical for four bit numbers and thus, by performing an addition so that groups of four bits are handled at each step, a four fold reduction in addition time will result over the maximum ripple carry adder. An adder that functions in this manner is sometimes called a "carry propagate" or "carry detect" adder.

Division time has also been substantially improved over the "non restoring" division technique described by Burks, Goldstine, and von Neumann [6]. A general class of methods applicable to computers of arbitrary radix has been described by J. E. Robertson [48]. These methods make use of certain multiples of the divisor which are assumed to be available during the division process and are best suited for use in digital computers with facilities for floating point arithmetic.

Stored table-lookup procedures have also been used in some "intermediate" class computers. The use of a stored addition table has been described by Maclean and Aspinall [49]. In the IBM 1620 a stored table is used to obtain the product of two decimal digits during the multiplication process.

Some other clever schemes have been suggested as partial solutions to the carry problem. One interesting idea, which has been suggested by Dr. A. Svoboda of the Academy of Sciences in Prague [59], consists of representing a number in terms of its residues with respect to a given set of relatively prime numbers. That is, given such a set of relatively prime numbers consisting of, say, $m_1, m_2, \cdots, m_n$, the set of residues of any number in the interval from zero to $m_1 m_2 \cdots m_n$ is uniquely defined by its residues $r_1, r_2, \cdots, r_n$ with respect to these moduli. If, now, we wish to add (subtract) or multiply two numbers in this range, we can obtain the residue representation of the result by adding (subtracting) or multiplying the corresponding residues, modulo a given base, since $a+b=c$ implies $r(a)+r(b) \equiv r(c) \pmod{m}$ where $r(a)$ denotes the residue of a, and $ab=c$ implies $r(a)r(b) \equiv r(c) \pmod{m}$. Thus, we can form each residue in the set of residues which identifies the sum (difference) or product independently of all other residue pairs, *i.e.*, no carry operation is involved. This sum or product is uniquely identified *if* it lies between zero and the product of the moduli. This idea has been used to a limited extent for the residue representation of the decimal digits with respect to the moduli 2, 5, but it appears to be economically unfeasible to apply this idea to numbers in a much wider range. The article by H. L. Garner [50] describes other work in this area.

There has been no great use of macro-operations in modern computers. While it may be desirable to incorporate, say, a built-in sine function or built-in square root [51] operation in a special purpose computer there appears to be no great advantage in including such operations in general purpose computers. There are at least two reasons for this. First, considerable work has been done in minimizing the mathematical routines which can be used to compute the elementary functions [52]. The square root of a number can, for example, be computed in little more than four multiplication times, to six significant decimal digits where the word length is ten decimal digits. A second reason for not having built-in macro-operations is the increasing use of more sophisticated assembly programs. These permit the programmer to assume the availability of

macro-operations in writing his program. It is then the task of the assembly program to replace the macro-operation by an equivalent set of machine language instructions. Thus, programmer convenience is not a good reason for including such instructions in the machine order list. In certain real-time situations where minimization of computer time is essential, it still may be desirable to implement such operations with the hardware. For example, the SAGE system [27] includes the facility to perform arithmetic operations (of the kind needed in spatial coordinate transformation) on pairs of numbers (two dimensional coordinates).

Floating point multiplication and division are now executed in times which are comparable with those for the corresponding fixed point computations. Floating point addition, however, in most modern computers, requires two to three times as long as fixed point addition. Seven years ago, there was hesitancy on the part of some applied mathematicians to adopt automatic floating point operations. One of the principal reasons for this was the often misleading appearance of precision which characterizes the result of an extended calculation. In using fixed point arithmetic, the problem solver may be made sensitive to the possibility of the loss of accuracy by the disappearance of significant digits. However, in "normalized" floating point arithmetic no such warning appears. This defect, while it is still troublesome, is far out-weighed by the elimination of the need to scale a computation and the programming ease which floating point arithmetic makes possible. There have been, however, several attempts to solve this problem. Numerous experiments have been conducted in which a "significance indicator" accompanies every number during the course of a calculation. These significance indicators can be combined in accordance with certain statistical distributions of the expected round-off error when an arithmetic operation is performed on the operands. This new significance indicator then accompanies the result of the operation and provides an estimate of its accuracy. However, we are not aware of any attempt to make automatic the manipulation and preservation of these significance indicators during all computations. In the MANIAC III computer the order code will include certain unnormalized operations designed so that leading zeros will provide a measure of significance [53]. Unnormalized operations have also been provided on some of the other large scientific computers.

The "noisy" mode in STRETCH is an attempt to determine the effect of round-off error in a lengthy calculation. When the computer operates in this mode, ones, rather than zeros, are introduced in the low-order bit positions during the left shifting that occurs in normalized floating point operations. By comparing final results obtained in the normal mode with those obtained in the "noisy" mode, some estimate of the significance of these results can be obtained. The "perturbation" of intermediate results may cause significant differences in the results when the word length is inadequate for a given calculation.

C. Logical Operations

Facilities to perform logical operations on variable fields have been greatly increased in some modern binary computers. For example, in the STRETCH computer [54] it is possible to allow any of the sixteen logical connectives of two variables to operate upon each pair of bits in the memory and accumulator operands (variable fields). A logical connective is defined by a 2×2 truth table which defines all possible results obtained from the four input combinations of 0, 1 and there are, thus, sixteen such possible connectives. Essentially, the truth table information identifying the connective is contained in the instruction word. Little additional cost and complexity were introduced by permitting all sixteen logical operations rather than only the commonly used NOT, AND, OR and EXCLUSIVE OR. While the provision of such instructions is certainly a convenience, it is a little disappointing to note that no "deep" applications of digital computers appear to depend upon the ability to perform long sequences of such logical operations. We seem to be a long way from a successful application of Boole's "Laws of Thought" to those problems whose solutions involve the more subtle behavior of human intelligence. Very useful byproducts of these connective operations which are included in the result consist of counts of the number of leading zeros and total number of ones in the result field.

Instructions are available in several computers which are designed to simplify and speed up the conversion between, usually, the binary and decimal number systems.

D. Error Detection

It is apparent that as computers become faster the number of permissible errors per number of instructions executed must decrease in order for effective use of the machine to be made. Stopping a high speed computer is to be avoided unless absolutely necessary. Therefore, schemes have been implemented which enable the computer to detect and correct many of its own mistakes. The use of error detection and correction codes [55], [60] which appear in several new computers, provides much more economical checking than duplicate circuitry. When these codes are used, additional bits appear in every machine word. If m bits accompany the normal n bit word to serve as an error detection and correction code in a binary machine, it is possible for the configuration of these m bits to indicate, either that all $m+n$ bits are correct, or that one bit is in error and it can specify which one is in error. It is easily seen that a necessary condition for such an indication to be feasible is that $2^m \geq m+n+1$. Double errors can also be detected, but not identified, if one additional bit is used. If the detection and correction of multiple

bit errors is desired, then more bits are needed in the error detection field. The number of additional bits required increases rapidly with the multiplicity of the error to be detected. Recent suggestions involving some nontrivial mathematical ideas [56] have been made which will permit the economic detection and correction of multiple errors subject to the condition that these bit errors occur within a specified interval. This condition is not very restrictive because, in practice, when a machine error occurs in, say, data transmission, "bursts" of errors, where the errors are not widely spaced are not improbable.

V. Input-Output Control

A. The Input-Output Control Task

Perhaps in no part of their logical organization have computers so universally and thoroughly advanced since 1953 as in input-output control. The change in emphasis from scientific to business applications, and the expansion of most problems beyond the capacity of internal memory have sharply magnified the amount of data passed. This magnification has, in turn, made concurrent operation of I/O devices and central processors almost mandatory.

Properties of Input-Output Devices: It is useful to distinguish two purposes for which input-output devices are used, although at present most computers use the same control techniques for both purposes. Some devices, such as card readers, printers, card punches, and displays, are used primarily to furnish new data to the computer or to transmit final results. This can be called *true input-output*. Others, such as magnetic drums and disk files, are used primarily for *external storage*, to give high capacity or low cost at the expense of slower access. Some devices, notably magnetic tapes, serve both purposes. However, different tape units for the two different purposes seem to be evolving. In general, all kinds of devices for true input-output are designed primarily for compatibility with other equipment and for operating convenience. Devices for external storage are designed primarily for high capacity, high data rates, low cost per bit, and/or short access times to specific data.

In almost all I/O devices, cost and capacity requirements dictate mechanical motion of the storage medium. This motion gives all devices several common properties which constitute the principal problems in designing I/O control systems:

1) Access to randomly selected data is many orders of magnitude slower than in a computer's internal memory. Consequently, it is usually desirable to transfer information in fairly large blocks.
2) Data transmission rates are usually much slower than between central registers and internal memory. Consequently, reading or writing times for data may considerably exceed processing time.
3) Timing of the motion of the I/O device is usually quite independent of timing within the associated computer.
4) I/O devices are self-indexing, whether or not individual locations are addressable. That is, the reading or writing of a datum is accompanied by a motion that automatically prepares the device to read or write the successor datum.

Computer-Device Communications: Between a computer and its I/O devices flow not only data read or written, but also a considerable number and variety of control signals. The generation and handling of these has become considerably more complex as computers have evolved. Consider, for example, the reading of a tape device by a typical computer. The signals italicized in the following sequence occur regularly; the others may occur and must be provided for:

1) *The computer selects a tape device.*
2) The device notifies computer if it is inaccessible (busy, no tape, door open, fuse blown, etc.).
3) *Data in 6-digit characters flow from device to computer.*
4) Device notifies computer if parity check fails.
5) Device notifies computer of device malfunction (fuse blown, door open, etc.).
6) *Device notifies computer of end of block.*
7) Device notifies computer of end of file, longitudinal parity check failure, or other exceptional end of record.
8) Computer notifies device if end of input area is reached.

In summary, the input-output control must

1) Specify the I/O device to be used,
2) Buffer the independent timing, slow access, and low data rate of the device against the internal computer timing,
3) Assemble characters from the I/O device into computer memory words,
4) Generate successive memory addresses in which words of a block are to be stored,
5) Recognize or generate exceptional signals and provide for their handling.

The methods of generating data addresses and device specification have been quite closely related to buffering methods, which will be reviewed below. The methods of handling exceptional signals have usually been similar to methods of instruction sequencing, and differ primarily according to whether I/O operation is concurrent with computing.

In early computers, most exceptions, especially any requiring human action, caused machine stop. The inefficiency of this motivated the use of hardware interlocks to suspend operation until a busy unit is free. Some later machines incorporated several indicators which could be set by exception conditions and tested by branch instructions. In still more advanced computers,

I/O exception conditions constitute a principal reason for a program interruption system.

B. Buffering Techniques

Direct Program Control: The simplest and earliest I/O control technique was to use the stored program directly for specification of all I/O actions and to use the arithmetic registers for direct receipt and transmission of data. In the IBM 701 [32] and 704, for example, an instruction is used to select and actuate an I/O device for writing, and an iteration of copy instructions each specifies a memory word whose contents are transmitted to the multiplier-quotient register. The shift mechanism, needed in this register for multiplication and division, is used to disassemble the word into characters for magnetic tape recording. Interlocks cause premature instructions to wait for the I/O device; the programmer is responsible for not exceeding permitted times. Most exceptions cause machine stop.

Direct program control has been used in several computers using primarily paper tape, from the Mark I to the fairly recent Royal LGP 30. In these simpler computers, I/O word transfer operations use the accumulator, and thus may not be overlapped at all with other operations. In the IBM 704, operations not using the multiplier-quotient register may be executed while transfers between the MQ and I/O device are in progress, so long as timing rules are observed.

Block Transfer: A somewhat more sophisticated system, used for example in the IBM 705, utilizes the arithmetic registers for buffering and transfer, but has hardware to generate addresses automatically for a block transfer. Whole blocks of data may thus be read or written at behest of a single instruction. Processing and input-output may not, however, proceed concurrently. In this machine, as in several others designed for business use, individual characters are addressed, and no word assembly or disassembly need be performed.

In block transfer, the program must specify the I/O device, the beginning of the block in memory, and the extent of the block. The extent is often specified by a unique control character at the end of the block. Block transfer control will, for a given speed processor, handle higher data rates than direct program control, which requires multiple instruction executions between each I/O transfer. Block transfer also requires somewhat simpler programming.

Fixed-block Buffers: Concurrent computing and input-output requires the use of a separate set of registers for I/O. In early computers, such as the SR UNIVAC I, a fixed set of such registers is reserved. On input, a block of data is read into the registers at command of a single instruction; the buffer has its own control which indexes from one register to another. Word assembly is also performed automatically. When the buffer is full, a single command usually causes its contents to be transferred to a similar-sized block starting at a specified location in memory. In serial-access memories, such as delay lines or drums, such block transfer is fairly simple, because such memories are naturally self-indexing. Typically, the location of the block in main memory is somewhat constrained.

Whenever there is only one device per buffer, input may be improved by initially filling the buffer from the first block on the device. Thereafter, each block transfer from the buffer to memory also initiates another reading from the device. Program execution need wait only for the buffer-memory transfers.

On output, this short-delay action is always possible. A memory-buffer transfer initiates output, which proceeds at the slow device rate while program execution continues.

In some computers the buffer registers may be directly addressed; block transfer instructions are also usually provided. The programmer must avoid using such registers when I/O transfers are underway and the register contents are uncertain.

In the RW 400, the buffers (as usual, self-indexing) are multiplexable, and any buffer may be switched under program control to operate with any I/O device or with any computer in the system.

The use of a reserved set of registers for I/O buffering has two disadvantages: the cost of the extra or reserved hardware, which may not always be fully used, and the limitation on block size imposed by the buffer. In some computers, the block size may be smaller than that of the buffer; it may never be larger. This may require the use of time and space consuming interblock stops more frequently than is efficient.

Memory-Buffered Concurrent Operation: Concurrent operation can be obtained without block-size inflexibilities and time-consuming buffer-memory transfers, through the use of main memory for assembly of blocks. This requires somewhat more complex control.

The IBM 709 incorporates a representative system. Two or more concurrently-operating *data synchronizer* channels each contain one-word buffers used for assembly and disassembly of words. Program instructions select I/O devices and specify for each operation the memory area to be used. This is done by giving the channel the address of a *control word*, which in turn specifies the location and extent of the memory area. The channel initiates memory references as needed, and suitable interlocks delay computer references to memory when conflicts occur.

It should be remarked that the control-word form of specification may be used with block transfer control or ordinary buffers, as well as with data synchronizer channels. Because control word and index formats may be made alike, control word specification possesses several advantages for any of these uses.

Whenever I/O and program execution are concurrent, it is usually desirable for the program to suspend references to registers participating in I/O transfers until completion of these transfers. With separate buffers, no reference will occur until the next I/O opera-

tion. It suffices, in that case, for the completion of I/O transfers to be tested only when a new I/O operation is initiated. With memory-buffered systems, however, the program may make other references to the I/O storage area, so the program must be able to determine completion of transfers independently of initiating new ones. In the IBM 709, completion of an I/O transfer sets an indicator upon which the program can branch. In later computers, transfer completion causes program interruption.

With present-day technology, the control circuits of a channel are unnecessarily rapid for the data rates of the devices. In systems with multiple channels, these control circuits may be shared. In STRETCH, an *exchange* incorporates channels in multiples of eight to thirty-two. A single register is used for word assembly and is time-shared among all channels. A small 1-μsec core memory holds two data words and a control word for each channel. One data word is that currently being assembled, the second is awaiting a main-memory access.

Independent Input-Output Programming: It is often most efficient to distribute a single tape record into several solid memory blocks. This ability, often called scatter-read-write, has been incorporated in several recent computers [1]. The general technique is to permit a channel to fetch a sequence of control words to govern a single operation. In the IBM 709, for example, control words from successive memory locations may be fetched to control a transfer and a form of branching in the sequence is provided. In STRETCH, each control word specifies its successor.

In essence, such provisions make the I/O controller a separate stored-program processor. The flexibility of such a device is of course greater when the control word sequence can specify the device selection and the operation to be performed.

In the NBS Pilot and the SR LARC [34] these concepts are carried to a logical conclusion, and the I/O processor has quite flexible processing powers. In the Pilot, for example, program control specifies assembly and disassembly of all words and the initiation of signals to the I/O devices. In both machines, I/O exceptions are handled by the I/O processor, which may interrupt the main computer when necessary.

VI. Conclusion and Extrapolation

Predictions as to the logical organization of future computers must be divided into near- and far-term, with the dividing event the mastery of batch fabrication of logical and memory components. Present research in thin magnetic films, cryogenics, batch-produced semiconductors, and molecular electronics all point toward this development. A batch-fabricated technology will stimulate the design of ultra-concurrent computers which use perhaps millions of elements that may be individually slow. Unger [57] and Holland [58] have made preliminary studies of suitable machines for such technology.

In the near-term, smaller computers will probably continue to have fundamentally conventional organizations, but will be increasingly equipped with modest versions of the innovations that already are appearing in large machines.

The evolution of large machines using individually-fabricated components can be expected to follow several trends now seen.

Indexing and indirect addressing systems will become increasingly elaborate, and more use will be made of independently programmed auxiliary address generators, such as those in Pilot and HARVEST. Large computers will universally provide some method of protecting portions of memory from inadvertent or unauthorized use.

Instruction information density will be increased by more use of variable-address instructions and by the wider use of abbreviated addresses.

As Mersel predicted [21] program interruption provisions appear likely to be universally adopted in larger computers. As more real-time applications are mechanized, the necessity of this technique becomes increasingly important. Closely allied, is the provision of rapid program relocation methods. Multiprogramming appears certain to become a more widely used operating technique and efficient multiprogramming demands interruption, address protection, real-time clocks, and program relocation facility.

The use of sophisticated addition and multiplication schemes will also become universal. Also, new large machines will contain more logical and manipulative power for handling bits as such and for handling portions of words.

Concurrent operation of input-output devices and computers are already almost universal among large machines. The use of independently programmed I/O exchanges or controllers appears certain to increase.

The whole trend in logical design reflects two dominant forces: the increasing application of computers to real-time control problems, and the growing realization that hardware cost is only one component of the cost of data processing. Since the total cost of getting answers can often be reduced by increasing hardware cost, increasing elaboration of hardware will continue so long as the workloads permit the resulting machines to be fully utilized.

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High-Speed Arithmetic in Binary Computers*

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Summary—**Methods of obtaining high speed in addition, multiplication, and division in parallel binary computers are described and then compared with each other as to efficiency of operation and cost. The transit time of a logical unit is used as a time base in comparing the operating speeds of different methods, and the number of individual logical units required is used in the comparison of costs. The methods described are logical and mathematical, and may be used with various types of circuits. The viewpoint is primarily that of the systems designer, and examples are included wherever doing so clarifies the application of any of these methods to a computer. Specific circuit types are assumed in the examples.**

Introduction

THE PURPOSE of this report is to describe various methods of increasing the speed of performing the basic arithmetic operations in such a manner that one method may be readily compared with another, both as to relative operating efficiency and relative equipment cost. It is divided into three parts: Adders, Multiplication, and Division.

Adders

As it is generally recognized that most of the time required by adders is due to carry propagation time, this section deals with methods of reducing this time, together with their efficiency and relative costs. It considers adders both from the standpoint of reducing the length of the carry path when using a fixed-time adder and of recognizing the completion of an addition to take advantage of the short length of an average carry. Circuits shown are in terms of basic logic blocks, and use the transit time of a logical block as a unit to permit the application of conclusions to various types of circuits.

Multiplication

In multiplication, if one addition is performed for each *one* in the multiplier, the average multiplication would require half as many additions as there are bits in the multiplier. This can be improved considerably by the use of both addition and subtraction of the multiplicand. The rules for determining when to add and subtract are developed, and the method of determining the number of operations to expect from the bit grouping is explained. This results in a variable number of add cycles for fixed-length multipliers. For some applications a fixed number of cycles is preferable. To accommodate this requirement, rules are developed for handling two- and three-bit multiplier groupings.

Multiplication, which involves repeated additions in which the selection of the various addends is not affected by a previous sum, offers the possibility of improved speed by the use of carry-save adders. Conditions under which such improvements will be realized are investigated, and methods that may be used to reduce the amount of equipment required are described.

Division

Working from the premise that a division should require no more additions than would be required if the resulting quotient were used as the multiplier in a multiplication, the development of such a method is traced through several stages. Then another and still faster method is also described. Methods of evaluating the speeds of these various methods are developed in such a manner as also to permit evaluation of the effects of variation in maximum shifter size.

General

For the purpose of illustrating points in the use of these various arithmetical methods which may affect their application to computers, several typical systems circuits are shown, and the use of these is assumed in the numerical examples included. The following is a brief description of the circuits that are assumed available and a definition of terms that will be used.

DC rather than pulse-type logic is assumed. Registers, or data storage devices, are assumed to be separate from the adder. The use of a separate shifter rather than a shifting register is assumed. Most registers used are "latch-registers"; this means a register capable of being set from data lines, which are in turn controlled by the output of the same register upon the application of a latch-control signal. A gate is a group of two input AND circuits, each having one of its two inputs connected to a common line, and the other input to a data input line. A shifter is a device for transferring all bits in a register a specified number of positions left or right. The term "addition" will be used to include both addition and subtraction, and the same adder will be used for both. Subtraction will always be performed by the use of the two's complement of the number to be subtracted from the other. This will be obtained by inverting all bits in the number and also forcing an additional *one* into the carry position of the low order bit position of the adder when performing the addition.

Logical circuits are shown with inputs on the left and outputs on the right. The bottom output position represents the logical function described in the box, while the top output position represents its inverse. The logical symbols used within the boxes are AND (&), INCLUSIVE OR ($\vee$), and EXCLUSIVE OR ($\forall$). When the word OR is used alone, it means INCLUSIVE OR.

* Received by the IRE, July 25, 1960.

† Product Dev. Lab., Data Systems Div., IBM Corp., Poughkeepsie, N. Y.

Unless otherwise specified, arithmetic used in examples is assumed to be binary floating point, although the methods described are not limited in their use to this type of arithmetic. When a number is described as normalized, it means that the fraction has been shifted in the register until the high order *one* in the fraction is located just to the right of the binary point, and the exponent has been adjusted accordingly. Thus a normalized fraction will always have a value less than one and equal to or greater than one-half. In the examples, exponent handling is implied but not described in detail.

Binary Adders

Binary Adders, Fixed Time

The basic binary adder is comparatively simple and quite well known. It is also comparatively slow. Fig. 1 shows one version of one stage of such an adder.

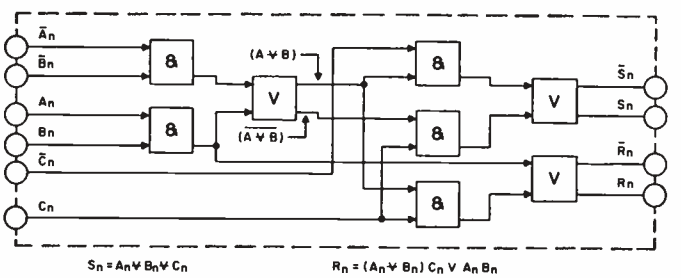


Fig. 1—Full adder, one stage.

In the discussion of adders, the lowest order bit or adder position will be designated as 1. The two multibit numbers being added together will be designated as A and B, with individual bits being A_1, A_2, B_1, etc. The third input will be C. Outputs will be S (sum) R (carry), and T (transmit).

The conventional ripple-carry adder consists of a number of stages like that shown in Fig. 1, connected in series, with the R output of one stage being the C input of the next. The time required to perform an addition in such an adder is the time required for a carry originating in the first stage to ripple through all intervening stages to the S or R output of the final stage. Using the transit time of a logical block as a unit of time, this amounts to two levels to generate the carry in the first stage, plus two levels per stage for transit through each intervening stage, plus two levels to form the sum in the final stage, which gives a total of two times the number of stages.

The usual forms of the logical description of the sum and carry from the nth stage of an adder are $S_n = (A_n \forall B_n \vee C_n)$ and $R_n = (A_nB_n \vee A_nC_n \vee B_nC_n)$. Also, from the description of connection between sections, $C_n = R_{n-1}$. If the carry description is rearranged to read $R_n = (A_n \forall B_n)C_n \vee A_nB_n$, and if T_n is defined as $(A_n \forall B_n)$ and D_n is defined as (A_nB_n), then

$$R_n = D_n \vee T_nC_n.$$

This separates the carry out of a particular stage into two parts, that produced internally and that produced externally and passed through. The former is called a generated carry and the latter is called a propagated carry. From this the description of the carry into any stage may be expanded as follows:

$$C_n = R_{n-1}$$

$$C_n = D_{n-1} \vee T_{n-1}R_{n-2}$$

$$C_n = D_{n-1} \vee T_{n-1}D_{n-2} \vee T_{n-1}T_{n-2}R_{n-3}$$

$$C_n = D_{n-1} \vee T_{n-1}D_{n-2} \vee T_{n-1}T_{n-2}D_{n-3} \vee T_{n-1}T_{n-2}T_{n-3}R_{n-4}.$$

This can be continued as far as is desired.

Fig. 2 illustrates the application of this principle to a section of a carry propagate adder to increase its speed of operation. By allowing n to have successive values starting with one and omitting all terms containing a a resulting negative subscript, it may be seen that each stage of the adder will require one OR stage with n inputs and n AND circuits having one through n inputs, where n is the position number of the particular stage under consideration.

It is obvious that circuit limitations will put an upper limit on the number of stages of an adder that can be connected together in this manner. However, within this limit the maximum carry path between any two stages is two levels, or six levels for the complete addition.

Assume that five stages represent a reasonable number of adder stages to be connected in this manner and designate such an arrangement as a "group." The group containing the five low-order positions of the adder will be group 1, etc. A carry into group n will be C_{gn}, while a carry out of the group will be R_{gn}. If these five-bit groups are now connected in series with $C_{gn} = R_{g(n-1)}$, a a carry will require four levels to be produced and reach the output of the first group, two levels to go through each intermediate group, and four levels to reach and be assimilated into the sum in the final group. Thus, for five-bit groups, the maximum carry path length would be $4+(2n/5)$ as compared to $2n$ for a straight ripple-carry adder. For a 50-bit adder this would give 24 levels as compared to 100.

Since each five-bit group may be considered as one stage in a radix-32 adder, a transmit signal may be generated to take a carry across the group. This will be designated as T_{gn}, and will be defined as $T_g = T_1T_2T_3T_4T_5$, where the numbers 1, 2, etc., refer to positions within the group rather than within the adder. At the same time D_{gn}, which includes only carries originating within the group, may replace R_{gn}, which includes the effect of C_{gn}, whenever a higher level of look-ahead than the one under consideration is being used with it. The use of

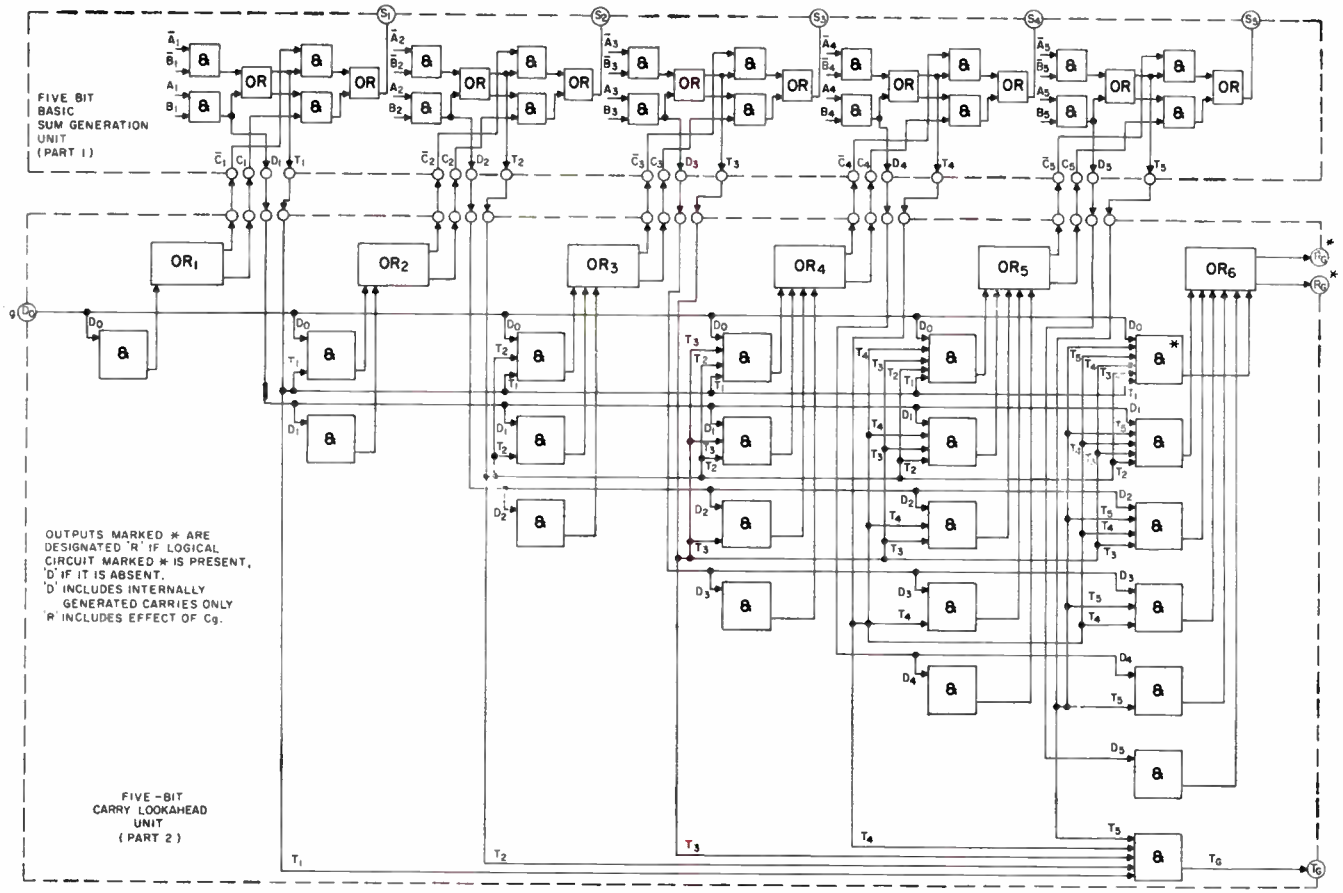


Fig. 2—Five-bit adder group with full carry look-ahead.

R_{gn} where D_{gn} is called for will not produce an error, but will add unnecessary components.

This process may be continued by designating five groups as a section and then using carry speed-up circuits between the sections. Carries into a section will be C_{sn}, and carries out of a section will be D_{sn}. (If the third level of carry look-ahead is not used, R_{sn} must be used in place of D_{sn}.) The maximum path length for a carry to be generated within a section and reach the output D_{sn} is six levels. The maximum path length for a carry appearing at the input to a section as C_{sn} to affect the sum is also six levels. The maximum path length for a carry originating within a section to affect a sum within the same section is ten levels.

Carry look-ahead between bits within a group is called level one look-ahead, between groups within a section is called level two, and between sections is called level three. Table I gives a comparison of speed improvement for different amounts of look-ahead. Five bits to the group and five groups to the section are assumed. The time units are logical level transit times.

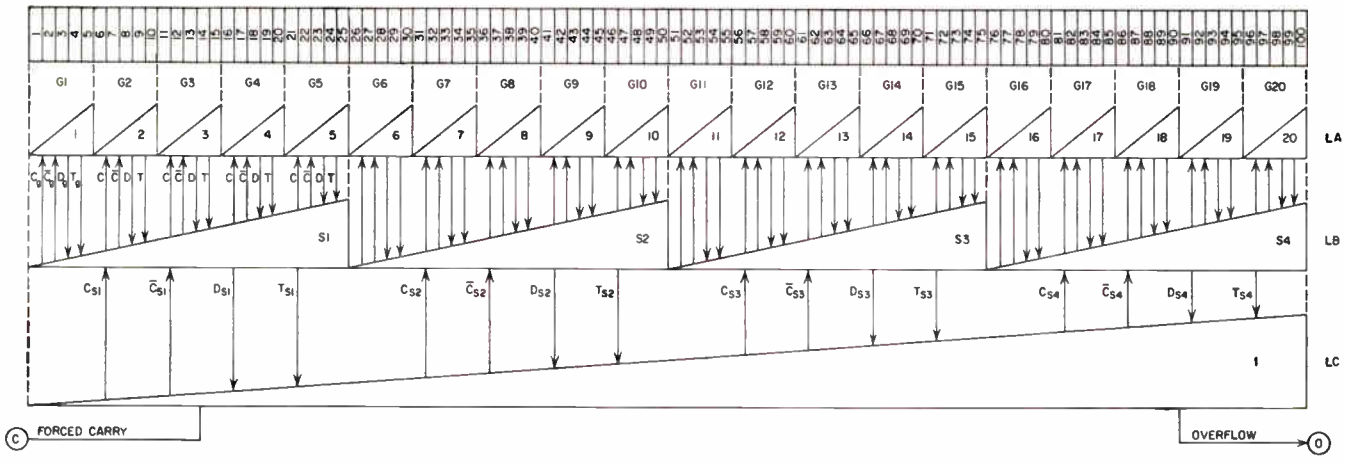
The transmit signal has been described as the EXCLUSIVE OR combination of A and B. Correct operation will also be obtained if the INCLUSIVE OR is used instead, of or in combination with, the EXCLUSIVE OR. The only effect will be a redundant signal at times.

TABLE I

Look-Ahead Levels→	0	1	1 and 2	1, 2, and 3
Adder Bits				
5	10	6	—	—
10	20	8	—	—
25	50	14	10	—
50	100	24	12	—
100	200	44	16	14

Figs. 2 and 3 together illustrate a 100-bit adder with full carry look-ahead. In Fig. 2 (part 1) are shown the details of the basic sum generation unit, while (part 2) shows the basic carry look-ahead unit. Fig. 3 shows the method of combining the parts to give the complete adder. The complete circuit shown in Fig. 2 represents one group in Fig. 3.

Various modifications may be made to the circuit shown in Fig. 3 if smaller size or less than maximum speed is required. Some of the possibilities which are likely to be of particular use to the computer designer are listed below, and their relative speeds and costs will be included in the comparison table. Some minor variations which these modifications may cause and which would be obvious to anyone considering the problem will not be described in detail. Comparisons will be made on the basis of 50-bit and 100-bit adders.



TRANSIT TIME

A_i TO D_G = 4 UNITS
C_g TO S = 4 UNITS
C_g TO D_g = 2 UNITS
A_i TO T_g = 3 UNITS
D_g TO D_S = 2 UNITS
D_S TO C_S = 2 UNITS
C_S TO C_g = 2 UNITS

LOGICAL UNITS

BASIC ADDER 5-BIT GROUP	= 30
5-INPUT LOOKAHEAD	= 28
4-INPUT LOOKAHEAD	= 22

	50 BIT ADDER	100 BIT ADDER
MAX TRANSIT TIME	12 UNITS	14 UNITS
LOGICAL UNITS		
BASIC SUM GENERATION UNITS	300	600
FIRST LEVEL CARRY	280	560
SECOND LEVEL CARRY	56	112
THIRD LEVEL CARRY	0	22
TOTAL	636	1294
LOGICAL UNITS/BIT	12.72	12.94

Fig. 3—Carry-propagate adder with full carry look-ahead.

1) Eliminate the look-ahead within groups, but retain it between groups and between sections.
2) Retain the look-ahead within groups, but use ripple carry between groups.
3) Use the very elementary carry speed-up circuit used with the completion recognition adder (Fig. 4). This can be used with any adder, and will give almost a four-to-one increase in speed over that of a full ripple-carry adder of 100 bits for only about 2.5 per cent increase in equipment. It provides a carry bypass circuit within rather than around the group. Its principal merit is the high percentage improvement per unit increase in cost.

Table II summarizes the comparative costs and speeds for five different adder versions for 50-bit and 100-bit adders. The 50-bit ripple-carry adder is used as a reference for cost comparison. The types being compared are 1) full ripple carry, 2) full carry look-ahead, 3) ripple carry within five-bit groups, look-ahead between groups, 4) look-ahead within five-bit groups, ripple carry between groups, 5) carry bypass within five-bit groups, ripple carry between groups.

Binary Adders, Variable Time

It can be shown that for a large number of binary additions the average length of the longest carry of each addition will not be greater than $\log_2 N$, where N is the number of bits in the numbers being added together. Random distribution of bits within the numbers is assumed. This gives an average maximum carry length of not greater than 5.6 for a 50-bit sum or 6.6 for a 100-bit sum.

In a ripple-carry adder a six-position carry would represent twelve units of time, as compared to fourteen units maximum for a 100-bit adder with full look-ahead. Also, the twelve units represent actual transit time, while the fourteen units represent predicted time with safety factor. In addition, the carry look-ahead adder represents 60 per cent more equipment than the basic ripple-carry adder.

The variable time (completion recognition) adder must contain additional equipment that will permit the recognition of the completion of carry propagation. Ideally, this equipment should have three characteristics. It should be inexpensive. It should not add to the

TABLE II

Adder Type	50-Bit Adder			100-Bit Adder		
	Logical Units	Comparative Cost	Time	Logical Units	Comparative Cost	Time
1	400	100.0	100	800	200.0	200
2	636	159.0	12	1294	323.4	14
3	466	116.5	24	954	238.4	26
4	580	145.0	24	1160	290.0	44
5	410	102.5	36	820	205.0	52

time needed to complete the addition. It should not indicate completion, even momentarily, when an addition is still incomplete, and if an input changes after an addition has been completed, the completion signal should immediately go off and remain off until the new result is completed.

Fig. 4 illustrates one version of a completion recognition adder. While it does not meet all of the requirements of an ideal unit, it does appear to be reliable when used with the proper restrictions. This adder requires approximately 1280 logical units for 100 bits, which is essentially the same as the 1294 units for the full carry look-ahead adder. Thus, where cost is concerned they may be considered the same. However, part of the additional equipment required for the carry-recognition circuits may also be used as part of the checking circuitry. To obtain equivalent checking with the carry look-ahead adder would require considerable additional equipment.

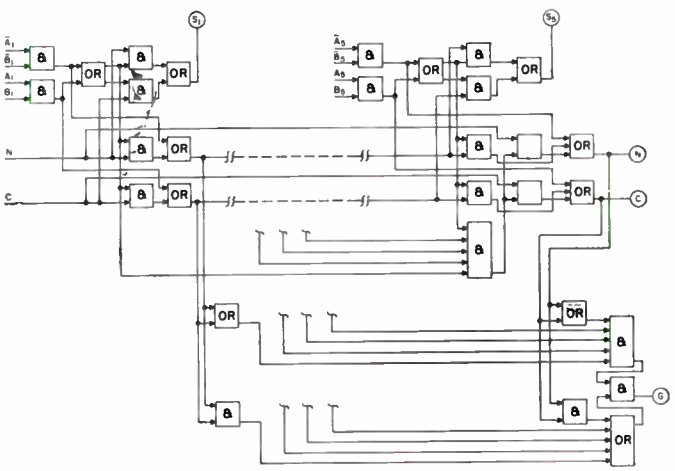


Fig. 4—Completion recognition adder.

Each stage of the adder generates a carry and a no-carry signal, and these are propagated through the adder along separate paths. If these signals are designated as C and N, completion of the addition is recognized by the existence of the condition [(C OR N) and not (C AND N)] at the output of every bit position in the adder.

The operation of this adder will be more readily understood if it is recognized that $C_n = A_n B_n \vee T_n C_{n-1}$ and that $N_n = \overline{A}_n \overline{B}_n \vee T_n N_{n-1}$. At the start of an addition the inputs to the adder must be cleared. This sets the N output of each block to *one* and the C output to *zero*. The desired inputs are then entered, which changes the N outputs to *zero* for those positions which have a *one* in either or both inputs. This turns off the completion signal. The C output is changed to *one* for those positions having an input of 11 and the T signal is changed to *one* for those positions having 01 or 10. The latter positions have *zero* on both the C and N lines. Signals will then ripple down either the C or N lines from positions having either 00 or 11 inputs until all positions have either the C or the N output energized, at which time a completion signal will be generated. To prevent false indications of completion, the two inputs must enter the adder simultaneously; once the operation has started, no changes may be made in the inputs, and both inputs must be changed to *zero* before the next addition may be performed. An alternative to this is to force *ones* into all input positions by using an additional input to the OR circuits that are usually present at the input to adders. The restriction here would be that the correct inputs are present at the input to the OR circuits at the time the forcing inputs are turned off.

No general statement can be made as to whether fixed-time or variable-time adders are better. The use of a completion recognition adder offers many attractions to the systems designer, particularly if his circuits have a large spread between average and maximum transit time. On the other hand, the limitations on data handling required to prevent ambiguities in the control signals may nullify some or all of the theoretical advantages. The best choice can only be made by a careful consideration of all of the factors involved for the particular application.

Binary Multiplication

Multiplication Using Variable Length Shift

Multiplication in a computer is usually performed by repetitive addition. For constant circuit and adder speeds, the time required to perform a multiplication is proportional to the number of additions required. The slowest way would be to go through one add cycle for each bit of the multiplier. Substituting shift cycles for add cycles when the multiplier bit is a *zero* can reduce this time; supplying the ability to shift across more than one position at a time when there are several *zeros* in a group can reduce the time still further. Assuming random distribution with equal numbers of *ones* and *zeros* in the multiplier, this should result in a 50 per cent reduction in time. This is as much improvement as is obvious from normal methods of performing multiplication.

Further improvements may be secured by taking advantage of some of the properties of the binary system. The rules for handling multiplication to obtain this improvement will be developed.

A binary integer may be written in the following form:

$$A_n 2^n + A_{n-1} 2^{n-1} + A_{n-2} 2^{n-2} + \cdots + A_2 2^2 + A_1 2^1 + A_0 2^0.$$

The actual number, as written, consists of the characteristics only and would be written $A_n A_{n-1} A_{n-2} \cdots A_2 A_1 A_0$, where each A would have a value of either one or zero. If such a number contained the coefficients $\cdots 011111111110 \cdots$, this part of the number would

have the value $2^{n-1}+2^{n-2}+\cdots+2^{n-x}$, where n is the position number of the highest order *one* in the group for which the lowest order position in the number is designated *zero*, and x is the number of successive *ones* in the group. The numerical value of this last expession may also be obtained from the expression 2^n-2^{n-x}, where n and x have the same values as before. For example, in the binary number 0111100, n is 6 and x is 4. The decimal equivalent of the number is given by $2^5+2^4+2^3+2^2=32+16+8+4=60$. It is also given $2^6-2^2=64-4=60$. Thus for any string of *ones* in a multiplier, the necessity for one addition for each bit can be replaced by one addition and one subtraction for each group. The only additional equipment required is a means of complementing the multiplicand to permit subtracting and, of course, some additional control equipment. To illustrate this a typical multiplier is shown below with the required operations indicated. Each group of *ones* is underlined.

1 1 1 1 0 0 0 0 1 1 1 0 1 1 1 0 1 0 1 0 0 0 1 0 1

\+ − + −+ −+−+− +−+−

Additional improvement may be obtained by using the fact that $+2^n-2^{n-1}=+2^{n-1}$ and $-2^n+2^{n-1}=-2^{n-1}$. This is illustrated by applying it to the above example. The original results are given first, with the operations to be combined underlined.

1 1 1 1 0 0 0 0 1 1 1 0 1 1 1 0 1 0 1 0 0 0 1 0 1

\+ − + −+ −+−+− +−+−

\+ − + − − −− + +

\+ − + −+ −+−+− +−+−

\+ − + − − + + + +

Two different arrangements are shown. Both will give the correct result, and the number of cycles required is the same. The first is that obtained by starting at the high order end, and the second by starting at the low order end.

For a given multiplier, the number of additions that will be required may be computed as follows. Define a group of *ones* as a series of bits containing not more than a single *zero* between any pair of *ones* within the series, containing at least one pair of adjacent *ones*, and starting and ending with a *one*. Then the number of add cycles is equal to the following: Two times the number of groups, plus the number of *zeros* contained within groups, plus the number of *ones* not contained within groups. This may be illustrated with the previous example.

1 1 1 1 0 0 0 0 1 1 1 0 1 1 1 0 1 0 1 0 0 0 1 0 1.

There are two groups. The first group contains no *zeros*, the second contains three. There are two *ones* not contained in any groups. This gives $(2\times2)+3+2=9$, which is the number of operations that was obtained. Within the limitation of using only multiples of the multiplicand that can be obtained directly by shifting and using only one of these at a time, it is believed that this represents the least number of additions with which a binary multiplication can be performed.

The rules for performing a multiplication may now be given. It is assumed that the multiplier and the partial product will always be shifted the same amount and at the same time. The multiplier is shifted in relation to the decoder, and the partial product with relation to the multiplicand. Operation is assumed starting at the low-order end of the multiplier, which means that shifting is to the right. If the lowest-order bit of the multiplier is a *one*, it is treated as though it had been approached by shifting across *zeros*.

1) When shifting across *zeros* (from low order end of multiplier), stop at the first *one*.

a) If this *one* is followed immediately by a *zero*, add the multiplicand, then shift across all following *zeros*.
b) If this *one* is followed immediately by a second *one*, subtract the multiplicand, then shift across all following *ones*.

2) When shifting across *ones* (from low order end of multiplier), stop at the first *zero*.

a) If this *zero* is followed immediately by a *one*, subtract the multiplicand, then shift across all following *ones*.
b) If this *zero* is followed immediately by a second *zero*, add the multiplicand, then shift across all following *zeros*.

A shift counter or some equivalent device must be provided to keep track of the number of shifts and to recognize the completion of the multiplication.

If the high-order bit of the multiplier is a *one* and is approached by shifting across *ones*, that shift will be to the first *zero* beyond the end of the multiplier, and that *zero* along with the bit in the next higher order position of the register will be decoded to determine whether to add or subtract. For this reason, if the multiplier is initially located in the part of the register in which the product is to be developed, it should be so placed that there will be at least two blank positions between the locations of the low-order bit of the partial product and the high-order bit of the multiplier. Otherwise the low-order bit of the product will be decoded as part of the multiplier. An alternative to this is for the fact that the shift counter indicates the end of the multiplication to force the last operation to be an addition.

It should be noted that whenever the shifting is across groups of *ones* the partial product will be in complement form, which means that the shifter must contain

provision for inserting *ones* in all high order positions that would normally be left blank by the shifting.

If the multiplication is performed starting from the high-order end of the multiplier, the partial product will always be in true form, but any operation may result in a carry traveling the full length of the partial product. The shifting rules are a little more complicated, as may be seen below.

1) When shifting across *zeros* (from high-order end of multiplier)

a) If the first *one* following the *zeros* is followed immediately by a second *one*, stop shifting at the last *zero* and add the multiplicand, then shift across following *ones*.

b) If the first *one* following the *zeros* is followed immediately by a *zero*, stop shifting at the first *one* and add the multiplicand, then shift across following *zeros*.

2) When shifting across *ones* (from high-order end of multiplier)

a) If the first *zero* following the ones is followed immediately by a second *zero*, stop shifting at the last *one* and subtract the multiplicand; then shift across the following *zeros*.

b) If the first *zero* following the *ones* is followed immediately by a *one*, stop shifting at the first *zero* and subtract the multiplicand, then shift across the following *ones*.

The high-order *one* of the multiplier is treated as though there were at least two *zeros* immediately preceding it.

As was previously stated, these two methods of decoding the multiplier will yield the same number of add cycles. This number is dependent on the number and distribution of *ones* within the multiplier. If random distribution is assumed, it can be shown that the average shift for each addition will be 3.0 bit positions when using an infinite shifter, or 2.9 bit positions for a shifter having a limit of six.

Multiplication Using Uniform Shifts

For some applications a method of multiplication which uses shifts of uniform size and permits predicting the number of cycles that will be required from the size of the multiplier is preferable to a method that requires varying sizes of shifts. The most important use of this method is in the application of carry-save adders to multiplication, although it can also be used for other applications. The use of carry-save adders will be discussed in a later section.

Two methods will be described. The first requires shifting the multiplier and partial product in steps of two, the second in steps of three. Both methods require the ability to shift the position of entry of the multiplicand into the adder in relation to its normal position. The latter is designated as the one-times-multiplicand position and used as a reference position in all descriptions. This small shifter will be the length of the multiplicand rather than of the partial product. Both methods may be used starting from either end of the multiplier, but because of the reduced requirements on the size of the adder, are usually used starting from the low-order end. The latter will be assumed for any operating descriptions, but for easier explanation the rules of operation will be developed assuming a start from the high-order end.

Uniform Shifts of Two

Assume that the multiplier is divided into two-bit groups, an extra zero being added to the high-order end, if necessary, to produce an even number of bits. Only one addition or subtraction will be made for each group, and, using the position of the low-order bit in the group as a reference, this addition or subtraction will consist of either two times or four times the multiplicand. These multiples may be obtained by shifting the position of entry of the multiplicand into the adder one or two positions left from the reference position. The last cycle of the multiplication may require special handling. Rules for this will be considered after the general rules have been developed.

The general rule is that, following any addition or subtraction, the resulting partial product will be either correct or larger than it should be by an amount equal to one times the multiplicand. Thus, if the high-order pair of bits of the multiplier is 00 or 10, the multiplicand would be multiplied by zero or two and added, which gives a correct partial product. If the high-order pair of bits is 01 or 11, the multiplicand is multiplied by two or four, not one or three, and added. This gives a partial product that is larger than it should be, and the next add cycle must correct for this.

Following the addition the partial product is shifted left two positions. This multiplies it by four, which means that it is now larger than it should be by four times the multiplicand. This may be corrected during the next addition by subtracting the difference between four and the desired multiplicand multiple.

Thus, if a pair ends in *zero*, the resulting partial product will be correct and the following operation will be an addition. If a pair ends in a *one*, the resulting partial product will be too large, and the following operation will be a subtraction.

It can now be seen that the operation to be performed for any pair of bits of the multiplier may be determined by examining that pair of bits plus the low-order bit of the next higher-order pair. If the bit of the higher-order pair is a *zero*, an addition will result; if it is *one*, a subtraction will result. If the low-order bit of a pair is considered to have a value of one and the high-order bit a value of two, then the multiple called for by a pair is the numerical value of the pair if that value is even and

one greater if it is odd. If the operation is an addition, this multiple of the multiplicand is used. If the operation is a subtraction (the low-order bit of the next higher-order pair a *one*), this value is combined with minus four to determine the correct multiple to use. The result will be zero or negative, with a negative result meaning subtract instead of add. Table III summarizes these results.

TABLE III

Multiplier	Operation	Multiplier	Operation
0−0 0	+0	1−0 0	−4+0=−4
0−0 1	+2	1−0 1	−4+2=−2
0−1 0	+2	1−1 0	−4+2=−2
0−1 1	+4	1−1 1	−4+4=−0

It is obvious from the method of decoding described that the multiplier may be scanned in either direction. When starting from the high-order end, the partial product will always be in true form, but starting from the low-order end will result in a complement partial-product part of the time. This means that the main shifter must be designed to handle the shifting of complement numbers.

The possibility that the low-order bit of the multiplier will be a *one* presents a special problem. For operations starting at the high-order end of the multiplier this may be handled in either of two ways. One requires an additional cycle only when the low-order bit is a *one*, and consists of adding the complement of one-times the multiplicand following a zero shift after the completion of the last regular operation. The other method adds an additional add cycle to every multiplication by always treating the multiplier as though it had two additional low-order zeros. The two extra *zeros* which this introduces into the product are then ignored.

When operating from the low-order end of the multiplier this problem may be handled more easily. On the first cycle there is no previous partial product. Therefore *zeros* are being entered into one side of the adder. If the low-order bit of the multiplier is a *one*, enter the complement of one times the multiplicand into the adder by way of the input usually used for the partial product. At the same time, the multiple of the multiplicand selected by decoding the first pair of bits of the multiplier is entered at the other adder input. This does not require any additional cycles.

Uniform Shifts of Three

This method of handling three bits of the multiplier at a time requires being able to obtain two, four, six, or eight times the multiplicand. One times may also be required to handle the condition of a *one* in the low-order bit position of the multiplier. One, two, four, and eight times can all be obtained by proper positioning of the multiplicand, but the six times must be generated in some manner. This can be done by adding one times the multiplicand to two times the multiplicand, shifting the result one position, and storing it in a register.

The development of the decoding rules for this method follows the same basic requirements already described for handling two-bit groups. This is evident from Table IV and will not be repeated.

TABLE IV

Multiplier	Operation	Multiplier	Operation
0−0 0 0	+0	1−0 0 0	−8+0=−8
0−0 0 1	+2	1−0 0 1	−8+2=−6
0−0 1 0	+2	1−0 1 0	−8+2=−6
0−0 1 1	+4	1−0 1 1	−8+4=−4
0−1 0 0	+4	1−1 0 0	−8+4=−4
0−1 0 1	+6	1−1 0 1	−8+6=−2
0−1 1 0	+6	1−1 1 0	−8+6=−2
0−1 1 1	+8	1−1 1 1	−8+8=−0

There are some general facts that apply to both the two-shift and the three-shift methods of multiplication.

1) The choice of true or complement entry of the multiplicand into the adder is dependent only on the condition of the low-order bit of the next-higher-order group of the multiplier.
2) Special provision must be made for the condition of a *one* in the low-order bit position of the multiplier. Procedure is the same for both methods.
3) Whenever complement inputs are used for multiplicand multiples, there must also be provision for entering a low-order *one* into the adder to change the one's complement to a two's complement. This includes the complement of one times the multiplicand used because of a low-order multiplier *one*. This can result in a design problem, since odd numbers in the two low-order groups of the multiplier may call for the entry of two additional *ones* into the low-order position of the adder, making a total of four entries. A solution to this is to decode the low-order group of the multiplier to call for the desired multiple, or one less instead of one more. Then the true value of one times the multiplicand can be used in the partial product position on the first cycle when the multiplier has a low-order *one*. This may be done very easily, on the first cycle only, by forcing the low-order bit of the group to enter the decoder as a *zero*, but using its actual value to determine whether or not to add one times the multiplicand. The justification for this may be seen from either table. This modification of the decoding will not work for any cycle except the first, and only when operating from the low-order end of the multiplier.

To permit a comparison, the illustrative multiplier used previously to show decoding for the variable-shift method will be shown below for variable shift, two-position shifts, and three-position shifts.

All decoding shown is based on starting at the low-order end of the multiplier. Multiplier groupings are indicated in (2) and (3). The use of multiples of four in (2) and of eight in (3) places the effective location of the

```
0  0  1  1  1  1  0  0  0  0  1  1  1  0  1  1  1  0  1  0  1  0  0  0  1  0  1
   +           −           +           −        −     +     +           +     +      (1)

   +2    −0      −2  +0    +2    −0    −2    −0    −2    −2    −4    +2    −4 +
0' 0  1' 1  1' 1  0' 0  0'  0  1' 1  1' 0  1' 1  1' 0  1' 0  1' 0  0' 0  1' 0  1'   (2)
   +           −           +           −        −  −        +  −     +

   +2        −0      −8        +4      −2        −2        +6      −8        +4 +
'0 0  1' 1  1  1' 0  0  0'  0  1  1' 1  0  1' 1  1  0' 1  0  1' 0  0  0' 1  0  1'   (3)
   +           −           +           −        −     + +  −           +     +.
```

operation under the low-order bit of the next higher group. An underline under a pair of operations in (3) indicates the use of the previously prepared three-times multiple. The (+) following the multiple figure for the low-order group indicates that one times the multiplicand is also used in the partial product entry position. The decoding for this particular group is assumed modified as previously described.

Variable Shift Multiplication Circuit

Fig. 5 shows a brief outline of a system capable of performing multiplication in the manner just described. At the start of the operation the multiplier is entered in the right half of the *MQ* register, the multiplicand into the *MD* register, one more than the multiplier size into the shift counter register, and two into the shift control register, and also the "use" trigger is set OFF. (It is assumed that the multiplier is initially entered into the same position of the *MQ* register as the low-order end of a double precision number would be, which would place its high-order bit immediately adjacent to the low-order position of the partial product. The initial shift of two separates these by two bit positions, the necessity for which was previously described. The initial shift counter register setting is adjusted for this. The decoder is located to give correct operation with this offset.)

Since the "use" trigger is OFF and the partial-product in the *MQ* register is also *zero*, the output of the main adder will be *zero*. The two in the shift-control register causes two to be subtracted from the contents of the shift counter register in the shift counter adder. The low-order end of the shifted multiplier goes into the decoder and is decoded to give the next shift required and to determine whether the next operation will be add-true, add-complement, or neither (if shift called for is larger than shifter can give). When sufficient time has been allowed for these operations to be completed, a latch control signal sets the results into the proper registers, and the next cycle starts. These cycles are repeated as many times as required, the shift called for as a result of decoding being compared each time with the contents of the shift counter register to determine when sufficient cycles have been taken.

To determine the time required for a cycle, three data paths must be considered and the longest used. They all include time to power the latch control signal and set information into the proper trigger, plus any safety factor that must be allowed because of variation in

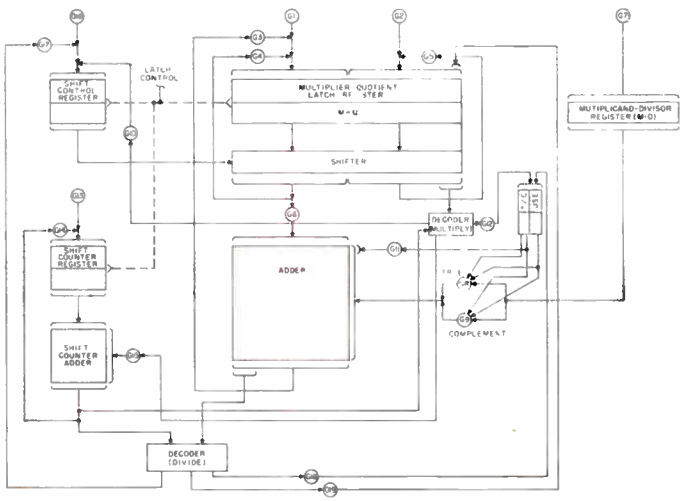


Fig. 5—Computer arithmetic system.

transit times. One path is from the *MQ* register, through the shifter to the decoder, through the decoder to the shift control register or to the multiplicand true-complement control trigger. A second path is from the shift control register or the shift counter register through the shift counter adder, and back to the shift counter register. The third path is from the *MQ* register, through the shifter to the main adder, and through the main adder back to the *MQ* register. It will be assumed initially that the third path is the longest.

It has already been shown that most of the time required in an adder is required for propagation of carries, and various methods have been described for reducing this. The most efficient of these reduced the time to 12 transit time units for a 50-bit adder for a component increase of 59 per cent. Four of the 12 units are due to the basic adder, and 8 are due to carry propagation.

Multiplication Using Carry-Save Adders

When successive additions are required before the final answer is obtained, it is possible to delay the carry propagation beyond one stage until the completion of all of the additions, and then let one carry-propagate cycle suffice for all the additions. Adders used in this manner are called carry-save adders.

A carry-save adder consists of a number of stages, each similar to the full adder shown in Fig. 1. It differs from the ripple-carry adder in that the carry (*R*) output is not connected directly to the next-higher-order stage

of the same adder, but goes to an intermediate register or other device in the same manner as the sum (S) output. Thus a carry-save adder has three inputs which, as far as use is concerned, may be considered identical, and two outputs which are not identical and must be treated in different manners.

The procedure for adding several binary numbers by using a carry-save adder would be as follows. Designate the inputs for the nth bit as A_n, B_n, and C_n, and the outputs for the same bit as S_n and R_n, where S_n is the sum output and R_n is the carry output. In the first cycle enter three of the input numbers into A, B, and C. In the second cycle enter the S and R obtained from the previous cycle into A and B and the fourth input number into C. In this operation S_n goes into A_n, but R_n goes into B_{n+1}, where B_{n+1} is in the next higher-order bit position than B_n. This is in accordance with the customary rule for addition that a carry resulting from adding one column of figures is added into the next higher-order column. The third cycle is the same as the second, etc. This is continued until all of the input numbers have been entered into the adder.

Carry propagation may be performed in either of two ways. Since each add cycle advances all carries one position, add cycles as already described may be continued with zeros being entered into the third input each time until the R outputs of all stages become zero. The alternative is to enter S and R into a carry-propagate adder and allow time for one cycle through it. This carry-propagate adder may be completely separate from the carry-save unit, or it may be a combined unit with a control line for selecting either carry-save or carry-propagate operation.

Before carry-save adders can be used in the multiplication loop, it is necessary to know the answers to these questions: 1) How should they be used? 2) How much additional equipment is required? 3) How much time will be saved? Assume that the circuit shown in Fig. 5 is modified by changing the adder to a CP/CS adder which is so designed that the ability to operate as either a carry-save or a carry-propagate adder does not cause it to be any slower when operating in the carry-propagate mode than is a comparable adder without this feature. Such an adder can be constructed at an additional component cost of about 50 per cent of the number of components in the corresponding ripple-carry adder. Also, since the partial product will now become a partial sum and a partial carry, and since the latch-register and shifter presently shown can only handle one of them, a duplicate latch-register and shifter must be provided for the other.

Figuring in necessary gates and mixing circuits, and allowing the equivalent of four levels for rise time, skew, and uncertainties in the latch driver power circuits, the data path loop contains fourteen levels besides those in the adder. Also, for the system shown in Fig. 5, no speed advantage is gained by making the main adder faster than the path through the decoder and shift-counter-adder. The latter will be in the neighborhood of eleven levels, seven for the adder and four for the complete decoder. Eleven levels, however, can be obtained at considerably less cost in equipment with the carry-propagate adder with full look-ahead. From this it may be concluded that there would be very little, if any, time gain and considerable additional expense if the adder in Fig. 5 were changed to a CP/CS adder with the necessary associated changes.

The above does not mean that faster multiplication cannot be obtained through the use of carry-save adders. It merely indicates that that particular method of applying it would not produce the desired result.

In Fig. 5 the high-speed main adder represents probably about half of the equipment in the complete data path. Figuring the adder as twelve, and the remainder of the path as fourteen, the total loop path is the equivalent of 26 logical levels. If a carry-save adder were connected in series with the present adder, then the total path length would be fourteen plus twelve plus four, or thirty; however, two additions could be performed in each cycle, which would halve the number of cycles. This is, of course, an oversimplified description of the method and its results, but its proper application will permit profitable use of carry-save adders in multiplication.

When two or more adders are operated in series in the performance of multiplication, an attempt to have a variable shifter ahead of each of them will result in a more complicated decoder, longer path length, and considerable additional equipment. For this reason, a fixed-shift type of operation, such as one of those already described, is more desirable than the variable-shift methods. The comparative merits of and requirements for two- and three-bit shifts have already been described, together with the decoding rules for each. The application of carry-save adders will be described in terms of the two-bit shift. Necessary variations in using the three-bit shift will be readily apparent from the previous description.

Fig. 6 illustrates a system that will handle eight bits of the multiplier at a time. It shows three carry-save adders operating in series, with the two outputs of the last of these going to a carry-propagate adder. One of the three inputs to CSA 1 is the partial product from the previous cycle. The other two are multiples of the multiplicand determined by decoding two groups of multiplier bits. Two of the three inputs of CSA 2 are required for the two outputs of CSA 1, leaving one for a multiple of the multiplicand obtained by decoding the third group of the multiplier. In a similar manner, CSA 3 provides an input for a fourth multiple. The two outputs of CSA 3 go to the inputs of the carry-propagate adder, and the single output of the CPA goes to the main latch-register as the partial product for the next cycle. The modification of the decoding of the first group for the first cycle is used as was described, so that the true value of one times the multiplier can be used

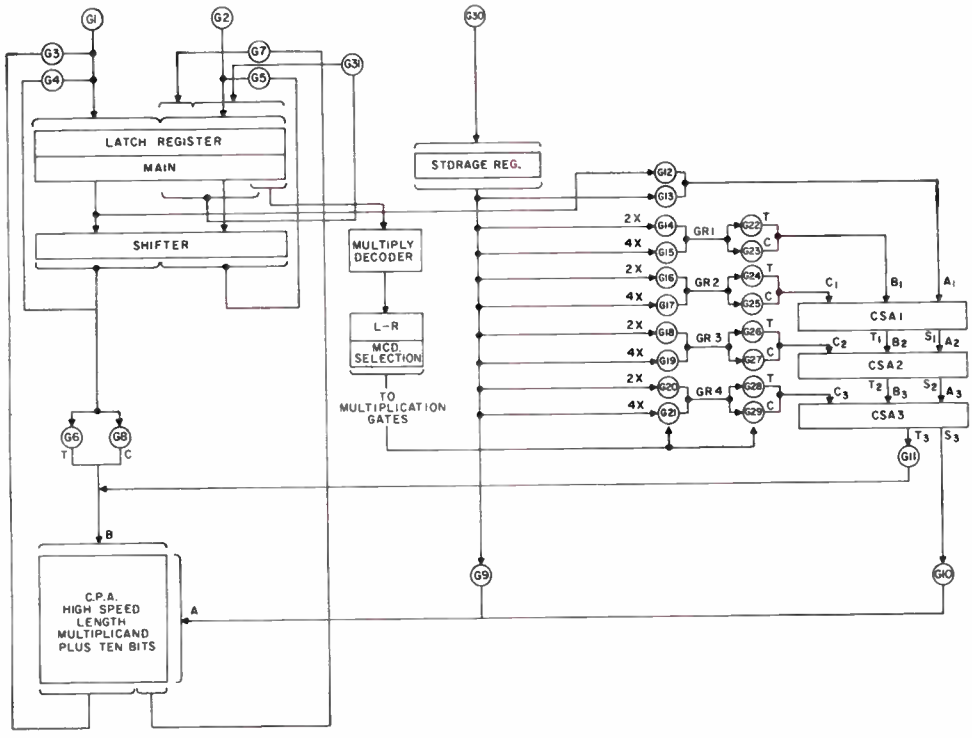


Fig. 6—High-speed multiplication system.

when the low order bit of the multiplier is a *one*. Entry for this is shown as G13.

The details of one cycle of the multiplication of two 16-bit binary numbers are illustrated in Fig. 7. During the first add cycle a 16-bit number is being multiplied by an 8-bit number. This may give a true result not exceeding 24 bits in length. Therefore a *one* in position 25 will indicate a complement partial product. One times the multiplicand, when required, goes into positions 1–16 of the A input of CSA 1. Decoding of the low-order group of the multiplier calls for zero, two, or four times the multiplicand to be entered at the B input of CSA 1. This multiple is referenced to position 1 of the adder, which means that two times the multiplicand would go to positions 2–17, while if four times were called for, it would go to positions 3–18. All other positions of this adder input get *zeros* if the input is true, and *ones* if it is complement.

Since the low-order bit of group 2 of the multiplier is two positions to the left of the corresponding bit of group 1, the reference position for determining entry into the adder is also two positions to the left of that for group 1, that is, position 3 instead of position 1. This means that a two times multiple for group 2 will go into positions 3–19, while a four times multiple will go into positions 4–20. Again, unused positions get *zeros* for true and *ones* for complement.

For CSA 2 the A_2 input is the sum outputs (S_1) from CSA 1 carried down in the same columns. The B_2 input is the carry outputs (R_1) of CSA 1, each shifted one column left, which leaves column 1 for the complement forced carry input for group 2. The C_2 input is obtained from decoding group 3, and is referenced to column 5.

For CSA 3 the A_3 input is the sum output of CSA 2 brought straight down, and the B_3 input is the carry output of CSA 2 shifted one position left, which leaves column 1 of B_3 for the complement forced carry entry due to group 3. The C_3 input is obtained by decoding group 4, and is referenced to column 7. The sum outputs of this adder go into the corresponding columns of one of the inputs of the carry-propagate adder, while the carry outputs go into the carry-propagate adder shifted one position left. This leaves one entry in column 1 available for the forced carry input associated with group 4. The forced carry associated with group 1 can also be entered into the carry-propagate adder by way of the carry input circuit of position one. Rather than use a special adder connection, this can be done by entering an input into both sides of position zero when the carry input is desired.

For all of the adders, carry outputs from column 25 that would normally go into column 26 of the next following adder are ignored and lost, as it would serve no useful purpose to retain them. Column 25 supplies the required information as to whether the partial product is in true or complement form.

Fig. 7 assumes that each carry-save adder has a length equal to the length of the partial product developed in each cycle. Means for reducing each of these to approximately the length of the multiplicand will be described following a summary of the operating sequence. The sequence is essentially the same for either version.

Step 1: Enter the multiplier into the right half of the

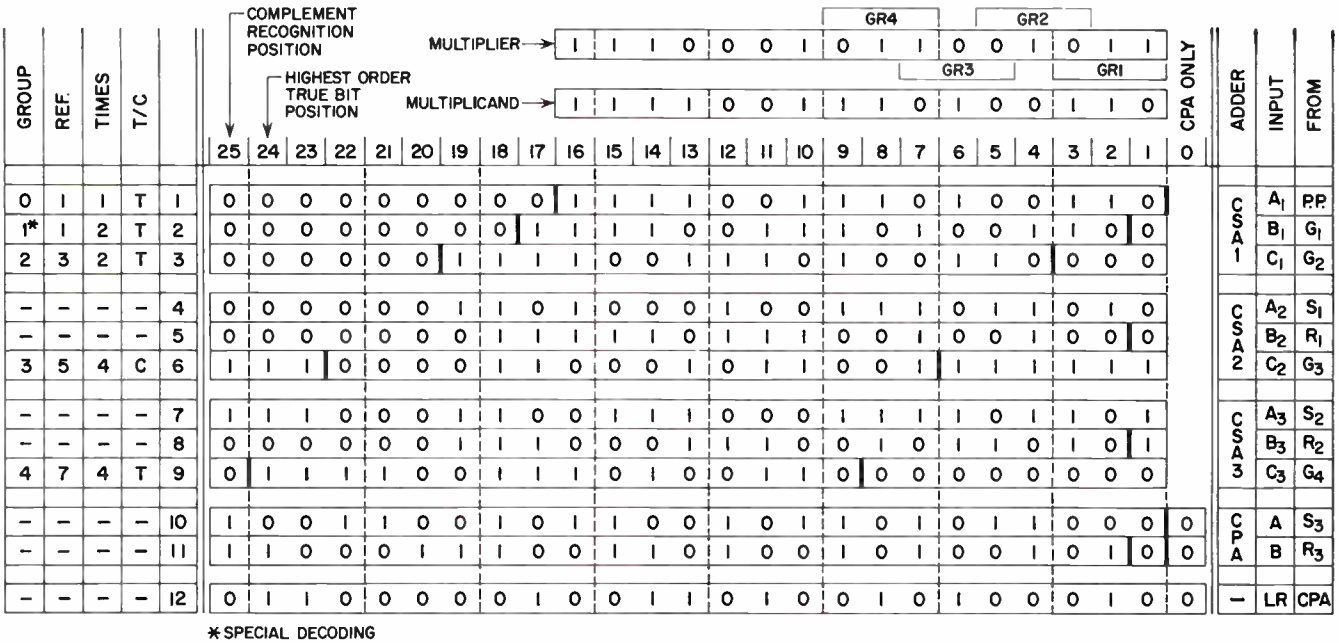


Fig. 7—First cycle of multiplication example using carry-save adders.

MQ register and the multiplicand into the *MD* register. Set the shifter to shift the right half of the *MQ* register eight positions to the right, keeping it at this setting throughout the multiply operation. Clear the multiplicand selection register. Set the first-cycle trigger to cause proper treatment of the low-order bit of the multiplier.

Step 2: Energize the latch-control signal. This sets decoder results into the multiplicand selection register that controls the gates into the carry-save adders, shifts the multiplier right eight positions to discard the low-order eight bits and bring the next group of bits into the decoder, and sets the output of the CPA adder (*zero* in this case) into the *MQ* register.

Step 3: Energize the latch-control signal (after sufficient time has elapsed for the data to have passed through all of the adders). This sets the results of decoding the second set of eight bits of the multiplier into the multiplicand selection register, shifts the multiplier eight positions right, and enters the data from adder output positions 1–25 into positions 9–33 of the *MQ* register. The low-order eight bits of this partial product are in their final form. These are in positions 9–16 of the register. Therefore, on this cycle, the entire adder group is effectively shifted eight positions, which means that data from register positions 17–33 will go to the $.I_1$ input of CSA 1 positions 1–17. Since position 33 contains a *zero* if the partial product is true and a *one* if it is complement, input positions 18–25 of $.I_1$ will be set to agree with the input to position 17.

Step 4: Energize the latch-control signal. This sets the decoder output into the multiplicand selection register (has no meaning since multiplier was shifted out of register by Step 3, but no advantage is gained by suppressing it), shifts the partial product that was in positions 9–16 of the *MQ* register into positions 1–8, and enters the remainder of the product from the carry-propagate adder into positions 9–33. Note that the data that was in positions 17–33 is replaced, and not shifted elsewhere. This completes the multiplication.

Component Reduction with Carry-Save Adders

A carry-save adder takes in three signals and gives out two. If the number of inputs is reduced to two, the number of outputs still remains at two. Therefore, when two or more carry-save adders are used in series, any bit positions which always have *zeros* for one of the three inputs may be omitted. This eliminates two outputs from the omitted adders, thus vacating inputs to two positions farther down the adder chain. The two inputs that would have gone to the omitted adder positions can then go to these two positions. An input may be moved from any one place in the chain of adders to any other place as long as it is always kept in the same column.

When the two's complement of a binary number is desired, the one's complement is obtained, and then a *one* is added to this in the column of the lowest order bit. The column into which the *one* is entered may vary from this if the column selected is the same as, or of a lower order than, the column containing the lowest-order *one* in the true value of the number, and also if the *zeros* to the right of the selected column are not inverted when forming the one's complement of the number.

The application of these two principles will permit the elimination of a number of low-order positions from the adders shown in Fig. 7. This is illustrated in Fig. 8.

Since the input C_1 never needs to have anything except *zeros* in positions 1, 2, and 3, and since nothing needs to be added into these columns in any other

adder, the inputs for these columns that would normally go to A_1 and B_1 may be shifted down to the CPA inputs and all carry-save adder positions for these columns eliminated. The forced-carry input for group 1 remains the two CPA inputs in column zero. In Fig. 8, terminations for the adders are indicated by double vertical lines. Positions outside these terminations are designated by numbers in circles, and the position to which these are transferred is designated by the same number in a hexagon.

The three inputs for CSA 2 are the sum and carry from CSA 1 and the multiple obtained by decoding group 3. The lowest-order column required by the latter is six, which means that the inputs to columns 4 and 5 may be transferred. It should be noted that with the group 2 multiple ending at column 4, the forced carry for this was moved to column 4 of B_2, and is now being transferred to the same column of CPA input B. CSA 3 is then treated in a similar manner. Altogether, these modifications have eliminated fifteen adder positions from the low-order ends of the adders.

The modification of the high-order end of the adders is based on the fact that, since the inputs are staggered, the adders will have a number of high-order positions containing either a string of *ones* or a string of *zeros*. When two of the three inputs meet this condition, these two inputs may always be replaced by a single input, which reduces the total number of required inputs to two. As has already been shown, when this condition exists, these stages of the adder may be eliminated, and the pair of inputs moved down to the next adder in the chain. The operation of this is illustrated below for the various combinations that may occur:

Two Complement Inputs

1	1	1	1	′	1	*	X	X	X	X	A_1
1	1	1	1	′	1	*	X	X	X	X	B_1
D	E	F	G	′	H		X	X	X	X	C_1
1	1	1	1	′	S		S	S	S	S	A_2
D	E	F	G	′	R		R	R	R	R	B_2

One Complement Input

1	1	1	1	′	1	*	X	X	X	X	A_1
0	0	0	0	′	0	*	X	X	X	X	B_1
D	E	F	G	′	H		X	X	X	X	C_1
$\overline{H}$	$\overline{H}$	$\overline{H}$	$\overline{H}$	′	S		S	S	S	S	A_2
D	E	F	G	′	R		R	R	R	R	B_2

No Complement Inputs

0	0	0	0	′	0	*	X	X	X	X	A_1
0	0	0	0	′	0	*	X	X	X	X	B_1
D	E	F	G	′	H		X	X	X	X	C_1
0	0	0	0	′	S		S	S	S	S	A_2
D	E	F	G	′	R		R	R	R	R	B_2

The three inputs shown together represent the inputs as they would be if the complete adder were used. The asterisks in two of the inputs indicate that there are never any high-order true bits to the left of this point for these two inputs. The apostrophes indicate the point at which it is desired to terminate the adder shown with three inputs. The two inputs below are two of the three inputs of the next following adder. For columns to the right of the termination point of the first adder, the inputs to the following adder are the sum (S) and carry (R) outputs of the adder above. To the left of the termination of adder 1, the B_2 input of adder 2 becomes what would have been the C_1 input of adder 1 for the same columns. Note that the carry output of the highest-order column of adder 1 after it is terminated does not go into the next higher order of column B_2, as this position is occupied by G from C_1. The corresponding A_2 inputs to adder 2 are the same for all bit positions to the left of the termination point of adder 1, and are determined from the three inputs to the highest order column of the terminated adder 1.

Fig. 8 illustrates the effect of applying this method to the adders of Fig. 7. In CSA 1, input A_1 is determined by its true or complement condition starting with column 17, B_1 with column 19, and C_1 with column 21. It is therefore possible to terminate this adder with position 19, and move the normal C_1 inputs for columns 20 and 21 to the corresponding columns of C_2.

The normal full adder used for each position of the CSA contains the following logic:

$$S = (A \veebar B) \veebar C, \tag{4}$$

$$R = (A \veebar B)C \vee AB. \tag{5}$$

For the high-order column of the terminated adder, in this case column 19, this is modified to the following:

$$S = (A \veebar B) \veebar C, \tag{6}$$

$$D = (A \veebar B)\overline{C} \vee AB. \tag{7}$$

In (4), (5), and (6), the terms A, B, and C may be applied to any of the three inputs to the adder. This is not true in (7), where the terms A and B refer to the two inputs determined by the fact that they are in true or complement form, while C refers to the data input. D describes the input that goes to all higher-order positions of the next adder, and for that adder it may be treated as are those positions whose input is determined by knowledge of whether the input is true or complement.

By continuing with this procedure, CSA 2 may be terminated at position 21, the position 21 circuit being modified as described above; and CSA 3 may be terminated with column 23, the position 23 circuit also being modified.

The three carry-save adders as originally described in Fig. 7 required a total of 75 individual full adders. The same adders with the modifications described require 45 full adder units plus three modified units, a saving of 27 units.

For the operation described, the length of the carry-propagate adder had to exceed the length of the multiplicand by two more than the length of the section of the multiplier handled during each cycle. If this additional length is not required for other operations, and if the main part of the adder uses fully carry look-ahead, the reduced path length for the low-order bits in the carry-

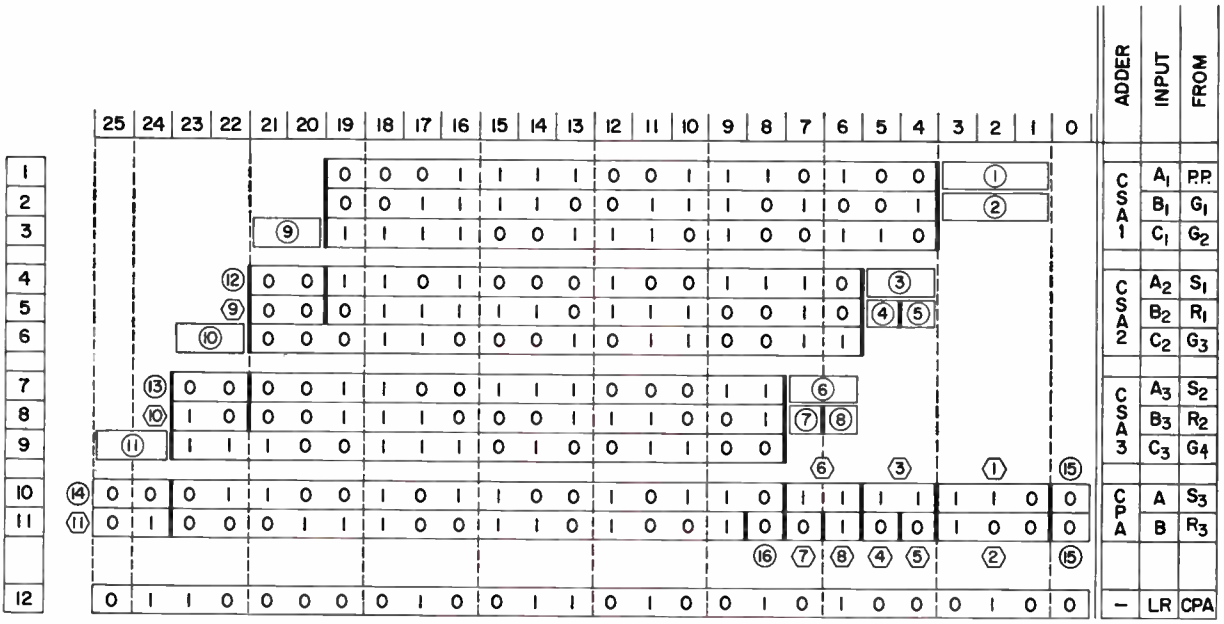


Fig. 8—Modified high-speed multiplication adder system.

save adders resulting from the modifications made to save components permits the use of a ripple-carry adder for most of the extension to increase the length of the main adder without causing any loss in speed.

From the information given, the modifications required to permit the use of three-bit multiplier groups instead of two-bit groups are obvious. The question of how many carry-save adders to connect in series is a matter of economics to be decided for a particular application. The example given was intended merely to help describe the general method, and many modifications of it to suit special conditions will be readily apparent.

Binary Division

There are several methods, of varying complexity and speed, by which division may be performed in a computer. The implementing of a particular method will vary between computers because of differences in circuits and machine organization. It is the intent here to discuss primarily basic methods, and to illustrate these methods, when required for clarity, with a particular type of machine organization. The characteristics of this type were described in the Introduction.

The time required to perform a division is proportional to the number of additions required to complete it, and the methods that will be described for increasing speed will be primarily concerned with the reduction of the required number of additions. These methods will all use a variable length shift, and the number of additions required for any particular example will be dependent on bit distribution.

For all methods of division it will be assumed that prior to the start of the actual division the divisor is so positioned in the divisor register that it has a *one* in the highest-order position of the register. It will also be assumed that the divisor and dividend are binary fractions with the binary point located just to the left of the high-order position. Thus the divisor will always have a numerical value less than one, but equal to or greater than, one-half. These assumptions do not limit the application of the principles of operation to be described, and they simplify the description.

Since all of the methods to be described involve variable shifts, it will always be assumed that a shift counter of some type is included, that this counter is set initially with the number of quotient bits to be developed, and that any shift-determining circuits include means for comparing the shift called for against the number still allowed by the shift counter and then acting on this information according to the rules that will be developed for the particular method.

In all descriptions the term dividend will be used to mean both the initial and partial dividend, while the term remainder will mean the final remainder after the quotient is completely developed.

Fig. 5, which was used in the description of multiplication, will also be used as the basic circuit for describing division. Any modifications required by a particular method will be described. All operations start by setting the dividend into the *MQ* register, the divisor into the *MD* register (including normalization of the divisor if it is not already in this condition), and the quotient length into the shift counter (which is assumed to count down). The high-order bit position of the dividend (with a shifter setting of zero) and the high-order bit position of the divisor enter the same column of the adder unless stated otherwise. Dividend shifting is to the left, which clears the right end of the *MQ* register as the operation proceeds. The quotient is developed at the right end of the *MQ* register and shifted along with the dividend. The dividend decoder is assumed to

be on the high-order end of the adder output, which means that the initial operation always starts with a forced zero shift, following which the decoder takes control of the shifting.

Some additional general rules that apply to all methods, particularly those that deal with starting and terminating a division, will be discussed following the detailed descriptions of the several methods.

Division Using Single Adder, One-Times Divisor, and Shifting Across Zeros and Ones

Assume a dividend in true form. Since the high-order bit of the divisor is required to be a *one*, if the high-order bit of the dividend is a *zero*, the divisor is obviously larger than the dividend which will result in a *zero* quotient bit. A *zero* may therefore be placed in the quotient, and the dividend and quotient each shifted left one position before any addition is performed. If there are n leading *zeros*, and the decoder can recognize them, n positions may be shifted across in one operation, a *zero* also being inserted in the quotient for each position shifted.

With the dividend true and the high-order bit a *one*, an addition must be performed to determine whether or not the dividend is larger than the divisor. If the result of the operation is true, the dividend was larger, and a *one* is entered in the quotient. If the result is complement, the dividend was smaller than the divisor, and a *zero* is entered in the quotient. In either case, the result of the addition replaces that part of the previous dividend in the MQ register that was used in the addition. If the result of the addition was a complement number, this will now make the entire new dividend a complement number, even though part of it did not go through the adder.

Shifting the dividend one position left is equivalent to dividing the divisor by two with respect to the original dividend. For a true dividend with a high-order *one*, if one times the divisor results in a *zero* in that position of the quotient (divisor larger than dividend), then one-half of the divisor (next shift position) will always result in a *one* in the following bit position of the quotient. (Dividend is equal to or greater than one-half, while one-half of divisor must be less than one-half.) If, after the first addition, the dividend had been returned to its original value, then, using the first addition as a point of reference, the second addition would have given a true result (indicating the *one* in the quotient) with a value equal to the original dividend minus one-half of the divisor. If, instead of returning to the original dividend, shifting, and adding complement, the complement result of the previous addition had been retained and shifted, and the true value of the divisor added to it, the result would have been (original dividend minus divisor) plus (one-half divisor). This would also be a true final result having the same value as was obtained by the previous method.

Assume that a partial division has been performed yielding a partial quotient of 01111 and a corresponding partial dividend. This result could have been obtained by any of the following series of operations:

dividend $+(-1/2-1/4-1/8-1/16)$ divisor,
dividend $+(-1.0+1/2-1/4-1/8-1/16)$ divisor,
dividend $+(-1.0+1/4-1/8-1/16)$ divisor,
dividend $+(-1.0+1/8-1/16)$ divisor,
dividend $+(-1.0+1/16)$ divisor.

These are all equal to dividend minus 15/16 divisor. From this it may be stated that if a complement result is obtained under the condition that it is known that the next succeeding quotient bit is a *one*, then as many positions of the dividend may be shifted across, a *one* being entered in the quotient for each position shifted across, as is known will still result in a true dividend following the addition.

Since the high-order position of the divisor, in its true form, always contains a *one*, a true result will always be obtained if the high-order bit position of the complement dividend contains a *one*. This justifies shifting across all except the last *one* in a string of high-order *ones* in a complement dividend, together with the entering of a *one* in the quotient for each position shifted across. It is also known that if an addition is performed without shifting across the final *one*, a true dividend will always be obtained together with another *one* in the quotient. If the complement result had been shifted one position farther, the new dividend obtained would be the same following the addition of the true divisor as would have been obtained following a one-position shift of the true dividend and the addition of the complement of the divisor. Thus, it is evident that with either true or complement dividends it is only necessary to perform an addition when it is not evident what the quotient bit should be. From this the following operating rules may be stated.

1) When the dividend is true, shift across any leading *zeros*, entering a *zero* in the low-order end of the quotient for each position shifted across except the last; then add the complement of the divisor.

   a) If the result is true, enter a *one* in the low-order position of the quotient, then shift across *zeros*.
   b) If the result is complement, enter *zero* in the low-order position of the quotient, then shift across *ones*.

2) When the dividend is complement, shift across any leading *ones*, entering a *one* in the low-order end of the quotient for each position shifted across except the last; then add the true divisor.

   a) If the result is true, enter a *one* in the low-order position of the quotient; then shift across *zeros*.
   b) If the result is complement, enter a *zero* in the low-order position of the quotient; then shift across *ones*.

If the decoder calls for a larger shift than can be ob-

tained from the shifter in one operation, use the maximum shift available and suppress both the true and complement entry of the divisor to the adder. This will pass the high-order part of the shifted dividend through the adder with zero added to it so that it is available to the decoder. If the dividend is complement, the output of the adder following this will be complement, which would normally result in the setting of a *zero* in the low-order position of the quotient. However, this is in the middle of a shift across *ones*, not an addition to determine the proper quotient bit following a shift, and the dividend only goes through the adder because of the necessity of making it available to the decoder. Therefore, in this case, the low-order bit of the quotient following the shift must be set to agree with the bits being shifted across. The same control that suppresses the entry of the divisor into the adder can also control this.

Some special rules are required to terminate the division and to insure that the final remainder will be in true form. These are listed below.

1) Dividend true, shift called for by decoder larger than allowed by shift counter. Treat in same manner as when shift called for is greater than capacity of shifter. Make shift allowed by shift counter, suppress entry of divisor into adder, set low-order bit of quotient to agree with bits being shifted across. This will complete the division.
2) Dividend true, shift called for by decoder equal to that allowed by shift counter. Treat in the normal manner. If resulting adder output is in true form, division is complete with its entry into the register. If the resulting adder output is in complement form, one additional cycle is required to get remainder into true form. See 4) below.
3) Dividend complement, shift called for by decoder equal to or greater than that allowed by shift counter register. Use allowed shift and proceed in normal manner. If the resulting remainder is in true form, division is complete. If the resulting remainder is in complement form, the resulting quotient is complete, but one additional cycle is required to get remainder into true form. See 4) below. The latter condition can only occur when the shift called for and the shift counter register are equal.
4) Dividend complement, shift counter register is zero. Take zero shift, add the true value of the divisor, suppress entry from adder output into low-order bit position of quotient as the bit there is already correct (*zero*) and the true output of the adder would change it to a *one*.

If the following binary division is performed according to these rules, it will require fourteen add cycles to complete the operation:

$$110,110 \overline{)10,111,111,110,111,001,111,000,100,100} \quad 011,100,011,011,001,001,010,110$$

To compare this with the inverse operations required for multiplication, the quotient is shown below with the various additions and subtractions used shown above the corresponding bit positions, and the corresponding operations as determined from the multiplication rules shown below.

```
−     +     −  +  −  +     −    −+  −+−    +o [14]
011,  100,  011,  011,  001,  001,  010,  110
−     +     −     +  +     −     −    −−    +o [11]
```

Division Using Double Adder and One-Half, One, and Two Times Divisor

If a quotient contains a string of *zeros* followed by a string of *ones*, it is possible to shift across the *ones* only if the addition made after the shift across the *zeros* resulted in a complement dividend. If the result was a true dividend, then it is necessary to make a separate addition for each *one* in the string. This means that in some instances better results would have been obtained if the addition had been performed one position sooner than the position resulting from following the shift rules. This condition is most likely to occur with a small divisor, as a small divisor is less likely to produce a change in the sign of the dividend than a large divisor.

When a quotient contains two strings of *ones* separated by a single *zero*, more efficient operation will be obtained if it is always treated as one string of *ones* with an interruption. This may be seen by comparing the fourth and fifth operations of the previous divide example with the fourth operation of the potential divide system obtained by an inversion of the multiplication rules and shown for comparison. In this case, it is desired that the addition at the end of the first group of *ones* produce a complement result which will supply the single *zero* for the quotient and leave the remainder in complement form for shifting across *ones* again; the inverse applies if the quotient is two strings of *zeros* separated by a single *one*. To obtain this condition, it is sometimes necessary to perform the addition one position later than the position given by the shift rules. However, if this extra length shift is taken at other times it may produce incorrect results. The failure to obtain optimum operations under these conditions is most likely to occur when the divisor is large because a large divisor has a greater probability of producing a change in the sign of the dividend.

It has been shown that the efficiency of the division operation may be improved if, on certain occasions, the addition following a shift could be made with the divisor one position to the left of the normal position, and on

other occasions one position to the right of the normal position. By normal position is meant that position reached by shifting across all leading *ones* for a complement dividend or across all leading *zeros* for a true dividend. The divisor used in the normal position is designated as one times divisor, left of normal position as two times divisor, and right of normal position as one-half times divisor.

One method of obtaining this improvement is by double addition. It requires that the main adder be slightly longer than twice the length of the divisor, or that there be two adders available. The procedure is to perform two additions simultaneously and then use the result that produces the largest shift. If a double-length adder is available, the two additions may be performed in it as long as there is at least one position with no inputs to it between the two operations. One addition will always be performed with the divisor located, with reference to the dividend, as called for by the shift decoder. The other addition will be performed using twice the divisor if the two high-order bits of the divisor in its true form are 10 (value of divisor less than three-fourths), and one-half the divisor if the two high-order bits are 11 (value of divisor equal to or greater than three-fourths). Thus a small divisor uses the larger multiple, while a large divisor uses the smaller multiple for the auxiliary addition.

The circuitry required is similar to that of Fig. 5 except that the adder size is increased, gates are added to enter the dividend into the other half of the adder also, and to select two times or half times the divisor for entry there, the decoder is increased to decode and compare the two results, and a gate is added to permit a choice of the two outputs.

Although the two additions may be performed in two parts of one adder, the two parts will be called adder A and adder B. Adder A will correspond to the adder described in the previous method, while adder B will be the alternate adder. The output of adder B will be used only if its use results in a greater shift than would result from using adder A. If the shifts called for by the two adder outputs are the same, the adder A results will be used.

If the previously described example were performed using this method, the resulting operations would be exactly the same as those obtained by using the inverse of the multiplication rules. The rules for quotient development and division termination are very similar to those for the system using a single length adder, and will be developed when it is described.

Fig. 9 is a table showing all possible results that can be obtained for a five-bit true divisor and complement dividend under the restrictions that a true divisor always has a high-order *one* and a complement dividend is always used following shifting across all leading *ones*, which means that it will always have a high-order *zero*. A corresponding table can be prepared for complement divisor and true dividend. If this is done and the two are compared, it will be found that for the same position the result on one table will be the exact inverse of that on the other table. For example, at column 3, row 10, of Fig. 9 the result is 00110, while the corresponding position of the other table would be 11001. The number of positions to be shifted is the same in both cases. The information of primary interest to be obtained from these tables is the number of shifts, which is shown in Fig. 10.

From this table it is apparent that points of maximum shift lie along the diagonal representing equal values for divisor and dividend. Also, if random distribution of divisor bits between problems and dividend bits between and within problems is assumed, then the average shift per cycle will be $651/256 = 2.54$ for a five-bit divisor used with a shifter capable of handling shifts of five or less. (It can be shown that the distribution of bits within a dividend does not remain completely random as the division progresses. However, the variations will not be sufficiently great to invalidate the results of the comparisons of efficiencies of different methods of division based on the assumption of complete randomness.)

Fig. 11 shows a table of shifts that may be obtained when using one-half times the divisor or two times the divisor. Both are shown on the same table, half of the table being used for each. These results apply both for dividend complement with divisor true and for dividend true with divisor complement. On this and the preceding figure, the pattern of shifts along any row should be noted, as each row contains a section of the pattern. The pattern goes both ways from the line of maximum shifts, and is one "5", one "4", two "3's", four "2's", eight "1's", and all that follow "0". Any selection system used must not permit the selection of zero shift during normal operation, as this will result in an error in the problem.

When one-half or two times the divisor is used, the dividend is positioned in the same manner as if one times the divisor were to be used; then the divisor is entered into the adder shifted one position to the left or right of where it would have been for one times. The columns of the output of the adder that are examined to determine the next shift are the same ones that would have been examined had one times the divisor been used. When preparing the table and using one-half times the divisor, the low-order bit of the divisor is lost as a result of the right shift. This would not be the case in an actual operation, as the adder would have been extended by one position and an additional bit of the dividend would have been brought into the adder. When two times the divisor is used, the high-order bit of the original divisor is entered into the overflow position of the adder, but for all the combinations for which two times the divisor would be used, this combines with the complement dividend to produce a true divisor with no overflow. Therefore this five-bit remainder used for the chart is correct.

Examples of the use of one times the divisor are

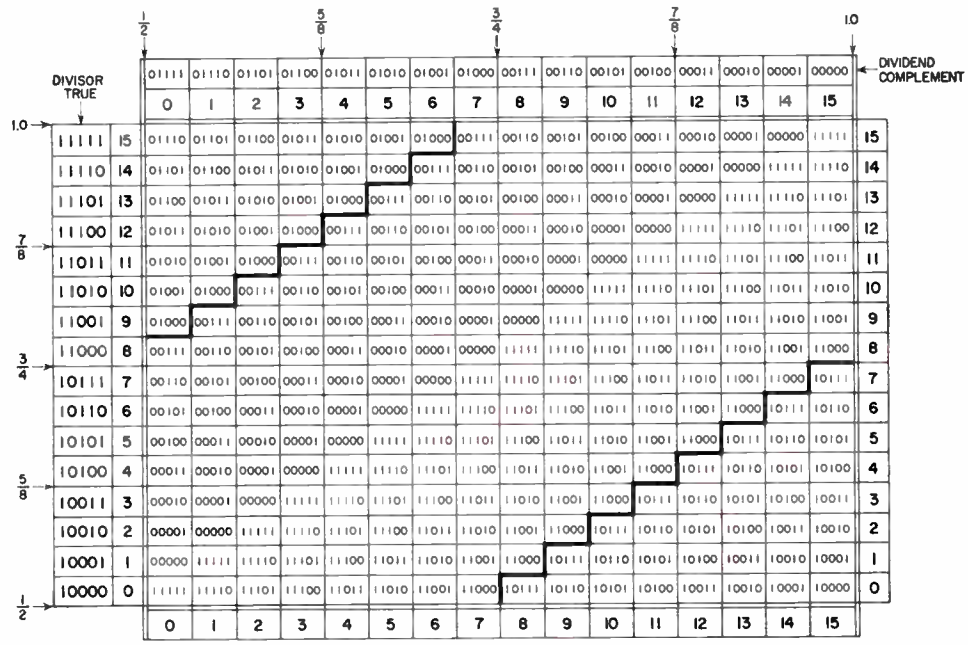
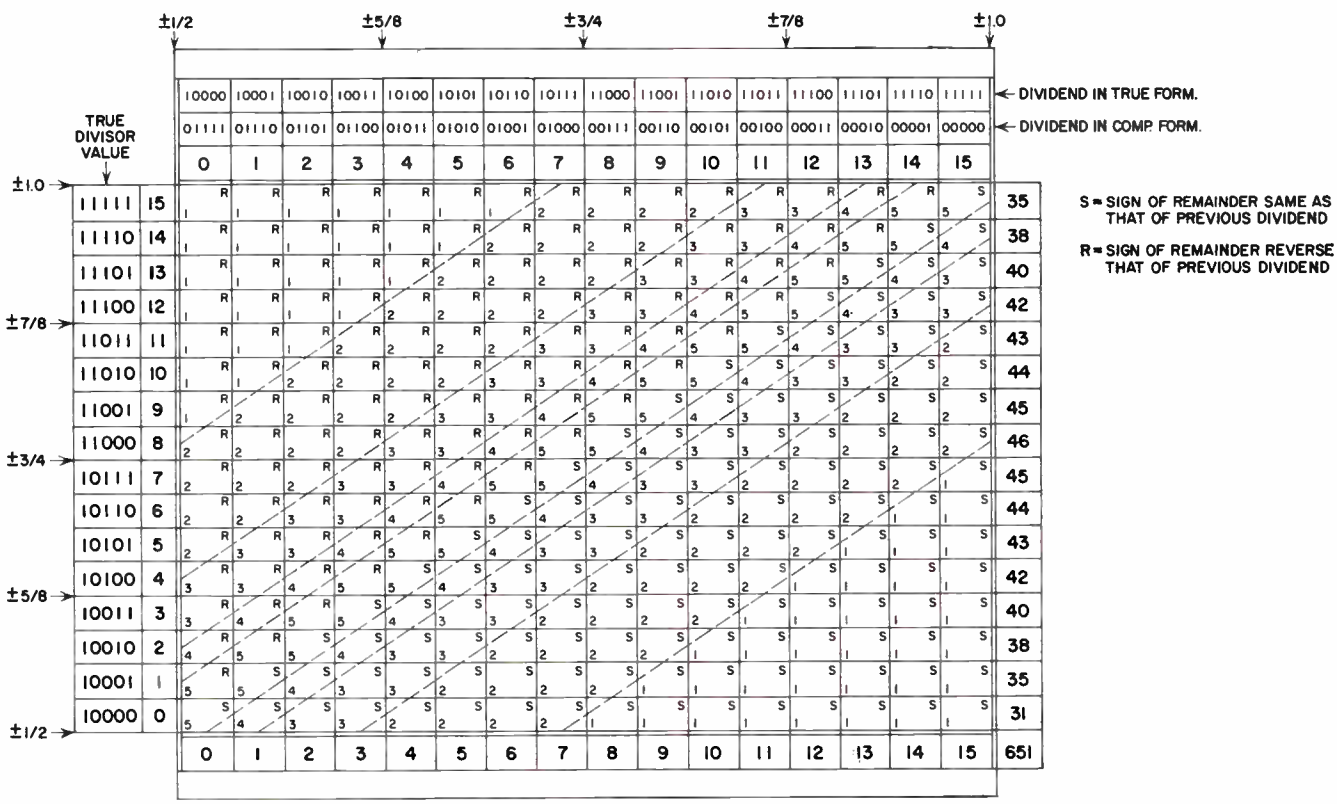


Fig. 9—Division table, divisor true, dividend complement, using one times divisor.



	SHIFTS					
SHIFT LENGTH	1	2	3	4	5	TOTAL
NUMBER	64	80	52	29	31	256
PERCENT	25.0	31.3	20.4	11.3	12.0	100.0

$\frac{651}{256} = 2.54$ BITS/CYCLE

$\frac{48}{2.54} = 19.0$ AVERAGE SHIFT CYCLES FOR 48 BIT QUOTIENT WITH 5 BIT DIVISOR

Fig. 10—Division table using one times divisor with five-bit divisor.

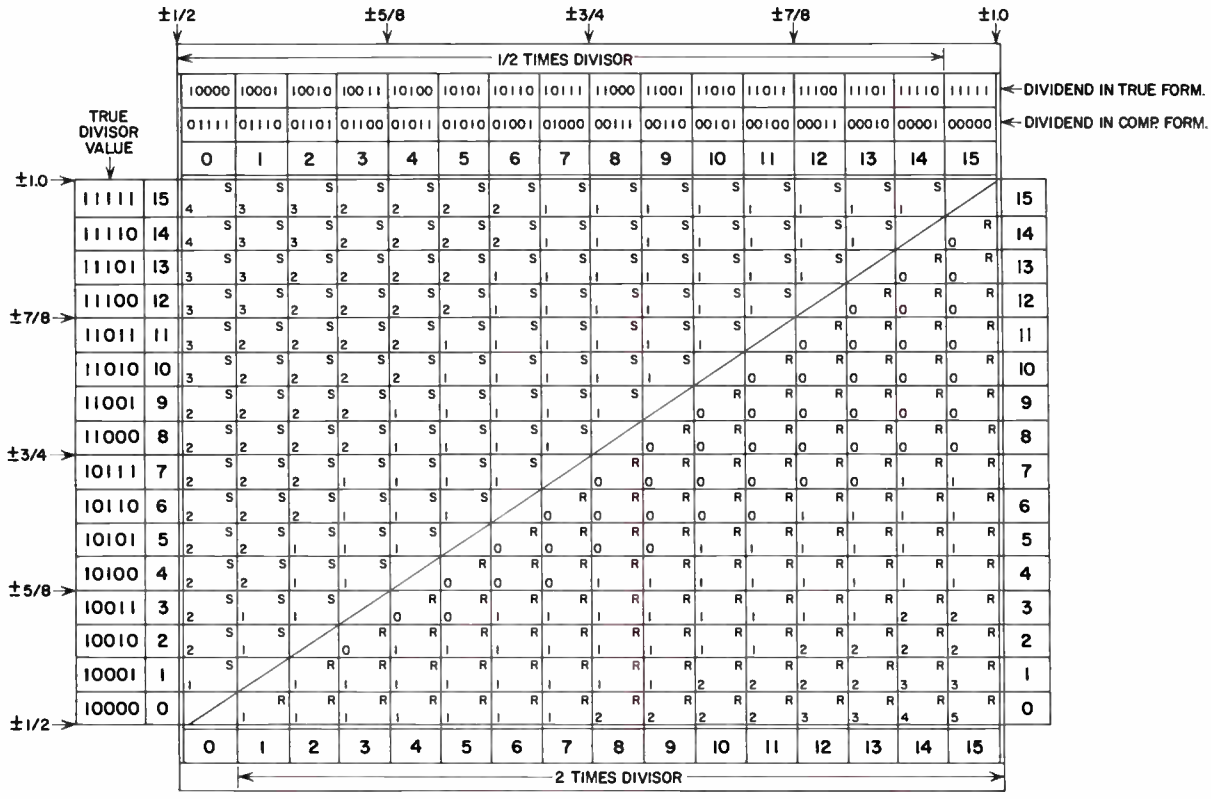


Fig. 11—Division tables using 2.0 and ½ times divisor.

shown in Table V, followed by examples of one times and one-half times. The examples on the left use one times, while the top right uses two times and the bottom right one-half times. The part of the result that is used in the figures is to the right of the binary point in each case. The part to the left is shown indirectly by the indication of true or complement result. The figure numbers, column numbers and row numbers refer to the table locations of the examples. The underlined part of the result indicates the amount of shift that would result in each case.

TABLE V

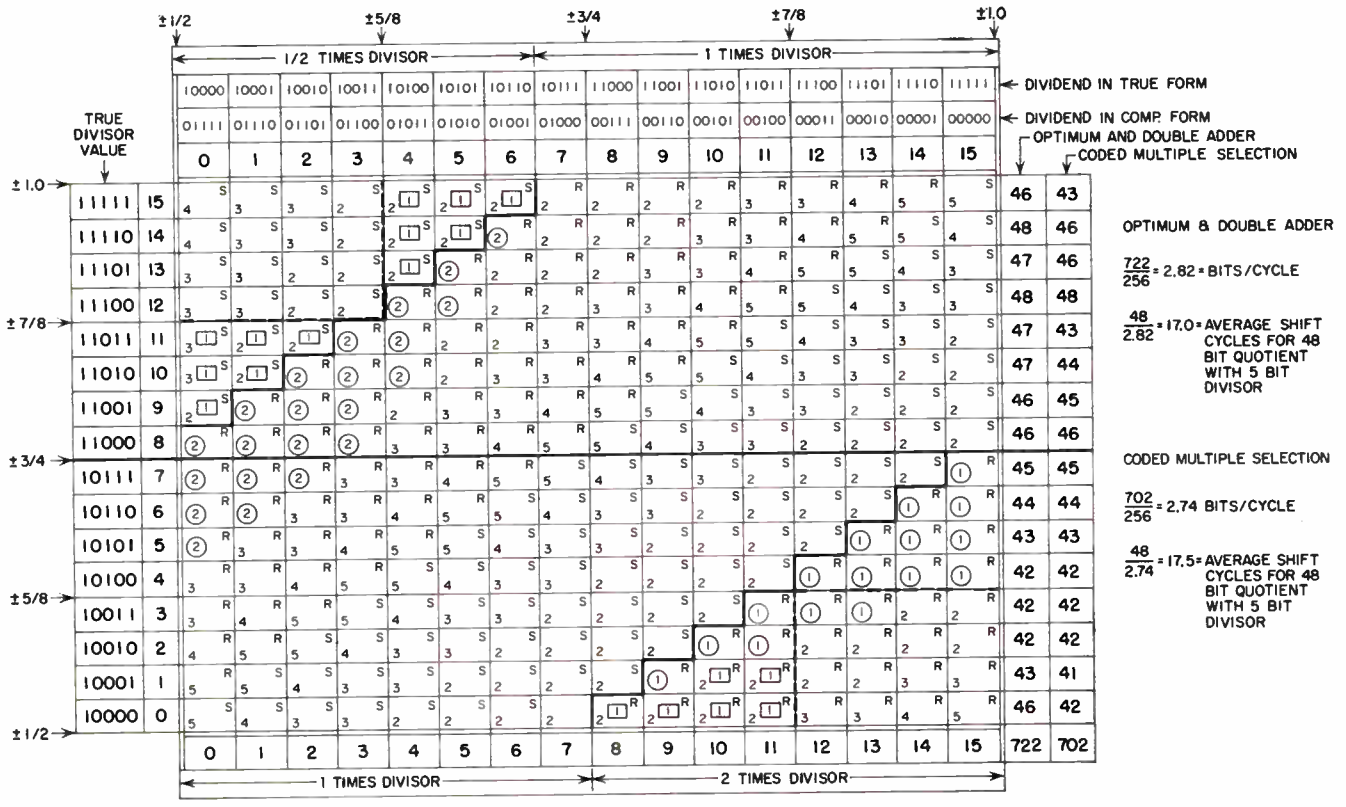
Figs. 9 and 10	Fig. 11	
11 · 00010 00 · 10001	11 · 00010 01 · 00010	Column 13 Row 1
11 · 10011	00 · 00100	
11 · 01110 00 · 11101	11 · 01110 00 · 01110	Column 1 Row 13
00 · 01011	11 · 11100	

Fig. 12 is obtained by replacing all of the positions calling for a shift of one on Fig. 10 with the shift called for on the corresponding position of Fig. 11. The three sections are shown separated by heavy stepped lines. The circled numbers represent shifts that are the same on both figures. This represents the optimum combination that can be obtained when using one-half, one, and two times the divisor, and gives an average of 2.82 bits per cycle.

The heavy line between rows 7 and 8 represents the division that was made between the use of half times and two times divisor in the double adder method. As may be seen, the optimum use for each multiple is within this division, which means that the double-adder method of division will give the same results as are obtained from optimum use of these particular divisor multiples. An alternate selection rule which may be used with the double adder method for these particular multiples is: If the output of the alternate adder does not call for a shift of two or more, use the output of the adder having the one times divisor input. This avoids the need for any compare circuits, and also gives correct results.

Division Using Single Adder With Half, One and Two Times Divisor

If only a single length adder is available, the use of the three divisor multiples to improve efficiency is still possible, although the improvement may be somewhat less. In this case the selection must be made by examining, or decoding, the high-order bits of the divisor and dividend before each operation to determine what multiple to use. The degree of improvement will be dependent on the number of bits included, as will the complexity of the decoding system and the time required by it. The selection must be sufficiently accurate that it will never call for a multiple that will result in a zero shift.



	SHIFTS – DOUBLE ADDER						SHIFTS – CODED SELECTION					
SHIFT LENGTH	1	2	3	4	5	TOTAL	1	2	3	4	5	TOTAL
NUMBER	16	110	66	32	32	256	34	94	64	32	32	256
PERCENT	6.2	43.0	25.8	12.5	12.5	100.0	13.3	36.7	25.0	12.5	12.5	100.0

Fig. 12—Division table using 2.0, 1.0, ½ times divisor with optimum coding.

The dashed lines in Fig. 12 that outline rectangles in the upper left and lower right corners indicate what may be expected from very simple decoding. This is based on the following rules: 1) If the high-order bits of the divisor are 111 and the high-order bits of the dividend are either 011 or 100, use the half times divisor multiple. 2) If the high-order bits of the divisor are 100 and the high-order bits of the dividend are either 000 or 111, use the two times divisor multiple. 3) If neither of these conditions exist, use the one times divisor multiple. This gives an average of 2.74 bits shifted per cycle as compared with 2.82 for the double adder.

Quotient Development and Termination When Using 1/2, 1.0, and 2.0 Multiples

When these multiples are used, an additional low-order register position is required. Designate the two low-order positions of this register as X and Y, where X is the position that is normally set by whether the output of the adder is true or complement when one times the divisor is used. Position Y is the next lower-order position in the register.

When the half times divisor is used, it is in the same position with respect to the dividend that the one times divisor would have been had the previous shift been one greater. Therefore the quotient bit determined by the output of the adder when the half times divisor is used must be placed where it will enter the quotient adjacent to position X, which is position Y. The quotient bit placed in position X must be the same that would have been placed there had one times the divisor been used, and will always be the same as the bits shifted across during the preceding shift.

The bit placed in position Y as a result of the use of the half times divisor is a correct quotient bit. In the event that its generation is followed by a shift of one, the information that the half times divisor was used must be stored so that on the next add cycle position X can be set from data that was in position Y instead of from the condition of the adder output.

It should be noted than when the remainder from the use of the half times divisor multiple is decoded to give the number of bits to shift across, the number will always be one greater than would have been obtained had the previous shift been one greater followed by the use of one times the divisor, which puts the end of the shift at the same place in either case.

Whenever the one times divisor is used, position Y is set to agree with the bits that will be shifted across on the next shift. It enters into all shifting operations except shifts of one. It may be shifted across position X,

but never into it (except for the special condition described above).

The two times multiple will be selected only when the one times multiple, if used, would not cause a reversal in dividend sign, but the use of the two times multiple will cause a reversal. Therefore, if the original dividend was true, X is set to a *one;* if it was complement, X is set to a *zero*. Y is set to agree with the bits that are to be shifted across as determined by the output of the adder using the two times multiple. This bit is not preserved in the event of a one-position shift.

The above information is summarized in Table VI.

TABLE VI

Original Dividend	Multiple Selected	X	Y	Y Definite
True	half times	0	1	yes
True	two times	1	1	no
Complement	half times	1	0	yes
Complement	two times	0	0	no

To terminate a division, follow the rules previously given, with the added restriction that if the shift called for is equal to the contents of the shift counter register, the choice of the divisor multiple is limited to the one times multiple.

Division Using Divisor Multiples of Three-Fourths, One and Three-Halves

It was previously stated that the largest shifts occurred along the diagonal of equal values of divisor and dividend. Fig. 11 shows that such diagonals for the half times or two times multiples would each intersect the rectangle at one corner only, the half times going through the corner at which the divisor has a value of 1.0 and the dividend 0.5, and the two times going through the corner at which the divisor has a value of 0.5 and the dividend 1.0. A multiple which would have its high points within the area so that the high values on both sides would be available should give a greater improvement in efficiency. To be of practical use, it should also be easy to generate. Such a multiple is three-halves times the divisor, which can be generated in one addition cycle by adding one times the divisor to one-half times the divisor. Three-fourths times the divisor can then be generated from this sum by shifting.

Fig. 13 shows a shift table obtained when using three-fourths and three-halves divisor multiples with five-bit divisors and five-bit dividends. The line of maximum shifts varies somewhat from the theoretical line because of the limits in size and the effects of truncating the three-fourths times multiple of five bits. Without these limits, the line of maximum shifts for the three-fourths times divisor multiple would go between the points of divisor equal to 2/3 dividend equal to 1/2 and divisor equal to 1.0 dividend equal to 3/4; for the three-halves times divisor multiple, the line would go between the points of divisor equal to 1/2 dividend equal to 3/4 and divisor equal to 2/3 dividend equal to 1.0.

Fig. 14 shows a combination of Figs. 10 and 13 to give the optimum arrangement when using the 3/4, 1.0, 3/2 multiples. The heavy stepped lines show the separation between the areas of use of the three multiples. The circled numbers represent shifts that are the same in the two adjacent areas. The separation line could go on either side of these positions without changing the result. The heavy horizontal line at divisor equals three-fourths represents the separation between the inputs to the alternate adder when these multiples are used in the double adder method, and the numbers in squares in the seven positions below this line indicate the shifts these positions would have as part of the one times area, instead of the three-fourths times area. The optimum arrangement here for the five-bit divisor indicates an average of 3.57 bits per cycle, while the use of these multiples in the double adder method gives 3.51 bits per cycle.

Fig. 15 shows a coding arrangement for multiple selection that gives the same results as are obtained from the double adder method. A simpler coding method, which uses the three-fourths times multiple when the high-order bits of the divisor are 11 and the high-order bits of the dividend are either 10 or 01, and uses the three-halves multiple when the high-order divisor bits are 10 and the high-order bits of the dividend are either 11 or 00, will give an average of 3.37 bits per cycle based on a similar table (not shown).

The use of the three-fourths, one, and three-halves divisor multiples requires an additional register position (Z) because the three-fourths multiple produces two advance quotient bits, three definite bits in all. These go into positions X, Y, and Z. The three-halves multiple produces two definite quotient bits in positions X and Y, and a tentative bit in position Z. The one-times multiple produces one definite quotient bit in position X and two tentative bits in positions Y and Z.

If the division example previously described were performed using the double-adder method with three-fourths, one, and three-halves divisor multiples, the number of operating cycles would be reduced from eleven to nine. One cycle would have to be added to this to allow for the generation of the three-halves times multiple of the divisor.

Fig. 16 illustrates graphically the various conditions that may occur when using the 3/4, 1.0, 3/2 divisor multiples. It shows an initial true dividend with complement divisor multiples only, but the inverse can easily be found from this by reversing all directions and interchanging *zeros* and *ones* in the quotient bit columns.

In example 1 the initial dividend is between 1 1/2 and 2 times the divisor. Selection here would choose the use of the 3/2 divisor multiple which would give two definite quotient bits and one tentative (indicated by a circle). The 1.0 times multiple could be used, though it would be less efficient. It would give one definite quo-

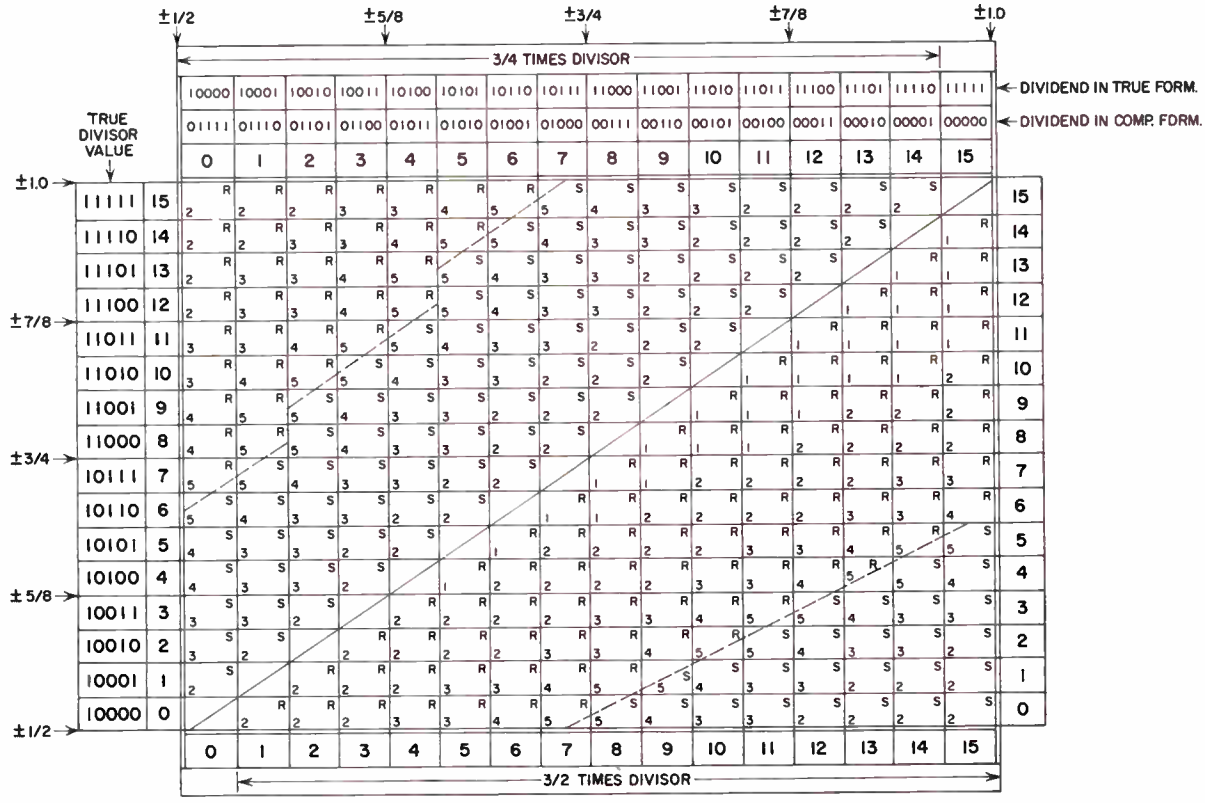
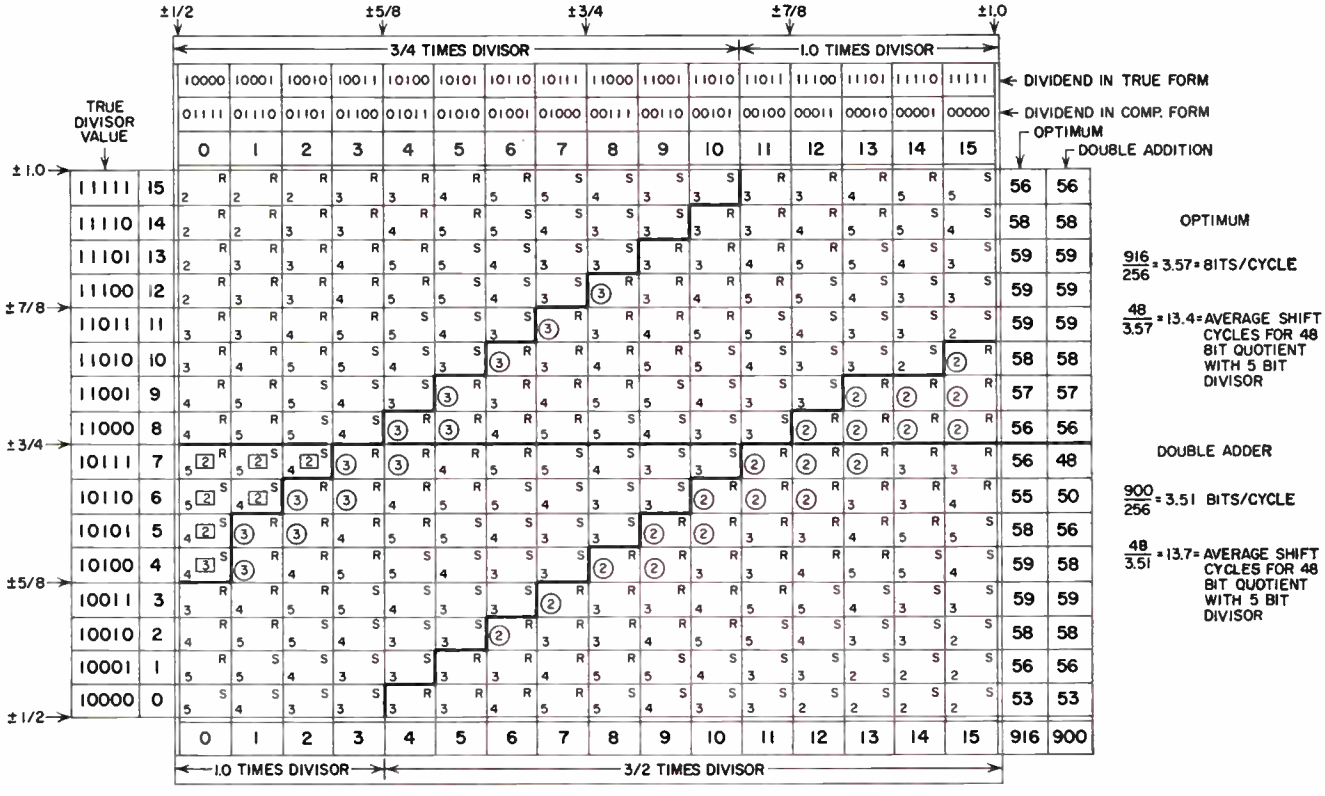
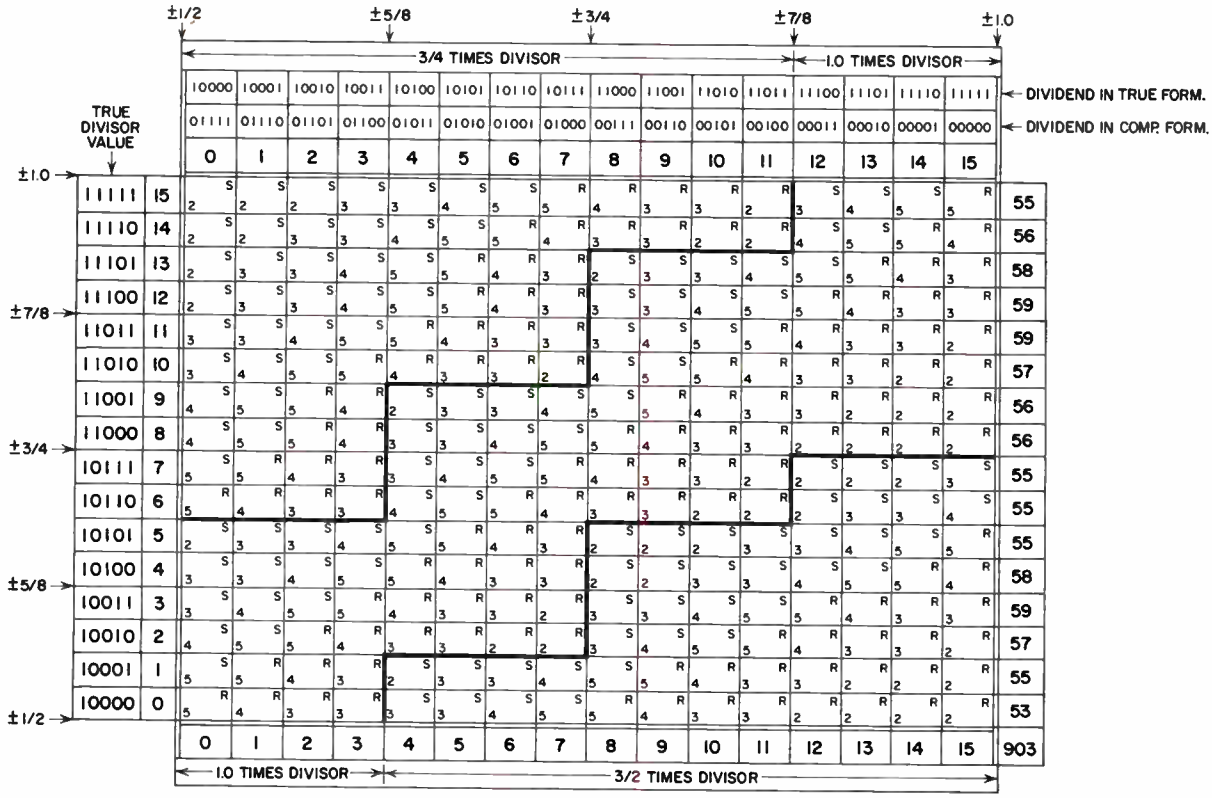


Fig. 13—Division tables using $\frac{1}{2}$ and $\frac{3}{4}$ times divisor.



	SHIFTS - OPTIMUM						SHIFTS - DOUBLE ADDER					
SHIFT LENGTH	1	2	3	4	5	TOTAL	1	2	3	4	5	TOTAL
NUMBER	0	37	96	61	62	256	0	43	97	57	59	256
PERCENT	0.0	14.5	37.5	23.8	24.2	100.0	0.0	16.8	37.9	22.3	23.0	100.0

Fig. 14—Division table using $\frac{1}{2}$, 1.0, $\frac{3}{4}$ times divisor with optimum coding.



	SHIFTS					
SHIFT LENGTH	1	2	3	4	5	TOTAL
NUMBER	0	96	174	118	124	512
PERCENT	0.0	18.8	33.9	23.1	24.2	100.0

$\frac{903}{256}$ = 3.52 BITS/CYCLE

$\frac{48}{3.52}$ = 13.6 AVERAGE SHIFT CYCLES FOR 48 BIT QUOTIENT WITH 5 BIT DIVISOR

Fig. 15—Division table using $\frac{3}{2}$, 1.0, $\frac{3}{4}$ times divisor with four-way by sixteen-way coding.

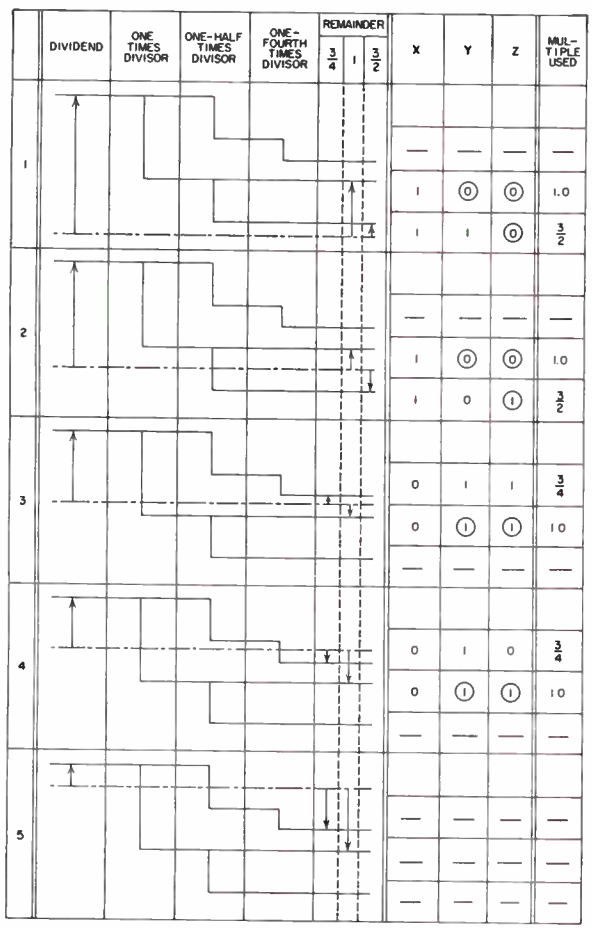


Fig. 16—Quotient development using 3/4, 1.0, 3/2 times divisor.

tient bit and two tentative bits. In this case the first tentative bit would be incorrect, and would be changed on the next cycle. The 3/4 multiple would not be selected for use with this initial condition.

In example 2 the initial dividend is greater than one times the divisor but less than one-and-a-half times the divisor. Either the 3/2 or 1.0 divisor multiple may be selected here, but not the 3/4 multiple as it would be less efficient than the 1.0 times multiple. Here again the 3/2 multiple gives two definite quotient bits and the 1.0 times multiple gives one.

Example 3 has a dividend less than one times the divisor but greater than 3/4 times. It may use either of these multiples, but not the 3/2 multiple. The 3/4 multiple gives three definite quotient bits, while the 1.0 multiple gives one definite and two tentative.

In example 4 the dividend has a value between 1/2 and 3/4 the divisor. This condition will always result in the choice of the 3/4 divisor multiple, though the 1.0 times will give correct results.

Example 5 shows a dividend having a value less than half the divisor. This condition could only arise as a result of an incorrect previous cycle as it would require a true dividend with a leading zero following the shift.

The use of the 3/4 multiple will never result in a following shift of only one. If it results in a shift of two, the fact that the 3/4 multiple was used must be remembered into the next cycle, and the entry into position X must be made from position Z instead of from data obtained in that cycle from the adder result. Similar precautions must be taken when using the 3/2 multiple to protect data from position Y in the event of a one-position shift.

Division termination procedure is the same as was previously described, with the additional requirement that the 3/2 multiple must not be used if the shift counter register agrees with the shift called for, and the 3/4 multiple must not be used if the shift counter register agrees with or is one greater than the shift called for by the decoder. In either case, the one-times multiple should be substituted.

Comparative Evaluation of Various Methods of Division

The effectiveness of several methods of performing division has been compared on the basis of five-bit divisors. These results need to be modified to show the effect of larger divisors. A simple method of doing this which will yield a close approximation to the desired result may be developed from a study of the pattern of shift amount variations in Fig. 10. From this it can be predicted that if a six-bit chart is constructed, it will show the same percentage of total operations for shifts of 1, 2, 3, and 4 positions. The present shift of 5, which actually represents five or greater, would split approximately evenly into five, and six or greater. The six or greater could then be split approximately evenly in six, and seven or greater. The accuracy of this even division increases as the number of positions in the square increases.

In a computer the need for large shifts occurs so infrequently that it is usually not considered practical to include a shifter capable of making, in one shift cycle, all shifts that may be required. Once the data has been expanded to include the possibility of long shifts, the effect of this on performance must be considered.

To permit easier expansion, the data for the five-bit divisor was transferred to a basis of 1000 operations rather than 256, the 1000 operations being obtained by using the percentage figures from the various tables with the decimal moved one position right. In each case the expansion was extended to include all shifts that would occur at least one-tenth of one per cent of the time. The remaining shifts, amounting to one-tenth of one per cent, were all assigned to the next shift length. All numbers of shifts were adjusted to be whole numbers. The average total positions shifted across for 1000 shifts was then obtained by multiplying each shift number by its frequency of occurrence, then adding these products together. This number divided by 1000 gave the average bits shifted across per cycle with no limitation on the shifter size.

Limiting the range of the shifter leaves the number of bits shifted across the same as for the operation with no limit, but it increases the number of shift cycles required to get across them. If a limit of four is assumed, a desired shift of five will require two operations, one shift of four and one shift of one. A desired shift of ten would require three operations, two shifts of four and one shift of two.

The results obtained in this manner for eight different division methods will be summarized in Table VII. A description of the column headings is given below.

1) Division using one times the divisor and shifting across *zeros* only. Data for this was obtained from Fig. 10 by assigning shift values of one to all complement results when starting with a true dividend.
2) Division using one times the divisor and shifting across *ones* and *zeros*, single addition.
3) Division using one-half, one, and two times the divisor with coded multiple selection.
4) Division using one-half, one, and two times the divisor with double addition, also with optimum selection.
5) Division using three-fourths, one, and three-halves times the divisor with simple (two by two) coding.
6) Division using three-fourths, one, and three-halves times the divisor with complex (four by eight) coding.
7) Division using three-fourths, one, and three-halves times the divisor with double addition.
8) Division using three-fourths, one, and three-halves times the divisor with optimum selection.

TABLE VII

Shifter Limit	Average Bits Shifted Across Per Shift Cycle							
	1	2	3	4	5	6	7	8
None	1.86	2.66	2.86	2.94	3.59	3.77	3.75	3.82
8	1.85	2.64	2.84	2.92	3.54	3.72	3.69	3.76
6	1.83	2.54	2.78	2.86	3.40	3.55	3.54	3.60
4	1.76	2.39	2.53	2.61	2.98	3.07	3.08	3.03
5*	1.80	2.54	2.74	2.82	3.37	3.58	3.51	3.58

* Five-bit divisor.

These figures are believed to represent an accurate comparison of the efficiencies of the different methods of division that have been described. The absolute accuracy is subject to the limitations previously explained.

Acknowledgment

Most of the material used in the preparation of this report was accumulated or developed during the design of the parallel arithmetic section of the IBM Stretch Computer. Particular mention should be made of the following original contributions.

The method of division described in the section "Division Using Single Adder, One-Times Divisor, and Shifting Across Zeros and Ones" was proposed by D. W. Sweeney, and was described in an IBM internal paper entitled "High-Speed Arithmetic in a Parallel Device," by J. Cocke and D. W. Sweeney, February, 1957.

The method of division described in the section "Division Using Divisor Multiples of Three-Fourths, One, and Three-Halves" was proposed by J. R. Stewart, and a theoretical evaluation of its advantages was made by C. V. Freiman.

The method of modifying the high-order end of the adders described in the section "Component Reduction with Carry-Save Adders" was proposed by F. R. Bielawa.

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Statistical Analysis of Certain Binary Division Algorithms*

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Summary—**Nondeterministic extensions of the nonrestoring method of binary division have been described by MacSorley [1]. One extension requires that the magnitudes of the divisor and partial remainders be "normal," *i.e.*, in the range [0.5, 1.0). This leads to a time improvement of more than two relative to conventional nonrestoring methods. Other extensions involve the use of several divisor multiples (or trial quotients). A Markov chain model is used here to analyze these methods. Steady-state distributions are determined for the division remainder and performance figures based on both this steady-state distribution and a random distribution are calculated. These are compared with the results of a computer simulation of 2^{14} randmly-chosen division problems using two specific methods of division.**

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Introduction

IN choosing the algorithms to be used for the various arithmetic operations in a digital computer, it is usually necessary to compromise between speeds of operation and costs of implementation. Should the amount of time required by a particular algorithm be variable, information about the statistical properties

of the operation time is required in order to make an appropriate decision.

This paper is specifically concerned with the statistical analysis of division methods which may be considered nondeterministic extensions of the nonrestoring method of binary division [2]. Since reliable information about the distribution of the divisor and dividend is rarely available, and since many iterations are usually required to complete a division problem, a steady-state value is determined for the average number of quotient bits generated per iteration for a particular method of division.

This steady-state average is obtained by describing the iterative division process in terms of a regular Markov chain. Though only used for division algorithms in this paper, the Markov chain method introduced should prove of value in other recursive arithmetic operations where the number of iterations is large.

The average obtained from the steady-state distribution of the remainder differs by only 2.5 per cent from that obtained by assuming the operands randomly distributed. Since the latter are much easier to determine than the steady-state averages, they will be used in evaluating various division algorithms.

Two nondeterministic methods of division were simulated in 2^{14} randomly chosen division problems. Both methods required that the divisor and each remainder be in normal form, *i.e.*, its magnitude in the range [0.5, 1.0). The first method used one divisor multiple (trial quotient) [4], while the second used three multiples. Extensive comparisons of the performance of the two methods are presented as Figs. 7–9.

Division

The methods of binary division which will be analyzed below have been discussed in detail by MacSorley [1] and are essentially extensions of the nonrestoring method described by Burks, Goldstine and von Neumann in their classic discussion of electronic computer design [2]. In Example 1 we have worked the same division problem twice—once using a restoring method and once using the analogous nonrestoring method.[1] Note that in illustrating these methods of division we have shown successively smaller multiples of the divisor subtracted or added to the remainder at each iteration. It will serve the purposes of our subsequent discussion if we assume that the remainder is shifted left during each iteration so that the same multiple of the divisor is used in each subtraction or addition. Example 2 uses the nonrestoring division of Example 1 to demonstrate this shifting of the remainders. For clarity, a sign-plus-magnitude representation has been used and both divisor (D) and dividend (R_0) have been chosen to be positive. We shall continue to assume that D and R_0 are positive.

These examples also illustrate the manner in which quotients are to be developed. A quotient register is initially set to zero and each time mD is subtracted (added) to the remainder, m is added (subtracted) from the contents of the quotient register ($m>0$). When, as in Example 2, the remainder is shifted, both the contents and the location of the binary point in the quotient register are shifted a like amount before m is added or subtracted.

Example 1: Restoring and Nonrestoring Division

divisor (D) = .1011 dividend (R_0) = .1111001

a) *Restoring division*

	remainders	*quotients*
dividend	+.1111001	
$-D$	−.1011	1.000
first remainder	+.0100001	
$-D/2$	−.01011	1.100
	−.0001011	
$+D/2$	+.01011	1.000
second remainder	+.0100001	
$-D/4$	−.001011	1.010
third remainder	+.0001011	
$-D/8$	−.0001011	1.011
	0	

b) *Nonrestoring division*

dividend	+.1111001	
$-D$	−.1011	1.000
first remainder	+.0100001	
$-D/2$	−.01011	1.100
second remainder	−.0001011	
$+D/4$	+.001011	1.010 or 1.1(−1)0
third remainder	+.0001011	
$-D/8$	−.0001011	1.011
	0	

[1] Readers desiring a basic discussion of various division methods are referred to Phister [3] and Richards [4].

Example 2: Nonrestoring Division with Remainders Shifted

divisor and dividend as in Example 1
R_j is the shifted remainder after j iterations
Q_j is the quotient after j iterations

R_0	$+.1111001$	Q_0	0000.
$-D$	$-.1011$		0001.
	$+.0100001$		
R_1	$+.100001$	Q_1	001.0
$-D$	$-.1011$		001.1
	$-.001011$		
R_2	$-.01011$	Q_2	01.10
$+D$	$+.1011$		01.01 or
			01.1(−1)
	$+.01011$		
R_3	$+.1011$	Q_3	1.010
$-D$	$-.1011$		1.011
	0	Q_4	1.011

Following the notation of Example 2, let Q_j be the quotient as developed in j iterations ($Q_0=0$) and let R_j be the shifted (partial) remainder after the jth iteration. These quantities are related in the following way:

$$R_0 = D \times Q_j + R_j \times 2^{-S_j}, \qquad (1)$$

where

$$S_j = \sum_{i=1}^{j} s_i,$$

the sum of the number of positions which the remainder is shifted at each iteration.

It is convenient to assume that D and R_0 are such as to make $m=1$ for both the restoring and the nonrestoring case. In the former, if R_j-D is positive, a shift of one position is performed, making $R_{j+1}=2(R_j-D)$. If R_j-D is negative, D is added back before the shift, thus "restoring" the remainder to a positive value and making $R_{j+1}=2R_j$. In nonrestoring division, D is subtracted (added) to R_j if R_j is positive (negative). The quantity $\pm(|R_j|-D)$ is shifted one position, making $R_{j+1}=\pm 2(|R_j|-D)$. Thus, both methods yield one quotient bit per iteration and $s_j=1$ at each iteration.

As Robertson has pointed out in his discussion of divisor multiple choice [5], only a small part of the time required to execute a division in a digital computer is spent in initiating or terminating operations. Any substantial improvement in over-all divide time must, therefore, involve reduction of the iteration time or reduction of the number of iterations per problem or both. Comparing the nonrestoring method with the restoring method, we note a marked improvement in length of iteration while the number of iterations is the same in both cases. (Of the methods we shall discuss, it is only in the restoring method that more than one addition or subtraction is included in our definition of the iterative cycle. Henceforth, each iteration shall include one addition or subtraction and one variable-length shift.)

Normalized Divisors and Remainders

We will say that a binary number is in normal form if its magnitude is in the range [0.5, 1.0). This is equivalent to saying that, for positive numbers, the first position to the right of the binary point is one, while all positions to the left of the binary point are zero. Let us now assume that D and R_0 are initially normalized and let us refer to $\pm(|R_j|-D)$ as the unnormalized remainder denoting it by R^*_{j+1}. In conventional nonrestoring division, $R_{j+1}=2R^*_{j+1}$; our first extension of nonrestoring division requires that at the end of each iteration R_{j+1} be in normal form.

As $|R^*_{j+1}|$ is in the range [0, 0.5), the length of shift required to go from R^*_{j+1} to R_{j+1} may be 1, 2, 3, $\cdots$, x_j, where x_j is the number of quotient bits which remain to be determined after j iterations. This normalizing of remainders to increase the number of quotient bits generated per iteration was proposed independently by Sweeney (January, 1957), Robertson [6], and Tocher [7] at approximately the same time. We shall herein refer to this method of division as the S-R-T method. Example 3 shows how this method saves one iteration in the division problem of Examples 1 and 2.

Example 3: Nonrestoring Division with Remainders Normalized (S-R-T Method)

divisor, dividend, and notation as in Example 2
s_j is the length of shift in the jth iteration

$$S_j = \sum_{i=1}^{j} s_i;$$

R^*_j is the unnormalized remainder in the jth iteration

	remainders		*quotients*	*shifts*
R_0	$+.1111001$	Q_0	00000.	
$-D$	$-.1011$		00001.	
R_1^*	$+.0100001$			
R_1	$+.100001$	Q_1	0001.0	$s_1=1$; $S_1=1$
$-D$	$-.1011$		0001.1	
R_2^*	$-.001011$			
R_2	$-.1011$	Q_2	01.100	$s_2=2$; $S_2=3$
$+D$	$+.1011$		01.011	
	0			
		Q_3	1.0110	$s_3=1$; $S_3=4$

(s_3 was taken as 1 as it was assumed that 5 quotient bits were to be determined.)

Number of Quotient Bits per Iteration (S-R-T Method)

The number of quotient bits generated on the jth iteration is the length of the shift required to transform R^*_j into R_j—previously defined to be s_j. This quantity is clearly a function of $|R_{j-1}|$ and D and hence the average number of shifts on the jth iteration depends upon the statistical distribution of $|R_{j-1}|$ and D. In Fig. 1 we have shown the functional dependence of s_j on $|R_{j-1}|$ and D. The maximum value of s_j is x_j but it will be shown that the average value of s_j, $\bar{s}_j$, does not change significantly as x_j is increased beyond a nominal value of ten or so. This practical independence of s_j from x_j enables us to treat s_j as unbounded ($x_j = \infty$). We will also treat D and R_j as continuous variables in the range [0.5, 1.0).

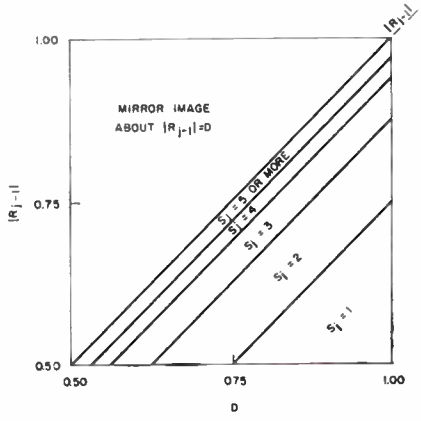

Fig. 1—s_j as a function of $|R_{j-1}|$ and D.

From Fig. 1, it is easily verified by summing weighted areas that, if the joint probability density of $|R_{j-1}|$ and D is uniform in the indicated range and if s_j is unbounded,

$$\bar{s}_j = \sum_{s=1}^{\infty} \frac{s(2^{s+1} - 3)}{2^{2s}} = \frac{8}{3} . \tag{2}$$

When $x_j = 10$,

$$\bar{s}_j = \frac{10 \times (2^{10} - 1)}{2^{18}} + \sum_{s=1}^{9} \frac{s(2^{s+1} - 3)}{2^{2s}} \cong 2.66. \tag{3}$$

Sweeney and Cocke used an approach somewhat different from that suggested by Fig. 1 and arrived at the same results obtained in (2) and (3). The value 8/3 will be referred to as the nominal shift average $\hat{s}$ of the R-S-T method as many assumptions have been made in its determination. Subsequent results will show that nominal averages calculated in this way are sufficiently close to actual averages to make them valuable as figures of merit for various division methods.

Steady-State Distributions of the Remainder

As indicated above, $\hat{s}$ is that value of $\bar{s}_j$ which is obtained when $|R_{j-1}|$ and D are randomly distributed. Even if this assumption is valid, it is clear that the joint distribution of $|R_j|$ and D will be far from random. Calculation of $\overline{s_{j+1}}$ then becomes exceedingly difficult and the joint distribution of $|R_{j+1}|$ and D is exceedingly complex. Average values of shift length could be obtained for each successive iteration but the result obtained would not seem to justify the work involved, as the initial assumption of randomness is highly arbitrary.

We will show below that we need only assume the initial distribution to be piecewise continuous in order to determine steady-state distributions of the remainder. Using these distributions, steady-state shift averages will be calculated and empirical results will be introduced to show that these averages are in excellent agreement with the actual averages obtained in division problems requiring in the order of twenty iterations.

In order to show that a steady-state distribution of remainder magnitudes exists, we will show that for each rational value of divisor a finite Markov chain may be found such that each iteration of the division process corresponds to a state transition of the chain.[2] Each state of the chain will correspond to an arbitrarily small interval of the remainder[3] and, since the chain will be shown to be regular, each state (and hence each interval of the remainder) will have a steady-state probability associated with it. It will develop that the probability density is uniform for each of these intervals and thus may be obtained by dividing the interval's steady-state probability by the interval's length.

Specific Example

Before describing the process of chain generation in general, let us develop the chain for a divisor of 3/5. First, we partition the range of the remainder in the following way. Place end-points at the smallest and largest shift boundaries in the range [0.5, 1.0). From Fig. 2(a), these are seen to be $3/5+1/4=17/20$ and $3/5-1/16=43/80$. We term the three intervals thus generated α^*, β^*, γ^*.

Note that a shift of length 3 would be used in forming the next remainder if the present remainder is in interval α^*. This follows from the fact that the magnitude of the unnormalized remainder would be in the range $[3/5-43/80,\ 3/5-1/2)$ or $[1/16,\ 1/10)$. We see that the end-points of α^* become $2^3/16$ and $2^3/10$ or 1/2 and 4/5 on the next iteration. Similarly, we see that γ^* is a 1-shift interval and that its end-points also have 1/2 and 4/5 as their images at the end of the next iteration.

[2] The terminology used in discussing Markov chains is that of Kemeny, *et al.* [8].

[3] Although we are dealing with remainder magnitudes, the term remainder shall be used for the sake of brevity.

The interval β^* is somewhat different. Both of its end-points are shift boundaries and by taking new end-points at $3/5+1/8$, $3/5+1/16$, $3/5\pm1/32$, $3/5\pm1/64$, $\cdots$, we could partition β^* into an infinite number of intervals with shift lengths varying from interval to interval. Each of these intervals, however, would map into the full remainder range on the next iteration—*i.e.*, the end-points of any of the intervals would have $1/2$ and 1 as their images. Because of this, we shall say that β^* maps into the entire remainder range.

We have seen that both α^* and γ^* have the interval $[1/2, 4/5)$ as their image. We thus define new end-points at $4/5$ and $3/5+1/8=29/40$, so that we may now say that each defined interval has some group of consecutively defined intervals as its image. Fig. 2(b) shows the inclusion of $4/5$ and $29/40$ as interval end-points. We say that β maps into the entire remainder range as it may be partitioned into an infinite number of intervals each of which maps into this range.

Let us use $\alpha\rightarrow(\alpha, \gamma)$ to indicate that interval α maps into the group of consecutive intervals α, β, γ. Referring to Fig. 2(b), we may then say

$$\begin{aligned}
\alpha &\rightarrow (\alpha, \gamma)\\
\beta &\rightarrow (\alpha,)\\
\gamma &\rightarrow (\alpha, \gamma)\\
\delta &\rightarrow (\delta, \epsilon)\\
\epsilon &\rightarrow (\alpha, \gamma).
\end{aligned} \tag{4}$$

The first part of our process terminates when a set of relations such as (4) has been determined. It will be shown below that only a finite number of intervals need be defined when the divisor is a rational number. We will now use the intervals of Fig. 2(b) to determine the remainder's steady-state density function.

Let $\{a\}$ be the event {the present remainder is randomly distributed over the interval α}. Referring to (4), we see that if the present remainder is randomly distributed over α, the next remainder will be randomly distributed over the interval (α, γ). It may then be said that

$$\{a\} \rightarrow \{a'\} \text{ or } \{b'\} \text{ or } \{c'\}, \tag{5}$$

where $\{a'\}$, $\{b'\}$, and $\{c'\}$ are three mutually exclusive events such that $\{a'\}$ is the event that at the end of the next iteration the remainder is randomly distributed over α, $\{b'\}$ is the event . . .

If we define the conditional probability p_{ab} to be $PR\{b'/a\}$, we see that it may be evaluated by dividing the length of β by the length of α's image. Thus, for the intervals of Fig. 3, we have

$$p_{ab} = \frac{29/40 - 43/80}{4/5 - 1/2} = \frac{5}{8}. \tag{6}$$

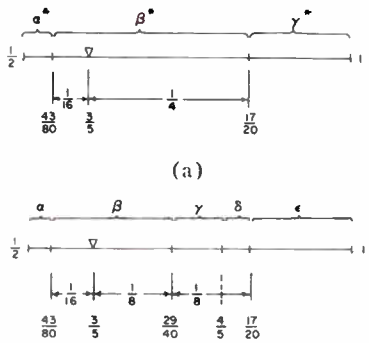

Fig. 2.

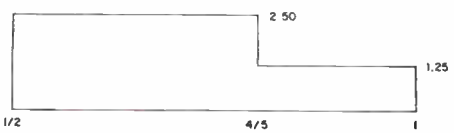

Fig. 3—Steady-state probability density function of the remainder for a divisor of 3/5.

If β were not contained in α's image, p_{ab} would equal zero.

These conditional probabilities are now taken to be the transition probabilities of a first-order Markov chain with states a, b, c, d, e. The transition matrix, P, for a divisor of $3/5$ and the partitioning of Fig. 2(b) is then determined to be

$$P = \begin{array}{c} \\ a \\ b \\ c \\ d \\ e \end{array} \begin{array}{c} \begin{array}{ccccc} a & b & c & d & e \end{array} \\ \begin{bmatrix} 5 & 25 & 10 & 0 & 0 \\ 3 & 15 & 6 & 4 & 12 \\ 5 & 25 & 10 & 0 & 0 \\ 0 & 0 & 0 & 10 & 30 \\ 5 & 25 & 10 & 0 & 0 \end{bmatrix} \end{array} \times \frac{1}{40}. \tag{7}$$

Inspection shows that each of the entries of P^2 is non-zero and hence the chain is regular. This permits us to solve for the steady-state probabilities of the various states of the chain. Label these probablities $p(a)$, $p(b)$, $p(c)$, $p(d)$, $p(e)$ and let the row vector $[p]$ be $[p(a)\ p(b)\ p(c)\ p(d)\ p(e)]$. We then have that

$$[p][P] = [p] \tag{8}$$

and

$$p(a) + p(b) + p(c) + p(d) + p(e) = 1. \tag{9}$$

Solving for $[p]$, we get

$$[p] = [3/32\ \ 15/32\ \ 6/32\ \ 2/32\ \ 6/32]. \tag{10}$$

This suggests that the steady-state density function of the remainder is as shown in Fig. 3.

In Example 4, we take the discontinuities of Fig. 3 and adjacent shift boundaries to be end-points of in-

tervals[4] and verify that Fig. 3 is the steady-state density function of the remainder for a divisor of 3/5. While the shift average for a divisor of 3/5 with a random distribution of the remainder ($\hat{s}$) is 2.65, the average when the distribution is that of Fig. 3 is 3.00. As will be seen, steady-state shift averages are higher than $\hat{s}$ for divisors less than 3/4 and lower for divisors greater than 3/4.

Example 4: Verification of the Steady-State Density Function for a Divisor of 3/5 [Fig. 4(a)].

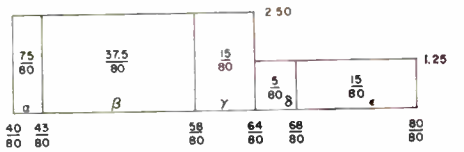

Fig. 4(a).

Since α maps uniformly into (α, γ), we may distribute the area of α, 7.5/80, uniformly over (α, γ) to obtain that portion of the density function of the next iteration's remainder which is contributed by interval α of the present remainder. Similarly distributing the areas of β, γ, δ, and ϵ, we obtain Fig. 4(b).

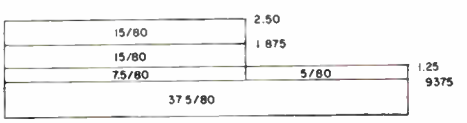

Fig. 4(b).

General Case

Before proving that the methods used above hold whenever the initial distribution is piecewise continuous, let us specifically state the steps involved in determining the steady-state distribution of remainders for any rational divisor in the range [0.5, 1.0).

1) For any rational divisor, D_0, find $0.5^{(1)}$ and $1.0^{(1)}$, the first-order images of 0.5 and 1.0. This is done by choosing K_1 and K_2 such that both $2^{K_1}(D_0 - 0.5) \triangleq 0.5^{(1)}$ and $2^{K_2}(1.0 - D_0) \triangleq 1.0^{(1)}$ are in the range [0.5, 1.0). We shall take $0.5 = 0.5^{(0)}$ and $1.0 = 1.0^{(0)}$.
2) Determine the jth order images of 0.5 and 1.0 from the $(j-1)$st order images ($j = 2, 3, \cdots$). This process continues until some order image of 0.5 is the same as the divisor or a lower order image of 0.5 or 1.0 and some order image of 1.0 is the same as the divisor or some lower order image of 0.5 or 1.0. The divisor may be an image of 0.5 or 1.0 but it has no image.
3) Partition the remainder range in the following way. Each of the images determined in (2), including $0.5^{(0)}$ and $1.0^{(0)}$, are taken to be end-points of intervals. In addition, if a shift region,

$$\left[D_0 \pm \frac{1}{2^K},\ D_0 \pm \frac{2}{2^K}\right)$$

contains one or more of the images generated above the boundaries of this region are also taken to be end-points. Naturally, no end-points are taken outside the range [0.5, 1.0).
4) Take each interval between adjacent end-points to be a state of a Markov chain and determine the transition probabilities p_{ab} of the transition matrix P, by dividing the length of the image of the interval α into the length of the interval β for all α and β such that interval β is included in the image of interval α. If β is not in α's image, $p_{\alpha\beta} = 0$.
5) Solve for the steady-state probabilities $p(a)$, $p(b)$, $\cdots$.
6) Find the probability density for an interval α by dividing $p(a)$ by the length of α.
7) Using the density function thus obtained, find the steady-state shift average for the divisor D_0. In Appendix I, these rules are used explicitly for $D = 35/64$.

Fortunately, it is not necessary to go through this process for each divisor of interest. In Appendix II, the steady-state probability density function of the remainder is given for various large intervals of the divisor. The shift averages of Table I are calculated from these distributions.

TABLE I

Divisor Interval	Steady-State Shift Average
$9/16 \leq D \leq 7/12$	$\frac{7D}{2-D}$
$33/56 \leq D \leq 31/52$	$\frac{31D}{8-3D}$
$17/28 \leq D \leq 3/4$	3
$3/4 \leq D < 1$	$\frac{2D}{2D-1}$

Existence and Uniqueness of Solution

We shall now prove that: a) step 2 of the seven-step process described above always terminates when the divisor is a rational number; b) the Markov chain obtained is regular and hence permits the determination of steady-state probabilities, and c) the steady-state density function obtained in this way is unique, provided the initial distribution of the remainder is piecewise continuous.

[4] We no longer require images of intervals to be a collection of defined intervals and hence the intervals now defined will, in general, be composites of those used to generate the density function. This is not true for $D = 3/5$.

In proving a), let us consider a rational divisor p/q and a rational value of R_0, p_0/q_0, where $p(p_0)$ and $q(q_0)$ are relatively prime positive integers such that $p<q\leq 2p(p_0\leq q_0{}^5\leq 2p_0)$. We then have

$$R_0 - D = \frac{p_0}{q_0} - \frac{p}{q} = \frac{p_0 q - p q_0}{q q_0}. \tag{11}$$

If $R_0 \neq D$, the first-order image of R_0, $R_0^{(1)}$, is then

$$R_0^{(1)} = \frac{2^{K_1}\left| p_0 q - p q_0 \right|}{q q_0} \qquad K_1 = 1, 2, \cdots, \tag{12}$$

where K_1 is chosen so that $R_0^{(1)}$ is in the range [0.5, 1.0). We may take

$$R_0^{(1)} = \frac{p_1}{q q_0}, \tag{13}$$

where p_1 is an even positive integer such that $p_1<qq_0 \leq 2p_1$.

In a similar way we can show that, if no $R_0^{(i)}=D(0 \leq i<n)$, then $R_0^{(n)}$ is of the form

$$R_0^{(n)} = \frac{p_n}{q q_0}, \tag{14}$$

where p_n is an even positive integer such that $p_n<qq_0 \leq 2p_n$. Clearly, some value of n, n_0, not greater than $qq_0/2$, may be found such that

$$R_0^{(n_0)} = D \tag{15}$$

or

$$R_0^{(i)} \neq D(0 \leq i < n_0) \text{ and } R_0^{(n_0)} = R_0^{(j)}\ 0 \leq j < n_0. \tag{16}$$

Thus, we have shown that any rational value of R_0 will generate only a finite number of images before one of the images is the same as the divisor or two images of different order are equivalent. One of the consequences of this is that only a finite number of images of 1/2 and 1 are required before images repeat or equal the divisor. Step 2, therefore, terminates in a finite number of images.

To prove that the Markov chain obtained by the above process is regular, we need only note that: a) some positive integer N exists for any nonzero interval of R_0 such that the Nth order image of that interval has 1/2 and 1 as its end-points, and b) at least one interval of R_0 has the interval [0.5, 1.0) as its first-order image. (In particular, one of the defined regions must contain D or have D as one of its end-points.) Thus, in the associated Markov chain, some positive integer n exists such that each entry of P^n is nonzero.

It remains to be shown that the steady-state density function obtained from the steady-state probabilities of the states of the Markov chain described above is unique. Suppose that it is not possible to assume that the distribution of the remainder is ever piecewise uniform with discontinuities only at the end-points obtained at step 3, but that the initial distribution of R_0 is piecewise continuous. We may then approximate this initial distribution as closely as we wish by a piecewise uniform distribution, with discontinuities at rational values of the remainder. We then generate images of 0.5, 1.0, and other end-points introduced in approximating the initial distribution. It has been shown above that only a finite number of images of rational numbers will be obtained before images repeat or equal the divisor. We next introduce a finite number of additional end-points as in step 3, and carry through steps 4–7. It is postulated that the resulting density function is the same as that obtained when only the images of 0.5 and 1.0 are used.

Let us assume that we have generated the steady-state density function for one Markhov chain which might be developed for some particular divisor. It is easily seen that this density function is unique by noting that only knowledge of the divisor is required to show that the density function repeats itself at the next iteration. Thus, any Markov chain developed for this divisor will have its state probabilities defined by this density function, provided states correspond to intervals of uniform density in the steady-state distribution. This will always be the case, for the discontinuities in the steady-state distribution are a subset of the end-points generated using the images of 0.5 and 1.0, and 0.5 and 1.0 are always end-points in any piecewise uniform approximation of the initial distribution.

Thus, we have proved that if the initial distribution is piecewise continuous (and hence may be approximated by a piecewise uniform density function with discontinuities at rational values of the remainder) and if the divisor is a rational number, a steady-state density function exists which may be obtained by using the seven steps given above. Since this density function is unique, it is often possible to postulate its form and solve only for the magnitude of the density in uniform intervals. This has been offered as an alternate method of getting the steady-state distribution for $D=35/64$ in Appendix I.

Simulation of the S-R-T Method

The steady-state shift average will accurately predict the actual shift average in a series of divisions only when the distribution of the remainder approximates its steady-state value for a large percentage of the iterations. The number of iterations required to approximate steady-state conditions naturally depends upon the initial distribution. Several examples (Appendix III), however, suggest that this number is small. {The theorems on the effect of initial distribution on the transient behavior of a Markov chain [8] would be of value only if the initial distribution of the dividend permitted a piecewise uniform approximation over intervals such as those of Fig. 2(b).}

[5] Only for the purposes of this proof do we allow $R_0=1$.

To determine an actual shift average for the S-R-T method, a simulation program was written by Bielawa and Schanzenbach. Dividends and divisors were 48 bits and 48 quotient positions were determined. The first five bits of the divisor were termed the divisor prefix and were assigned values from 10000 to 11111. The remaining 43 divisor bits were assigned randomly as were the last 47 bits of the normalized dividends. A total of 2^{10} random division problems were performed for each of the sixteen divisor prefixes. Shift averages were determined for each prefix and are shown plotted in bar-graph form in Fig. 5.

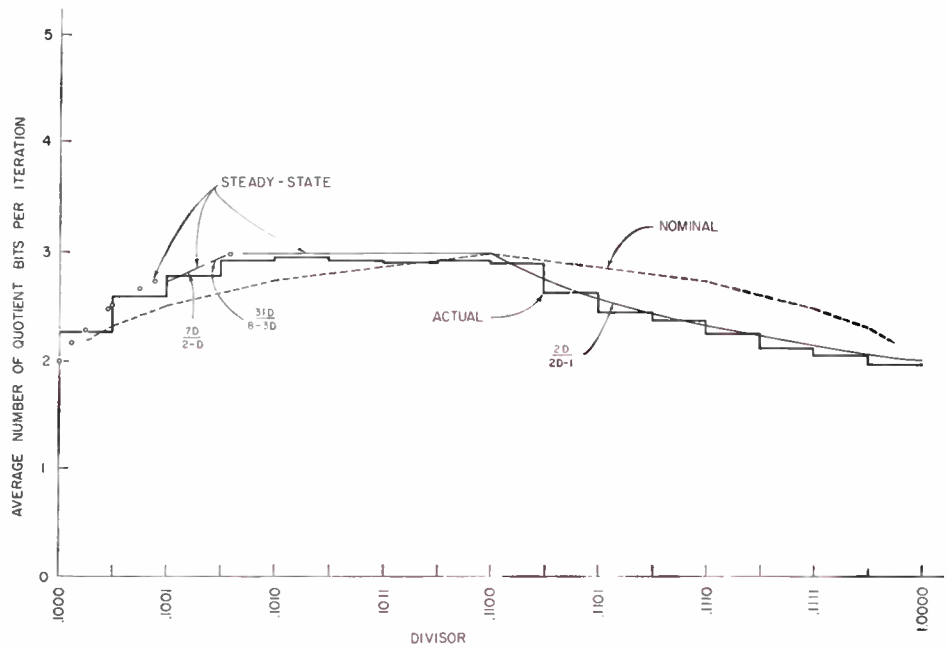

Fig. 5—Nominal, steady-state, and actual number of quotient bits per iteration as a function of the divisor (S-R-T Method).

Also shown in Fig. 5 are the nominal and steady-state shift averages as functions of the divisor. The latter were obtained from Table I and from calculations for particular divisors as shown. It is shown elsewhere that the actual first iteration shift average is in excellent agreement with the nominal shift average (2.675 as against 2.666). One would, therefore, expect the actual shift average to be somewhere between the nominal and steady-state averages, being closer to the latter if initial conditions are of less effect than steady-state conditions (successive distributions may be shown to monotonically approach the steady-state distribution). The fact that the actual shift average is very close to the steady-state average but always somewhat lower indicates that an initially random distribution approaches the steady-state distribution very quickly and that the last-iteration average is probably seriously affected by the fact that only a shift sufficient to complete the 48-bit quotient is ever used.

Division Multiples

If several multiples of the divisor are available throughout a division and if the multiple closest in magnitude to the remainder is chosen at each iteration, the number of quotient bits generated per iteration may be significantly increased. With normalized divisors and remainders, the choice of multiples is effectively limited to the range $[0.5D, 2.0D]$. As MacSorley [1] has shown, engineering considerations prohibit consideration of more than two or three multiples—and then only those which may be generated easily.

Use will be made of nominal shift averages in choosing pairs or triplets of multiples as the nominal value are relatively easy to calculate and do not appear to differ greatly from steady-state averages. To determine the nominal shift average for a particular group of divisor multiples, say $0.5D$ and $1.5D$, we need only draw the lines $|R_{i-1}| = 0.5D$ and $|R_{i-1}| = 1.5D$, as the line $|R_{i-1}| = D$ was drawn in Fig. 1, and demark shift areas by introducing boundaries of the form $|R_{i-1}| = 0.5D + 1/2k$ and $|R_{i-1}| = 1.5D - 1/2k$ $(k = 2, 3, \cdots)$. The nominal shift average is then simply the sum of weighted areas as was the case with the average for Fig. 1. Example 5 illustrates the determination of $\hat{s}$ for divisor multiples $0.5D$ and $1.5D$. Note that for this particular choice of two divisor multiples, $\hat{s}$ was actually lower than for the single divisor $1 \times D$ (7/3 as opposed to 8/3). It can be shown that the maximum value of $\hat{s}$ for two divisor multiples is 3.40 and corresponds to the multiples $0.85D$ and $1.17D$. In Table II we have presented values of $\hat{s}$ obtained for various combinations of

two or three divisor multiples. The group ($\sqrt{77/128}D$,D,$\sqrt{53/32}D$) yields the maximum $\hat{s}$ for any combination of three multiples one of which is $1\times D$.

Example 5: $\hat{s}$ for Divisor Multiples 0.5D and 1.5D

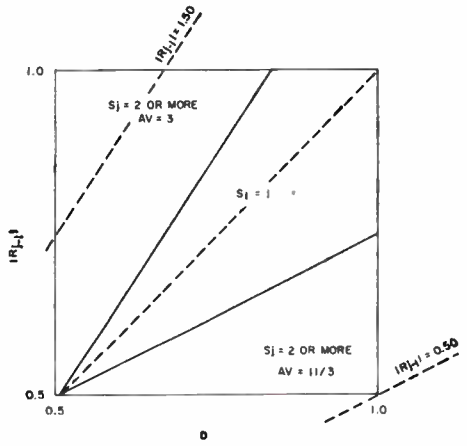

Fig. 6.

TABLE II

Divisor Multiples	Nominal Shift Average, $\hat{s}$
1.0	2.67
1.0, 2.0	2.75
0.5, 1.0	2.875
0.75, 1.0*	3.36
0.85, 1.17	3.40
0.75, 1.0,1.5	3.82
0.625,1.0,1.25	3.87
0.75, 1.0,1.25	4.047
$\sqrt{77/128}$, 1, $\sqrt{53/32}$	4.05

* Example 6 shows how one iteration is saved in the problem of Examples 1, 2, 3 if $0.75D$ is available in addition to $1.0D$.

$$\hat{s} = 3\times\frac{1}{3} + 1\times\frac{5}{12} + \frac{11}{3}\times\frac{1}{4} = \frac{28}{12} = 2.33.$$

Example 6: Using 0.75 and 1.0 as Divisor Multiples

divisor and dividend as in Examples 1–3

$$0.75D = 0.100001$$

	remainders	*quotients*
R_0	+.1111001	Q_0 00000.00
$-D$	−.1011	00001.00
R_1*	+.0100001	
R_1	+.100001	Q_1 0001.000
$-0.75D$	−.100001	0001.011
	0	
		Q_2 1.011000

THE 0.75-1.0-1.5 METHOD

MacSorley [1] has discussed most of the engineering considerations which were involved in selecting $0.75D$,D,$1.5D$ as the divisor multiples which are used in STRETCH-SIGMA's division algorithms. It may be of interest, however, to mention one of the aspects of quotient generation. When a remainder is positive, say, and $0.75D$ is subtracted leaving a negative next remainder, 010 are unambiguously the next three quotient bits. The magnitude of this negative remainder, however, may be such that a shift of two and not three is required for normalization. The algorithm for dealing with this case is quite simple. It states that 01 should be added to the quotient and the first bit of the next addition to the quotient inverted. Similar problems arise if $0.625D$-$1.0D$-$1.25D$ are used as divisor multiples but no simple algorithm exists for quotient generation.[6] This is basically the reason why the 0.75-1.0 -1.5 method is to be preferred even though its nominal shift average is somewhat lower.

The simulation program described above also performed the same 16×2^{10} division problems using the 0.75-1.0-1.5 method. No first iteration average is available as $1\times D$ was always used in that iteration. The second iteration average of 3.80 was in excellent agreement, however, with the nominal average of 3.82. Table III, and Figs. 7–9 present some of the comparative results obtained by using both methods to generate 48-bit quotients in 2^{14} examples. Note in Table III that the nominal and actual values differ by less than 6 per cent in both cases.

TABLE III

	Nominal shift average	Actual over-all shift average	Steady-state shift average (random divisor assumed)
S-R-T	2.67	2.53	~2.60
0.75-1.0-1.5	3.82	3.60	

CONCLUSIONS

The Markov chain model introduced to analyze division methods will prove of use in any iterative process where each iteration may be viewed as the mapping of a (relatively small) number of independent quantities into groupings of these same quantities. Naturally, the steady-state distributions obtained are of value only if the process requires a sufficient number of iterations to approach steady-state conditions.

Use of Bayes' Axiom in assuming all operands randomly distributed will often prove valuable in determining some crude performance figures for an arithmetic algorithm. If more reliable estimates are required and analytic techniques prove cumbersome, it is suggested that Monte Carlo methods be employed.

[6] The problem is alleviated considerably if several quotient registers are used in much the same way that Burtsev [9] has used two registers in his "carry-save" method of division.

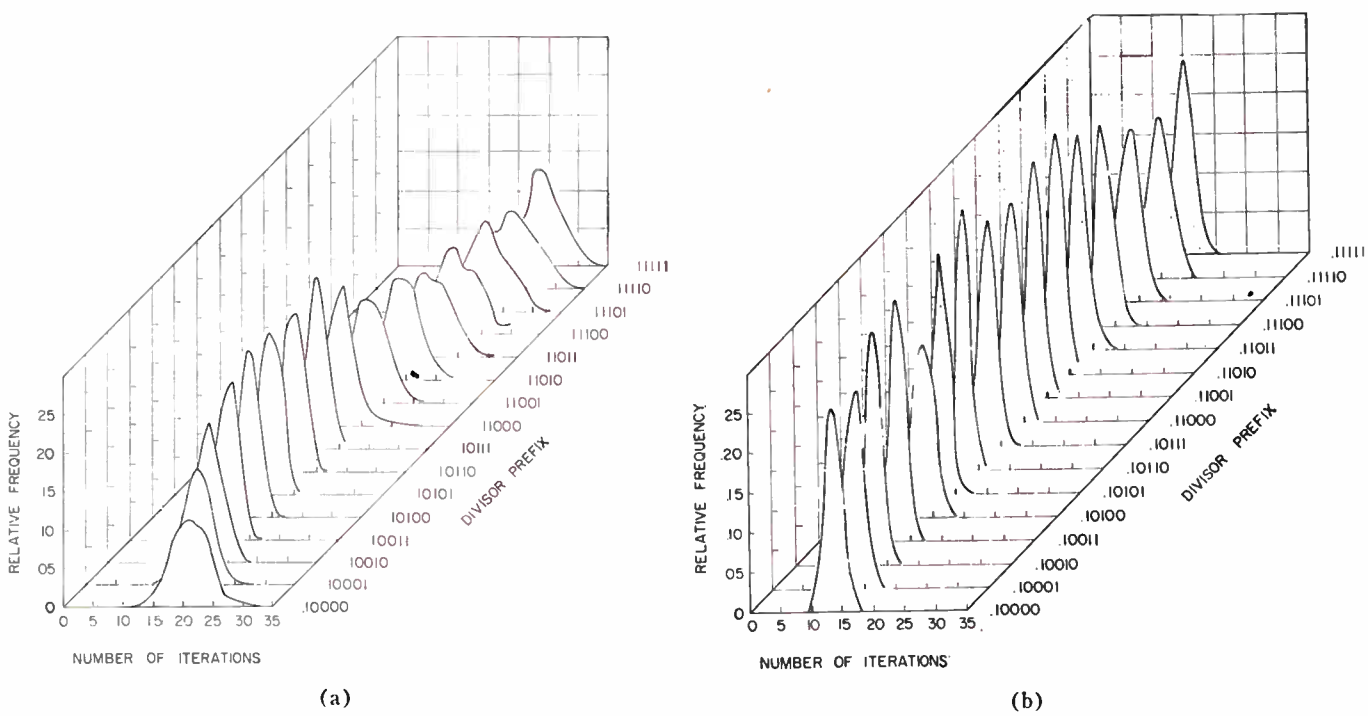

Fig. 7—Relative frequency of the number of iterations required to generate 48-bit quotients as a function of divisor. (Each curve is sketched from the results of 2^{10} randomly chosen problems in the divisor range shown.) (a) S-R-T Method. (b) 0.75-1.0-1.5 Method.

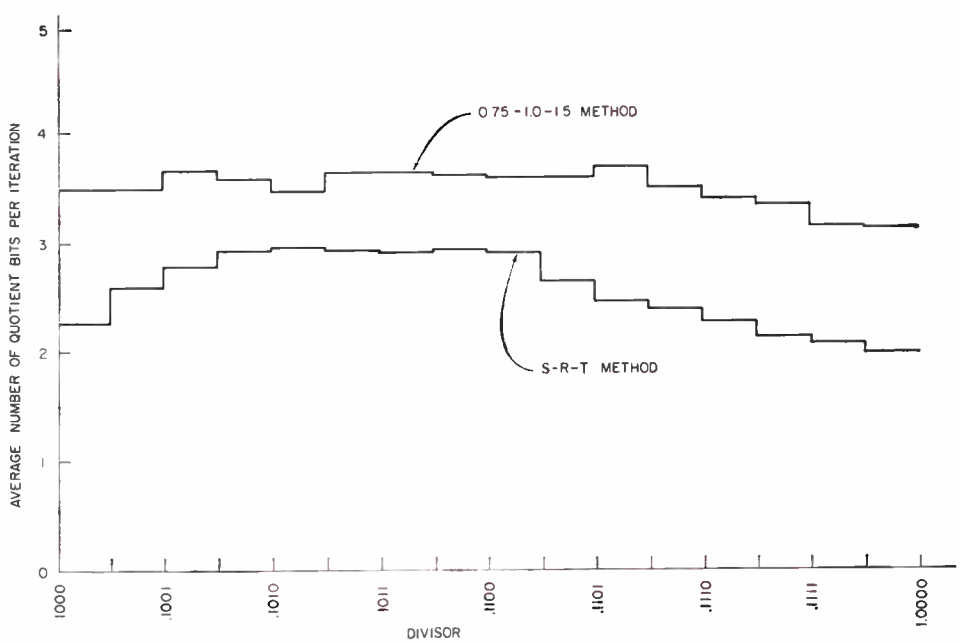

Fig. 8—Comparison of average number of quotient bits per iteration—S-R-T and 0.75-1.0-1.5 methods. (Each value is the average of 2^{10} randomly chosen division problems requiring from 9 to 35 iterations.

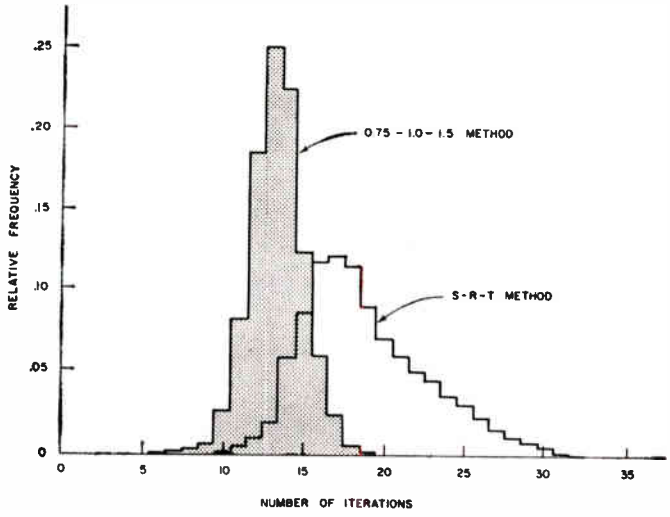

Fig. 9—Over-all relative frequency of number of iterations required to generate 48-bit quotients (see Fig. 7).

Appendix I

Explicit Determination of the Steady-State Shift Average ($D = 35/64$)

1) $35/64 - 1/2 = 3/64, \qquad 3/64 \times 2^4 = 48/64 \overset{\Delta}{=} 0.5^{(1)}$

(the denominator 64 will be omitted through step 3).

$64 - 35 = 29, \qquad 29 \times 2^1 = 58 \overset{\Delta}{=} 1.0^{(1)}.$

2) $48 - 35 = 13, \qquad 13 \times 2^2 = 52 \overset{\Delta}{=} 0.5^{(2)}.$

$58 - 35 = 23, \qquad 23 \times 2^1 = 46 \overset{\Delta}{=} 1.0^{(2)}.$

$52 - 35 = 17, \qquad 17 \times 2^1 = 34 \overset{\Delta}{=} 0.5^{(3)}.$

$46 - 35 = 11, \qquad 11 \times 2^2 = 44 \overset{\Delta}{=} 1.0^{(3)}.$ (17)

$35 - 34 = 1, \qquad 1 \times 2^5 = 32 \overset{\Delta}{=} 0.5^{(0)}.$

$44 - 35 = 9, \qquad 9 \times 2^2 = 36 \overset{\Delta}{=} 1.0^{(4)}.$

$36 - 35 = 1, \qquad 1 \times 2^5 = 32 \overset{\Delta}{=} 0.5^{(0)}.$

3) End-points from (2) are 32, 34, 36, 44, 46, 48, 52, 58, 64; shift boundaries fall at 33, 34, · · · , 36, 37, 39, 43, 51; therefore, we define intervals to be determined by the following end-points.

$$32, 33, 34, 36, 43, 44, 46, 48, 51, 52, 58, 64.$$

4) Defining these intervals to be $\alpha, \beta, \cdots, \kappa$, we get

$$P = \begin{bmatrix} 6 & 6 & 12 & 42 & 66 & 12 & 12 & 0 & 0 & 0 & 0 \\ 3 & 3 & 6 & 21 & 3 & 6 & 6 & 9 & 3 & 18 & 18 \\ 3 & 3 & 6 & 21 & 3 & 6 & 6 & 9 & 3 & 18 & 18 \\ 3 & 3 & 6 & 21 & 3 & 6 & 6 & 9 & 3 & 18 & 18 \\ 24 & 24 & 48 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 84 & 12 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 24 & 24 & 36 & 12 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 48 & 48 \\ 48 & 48 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 16 & 56 & 8 & 16 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 16 & 24 & 8 & 48 & 0 \end{bmatrix} \times \frac{1}{96}. \qquad (18)$$

5) Noting that $p(a)=p(b)$, $p(d)=7p(e)$, $p(h)=3p(i)$, and solving, we get

$$[p]=\frac{1}{1663}\times[64\ 64\ 127\ 441\ 63\ 122\ 106\ 147\ 49\ 288\ 192]. \tag{19}$$

6) The density from 32/64 to 34/64 is $64/1663\times 64/1 = 4096/1663$,
The density from 34/64 to 36/64 is $127/1663\times 64/2 = 4064/1663$,
The density from 36/64 to 44/64 is $441/1663\times 64/7 = 4032/1663$,
The density from 44/64 to 46/64 is $122/1663\times 64/2 = 3904/1663$,
The density from 46/64 to 48/64 is $106/1663\times 64/2 = 3392/1663$, (20)
The density from 48/64 to 52/64 is $147/1663\times 64/3 = 3136/1663$,
The density from 52/64 to 58/64 is $288/1663\times 64/6 = 3072/1663$,
The density from 58/64 to 64/64 is $192/1663\times 64/6 = 2048/1663$.

7) Shift averages for the intervals of (6) are found to be

4.5, 7, 3.375, 2, 2, 1.75, 1, and 1, respectively.

This leads to a shift average of 2.67 for the divisor 35/64.

Suggested Alternate Method

It is usually easier to postulate a form for the steady-state density function than to go through the above steps. In particular, assuming the density function to be piecewise uniform with discontinuities only at the end-points obtained in step 2 usually permits us to solve for densities of step 6 in a slightly more direct way. This method of assumed form was generalized to cover divisor intervals and was used to obtain the probability density functions tabulated in Appendix II.

Appendix II

Steady-State Probability Density Function of the Remainder for the Indicated Divisor Intervals

In each of the intervals given below, the steady-state density function is found to be piecewise uniform and monotonically decreasing. In Table IV, the points of discontinuity are listed as functions of the divisor and the ratios of the various levels of uniform density are given. This information is sufficient to determine the steady-state remainder distribution for any divisor in one of the tabulated ranges. For example, if $D=0.875$, we have a point of discontinuity at $2D-1=0.75$. Since the density levels are in the ratio 2:1, we determine that the density in the range $[0.5, 0.75)$ is 8/3 while that in the range $[0.75, 1.0)$ is 4/3. For brevity, we have not shown how the steady-state shift averages of Table I have been obtained from Table IV. We have also omitted the general steady-state solutions for divisors of the form $1/2+2^{-k}\hat{s}(k=2, 3, \cdots)$ even though most of the individual steady-state averages of Fig. 5 correspond to divisors of this form. Let it finally be noted that the divisor intervals included in Table IV include almost 85 per cent of the entire remainder range and that a steady-state average may be determined for any rational divisor not included. The proof that Table IV actually yields the steady-state density function for all of the divisor values shown is straightforward but too cumbersome to be included.

TABLE IV

Divisor Interval	Discontinuities	Density Ratios
[0.75, 1.0)	$2D-1$	2:1
[0.625, 0.75)	$4D-2$, $3-2D$	4:3:2 4:2 when $4D-2=3-2D$)
[17/28, 0.625)	$14D-8$, $8-12D$, $3-2D$, $8D-4$	16:15:14:10:8 (16:14:10:8 when $14D-8=8-12D$; 15:10 when $14D-8=3-2D$)
[33/56, 31/52]	$28D-16$, $16-26D$, $8D-4$, $3-2D$, $8-12D$	32:31:30:26:18:16 (32:30:26:18:16 when $16-26D=28D-16$)
[9/16, 7/12]	$8D-4$, $4-6D$, $3-2D$	8:7:6:4 (8:6:4 when $4-6D=8D-4$)

Appendix III

First-Iteration Probability Density Function of the Remainder for Several Initial Distributions ($D=2/3$) (Fig. 10)

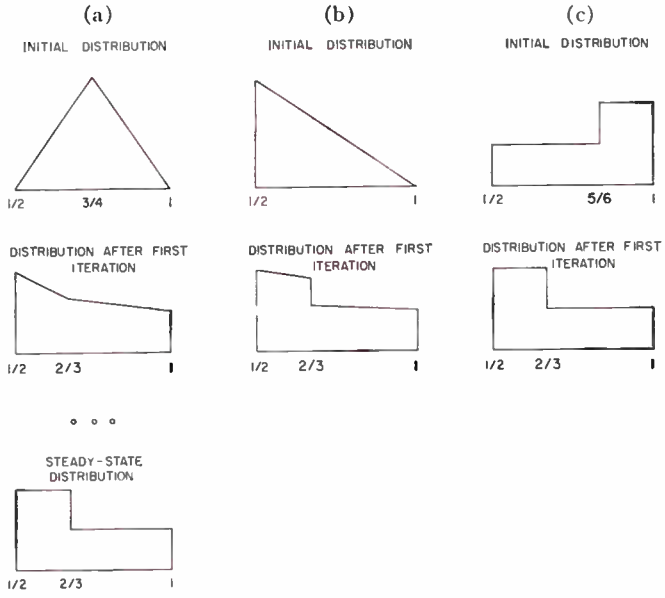

Fig. 10.

Acknowledgment

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Computer Memories A Survey of the State-of-the-Art*

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Because of the fundamental role played by high speed memory (or storage) units in computers, and because of the breadth of new activity and the wide interest in this aspect of computers, Dr. J. A. Rajchman was requested to explain significant techniques and devices that perform the memory function. Specialists and non-specialists alike will find this to be a useful, interesting, and authoritative presentation of the state-of-the-art. —*The Guest Editor*

Summary—**Computer memory developments of the last decade, the present state, and efforts for improvements are surveyed. The following topics are included: principles of storage and selection of random-access memories; principles and engineering considerations of current-coincident-driven core memories; magnetic decoding and load-sharing switches; word-organized one-core and two-core-per-bit memories; fast and impulse switching; transfluxor memories; non-destructive read-out memories; ferrite apertured plates; twistors; fixed read-only memories; thin magnetic film memories—dots, sheets, coated wires and rods; present operational memories typically with capacities of 10^5 to 10^6 bits and read-write cycles of 2 to 15 μsec; likelihood of the order of 100-nsec read-write cycle times attainable with ferrite and thin film memories; consideration relating to large capacities; ferroelectric memories attempts; cryoelectric superconductive memories—principle, superconductive films, Crowe cells, continuous sheets, systems, and the outlook for large capacities; tunnel diode memories which promise a read-write cycle of the order of 10 nsec; and outlook for content addressable memories.**

I. Introduction

COMPUTING, or more broadly, processing of information, consists of causing the interaction of some parts of the information to interact with others in order to produce new information and in general of compounding this procedure by causing interactions between parts of the new information. Since these steps are successive and, in general, all input information is not available simultaneously, provisions must be made for storing information. The basic idea of modern digital computers consists of extending the necessary storing of the information to be processed to include storage of the program describing the process to be performed. It is not surprising, therefore, that the art of storing information is central to the whole art of digital computers.

In general, the storing and processing functions are separate. There is a central memory to and from which all data are routed, and a processor, which receives from the memory data to be processed and the description of the prescribed process, and which delivers back to the memory the resulting new information.

The routing to and from the memory can be obtained, in principle, by the sequential flow of data and programming information, provided this information is properly preordered. Such serial access has been investigated extensively because it is well suited to the physical motion of tapes or drums, the natural propagation of disturbances in delay lines, the flow of signals from a continuously scanned electrostatic storage tube, etc. It has been found that the required preordering of information is often more onerous than the execution of the desired processing; more detrimental yet is the fact that the necessity of advance ordering prevents (or at least greatly restricts) the use of a key programming tool, namely the possiblity of conditional addressing. This is the possibility of making the choice of data to be taken at any time to be dependent on the results of the process in progress. Clearly, what is needed is free access to any information at any time, independent of previous accesses. Selectively addressable electronic memories, or "random"-access memories, so called to emphasize the freedom of accessibility, have been conceived for this purpose and mark the real advent of modern high-speed computers.

A random-access memory is a store of information words or groups having a fixed number of bits which are codes for numbers, characters, orders, etc. Each m-bit word is associated with an identifying label, or address, which itself consists of a fixed number n, of bits. To insert information into the store, *i.e.*, to write or "read-in" into it the m bits of the word, the n bits identifying the address and a signal commanding write-in are given. This causes the particular m-bit word to be stored. To read-out any word, its n-bit address and a signal commanding read-out are given. This causes an m-bit output from the memory corresponding to the selected stored word.

The storage capacity of the memory is $m2^n$ bits or 2^n words of m bits, if all possible n-bit addresses are permissible, as is commonly the case. The time required for access is in general different for read-out and write-in. The operation of most present-day memories requires that both steps be taken for every access so that the sig-

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nificant time is the cycle time required to accomplish both read-out and write-in at a certain address and leave the memory available for the next access. Unless otherwise stated, we shall call this the access time.

This paper surveys random-access memories with a capacity in the range of one hundred to millions of words of one to hundreds of bits each, with an access time ranging from a fraction of a microsecond to tens of microseconds. This is the range of present, and presently sought for, high-speed electronic memories. The paper does not include memories with a capacity of one or a few words which are usually called registers and which should be grouped with logic circuitry with which they are usually intimately associated. Nor does it include the important class of electromechanical memories such as disks, drums or fast-stop-go tapes, with which a degree of random access and large capacities have been achieved, but which have relatively long access times ranging from a few tenths of a second to tens of minutes.

II. General Considerations

A few general considerations on possible methods of making random-access memories may be useful, to put into perspective present solutions and the search for better ones. For every bit, there must be a discrete physical storage cell capable of being set into one of two distinct states. The cell must remain in the set state indefinitely, or until it is changed to the other state. The selection of a particular cell, for establishing or ascertaining its state, must be determined uniquely by the presence of the n signals defining its address. There are thus two basic aspects to memory: storage and selection.

A. Storage

The two distinct states of the storage cell can be natural states which require no external energy to be maintained. This is the case for ferromagnetic, ferroelectric, and superconductive cells, all of which have a hysteretic characteristic, *i.e.*, the following property. The quantity defining the state (magnetic induction, electric polarization, or induced supercurrent) has remanent states corresponding to no energization. The sign of this quantity can be changed by an excursion of the energizing force (magnetizing force, electric field, or primary inducing current) from zero to a sufficiently positive or negative value at which it remains for a sufficiently long time and then back to zero. The required absolute value of the excursion and its timing depend on the amount of stored energy (magnetic, electric, or magnetic, respectively) and the details of the mechanism of energy loss during the transitions. In all three cases, the amount of required energy is controllable by existing electronic elements, and the time can be in the microsecond range. These possibilities, and the fact that the nonlinear response to energization facilitates the selection of the element, as will be explained, have made the ferromagnetic, ferroelectric and superconductive elements prime contenders for storage cells of random-access memories.

Storage elements requiring external energization to maintain the stored state have been the basis of important developments and some types are running contenders, particularly for ultra-high-speed memories. The external energization can be used to create artificially two stable states. For example, an electrically floating target subjected to constant electron bombardment will assume one of two stable potentials under conditions insuring the proper secondary emission mechanism. This has been exploited in the selective electrostatic storage tube [1] with matrix grid selection as well as in deflected beam barrier grid tubes [2]–[4]. In a more recent proposal [5], tunnel diodes are maintained by a dc source at one of two stable potentials existing by virtue of the negative resistance of the device. In the above examples, the stable states are static and maintained by dc power. Dynamically stable elements maintained by ac power are possible also [6] as, for example, parametrically excited oscillators which can be made to oscillate in one of two opposite phases at a frequency one-half that of the energizing source. External energization can also be used to hold information in elements which have no stable states, such as condensers. Two distinct ranges of stored energy can be maintained, despite unavoidable energy losses, through the artifice of periodic rechanging of every element in the memory. This is the principle of the diode condenser memory [7], [8] and Williams' [9] storage tube.

B. Selection

The selection of one out of 2^n words (typically 256 to 16,384) according to its n-bit coded address ($n=8$ to 14) is a decoding function basic to random-access memories and has been one of its main problems. In the mid-forties, when the first high-speed memories were being actively developed, electronics was still chiefly vacuum-tube electronics. A natural solution to the problem was the use of an electron beam which could be deflected to select electrostatic storage elements on a target in the manner so successfully employed in television pick-up tubes. The required amplitude of deflection is obtained through digital-to-analog conversion [3], [9], a process which turns out to be a difficult circuit task. Purely digital selection through the use of an array of beams switched by combinatorially connected control electrodes avoids the conversion difficulty but leads to rather complex tube structures [1]. The early fifties saw the advent of the first core memories [10], [11] in which selection by a reasonable number of tube drivers was made possible utilizing the nonlinear property of the storage cores. This was also the start of the era of solid-state electronics through the practical appearance of the transistor, which was soon applied to core memories. Transistor-driven core memories have become, and are today, the classic form of random-access memories.

In attempting a unified survey of present and possible future memories, it is convenient to consider the selection problem from a general point of view without regard to its historic evolution.

Conceptually, the simplest organization of a random-access memory consists of completely separating the address selection function from the storing function. Such memories are variously known as "word-organized," "switch-driven," or having "linear" or "end-on" selection. The memory elements are in a rectangular array with each row line corresponding to a word and each column line to a bit (Fig. 1). The 2^n word lines are driven by a decoder switch which selects one of the lines uniquely from its n-bit coded address. To write-in, the bit lines are energized according to the m bits of the word to be stored. To read out any word, the appropriate word line is selected, and the signals of the bits corresponding to the stored word appear on the bit lines.

Great economy in decoder switching is obtained if the storing cells are made to participate in the address selection function. Consider, for example, that the cell can respond to two simultaneous address selecting signals, instead of one. It is then possible to energize the 2^n words by two $2^{n/2}$ sets of selecting lines x and y (Fig. 2). The economy of the required decoder is evident, as the single n to 2^n decoder (*e.g.*, $n=12$ to $2^n=4096$) has now been replaced by two much smaller decoders of $n/2$ to $2^{n/2}$ (*e.g.*, $n/2=6$ to $2^{n/2}=64$) capacity. The logic at the cell level is more complicated, as two address signals instead of one must be coped with. Greater participation to the switching function by the storing cell could be obtained by having 3, 4 or 5 (up to n) selection signals on the cell and providing the appropriate cell logic. It is found that two signals are sufficient to bring the decoder problem to within practical proportions, and the complication resulting from the use of additional signals is generally not warranted. Memories organized with such partial cell participation in the selection are variously called "bit-organized," "current-coincident," or "coincident."

The practical attainment of large memory capacities, *e.g.*, hundreds of thousands to tens of millions of bits, obviously requires the possibility of making very simple and inexpensive storing cells. Hysteretic elements provide a simple means to obtain storage and the required logic at each element. This is achieved as follows. Let there be two periods to every access, a read and a write period. To read, let the single or a linear combination of two or more word-selecting signals energize the hysteretic device in a given polarity, so as to exceed the switching threshold (Fig. 3). This will cause the switching of those elements of the selected word, and those elements only, which were initially in the remanent state previously brought about by energizations of the opposite polarity, and will leave unaffected all others. The switching of a hysteristic element can create a transient signal (*e.g.*, an induced voltage) in an appropriate circuit. In general, these signals occur on m

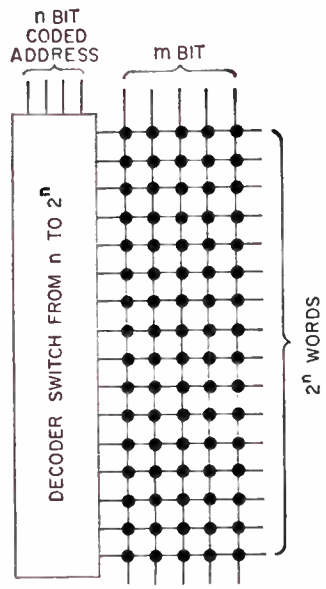


Fig. 1—Word-organized memory.

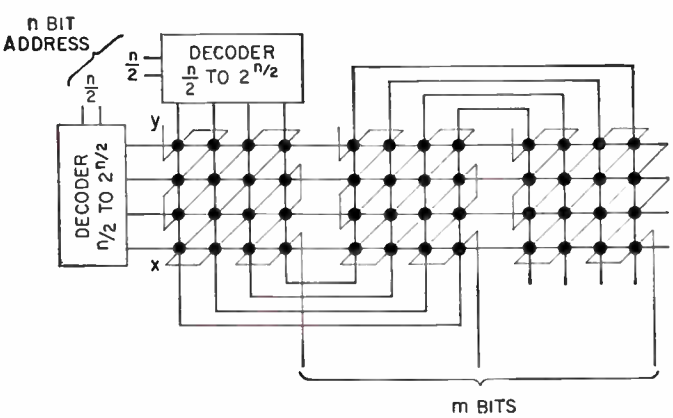
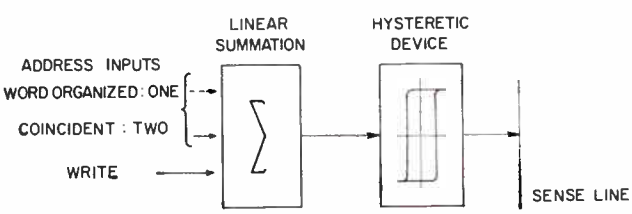


Fig. 2—Coincident- or bit-organized memory.



	READ PERIOD	WRITE PERIOD
ADDRESS	+	−
DIGIT SENSE	SENSE	
DIGIT WRITE		+OR −

Fig. 3—Schematic of hysteretic memory cell.

common circuits each linearly coupling the 2^n elements belonging to a given bit of all words and thus constitute the m required read-out signals. In the second, or write step, the address signal or signals are of opposite polarity from those in the read step, and are linearly combined with the bit write-in signal. The amplitudes of all signals are chosen so that the combined signals never reach the threshold of switching except on those bits of the selected word which have the proper bit write-in signals. These m-bit write-in signals can have the same or opposite polarity from the address write signals depending upon the particular system design. The written-in word can be the word just read out in the previous read period and can thereby restore the information momentarily lost in the so-called destructive method of read-out of hysteretic devices just described. It can also be a new word to be inserted in the memory, in which case the read-out signals of the first period are ignored.

The two-period read-write access system is naturally suited to hysteretic devices. The first period in which all elements are brought to a standard cleared state serves for read-out as well as one polarity write-in, so that in the second write-in step only the elements to be brought to the opposite state need be switched.

Hysteretic elements furnish all storage and logic functions required of an element of a random-access memory, provided that the threshold for the onset of switching is distinct enough so that the desired linear combination of driving signals produces switching while no switching occurs even with a single dissident contributing signal. It is also necessary that whatever transients occur at unselected elements due to partial excitations should not unduly add up in the sensing circuits to avoid masking the read-out signals which are also transients. These conditions require in general a so-called rectangular hysteresis loop and uniformity of properties from element to element. How much deviation from ideal properties can be tolerated depends on the precise nature of the memory system. This important question is considered in the following specific memory descriptions.

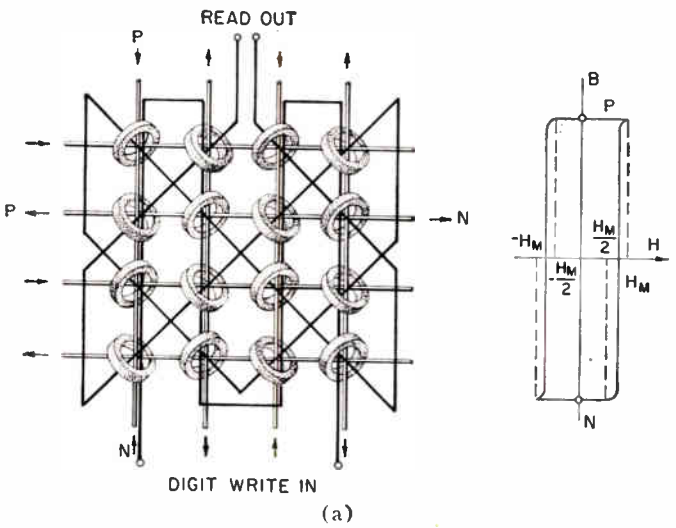
III. Magnetic Memories

A. Current-Coincident Core Memories

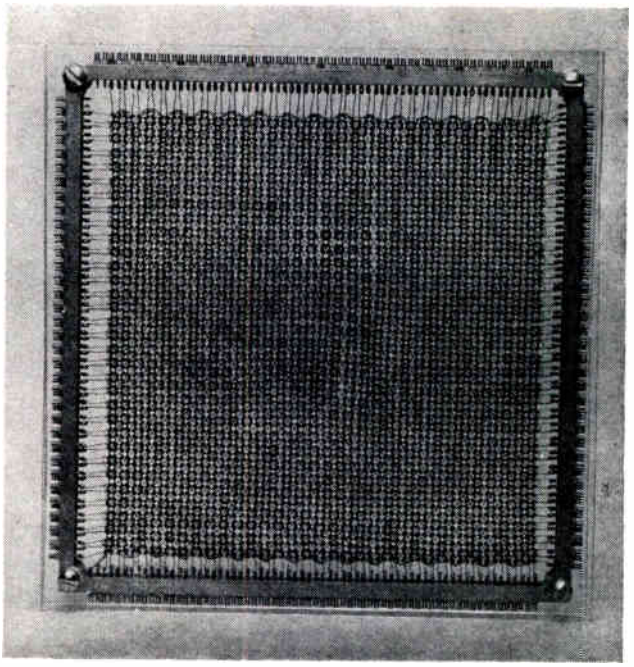
1) Principle: Arrays of individual cores operated in current coincidence were the first type of hysteretic memory introduced about a decade ago [10], [11]. First experiments and models were with ribbon-wound molybdenum permalloy cores [10]–[12]. Bit-organized ferrite core arrays are today the most widely used type of high-speed memory.

The cores corresponding to each bit of the word are arranged in a plane in rows and columns, *i.e.*, $2^{n/2}$ rows and $2^{n/2}$ columns for 2^n words. There are m planes corresponding to the m bits of the word. Each core is linked by four windings. Two of the windings are connected in series by rows and columns and the other two, the bit-write and the bit-sense or read-out windings, are common windings linking all cores in a plane. "Single-turn" windings consisting of straight conductors are generally used (Fig. 4). All cores are magnetized to one or the other of two remanent inductions represented by the points P and N on the idealized hysteresis loop of the figure. In this state the array is holding information previously written in.

To read out, equal pulses of current are applied simultaneously to row and column windings in each array corresponding to the selected word. The amplitude of these currents is so adjusted that their doubling effects produce sufficient magnetomotive force to exceed the knee of the loop for the selected cores in each array at the intersections of these lines, but insufficient to exceed the knee for the other cores on the selected



(a)



(b)

Fig. 4—(a) Current-coincident memory. (b) Typical core plane.

lines where they act singly. Consequently, the selected cores will be magnetized in a standard direction, for example toward P, while all other cores will remain unaffected. It follows, therefore, that the existence of an induced voltage in each of the m read-out array windings, which can be caused in each array only from the switching of the selected core, will indicate that that core was switched from N to P, while absence of such voltage indicates that it was originally in state P. The read-out is ascertained by the pattern of voltages on the m read-out windings. The interrogation may change the stored information in the so-called "destructive" read-out mode and must be rewritten to be retained in the memory, as was mentioned previously.

To write, pulses of current are applied simultaneously to the selected row and column windings of all arrays as well as to the individual bit write windings of certain arrays. The amplitudes of these pulses are equal (and equal to those of the read-out pulses) and therefore too small to singly change the state of any core. The row and column pulses tend to drive the cores toward N and the bit write pulses toward P. Consequently, only those selected cores subject to row and column pulses in arrays where the inhibiting action of the bit write pulses are absent will be driven to N, all others will remain in P. The inhibit pulses will not affect any cores on unselected addresses.

This memory system depends on the discrimination, due to a two-to-one ratio of excitations on the selected cores to that on the most energized nonselected cores, and yet the selection is according to three signals: two addressing and one write signal. This is possible because the hysteresis loop has, in fact, two thresholds, one on the positive and one on the negative range of magnetomotive driving forces. The operation of the system is shown by the schematic of one element Fig. 5(a).

2) *Disturb Voltages:* Departure from ideal rectangularity of the hysteresis loop of available materials was an important limitation in the development of the core memories. Only moderate rectangularity is sufficient to prevent cumulative demagnetization due to repetitive half-demagnetizing steps, so that loss of stored information has never been a serious problem. On the other hand, the voltages induced in the read-out winding by the half-excited cores on the selected lines did present a problem, as these "disturb" voltages are additive and may mask out the desired read-out signal, particularly in large arrays. Direct pick-up from the exciting windings also adds to the disturbs. Common practice is to use a reading winding in which the directions of core linkage are opposite on the two halves of every line, as in a "checkerboard" pattern, so that the disturb voltages tend to cancel each other (Fig. 4). The cancellation depends on the uniformity of core properties. Great efforts have been devoted to methods of fabrication and of testing of cores. Very good results have been obtained in recent years. However, cancellation is, in general, not a sufficient remedy to the problem of the disturb voltages, even with the most uniform cores.

The reason for this is that the reversible flux change due to partial excitation of a given polarity is, in general, somewhat different for the two states of remanence of the core, so that the degree of cancellation depends on the pattern of remanent states established by the particular stored information. The difference between these two flux changes is commonly referred to as "delta-flux." This difficulty can be alleviated by using, after writing, a routine to "postdisturb" or "predisturb" the core with a demagnetizing half-excitation, a procedure which tends to equalize the reversible flux changes for the two remanent states during subsequent half-excitations and thereby improve the cancellation of disturb voltages.

The most widely used artifice to discriminate against the disturb voltages consists of time strobing the output voltage, and is based on the fact that the unwanted reversible flux changes on the half-exited unselected cores occur much faster than the wanted irreversible flux change on the selected core. Another method [13] consists of integrating the read-out signal, preferably over a reading cycle with two periods, to effectively discriminate between reversible and irreversible flux changes. Still other schemes have been proposed. For example, the row and column can be energized one after the other so that only the half-excited cores on the column contribute to the disturb read-out voltage [14]. This system favors the use of a rectangular array with long rows and short columns. Among all the methods which deal with the disturb problem, strobing is the most commonly used, as it is very effective and does not lengthen the time required for access to the memory.

The problem of the disturb voltages was brought sufficiently under control in the early fifties so that

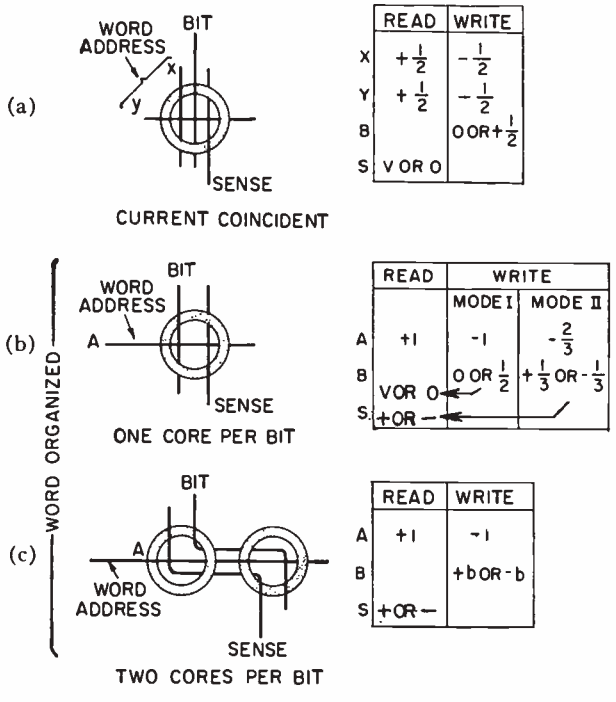


Fig. 5—Storing element and energizations for (a) current-coincident memory, (b) word organized one-core-per-bit, (c) word organized two-cores-per-bit.

arrays of $16 \times 16 = 256$ cores were being operated in computers, and arrays of 10,000 cores were being developed in the laboratory [13]. The rectangularity and uniformity of present-day ferrite cores is such that arrays of $64 \times 64 = 4096$ cores up to $256 \times 128 = 32{,}768$ are in use. In large arrays, the problem of disturb voltages is solved by the simple expedient of splitting the read-out winding and using a separate sense amplifier or preamplifier in each part. A particularly advantageous way to split the winding is by grouping together square subdivisions of the plane along diagonals, as then there are disturb contributions only from the cores on the selected lines contained within the subsquare including the selected core [15], [16].

3) Cores: In most present-day ferrite core memories, the mechanism of switching of the square loop cores is primarily through domain wall motions, for the case in which switchover occurs in times longer than 10^{-7} second. The switching time T is related to the magnetizing force H by

$$T(H - H_c) = S_w, \tag{1}$$

where H_c is the coercive field, and S_w a constant, the switching constant [17].

In the current-coincidence mode of operation, the total magnetizing force due to the addition of row and column current drives cannot exceed $2H_c$, since the magnetizing force due to the row or column drive alone cannot exceed H_c. In practice, it is generally found that an optimum discrimination between full- and half-excitations is obtained when $H = 1.5H_c$. It is seen, therefore, that the switching time is proportional to the switching constant and inversely proportional to the coercive force.

The commonly used cores are made of manganese magnesium ferrite. By varying the composition and heat treatment it is possible to obtain a fairly wide range of coercivity. However, it is found possible to exert only a small influence on the switching constant S_w, which is of the order of 10^{-6} oersted-second for a wide variety of ferrite materials. Consequently, the present practice consists in making so-called fast materials with relatively high coercive force, and so-called slow materials with relatively low coercive force, but among the various compromises between speed and required driving current, the essential figure of merit S_w remains nearly constant. This is also true for cores made from thin metal ribbon, such as were used in early memories.

In any case, relatively large ampere-turns are required to obtain the requisite magnetomotive forces. The use of single turn windings is dictated primarily by simplicity of construction, but is also necessary to avoid excessive back voltages and delays in large memories. Since the magnetomotive force is inversely proportional to the flux path length, ring-shaped cores are universally made of as small a radius as is technologically possible, so as to minimize the required driving current. Some of the early experiments [13] were with 0.034 inch ID, 0.050 inch OD, but most of the first memories used 0.050 inch–0.080 inch cores, which were considered the smallest practical to make and wire. Present improved manufacturing is mostly with the smaller 0.030 inch–0.050 inch cores. Typical characteristics of commercially available cores are listed in Table I.

4) Addressing and Digit Write-Read Circuits: The functions required of the addressing circuits are the following (Fig. 6). The n-bit address, stored in a register, must be decoded. In the current coincident memory two decoders for $n/2$ bits each are required. The two sets of $2^{n/2}$ outputs of the decoders are used to drive the row and columns of the core arrays. Positive and negative pulses are required for the read and write cycles, respectively.

The advent of relatively high-current transistors has brought about an all diode-transistor solution to addressing circuits which is in common use today. Diode or transistor decoders of the combinatorial type are often made in two steps [15], each $n/4$ to $2^{n/4}$. The outputs of the decoders are amplified by high-current-output transistors which drive the memory. A read-write gate determines the polarity of the drive. Various ways of obtaining the two polarities are used. In some cases the output transistors can provide both polarities directly [15]. In others, a transformer couples the memory lines to two single-polarity driving transistors [18]. In some earlier hybrid circuits, the output transistors "steered" the current from a tube-drive [19].

TABLE I
TYPICAL CHARACTERISTICS OF FERRITE MEMORY CORES

Outside Diameter	mils	0.050	0.050	0.080	0.080	0.040
Inside Diameter	mils	0.030	0.030	0.050	0.050	0.025
Height	mils	0.015	0.015	0.025	0.025	0.012
Switching Time	μsec	0.15	1.3	1.2	2.7	0.35
Drive	ma	1100	350	740	360	800

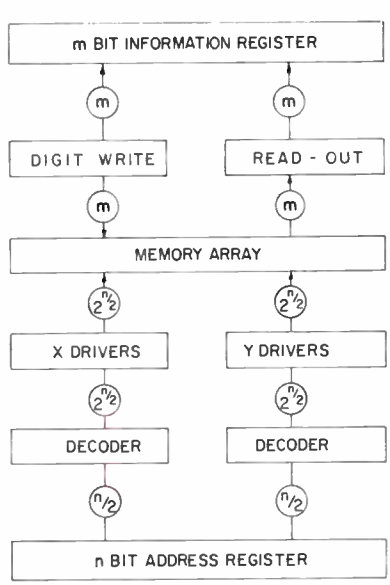


Fig. 6—Schematic of typical current-coincident memory system.

The m bits of information to be stored in or to be read from the memory are generally stored in a register which serves not only for the input and output but also as a buffer necessary in the process of rewriting the information momentarily lost from the arrays in the destructive read-out process. Transistor amplifiers, similar to those used for addressing, are used to supply the digit-write inhibit pulses and are triggered, on command to write, according to the bits stored in the register. The m read-out signals, after suitable amplification and strobing, set the register on command to read.

The transistor sensing circuits are complicated by the pick-up on the read winding resulting from the excitation of the write winding of the preceding write-in operation. Without adequate measures, this unwanted pick-up would be many times larger than the desired signal and would paralyze the relatively sensitive amplifiers for a time which could well be longer than the total time required to read, write, and decode. It is customary to wind the digit write and digit sense windings on the core arrays so as to minimize both magnetic and capacitive pick-ups. This is achieved by a pattern of alternate core orientations and right angle crossings of write and sense winding wires (Fig. 4). A further artifice consists of using carefully balanced sense amplifiers transformer-coupled to the sense windings.

A typical transitor-diode-driven current-coincident core memory of 4096 words of 40 bits each may require about a thousand transitors and several hundred diodes.

B. Magnetic Switching

The relatively large numbers of transistors and diodes and the considerable power required may be reduced by using magnetic switches. These were first conceived in the pretransistor era to reduce the number of high-current tube drivers and to simplify decoding. Magnetic switches for decoding and load-sharing are still useful with the advent of transistors and are in common use.

Consider an array of switch cores linked by row u and column v windings [13] (Fig. 7). All cores are biased by a direct current. The excitation of a u or v line alone is just sufficient to cancel the bias and therefore does not switch any core. The simultaneous excitation of u and v switches the selected core. At the termination of the u and v drives, the dc bias restores the selected core to its initial state. Each core of the $u \times v$ array is provided with an output winding which is coupled to a row x of the memory array. Another $u \times v$ array is used to energize column y of the memory. The switches accomplish several functions: 1) they provide part of the address decoding; 2) they provide both polarities of output with single polarity inputs, thus simplifying the driving problem as well as the winding of the memory array; and 3) they allow convenient means for impedance transformation, and matching to tubes or transistors, as it is relatively easy to provide several turns on the switch cores which are larger and less numerous than the memory cores.

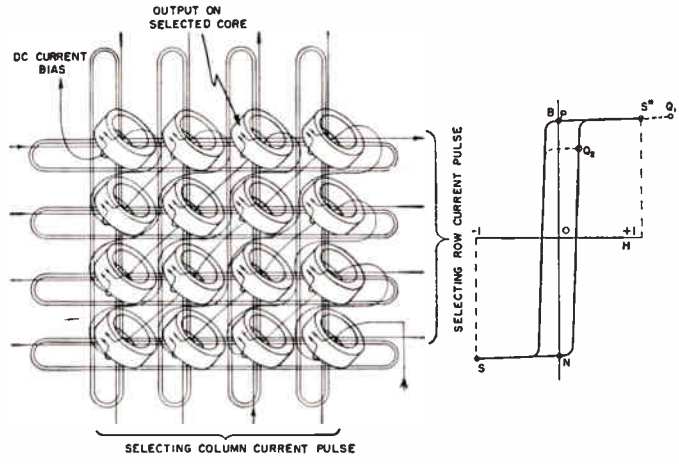


Fig. 7—DC-biased magnetic switch.

There are other modes of operating the switch which do not require a dc bias. For example, in the switch array the selected line v can be driven in the switching direction while all lines u except the selected one can be driven in the inhibiting direction [20]. Alternatively, by the proper connection of outputs in shunted groups, it is possible to operate the switch in a so-called "set-a-line" mode in which the selected line u is driving and the selected line v is inhibiting [21]. It is also possible to use combinatorial magnetic switches [11]. Among all of these decoder-type switches, the dc bias type is the most widely used.

Alternatively to a primary decoding function, magnetic switches can be used for channeling the power of several sources to a single load. Such "load-sharing switches" [22]–[24] permit the use of relatively low-current transitors to provide the relatively large current for memory arrays. The energization of a number of inputs can be made to drive a generally smaller number of cores in such a way that the selected core receives the total excitation from all the sources, while the other cores receive zero excitation. Fig. 8 illustrates the wiring arrangment for the case of eight inputs and outputs. The signs + and − refer to the direction of linkage through the core of each of the eight input windings linking the cores in series. The currents from the source are assumed to be + or − one unit of current. It is clear from inspection that if the input circuits are excited according to the pattern of polarities corresponding to any one of the eight patterns of winding polarities of the cores, the selected core will have eight units of excitation while other cores will have precisely no excitation. In such a switch, the combinations of windings are exploited for load-sharing purposes rather than to gain a combinational advantage in coding or decoding. In general, the inputs to such a switch must be decoded by some other means. It should be mentioned that there are no particularly severe requirements on the nonlinearity of the cores, as the saturation characteristics are useful only to attenuate the effects of whatever inequalities of amplitude there may be between inputs. Load-sharing switches are in use with large capacity memories [20].

CORES \ INPUTS	1	2	3	4	5	6	7	8
1	+	+	+	+	+	+	+	+
2	+	−	+	−	+	−	+	−
3	+	+	−	−	+	+	−	−
4	+	−	−	+	+	−	−	+
5	+	+	+	+	−	−	−	−
6	+	−	+	−	−	+	−	+
7	+	+	−	−	−	−	+	+
8	+	−	−	+	−	+	+	−

Fig. 8—Pattern of windings for a load-sharing switch.

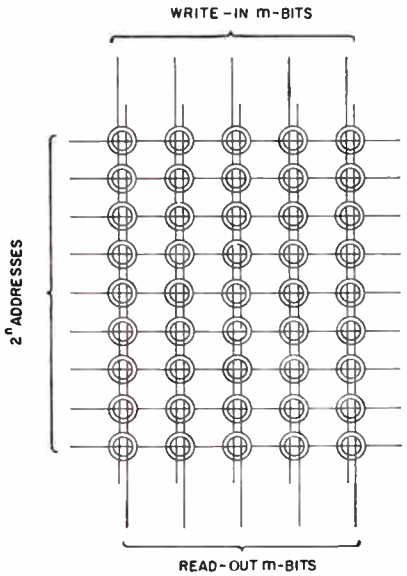


Fig. 9—Word-organized core memory.

It is also possible to combine decoding with load-sharing functions [11], [24], if some excitation on nonselected cores is tolerated. For such switches, cores with pronounced nonlinearity are necessary to minimize unwanted outputs on partially energized nonselected cores.

C. Word-Organized Core Memories

1) One-Core-per-Bit: Consider an array of cores with row and column windings (Fig. 9). Let each row correspond to a word and each column to a bit of the words. Assume that all cores are in states P or N and are storing information previously written in.

To read out a given word, the desired row is energized with an amplitude large enough to switch the cores of the row to one of the two states, *e.g.*, N. Voltages are induced simultaneously on all the columns in which the cores of the row being interrogated were previously in state P, and only on these columns. These are the read-out signals. The read-out step is truly by external word addressing and involves no current coincidence. This has two important implications. First, the read-out signals are free from any disturb signals from cores of other words, as these cores are not energized at all. The only undesired signals on the read-out column are due to "elastic" flux excursions of the cores on the selected row in state N being driven further into saturation. The wanted flux change from state P toward the saturated state N is always easily distinguishable from these elastic flux excursions. Consequently, considerable deviation from ideal rectangularity of the hysteresis loop is tolerable. Second, the read-out current is not limited in amplitude by the selection mode to produce a magnetomotive force equal to 1.5 or $2H_c$, but can be as large as desired, many times larger than the coercive force, H_c. Consequently, it is possible in principle to make the switching time during read-out arbitrarily short simply by making the selecting current sufficiently large [see (1)]. The speed is limited by the practical difficulty of obtaining an adequate external switch.

To write or rewrite, the current in the selected row is reversed, *i.e.*, it tends to drive the cores to P. Simultaneously, digit write currents are applied to certain or all columns. The amplitude of the write current and the amplitude and polarity of the digit currents must be so chosen that the desired cores on the selected row are switched to P, while cores on unselected rows are not switched at all. This can be obtained in different ways. For example, the selected row and the column currents could be of the same polarity and both equal to half the nominal switching current, the column currents being present only in columns where the selected core is to be in P. Conversely, the selected row current could be the full switching current and the digit currents on the complementary columns of inhibiting direction and half amplitude. In both cases the ratio of excitations between the selected core and the most energized nonselected core is 2:1. This ratio can be increased to 3:1, by using 2/3 of the nominal drive on the selected row and 1/3 of the drive on all columns, the polarity of the column drive being + or − depending on the polarity to which it is desired to magnetize the cores. Shorter write time is possible with the greater ratio. Even so, the write-in step is not determined by external means but depends on the drive current amplitudes. Therefore, the currents and the resulting speed of writing are limited. The schematic of a one-core-per-bit word-organized memory is shown in Fig. 5(b).

The advantages of word-addressed memories are obtained at the expense of an external driving switch. Transistor switches driven by diode or transistor decoding switches can be used. To obtain both polarities of drive, a single transistor per word can suffice as it is well suited to deliver very large currents of one polarity for read-out and a relatively small current of the opposite polarity for write-in [15]. Memories so driven with read-out times less than 1 μsec and write-in times of several microseconds have been reported [15]. It is also possible to use magnetic switches of various types.

Depending on the stored word, there can be any number from 0 to m of cores switching when a word line

is energized. To keep the word current constant despite this variable load, large resistances in series with the word line are generally resorted to. This wastes power and is particularly objectionable when magnetic switches are used.

2) Two-Cores-per-Bit: The driving switch can be simplified [21] by the use of two-cores-per-bit instead of one, as the voltage induced on the selected row can be made independent of the stored information, *i.e.*, the same for every access. The use of two-cores-per-bit has also fundamental advantages for high speed, as is explained later [25]. The two cores store one bit of information by being either in states PN or states NP [Fig. 5(c)]. On read-out, a large current is applied to the selected row and brings all cores on the row to state N. This induces a voltage on one or the other column winding of the pair belonging to each digit. By connecting the two column windings in series opposition, a positive or negative read-out voltage is obtained depending on the stored bit. This arrangement automatically neutralizes the effect of the elastic excursions of flux of the cores driven further into saturation. To write-in or rewrite, the current on the selected row is reversed and, simultaneously, positive or negative currents are sent through the series connected column pair depending on the nature of the bit to be written in.

Word addressing by a magnetic switch has a number of advantages. Fig. 10 shows a dc biased core switch, each core driving a word of the memory. Fig. 11(a) shows a switch core and its memory load in the case of a word with a single bit. There are three identical cores, the switch core and the two memory cores. Assume the resistance of the coupling electric loop to be negligible. Assume also that the switch core is initially in state N and the memory cores are either in states NP or PN. When the selecting currents on the rows and columns of the switch overpower the dc bias and reverse the switch core from N to P, whichever memory core was in state P is switched to state N. This occurs because the total amount of flux linked by a zero resistance loop must remain constant. The identity of the memory core being switched determines the polarity of the read-out signal on the digit winding. When the selecting currents driving the switch terminate, the dc bias restores the switch core from P to N. This tends to switch both memory cores to P. If there were no current in the digit winding at that time, the two identical memory cores would be switched halfway, absorbing equally the flux change of the switch core. A subsequent read-out, due to a new switching of the switch core from N to P, would switch the two memory cores equally, and consequently no read-out voltage would be obtained. However, if during the return of the switch core from P to N, a current is sent through the digit winding which favors one core and hinders the other, the flux change in one core will be greater than that in the other. Consequently, on a subsequent read-out, a voltage is obtained as both memory cores are brought to the standard N condition. The read-out voltage depends on the amplitude and polarity of the write-in current in ac-

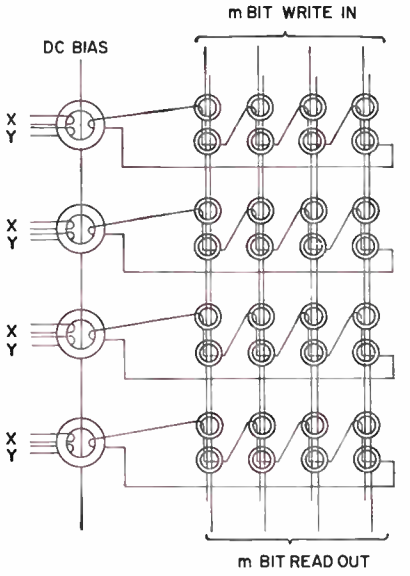


Fig. 10—Magnetic switch driven word-organized memory (two-cores-per-bit).

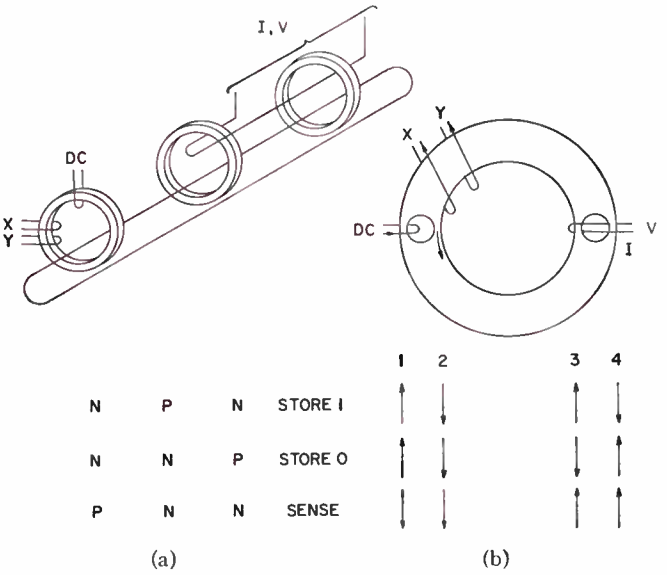


Fig. 11—(a) Switch drive of a two-core-per-bit memory. (b) Transfluxor memory element.

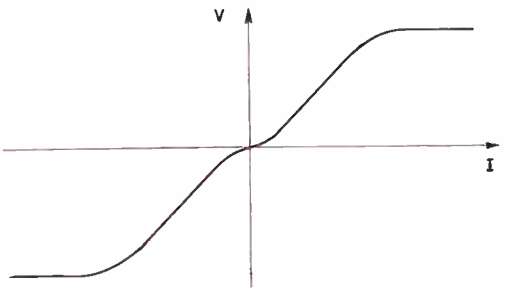


Fig. 12—Read-out voltage vs digit write current for two-core-per-bit memory cell and transfluxor memory element.

cordance with a typical characteristic curve, as shown in Fig. 12.

The system, described for simplicity for a one-bit word, is adaptable to many-bit words. A single switch for the whole memory is made up of cores, each with sufficient large flux capacity to supply the flux changes of the m-bit memory core pairs which it drives.

The system described above depends on transferring a limited amount of flux from the switch core to the memory cores. This principle has several interesting consequences [21], [25]. The read-out step can be arbitrarily fast as in other types of externally addressed memories. The write-in step is still dependent on current selection but the two disadvantages of that selection system, limitation in speed and small tolerances in the amplitude of drive, are largely overcome. The pair of memory cores really stores analog information, *i.e.*, gives a read-out output voltage which is a function of the digit write amplitude according to the characteristic of Fig. 12. For digital storage, only the polarity of the output is ascertained, so that the digit write current can have any value between a minimum which insures no false indications due to unavaoidable inequalities between the cores or to noise, and a maximum which insures that the state of storage of nonselected cores is not altered. The ratio of maximum to minimum permissible amplitude of the write digit pulse has a practical range of 3 to 1 when the durations of that pulse and the address-selecting pulses are of the length dictated by the conventional current-coincident operation. Actually, it is possible to use very intense address drive producing very fast switch-overs not only for the read-out step, but also for the write-in, as some unbalancing of flux distribution between the two memory cores will occur in principle for any value of digit write current. However, it is preferable to use the greatest permissible value of digit write current in order to obtain as large a read-out signal as possible. For very short pulses, this maximum value is several times greater than it is for pulses of duration compatible with conventional current operation. Therefore, there is essentially no significant limit to the maximum permissible drive in the whole read-write cycle, so that two-cores-per-bit magnetically switch-driven memories have the possibility of being very fast.

3) Fast and Impulse Switching of Ferrite Cores: The possibility of using extremely high-current pulses both for the read and the write cycles in a two-core-per-bit word-organized memory driven by a magnetic switch is dependent on the fact that the total flux changed in the memory cores is necessarily limited to the flux in the switch core. Since the flux changes are transmitted through an electrical linkage loop, the flux limitation must result in a limitation of the duration of the induced current in the loop. This demonstrates that it ought to be possible to obtain any desired change of flux in a core in a very short time, provided sufficiently intense current impulses are used. Extensive studies of impulse switching of ferrites in the last few years confirm this expectation [25]–[34].

Let us consider a core brought to a standard level of saturation, as for example the zero state resulting from a large read pulse. When a pulse I producing a field exceeding the coercive force is applied to the core, the core will switch completely provided the pulse is longer than a minimum time T. The relation between I and $1/T$ is made up of two or three straight line segments corresponding to different values of S_w presumably resulting from different switching mechanisms [33]. When the pulse duration t is shorter than T, only part of the flux is reversed, as was found in fast transfluxor setting characteristics [28], [29]. Later extensive experiments [30], [31] with impulse switching of cores revealed a number of interesting properties. For example, an amplitude (*e.g.*, 600 ma) of a short pulse (*e.g.*, 150 nsec) can be chosen to produce practically no flux change, while a relatively small increase (*e.g.*, 200 ma) can produce a substantial change. This nonlinear behavior was applied to a word-organized memory [34] in which the word write current supplies the larger part of the reversing current, and the digit or exciter current, the smaller part, insufficient to disturb nonselected cores. The memory has 1024 words of 80 bits each and is operated sequentially with addressing times of less than 1 μsec. It is believed that comparable cycle times are possible also with random-access operation.

When the duration t of the pulse is sufficiently reduced there is no irreversible flux change, even partial. However the amount of reversible flux change depends strongly on the remanent state of the core and can be used for nondestructive read-out [26], [30], [35]. These effects were first observed [26] with molybdenum permalloy cores with pulses of about 100-nsec duration, and were attributed to domain wall viscosity effects.

4) Transfluxors and Multiaperture Cores: The drive of a memory by a magnetic switch was shown to be based on transfer of flux from the switch core to the memory cores by means of electrical linkages. This concept can be generalized to direct geometrical transfer of flux between branches of cores having multiple flux paths [96]. The principle of the transfluxor and multiple-aperture cores called by other names depends on such transfers of flux. These devices have broad utility for many switching and storing functions, all of which will not be surveyed here. Only their applications to memories will be considered.

A three-apertured transfluxor can be used instead of the switch core and the two memory cores of a one-bit word memory [96], [29] (Fig. 11(b). Here the dc links leg 1, and the selecting currents X and Y link the central aperture; *i.e.*, both legs 1 and 2. When the sum of energizations of the windings X and Y exceeds that of the dc bias by an amount sufficient to produce switch-over between leg 1 and legs 3 and 4, the latter will be brought to saturation. If they have been previously left in unequal states of remanence, this will produce an output voltage on the digit winding linking legs 3 and 4. When the selecting currents X and Y terminate, the dc tends to transfer the total flux of leg 1 through legs 3 and 4. Assuming for a moment that the path lengths 1

to 3 and 1 to 4 are equal, this would produce equal amounts of flux (equal to half that contained in leg 1) through legs 3 and 4. If, during this time, a digit current is sent through the digit winding, unequal amounts of flux will be transferred, because that current will favor transfer of flux to one leg and hinder it to the other. Consequently, the relation between the read-out voltage and write-in current will be similar to what it was for the three cores (Fig. 12). It is interesting to note that the total amount of flux through legs 1, 2, 3, and 4 must not only be constant in this case, but identically zero. For this reason it is necessary to have an additional leg, leg no. 2, which is really a dummy and serves merely to make up for the balance of flux.

If the lengths of path 1 to 3 and path 1 to 4 are not equal, as is true in the case of the core having the geometry shown in Fig. 11, there will be unequal division of flux between legs 3 and 4 even when the digit current is zero. Various geometries are possible to make these flux paths equal. One geometry consists of properly shaping the center aperture in the shape of a "U." Another consists of locating legs 3 and 4 on either side of leg 1 and splitting dummy leg no. 2 in two halves. A right angle aperture can also be used.

In another three-aperture core arrangment [36], a dc bias and X and Y windings through the central aperture are used also. The sense winding is on leg 4 only. The direction of magnetization of that leg stores the bit. To read, the X and Y windings are energized and overpower the effect of the dc in the windings in legs 1 and 2. This causes the flux to be clockwise (Fig. 13) in the whole core and may reverse leg 4 if it was magnetized upwards from a preceding write. At the termination of the X and Y pulses, the dc causes flux changes in legs 1 and 3 only. To write "one" the X and Y currents are applied in the opposite direction causing the whole core to be magnetized counterclockwise, *i.e.*, causing leg 4 to be magnetized upward. In an m-bit arrangment, the bias winding has a pulse component in a direction and amplitude to inhibit the action of the X and Y windings on the digits which it is desired to keep in the "zero" condition established in the read period.

The three-hole cores of the above two systems act simultaneously as the storage cell and as the access switch. Because the operation is dependent on geometry of the core, there is considerably less dependence on the existence of a well-defined threshold of switching, and a greater latitude to deviate from ideal loop rectangularity. This allows a greater permissible range of operating temperatures. The dc bias system allows as large drives as desired, and therefore the speed of operation is not intrinsically limited.

The same advantages of speed and tolerances exist in a three-hole memory core operated in an inhibited flux mode for a word-organized memory [37]. The word line links the central hole, the bit write line links leg 1 and the sense line leg 4 (Fig. 14). To read, a current pulse is applied to the word line of sufficient amplitude to magnetize the whole core in a given direction, *e.g.*,

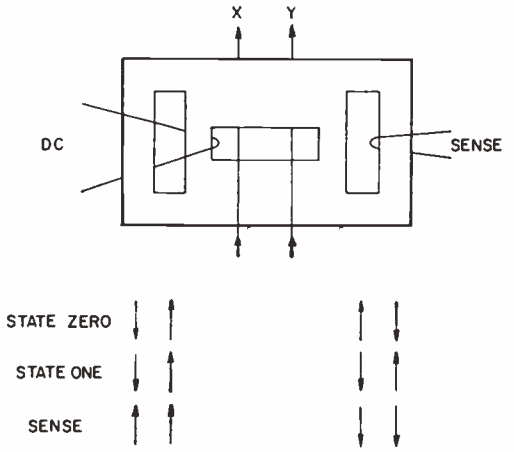


Fig. 13—Multipath memory core.

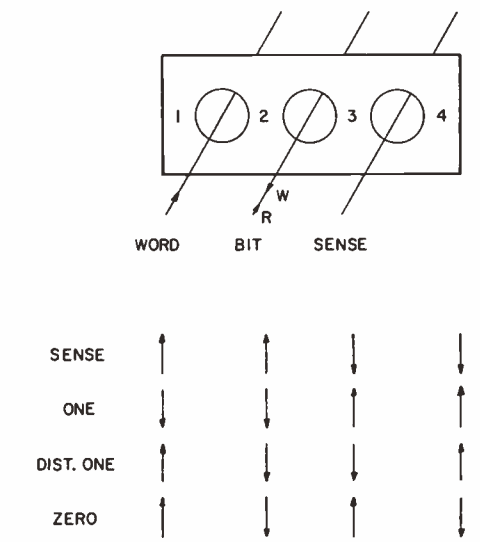


Fig. 14—Inhibit flux drive of three-hole memory cell.

clockwise. This produces a read-out signal if leg 4 had previously been magnetized upwards and stored a "one." To write, the word current is reversed and, simultaneously, bit write currents are applied to windings in leg 1 on the bit location where it is desired to write "zero." These bit currents inhibit switching of leg 1 and therefore cause flux to switch only around the central aperture in legs 2 and 3, leaving leg 4 in the "zero" state established by the read pulse. The bit current on unselected cores causes switching between legs 1 and 2 without disturbing leg 4. In experiments with single cores having 0.015-inch holes, switching times of about 1 μsec were reported.

A thousand-word memory made with three-hole cores was described [38] in which the inhibit flux mode was obtained slightly differently. The word winding threads both the central aperture and the aperture between legs 1 and 2. The bit location in which the bit currents are applied corresponds to writing a "one" instead of a "zero" as in the previous arrangement and this results in a polarity of bit current which disturbs "zero's" rather than "one's" on unselected word locations.

D. Nondestructive Read-Out Memories

The transfluxor's main property is the possibility of ascertaining the state to which it was set without altering that state. This nondestructive read-out property can be used for memories in which read-out need not be followed by a rewrite.

In a two-apertured transfluxor having three legs [39], [40], the amount of remanent flux in leg 1, which is equal to the negative algebraic sum of fluxes in legs 2 and 3, determines how much transfer of flux between legs 2 and 3 is possible (Fig. 15). There can be an indefinitely long back-and-forth exchange of flux between these two legs, the amount of which is determined by the flux initially set in. The transfluxor is blocked when legs 2 and 3 are saturated in the same direction as one or the other leg denies flux flow. The amount of setting determines the amount of flux that can be changed in one of the legs 2 or 3 before it is saturated. That same amount will necessarily appear in the other leg. The device can be used to store analog as well as digital information. Only its digital applications are of interest here.

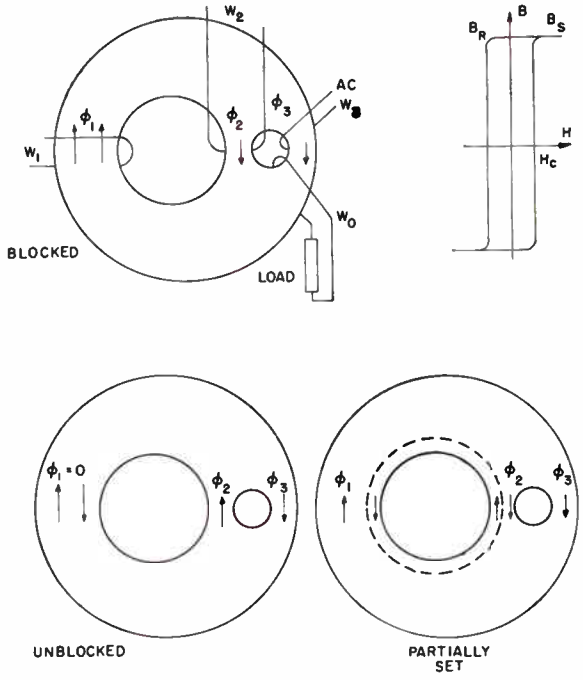


Fig. 15—Principle of transfluxor.

An array of two-hole transfluxors can be linked with one set of column and row windings through the large input apertures, and another set through the small output apertures [40] (Fig. 16). Current-coincident setting of the transfluxors is possible because a threshold of current is required to produce setting around the larger aperture, and similarly, coincident read-out can be obtained because a threshold of current is required to switch the flux around the smaller read-out aperture. A nondestructive current-coincident m-bit random-access memory can be made by providing digit write and digit sense windings through the large and small apertures, respectively (Fig. 16). In such a transfluxor memory, the read-out can be faster than with core memories with destructive read-out.

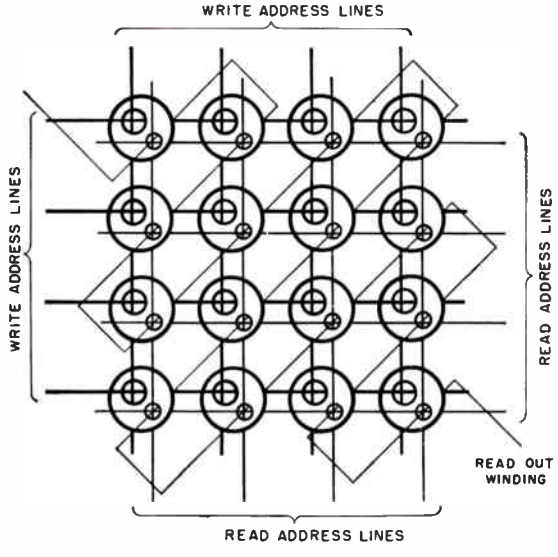


Fig. 16—Nondestructive read-out transfluxor memory.

Additional read-out holes can be provided in the transfluxor so that it is possible to read out information simultaneously to several destinations. This is the principle of a multiload transfluxor memory [41]. It is also possible to combine the nondestructive properties of the transfluxor with the various methods of fast setting described above [28], [29].

The nondestructive read-out of the transfluxor depends on switching back and forth the nonelastic flux set successively in legs 2 and 3. Such action is possible also with cores having two holes at right angles to each other [40], [42]. Alternatively, nondestructive read-out can be obtained in a number of ways by switching elastic reversible flux in simple ring cores or in multiaperture cores. An early proposal is based on the difference of polarity of the curvature of the hysteresis loop at the two remanent states which can be determined by the phase of the beat resulting from applying two small amplitude ac voltages of different frequencies to the X and Y windings [43]. Recent work with impulse switching mentioned above consists of observing the amplitude of reversible flux resulting from the application of large-amplitude pulses so short as to produce no irreversible changes [26], [30], [35]. It is also possible to ascertain the sense of remanent flux by the polarity of its change as it is momentarily diminished through the application of an orthogonal field. This can be achieved in a bobbin coil by sending a current through its ribbon [43]. In ferrite ring cores, the orthogonal field can be obtained by a solenoid wrapped around the core [44] or, as in a recent proposal [45], by a solenoid wrapped diametrically around the core. In ferrite cores having nonintersecting orthogonal holes of various forms, nondestructive mechanisms have been proposed on the basis of the rotation of the magnetization in the legs of the core common to

the main remanent flux path and an orthogonal interrogating reversible path [42], [43]. It is also possible to use an interrogating hole parallel to the writing hole, or hole cluster, and applying an interrogating small-amplitude current to one of its legs and obtain thereby more or less flux change depending on the direction of remanence of the leg [46].

In general, nondestructive read-out memories are particularly useful when frequent and rapid read-out is necessary and relatively slow write-in can be tolerated. This is the case in a number of applications ranging from data processors in which the ratio of read-outs to write-ins may be typically 4 or 5 to application where there is essentially read-only. This is the case, for example, for an airborne memory to be set on the ground and frequently read out in flight. Nondestructive read-out can give also added insurance that information in the memory is not lost due to a malfunction in the read-rewrite circuitry of destructive memory, but proper engineering is required to take advantage of this possibility. In general, the nondestructive memory is more complicated, as separate addressing circuits for write-in and read-out are necessary; for this reason the simpler destructive read-out memories are used more commonly. Common addressing circuits are possible in certain forms of word-organized memories driven by fast impulses, which are thus particularly advantageous for nondestructive read-out [26], [30], [35].

E. Ferrite Apertured Plate Memories

Arrays of individual ferrite cores have become a classical solution to selective access high-speed memories. The techniques of making and wiring individual cores can be improved upon by using an integrated method by which a large number of elements are made and wired in one step, as in the case of ferrite aperture plates.

A plate with a regular [21], [47], [48] array of holes is molded from square-hysteresis-loop ferrite material. The direction of remanent magnetization around each aperture stores one bit of information. There is no interference between magnetizations around adjacent apertures because for a given current through an aperture, the magnetizing force diminishes gradually with radial distance and, at a well-defined distance chosen to be less than half the width of the leg between adjacent apertures, becomes smaller than the threshold of switchover. The plate thus constitutes a unit conveniently fabricated as a whole in a single step and is equivalent to a number of cores. Furthermore, the ferrite being an insulator, it is possible to "print" windings directly on the plate and thereby eliminate the need for some of the manual threading. This is particularly suitable for making a winding which links all the holes in series.

Plates with an array of $16 \times 16 = 256$ holes have been developed and are finding increasing use [21] (Fig. 17). The holes are 0.025 inch in diameter and are spaced 0.050 inch center-to-center. The plate is less than an inch square. Squareness of the hysteresis loop and switching characteristics are comparable to those of individual cores made of the same material. Very uniform properties from hole to hole and plate to plate have been obtained. About 300 milliampere-turns are required to switch over the magnetization around an aperture in 1.5 μsec.

The plates, stacked with all the holes in register, are threaded in a single operation which does not need to be repeated separately for each plane as is necessary for memory core planes. Plate memories can be used in current coincidence or external word selection.

For current-coincidence operation, the holes of the stack of plates are threaded back and forth by row X and column Y windings. With this wiring pattern the direction of coupling of the selecting lines is the same as that of the printed winding and, therefore, during read-out the disturb voltages would add up rather than tend to cancel each other. This difficulty can be overcome by various wiring arrangements. For example, four plates can be used in a module [49], [53]. The plates are arranged in a square and are connected in series diagonally in pairs. The two diagonal pairs are connected in series opposition and the midpoint is grounded. A stack of quartets of plates is wired as a whole by X and Y selecting windings. In the reading step, the polarity of the difference voltage between the two nongrounded terminals of the diagonally connected plates is sensed by a difference amplifier and is indicative of the identity of the stored bit. The disturb signals tend to cancel each other. For writing or rewriting, the inhibit signal is sent into both branches of the common winding, in one polarity in one and the other polarity in the other. Extremely good discrimination is obtained with this arrangement. This is due in part to the high uniformity of the plates and in part to the lack of any appreciable air coupling. Planes of that type including as many as 16 plates yield satisfactory discrimination ratios. It is also possible to print patterns of windings

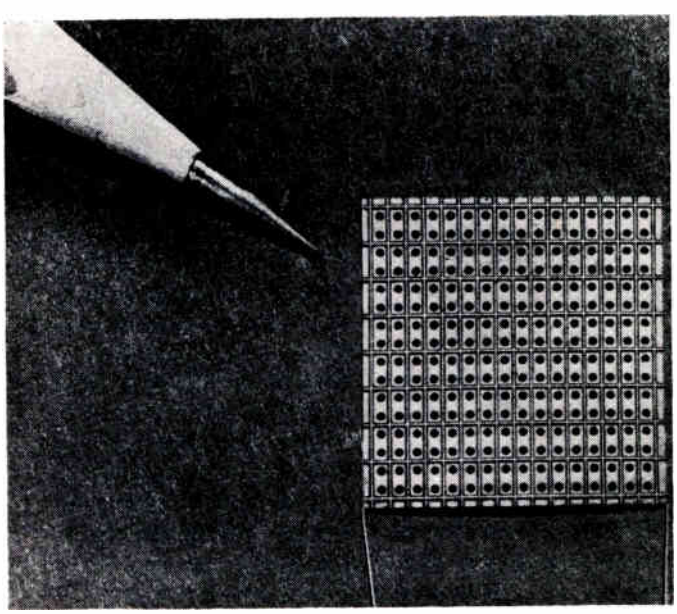


Fig. 17—Ferrite apertured plate.

with three or four terminals to obtain similar operation. This is done in a recent development of a 4×32 rectangular plate [50].

The apertured plates are particularly suitable for external word addressing [21] as the switch can be made of plates identical to those used for the memory. The memory stack and the switch stack can be wired as a whole with a bundle of wires going through all the holes. The switch stack is wired in addition with X and Y selecting windings. The switch can be operated in a number of ways such as set-a-line system [21], [51], and the dc bias system. The latter seems to be the most advantageous. Bias current can be conveniently supplied through the printed winding. The memories with a dc bias switch and a pair of plates for each digit were made according to the system explained previously in connection with core memories [52]. In this case, the operation is not strictly flux limited, since the amount of flux available from a plate hole increases monotonically with the drive. It turns out, however, that very fast operation and larger tolerances in current are possible with the plates than with cores [52].

Apertured plates are fundamentally more economical to fabricate and test than are the corresponding number of individual cores. Also, their assembly and wiring into memories is considerably simpler. Furthermore, a smaller driving energy is necessary, as it is possible to use a much smaller amount of material to store one bit than is necessary with individual cores which become unmanageable when very small.

A 4096 word with a 16-bits-per-word memory operating in current-coincidence with a cycle time of about 4 μsec was reported recently [48]. This memory utilizes 16×16 ferrite "sheets" similar to the "plates" described above.

F. The Twistor

A way to utilize a magnetic wire for the elements of a random-access memory was reported in 1957 [54]. Consider a magnetic wire or ribbon wrapped around an insulated nonmagnetic wire (*e.g.*, enameled copper) in the form of a helix making an angle of 45° with respect to the axis. Let there be in addition a solenoid around the wire (Fig. 18). This constitutes the "barber-pole-type" form of twistor. The combined effect of a current I_s through the solenoid and of a current I_w through the wire produces a magnetizing force parallel to the helical wire. The lines of flux will follow the easy path along the helical wire and return from the ends of the wire through the space surrounding the element. The hysteresis loop is very rectangular due to the anisotropy of the wire created by its longitudinal tension. The air return path has no serious shearing effect on the loop as long as the ratio of length-to-diameter of the element (enhanced by the helical path) is sufficiently large to insure that the demagnetizing field is smaller than the coercive force.

Originally, a form of twistor which consisted simply of a twisted magnetic wire was reported. The twist causes lines of strain at 45° with respect to the axis. The resulting anisotropy produces an easy direction of magnetization and permits twistor action by the combination of a current through the magnetic wire itself and through a solenoid wrapped around it. As the operation is dependent on the amount of twist, this seemingly simpler type of twistor is not as convenient to use in large memories as the barber-pole type.

The twistor can be operated in a bit or in a word-organized mode. A word-organized memory system driven by a ferrite core dc-biased switch has been described [55]. The barber-pole twistor wires correspond to the digits of the word. The words are selected by one-turn solenoid coils which link the twistors by lines and which produce axial magnetic fields (Fig. 19). Read-out is obtained by sending, through the selected word line, a current I_s intense enough to switchover the twistors which it links. The twistors which were previously magnetized in the opposite direction, switch-over and produce a read-out signal on the corresponding twistor central wires. These signals are relatively intense because the magnetic wire wraps around many times the "single-turn" central wire. This gain in voltage is a unique property of the twistor. The twistors which were previously magnetized in the direction of the read-out drive undergo small reversible flux charges.

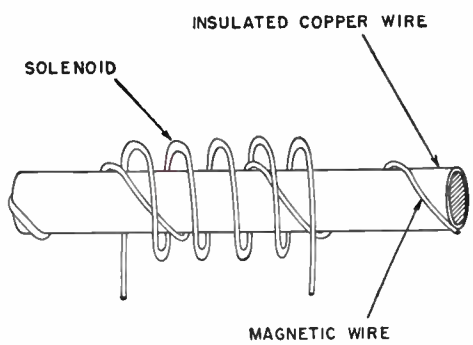


Fig. 18—Twistor.

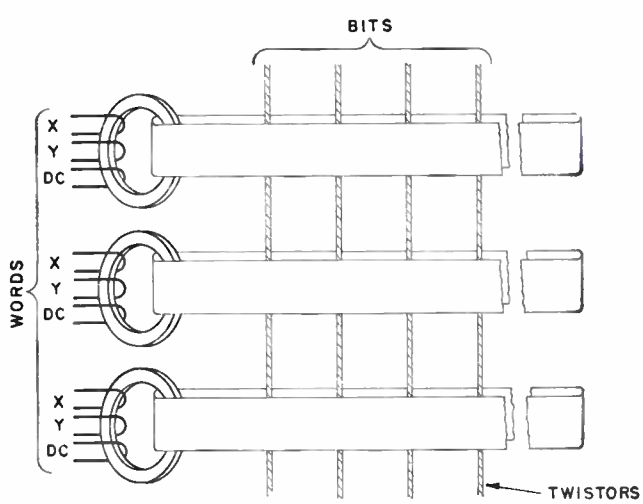


Fig. 19—Twistor memory.

The write-in is obtained by a current-coincidence mode, as the effects of the currents I_s in the word solenoids and of the current I_w in the central wires add algebraically.

The barber-pole twistors are made by wrapping on 0.003-inch insulated copper wire a 0.001-inch permalloy wire flattened to 0.0003 inch. These wires are embedded in parallel lines spaced ten to the inch between two sheets of polystrip plastic. Similar polystrips with embedded ribbons of copper wire are placed on either side of the twistor sheets to provide the words selecting coils.

Some developments of twistor memories include a random-access memory of 500 words of 100 bits each with a cycle time of 6.4 μsec [56]. Also reprinted is a twistor buffer store [57]. A new form of twistor, the counter-wrapped twistor, was reported recently [58].

G. Fixed Memories for Read-Only

The twistor memory has been adapted for the storage of semipermanent information [59]. This is a type of fixed memory with random-access "read-only" capability. The information is stored by the pattern of small permanent magnets superimposed on the array of twistor elements. The field of the permanent bar magnet is along the direction of the twistor central wire, and opposite to the field created by the word solenoid. It is sufficiently intense to prevent switchover of the twistor element over which it happens to lie. The selected word solenoid is energized positively and then negatively and this causes a back and forth switching of the twistors not paralyzed by the magnets. The resulting induced voltages are sensed on the central wires. The pattern of magnets is made by etching sheets of Vicalloy bonded to plastic cards. The cards are inserted between layers of twistor arrays in arrangements which provide for proper registry. A 512-word, 26-bit-per-word store operating in a cycle time of 5 μsec has been reported [59]. This card changeable nondestructive read-out twistor store is fully transistorized and uses 50 watts of power.

The twistor permanent memory is really a large code converter with a semi permanent pattern of conversion. Other forms of such fixed memories are related to core memories or to the switching concepts used in the electrically accessible memories and are thus a natural parenthetical subject in this paper.

Fixed memories can be obtained simply by omitting cores at selected locations of conventional arrays and permanently writing a one in all locations having cores. The vacancies can be created in the original wiring or by breaking selected cores of an initially full array. Shorting selected cores to paralyze their operation is also possible. It has been proposed [60] also to thread each word line through selected cores of a single row of cores.

Switching arrays comprising N inputs and M outputs such that the excitation of one input causes a given pattern of excitation among the M outputs, (as in the word organized twistor memory) was accomplished [61] years ago by a pattern of resistances coupling selected intersections between two groups of M and N parallel intersecting conductors. In a recent development [62], ferrite slugs are positioned at selected intersections of N parallel elongated coils with M such coils placed at right angles. Reported also is a development depending on capacity couplings at the selected positions [63]. In these switches, the resistive, capacitive or inductive couplings are linear and operate only if the M necessary sensing output devices have nonlinearity, preferably a sharp threshold of response.

Permanent memories are useful in computers to store subroutines for microprogramming and for storing arithmetic or other tables. It is often possible to use access circuitry in common with the inner high-speed memory proper. Interest in permanent memories is increasing, as they can substitute in certain cases for parts of the regular memories and provide faster access and larger capacity at lower cost. Permanent memories have a number of other applications in data processing and data transmission as well as in telephone switching.

H. Thin Film Memories

About five years ago it was suggested [64] that memory elements made of thin Permalloy films could have high switching speeds inherent to a rotational mechanism of flux reversal and could be fabricated conveniently by evaporation techniques. Since then, the physics of the film behavior and various memory systems and fabrication techniques have been studied extensively [67], and initial successes with experimental memories have been reported. The subject has been surveyed recently with some detail [65].

The magnetic alloy of zero magnetostriction consisting of 81.5 per cent nickel and 18.5 per cent iron is deposited on a smooth substrate through evaporation in vacuum or through electroplating. Uniaxial anistropy is established in the films by an orienting field during the formation of the element or in a subsequent anneal. Anisotropy can also be established through evaporation at an oblique angle [68]. The material acquires an easy direction of magnetization along which the hysteresis loop is square and a hard direction at right angles to the easy direction along which there is a straight characteristic and practically no hysteresis. The film is characterized by a coercive force H_c along the easy or longitudinal direction and an anisotropy field H_k along the hard or transverse direction [Fig. 20(a)]. At remanence, the film is magnetized longitudinally in one direction or the other. Magnetization reversal can occur either by domain wall motion or by rotation, or by both depending on the nature and geometry of the film and the nature of the drive. The switching threshold and the switching time depend on both the value of the longitudinal field H_L and the transverse field H_T. Typical dependence is illustrated in Fig. 20(b). In general, the switching coefficient S_w has different values for different strengths of H_L and H_T, generally a relatively high value of the order of one oersted-microsecond

for low drive when switching is mostly by wall motion and values lower by an order or even two orders of magnitude for high drives when switching is mostly by rotation [65], [67], [69], [70].

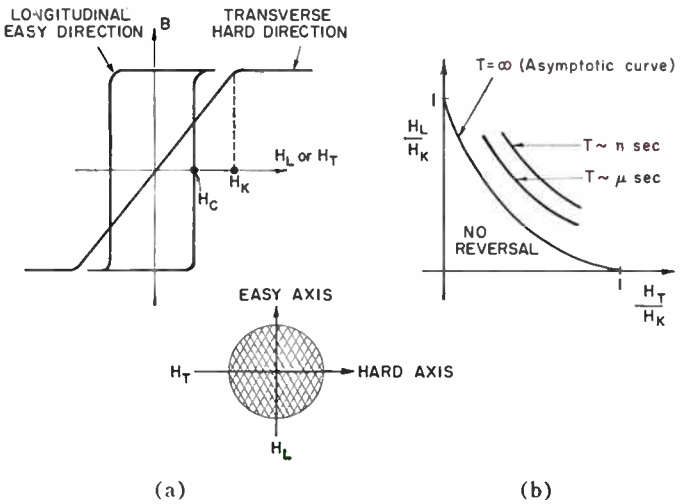


Fig. 20—Magnetic thin film characteristics. (a) Longitudinal and transverse hysteresis loops. (b) Time of reversal relation to longitudinal H_L and transverse H_T fields.

Memories can be made by evaporating a regular array of circular spots on a glass substrate. The circular shape is chosen to eliminate anistropy effects during rotation of the magnetization. In order to keep down the demagnetization effect of the free poles at the edges of the film, the ratio of radius-to-thickness is made very large, typically about 2×10^4.

An early experimental memory [71] had 4-mm-diameter dots 2000 Å thick. The conductors were flat strips placed in close proximity to the glass. At the element position, the row, the column, the inhibit, and the sense conductors were made to run parallel to each other and made a small angle with respect to the hard direction of magnetization of the elements. The application of the drive currents in conventional current-coincident operation produced a main component of field in the longitudinal direction and a smaller transverse component which enhanced switching. Difficulties were encountered with uniformity of spots.

In a more recent memory [72], combinatorial advantage is taken of the possibility of controlling separately the longitudinal and the transverse field components. The memory is word-organized with the attendant greater tolerances on film characteristics, particularly with respect to uniformity. The word line provides the transverse field and the bit line the longitudional write field. The application of the selected word line current rotates the element to the hard direction. This induces a voltage on the sense winding of a polarity corresponding to the previously stored remanent state in the easy direction. There is a dc current through all bit lines, and an opposing greater current is applied to all lines on which it is desired to write a one. At the termination of the word current the magnetization, momentarily in a naturally unstable state of hard magnetization between two stable states, rotates to the easy direction corresponding to the longitudinal field in the direction of the dc bias or the write current. The sense winding is made of two balanced halves to reduce coupling to the write winding. The simple straight windings required were made by winding a few turns around the glass substrate. A 32-word, 10-bit-per-word memory using 1.5-mm spots 600 Å thick was operated so as to demonstrate the feasibility of a cycle time of 0.5 or even possibly of 0.2 μsec (Fig. 21).

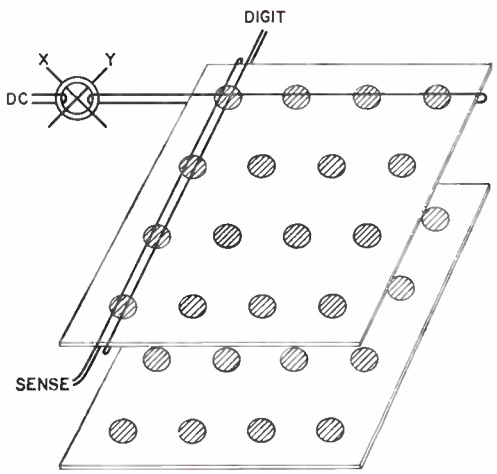


Fig. 21—Thin film dot array memory.

A very recently described memory [73] utilizes a continuous film evaporated on an aluminum substrate instead of a dot array on glass. The film, made of an alloy called gyralloy, is about 1000 Å thick. The memory is word-organized and uses also transverse field word and longitudinal field bit drives. However, the biasing to favor the zero direction is obtained by inclining the two windings slightly with respect to the anistropy axis of the films, instead of dc currents in the bit lines. The conductors are flat strips obtained by evaporating copper directly on the suitably insulated film or by laying thin films of plastic carrying the strips. Because the conductors are in close proximity to the film, the induced magnetic fields are very localized and the film switches right under the conductors and only a small distance away. The reversal stops abruptly at a point where the field is insufficient for switching. In a sense, the storing elements are created by the magnetic field instead of having to be fabricated. This simplifies the construction and eliminates exacting requirements of dot-to-winding alignments. A more fundamental advantage is the greater ease of obtaining uniform elements through the elimination of spot edges whose erratic nature was found to be an important cause of variability of switching properties. Also, there are several advantages to the use of a metal substrate. The sense line whose return is through the grounded substrate is very close to it, being separated only by the magnetic film and a thin insulation, so that it offers very little effective area for coupling to the write winding.

The magnetic field at the film due to the drive is increased by the eddy currents in the plate. The inductance of the drive winding is kept at a minimum. A prototype memory with 50 words of 50 bits each was built. It has lines spaced about 3 mm apart on aluminum plates of 3×7 inches. Word currents of 1.2 amperes and digit currents of 0.5 ampere yield signals of 3 mv for word pulses rising in 40 nsec (Fig. 22).

Another proposed form [74] of thin film memory having continuous elements in one direction, consists of using electro-deposited nickel-iron films on a copper wire in which a circumferential easy direction is obtained by the presence of a current through the wire during plating. The plating is a continuous operation obtained by pulling a wire through the electrolyte. As with twistors, the plated wire can be used in a word-organized memory in an arrangement of as many parallel lengths of wire as there are bits and surrounding the bundle by a number of solenoids, one for each word. The axial field due to the word solenoid can produce nondestructive read-out by rotations of the magnetization of less than 90°. The sense voltages appear on the wire. Because there are no demagnetizing effects in the closed flux path in the easy direction, films as thick as 12,000 Å can be used, yielding correspondingly stronger signals. Typically, 50 mv from a 1.5-mm length of 0.005-inch wire are obtained in 0.15 μsec. Write-in is by coincidence of currents through the solenoids and through the wires.

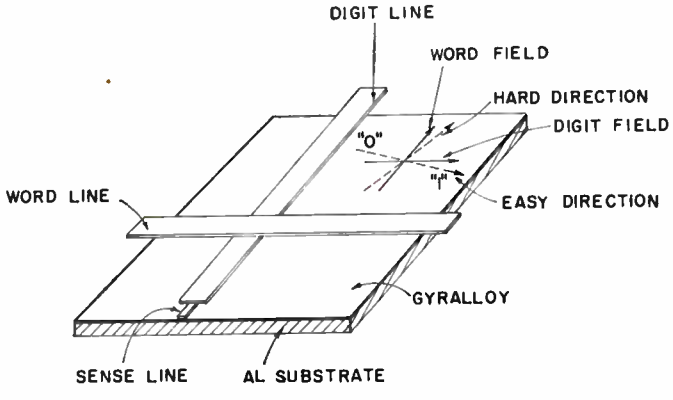


Fig. 22—Continuous sheet thin film magnetic memory.

A form of memory similar in geometrical concept and mode of operation to the wire memory consists of using a set of parallel cylindrical glass rods on which thin films have been evaporated [75], [76]. An experimental model of another cylindrical film memory was reported [77]. The model with 256 bits has yielded a cycle time of less than 1 μsec.

I. State-of-the-Art of Magnetic Random-Access Memories

The present state-of-the-art in computer magnetic random-access memories can be summarized as follows.

The most widely-used type are memories made of ferrite cores (50–80 or 30–50) which are transistor driven. Storage capacities vary between 10^4 and 10^6 bits and cycle access time is of the order of 10 μsec. Some of the later memories have access time of about 2 μsec.

Ferrite plate and twistor memories are in use also with capacities of about 10^5 bits and cycle times of the order of 3 to 5 μsec.

Typical memories are listed in Table II.

J. Considerations on Speed and Capacity of Magnetic Memories

1. Speed: A few general considerations apply to the present reported efforts to speed up memories with thin films or ferrites. These are: the inherent switching speed of the element for driving current attainable with the best semiconductor drivers, its ability not to overheat at high repetition rates, the transmission time along driving and sensing lines which is mostly determined by the physical size of the element, the amplitude of the read-out signal, the importance of masking signals inherent in the operation, and the ease of obtaining sufficiently uniform elements.

Thin film elements cannot be arbitrarily small because of the demagnetizing effects resulting from the open magnetic path. Smallest practical spacing with dot arrays and continuous film appears to be about 10 to the inch. With this size and the best materials, currents of a few hundred milliamperes available from the latest transistors can switch the film in tens of nanoseconds. Transmission delay per bit is about 0.02 nsec assuming a propagation speed of 10 cm/nsec or a third

TABLE II
TYPICAL MEMORY SYSTEMS

Type	Words	Bits/Word	Cycle Time μsec	Remarks	Year
Tx-2 *S* Memory	65,536	37	6.5	Core current-coincident	1957
Tx-2 *X* Memory	64	19	4.10	Word-organized two-cores-per-bit	1957
Transac S-100	4096	38	20.0	Core current-coincident	1957
IBM 704—738 Memory	32,768	36	12.0	Core current-coincident load-sharing	1957
RCA 501	16,384	28	15.0	Core current-coincident	1958
Lark	10,000	60	4.0	Core current-coincident	1958
Bull Gamma 60	32,768	6	10	Core current-coincident	1959
Siemens 2002	1000 to 10,000	49	14	Core current-coincident	1959
BTL Twistor Memory	500	100	6.4	Twistor memory elements. Word-organized	1959
Stretch 7302	16,384	74	2.18	Core current-coincident oil-cooled load-sharing switch	1960
Telemeter LQ	512–8192	4–100	1.5	Core word-organized	1960
BTL Sheet Memory	4096	16	4.0	Ferrite sheets or plates. Current-coincident	1960

of the speed of light. The signal output is of the order of 1 mv. To be amplified to usable levels, amplifiers with delays of the order of 10 nsec are required. Masking signals in the sensing circuit induced from the addressing and digit write windings are very large due to the required high currents. Using neutralizing winding geometries and closely-spaced grounding planes, it has been possible to reduce the peak of masking signal to be two orders of magnitude greater than the read-out signal, a reduction still short of ideal. Thin films present no overheating problems. Great difficulties have been encountered in obtaining uniform films. Intensive studies of basic reasons for observed variations are likely to overcome this difficulty.

Ferrite memory elements can be switched by currents whose amplitude is not restricted by the operational mode. This is possible either through the use of short pulses or by using a multiaperture geometry. Also favorable to fast switching is the decrease of the switching constant with the intensity of the drive. Cores can be made arbitrarily small with no fundamental limit due to demagnetizing fields since the flux paths are closed. Diminution of size reduces the current requirements, the transmission time per bit, and the effects of heating at high repetition rates. Miniaturization is a question of technique. With present molding practice, multiaperture cores have been made with 0.015-inch holes which switch in tens of nanoseconds with currents of hundreds of milliamperes, available from the best of present transistors. Element spacings of 20 per inch seem feasible leading to a transmission delay of 0.01 nsec/bit. Signal output voltages are in the order of one volt with present core size, leading to a simple amplifier with a short delay. While the masking effects of the pick-up in the sensing loop are relatively less important it is still difficult to cope with the large pick-up due to digit writing. Uniformity problems have been largely overcome by the extensive strides of the ferrite technology.

At present, small capacity film and ferrite memories have been operated with a fractional microsecond access time. It is likely that memories of a capacity of a few hundred short words can, and probably will, be made in the near future with both techniques to achieve a 100-nsec write-read cycle and corresponding 10-Mc repetition rates. Capacities of thousands of words with cycle time of about 1 μsec have been already achieved with ferrites and are very likely to be obtained with films. The question of obtaining the larger capacities at the higher speed awaits further engineering with either technique.

2) Storage Capacity: The question of obtaining large storage capacities, at any electronic speed, is mostly one of economy in the fabrication. Present cost per bit is an appreciable fraction of a dollar. Capacities of billions of bits are thus economically unthinkable even if technically realizable. The magnitude of the problem can be illustrated by the consideration that a third of a century would be required for an automatic cell fabricating machine yielding a bit per second to produce a billion elements. Obviously integrated means to fabricate many elements in a single step are indispensable. The apertured ferrite plate and the twistor are examples of such integrated techniques with which a modest progress has been achieved.

Major innovations in the concepts of construction are still required to obtain electronically addressable random-access memories with billion-bit capacities. Because such memories would have crucial practical importance in a number of applications, one can optimistically assume that such concepts will be found. In the meantime, electromechanical random-access memories with capacities of millions of bits and access times of about a second will be utilized.

IV. Ferroelectric Memories

In ferroelectric materials internal polarization effects produce a hysteretic relation between the electric induction D and an applied electric field E. The D-E loops are similar to the B-H loops of ferromagnetic materials. Some materials, such as barium titanate, exhibit square hysteresis loops (Fig. 23).

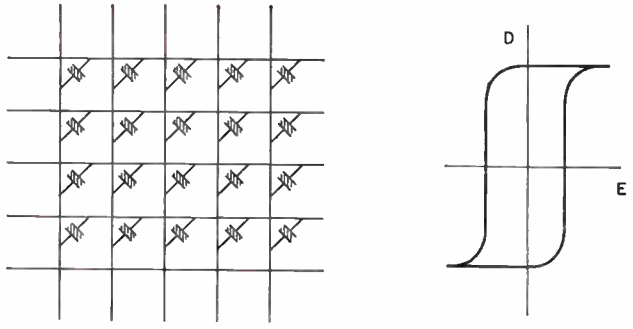


Fig. 23—Ferroelectric memory array and hysteresis loop.

When a varying electric field is applied to a ferroelectric condenser, the integrated current that flows through it can be thought as being a trapped charge Q. Thus, a hysteresis relation exists between the measurable quantities Q and applied voltage V. With square loop materials, practically no current flows when the condenser is driven from remanence further into saturation, but a large current flows momentarily when the condenser is reversed from one remanent state to the other. The time of reversal is inversely proportional to the excess of the applied electric field with respect to a constant field (the coercive field). A relation similar to relation (1) can be written.

Proposed memory systems [78]–[79] utilize an X-Y array of ferroelectric condensers in which each condenser is connected between a row conductor X and a column conductor Y (Fig. 23). The application of voltages to one column and one row conductor produces a voltage difference on the element at the intersection which is greater than that which appears on the other elements of the selected lines. Consequently, if the hysteresis loop is reasonably rectangular, voltage coincident systems similar to the current coincident systems of magnetic memories can be used. Because no third electrode is available on the condenser, the

read-out cannot be obtained from an *ad hoc* circuit as is possible in magnetic memories. One must resort to measuring the current which flows in the selected lines at the instant of selection and sense, whether or not it has an increment due to the reversal of the selected element. Because of lack of perfect loop squareness, the total current flowing through the unselected elements on the selected line may be much larger than this increment. This makes it very difficult to operate the memory in voltage coincidence, as was found in various reported attempts [78]–[80]. In a word-organized memory, sensing could become a manageable problem.

Most work was done with barium titanate [78], [79]. Arrays of 16×16 elements were made on single crystals of less than a square centimeter area by painting two perpendicular sets of parallel strips on the two sides of the crystal [78]. Also arrays of single units were used [79]. Difficulties were encountered with element uniformity, with creeping of the remanence due to repeated partial depolarizing voltages, and with loosening of the electrodes caused by piezoelectric effects. With more recent materials such as Gash, Thiourea, and Triglycine Sulfate, these difficulties would not be as severe.

The ferroelectric approach has not come out of the experimental stage and it is questionable whether it ever will be able to compete with its magnetic counterpart. Apart from practical difficulties encountered thus far, there are inherent reasons for this. 1) The ferroelectric condenser is a two-terminal device which makes sensing difficult, as mentioned above, and precludes also any signal cancellation circuit arrangements. 2) There is no topological necessity to provide for the geometrically more complex linkage of windings through holes as in the closed flux-path magnetic approach. However, it turns out that this topological necessity of magnetics is not as severe as first believed. On the other hand, the problem of making electrodes with sufficiently intimate and stable contacts is more difficult than first suspected. This is because the slightest interface layer between the dielectric and the electrodes introduces a series impedance much greater than the impedance of the ferroelectric at the instant of switching. 3) In ferroelectric materials the stored energy per unit volume is much higher than it is in magnetic materials with which extreme miniaturization is already necessary to bring drive requirements down to a reasonable level. 4) At present, ferroelectric materials are not as fast as magnetic materials.

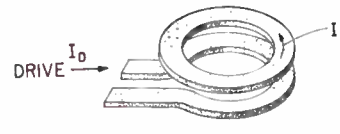
V. Cryoelectric Memories

A. Superconductive Memories

1) Principle: About five years ago, Buck reported [81] on his demonstrations of the utility of superconductive phenomena for computer elements. Since then, intensive work in this field has established superconductive, and more generally cryoelectric, techniques as main contenders for computer logic and memory realizations. Logic gating by cryotrons is based on the control exercised by a magnetic field in the transition of the superconductive to the normal state. Memory cells, realizable by cryotrons, are obtained more elegantly through the use of superconductive persistent currents or trapped flux. The operation of such cells is as follows.

Consider a closed loop of superconductive metal and in close proximity to it another driving loop (Fig. 24). Let us suppose that a superconductive current flows in the closed loop in a given direction as a result of a previous write-in. Let the current in the driving loop rise and the polarity be such that the induced EMF in the loop will tend to increase the supercurrent. The loop current I will increase until it reaches a critical value I_c, at which time the loop becomes normal and the current starts to decay as a result of the nonzero resistance. If the drive current is maintained, the loop current will decay to zero. This occurs due to Joule heating of the loop by its current I, which raises the temperature sufficiently to decrease the critical current I_c and keeps it lower than the current I so that the loop does not become superconductive until the current I has decayed to zero. Now, if the driving current is turned off, a supercurrent of opposite polarity will be induced which will not reach the critical value since there is no previously induced additive current. In this way the supercurrent of the loop is switched.

The operation is similar to that of an element possessing hysteresis. There are two distinct remanent states corresponding to the two directions of flow of the supercurrent. These states persist indefinitely without any external holding energy. To switch from one state to the other, the drive must exceed a certain threshold in the direction establishing the desired state and it must remain at the high value for a sufficiently long time. In the case of the superconductive cells, this time is necessary to dissipate the stored magnetic energy in the resistance of the loop and is determined solely by the thermal and L/R time constants of the element. It does not depend on the strength of the drive, as is the case with ferromagnetic and ferroelectric cells. The operational similarity of the superconductive cell to hys-



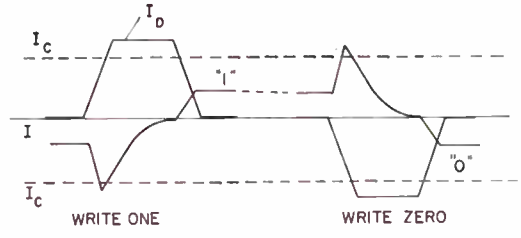


Fig. 24—Principle of superconductive persistent current storage cell.

teretic cells allows it to be used in similar memory systems.

To obtain a low L/R time constant, the resistance R of the material when it becomes normal should be as high as possible and the magnetic flux created by the supercurrent should be as small as possible. This can be achieved using thin film superconductive elements made by evaporating in high-vacuum suitable metals and separating insulating layers. Films about 2000 Å thick are found to have appreciable resistance in the short lengths of interest. The magnetic flux around a superconductor is kept small by confining it to occupy a very small volume, by means of sandwiching superconductive ground films which are perfect magnetic shields. The limit of this confinement is the ability of making adequate thin insulating films. Furthermore, with this flat construction of the cells, the ratio of heat dissipating surface to heat storing volume is high so that the thermal time constants can be very short. Indicative of the short L/R and thermal time constants obtainable by the thin film techniques are elements which have been switched in a few nanoseconds [82]. The film fabrication techniques provide also a convenient means to make whole arrays of elements in an integrated manner with all the necessary interconnections. For these reasons, all current research is with thin film devices in contrast to the earlier work with wire wound devices.

2) The Crowe Cell: A storage cell can be made [83] by using a film with a hole crossed by a narrow diametrical strip bar (Fig. 25). The persistent current flows in a figure-eight pattern with a heavy concentration in the strip which is the active part of the cell. The drive and sense lines are placed on either side of the cross bar and are separated from it by proper insulation. When the drive exceeds a threshold value the cell switches, *i.e.*, the direction of the persistent supercurrent in the cross bar reverses. At that instant the flux linkage around the cross bar and the sense winding reverses and a voltage is induced in the sense winding.

An extremely important property of the Crowe cell is the complete lack of spurious coupling between the drive lines and the sensing lines separated by perfect superconductive shields. The coupling appears only at the desired location when the selected cross bar becomes momentarily normal. Consequently, the ratio of wanted to unwanted signals is determined only by spurious pick-ups in the leads. This pick-up can be compensated for with high accuracy because there are no "delta" noise effects.

3) Continuous Sheet Superconductive Memory: The main difficulties experienced with Crowe cells are the variation of the currents required for their switching. The lack of uniformity may preclude their use in current-coincident systems. These variations are due chiefly to the strong dependence of critical field on the nature of the edges of the bridge [84].

There is a promising possibility [85] that these difficulties can be eliminated by using a continuous sheet of superconductor without any fabricated holes. Two perpendicular sets of parallel suitably insulated lead strips are evaporated on top of a continuous film of tin. When an X and a Y strip carry a current I, the magnetic field pattern at their intersection is at 45° with respect to the strips (Fig. 26). The intensity of the field is maximum at the intersection, and diminishes gradually with distance. Consequently, there is a region limited by a definite boundary within which the supercurrents induced by the change of the field exceed the critical value and outside of which it does not. In this way a superconductive elemental region is created without the necessity of any holes in the film. It is found that these regions are stable.

In all other respects the continuous sheet element operates as the original Crowe cell. The sense winding is located on the opposite side of the film with respect to the drive lines and picks up a voltage only at the instant and location at which a selected element is switched.

4) Other Types of Cells: Another type of cryoelectric memory element is the persistor [86] and the closely related persistatron [87]. In the persistor memory element, a superconducting inductor is in parallel with a switch element that is normally superconducting, but which becomes resistive when the current exceeds a critical value. When a suitable current pulse is applied to a persistor memory element, a persistent circulating current is stored. A second pulse in the same direction

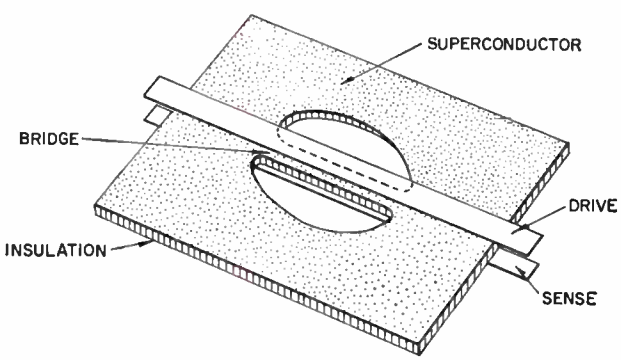


Fig. 25—Crowe cell.

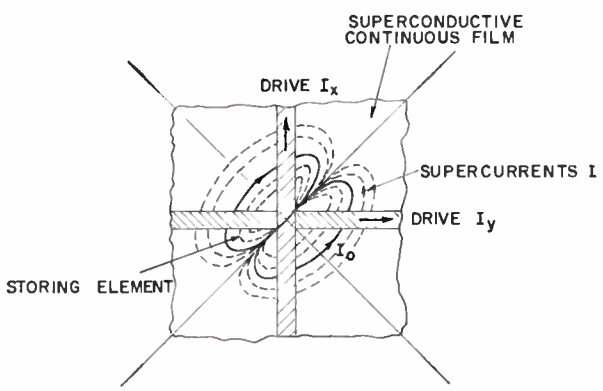


Fig. 26—Persistent current storage in discrete region of a continuous superconductive sheet.

as the first makes no change, but a pulse in the opposite direction reverses the circulating current and produces a voltage across the element. By mutual inductance coupling to two or more driving circuits, these memory elements can be made to operate in matrices. Memory elements of this type have been operated with 15-nsec pulses at a 15-Mc repetition rate. The great advantage of complete shielding of the sense line from the drive lines afforded by the memory planes in the Crowe type memories is not obtained in persistor memories, and thus arrays of only limited size can be made.

5) *Memory Systems:* The circuits for addressing and sensing superconductive memory arrays can consist of cryotrons. These devices can be fabricated by similar thin film techniques, making it possible to make the whole memory by an integral construction. This has the advantage that only a few leads—for the n address bits, the m information bits and for controls and power supplies—need to be brought into the cold chamber. Cryotron trees and cryotron sensing amplifiers can be used. The speed of the memory would depend mostly on the speed of the cryotrons. Although low gain can be tolerated in this application, it is unlikely that cycle times of less than 1 μsec could be obtained with any reasonable storage capacity.

It is possible also to use transistor or tunnel diode circuits at room temperature in conjunction with superconductive memory arrays. Higher speeds of operation, could be obtained in such a hybrid arrangement which does not seem to present insurmountable matching problems. Cycle times of tens of nanoseconds are conceivable.

6) *Outlook:* Superconductive techniques for memory have a number of inherent advantages: persistent current flow is a natural form of storage, there are sharp switching thresholds, there are perfect shields against undesired signals, switching times can be of the order of a few nanoseconds, and the stored energy per bit can be very low. Furthermore, elements small enough to allow packing of at least 100/cm seem possible yielding a transmission delay of only 10^{-12} sec/bit. There is also promise in vacuum evaporation for a good integrated technique of memory fabrication.

The necessity of maintaining the memory at the temperature of boiling liquid helium is an inconvenience at present. Special experimental techniques are required. Liquid helium, although reasonable in price, is not always readily available, and it is wasted. However, closed cycle refrigerators are being developed [88] with sufficient cooling capability for a reasonable computer, typically capable of maintaining an electric load dissipating as much as 3 watts and occupying a cubic foot at a temperature of 3.3°K. When these become an economic reality, cryoelectric elements may prove no less practical than conventional components requiring air conditioning or cooling systems.

Results of efforts to implement memory potentialities have been reported in three areas: 1) greater understanding of the superconductive phenomena, particularly with regard to the transition between superconductive and normal states; 2) experiments with single and a few memory cells, demonstrating that all required properties for memory systems can be obtained and that the switching times can be very short; and 3) suggestions on methods to make memory systems. No fundamental difficulties have been found. The problem seems to be chiefly one of technology.

It is reasonable to expect that superconductive memories with thousands of words and cycle times in the microsecond range will become a reality in the near future.

B. Cryosar Memory Applications

A high-speed semiconductor cryoelectric element, the cryosar [93], may be used for making random access or fixed memories or for driving superconductive memories. The cryosar is a two-terminal device made of doped germanium. There are two forms.

In one, the impurities such as indium are not compensated. The element exhibits a very high resistivity up to a certain critical field, after which the current increases by orders of magnitude. There are thus two distinct regions: one of high and one of low resistance. Such diodes can be used for making fixed memories or function tables [93]. It has also been proposed to use these monostable diodes for drivers of superconductor memories [94]. Such drivers could probably switch more current in less time than cryotrons. Devices of this kind have been proposed for making fast amplifiers [95].

In the second type of cryosar, the indium impurities in the germanium are compensated for by antimony impurities. The result is the existence of a negative resistance characteristic, which makes it possible to set the device into one of two stable states. Cryosars of this type can be used to make memory arrays [93].

Both types of cryosars can be switched from one state to the other in very short times. Times of less than 10 nsec have been reported. The high speed is an inherent property of the impact ionization mechanism responsible for the onset of high conductivity.

The cryosar structures are very small and the device lends itself to vacuum evaporation construction techniques. Integrated methods of making arrays of cryosars on a single germanium crystal have been reported [93].

Experiments with cryosars are very promising. Their importance in the memory art awaits further engineering.

VI. Tunnel Diode Memories

Cycle access times as short as 100 nsec appear to be attainable with advanced magnetic techniques, as mentioned earlier. However, a shortening by another order of magnitude to access times of 10 nsec becomes less certain. This has prompted attempts to utilize tunnel diodes for the purpose.

Although the tunnel diode advent is very recent, its characteristics are already universally known. The voltage current characteristic exhibits in the forward direction a rise to a maximum, a drop corresponding to negative resistance, a minimum, and a subsequent rise (Fig. 27). A tunnel diode in series with a resistance can be biased so as to have two stable potentials, one in the voltage range below the peak and the other above the valley. Switching from one state to the other has been observed in times shorter than 1 nsec and is obtainable in 2 or 3 nsec in readily available units.

A memory can be made using an array of bistable tunnel diodes [5], [6], [89], [90]. Row and column lines are resistively coupled to each diode and bistability is obtained by proper biasing of both lines (Fig. 28). Any selected diode can be set to one or the other state by coincident voltage of appropriate polarity and amplitude, on the corresponding row and column lines. The memory can be organized for coincident-bit addressing requiring two-to-one selection discrimination or for word addressing needing only three-to-one discrimination. The maxima and the minima of the characteristics provide the necessary thresholds and are sufficiently uniform to make possible either of these coincident write-in systems.

Read-out is obtained by driving the selected element or elements to the high state and observing whether or not switching occurs. In a second following writing period, the elements which have changed state are restored by appropriate control of the writing circuits in a manner analogous to that used in destructive read-out magnetic memories.

To obtain the read-out signal, several solutions are possible despite the difficulty presented by the use of two-terminal devices already mentioned in connection with ferroelectricity. The signal can be obtained by direct pick-up from a common circuit resistively or capacitively coupled to all elements corresponding to a bit of a word [89]. This attenuates the signal in proportion to the number of words and thereby brings about an unavoidable delay due to necessary high amplification. Several methods to couple through induction or radiation have been suggested also [90], [5].

Drivers of tunnel diode arrays must be able to supply pulses of relatively large power. The current is large because many elements are driven in parallel, and the voltage is high because the voltage of the series current regulating resistances must be several times greater than the voltage swing of the tunnel diode. Typically, hundreds of milliamperes and several volts must be provided. The best promise for a switch of this power-handling capacity operating in nanoseconds is the tunnel diode itself. Sufficient voltage can be obtained by connecting a number of tunnel diodes in series, and adequate current simply by using sufficiently high current units.

Physically small storing elements are possible. The active region of a tunnel diode is typically about a

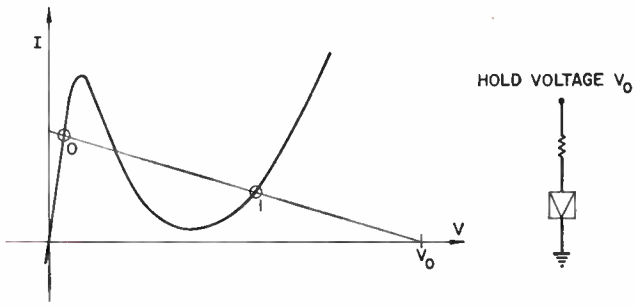


Fig. 27—Tunnel diode characteristic and storage element.

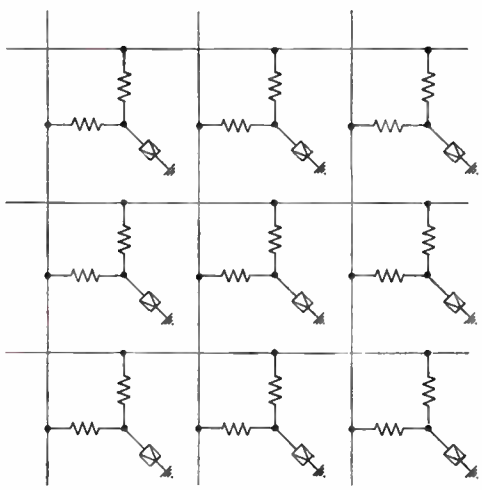


Fig. 28—Tunnel diode memory array.

square mil, so that very close spacing is possible with adequate integrated technology. Presently available individually packaged units have been reduced to a capsule 1.2 mm in diameter and 0.7 mm high. These units and their associated resistances can be packed at about 5/cm. The delay per bit is thus about 0.02 nsec/bit. A tolerable 5-nsec transmission delay permits the use of 250 elements per line. Center-tapping of the lines and other artifices permit one therefore to contemplate memories of about 1000 words.

It appears thus that tunnel diode memories may achieve cycle times of the order of 10 nsec: the diodes themselves are fast enough, there does not seem to be insurmountable sensing or driving problems, and the physical size of the storing elements is sufficiently small. Their use entails the requirements of dc holding power not necessary with hysteretic devices. Also the cell structure of a tunnel diode element is relatively more complicated than that of magnetic storing elements. Despite these disadvantages with respect to the more elegant hysteretic types, the tunnel diode offers at the present time the best and possibly the only solution to 10-nsec random-access memories.

VII. Conclusion

About 15 years ago, the central importance of a high-speed electronic memory for computers was recognized.

The first types depended on serial access. These were soon followed by the development of electrostatic storage tubes with which it was possible to obtain far more versatile random-access addressing. About eight years ago, random-access magnetic memories started to displace tubes and are now the dominant type in use. Ferrite core memories with capacities of hundreds of thousands to a million bits and access cycle times of 2 to 15 μsec are common.

Present efforts with impulse switching of single and multiple-apertured ferrite cores as well as the work with thin magnetic films are likely to lead to memories with an access time of 100 nsec. The advent of the tunnel diode two years ago opens the possibility of memories with access time an order of magnitude shorter.

Ferrite aperture plates, three years ago, and the twistor two years ago, were significant steps to provide the integrated fabrication methods necessary to obtain large storage capacities. Ferroelectric memory experiments for the same purpose did not show promise. On the other hand, superconductive elements which have a history of only five years offer great promise. These cryoelectric elements can be fabricated through vacuum evaporation by methods which may provide the required integrated technique.

Selective addressing by coded addresses known as random access is a great improvement with respect to serial time addressing. This is chiefly because of the freedom of organizing successive processing steps in any desired order, and in particular in an order depending on the progress of the processing itself. A still greater versatility of addressing would be obtained if it were possible to address the memory directly by its stored contents instead of indirectly by the labelling addresses. This would allow, for example, to answer the question as to whether or not a given word is stored in the memory without scanning through all the words. Also it would be possible to find a complete stored word upon giving a few of its digits. Such content addressable memories must have logic circuits associated with all storage elements. Some experiments with content addressable memories or "catalog" memories were reported four years ago [91] and utilized wire-wound cryotrons for storage and logic. More recent work is with evaporated cryotrons [92].

Progress of computer memories in the last 15 years has been tremendous and its rate steadily increasing. This trend is likely to continue because the memory is the central part of all data processors and any improvements in it have a determining influence on the performance of the whole system. We can look forward to faster, larger, cheaper, and more versatile memories.

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A Computer Subsystem Using Kilomegacycle Subharmonic Oscillators*

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Summary—An investigation was made of the problems associated with a high-speed carrier computer, and a computer subsystem was constructed employing subharmonic oscillators driven with a 3.7-kMc sine wave source. The three-phase power source was modulated at a 30-Mc rate so the interval between successive logic operations was 11 nsec. The logic module is a balanced resonant varactor circuit having a pulsed subharmonic output at 1.85 kMc and a rise time of 3 nsec.

The output from each module, at a level of about 1 mw, is distributed through a network of resistors and coacial lines to the modules of the succeeding power supply phase. The logic is done at 1.85 kMc by forming a majority of three from the three inputs. This majority logic, with the readily available inversion operation, provides a universal set of logic gates.

The subsystem consists of four main parts: the logic modules, the 1.85-kMc signal distribution, the 3.7-kMc power distribution, and the power supply.

The subharmonic oscillator has advantages characteristic of a carrier computer; among these is the ability to transform impedance levels, and the ability to get a logic inversion by adding a cable length to give 180° phase change of the signal. Advantages peculiar to the subharmonic oscillator system are the simplicity of the varactor and its inherently fast operation. This approach also has a high logic gain, and provides fully timed and amplitude limited pulses at the output of each module.

Three-phase operation gives an effective directivity to the single port gate. Disadvantages of this system are the elaborate power supply and the high engineering design cost.

The power supply consists of a klystron oscillator supplying a CW signal to the hybrid modulator. The nonlinear element in the modulator is a varactor, which is also driven by a 30-Mc trapezoidal wave having a 3-nsec rise time. The modulator output, of 150-mw peak, is amplified by a traveling-wave tube to yield the single-phase supply of 6 watts, which is converted to the three-phase supply.

The conversion is accomplished by a three-way power splitter having three transmission lines of lengths differing by 11 nsec. A ferrite isolator is inserted in each phase to minimize interaction. After the ferrite isolators. the power distribution circuitry employs a group of hybrids which serve to divide the power while maintaining impedance matches looking both ways at each junction.

The logic module is contained in a rectangular brass box having a volume of 0.16 cubic inch. Miniature coaxial lines connect the logic nodules to each other and to the power supply, giving a completely shielded subsystem.

The subsystem constructed contains a three-phase ring, two majority gates, and their majority logic drivers, comprising a total of seven subharmonic oscillators. Operation is stable, with reasonable allowable variations in the power supply frequency and amplitude.

INTRODUCTION

THE variable-capacity diode, when placed in a resonant circuit, has the property of generating energy at a frequency just half that of the sinusoidal driving frequency applied to the resonant circuit. This subharmonic frequency is phase locked to the driving frequency in one of two possible phases. Such a circuit is known as a "phase-locked oscillator" (PLO) or as a "subharmonic oscillator" (SHO).

Since the choice of phase for locking may be determined by a locking signal 40 decibels or more below the level of the subharmonic signal, the circuit may be used as a nonlinear, high gain amplifier, and so is sometimes called a parametric amplifier. The circuit acts as an ideal limiter in that the subharmonic output level is independent of the locking signal level. The circuit has memory in that the subharmonic oscillations persist after the phase-locking signal has stopped.

No well-separated input and output terminals exist in this circuit. Single-port devices can be given directivity by using a 3-phase clocking pulse, which is the method here used. Previously reported work on balanced PLO's has been carried out at low frequencies, approximately 5 Mc.[1] The present work is intended to show that the balanced circuit can be used in the kMc frequency range, thus eliminating the microwave filter necessary in unbalanced PLO's. Four kMc was chosen for the pump source because the varactors available were capable of oscillating when pumped at this frequency.

The varactors employed were the Hughes 1N896, having inductances of approximately 5 millimicrohenries and capacitances of 1.25 $\mu\mu$f at a bias of -1 volt. The capacity swing over the useful bias range can be expected to go from 2.0 to 0.75 $\mu\mu$f. These are typical values based on measurements made at this laboratory.

The rectangular box shown in the photograph of Fig. 2 emerged as a structure having a good combination of characteristics for the circuit. Some concepts involved in the design are as follows:

1) Consider the rectangular structure as the outside, or shield, of a shielded two-wire line.
2) The varactors and attending leads are the two conductors for the line.
3) One end of the loop formed by the two diodes is grounded to the box, thus forming a shorted section of transmission line. From transmission theory, the approximate inductance for the loop can be calculated.

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4) The varactor inductance (5 millimicrohenries) is included as part of the total inductance of the loop.
5) The varactor capacitance is in series with the loop.
6) The loop capacitance and inductance should be series resonant at the signal frequency.
7) The varactors were connected cathode-to-cathode and plate-to-plate around the loop to facilitate biasing.
8) The output loop permits simultaneous adjustment of coupling as well as balance.

Design Considerations

A top view of the PLO used in this work is shown in Fig. 1, and Fig. 2 is a photograph showing typical PLO construction. The varactors are mounted in box C with cathodes towards clip E.

The equivalent circuit for the PLO shown in Fig. 1, minus the input matching network, is given in Fig. 3. This input matching network will be discussed in a subsequent section.

The parameters in Fig. 3 are defined as follows:

C, r and L_d are the varactor parameters.
E is the subharmonic signal generated as a result of the applied pump power.
L_1 is the equivalent inductance added to the circuit by the geometry and dimensions of the box shown in Fig. 1.
L_2 is the inductance of the output loop.
M_1 and M_2 are the mutual coupling.

The inductance L_2 can be varied by changing the size and geometry of the loop. The amount of pump signal coupled to the output can be controlled by adjusting the relative magnitude between M_1 and M_2.

The cross-section dimensions of the PLO enclosure were chosen in such a way that the characteristic impedance of the line would be 91 ohms. The choice of 91 ohms was dictated by the desire to make the PLO enclosure of minimum dimensions compatible with the varactor dimensions. From the varactor parameter values, it is apparent that approximately 3 mμh of inductance outside the varactors is required. For a characteristic impedance of 91 ohms, the additional 3 mμh can be achieved by making the structure 0.5 inch long, with the inside cross-sectional dimensions being 0.45 inch $\times$ 0.45 inch.

The inductance of the varactor leads can be calculated if the varactors are considered as forming the conductors of a two-wire transmission line inside the rectangular box, shorted at one end. Such an inductance is

$$L = Z_0(1.016)(\sqrt{\epsilon} \times 10^{-3}) \cdots \mu\text{h/foot},$$

where $Z_0 = 91$ ohms.

By taking into consideration the lead inductances, the average values of varactor parameters and effects of

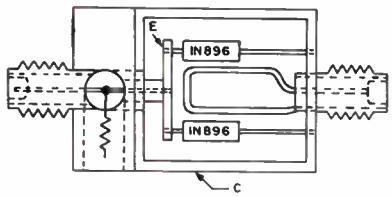


Fig. 1—PLO: top view.

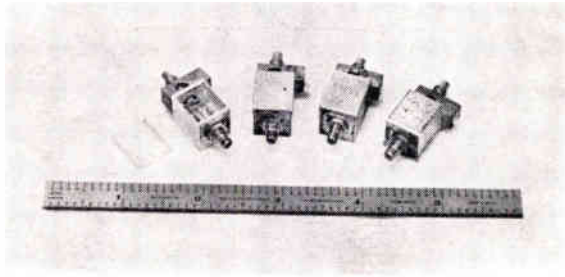


Fig. 2—Photograph of typical PLO's.

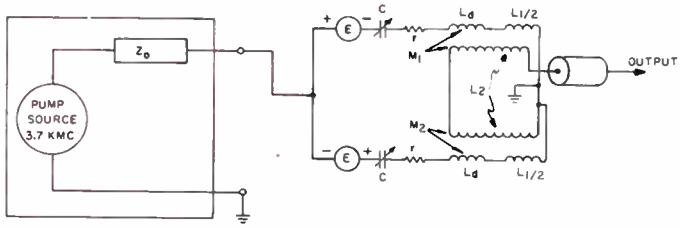


Fig. 3—PLO equivalent circuit without input matching network connected to power source.

output loading, the range within which the input impedance should fall, can be determined.

The output load cannot be directly related to the input because the PLO is a balanced circuit and as such the output is not reflected to the input as in common coupled circuits.

We will consider the PLO circuit at two frequencies, and neglect the variation of capacity with the variation of pump signal, and the fact that coupling factor (k) cannot be accurately measured.

Consider the PLO circuit shown in Fig. 4 as a coupled circuit at two frequencies: the power source frequency (f_p) or the signal frequency (f_s). In this case, the frequencies are 3.7 kMc and 1.85 kMc, respectively.

L_p = apparent inductance, consisting of varactor inductance plus added inductance due to PLO enclosure = 13 $\mu\mu$h.
k = coupling coefficient, estimated to be approximately 0.5.
R_L = output load, 50 ohms.
r = varactor spreading resistance = 4 ohms.
$C_{(v)} = 1.25$ $\mu\mu$f.

From circuit theory, neglecting the nonlinear varactor effect, Fig. 4 can be represented by the equivalent circuit in Fig. 5, where

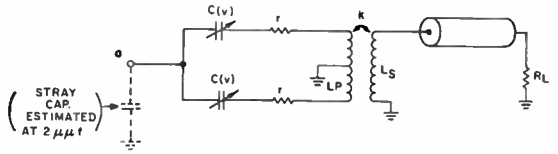


Fig. 4—PLO equivalent circuit showing input stray capacitance.

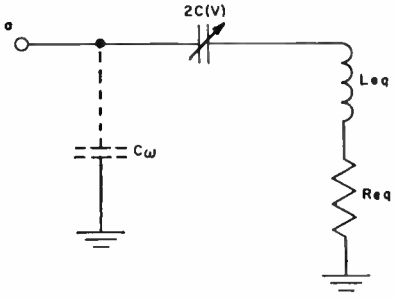


Fig. 5—PLO circuit reduced to series equivalent.

$$\begin{cases} L_{eq} = \dfrac{(1-k^2)}{2} L_p \\ R_{eq} = \dfrac{2rQ_s + k^2\omega_s L_p}{2Q_s} \end{cases}$$

and

$$\begin{cases} \omega_s = (2\pi)(f_p/2) \\ Q_s = \dfrac{\omega_s L_s}{R_L} . \end{cases}$$

The value of L_s can be calculated from the dimensions of the PLO pick-up loop.

Calculations based on typical values for the equivalent circuit on Fig. 5 indicate that the reactive part of the PLO input impedance should be substantially capacitive; laboratory measurements confirmed this.

With such an impedance the PLO will present a mismatch to the pump source regardless of the value of R_{eq}. The calculated PLO input impedance, using the equivalent value derived from Fig. 5, shows the VSWR to be between 9 and 10. The measured VSWR for seven PLO's tested was found to range between 8 and 12.

There are at least two undesirable effects which can result from such high mismatches. They are:

1) PLO input phase angle will vary rapidly with small changes in varactor parameters or input stray capacity.
2) A high VSWR combined with an imperfect PLO balance will permit creation of spurious frequencies.

In order to reduce these undesirable effects, it was decided to introduce a matching network (Fig. 6) at the PLO input. The values of L and R were determined empirically by monitoring the VSWR at the input terminals as L and R were varied. Capacitors C_1 and C_2 are dc blocking capacitors to permit dc biasing of the varactors. The dimensions and characteristic impedance of shorting stub L in Fig. 6 are given in Fig. 7. The best value for R was found to be 68 ohms. Capacitor C_2 is a virtual short for the pump frequency, and is formed by insulating a cylindrical brass slug (s) from the stub outer conductor by a 0.002 inch thick Teflon tape. Using this type of matching network, PLO VSWR's were reduced from the range of 8 to 12 to values of less than 2 for every PLO.

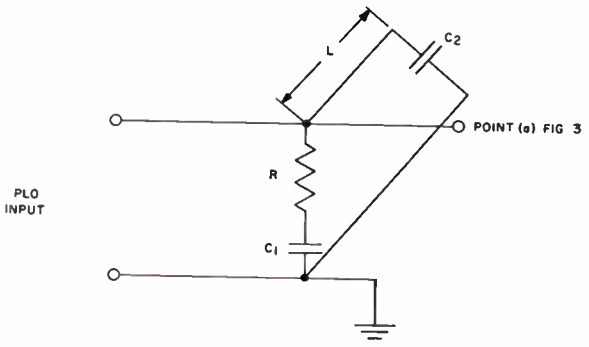


Fig. 6—PLO input matching network.

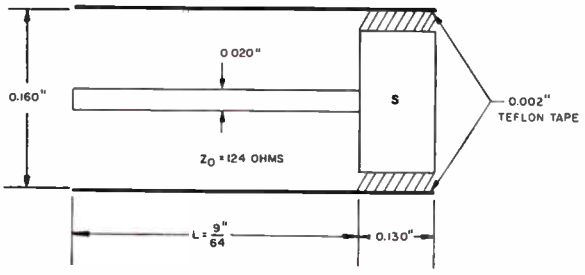


Fig. 7—Details of that part of Fig. 6 designated by L.

Normally it would be expected that the incident power requirements for the PLO would decrease as the input match is improved; however, it increased due to losses in the matching network. For PLO's without matching networks, the incident power requirements ranged from 12 to 25 mw; PLO's with matching networks required incident power requirements ranging from 30 to 100 mw. With a matching network, a typical PLO efficiency is 1 per cent.

This increased power requirement theoretically could be overcome by employing a four-terminal matching network, made up of lossless elements; however, such a network has three serious drawbacks:

1) The network would be larger than the one employed.
2) The lossless elements provide energy storage which has the effect of increasing the PLO response time.
3) This lossless network can act as a resonant circuit and thus cause the PLO to generate spurious frequencies.

Electrical Tests

A. PLO Internal Impedance

The measurement technique employed to determine the PLO internal impedance is the same as that for linear networks, and is based on the "Maximum Power Transfer Theorem of Linear Networks." This theorem states that a generator with a complex internal impedance will deliver maximum power to an external load when the external load is equal to the complex conjugate of internal impedance.

The equivalent circuit of the oscillating PLO when looking back into its output terminal is shown in Fig. 8.

The technique for finding the maximum power the PLO can deliver under fixed input power conditions and thus indirectly finding the PLO internal impedance is as follows.

Using a line stretcher, shorting stub and thermistor as the PLO termination, vary the line stretcher and stub alternatively while observing the output power on a power bridge. A unique combination of stub and line stretcher length will be found for which the power measured will be a maximum.

From the knowledge of the minimum shifts, the VSWR, and some basic transmission line equations, the impedance that the termination presents to the PLO can be determined. The PLO impedance is the complex conjugate of this impedance. An impedance plot resulting from the above measurement is found in Fig. 9, which shows the internal impedances of two PLO's. Several output power levels are recorded along the constant VSWR circles to show how the power varies from maximum to minimum.

An important consequence of the internal impedance measurements was the discovery that for certain impedances presented to the PLO output terminals, the PLO will generate spurious frequencies which interfere with the phase-locking properties of the PLO.

The need to determine conditions under which spurious frequencies are generated resulted in a measurement technique described below, for analyzing the output spectrum of PLO's.

B. Spectrum Analysis of PLO Output

The PLO output spectrum was measured using a heterodyne detector, a procedure that involves a local oscillator, a crystal mixer and a high gain intermediate frequency amplifier. The resolution of such a spectrum analyzer is the bandwidth of the IF amplifier, in this case 0.5 Mc. The sensitivity depends on the noise figure of the crystal mixer; levels of −70 dbm were easily detected.

The normal output of a PLO is about 0 dbm (one milliwatt). The IF amplifier used is the General Radio Model 1216.

Such an arrangement was used to measure the levels of the two sneak signals due to unbalance, as well as to detect signals that were neither at the pump or subharmonic frequency.

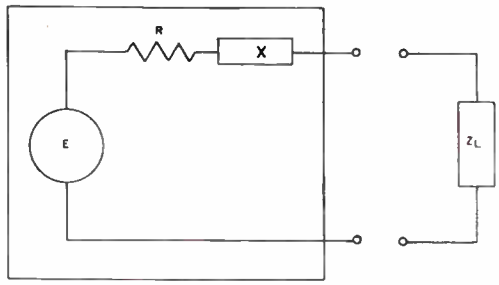


Fig. 8—Equivalent circuit of oscillating PLO as viewed from output terminals.

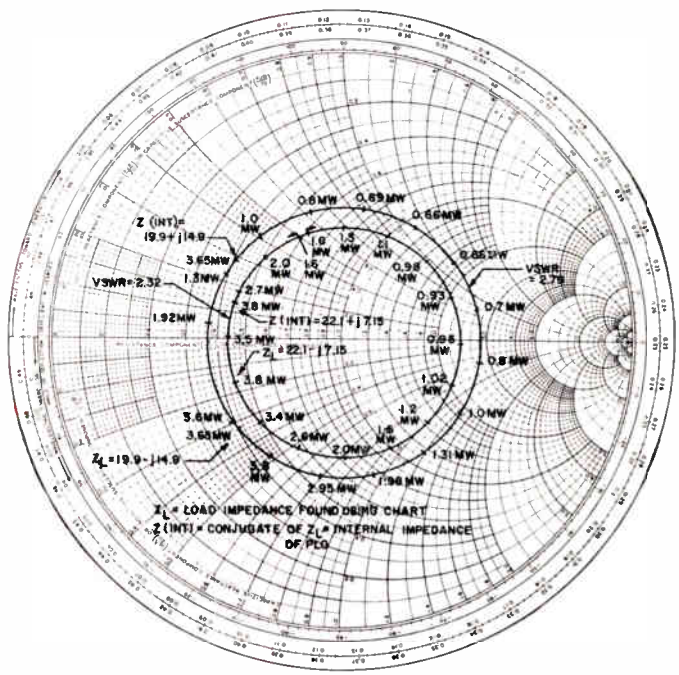


Fig. 9—Graph of PLO power output as a function of load impedance.

Driving the PLO from a pump source having an impedance equivalent to a VSWR greater than two permits the PLO to generate spurious frequencies. Similarly, loading the PLO with an impedance having a VSWR greater than two at the subharmonic frequency may result in the generation of spurious frequencies. The exact conditions under which spurious frequencies arise depend on the degree of balance in the PLO and on the length of the transmission lines connected to the PLO. With well balanced units and with short connecting lines, larger VSWR's can be tolerated. Theoretical considerations show that a transmission line with a high VSWR has properties similar to those of a tuned circuit.

The existence of spurious frequencies can be quantitatively explained by the Manley-Rowe relations.[2]

[2] J. M. Manley and H. E. Rowe, "Some general properties of nonlinear elements," Proc. IRE, vol. 44, pp. 904–913; July, 1956.

The spectrum analysis equipment can also be employed to determine the degree of isolation between pump and signal power both at the input and output PLO terminals.

The ratio of signal-to-pump level at the output terminals is controlled primarily by the orientation of the output loop with respect to the varactors. The optimum output loop orientation is a compromise between a desire for maximum signal and a minimum pump signal.

The ratio of the pump-to-signal level at the input ports is primarily a function of the varactor characteristics, but it is also affected by the output loop orientation.

Table I shows typical isolation levels attained at the PLO input and output terminals.

TABLE I
ISOLATION BETWEEN PUMP AND SIGNAL*

PLO No.	Input Terminal		Output Terminal	
	Signal (db)	Pump Signal (db)	Signal (db)	Pump Signal (db)
1	10	35	44	24
2	15	34	43	21
3	6.4	37	42	27
4	10.0	30.0	42.0	26.0

* Input and output sides are not related to the same absolute level.

C. Biasing

In the 2-kMc pumped PLO's and the first 3.7-kMc pumped PLO's, the bias was injected by means of a resistor connected inside the PLO box. The subsequent technique was to inject the bias at some remote point in the pump distribution system. This technique had the decided advantage of requiring only one bias injection point, and the elimination of a biasing resistor at each PLO.

For the final subsystem built, the method of a single bias injection point was abandoned, although the method of injecting it remotely was retained.

The single bias injection point was abandoned when the power distribution system was converted from the transmission line transformer to the 3-db coupler type, because the coupler system could not be conveniently built with a common dc source feeding all PLO ports.

There are two basic types of PLO biasing:

1) Use a dc source such that the bias level will permit the PLO to oscillate whenever the RF pump power is applied.
2) Use a pulsed bias. For the pulsed bias, the pump power is maintained at a constant level and the PLO's turn on and off according to the instantaneous pulsed-bias conditions.

Experiments showed that for a pump frequency of 3.7 kMc, a modulation rate of 140 Mc is possible if bias modulation is used. Typical PLO performance at a 40-Mc bias-modulation rate is shown in Fig. 10. The figure shows the bias modulating wave superimposed on the PLO output.

From the standpoint of operating speed, it would appear that the pulsed bias approach is attractive. However, there exists the possibility of other problems. The most serious of these is the PLO phase shift with change of bias. The phase shift during the bias build-up period might prevent proper phase lock between PLO's. Because of time limitation, this problem was not investigated and the pulse bias method was dropped in favor of a fixed bias.

Laboratory measurements showed that the fixed bias requirements at an input pump power level of 100 mw peak varied from 1.5 to 1.9 volts for a lot of eight PLO's.

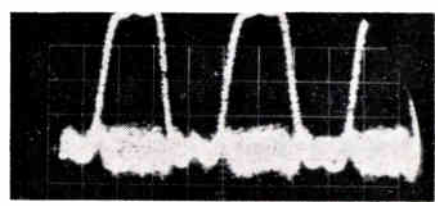


Fig. 10—Photograph showing both biasing wave form (large square wave) and PLO output modulated at 140-Mc rate.

D. Phase-Locking Range

Phase-locking range is defined as the range over which the phase of a control signal, derived from a PLO, can be varied before it loses the ability to control the output phase of other PLO's in the system.

In addition to phase-locking range, the amount of phase shift that the signal distribution box introduced must also be determined. The distribution box phase shift plus the cable connecting two adjacent boxes must always add up to an even number of half wavelengths for locking in phase, and an odd number of half wavelengths for out-of-phase locking.

A block diagram for measuring signal distribution phase shift, and phase-locking range is shown in Fig. 11. The length of cables *b* and *c* is adjusted so that the delay between network *A* and the viewing point *d* is equal to the delay between network *B* and viewing point *d*. Under these circumstances, the output of the two PLO's, when viewed at point *d*, will be the sum or difference depending on whether the PLO's are in or out of phase. Whether the outputs are locked in or out of phase depends on the length of cable *a*. Fig. 12 presents four photographs showing waveforms of various phase-locked conditions.

The phase-locking range is determined by varying the length of cable *a* by known increments and observing the output at point *d*. Thus, starting with the case depicted by Fig. 12(d), the two PLO's will continue locked in phase until cable *a* is changed by an amount

ΔL, at which point the two PLO's will no longer be locked and the output will begin to alternate between the conditions depicted in Fig. 12(d) and 12(c). This condition will persist as cable *a* is further changed. As the length of cable *a* is further changed, the output will abruptly change to an out-of-phase locked condition, as depicted by Fig. 12(c). A diagram of the phase-locking pattern is shown in Fig. 13.

The phase-locking ranges are designated by ΔL_2 and ΔL_4. The electrical equivalents for the ΔL's in a typical case are given in Table II.

In an ideal system ΔL_1 and ΔL_3 are zero, while ΔL_2 and ΔL_4 are each 180°. To permit the widest variation in tolerances, the cables connecting distribution boxes should provide operation in the middle of either ΔL_2 or ΔL_4.

The minimum connecting cable lengths are determined by mechanical requirements. For the subsystem under study, the minimum cable length for out-of-phase locking is 5.33 inches, and for in-phase locking it is 7.49 inches. These lengths take into account the fact that the velocity of propagation in the cable is 68 per cent of the velocity of propagation in free space.

Signal Distribution

The signal distribution system is composed of the distribution boxes and their associated connecting coaxial cables. The cylindrical shaped distribution boxes house a network of resistors which combines the inputs for majority logic, as well as providing the outputs for majority logic at remote modules. The major requirements of the distribution system are:

1) The maximum amplitude deviation between any of the three signals making a majority group must not exceed 2.5 db.
2) The sneak path signals must be kept at least 20 db below the direct signal.
3) The distribution box must present a good impedance match to the connecting PLO and to each coaxial cable entering the box.
4) The phase shift through the distribution system must be near the center of the phase-locking range of the PLO's.

A cross section of the distribution box is shown in Fig. 14.

Points designated *a* connect to corresponding points on similar boxes which together form the signal distribution system. In cases where all *a* points on one distribution box are not required to connect to similar *a* points on other boxes, those excess *a* points are terminated in 50-ohm impedances. Thus instead of 39 ohms in series with the center of the box, 89 ohms is connected from the center to ground.

The 20-ohm impedance section of line shown in Fig. 14 transforms the impedance at the center of the distribution box to 50 ohms at the PLO connecting port.

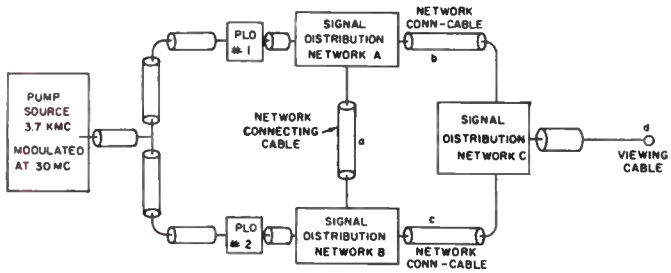


Fig. 11—Phase-locking range test set-up.

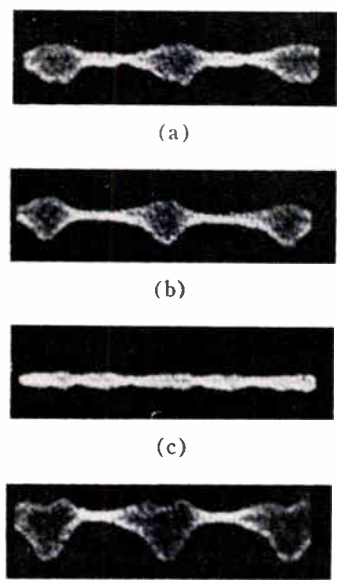


Fig. 12—(a) Output from PLO #1 only; (b) output from PLO #2 only; (c) combined out-of-phase output from PLO #1 and #2; (d) combined in-phase output from PLO #1 and #2.

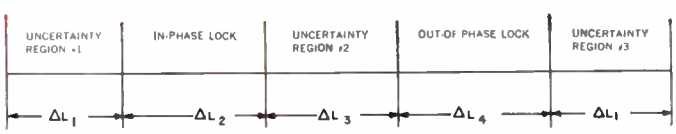


Fig. 13—Line diagram showing phase-locking characteristics.

TABLE II
Phase-Locking Range in Electrical Degrees

	ΔL_1	ΔL_2	ΔL_3	ΔL_4
Electrical degree	32°	146°	36°	146°

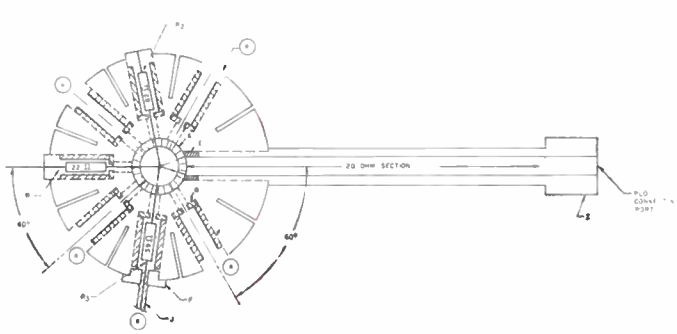


Fig. 14—Cross-sectional view of distribution box.

TABLE III
DIRECT AND SNEAK SIGNAL ATTENUATION VS FREQUENCY

Frequency	1.55 kMc		1.85 kMc		2.15 kMc	
Module Number	Direct Attenuation (db)	Sneak Attenuation (db)	Direct Attenuation (db)	Sneak Attenuation (db)	Direct Attenuation (db)	Sneak Attenuation (db)
301 to 303	23.5	—	22.8	—	22.7	—
301 to 404	22.5		22.0		23.0	
302 to 301 via 404	—	46.0	—	44.0	—	43.0

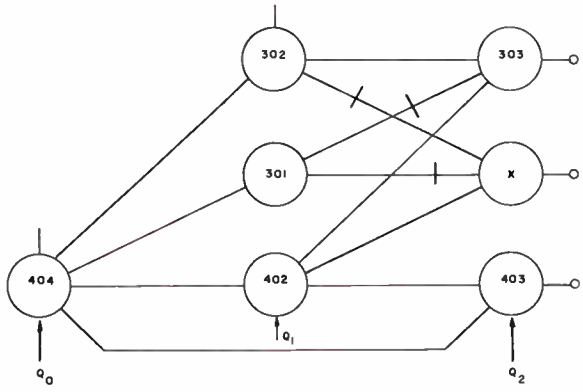
Table III shows attenuation characteristics which are typical for the distribution network subsystem. Direct attenuation is defined as the attenuation between the input ports of two distribution boxes which are connected by only one signal cable. The sneak path attenuation is defined as the attenuation between two input ports when the two ports are separated by a third distribution box.

The logic performed by the subsystem can be explained with the help of Fig. 15(a). Although not shown in the figure, a PLO is directly connected to each of the distribution boxes. The three columns designated by θ_0, θ_1 and θ_2 indicate the three phases of the pump source; each column shows how many PLO's are powered by each phase. The three boxes 404, 402 and 403 with attached PLO's comprise a circulating ring which by definition stores a "one" or a "zero" in its phase. This ring phase is used as the reference to check the majority logic performed at boxes 303 and X.

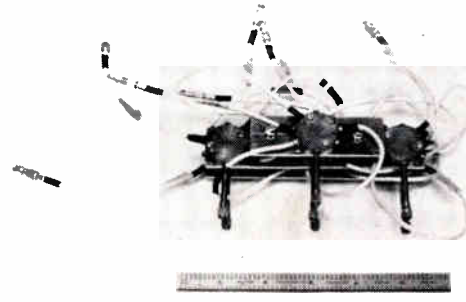
The lines between boxes in Fig. 15(a) represent coaxial cable. These cables are of two lengths, differing by 180° at the signal frequency, 5.33 inches for out-of-phase locking and 7.49 inches for in-phase locking; the shorter cables are designated by a short cross bar. The PLO connected to box X receives two signals out of phase with the reference ring and one in phase; its output will be out of phase with the output from the PLO connected to box 403. The outputs of these two PLO's will be out of phase. On the other hand, the PLO connected to box 303 receives two signals in phase with the reference ring and one out of phase. Its output, therefore, will be in phase with the output from the reference PLO connected to box 403. A visual demonstration of the two types of combination is shown in Fig. 12(c) and 12(d), respectively.

This system of logic requires but a single type of gate, the majority gate. The construction described above of two majority gates with different input patterns indicates the feasibility of such a system at microwave frequencies.

To determine the susceptibility of the majority logic performance to variations in PLO characteristics, the PLO's on distribution boxes 301, 302, and 402 were interchanged in their six possible combinations. Majority logic was performed with every combination.



(a)



(b)

Fig. 15—(a) Subsystem logic diagram. (b) Photograph of logic diagram.

TABLE IV
DIRECT SIGNAL ATTENUATION OF DISTRIBUTION SYSTEM

Path	Attenuation (db)
X to 301	20.9
X to 302	23.1
X to 402	21.5
404 to 403	21.8
404 to 402	20.4
404 to 302	20.2
404 to 301	22.0
403 to 402	24.0
303 to 402	19.5
303 to 302	21.8
303 to 301	22.5

Fig. 15(b) is a photograph of the subsystem represented by Fig. 15(a). The attenuation between distribution boxes for the subsystem shown in Fig. 15 is given in Table IV.

Pump Power Distribution System

The power distribution system consists of the following:

1) A 2K43 klystron used as the basic source of carrier pump.
2) A square wave modulator operating at a frequency of 30 Mc which modulates the output of the 2K43 klystron.
3) A TWT which converts the modulated-klystron low-level signal to a high-level pulsed-pump source.
4) A three-way divider. The output lines on the divider are delayed with respect to each other by $\frac{1}{3}$ of the 30-Mc period. These delays effectively create a three-phase pump power system.
5) The five 3-db directional couplers which distributed the power from each of the three delay lines to the seven PLO's in the subsystem.

Directional couplers are linear four-part devices, commonly used at microwave frequencies, which have unidirectional properties.

The 3-db couplers used serve as two-way power splitters with the additional property of preventing interaction between the two outputs parts.

A block diagram of the power distribution system is shown in Fig. 16.

A diagram of that part of Fig. 16 designated as "system of 5 couplers" is shown in Fig. 17(a). Fig. 17(b) is a photograph of the couplers; in addition the figure shows the set of seven PLO's and the signal distribution network. In Fig. 17(a), couplers *A*, *B*, and *C* are commercial items whereas couplers *D* and *E* are of the strip transmission line type which were laboratory made. Fig. 17(a) also shows the relative power levels of the six output ports, measured with respect to port five. Ideally, these six ports should be at the same power level. It is important, however, to note that despite the wide variation in pump levels, the subsystem functioned properly. More important than even-power level distribution for the proper functioning of a system is the need for VSWR's of less than 2:1 when looking into the pump power distribution ports. Experience with the design of couplers *D* and *E* [Fig. 17(a)] shows that a VSWR of less than 2:1 can be easily accomplished.

Conclusions

This work shows that computer subsystems using kilomegacycle subharmonic oscillators, in which majority logic is employed, is feasible. The nonuniformity in the operating characteristics from one PLO logic module to the next and the nonuniformity of pump power levels suggest that more engineering work and time could profitably be spent on these problems. It is also apparent that the PLO input matching network is too inefficient to be attractive in a large system.

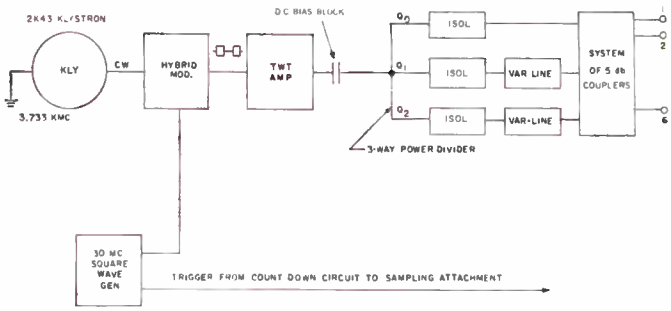
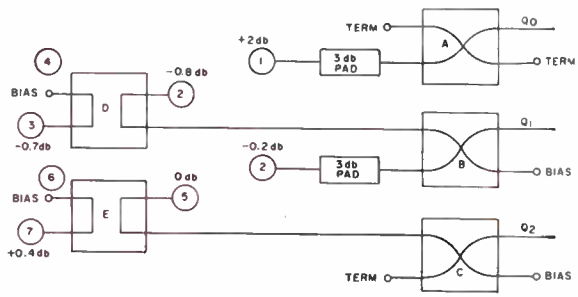
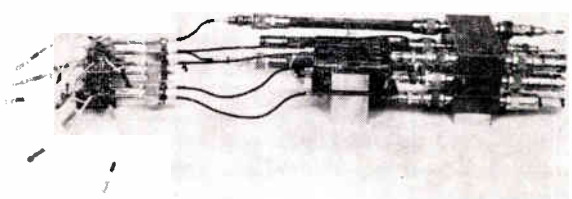


Fig. 16—Block diagram of power distribution system.



(a)



(b)

Fig. 17—(a) Detail diagram of five-directional couplers (Fig. 16) showing relative power levels at PLO connecting parts. (b) Photograph showing the PLO subsystem connected to the five-directional coupler shown in (a).

Although in theory there are several techniques for distributing the pump power, it has been found that the only practical technique is to use 3-db directional couplers.

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[2] A. Uhlir, Jr., "The potential of semiconductor diodes in high-frequency communications," Proc. IRE, vol. 46, pp. 1099–1116; June, 1958.
[3] E. A. Guillemin, "Communication Networks," John Wiley and Sons, Inc., New York, N. Y., vol. 1, ch. 8.
[4] J. Hilibrand, C. W. Mueller, C. F. Stocker, and R. D. Gold, "Semiconductor parametric diodes in microwave computers," IRE Trans. on Electronic Computers, vol. EC-8, pp. 287–297; September, 1959.
[5] W. Sauter and P. J. Isaacs, "Microwave Logic Circuits Using Diodes," presented at Symp. on Microwave Techniques for Computing Systems, Washington, D. C.; March, 1959.
[6] W. R. Beam, D. J. Blattner, and F. Sterzer, "Microwave Carrier Techniques for High-Speed Digital Computer," presented at Symp. on Microwave Techniques for Computing Systems, Washington, D. C.; March, 1959.
[7] E. Goto, "The parametron, a digital computing element which utilizes parametric oscillations," Proc. IRE, vol. 47, pp. 1304–1316; August, 1959.
[8] F. Sterzer, "Microwave parametric subharmonic oscillators for digital computing," Proc. IRE, vol. 47, pp. 1317–1324; August, 1959.

A Survey of Tunnel-Diode Digital Techniques*

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Summary—**The tunnel diode, because of its high switching speed, wide environmental tolerance, and adaptability to digital computing circuits, has attracted much attention in the digital computer field. Efforts have been devoted to its application in both memory and logic circuits. Results have been most promising in high-speed random-access memories and in dynamic logic systems utilizing multiphase clock sources. This paper discusses the major techniques that have been reported plus some that have been developed by the authors and their associates at Bendix Research Laboratories.**

Introduction

THE tunnel diode appears likely to take a place along with the semiconductor diode rectifier, the transistor, and the ferrite core in the field of digital computing equipment. It may, in fact, replace all of these devices in high-performance computers of the future, for the tunnel diode can be employed in both memory and logic applications. The purpose of this paper is to point out the outstanding characteristics of tunnel diodes and describe several methods of using these devices in digital circuits.

A notable characteristic of the tunnel diode is its fast switching speed. Currently available tunnel diodes switch in about one nsec (nsec = nanosecond = 10^{-9} second), and faster speeds are expected in the future. The peak current and the reverse current in a tunnel diode are due to the "quantum-mechanical tunneling" of majority carriers across a very thin semiconductor junction, a process which theoretically occurs at nearly the speed of light.[1] Junction capacitance and external circuit parameters are the important practical limiting factors on switching speed.

The tunnel diode is also capable of operation over wide temperature ranges and can withstand relatively large doses of nuclear radiation. These characteristics are due to the very heavy doping which is employed and to the lack of dependence on minority carrier lifetimes. The heavy doping also results in a tolerance of surface contamination. The characteristics of tunnel diodes should therefore not be greatly affected by time, and hermetically sealed packages may not be necessary.

A third desirable tunnel-diode characteristic is the mechanical simplicity which results from its having only two terminals. Since there is no necessity to connect a third lead to an extremely small area, as is the case for transistors, the device should be reasonably economical to manufacture.

* Received by the IRE, August 4, 1960.
† Bendix Corp., Res. Labs. Div., Southfield, Mich.
[1] R. N. Hall, "Tunnel diodes," IRE TRANS. ON ELECTRON DEVICES, vol. ED-7, pp. 1–9; January, 1960.

The above factors account for the interest which the tunnel diode has excited since its introduction. There are, however, problems involved in designing circuits to utilize the device. Most of these stem from three sources. First, gain can only be achieved by utilizing the negative-resistance characteristic of the tunnel diode. Second, the tunnel diode has only two terminals, and these must be used for both input and output. Third, the voltage signal obtainable from tunnel diodes is quite small, less than ½ volt for germanium units and under 1 volt for gallium arsenide units. The influence of these factors on circuit design will be pointed out in the body of the paper.

The paper is divided into two main sections, which cover memory and logic applications, respectively. Circuits and organizations of random-access memories are given particular attention in the discussion of memory applications. Several of the circuits that are suitable for logic are also inherently suitable for storage—the equivalent of flip-flop or shift-register storage in transistor circuitry. These circuits are discussed in the section which describes logic applications. The discussion of logic circuits also includes a description of several other tunnel-diode circuits, such as approximations to current and voltage sources, which are useful in conjunction with logic circuits.

Memory Circuitry

The characteristic current-voltage curve of the tunnel diode suggests the possibility of adding a series resistor and a voltage source such that two stable states, *A* and *B* of Fig. 1, are produced. (Point *C* is, of course, unstable.) These two stable states can be assigned correspondence with the two values of a binary variable. To make a useful storage element it is then necessary to provide a means for changing the state of the circuit from one stable state to the other and a means for sensing the state of the circuit.

The state of the circuit can be changed by varying the source voltage, the resistor, or both. Varying the voltage is generally simpler and is the technique in general use. The state of the circuit can be sensed in a number of ways which can be grouped into two major classes: destructive and nondestructive.

In destructive read-out a signal is applied to establish a certain state of the circuit. If the circuit is already in that state, no major change occurs; if it is initially in the other state, a major change does occur. The occurrence or nonoccurrence of a change in state can be sensed in various ways. Destructive read-out is discussed later in connection with a particular system.

In nondestructive read-out, either the static state of the circuit is sensed directly or else a signal is applied to disturb the circuit in some way which will produce different responses for the two possible states, but which will not change the state of the circuit. A number of nondestructive read-out techniques for use with variations of the circuit of Fig. 1 have been reported.[2,3] One of these techniques utilizes the fact that the curvatures of the two positive-resistance portions of a tunnel diode $I-V$ characteristic are different. Therefore the amplitude of the beat frequency produced when two signals with different frequencies are applied to the tunnel diode will be greater for one state than for the other. Another of these techniques utilizes the fact that in some tunnel diodes the junction capacitance is a significant function of the applied voltage in one of the positive-resistance regions but not in the other. Such a tunnel diode can be connected into a parametric oscillator circuit which will give rise to subharmonic oscillations only if the tunnel diode is in the state in which the capacitance varies with voltage. Still another of these techniques utilizes an auxiliary tunnel-diode circuit connected to each memory element. In one variation of this technique the auxiliary circuit can be forced into oscillation by applied signals of a certain amplitude if the memory element is in the high-voltage state but not if it is in the low-voltage state. The oscillation is caused by forcing the tunnel-diode operating point into the negative-resistance region. Enough energy is radiated for detection by a tuned amplifier. In another variation the tunnel diode in the auxiliary circuit is normally held in the low-voltage state, and the applied signals can drive it to the high-voltage state if the memory element is in the high-voltage state, but not if the memory element is in the low-voltage state.

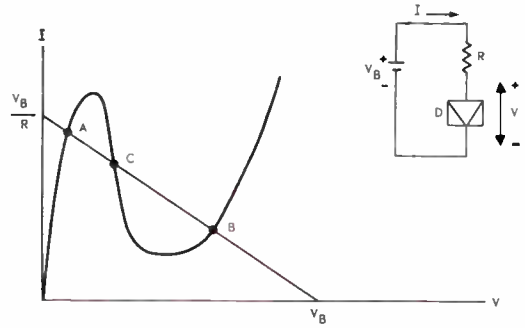

Fig. 1—Tunnel-diode characteristic curve with load line.

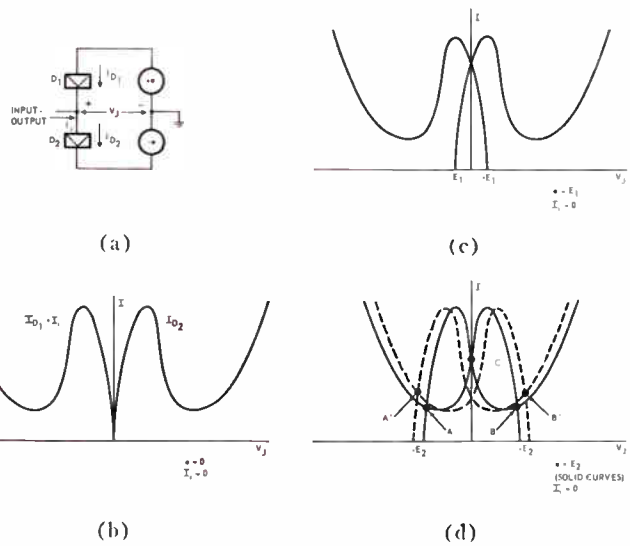

Fig. 2—(a) Goto-pair memory element. (b–d) Graphical representation of successive conditions during switching.

At least one basic approach to tunnel-diode memories in addition to that illustrated in Fig. 1 has been reported. An approach which can be utilized for either memory or logic has been proposed by E. Goto of the University of Tokyo[4] and is referred to as the "Goto-pair" approach. This approach is illustrated in Fig. 2, and the operation of the circuit will be described with references to the plots of that figure. These plots show the use of conventional techniques of graphical circuit analysis to determine the voltage at the junction of the two tunnel diodes (V_j) as the source voltages ($+e$ and $-e$) are varied. The value of V_j at any time will, of course, correspond to an intersection of the two curves that represent 1) the $I-V_j$ curve for tunnel diode D_2 and 2) the $I-V_j$ curve for tunnel diode D_1 displaced from the horizontal axis by an amount equal to I_i, the current forced into the input-output terminal. In this discussion it is assumed that the two tunnel diodes have identical characteristics.

As the source voltages are increased from 0 [Fig. 2(b)] to some voltage less than the peak voltage of the diodes [Fig. 2(c)], V_j will remain at 0. As the source voltages are increased still further, to a point beyond the peak voltage of the tunnel diodes [Fig. 2(d)], there will be two possible stable operating points, A and B; point C is not stable. The actual operating point (A or B) can be established by forcing a small control current to flow either into or out of the junction of the diodes just before and during the time at which the source voltages equal the diode peak voltages. If the control current is forced into the junction, the resulting final operating point will be B; if the control current is forced out of the junction, the final operating point will be A.

A method for using this basic circuit for memory is described in Goto, *et al.*[4], and is attributed to Murata. In it, after the state of the circuit has been established, the source voltages are normally held in the condition indicated by Fig. 2(d). If the source voltages are then both changed slightly in magnitude as indicated by the dashed curves of Fig. 2(d), the new (temporary) operating point will be A' or B' depending on whether the

[2] J. C. Miller, K. Li, and A. W. Lo, "The Tunnel Diode as a Storage Element," Presented at Internat. Solid-State Circuits Conf., Philadelphia, Pa.; February 10–12, 1960.

[3] J. A. Rajchman, "Solid-state microwave high speed computers," *Proc. EJCC*, pp. 38–47, December 1–3, 1959.

[4] E. Goto, K. Murata, K. Nakazawa, K. Nakagawa, T. Motooka, Y. Matsuoka, Y. Ishibashi, H. Ishida, T. Soma, and E. Wada, "Esaki diode high-speed logical circuits," IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-9, pp. 25–29; March, 1960.

initial state was A or B. From Fig. 2(d) it can be seen that if the junction of the tunnel diodes was negative the new (temporary) operating point will be more negative, and if it was positive it will be more positive. Thus the direction of the change of the junction voltage will indicate the state of the circuit. The amount of the change will be related to the difference in slope of the two positive-slope portions of the tunnel-diode characteristic curve.

A variation of the basic circuit just described is shown in Miller, *et al.*[2] In this variation there is only one voltage source, and it is connected across the two tunnel diodes. The output voltage is the voltage across one of the tunnel diodes, and it is the magnitude of this voltage, rather than the polarity, that is significant.

The discussion thus far clearly indicates that there are many ways in which tunnel diodes can be used as basic components in memory circuits. Also, it is still early in the history of tunnel diodes, and it is likely that many other ways will be developed. However, among the most promising of the approaches that have been reported so far are those that utilize the basic circuit of Fig. 1 in destructive read-out schemes. The major advantages of these approaches are simplicity and high-speed operation. They are attractive for use in high-speed random-access memories suitable for parallel computers, particularly those required to operate under adverse environmental conditions such as those encountered in military and space applications. These approaches to the design of a practical memory will be discussed in some detail.

Fig. 3 illustrates the switching conditions for the basic circuit of Fig. 1, assuming that the load resistor is held constant (as will most likely be the case in practice). If the applied voltage is V_B both before and after switching, then the change in state from point A to point B (or vice versa) will be indicated by a change in current, I_s, and a change in voltage, V_s.

Fig. 4 shows four possible memory circuits based on the circuit of Fig. 1. Two fairly basic configurations of memory element are shown, each with two possible means of sensing changes in the state of the element. In each circuit diagram the basic memory element, *i.e.*, that portion of the circuit that must be repeated for each bit of information storage capability, is pointed out. The inductors and capacitors shown are used to route the drive pulses and the bias current over the desired paths. In the circuits utilizing the voltage-output element, the resistors and voltages would be relatively large compared to those depicted by the load lines on Fig. 3; the load lines for this type of element would usually have much smaller slopes than those in the figure. The purpose of this is to increase the change in voltage that occurs upon switching. However, the power dissipation is also increased, so a compromise must be reached.

All of these circuits appear to be feasible for use in practical memories, and it seems that the major problems associated with any of the approaches have parallels in the other approaches. An experimental memory utilizing the approach shown in Fig. 4(d) has been reported.[5] An experimental model of a memory utilizing the approach shown in Fig. 4(a) in a coincident-selection system has been built and is further discussed below.

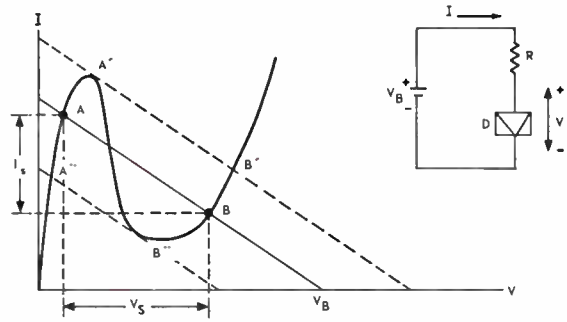

Fig. 3—Switching conditions for tunnel-diode and resistor combination.

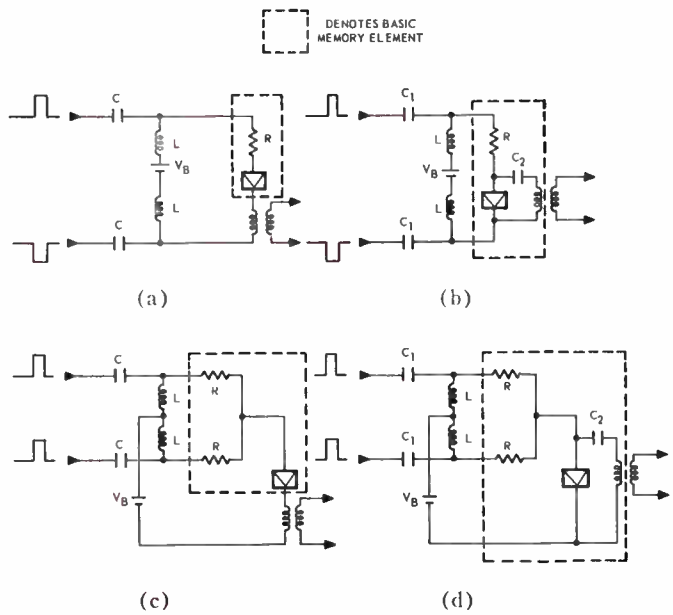

Fig. 4—Variations of basic memory circuits. (a) Two terminal current-output element. (b) Two terminal voltage-output element. (c) Three terminal current-output element. (d) Three terminal voltage-output element.

Fig. 5 shows the way in which the current-output element shown in Fig. 4(a) is connected into a matrix in an experimental system. To select a particular element in this matrix, a drive pulse of amplitude greater than half enough to switch an element, but less than enough, is applied to one of the lines connected to the element. A similar pulse but of opposite polarity is applied to the other line connected to that element. If the element was not initially in the state to which the drive pulses would tend to drive it, it will switch to that state. If the purpose of the selection was to determine the

[5] M. M. Kaufman, "A tunnel diode tenth microsecond memory," 1960 IRE International Convention Record, pt. 2, p. 114–123.

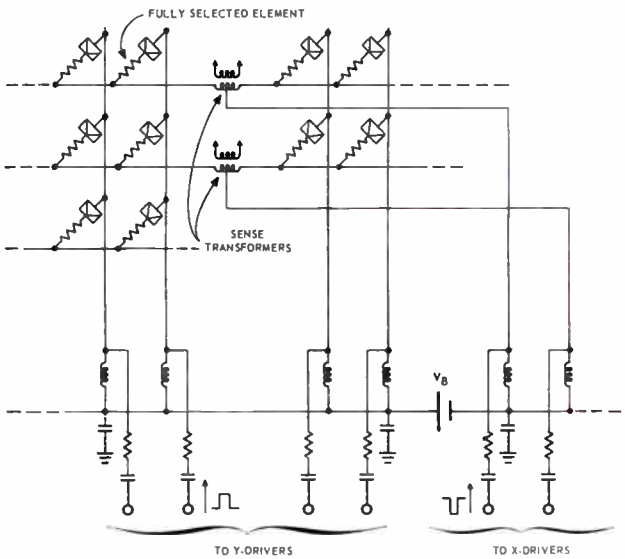

Fig. 5—Partial schematic of a memory matrix.

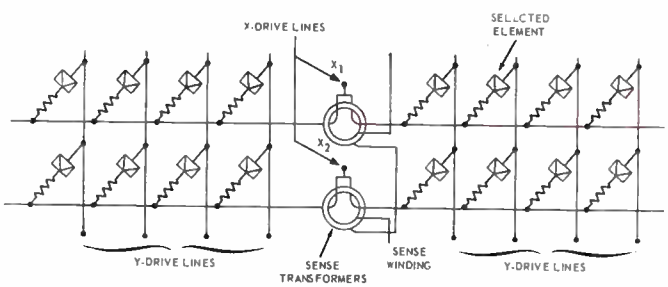

Fig. 6—Method of cancelling effects of partial-select currents.

state of the element, the sensing circuitry must indicate whether or not there was a switching of the element. If the element did switch, then a "permanent" change in the current through the primary winding of the sensing transformer connected to that element will take place. Note, however, with reference to Fig. 3, that while the drive pulse is present there is a change in the current through every element connected to either of the driven lines. After the drive pulse is removed these temporary changes die out, but a change due to the switching of the element persists. However, for high-speed operation it is desirable to sense the switching of an element as soon as possible, and therefore it is desirable to cancel out the changes due to partial switching of elements. Such cancellation can be accomplished to a considerable extent, as described below.

If the selected element switches, the effect is that of two partial-select currents plus a permanent change in current. If it does not switch, the effect is just that of two partial-select currents. Consider Fig. 6 which shows a section of a typical matrix. Note that the drive lines to the two halves of a horizontal line of the matrix are passed through the sense transformer core in opposite directions, and that the secondary windings of these two transformers are connected so as to have their outputs in opposition. Now consider what happens when drive pulses are applied to the selected element. The pulse on the X_1 drive line will cause partial-select currents in all the elements on that line. However, half of these partial-select currents pass through the associated transformer core in one direction, while the other half pass through it in the other direction; thus their effects cancel. The Y drive line connected to the selected element will cause partial-select currents in each of the two elements to which it is connected. These two partial-select currents must pass through the transformer cores shown in the diagram, and they will produce output voltages in the transformer secondaries. However, since the secondaries are connected in series opposition, the effects of these partial-select currents are canceled.

Thus the effects of all the partial-select currents in the matrix section shown in Fig. 6 can be made to cancel, provided that all partial-select currents are equal and that the transformers are identical. To take advantage of this cancellation scheme there must be an even number of memory elements along each axis of a matrix; otherwise the matrix could not be considered to be made up of sections such as that shown in Fig 6. A disadvantage of this cancellation scheme is that half the memory elements will produce one polarity of output from the sense circuitry and the other half will produce the opposite polarity. However, a fairly simple scheme for handling these two output polarities has been devised.

The assumption that all partial-select currents are equal is not completely valid. As can be seen from an inspection of Fig. 1, the slopes of the two positive-resistance portions of a tunnel diode I–V characteristic are not the same. Thus an element initially at point A (Fig. 1) will produce a different partial-select current than an element initially at B. This effect can place a limitation on the number of memory elements of a particular type that can be connected to a single sense circuit and still provide a sufficient signal-to-noise ratio for good operation at high speed.

In order to make a complete memory, a number of matrices such as the one shown in Fig. 5 must be combined. An example of how this can be done is illustrated in Fig. 7. It will be noted from Fig. 7 that along one axis of the memory the corresponding lines of all the matrices can be connected together. This is due to the fact that when a word is to be written into memory a partial-select drive pulse can be applied to one of the corresponding lines of every matrix in the memory. However, along the other axis of each matrix a drive pulse must either be applied or not applied to the selected line, depending on whether or not it is desired to write a ONE into the element. Thus, as is shown in Fig. 7, drive circurity must be provided for every line coming out of one face of the memory. Also, this circuitry must be capable of being controlled so as to write a ZERO, *i.e.*, not to switch an element, when the corresponding bit-position of a word is to contain a ZERO.

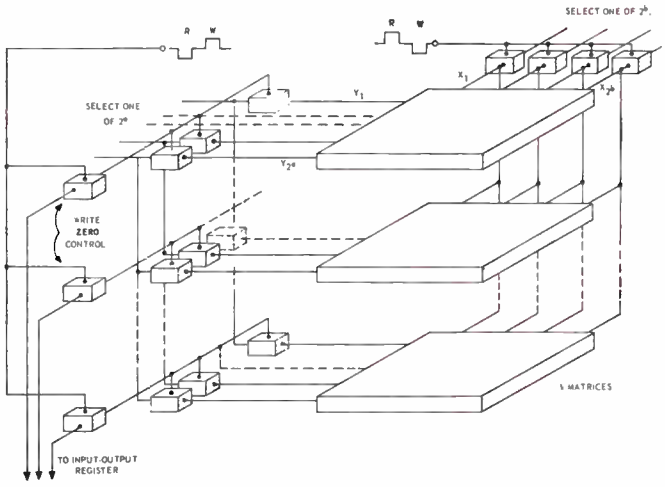

Fig. 7—Interconnection of matrices and drive circuitry.

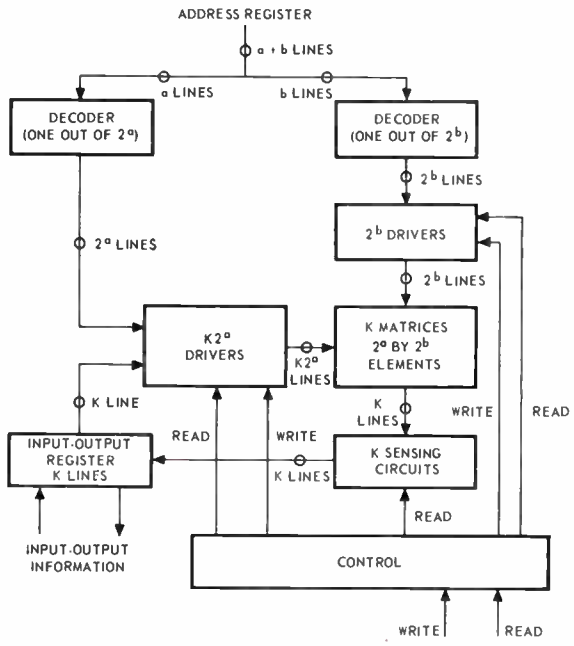

Fig. 8—Block diagram of complete memory.

Fig. 8 shows a block diagram of a complete memory corresponding to Fig. 7 and gives a rough indication of the equipment that is required, as a function of memory size.

Although the above discussion has been in terms of a coincident-selection system, it is also feasible to use this element in linear-selection systems. Such a memory is likely to require more equipment than a coincident-selection memory of comparable capacity, especially for memories larger than about 64 words. It appears at present that linear selection is preferable for small memories and that coincident selection is preferable for large memories, with the dividing line being approximately 64 to 128 words.

Logic Circuitry

General Characteristics

Although there are many possible tunnel-diode logic circuits, they can be generally described as having the following characteristics in common. First, the logic gain (number of inputs plus number of outputs) will depend very much upon the tolerances which can be held in tunnel-diode characteristics and in the components and supply voltages associated with the circuit. Secondly, since the tunnel diode is a two-terminal device, the same pair of terminals must be used for both input and output. This characteristic requires special attention, both in circuit design and logic design. Finally, tunnel-diode logic circuits are generally designed in such a way that input signals can trigger a circuit in only one direction, *e.g.*, from the ZERO state to the ONE state. The circuit must therefore be reset by some external source before another logic operation can be performed.

The basic circuit configuration shown in Fig. 9 will be employed to illustrate the principles involved in tunnel-diode circuit and logic design. The operation of the circuit is similar to that of the memory element of Fig. 3, except that the logic circuit is best explained in

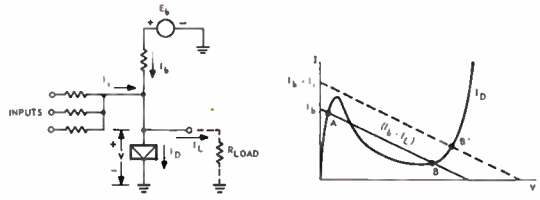

Fig. 9—(a) Basic analog-threshold logic circuit. (b) Characteristic curve and load line.

terms of current control instead of voltage control. In the circuit of Fig. 9(a), the tunnel diode and the load resistor, R_L, are supplied from an essentially constant current, I_b, which is derived from a resistor in series with a relatively high voltage, E_b. Fig. 9(b) shows the I–V characteristic of the tunnel diode with a resistive load line which yields two stable operating points, A and B. When the supply current is first turned on, the circuit assumes the state indicated by point A. However, if an input signal supplies a small additional current, the load line moves vertically as indicated by the dashed line. The only stable operating point is then point B'. Removal of the input signal after switching has occurred causes the load line to return to its original position, but the circuit is then in the state indicated by point B. The circuit will remain in this state until the supply current is turned off.

It is readily seen that the tolerances on the tunnel-diode peak current and supply current are both quite important to successful operation of this circuit. Logic gains of four or five are attainable with reasonable tolerances.

The above circuit also illustrates that the output sig-

nal of a logic circuit can affect the circuits which supply the input signals. One of several possible external means can be used to control the direction of information (signal) flow. The most straightforward approach is to place a conventional rectifying diode in each input path. Because of the small voltage excursions in tunnel-diode logic circuits, the switching action obtainable with conventional diodes is not very good. However, this method has been successfully used in several experimental circuits.[6]

An ideal coupling element to provide directionality and input-output isolation is the backward diode, whose characteristic curve is shown in Fig. 10. The backward diode can be described as a tunnel diode having zero or very low peak current. It can therefore be used as a rectifying device over the voltage range of interest in tunnel-diode logic circuitry. The commercial availability of backward diodes has, at the time of this writing, only recently been announced. Therefore, very little experimental work has been done with circuits which employ this device.

Another method for controlling the direction of information flow utilizes a three-phase power supply, or clock, analogous to the three-phase pump employed in parametron computer logic.[7] Fig. 11 shows a recirculating storage circuit which uses an overlapping three-phase power supply and the threshold logic circuit of Fig. 9. Information flows from left to right in synchronism with successive phases of the power supply. Note that the three circuits shown in the figure actually store only one binary digit of information. This is typical of storage registers, flip-flops, and counter circuits which employ this type of logic implementation.

Special requirements are placed on power or clock supplies because of the external reset signals which must be provided for tunnel-diode logic circuits. At least two sources of reset signals are necessary because the information contained in a system of logic circuits would be lost if all of the circuits were reset at the same time. Two-phase supplies are indeed suitable for some types of logic circuits if directionality is supplied by another means, such as rectifying diodes. However, if logic circuits such as those of Fig. 9 are used, the power supply must also control the number of logic stages through which a signal can propagate while a particular supply phase is turned on. If an overlapping two-phase supply were employed, all of the circuits in a system would be energized during the overlap period. Signals could therefore propagate through an indeterminate number of logic stages during this time. However, with a three-phase supply as shown in Fig. 11(b), one of the phases is always turned off, so input signals cannot affect the circuits in that phase. Synchronous propagation of signals can thereby be maintained in all portions of a system of logic circuits.

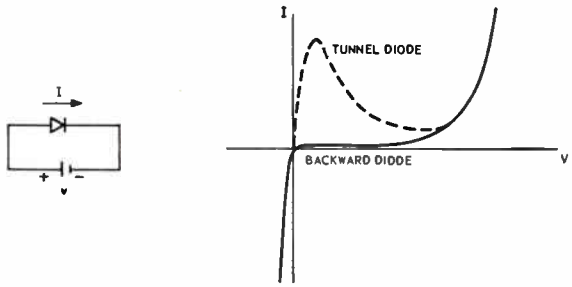

Fig. 10—Backward-diode I-V characteristic.

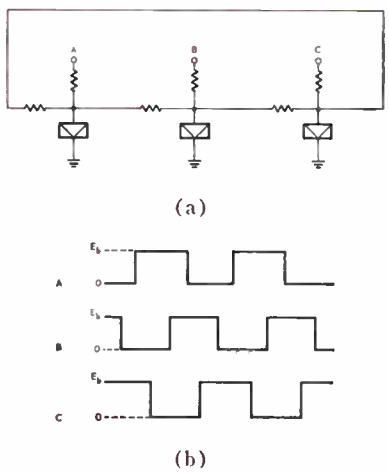

Fig. 11—(a) Recirculating storage circuit. (b) Power supply waveforms.

Gating Circuits

Threshold circuits can be used for the more common logic functions such as OR, AND, and NOT, as well as the less common functions of EXCLUSIVE OR, MAJORITY, and N-out-of-M logic (*e.g.*, 2 out of 5). All of the above functions can actually be performed by two basic circuits which have previously been described.[8,9] With proper biasing, the circuit of Fig. 9 will perform as an N-out-of-M circuit for any value of N from 1 to M. The OR, AND, and MAJORITY functions are simply special cases of N-out-of-M functions. Tolerances, of course, become more critical as N increases and reach the worst case for an AND gate. In this case it may be quite difficult to distinguish between the condition where all inputs are energized and the condition where all but one of the inputs are energized.

The NOT and EXCLUSIVE OR functions are performed by the circuit of Fig. 12. Here, the function performed depends upon the relative peak currents of the

[6] G. W. Neff, S. A. Butler, and D. L. Critchlow, "Esaki (Tunnel)-Diode Logic Circuits," Presented at 1960 Internat. Solid-State Circuits Conf., Philadelphia, Pa.; February 10–12, 1960.

[7] E. Goto, "The Parametron, a digital computing element which utilizes parametric oscillation," PROC. IRE, vol. 47, pp. 1304–1316; August, 1959.

[8] M. H. Lewin, "Negative-resistance elements as digital computer components," *Proc. EJCC*, pp. 15–27; December 1–3, 1959.

[9] M. H. Lewin, A. G. Samusenko, and A. W. Lo, "The Tunnel Diode as a Logic Element," Presented at Internatl. Solid-State Circuits Conf., Philadelphia, Pa.; February 10–12, 1960.

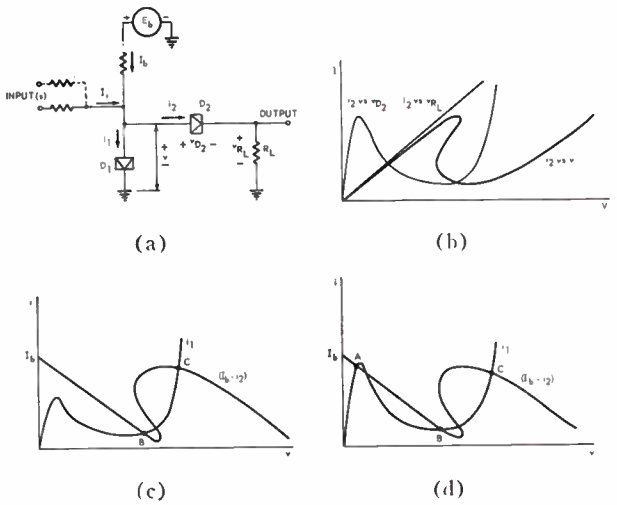

Fig. 12—(a) NOT or EXCLUSIVE OR logic circuit. (b) Composite I-V characteristic of D_2 and R_L in series. (c) NOT circuit graphical construction. (d) EXCLUSIVE OR circuit graphical construction.

two tunnel diodes employed in the circuit. Fig. 12(c) illustrates the graphical representation of a NOT circuit. When the supply current is first turned on, the circuit assumes the state indicated by point B on the characteristic curve. Here, almost all of the supply current is passing through the output diode and output resistor; therefore, the output voltage is high. However, an input current will eliminate the stable intersection at point B, causing the operating point to shift to the vicinity of point C. In this state very little current flows to the output diode and resistor, so the output voltage is low.

Fig. 12(d) shows the graphical construction for the EXCLUSIVE OR circuit. The only difference between this circuit and the NOT circuit is that the peak current of D_1 is slightly higher, yielding a third stable intersection. In this circuit, if no inputs are applied, the stable state is indicated by point A, which represents a low output current and hence a low output voltage. If either one of the two inputs is at a high level, sufficient signal current flows into the circuit to cause the operating point to shift to point B, yielding a high output voltage. The circuit constants are adjusted so that both inputs must be high in order to shift the operating point to point C, where the output voltage is again low.

Many other threshold logic circuits can be devised to perform particular functions; however, those which have been described demonstrate the principles involved and illustrate the flexibility of this approach to logic circuit design. All of the circuits which have been described are receptive to input signals at any time while the power supply is turned on. Therefore, in many cases it is possible to cascade several levels of gating in one power supply phase. Precautions must be taken, however, to prevent any possible erroneous operation due to backward information flow. Either conventional rectifying diodes or other nonlinear coupling elements can be used for this purpose.

A second class of tunnel-diode logic circuits will be referred to as "locking" circuits. A locking circuit is also a threshold device, but instead of responding to an input signal at any time, it is receptive to an input signal only during the rising portion of the power-supply waveform. It then locks into one or the other of its two possible stable states. One version of the locking circuit is the Goto pair (or "twin").[4] The basic operating principles of this circuit have been described in the discussion of memory circuits. When used as a logic circuit, the Goto pair performs the MAJORITY logic function. Fig. 13(a) shows an example of such a circuit. An odd number of identical resistors is connected at the junction between the two diodes. The input terminals are supplied by voltage signals from the output terminals of other Goto-pair circuits. These signals are of nearly equal magnitude, but the polarities may be either positive or negative. It is easily seen that the direction of input current flow is determined by the polarity of the majority of the input signals. Therefore, if the two tunnel diodes have identical characteristics the resultant state of the circuit is determined by the majority of the input signals.

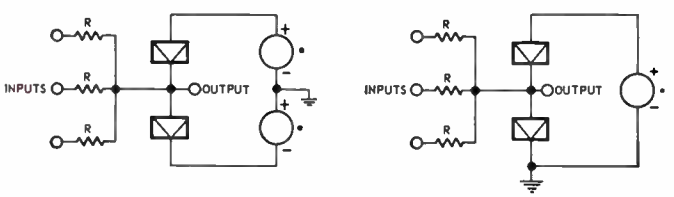

Fig. 13—(a) Goto-pair MAJORITY logic circuit. (b) Single-ended pair logic circuit.

A variation of the Goto-pair circuit is shown in Fig. 13(b). This circuit will be referred to as the single-ended pair. Lewin describes a circuit of this type which uses matched tunnel diodes.[5] Experimental work has also been performed with a circuit which used unmatched tunnel diodes. In this case, the upper diode in Fig. 13(b) is chosen to have a peak current which is slightly less than that of the lower diode. Therefore, in the absence of an input signal, the upper diode reaches its peak current first and switches to its high-voltage state. The lower diode remains in its low-voltage state, yielding an output voltage which is near ground. However, an input signal which supplies sufficient current to the junction of the two tunnel diodes can influence the switching action by causing the lower diode to reach its peak current first, resulting in a high output voltage from the circuit. In either case the circuit locks into either the low state or the high state by the time the power supply voltage has reached its maximum value. The proper choice of input resistor values and of the difference in diode peak currents will yield either an OR gate, AND gate, a MAJORITY gate, or an N-out-

of-M gate, so the circuit is quite flexible in regard to the basic logic functions which it can perform.

The locking circuits which have been described have one very desirable characteristic in that they are relatively insensitive to power supply tolerances. The most important tolerance involved is that on the difference between the peak currents of the two tunnel diodes in a pair. It is therefore possible to use diodes whose characteristics change appreciably with temperature, provided that the temperature coefficients of peak-current variation are similar in sign and magnitude for both diodes in a pair.

It is possible to employ a two-phase power supply with locking circuits if directionality is maintained by some other means. During the time that both supply phases are turned on, signals cannot propagate from a gate in one phase to a gate in the other phase because of the locking characteristic. It is therefore possible to maintain control of the distance over which information will propagate during each power supply cycle. The two-phase supply is an advantage because it simplifies supply requirements and reduces the number of circuits in recirculating storage registers. Because of the locking characteristic, however, it is not possible to cascade several locking circuits which are connected to the same power supply phase, for the first circuit in the sequence will not reach its final output voltage until after the following circuits have started to switch. Combinations of locking gates and single-diode threshold gates are useful where cascading is desirable.

Because of the extreme sensitivity of threshold AND circuits to variations in component values and signal levels, attention has been directed toward the development of alternative methods of implementing the AND function. Tunnel diodes can be employed as relatively satisfactory switches. For example, a typical germanium tunnel diode with a 1-ma peak current has a resistance in the back direction of about 15 ohms. In contrast, the resistance in the valley region is on the order of 1500 ohms. One possible AND circuit utilizing this property is shown in Fig. 14. This circuit is similar to conventional diode gating techniques in that it requires as many tunnel diodes as there are functions to be gated together.

For the two-input circuit shown, it is assumed that the input voltages can be either 0 or 0.3 volt; the output load will be neglected. If both inputs are the same, either 0 or 0.3 volt, then the output voltage will be the same as the input voltage. If the two input voltages are different, however, the output voltage will be very near to the lower input voltage. The graphical construction of Fig. 14(c) illustrates the case in which the input to D_2 remains at 0 while the input to D_1 rises to 0.3 volt. The lower curve represents the I–V characteristic of D_2. The upper curves are the I–V characteristic of D_1 constructed as load curves for several input voltages. The output voltage of the circuit for a particular input voltage is represented by the intersection of the lower

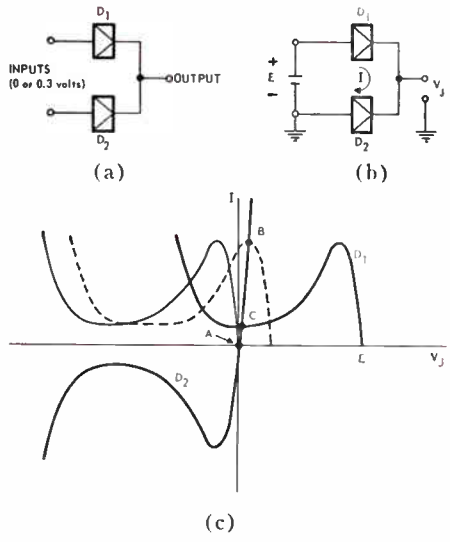

Fig. 14—(a) Tunnel-diode AND gate. (b) Current and voltage notations for graphical analysis. (c) Graphical representation of AND gate operation.

curve with the appropriate upper curve for that input voltage. Intersections A and C show that the output voltage is in fact very nearly 0 volts whether the input to D_1 is 0 or 0.3 volt.

The principal disadvantage of this AND gate is the effect of intersection B in Fig. 14(c). Momentarily, while the input signals are changing, the signal sources must accept or supply the peak current of one of the tunnel diodes. This requirement cannot readily be met by the basic threshold gate, because the acceptance of any current is likely to initiate switching to the high state. However, locking circuits are capable of supplying or accepting current. A combination of locking circuits and tunnel-diode AND gates of this type therefore appears to be feasible.

Test Results

Several of the basic approaches to tunnel-diode logic circuit design have been tested in small digital systems. A photograph of a four-stage binary counter is shown in Fig. 15. Fig. 16 shows logic and circuit diagrams of one stage of the counter. A three-phase power supply was employed, but conventional germanium diodes were also used to isolate the inputs and outputs of each circuit. These increase the power available at the output of each circuit, since current cannot flow back into the driving circuit. Observation of switching waveforms while operating the counter showed signal rise-times of about 10 nsec.

Simpler logic configurations employing the single-ended locking gate have been tested at frequencies in the 10-Mc range. Fig. 17 shows the circuit of a recirculating flip-flop. Directionality and input-output isolation are provided by conventional germanium diodes which, in conjunction with the locking characteristic of the circuits, permit the use of a two-phase power supply. Power supply and signal waveforms are shown in Fig. 18.

Conclusion

The outlook for the application of tunnel diodes in digital systems is encouraging. The high switching speed, wide environmental tolerance, and basic simplicity of the device are all desirable properties for computer applications. Presently available tunnel diodes easily lead to clock rates as high as 30 Mc in logic circuits[4] and read-write cycle times as low as 0.1 microsecond in random-access memories.[5] Clock rates of 1000 Mc and memory cycle-times of 0.01 μsec may be possible with advances in tunnel-diode technology.

Much work remains to be done in the areas of device development and circuit design. Particular attention must be given to the manufacture of tunnel diodes with uniform characteristics. There is also ample opportunity for the development of novel circuit and logic techniques. Improvements in auxiliary circuits, such as power and clock supplies, will also be required as computing rates increase.

Acknowledgment

The authors are indebted to a number of their associates at Bendix Research Laboratories for support in this work. In particular, the guidance and encouragement of Dr. E. C. Johnson are gratefully acknowledged.

Calculated Waveforms for Tunnel Diode Locked Pair*

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Summary—**An introductory analysis of the tunnel diode locked-pair circuit is presented. The characteristics of the tunnel diode, together with the simplicity of the locked-pair circuit, make it a major contender for use as a high speed computer element. High speed and high gain are the main advantages of the locked-pairs; the three-phase power supply and lack of a simple means for logical inversion are its main disadvantages. The basic circuit consists of two tunnel diodes in series, the node common to the tunnel diodes being both the input and output terminal. As a computer element, the locked-pair functions in much the same manner as the phase-locking harmonic oscillator (PLO). Like the PLO, the locked pair overcomes the difficulty of coincident input and output terminals by using a three-phase voltage source.**

The feasibility of using a digital computer to solve nonlinear circuit problems is also demonstrated. A digital computer makes possible an exact solution by doing away with relatively ineffectual linear approximation techniques. Furthermore, the stray parameters associated with laboratory work at high frequencies are excluded, thereby disclosing the true nature of the circuit.

THE PURPOSE of this paper is to present an introductory analysis of the tunnel diode locked-pair circuit. The characteristics of the tunnel diode, together with the simplicity of the locked-pair circuit, make it a major contender for use as a high-speed computer element [1], [2]. High speed and high gain are the main advantages of the locked pair; the multiphase power supply and lack of a simple means for logical inversion are the main disadvantages. The basic circuit consists of two tunnel diodes in series, the node common to the tunnel diodes being both the input and output terminal. As a computer element, the locked pair functions in much the same manner as the phase-locking harmonic oscillator (PLO). Like the PLO, the locked pair overcomes the difficulty of coincident input and output terminals by using a three-phase voltage source. However, the theory of three-phase majority logic is not essential to the understanding of this paper [3], [4].

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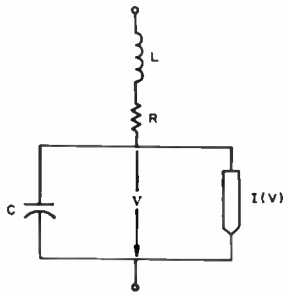
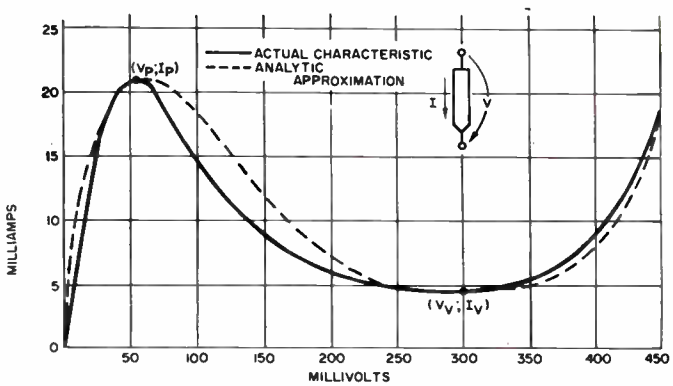
I. Basic Concepts of Locked-Pair Circuitry

The equivalent circuit of a tunnel diode is shown in Fig. 1(a), and the volt-amp characteristic of the nonlinear conductive element is shown in Fig. 1(b).

To understand the basic operation of the locked pair, examine the idealized circuit of Fig. 2, where diode inductance and capacity are neglected. Assume that tunnel diode B is the active element, and A is the load. For the moment, neglect the source resistance. Increasing the voltage E "draws" the load curve A across the characteristic of the active element B. This is analogous to what is done with tube and transistor circuits, the difference here being the nonlinear load. Fig. 3 indicates the current-voltage relationships for the circuit of Fig. 2, at a particular value of source voltage, where it is seen that the load curve A intersects the element curve B at three points. Points 1 and 3 are stable, while point 2 is unstable. The state in which the circuit locks, as the source voltage is increasing, depends on which of the two characteristics first reaches its negative conductance region. By inserting a locking current, I_L (Fig. 2), the operating point is predetermined (Fig. 4). The effect of I_L is to shift the family of operating points, causing element B to reach its negative conductance region before



(a)



(b)

Fig. 1—Tunnel diode. (a) Equivalent circuit. (b) Typical negative conductance characteristic.

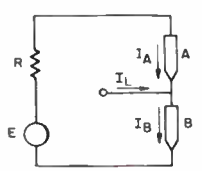


Fig. 2—Idealized locked-pair circuit (inductance and capacity neglected).

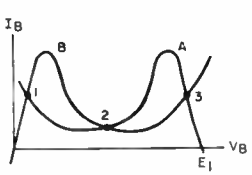


Fig. 3—Current and voltage relationships for circuit of Fig. 2 for $E=E_1$.

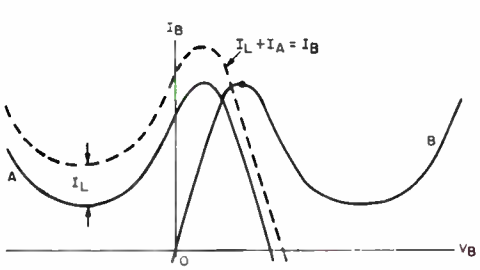


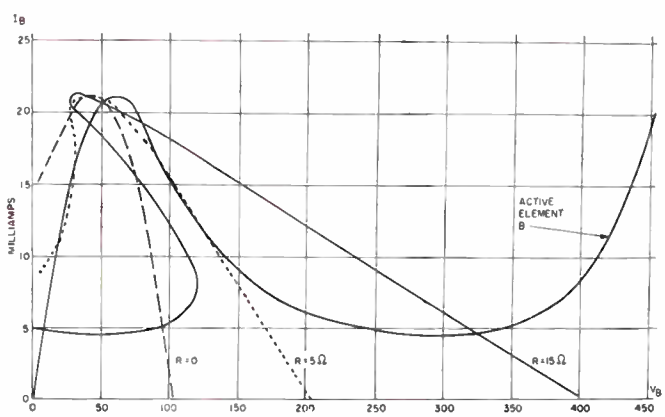
Fig. 4—Relation of characteristics near critical point of switching.

element A. Thus, diode B goes to its high voltage state. When the voltage E becomes equal to E_1, point 3 of Fig. 3 will be the operating point, so that a locking current into the node causes the circuit of Fig. 2 to have a high-voltage output. Conversely, a locking current out of the node would cause a low-voltage output (operating point 1 of Fig. 3).

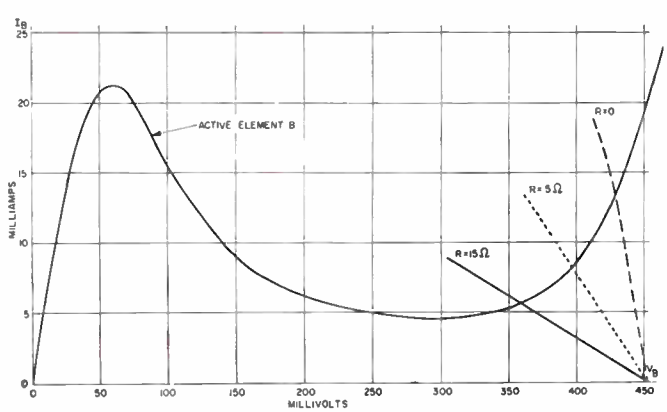
The locked pair is susceptible to a locking signal in the region where the peaks of the diode characteristic are crossing; thereafter it is relatively insensitive to spurious signals.

A significant difference in diode peak current produces the same effect as the locking current; hence, the locking current must be large enough to overcome the differences in diode characteristics.

The effect of source resistance on diode switching will now be examined. As in Fig. 2, tunnel diode B will again be considered the active element. However, the load curve now is the series combination of the source resistance R and the I-V characteristic of diode A. The source resistance affects the peak of the load curve by moving it to a higher voltage. Hence, a larger source voltage is needed to bring the characteristics to the critical point of switching, which is indicated quantitatively in Fig. 5(a). Fig. 5(b) indicates the operating



(a)



(b)

Fig. 5—Graphical interpretation of circuit in Fig. 2 for various source resistances. (a) Prior to switching. (b) After switching.

point of the circuit when the source voltage has reached an arbitrary maximum. The effects of a high source resistance are seen as a delay in switching, and a reduced output voltage.

The waveforms for the circuit of Fig. 2 can be obtained by making a point-by-point plot from the characteristics shown in Fig. 5. The current and output voltage waveforms in Fig. 6 are plotted for a sinusoidal source voltage, and a source resistance of 5 ohms.

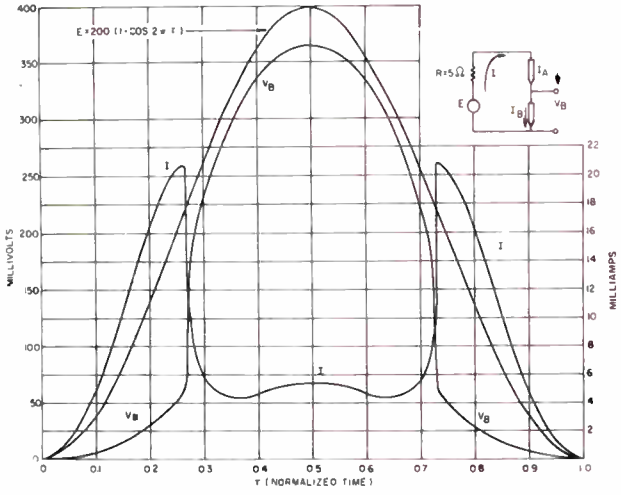


Fig. 6—Waveforms of idealized locked-pair circuit (inductance and capacity neglected).

II. Computer Solutions

The technique related above and used for Fig. 6 is invalid when the effects of capacitance and inductance are appreciable. Through use of a digital computer, a solution considering the effect of diode capacities can be easily realized. Such a computer solution excludes the stray parameters associated with laboratory work at high frequencies, thereby disclosing the basic nature of the circuit.

For the ensuing discussion a sinusoidal source voltage is assumed, because it seems to be the most practical waveform for driving a large number of locked-pair circuits.

A dc component is added to the sinusoidal source voltage to keep the diode voltage from having negative values. A negative voltage across the diode would cause an unnecessary loss of power, and if the diodes V-I characteristics are not well matched, the circuit would exhibit an undesirable output voltage during negative excursions of the driving voltage. Therefore, the source voltage will be of the following form, as plotted in Fig. 6:

$$E = K_1 - K_2 \operatorname{Cos} 2\pi \text{ ft.}$$

The values of K_1 and K_2 are somewhat arbitrary. However, the dc component K_1 must be of such a value that the minimum excursion of driving voltage is less than the peak voltage of the diode characteristic [V_p in Fig. 1(b)], otherwise the circuit will never relax. That is, the same diode will always go to its high state regardless of the polarity of the locking signal. For the problems solved on the computer, the chosen dc voltage component was equal to the peak sinusoidal value:

$$K_1 = K_2.$$

The nominal inductance of RCA germanium tunnel diodes is 0.4 nanohenry, yielding an inductive reactance of 1 ohm at 400 Mc. Thus, for the values of frequency and source resistance used in these examples, the inductance of the tunnel diode may be neglected.

RCA germanium tunnel diodes (nominal 20-ma peak current) with identical nonlinear characteristics are assumed. To facilitate computation, the programmers[1] developed an analytical expression to approximate the nonlinear characteristic. The experimental tunnel diode curve is compared with its analytic approximation in Fig. 1(b). The general analytic approximation is

$$I(V) = [A_1V + A_2V^3 + A_3V^5 + A_4V^7]e^{-V/V_P} + A_5[e^{39V} - 1],$$

where V is in volts, I is in milliamps and Vp is the voltage of peak current. The constants were evaluated on a digital computer for the tunnel diode curve in Fig. 1(b).

$$A_1 = 950.2 \qquad A_4 = 2.907 \times 10^6$$
$$A_2 = 702.6 \qquad A_5 = 3.442 \times 10^{-7}$$
$$A_3 = -1.133 \times 10^5$$

The first problem was solved for the circuit of Fig. 2 with diode capacity included. In order to keep the problem as simple as possible, no locking signal is applied; instead, the diodes switch because of the difference in capacity. In this instance, diode B always switches to its high-voltage state because it has the smaller capacity.

The defining equations derived from Fig. 2 are:

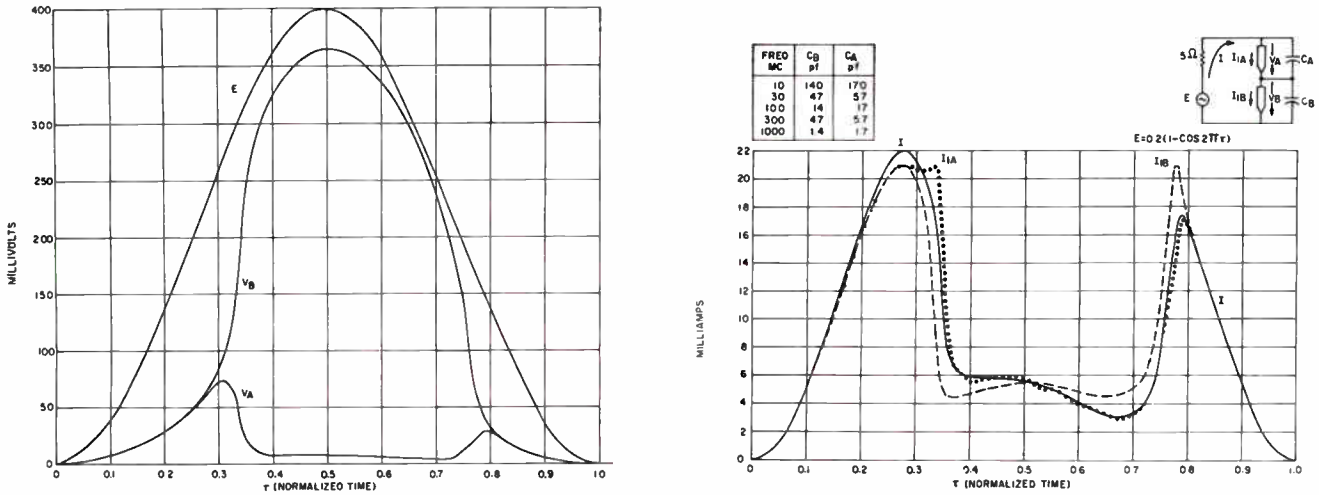
$$E = K_1 - K_2 \operatorname{Cos} 2\pi\tau = IR + V_A + V_B,$$
$$I = I_{1A} + I_{2A} = I_{1B} + I_{2B},$$
$$\frac{dV_A}{d\tau} = \frac{I_{2A}}{fC_A}, \qquad \frac{dV_B}{d\tau} = \frac{I_{2B}}{fC_B},$$

where

τ = ft, the normalized time (f = frequency in cps),
R = 5 ohms, the source resistance,
K_1 = 0.2 volt, dc component of source voltage,
K_2 = 0.2 volt, peak value of sinusoidal component of source voltage,
C_A = 170 $\mu\mu$f, capacity of tunnel diode A,
C_B = 140 $\mu\mu$f, capacity of tunnel diode B.

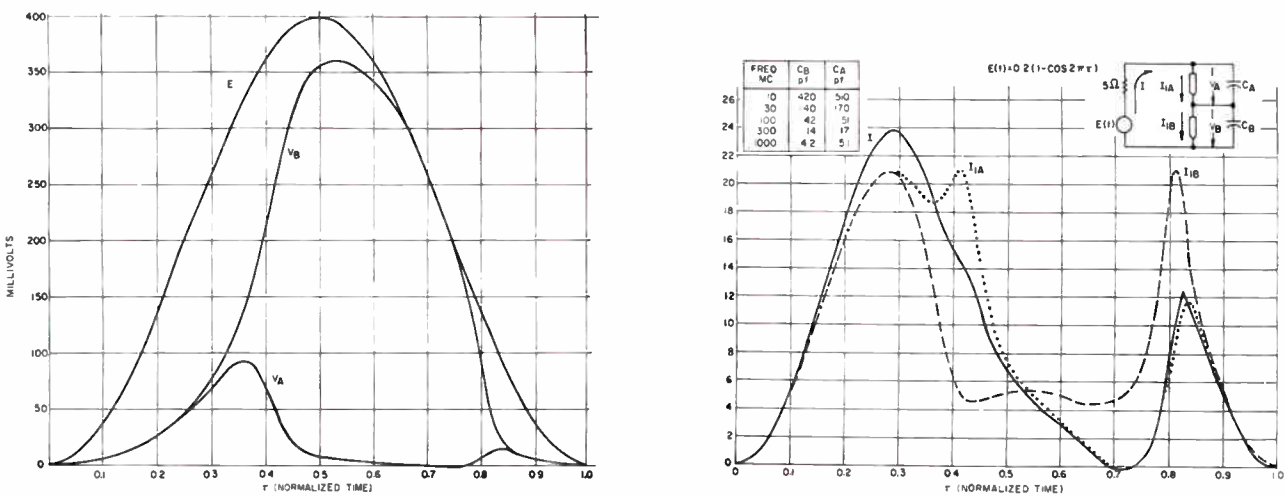
Solutions were obtained for frequencies of 10, 30, 100 and 300 Mc. The resultant voltage and current waveforms are shown in Figs. 7–10.

[1] Both computer solutions were obtained with the assistance of R. W. Klopfenstein, Dir. of Math. Services, and G. B. Herzog, RCA Labs., Princeton, N. J.



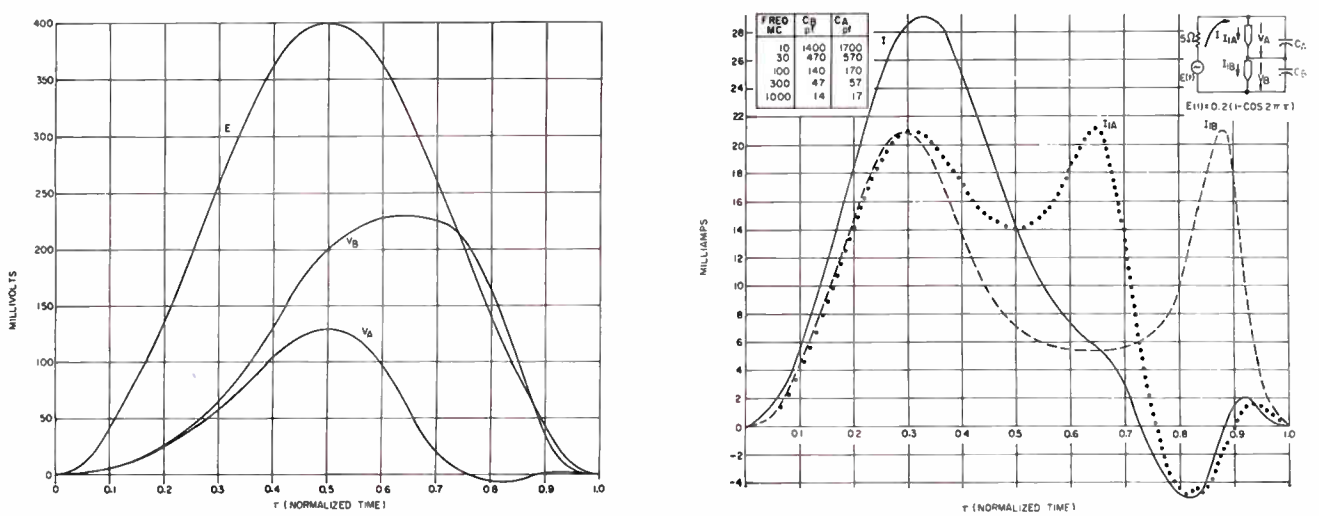
(a) (b)

Fig. 7—Tunnel diode locked-pair circuit; base frequency 10 Mc.
(a) Voltage waveforms. (b) Current waveforms.



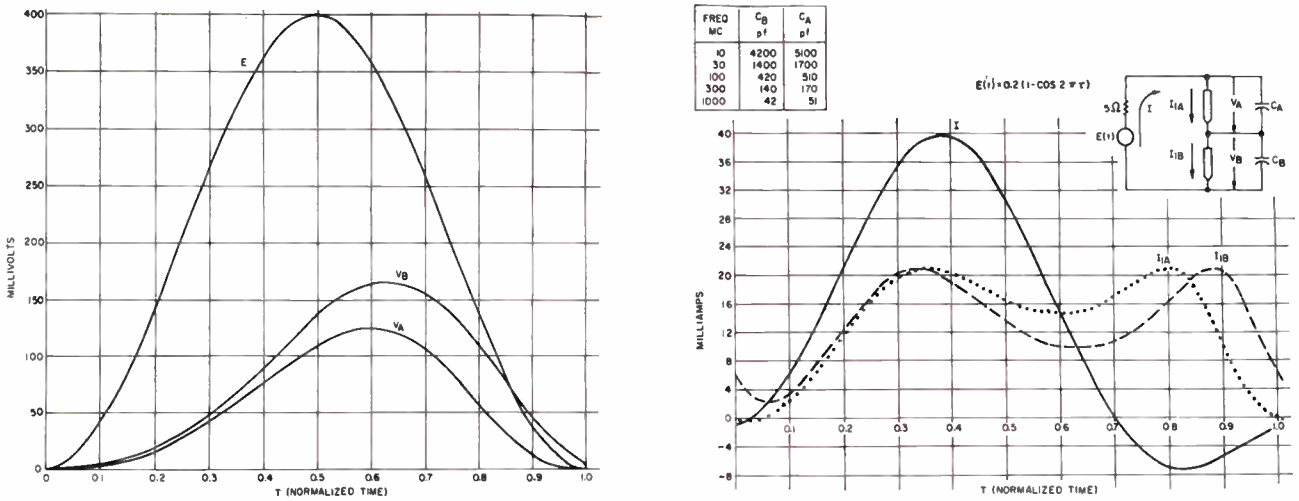
(a) (b)

Fig. 8—Tunnel diode locked-pair circuit; base frequency 30 Mc.
(a) Voltage waveform. (b) Current waveforms.



(a) (b)

Fig. 9—Tunnel diode locked-pair circuit; base frequency 100 Mc.
(a) Voltage waveforms. (b) Current waveforms.



(a) (b)

Fig. 10—Tunnel diode locked-pair circuit; base frequency 300 Mc. (a) Voltage waveforms. (b) Current waveforms.

Note that capacity and frequency appear only as a product in the defining equations of the circuit. Therefore, the waveforms can be interpolated for different values of frequency and capacity through use of

$$f_{II} = \frac{140}{C_{BII}} f_I \qquad C_{AII} = \frac{170}{140} C_{BII},$$

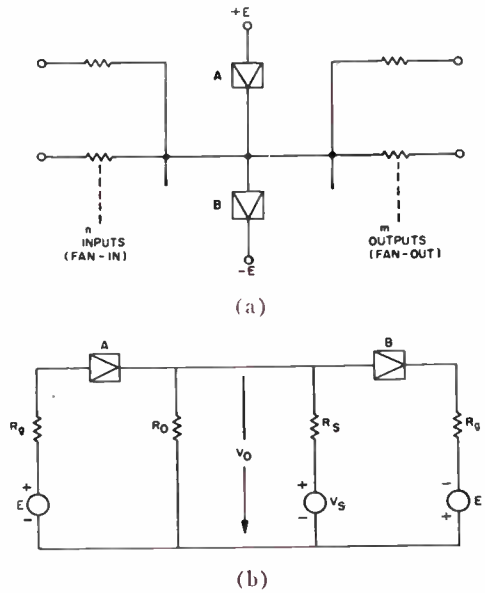
where f_I is the frequency for which the waveforms were originally calculated, and C_{AII}, C_{BII}, and f_{II} are the new values of capacity and frequency for which the waveforms are also valid.

From the voltage waveforms it is seen that switching is quite apparent at 10 and 30 Mc [Figs. 7(a) and 8(a)]. Although some switching is evident at 100 Mc [Fig. 9(a)], it is not distinct. However, at 300 Mc [Fig. 10(a)] the diode capacity effectively shunts the nonlinear element and switching does not occur. Also note that at 300 Mc the diode voltages are almost sinusoidal. Examining the waveforms of Fig. 6 which neglect capacitance effects, in conjunction with the waveforms of Figs. 7–10, the effects of capacity become more clear. From the current waveforms it is seen that as the frequency increases, the capacity retards the appearance of sharp irregularities in the curves.

III. Locked-Pair Circuit with Loading

From the previous discussion it should be noted that the two possible voltage outputs for the curves of Fig. 3 are positive. To perform majority logic, it is desirable to drive the locked-pair circuit from both ends with voltages of equal magnitude but opposite polarity. The two possible voltage outputs of the circuit will then be equal in magnitude but opposite in sign.

A typical locked-pair majority gate is shown in Fig. 11(a). The locked-pair is controlled by the majority of n inputs (n must be odd), and in turn will deliver signals to m number of locked-pair circuits. The input-output impedance of the locked-pair circuit will be neglected, since it is small in comparison with the coupling resistor. For majority rule in the worst case, all but one input current will be cancelled. Hence, the sum of the current inputs to the locked pair at a minimum is V_0/R_c, where V_0 represents the output voltage of a locked-pair circuit and R_c is the value of a coupling resistor. The equivalent circuit of the majority gate is shown in Fig. 11(b).



(a)

(b)

Fig. 11—Locked-pair majority gate. (a) Basic circuit. (b) Equivalent circuit of (a), including source resistance.

The circuit of Fig. 11 was solved on the computer for a fan-in and fan-out of six. ($m=n=3$.) As in the first problem, equal tunnel diode V-I characteristics were assumed. The defining equations of the circuit in Fig. 11(b) are:

$$E = K(1 - \text{Cos } 2\pi\tau) = I_A R_g + V_A + V_0,$$

$$E = K(1 - \text{Cos } 2\pi\tau) = I_B R_g + V_B - V_0,$$

$$V_0 = I_0 R_0 = V_s - I_s R_s,$$

$$V_s = \frac{K}{3}\left[1 - \text{Cos } 2\pi(\tau + \tfrac{1}{3})\right],$$

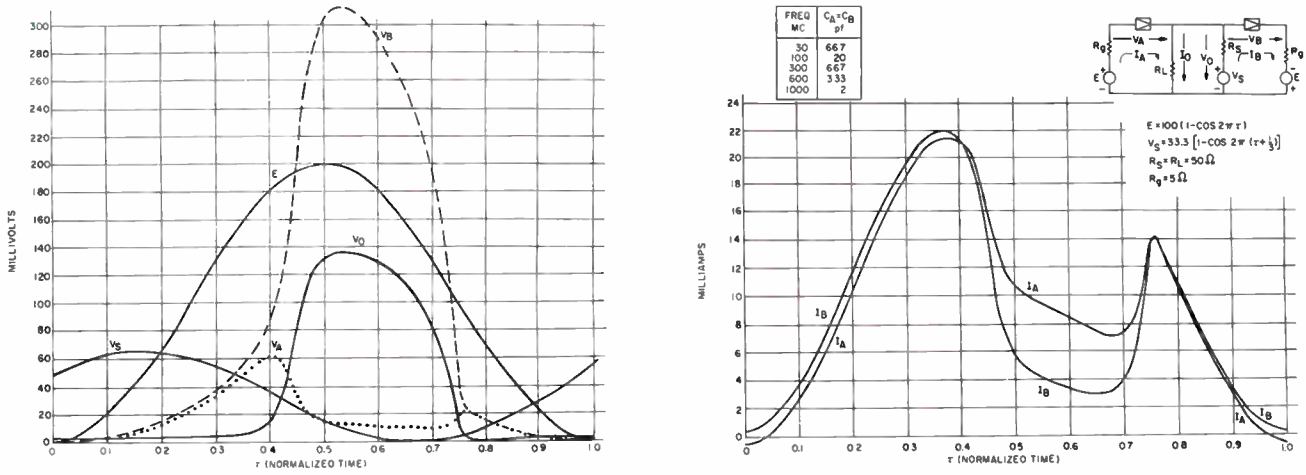
$$I_A = fC_a \frac{dV_A}{d\tau} + I_{1A}; \qquad I_B = fC_B \frac{dV_B}{d\tau} + I_{1B},$$

$$I_A + I_s = I_0 + I_B,$$

where

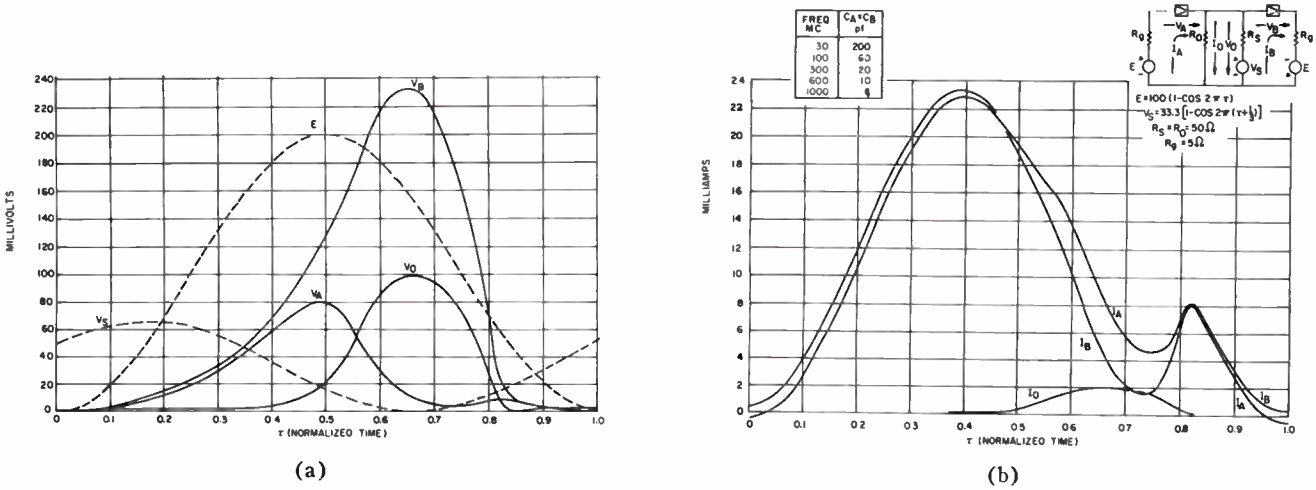
$K = 0.10$ volt,
$R_g = 5$ ohms, the source resistance,
$C_A = C_B = 20$ $\mu\mu$f,
$R_0 = R_c/m = 50$ ohms, the equivalent load or output resistance,
$R_s = R_c/n = 50$ ohms, the equivalent locking source resistance,
$V_s = E/3$, the simulated equivalent locking signal for $n = 3$,
$\tau = ft$, the normalized time.

The smaller values of capacity used indicate that the diodes will switch at higher values of frequency than those used in the first problem; therefore, frequency values of 100, 300 and 600 Mc were used in this problem. As in the first problem, capacity and frequency appear only as a product in the circuit equations; thus, the waveforms become valid for other capacity and frequency values. The simulated locking signal V_s is optimistic since it assumes the maximum output voltage of the locked-pair circuit is equal to the maximum value of the source voltage E. Also, the locking signal is assumed to lead the source voltage by 120°; however, the actual locking signal is not only a function of the switching delay induced by the source resistance R_g, but is also a function of the phase shift caused by the capacitors. This may be seen by examining the output voltage and current waveforms in Figs. 12–14.



(a) (b)

Fig. 12—Output waveforms; base frequency 100 Mc. (a) Voltage. (b) Current.



(a) (b)

Fig. 13—Output waveforms; base frequency 300 Mc. (a) Voltage. (b) Current.

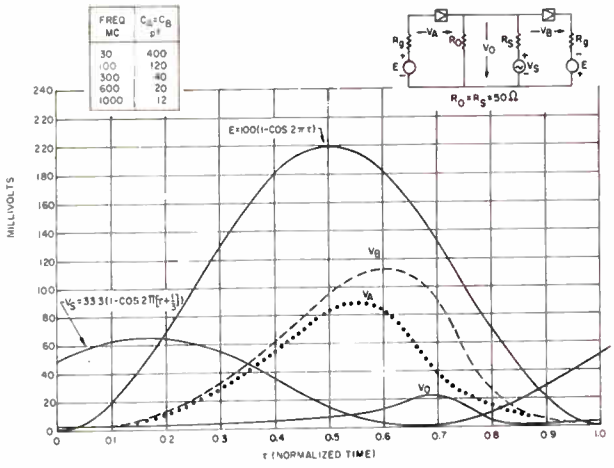


Fig. 14—Output voltage waveforms; base frequency 600 Mc.

From the figures, note that the output voltage waveforms would barely be able to control the next stage because the next stage lags by $\tau/3$. For more positive control, the output voltage waveform should be either shifted to the right 0.1τ to 0.15τ or be maintained for a longer portion of the cycle. Larger capacity would yield some positive phase shift, but only at the sacrifice of amplitude. A decrease in source resistance would increase the effective period of the output voltage; however, from practical considerations, 5 ohms is already small. One solution is to increase the source voltage. An attractive solution would be to use a larger source voltage and have it clipped.

In general, the current and voltage waveforms for this problem are what would be expected after examining the waveforms of the first problem, *i.e.*, the waveforms become "smoother" and the voltage waveform of the diode in the high state (diode B) decreases in amplitude as the frequency is increased. The output voltage at 600 Mc is almost zero. Although at 600 Mc the neglect of inductance may not be entirely valid, the waveforms indicate the restrictions placed on the circuit by diode capacity alone.

The waveforms indicate that definite switching occurs when the ratio of diode capacitive reactance, calculated at the driving frequency, to maximum negative resistance is three or greater. This can also be expressed in terms of cutoff frequency.

$$f_{co} = \frac{1}{2\pi C R_N}$$

$$\frac{X_c}{R_N} = \frac{1}{2\pi f C R_N} = \frac{f_{co}}{f},$$

where

Xc = capacitive reactance of diode capacity,
f = driving frequency,
f_{co} = cutoff frequency of tunnel diode with the equivalent series resistance of the tunnel diode negligible,
R_N = the absolute value of the tunnel diode maximum negative resistance.

Then distinctive switching occurs when

$$\frac{f_{co}}{f} \geqq 3.$$

A convenient indication of tunnel diode speed is the ratio of peak current and diode capacity. Rearranging the above expression and keeping R_N conservative, a useful indication of speed is

(maximum switching frequency in Mc)

$$= 250\left(\frac{\text{peak current in ma}}{\text{capacity in pf}}\right).$$

Using this conservative relationship, the maximum operating frequency for the diodes used in the first and second computer solutions is

$$f_{max} = 250\left(\frac{21}{155}\right) = 34 \text{ Mc/s},$$

$$f_{max} = 250\left(\frac{21}{20}\right) = 260 \text{ Mc/s},$$

respectively.

Fig. 15 shows the waveforms at 300 Mc for equal signal source and load resistors of 30 ohms. The only noticeable effect of this increased loading is to decrease slightly the output voltage. However, upon increasing the power supply resistance from 5 to 10 ohms, the diodes did not switch at all (Fig. 16).

IV. Graphical Interpretation of Loading

The effects of loading and source resistance, neglecting capacity effects, can be predicted by graphical means similar to those indicated in Section I. From the discussion of Fig. 2, when element B went to its high voltage state, element A stayed in its low voltage state. Since the voltage across nonswitching element A remains less than V_p, element A can be approximated by a resistance equal to V_p/I_p. Then the equivalent circuit that is seen by active element B can be written from Fig. 11. This Thevenin equivalent circuit is shown in Fig. 17 where

$$E_T = E + \frac{ER_L}{R_0 + R_L + r_A}, \text{ Thevenin equivalent voltage,}$$

$$R_T = \frac{(R_0 + r_A)R_L}{R_0 + r_A + R_L} + R_0, \text{ Thevenin equivalent resistance,}$$

$$r_A = \frac{V_{pA}}{I_{pA}}, \text{ linear approximation of element } A \text{ for } V_A < V_{pA},$$

$$R_L = \frac{R_s R_0}{R_s + R_0}, \text{ total loading.}$$

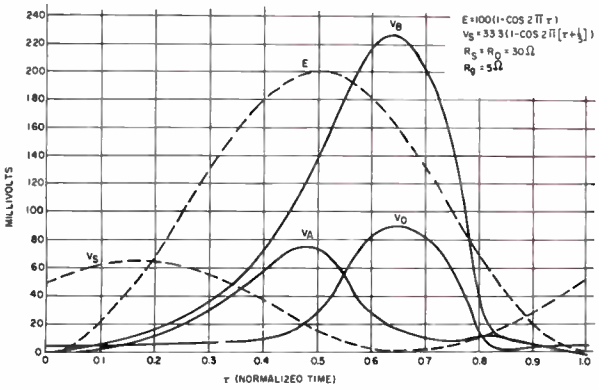


Fig. 15—Output voltage waveforms with increased loading; base frequency 300 Mc.

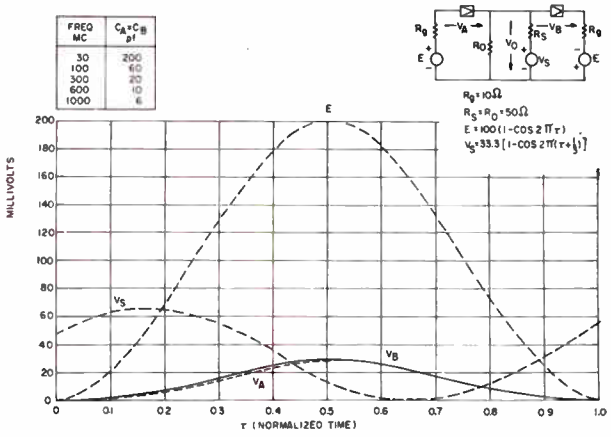


Fig. 16—Output voltage waveforms with source resistance doubled; base frequency 300 Mc.

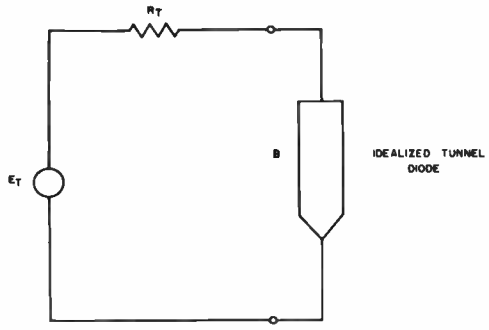


Fig. 17—Thevenin equivalent circuit of Fig. 11.

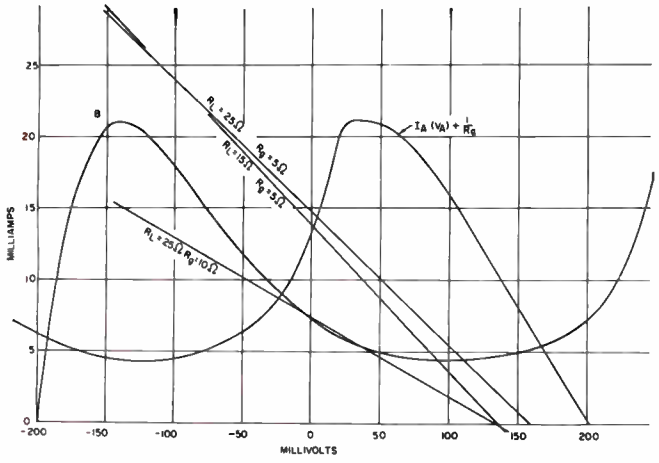


Fig. 18—Graphical interpretation of circuit in Fig. 11 using analytic approximation of tunnel diode characteristic (same parameters as used for 2nd computer solution).

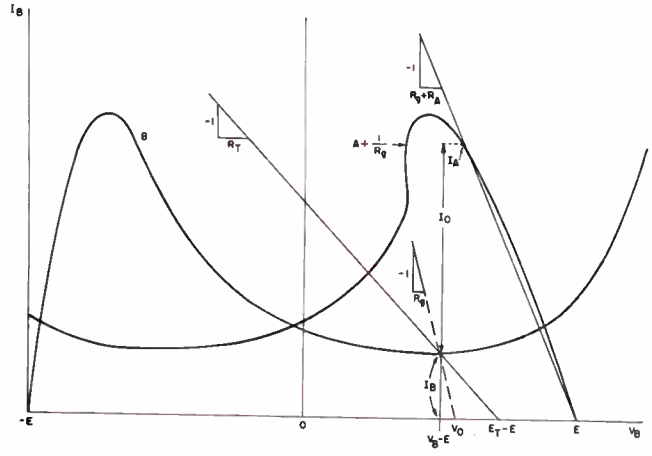


Fig. 19—Graphical interpretation of locked-pair logic gate (Fig. 11).

The current-voltage relations in this equivalent circuit are shown in Fig. 17. The intersection of the B characteristic with the load line R_T yields the voltage drop and current of the active element, B. Once these values are known, the rest of the circuit variables can be determined.

A graphical analysis was performed for the parameters used in the second computer solution. The results are plotted in Fig. 18 for the source voltage E, equal to its maximum value of 200 mv. These results predict quite accurately [to within 1 per cent for the 100 Mc computer solution, Fig. 12(a)] the maximum output voltage and the voltage across diode B. The maximum output voltage of the locked-pair circuit can be approximately determined by

$$V_0 = E_T - E - I_{VB}(R_T - R_g),$$

where I_{VB} is the valley current of the tunnel diode that is in its high voltage state, and the other parameters are as previously defined.

This equation was obtained from Fig. 19, and was based on the assumption that the current in the active element is near the valley of the V-I characteristic. This approach may be used where the diode capacitive reactance is at least ten times the magnitude of the maximum negative resistance.

From Fig. 18 it can be seen that the load line R_T changes very little when the total load resistance is decreased from 25 to 15 ohms, as was noted in the corresponding computer waveforms of Figs. 13(a) and 15. Also predicted in Fig. 18 is the fact that the diodes will not switch when the source impedance is increased from 5 to 10 ohms, as seen in the computer waveforms of Fig. 16. The criteria for diode switching, as affected by loading and source resistance, is determined from Fig. 19,

$$R_T < \frac{E_T - V_{pB}}{I_{pB}}.$$

where V_{pB} and I_{pB} are the coordinates at the point of peak current from the characteristic of the diode that is expected to go to its high state.

All the calculated results agree with the unpublished experimental data, and show that a digital computer is a powerful aid in the analysis of such complex nonlinear circuit problems.

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Magnetic Film Memory Design*

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Summary—**Thin magnetic films of permalloy have characteristics ideal for high-speed digital storage. A simple rotational model modified to include the effects of wall switching and dispersion of the preferred direction of magnetization provides a basis for describing properties of engineering interest. A selection system has been chosen which allows great latitude in film uniformity. Production of films with magnetic properties uniform to within ±10 per cent is readily achieved. Specifications for operation in a destructive mode can easily be met by existing film arrays; the nondestructive mode is considerably more stringent unless very small signals can be tolerated. The first film memory has been in reliable operation since the summer of 1959. It has 32 ten-bit words and has been operated with a minimum cycle time of 0.4 μsec.**

Higher speed and larger capacities will require higher bit densities and improved techniques to minimize undesirable coupling between drive and sense lines. The use of 10×60 mil rectangles, balanced sense windings, and longer words will hopefully permit memories of about 200,000 bits with cycle time under 0.2 μsec.

I. Introduction

SINCE 1955, when Blois[1] succeeded in preparing oriented films of permalloy there has been considerable study of their fundamental magnetic properties and their possible engineering application as digital storage elements.

The primary motivation for much of this work derives from the unique promise of films to provide extremely fast, random-access storage systems at relatively low cost, based on the following considerations:

1) The switching time of films is about 1 nanosecond (nsec) for fields of approximately 2 oersteds.[2,3]

2) The low uniaxial magnetic anisotropy permits reversible or nondestructive readout with the application of modest transverse fields. For destructive readout it allows a word selection system which permits wide latitude in film properties.

3) The preparation of extremely thin layers (by either evaporation or plating) provides low flux which reduces the voltage drive required and eliminates heating at high frequencies.

4) The simple planar substrate-supported film makes possible extremely high bit-densities and allows the use of low-impedance strip transmission lines for high-frequency pulse distribution, factors of utmost importance in determining the compatibility of high speed and large capacity.

5) Film preparation permits the fabrication, handling, and testing of entire arrays rather than individual components.

6) The open-flux structure eliminates the need for threading holes and permits the use of evaporated or etched wire techniques.

Having stated the considerations which have stimulated the study of films for storage, a more detailed outline of their properties and a discussion of the practical engineering problems are given below. This is followed by a description of the first operating magnetic film memory and a brief estimate of future approaches and goals.

II. Film Physics

Permalloy films are normally prepared by either vacuum deposition or by electroplating in a magnetic field. The resultant film exhibits a uniaxial magnetic anisotropy, *i.e.*, develops a preferred or easy axis.[1] If an anisotropy energy $K \sin^2 \theta$ is assumed, where θ is the angle the magnetization makes with the easy axis, torque and energy calculations give the ideal static and dynamic magnetization characteristics.[4,5] For combinations of applied transverse and longitudinal fields, Fig. 1 gives the family of curves of equilibrium angle be-

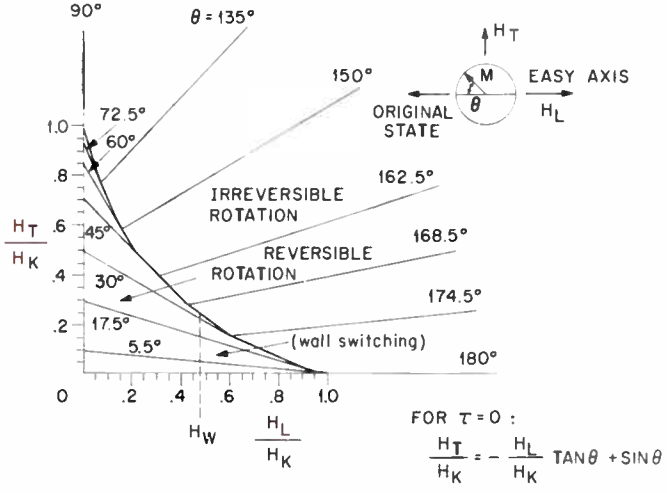

Fig. 1—Equilibrium angle of magnetization vector for applied transverse and longitudinal fields.

* Received by the IRE, August 2, 1960.

† Mass. Inst. of Tech. Lincoln Lab., Lexington, Mass.

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[4] D. O. Smith, "The static and dynamic behavior of thin permalloy films," *J. Appl. Phys.* vol. 29, pp. 264–273; March, 1958.

[5] C. D. Olson and A. V. Pohm, "Flux reversal in thin films of 82% Ni, 18% Fe," *J. Appl. Phys.*, vol. 29, pp. 274–282; March, 1958.

tween the magnetization vector and the original easy-axis direction. Equilibrium occurs when the torque τ, due to the applied fields, is zero. Values of θ less than 90° correspond to reversible rotation, values greater than 90°, irreversible rotation. These plots assume a coherent rotation of the magnetization throughout the film, *i.e.*, all the spins are aligned and rotate simultaneously. The threshold curve marking the boundary between reversible and irreversible rotation is also shown in Fig. 1 and contains almost all the information necessary for describing the various selection systems (*i.e.*, multicoordinate drive-field combinations) which may be used to read and write information in a single film element in an array. From these curves it is easily shown that a plot of transverse flux ϕ_T vs transverse field H_T (the transverse loop) will be linear up to H_k, where saturation occurs. The longitudinal loop (longitudinal flux ϕ_L vs longitudinal field H_L) is square with a threshold which corresponds to H_k. These loops are shown in Fig. 2(a).

So far an ideal uniaxial anisotropy has been assumed and the rotational threshold curves are derived directly from this model. Experimental hysteresis loops are contrasted with those predicted by theory in Fig. 2. The knee of the longitudinal loop H_w may be considerably below H_k. This occurs because the longitudinal loop is not a rotational loop as expected, but rather the result of domain-wall switching (*i.e.*, a sequential piecewise switching of small areas of material) similar to that occurring in bulk toroids. This process is inherently slower than rotation and provides an undesirable method for changing information.

To a first order, the values of H_k and H_w will specify the operating currents. The fields needed for rotational switching vary directly with H_k while the maximum longitudinal field which can be applied without causing wall motion is H_w.

Another departure from the model is that the transverse loop opens slightly at high fields and in some cases may be almost square, suggesting a poorly defined easy axis. Experimentally it is found that films do exhibit an apparent dispersion of the easy axis.[6,7] Fig. 3 indicates how angular dispersion may be measured.

In interpreting this measurement it is convenient to assume that each individual crystallite or other basic unit of unidirectional anisotropy, whatever its scale, switches independently of neighboring regions according to the rotational model. The first step in making the measurement is to align the film in a hysteresigraph as shown in Fig. 3(a) with $H_L=0$. An ac transverse field greater than H_k will cause the magnetic vector of those regions with their hard axes in quadrants II and IV to rotate in a counter-clockwise direction. For those re-

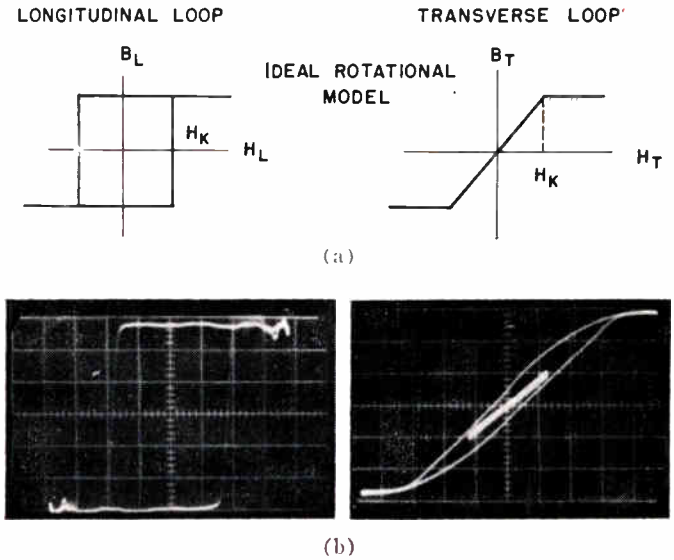


Fig. 2—(a) Ideal magnetic-film *B-H* loops for rotational model; (b) experimental *B-H* loops.

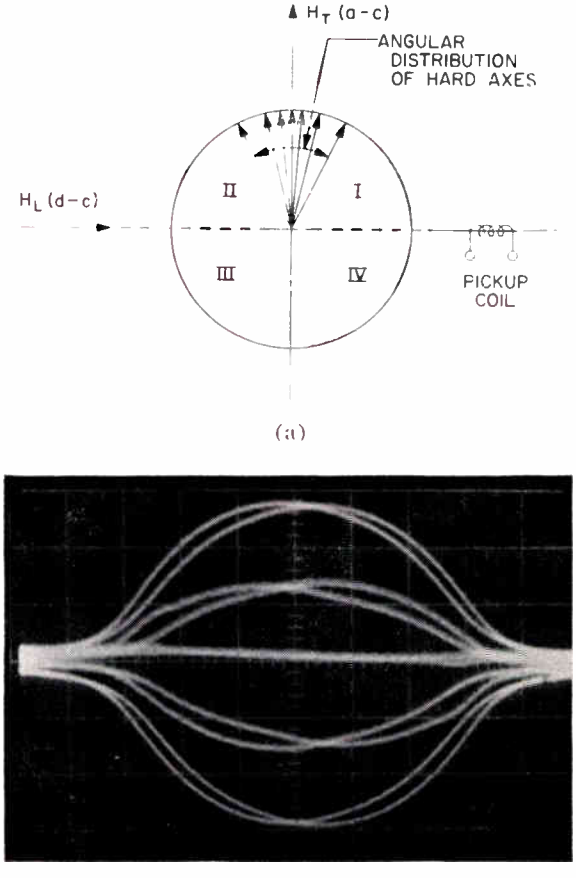


Fig. 3—(a) Experimental technique; diagram for easy-axis dispersion measurement. (b) *B-H* loops of longitudinal flux as a function of transverse field for longitudinal dc field values of +0.35, +0.14, 0, −0.14, and −0.35 oersted, reading from top to bottom.

[6] R. G. Alexander, "Anisotropy field measurements on Ni-Fe thin films," *J. Appl. Phys.* vol. 30, pp. 266S–367S; April, 1959.

[7] T. S. Crowther, "Angular Dispersion of the Easy Axis of Thin Ferro-Magnetic Films," M.I.T. Lincoln Lab. Group Rept. 51-2; February 24, 1959; revised March 30, 1960.

gions with their hard axes in quadrants I and III [Fig. 3(a)], rotation will be clockwise. When the two rotating components are equal, $\phi_L = 0$, and a null is obtained. For zero dispersion, the application of an infinitesimal positive H_L dc field will cause the magnetization of the entire film to oscillate back and forth only in quadrants I and IV. For finite dispersion the field required to keep all of the flux in quadrants I and IV can be used to calculate the dispersion. For a single region with skew α the dc field required will be given by

$$H_L = H_k \sin \alpha.$$

That is, the dc field must be larger than the longitudinal component of the ac field when it has the value H_k.

In addition, it is often found that there is a gross skew of the easy axis upon which the dispersion is superposed. The consequences of both effects is an equivalent rotation of the threshold curve (Fig. 4), which will vary for different regions of material. Therefore, small sections will tend to switch somewhat below the threshold curve as plotted for the nominal easy axis. This causes incoherent rotation and reduces the maximum allowable field for reversible switching which is of great importance for nondestructive readout.

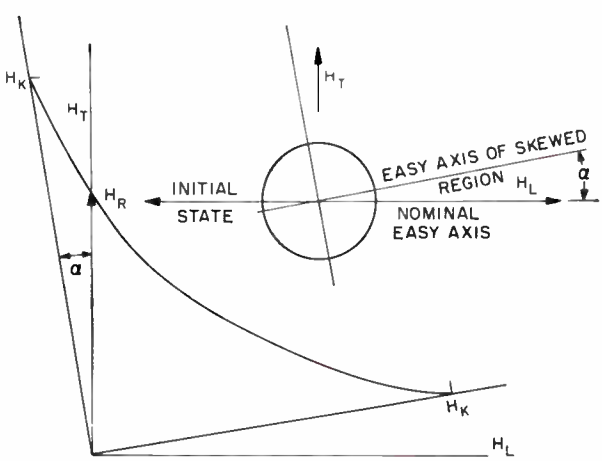


Fig. 4—Limit of transverse field H_R, for reversible rotation of a film with skew of easy axis α.

III. Film Preparation

Evaporation

There are several parameters which are of first-order magnetic significance in preparing films by evaporation.

Angle of Incidence: By inclining the substrate at large angles to the incident vapor beam it is possible to produce films whose easy axes are perpendicular to the incident beam and have anisotropy values of hundreds of oersteds. This is thought to be produced by oriented voids resulting from self-shadowing.[8] The incident vapor beam should be maintained normal to the surface in order to prevent skewing of the easy axis due to oblique incidence. For a small source such as a crucible this means delimiting the substrate area and keeping the source as far from the substrate as is practical. In practice, one square, 1.6 inches × 1.6 inches, is evaporated at a time, at a distance of about 12 inches.

Composition: Both H_k and magnetostriction are known to vary with composition.[9] For all practical purposes the zero-magnetostrictive composition, 81 per cent Ni-19 per cent Fe, is the most desirable because it eliminates most of the skew problem due to stresses, while providing low H_k and low dispersion. It should be pointed out, however, that films are compositionally inhomogeneous with random local variations of at least 1 to 2 per cent common in almost all films.[10] The extent to which this influences dispersion is not clear but it means that any measurement of magnetostriction represents an average value only.

Thickness: Wall coercive force for an infinite planar film is found to vary inversely with thickness according to $H_w = t^{-n}$ where n usually varies between 1/2 and 3/2 depending upon the substrate surface and method of film preparation.[11,12]

Spot Shape: Spots may be formed by evaporation through a mask or by etching from a continuous film using standard photoresist techniques.

The lower limit for spot size and the upper limit for thickness are imposed by the self-demagnetizing field resulting from free poles at the film edges. The demagnetizing field is proportional to thickness and inversely proportional to spot diameter. At the center of a circular spot it is given approximately by

$$H_D \approx 1/32 \text{ oersted} \times \frac{\text{thickness (in thousands of angstroms)}}{\text{diameter(in inches)}}.$$

H_D must be small compared to H_w to prevent reverse domains from forming with resultant loss of information. For a 1/16-inch diameter spot 1000 Å thick, this gives a demagnetizing field of $\frac{1}{2}$ oersted, a value perhaps $\frac{1}{2}$ to $\frac{1}{4}$ the typical wall-coercive force. For asymmetrical shapes such as rectangles, the contribution to H_k because of shape anisotropy must be taken into account. This will again increase with demagnetizing field and hence depend upon thickness.

Dispersion is found to increase with decreasing spot

[8] D. O. Smith, M. S. Cohen, and G. P. Weiss, "Oblique-incidence anisotropy in evaporated permalloy films," *J. Appl. Phys.*, vol. 31, pp. 1755–1762; October, 1960.

[9] D. O. Smith, "Anisotropy in permalloy films," *J. Appl. Phys.*, vol. 30, pp. 264S–265S; April, 1959.

[10] W. W. L. Chu, J. E. Wolfe, and B. C. Wagner, "Some observations on evaporated permalloy films," *J. Appl. Phys.*, vol. 30, pp. 272S–273S; April, 1959.

[11] K. H. Behrndt and F. S. Maddocks, "Influence of substrate processing on the magnetic properties and reproducibility of evaporated nickel-iron films," *J. Appl. Phys.*, vol. 30, pp. 276S–277S; April, 1959.

[12] I. W. Wolf, H. W. Katz and A. E. Brain, "Magnetic Properties of Electrodeposited Thin Films," presented at the Electronic Components Conf., Philadelphia, Pa.; May 6–8, 1959. This work was done at the G.E. Co., Syracuse, N. Y., under a subcontract from M.I.T. Lincoln Lab.

size, probably due to the influence of the demagnetizing field and edge domains.

Substrate Surface: In order to produce films which are well oriented it is necessary to deposit upon a locally smooth surface such as fire-polished glass or mica. The presence of oil stains, fingerprints, and other contamination leads to poor reproducibility, especially in H_w. To provide a uniform surface the substrate is normally cleaned ultrasonically, placed in the bell jar and a layer of SiO evaporated just prior to the permalloy.

Substrate Temperature: The usual practice is to heat the substrate to about 400°C before and during deposition. This tends to drive gases from the substrate and provides an anneal which generally results in substantially lower H_k values than for films made at room temperature.

Rate of Deposition: For evaporated films the rate of deposition has a direct effect on film structure and, in general, higher evaporation rates produce more uniform films.

Pressure: The exact effect of residual gases in the vacuum system is not entirely understood, but the presence of oxygen in various amounts is known to play a considerable role in determining magnetic characteristics of bulk materials.[13] Evaporation at conventional pressures of 10^{-5} mm Hg yields satisfactory films for most purposes. The improvements to be obtained from operation at ultrahigh vacuum remain to be determined.

Electroplating

Electrodeposited permalloy films comparable in magnetic properties to evaporated films have been prepared by Wolf, *et al.*[12] These films are plated on a coating of sputtered gold which must be kept quite thin (about 100 Å) in order to obtain well-defined anisotropy. In addition, control of sputtering voltage and plating-current density are very important. Voltages of 2 kv and current densities of 3 ma/cm² are typical.

The high resistance of the thin gold layer can lead to severe thickness gradients in the permalloy, because of the voltage drop from the electrode clip to the bottom of the slide. The substrate is usually reversed during the run and clipped at the other edge to average out any gradients.

In general, plated films seem to be somewhat higher in H_k than the best evaporated films, but there is much less variation in H_k with composition. Values of 3–4 oersteds are most common as compared to approximately 2 oersteds for evaporated films. In general, reproducibility seems to be somewhat better for plated films, especially from run to run, although the difference is not large.

[13] R. H. Heidenreich and F. W. Reynolds, "Uniaxial magnetic anisotropy and microstructure of ferromagnetic metal films," in "Structure and Properties of Thin Films," C. A. Neugebauer, J. B. Newkirk, and D. A. Vermilyea, Eds., John Wiley and Sons, Inc., New York, N. Y., pp. 402–409; 1959.

IV. Engineering Design

Selection Systems

The most important parameter in the design of a film memory is the choice of selection system, since this will determine the requirements for film uniformity, the location in time and space of pulse transients which may mask the signal, the requirements of peripheral circuitry, and the arrangement of signal and drive lines.

A number of selection systems have been proposed which have varied widely in effectiveness.[14–16] The one which will be described was employed in the design of the TX-2 memory at the M.I.T. Lincoln Laboratory.[15] With occasional variations[17,18] it seems, at the present time, to be generally accepted as the most desirable by workers in the field.

The memory is word-organized with word-lines supplying a field in the transverse direction sufficient to rotate the magnetization 90°. A current pulse of either polarity on the digit line supplies a field along the easy axis which will cause the magnetization to fall to the ONE or ZERO direction upon the termination of the transverse pulse. Readout occurs on the rise of the transverse pulse. The digit pulse starts at the middle of, and ends after the completion of, the transverse pulse. In the TX-2 memory a slightly different mode is used in order to eliminate the need for both a ONE and ZERO digit driver. A dc current in the ZERO direction flows continuously and a ONE pulse twice as large overrides the dc for writing ONE's. The only difference between the two modes is that the ONE and ZERO signals are equal but opposite in polarity for the first, while in the second the dc bias during read time increases the ONE and decreases the ZERO signal. The pulse sequences for both modes are shown in Fig. 5.

To provide nondestructive readout in the first mode of this system, it is only necessary that the transverse-read pulse be sufficiently below H_k to stay within the limits of rotational reversibility. For writing, the large transverse is used as above. The amount of reversible rotation which can be obtained will determine the amplitude of the signal. In general, the signal will be decreased by a factor of 2 to 5 from the destructive case. Note that unlike most nondestructive readout memory systems there is no need to clear before writing. Also, the same word equipment may be shared for nondestructive reading and for writing since there is only a difference in pulse height between the two.

Additional advantages of this selection system are

[14] A. V. Pohm and S. M. Rubens, "A compact coincident-current memory," *Proc. EJCC*, pp. 120–124; December, 1959.

[15] J. I. Raffel, "Operating characteristics of a thin film memory," *J. Appl. Phys.*, vol. 30, pp. 608–618; April, 1959.

[16] E. E. Bittman, "Using thin films in high-speed memories," *Electronics*, vol. 32, pp. 55–57; June, 1959.

[17] Remington Rand UNIVAC, Proj. Lightning, Second Phase, First Quarter Rept., NObsr, pp. 45–47; February 28, 1959.

[18] E. M. Bradley, "Making reproducible magnetic-film memories," *Electronics*, vol. 33, pp. 78–81; September, 1960.

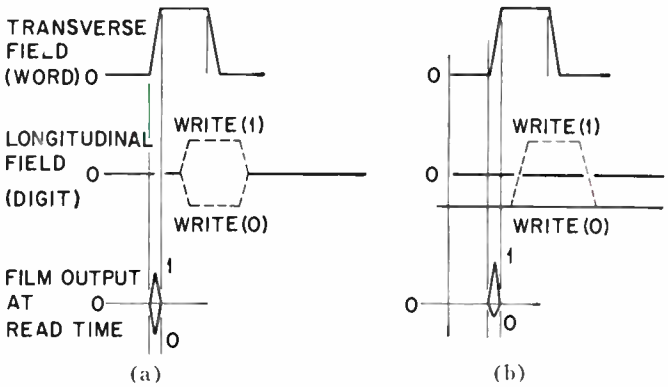


Fig. 5—Pulse sequences for two modes of destructive readout memory operation. (a) Mode using pulsed write zero; (b) mode using dc read and write zero.

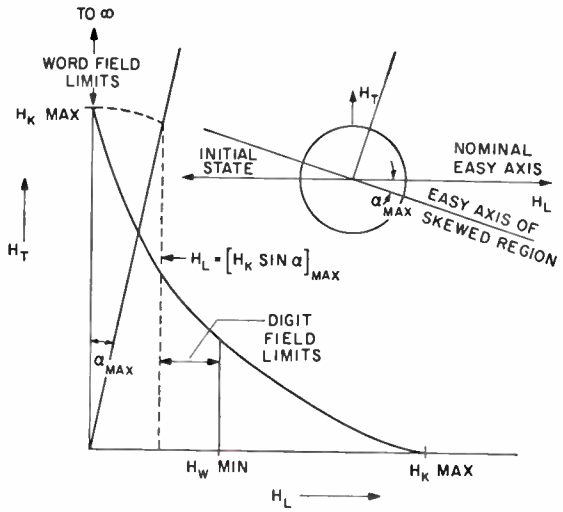


Fig. 6—Drive-current operating loci for variation of H_w, H_k, and α.

1) Only a unidirectional pulse is required on the word line.
2) The difference in polarity between ONE's and ZERO's means that the effect of variations in film output is reduced.
3) The word line is orthogonal to the sense line, resulting in low capacitive and inductive coupling at signal time.
4) All drive windings may be straight lines, thus providing simple fabrication and good transmission characteristics.
5) Wide variation in film characteristics can be tolerated.

Film Specifications

General conclusions about the film uniformity problem may be extremely misleading unless they are based upon the constraints imposed by the selection system which is used.

Fig. 6 shows the operating locus for H_L and H_T with variations in H_w, H_k, and skew angle α. For the destructive system described above, the following conditions have to be met assuming H_k, H_w, and α all vary:

$$H_T > H_{k\,\max}$$

$$H_L > [H_k \sin \alpha]_{\max}$$

$$H_L < H_{w\,\min}.$$

The transverse field must be larger than the maximum value of H_k and the longitudinal field must be less than the minimum wall coercive force but greater than the maximum effective longitudinal field produced by the nominally transverse word current.

For the nondestructive system, the above conditions hold for writing with the added proviso that for reading

$$H_T < H_{R\,\min}$$

(where H_R is shown in Fig. 4 for a single region). The nominally transverse field, then, must be smaller than the lowest reversible limit field, $H_{R\,\min}$, over the entire film.

Testing

Magnetic film characteristics are conveniently measured with a hysteresigraph and a pulse tester. Low-frequency (1000~) composite characteristics of arrays of spots are measured with the hysteresigraph. Two pairs of Helmholtz coils can be used to generate mutually perpendicular drive fields. The substrate is held below one sense coil and may be rotated in its plane. A second coil connected in opposition to the sense coil provides cancellation of air-flux coupling. The integrated signal is displayed on the Y axis of an oscilloscope while the X-axis displacement is proportional to the amplitude of the drive field. Figs. 2(b) and 3(b) are displays from the hysteresigraph. In order to achieve high sensitivity a number of noise-bucking methods must be employed and careful integrator design is required.[19,20]

The pulse tester is used to measure characteristics of spots within an array under pulse-switching conditions.[21] In order to insure identical conditions for all spots and to minimize the equipment required, the pulse tester uses only one set of drive and sense circuitry. A mechanical manipulator indexes the array under a set of crossed drive lines and a sense coil.

Three pulse tests are given to every element in each array. The first is a measurement of the ONE amplitude for the normal destructive read memory cycle. This test is performed twice, the second time with read and write polarities interchanged. A difference be-

[19] E. C Crittenden, Jr., A. A. Hudimac, and R. I. Strough, "Magnetization hysteresis loop tracer for long specimens of extremely small cross section," *Rev. Sci. Instr.*, vol. 22, pp. 872–877; December, 1951.

[20] D. D. Strassberg, "An Audio-Frequency Hysteresigraph for Thin Magnetic Films," M.I.T. Lincoln Lab. Group Rept. 51-10; October 16, 1959.

[21] A. H. Anderson and T. S. Crowther, "Techniques for Pulse Testing Magnetic Film Memory Elements," M.I.T. Lincoln Lab. Group Rept. 51-11; January 29, 1960.

tween ONE amplitudes for the two digit polarities indicates skew of the easy axis. If both ONE amplitudes are low, the reason may be high H_k, or read-disturbing (*i.e.*, the longitudinal field exceeding the wall-coercive force). A second pulse sequence determines whether or not read-disturbing is the cause of any low outputs. The final test checks the film for operation in the nondestructive read mode.

Film Uniformity

For both evaporated and electroplated[22] films, the variation of H_k and H_w from array to array is typically about 10 per cent. A group of twenty evaporated 16×16 arrays were selected for pulse testing after meeting hysteresigraph measurement specifications of $H_w \geq 1.0$ oersted and $H_k \leq 4.0$ oersteds. A digit field of 0.67 oersted was chosen which fixes the maximum allowable skew to less than 10°. An acceptable array was defined as one in which all the elements had a ONE output of 1 mv under normal memory-operating conditions. Of these twenty arrays, only four had any elements which failed to meet specifications for reasons other than faulty etching. These four imperfect films all failed for the same reason—excessive skew. Data on plated films show about the same results. Yields for nondestructive memory operation are much lower. Only two of the twenty evaporated arrays had elements which could all be read reversibly for transverse fields of $\frac{2}{3}$ H_k. This value of drive results in an output about one third that for a drive field greater than H_k.

The TX-2 Thin Film Memory

The first film memory, shown in Fig. 7, has been in operation in the control element of the TX-2 computer since the summer of 1959. It has 32 ten-bit words and uses destructive readout. Its operating speed in the machine is 0.8 μsec and it has been bench-tested at a 0.4 μsec cycle time. The memory uses two 16×16 arrays of circular spots $\frac{1}{16}$ inch in diameter and about 700 Å thick. Conventional round magnet wire is cemented to plastic boards to form the wiring mats which sandwich the film, forming closed loops for low impedance and minimum crosstalk. The word and digit lines each have two series turns, while the sense winding is a single turn crossed over in the center of the array for cancellation of coupling to the parallel digit line. Driving currents are 250 ma on the word line and 200 ma on the digit line (superposed on a negative bias of 100 ma). Input and output circuits are shown in Fig. 8. The current driver which supplies a 250-ma pulse with a rise time of 20 nsec is used for both the digit lines and a two-coordinate ferrite-core switch matrix. The switch matrix supplies current pulses to the word lines which are terminated in

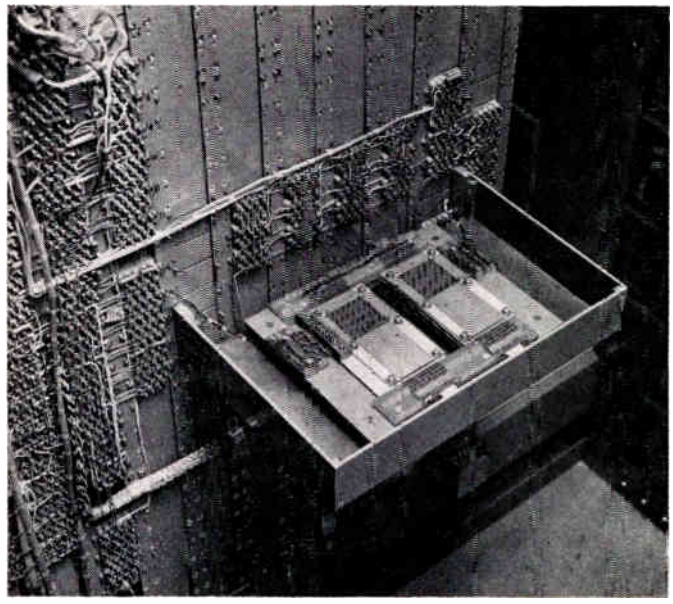
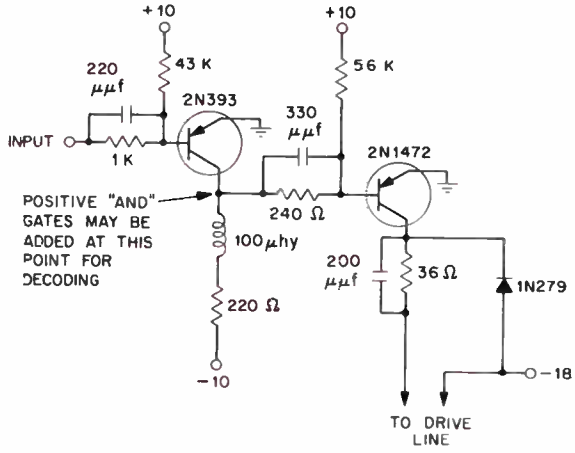
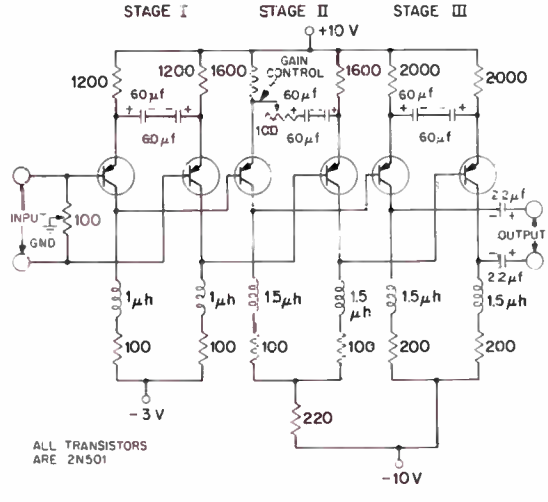


Fig. 7—Magnetic film memory in the TX-2 computer at the M.I.T. Lincoln Laboratory.



(a)



(b)

Fig. 8—(a) TX-2 film-memory driver; (b) TX-2 film-memory sense-amplifier.

[22] J. W. Wolf and T. S. Crowther, "Reproducibility of Electrodeposited Thin Film Memory Arrays," presented at the Electronic Components Conf., Washington, D. C.; May 10–12, 1960.

diodes for suppression of the core recovery pulse and half-select switch-core outputs. The three-stage differential sense amplifier has a voltage gain of 1000 and a rise time of 50 nsec.

V. Discussion

General Considerations

The combination of latitude in film requirements and improvements in film characteristics have reduced the uniformity problem to secondary importance for the destructive readout memory. While improvements in characteristics will always be welcome, they are not a crucial issue. However, for the nondestructive memory any increase in reversible limit and reduction of skew is extremely important.

Probably the most important engineering problem is to achieve the optimum combination of capacity and speed attainable (for a single memory) within the limitations imposed by transmission delays, crosstalk, and transistor-circuit bandwidth. Of course, it is always possible to utilize a multitude of small memories and thus obviate the need for large arrays in which problems arising from high speed are intensified. Economic considerations, however, require that the number of bits sharing common drive and sense circuitry be high.

Drive and Sense Configurations

There are two fundamental sources of noise in the form of crosstalk. A transient induced in the sense winding due to coupling to the digit winding to which it is parallel occurs during writing. This prevents squeezing the cycle time because of interference with the next readout. The crossover of the sense winding is intended to minimize the effect, but for long lines and very high bandwidth, cancellation is poor and considerable noise results. The second source of noise is due to capacitive coupling between the transverse line and sense or digit windings. This results in charging currents which induce spurious voltages in the sense winding during read time which can mask the signal.

The choice of a sense-digit winding combination which is balanced to ground and completely symmetrical with respect to all coupling is essential at very high frequencies. Two such configurations are shown in Fig. 9. The planar sense suffers the disadvantage that its impedance is relatively high and it requires an extra layer of fine wiring. The bridge circuit, on the other hand, requires that current be fed into the dummy line, thus doubling the digit current required.

One measure of the efficiency of any sense-digit combination is the degree of coupling between the film and windings. This will vary with the spacing between conductors and is limited by the thickness of the film substrate. A rough quantitative measure of the efficiency of the coupling is the ratio of signal current I_S to digit current I_D. (This is the reciprocal of the current gain required in the digit-sense channel for destructive readout operation.)

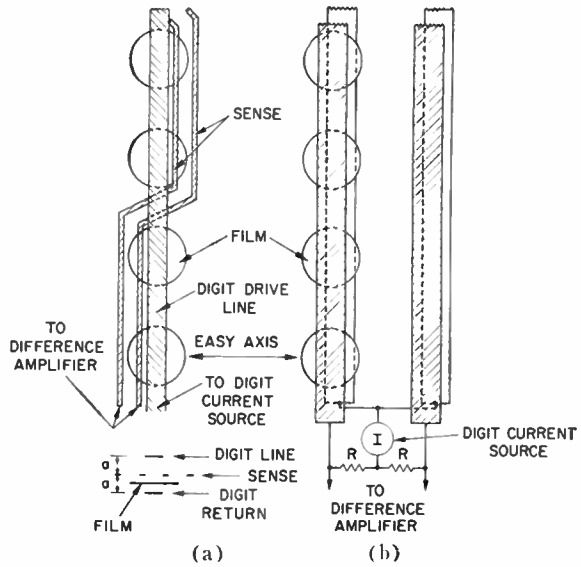


Fig. 9—(a) A balanced planar-sense line; (b) combined digit-sense line bridge circuit.

$$\frac{I_S}{I_D} = \frac{V_S/Z_0}{I_D}.$$

This ratio will increase as switching speed increases, and as Z_0 (or line separation) decreases, producing higher output voltage V_S. At present this ratio is of the order of

$$\frac{1 \text{ mv}/100 \text{ ohms}}{1 \text{ ampere-turn}} \approx 10^{-5}.$$

For 10-nsec switching and 1-ohm impedance level this would be increased to 10^{-2}. Perfect coupling (efficiency of 1) is not desirable either, because this would imply ideal transformer action which would result in heavy loading on the film. Probably somewhere between 10^{-1} and 10^{-2} would be an upper limit providing a range of three orders of magnitude of possible improvement which requires considerable exploration. As the line impedance is lowered it becomes necessary to take advantage of the lower impedance by properly matching to a sense amplifier for maximum energy transfer. For transistors with input impedance in the range of a few hundred ohms this requires a transformer input.

The lower limit to Z_0, without resorting to evaporated lines or deposition of the film on a conductor, is imposed by substrate thickness, which can be reduced to perhaps $\frac{1}{2}$ mil by using mica. For a 60-mil width this gives an impedance of about 3 ohms. To obtain lower values it is probably necessary to use evaporated lines. Here the limitation of frequency cutoff due to losses in the line imposes a lower limit on conductor thickness. It can be shown that for $(RC)^2 > LC$,

$$\omega_c = \frac{1}{2\sqrt{(RC)^2 - LC}};$$

and for $(RC)^2 < LC$,

$$\omega_c = \infty,$$

where R = total line resistance, C = total line capacitance, L = total line inductance, and ω_c = cutoff frequency of the line.

The point at which losses become significant is where

$$(RC)^2 = LC$$

or

$$R/Z_0 = 1.$$

For copper,

$$R/Z_0 = \frac{2 \times 10^{-6}}{377} \times \frac{D}{ST},$$

where T = conductor thickness in cm, S = line spacing in cm, and D = line length in cm.

If it is assumed that $S = T$, then for

$$R/Z_0 = 1$$

$$S = T = \sqrt{D \frac{2 \times 10^{-6}}{377}}$$

$$= 7300 \text{ Å } \sqrt{D}.$$

For equal insulator and conductor thickness, layers of 7300 Å are required for only 1 cm of sense line. For 10 cm 23,000 Å of each would be required. At a frequency of 1 kMc the skin depth limits the effective conductor thickness to about 10,000 Å so that the insulator spacing must be increased to about 55,000 Å for a 10-cm line. However, this is nearly the thickness of the mica substrate upon which we are trying to improve in the first place.

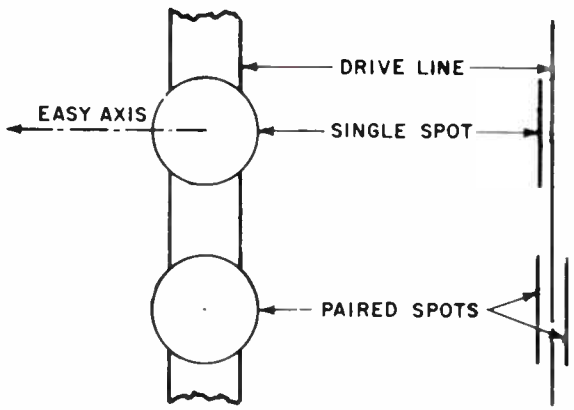
In other words, at high frequencies for even moderate sense line lengths, we cannot employ insulation spacing less than the thinnest bulk substrate available without beginning to run into rise-time degeneration. In addition, of course, this assumes that thick conductors can be evaporated without running into stress problems, insulators free of pinholes, and that neither of these affect the magnetic-film characteristics adversely.

Note that the sense line length is crucial in determining whether or not evaporated lines are desirable. A further problem with evaporated lines is that of interconnection. Until it is possible to raise the bit density high enough so that an entire memory can be fabricated in a single small area it will be difficult to make use of evaporated lines.

Bit Density

The choice of spot size is crucial in determining memory performance even with normal construction practices. Input currents are proportional to spot diameter, and signal decreases more than linearly with decreasing diameter because the film must be made thinner in order to prevent demagnetizing. Delays are also proportional to spot size. With a spacing of 10 spots per inch as in the TX-2 memory, a sense winding linking 1000 bits would be over 8 feet long. For a dielectric constant of 2 this would provide a delay of about 12 nsec.

If one attempts to reduce spot size in order to shorten line lengths it is desirable to resort to thicker films in order to maintain the signal level. It is possible to eliminate the consequent high demagnetizing field by using paired films to provide an almost closed flux path. Fig. 10(b) shows the effect, as observed with a Kerr magneto-optic apparatus, of reduction in demagnetizing force resulting from pairing two spots around a drive line (light and dark regions indicate regions of opposite magnetization). The spots are $\frac{1}{16}$ inch in diameter,



(a)

(b)

Fig. 10—(a) Diagram of paired film experiment. (b) Kerr magneto-optic demonstration of effect of film pairing. Light and dark regions are of opposite magnetization. Upper film is single, lower film one of a pair.

about 3400 Å thick; the easy axis is horizontal. The arrangement of spots and drive line is shown in Fig. 10(a). The "sandwich" spacing is two mils. Following a saturating longitudinal field the single spot is broken up because of the demagnetizing field, while the paired one remains nearly saturated. (In the photograph [Fig. 10(b)], the spots appear elliptical because they were photographed at an angle.) One of the difficulties with such a configuration is that the spacing between films must be kept small compared to spot diameter and yet accommodate the word, digit, and sense windings. Also, the currents required are twice that for an ordinary strip line around a single film.

Since in most memories the number of words is considerably greater than the number of digits, it is reasonable to attempt to shorten the sense winding and provide a more nearly square array. One such method uses rectangles whose easy axes are along the long dimension. With 10×60-mil rectangles it is possible to raise the packing density to 50 per inch along the sense winding where it is needed most, while retaining the 10 per inch spacing along the word. The demagnetizing factor for such a spot is slightly less than for a 60-mil circle so there is no need to decrease the thickness.

Another approach to providing a square array is to extend word length, *i.e.*, to provide multiple-word access. Word-organization and the low flux level of film elements make extended word length extremely attractive. For example, a 1000-word switch driving a word 200 bits long would have a number of advantages over a 4000-word switch driving 50 bits. In addition to reducing sense winding length, fewer word drivers, less word decoding, and fewer diodes would be required and parallel access to four words would be obtained. The cost would be an increase by a factor of four in digit equipment (driving and sensing). The efficiency of the digit-sense channel (*i.e.*, the degree of coupling) which determines the complexity and cost of the digit circuitry would be extremely important in such a system.

Memory Speed

The limitation on cycle time at present arises primarily from the noise occurring during the write transient interfering with the signal in the following cycle. While the bridge circuit is intended to minimize this transient it does not eliminate it entirely. It is possible to reduce the effect by reducing the number of times a write is followed directly by a read. Nondestructive readout accomplishes this by eliminating rewriting. An alternative method is to use a buffer of a few words to permit strings of reads before rewriting. The effect can also be reduced by using a slightly modified mode of memory operation. Instead of turning off the digit drivers after writing (Fig. 5), each would be left in its present state until the next write period. This eliminates the transient caused by termination of the digit pulse. The result is a reduction of cycle time by approximately the width of the write pulse of Fig. 5. This mode of operation produces either large ONES and small ZEROS, or small ONES and large ZEROS depending upon the polarity of the digit current. The state of the digit-driver is then used to interpret the signal which is read out.

Since a diode per line is required for the core switch in the TX-2 memory and only a single nonlinearity is required, it is possible to use the diodes alone for switching word lines and to eliminate the cores. A schematic of a diode switch matrix is shown in Fig. 11. The switch is

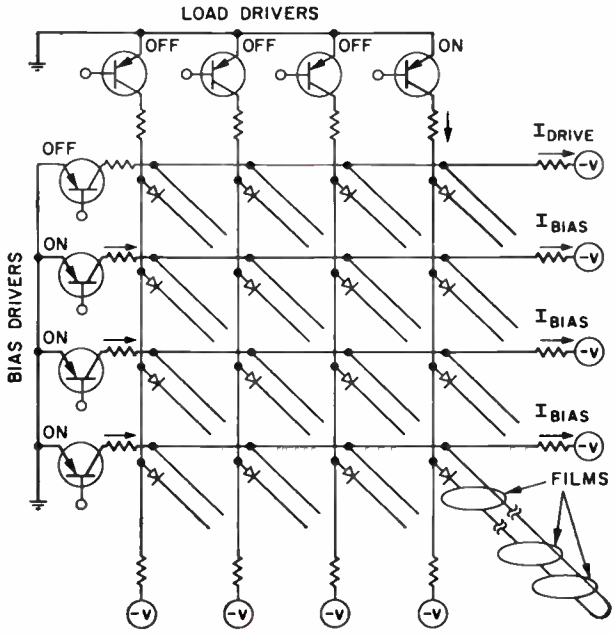


Fig. 11—Diagram of a 4×4 diode word-drive matrix. One drive line with films is shown at lower right.

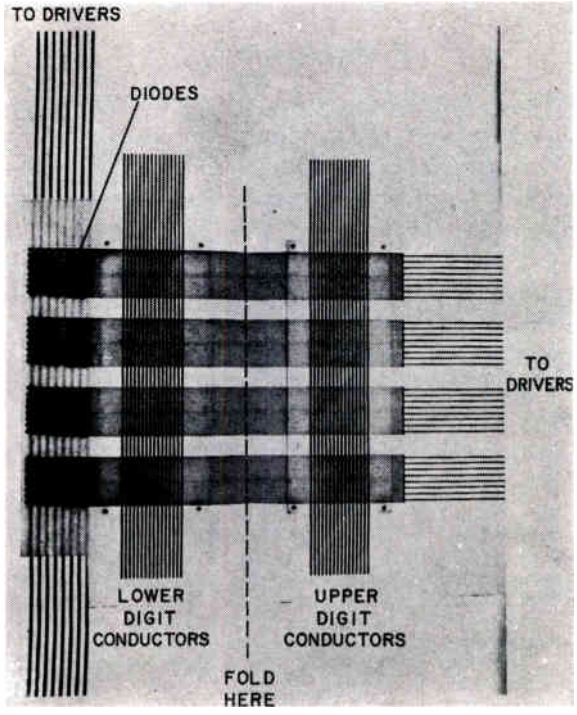


Fig. 12—An experimental diode matrix and 256-word memory using 10×60-mil films.

capable of gating 20-nsec rise-time pulses. Note, however, that although the cores were redundant they isolated the word lines from the driver thus allowing the word line to be grounded. This is extremely important at high frequencies in reducing the voltage coupled to the sense winding. Therefore, it may be necessary to use the diode matrix for selection, and to couple to each drive line with a linear transformer.

Present experiments center on a test memory which is shown in Fig. 12. This shows a 256-word diode switch (32×8) connected to word lines spaced on 20-mil centers for driving 10×60 mil rectangles. The bridge digit-sense circuit is used. This prototype is intended to be the forerunner of a full-scale memory with 1000 two hundred-bit words. The present goal is to attain a speed of between 0.1- and 0.2-μsec cycle time.

Acknowledgment

The authors wish to express their thanks to Dr. D. O. Smith and colleagues, whose work on the physics of films provided the sound basis without which an engineering program of the type presented here would have been impossible. The authors are indebted, also, to D. Strassberg and H. Blatt for their work on instrumentation and circuits. In addition, thanks are due to the many people who contributed to the preparation and testing of films and to the fabrication of wiring arrays.

The Development of the Flexible-Disk Magnetic Recorder*

R. T. PEARSON†

Summary—**A brief history of the development of the flexible-disk magnetic recorder is presented. Principles of the aeroelastic behavior of the disk and the results of a mathematical analysis of the equilibrium operating conditions are discussed. Experimental results are given which illustrate the effects of operating parameters on disk dynamics. These results indicate the design considerations necessary to produce a wide range of new storage devices. The characteristics of some of the newly developed models are presented.**

Introduction

THE maintenance of a small and constant separation between a recording head and its associated medium has been a major problem in the development of magnetic recording devices. A large number of successful solutions to this problem have been achieved for specific applications. The IBM RAMAC disk store,[1] for example, utilizes an air-floating head, while the H.D. File Drum manufactured by the Laboratory for Electronics, Inc., utilizes a read-write head supported hydrodynamically at a constant separation of 200 microinches from the drum surface.[2] Solutions such as these have provided excellent single-purpose devices, but they do not yield a good general approach to present and ever-changing data storage requirements.

The Storage Device Group of the Computer Products Division began a program two years ago aimed at the development of a new class of magnetic recording devices. The initial objective of this program was to solve the fundamental problem of reliable head-to-medium separation and thereby furnish the computer industry with a replacement for the conventional high-speed, medium-capacity drums and disks that are used quite universally at the present time. A separation means was sought which would be simple and inexpensive as well as reliable. Consideration was given to drum and disk geometries and to methods of achieving fixed-out-of-contact operation or fluid-bearing head operation. These approaches were discarded for reasons of cost and complexity. It appeared that initial studies should consider a radical design approach. The result of the design review was a study objective which gave first consideration to a system wherein the read-write heads would be fixed and the recording medium would in some manner be made to dynamically approach the heads.

Exploratory Experiments

The starting point of the experimental work was the concept of a recording medium dynamically approaching fixed heads, and a simple laboratory experiment was designed to illustrate the principle. A thin disk of mylar recording tape (2 mils in thickness) was attached to the

* Received by the IRE, July 29, 1960; revised manuscript received, October 25, 1960.

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[1] T. Noyes and W. E. Dickinson, "Engineering design of a magnetic-disk random-access memory," *Proc. WJCC*, pp. 42–44; 1956.

[2] H. W. Fuller, S. P. Woodsum, and R. R. Evans, "Design and systems aspect of the HD file drum," *Proc. WJCC*, Los Angeles, Calif., May 6–8, 1958, pp. 197–203; March, 1959.

hub of a rotating shaft, as shown in Fig. 1. The disk, rotating in air, was observed to vibrate over a wide range of speeds because of its low resonant frequency. A recording head shaped to produce an air-bearing effect was positioned at a point close to the periphery of the disk.[3] The disk was drawn into close proximity (1 mil) of the recording-head gap and assumed a stable standing-wave shape. Successful recording and playback was accomplished on this demonstration device. The introduction of additional read-write heads caused multiple modes and resulted in instability of the rotating disk. This experiment demonstrated, however, the concept of simple, automatically-controlled separation.

A second experiment was designed to control the standing-wave shape of the disk in a similar system by introducing a single air-bearing surface on the side of the disk opposite a recording head. In this device, heads were located a fixed distance away from the control surface. Recording was accomplished on only a few heads, and the approach had a poor volume-storage efficiency as well as the tolerance disadvantages of a fixed out-of-contact assembly.

An experiment was next performed which developed to be of key importance to the final device concept. A mylar disk was rotated in proximity to a smooth backplate and was observed to conform stably to the backplate surface. The experimental apparatus is illustrated in Fig. 2. A clearance hole was cut in the backplate to accommodate the driving hub. The disk was rotated and observed initially to vibrate as before, but as the backplate was moved axially toward the plane of rotation, the disk was attracted toward the plate where it operated at a stable equilibrium separation. The distance between the backplate and the disk was determined by the method shown in Fig. 2(a). A calibrated read-write head was located on the top surface of the disk and adjusted to an equivalent 1 mil head-to-medium separation by monitoring the readout voltage. The disk was then stopped and slid out of the gap and the head lowered until it contacted the backplate. Measurements taken by this method did not yield accurate separation (s) measurements as a function of radius (r), but showed the following important results: 1) The separation distance, s, was constant during rotation. 2) The separation distance was about 10 mils. 3) Separation was observed to vary as a function of the hub height. 4) The separation appeared to be relatively insensitive to shock.

An operating device was then constructed with several read-write heads mounted on bridges as shown in Fig. 2(b). This device operated satisfactorily, and recording densities of 150 wavelengths per inch were easily achieved on a 6-inch diameter disk.

[3] M. C. Shaw and F. Max, "Analysis and Lubrication of Bearings," McGraw-Hill Book Co., Inc., New York, N. Y., pp. 332–334, 1949.

Principle of the Flexible-Disk Recorder

At the conclusion of the latter experiment, it was clear that the operating model was still, in reality, a fixed-separation device. It appeared, however, that if the read-write heads could be incorporated into the backplate, and the disk made to operate in the same stable manner, except at a separation from the backplate in the order of 1 mil, an extremely promising storage device would result.

The desired reduction of separation was obtained by placing a thin sheet of solid material over the bottom of the hub clearance hole. Closing off this area caused the rotating disk to go into contact with the backplate. A new model was constructed as shown in Fig. 3 with an adjustable valve which allowed control of the rate at which air could enter beneath the disk, and which resulted in the ability to control the disk-to-backplate separation. This basic configuration represents all the essential components of the flexible-disk memory device. Experiments carried out on the model of Fig. 3 showed the following (not necessarily independent) parameters to have an effect on the operating separa-

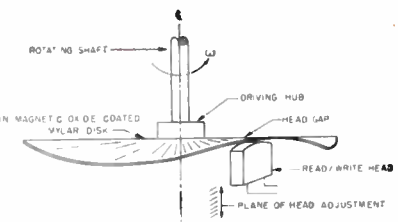


Fig. 1—Flexible mylar disk conforming to a rigid air-bearing head shape.

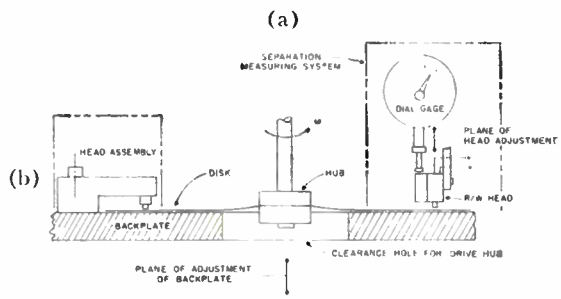


Fig. 2—Flexible mylar disk operating in equilibrium over a smooth backplate.

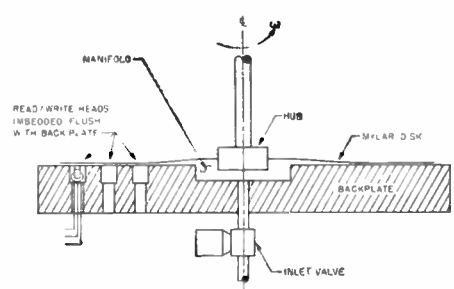


Fig. 3—Schematic diagram of the flexible disk device.

tion: 1) disk material and thickness, 2) the axial distance between disk hub clamping surface and the backplate, 3) the ratio of the hub radius to manifold radius, 4) angular velocity, 5) the volume rate of through-flow gas entering the manifold, 6) disk diameter, 7) the physical properties of the environmental gas, 8) the electrostatic charge on the disk, and 9) temperature.

It was possible at this point in the development to construct successful device models. Experimental observations were repeated which showed the early models to have excellent resistance to mechanical and temperature shock. Models were easily built since precision construction was obviated by installing heads in the backplate and then lapping the backplate surface smooth. The critical separation automatically occurred as a result of disk rotation. Figs. 4 and 5 illustrate some of the early experimental disk models.

Analysis of Disk Operation

In the nonoperating condition, the flexible disk is limp and rests against the backplate. When the drive shaft is rotated, the disk tends to straighten out under the action of centrifugal force and lift away from the backplate. At the same time, a circumferential velocity is imparted, by viscous friction, to the fluid in the space between the disk and backplate. This circumferential velocity gives rise to a centrifugal force on the fluid and a resulting outward radial velocity. These fluid velocities vary with radius and generate a pressure field in the separation gap that varies radially. These pressure forces differ from the pressure forces acting on the open, or atmospheric, side of the disk. The flexible disk deflects to equalize these pressure fields, and in so doing, counter centrifugal and curvature forces are caused to act on the disk material. The equilibrium operating condition exists as a balance of the pressure forces generated by the fluid flow, together with the normal components of the centrifugal and curvature forces in the disk. A typical radial disk shape is shown in Fig. 6, in which the separation coordinate is much exaggerated compared with the radial coordinate.

The complete mathematical analysis of this equilibrium condition is beyond the scope of this paper and a summary of current results is presented. (See Fig. 6 for geometry.) The flow analysis was derived from the Navier-Stokes equations and the continuity equation[4] with the following simplifying assumptions: steady flow, incompressible fluid, axial symmetry, laminar flow, very low Reynolds' number referred to gap width and angular velocity, and separation (s) small compared with radius (r).[5]

An order-of-magnitude analysis was performed which yielded the expression for hydrodynamic pressure in the

[4] H. Schlichting, "Boundary Layer Theory," McGraw-Hill Book Co., Inc., New York, N. Y., p. 44; 1955.
[5] A. H. Shapiro, unpublished notes, Mass. Inst. Tech., Cambridge Mass.; 1959.

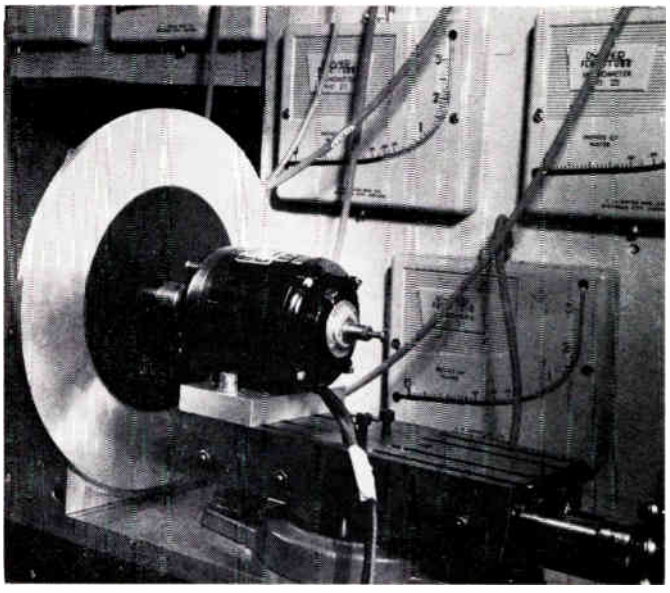


Fig. 4—5-inch-diameter disk rotating against a backplate equipped with radial pressure measuring manometers.

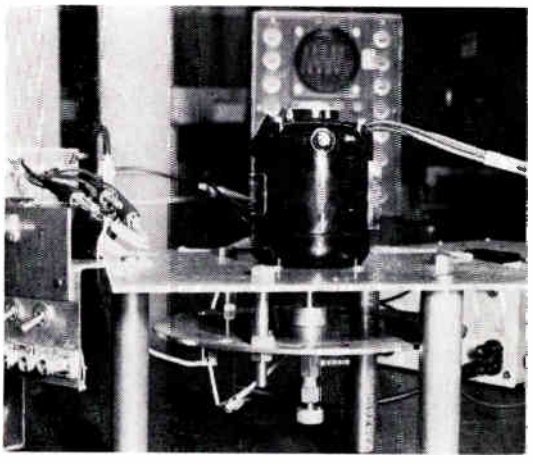


Fig. 5—Early operating flexible-disk model. Disk diameter: 6 inches; speed: 6000 rpm; separation: 1 mil.

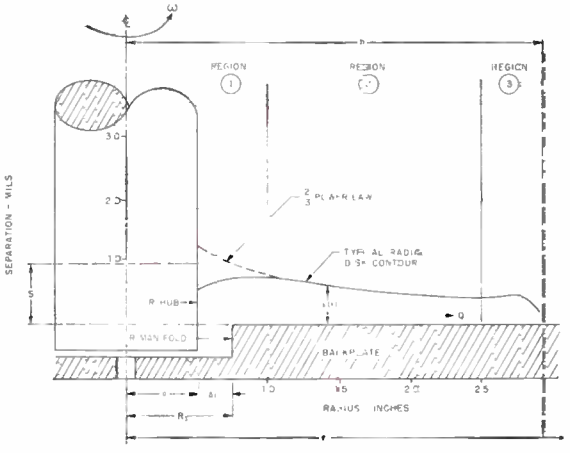


Fig. 6—Disk geometry and typical radial disk shape.

separation gap:

$$\frac{dp}{dr} = \frac{3}{10}\rho\omega^2 r - \frac{6NQ}{\pi r s^3}, \tag{1}$$

where p is the hydrodynamic pressure, r is the radial distance from center, ρ is the density of the gas, ω is the angular velocity of the disk, μ is the absolute viscosity of the gas, Q is the radial volume flow per unit time, and s is the separation distance between the disk and backplate. In this equation, the inertial term $(3/10)\rho\omega^2 r$ represents the centrifugal pressure field in the separation gap resulting from the circumferential velocity. The viscous term $-6\mu Q/\pi r s^3$ is the resistance to radial flow of the fluid in the gap which is equivalent to the pressure drop across a long, thin, circumferential slit.

The expression for elastic equilibrium of the disk was obtained from the mechanical forces acting upon the rotating disk. Fig. 7 depicts the pressure, centrifugal, and curvature forces acting on an element $rd\phi dr$ of the disk. Resolving the normal components of these forces which affect radial disk shape results in the expression for pressure,

$$-p = \sigma_r t \frac{d^2 s}{dr^2} - r\omega^2 \rho_d t \frac{ds}{dr}, \tag{2}$$

where t is the thickness of the disk, ρ_d is the mass density of the disk material, and σ_r is the radial tensile stress in the disk. The three forces acting upon the disk element have four possible equilibrium conditions, depending upon the slope and curvature of the element as shown in Fig. 8, and these are useful in picturing the principal forces acting at any particular region on the disk.

From (1) and (2), a differential equation is obtained for the equilibrium operating condition of the disk:

$$\frac{d}{dr}\left(t\sigma_r \frac{d^2 s}{dr^2}\right) - \rho_d \omega^2 \frac{d}{dr}\left(tr \frac{ds}{dr}\right) = -\frac{3}{10}\rho\omega^2 r + \frac{6\mu Q}{\pi r s^3}. \tag{3}$$

The radial stress is given by the equation

$$\sigma_r = \frac{(3+\nu)\rho_d \omega^2 b^2}{8\left(\frac{r}{b}\right)^2}\left[1 - \left(\frac{r}{b}\right)^2\right]\left[k + \left(\frac{r}{b}\right)^2\right], \tag{4}$$

where ν is Poisson's ratio for the disk material, a is the inner or shaft radius of the disk, b is the outer disk radius, and

$$k = \left(\frac{a}{b}\right)^2 \left[\frac{1-\nu}{1+\nu}\right] \left[\frac{1 - \left(\frac{a}{b}\right)^2\left(\frac{1+\nu}{3+\nu}\right)}{1 + \left(\frac{a}{b}\right)^2\left(\frac{1-\nu}{1+\nu}\right)}\right]. \tag{5}$$

With the aid of (4) and the introduction of a step function for the separation at the manifold boundary condition, (3) may be nondimensionalized to

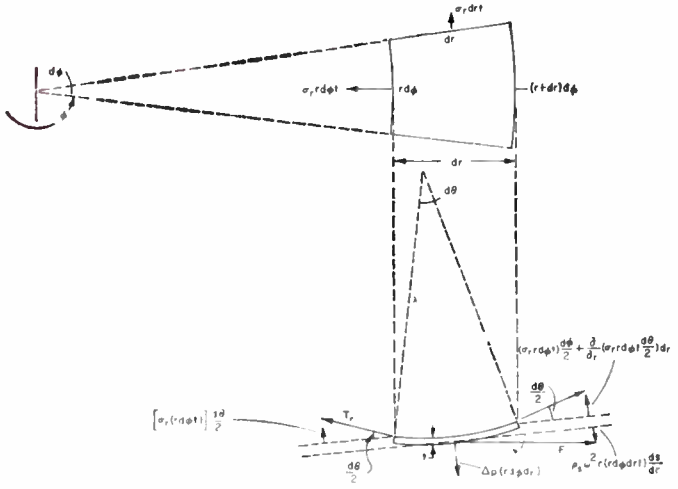


Fig. 7—Forces acting upon an element of the rotating disk.

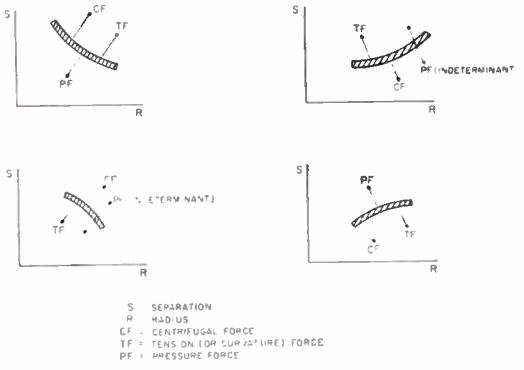


Fig. 8—Equilibrium conditions of disk forces. S=separation, R=radius, CF=centrifugal force, TF=tension (or curvature) force, PF=pressure force.

$$\frac{3+\nu}{8}\frac{d}{dx}\left[f(x)\frac{d^2 y}{dx^2}\right] - \frac{d}{dx}\left(x\frac{dy}{dx}\right) = -Gx + \frac{C_Q}{xy^3}U(x - x_0 - \Delta x_0), \tag{6}$$

where

$$f(x) = \frac{(1-x^2)(k+x^2)}{x^2},$$

$$G = \frac{3}{10}\frac{\rho}{\rho_d}\frac{b^2}{St},$$

$$Y = \frac{s}{S},$$

$$C_Q = \frac{\sigma Q \mu}{\pi S^4 \omega^2 \rho_d},$$

$$x = \frac{r}{b}, \qquad x_0 = \frac{a}{b}, \qquad \Delta x_0 = \frac{\Delta a}{b},$$

$$U_{(r)} = \begin{cases} 1, & r > 0 \\ 0, & r < 0 \end{cases}$$

S is the hub-to-backplate distance and Δa is the hub-to-manifold gap.

This equation, together with appropriate boundary conditions, represents the complete formulation for obtaining the equilibrium separation. The solution of this equation is unavailable by direct methods, but preliminary data are available from an analog computer solution where the Boundary Layer Technique[6] is used to divide the problem into three regions along the disk radius, as shown in Fig. 6.[7] Region I is the hub boundary region and typically extends radially for a distance in the order of twice the hub radius. This boundary region is important because it establishes what the rest of the disk shape shall be. The disk shape in this region develops to be a function of

$$m^3 = \frac{C_Q}{G} = \frac{20\mu Q}{\pi\rho\omega^2 s^3 R_i^2}, \tag{7}$$

where R_i is the manifold radius. The analog computer solution shows that for values of m less than or equal to 1, the disk curves downward as shown in Fig. 9(a) and for values of m larger than 1, the disk curves upward as shown in Fig. 9(b).

Region II extends over most of the remaining radius except for a short peripheral boundary region. Over Region II, the separation varies according to the expression

$$y = \frac{C_Q(G)^{1/3}}{x^{2/3}} = \frac{k}{x^{2/3}}. \tag{8}$$

This equation represents a family of approximately hyperbolic curves. The particular curve (*i.e.*, the value of k) that any disk will assume depends upon the boundary condition existing in Region I. The curves of Regions I and II are made to join smoothly together in the computer solution.

The peripheral boundary Region III (Fig. 6) would not exist if the pressure at the edge of the disk were atmospheric. With this condition, the separation follows (8) all the way to the outer edge. Experimental evidence, however, indicates that the pressure at this point is not atmospheric. A theoretical treatment is not yet complete for this condition of boundary Region III.

The power required to drive the disk is found from the shearing stress of the fluid in the separation gap at a distance r from the axis.[8] With the assumption of circular symmetry, the power becomes

$$P = 2\pi\omega^2\mu \int_{R_i}^{b} \frac{r^3 dr}{s(r)}. \tag{9}$$

[6] C. F. Carrier, "Advances in applied mechanics," in "Boundary Layer Problems in Applied Mechanics," Academic Press, Inc., New York, N. Y., vol. III; 1953.

[7] T. R. Goodman, "Theory of Spinning Disk, Equilibrium," Allied Res. Assocs., Inc., Boston, Mass., Tech. Rept. No. 808; 1960.

[8] Schlichting, *op. cit.*, p. 445.

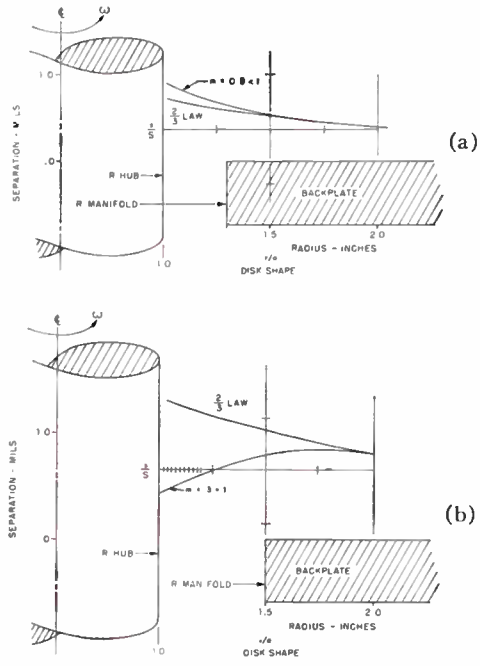


Fig. 9—Theoretical Region I disk profile.

The r^3 term in the integrand of (9) indicates that most of the power is dissipated at the outer radius. Hence, if R_i is small, and the separation follows the two-thirds power law,

$$P = \frac{3}{7}\frac{\pi\mu\omega^2}{s} b^4. \tag{10}$$

The power associated with the open side of the disk can be shown to be negligible.[9] Fig. 10 shows the theoretical power dissipation of (10) with angular velocity as a parameter and for a constant radial separation of 1 mil. The 2500 inches per second line represents the present peripheral velocity limitation imposed by the transition from laminar to turbulent flow of the air in the separation gap.

The above analysis predicts tape shapes that are in close quantitative agreement with experimental data obtained. In the case of the power equation, agreement within five per cent between the theory and experimental results has been achieved.

Experimental Program

The experimental program was designed to provide data for the theoretical studies, and to show feasibility of the flexible disk principle for magnetic recording applications. Magnetic recording requires a small and constant separation between a recording head and its associated magnetic medium. This optimum separation depends upon the recorded wavelength which, for disk storage, increases with radius. Because of this fundamental importance of separation to the device operation, the experimental program was concentrated on a

[9] *Ibid.*, p. 78.

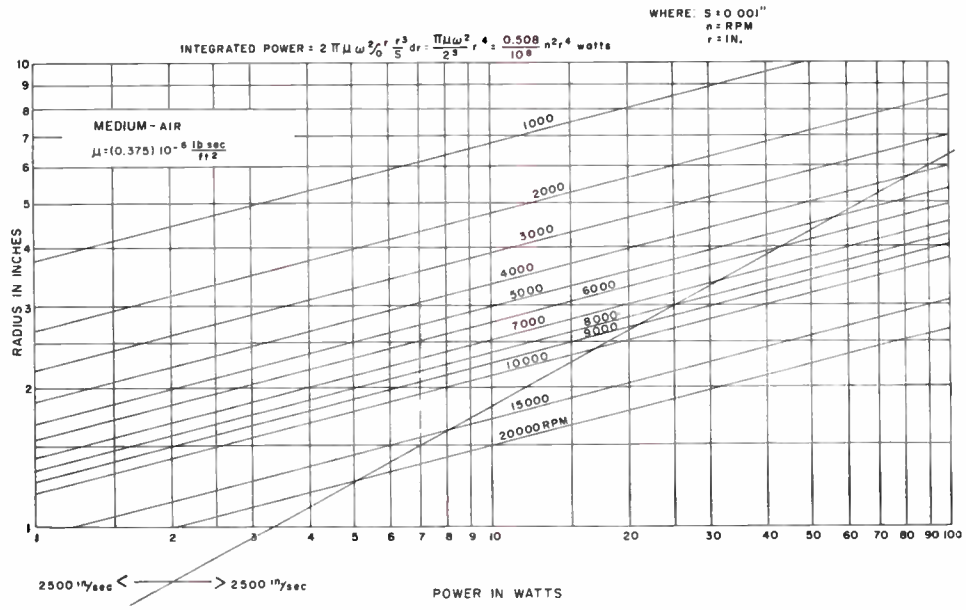


Fig. 10.

series of measurements which relate separation as a function of radius to the operating parameters.

Disk-to-stabilizing-plate separation was first measured magnetically by employing the well known formula,[10]

$$L = 20 \log \frac{E_1}{E_2} = \frac{54.6\Delta S}{\lambda}. \qquad (11)$$

where L is the amplitude loss in decibels, E_1 is the initial voltage readback, E_2 is the new voltage readback, ΔS is the change in head-to-medium separation, and λ is the recorded wavelength.

Recording heads were installed flush with the surface of the backplate of an experimental fixture and positioned on a diameter to allow separation measurements at every $\frac{1}{4}$ inch of disk radius. The disk was operated and a sinusoidal signal written by driving the recording heads with an appropriate current and frequency. The readback signal was then observed over a range of parameter changes including a zero, or in-contact, situation created by blowing a jet of air on the disk directly over each recording head. These data were then reduced by (11) and resulting disk shapes were plotted as shown in Fig. 11. This method of measuring separation provides an excellent way of studying dynamic stability, but the in-contact readings wore the disk and absolute separation accuracy was impaired. These experiments were inconclusive at the boundary Regions I and III (see Fig. 6), because heads could not be physically installed in the manifold Region I, and residual elastic curvature of the disk in Region III prevented usable recording separations. This magnetic instrumentation remains as the most effective and the simplest tool for studying the dynamics of the disk behavior, since any change in operating separation is observable as an output voltage.

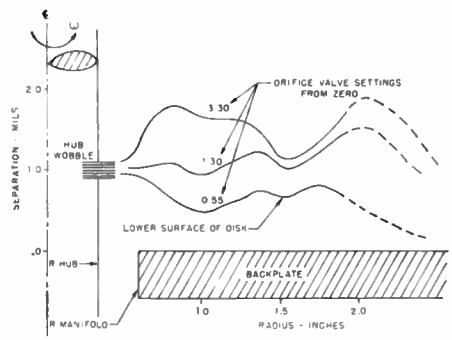


Fig. 11—Separation vs radius determining magnetically for various orifice settings. Disk diameter: 5 inches; speed: 12,000 rpm.

To solve the absolute separation instrumentation problem, an optical fixture was designed as shown schematically in Fig. 12. The observer focuses the microscope on a point on the rotating disk, illuminated by a stroboscopic light source. A dial or electric indicator mounted on the microscope barrel contacts a reference surface which is calibrated radially with the backplate. The optical assembly is mounted on a mechanical stage which permits registered motion across the disk radius. Because the disk is moving, a knife edge is provided as shown in Fig. 12 to give a projected image on the tape surface. The microscope is then focused on this image. The ultimate resolving power of this optical system is determined by rather complex factors, and present experimental depth discrimination is $\pm 7 \times 10^{-6}$ inches

[10] R. L. Wallace, "The reproduction of magnetically recorded signals," *Bell Sys. Tech. J.*, vol. 30, pp. 1145–1173; October, 1951.

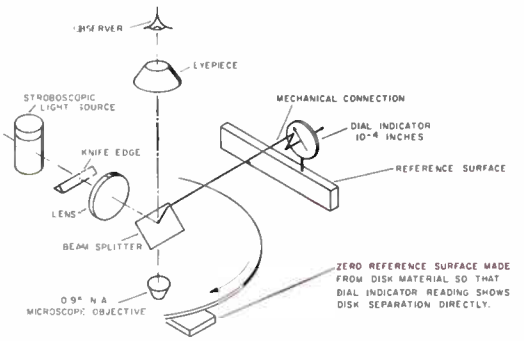


Fig. 12—Schematic diagram of optical system used to measure disk separation as a function of radius. *Note:* The optical system and the dial indicator are mounted on a movable carriage so that separation may be measured at any radius.

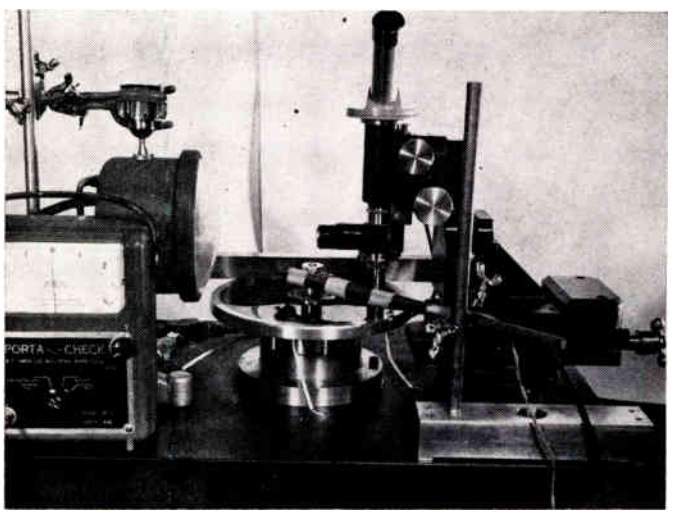


Fig. 13—Typical experimental set-up of optical separation-measuring apparatus.

under ideal conditions. Factors such as vibration, transient thermal expansion and surface variations decrease this static figure to about ± 20 to $\pm 40 \times 10^{-6}$ inches, depending upon conditions. The fixture is designed to vary accurately and measure the following principal dependent and independent variables of the system.

Independent:

Angular velocity
Vertical disk to backplate separation at the drive hub
Hub diameter
Manifold diameter
Disk thickness
Gas properties (ρ, μ, t).

Dependent:

Manifold pressure (volume flow)-sensitive manometers
Separation—optically
Power—dynamometer
Backplate temperature—thermocouples
Electrostatic charge.

Fig. 13 is a photograph of a typical experimental set-up on one of the optical fixtures

Experimental Observations

Five types of magnetic tape disks have been studied to date. These tapes all have a mylar base but differ in thickness and laminate construction as indicated in Table I. It is important for this circular recording requirement to have a random or circular orientation of magnetic particles on the tape so that the readout voltage will not be amplitude modulated as a result of magnetic orientation. The best tapes tested have shown approximately twenty per cent modulation caused by the orientation of magnetic particles. The tapes, coated on one side only, have a tendency to curl slightly at the periphery when cut into a disk. This curling influences the operating radial shape, as shown in Fig. 6. Additionally, the single-coated tapes have a large temperature dependency like a bimetal strip which is detrimental to device operation at environmental extremes. Fig. 14 illustrates the radial separation as a function of disk material for a 4.25-inch-diameter disk operating at 8000 rpm with a vacuum of 0.05 inch of water in the manifold. This vacuum is self-generated and controlled by the inlet orifice to the manifold.

From the standpoint of magnetic recording, a suitable radial separation is a straight line angling away from the backplate in the manner shown in Fig. 15. This disk shape would provide a constant recording resolution since the separation as a function of radius would be maintained at a constant fraction of the recorded wavelength. Since the driving power varies as the fourth power of the radius, and inversely with separation, this shape reduces substantially the driving power requirement. The disk shapes of Fig. 15 illustrates how an approximation of the ideal case was achieved for a specific requirement. These shapes are plotted from optical data taken on a 4.25-inch-diameter disk operating at 8000 rpm with zero pressure in the manifold. The separation coordinate is exaggerated 1000 times compared with the radial coordinate. Curve "A" is the natural disk shape resulting from rotation. This shape was modified by the introduction of atmospheric air through sixteen 1/16-inch-diameter holes in the backplate at a radius of 1.6 inches and by punching sixteen 1/16-inch-diameter holes in the tape periphery. The resulting shape illustrated by curve "B" closely resembles the initial requirements. The total power was reduced by these changes from 17 to 8.3 watts. The point of inflection representing minimum separation of curve "B" may be moved radially by varying the position of the secondary air supply holes. The down-turned periphery of the disk is characteristic of the single laminate tape used for this experiment.

A. *Effect of Holes in Disk*

Holes in the disk periphery, as mentioned in connection with Fig. 15, reduce power consumption by caus-

TABLE I
MAGNETIC TAPE

Mfr.	Des. No.	Thickness Mils	Lo-Temp. Perf.0F	Hi-Temp. Perf.0F	Abrasion Resistant	Orientation Per cent	Oxide Thickness Mils	Type of Performance	Edge Performance
3M	186	2.0	Poor 32°	140°	Excellent	20 per cent	0.50	Rigid	Curls; Holes Required
3M	199	1.35	G.—0°	250°	Good	>20 per cent	0.45	Flexible	Curls; No Holes Required
3M	197300	3	G.	250°	Good	>20 per cent	0.50	Rigid	Curls; Holes Required
Reeves	442	2.0	Med.		Good	≈20 per cent	Double Back	Rigid	No Curls; Holes Optional
3M	1033	2.67	G.	140°	Excellent	20 per cent	Double Back	Rigid	No Curls; Holes Optional

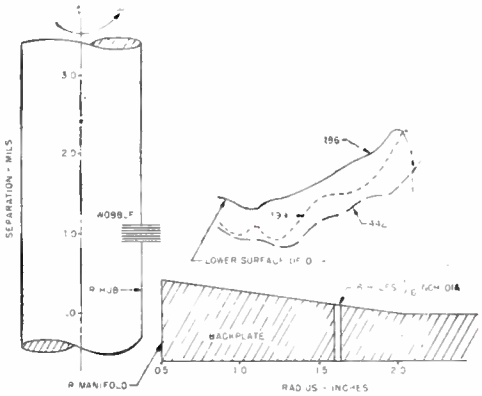


Fig. 14—Effect of disk construction on separation. Manifold vacuum: 0.05 inch H_2O; speed: 8000 rpm; disk diameter: 4.25 inches.

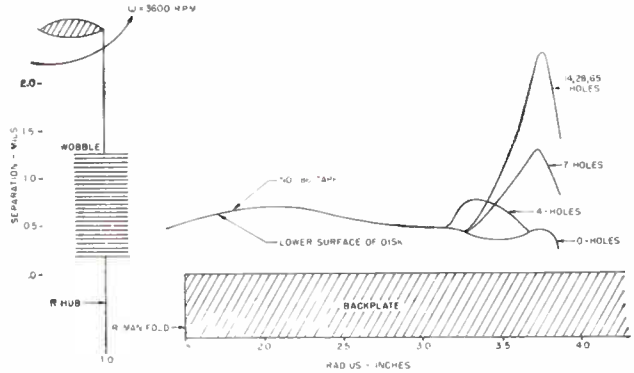


Fig. 16—Effect of peripheral holes on disk separation. Holes: $\frac{1}{16}$-inch diameter; disk: 7.5-inch diameter; zero manifold vacuum.

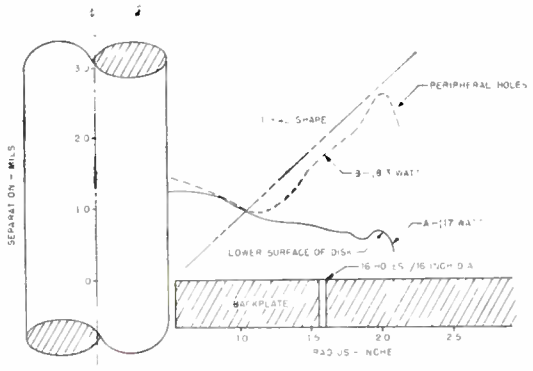


Fig. 15—Comparison of flexible disk contours and motor powers with and without holes in backplate and disk periphery. Disk diameter: 4.25 inches; speed: 8000 rpm; zero manifold vacuum.

ing the disk to lift away from the backplate at the outside edge. Fig. 16 illustrates the effect of the number of edge holes for a 7.5-inch-diameter disk of 186 tape operating at 3600 rpm with zero manifold pressure. The maximum lift occurs when fourteen holes are used, and the addition of more holes does not provide further power reduction. In some cases, peripheral separation may be 200 to 300 microinches; hence, it is important from a practical standpoint that these holes be free from burrs.

B. Effect of Grooved Backplate

Another method of separation control has been demonstrated as shown in Fig. 17. A circumferential groove is machined in the backplate as shown in diagram A of Fig. 17. Six air-feeder grooves, inclined at a slight angle to their respective radius, either supply or remove air from the separation gap depending upon the direction of rotation. This action results in the two stable separation curves shown.

C. Effect of Speed Variation

Fig. 18 illustrates the effect of speed variation on separation within the laminar flow region. The disk tends to straighten out as the speed increases. The maximum operating speed is presently estimated to be between 3000 and 5000 inches per second peripheral velocity. The limitation is imposed by the onset of aeroelastic flutter at the edge of the disk. This flutter condition is related to the transition from laminar to turbulent flow of the air in the separation gap. Double-backed and more rigid tapes have higher transition speeds than thinner, less rigid tapes. The transition velocity is related, as well, to the gas properties of the environmental fluid. The minimum speed of operation is governed by the elastic neutrality of the tape material. Edge curl of

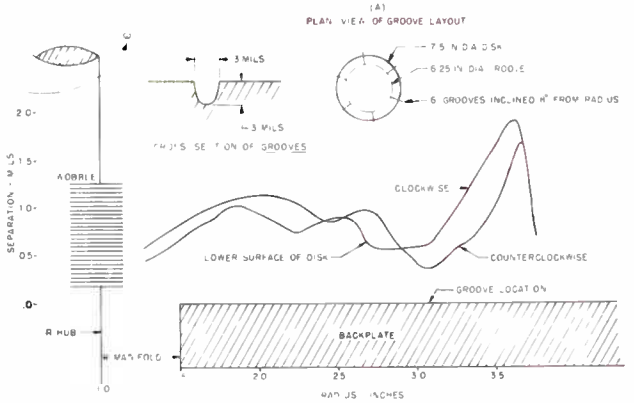


Fig. 17—Effect of direction of rotation on separation for grooved backplate. Disk diameter: 7.5 inches; speed: 3600 rpm; zero manifold vacuum.

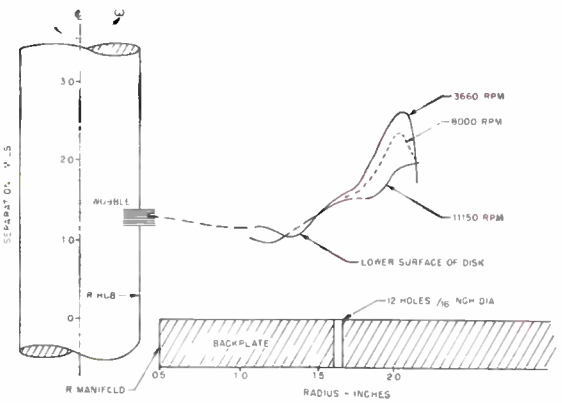


Fig. 18—Effect of speed variation on separation. Disk diameter: 4.25 inches; zero manifold vacuum.

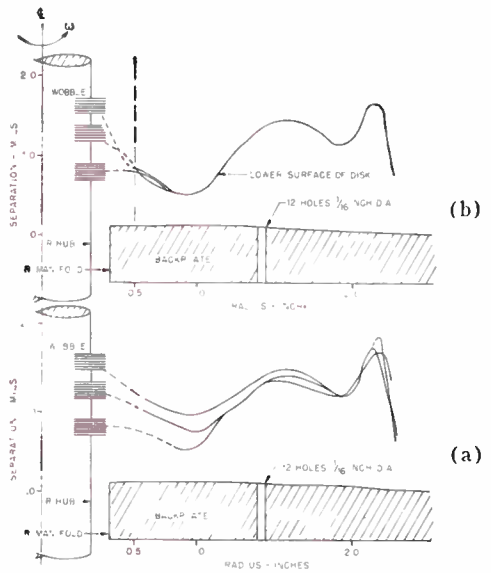


Fig. 19—Effect of hub height on separation for (a) zero manifold vacuum, (b) 0.06-inch H_2O manifold vacuum. Disk diameter: 4.25 inches; speed: 7690 rpm.

the unsymmetrical tapes is greatly exaggerated at slow speed because of diminished centrifugal forces.

D. Effect of Hub-Height Variation

The optical disk contours of Fig. 19 were obtained from a 4.5-inch-diameter disk of No. 199 tape rotating at 7690 rpm. The backplate was equipped with twelve 1/16-inch-diameter secondary pressure-regulating holes. Peripheral disk holes were not used for this experiment because of the flexibility of the No. 199 tape. The curves of Fig. 19(a) illustrate the effect of hub-height variation for a condition of zero manifold pressure. The essential linear hub and disk separation tendency existing from the hub to the 1.1-inch radius point would continue for the entire radius of the disk, if the secondary air-supply holes were omitted. Air entering these holes upsets the natural two-thirds power law tendency and acts as a control parameter to produce the independence of separation on hub height shown from the 1.1-inch radius point outward.

The disk shapes of Fig. 19(b), taken from the same data run, clearly demonstrate the manifold-vacuum-control principle. In this experiment, the flow-control valve was adjusted to produce 0.06 inch of H_2O vacuum in the center manifold. The curves show that for 1-mil hub-height variation, complete disk control is achieved at the 0.5-inch radius point. This important controlled separation feature makes it possible to construct devices which utilize standard-bearing assembly tolerances. Extreme hub-height elevations tend to level the disk out with respect to the backplate which is undesirable from a magnetic standpoint. The maximum separation control is achieved on flexible tapes with additional disk radius being required to control the thicker, more rigid tapes.

Fig. 20 shows the effect of hub-height variation on separation for a 7.5-inch-diameter disk of No. 186 tape operating in conjunction with a circumferential grooved backplate at 3600 rpm, and zero manifold vacuum. Curves A, B, and C have a value of the Region I flow constant $m<1$, and curves D, E, and F have a value of $m>1$. These disk shapes were predicted theoretically and illustrated in Fig. 9. The secondary control principle, as affected by a grooved backplate, is shown from the 3.2-inch radius point outward.

E. Effect of Manifold Vacuum

The effect of manifold vacuum on radial separation is illustrated by the disk contours of Fig. 21. The experimental conditions were No. 199 tape, 7690 rpm, 4.5-inch diameter and twelve 1/16-inch diameter secondary pressure regulating holes in the backplate. As mentioned in connection with the hub-height data, the linear effects to the left of the 1.1-inch radius point of Fig. 21(a) would continue for the entire disk radius in the absence of secondary air holes. The influence of manifold vacuum is more pronounced in the less rigid tapes, and at large hub heights. The separation becomes independent of manifold vacuum for small hub heights and small vacuums as shown in the curves in Fig. 21(b).

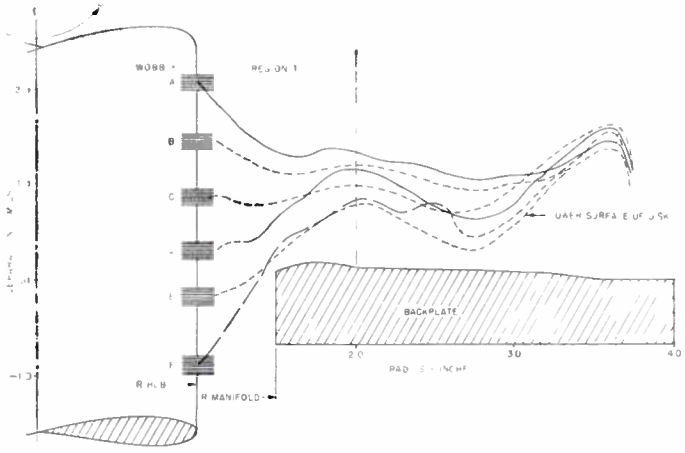


Fig. 20—Effect of hub-height variation on separation. Speed: 3600 rpm; disk diameter: 7.5 inches; zero manifold vacuum.

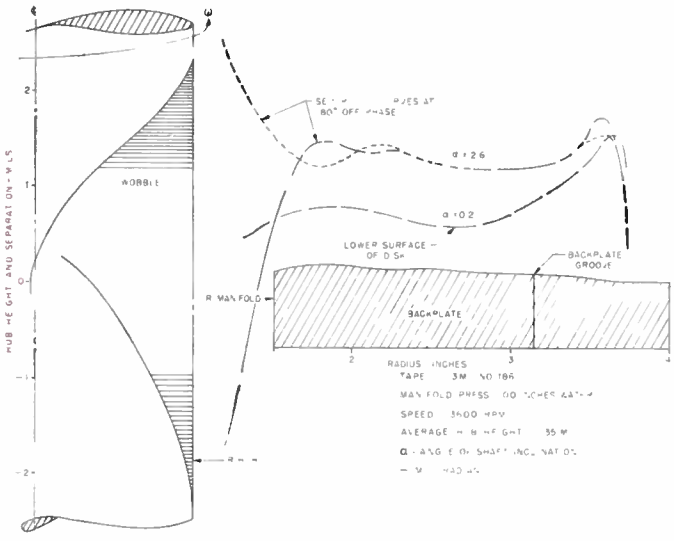


Fig. 22—Effect of hub wobble on separation and axisymmetry. Disk diameter: 7.5 inches; speed: 3600 rpm; zero manifold vacuum.

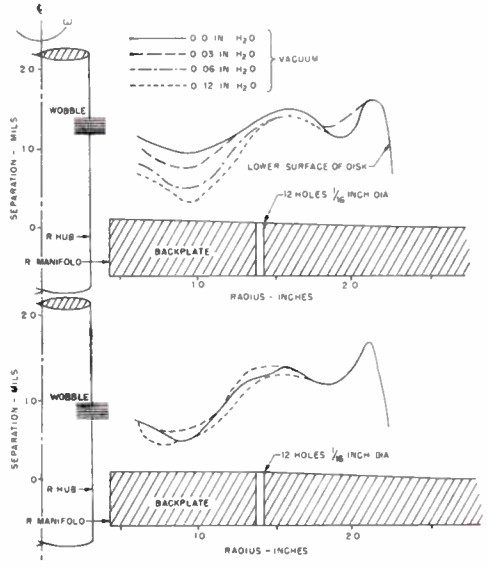


Fig. 21—Effect of manifold vacuum on separation. Disk diameter: 4.25 inches; speed: 7690 rpm.

F. Effect of Shaft Inclination or Wobble

The net effect of shaft inclination or hub wobble is shown in Fig. 22, where the shaft inclination with respect to the backplate is increased from 0.2 to 2.6 milliradians. A 7.5-inch-diameter disk of No. 186 tape, operating over a grooved backplate at 3600 rpm, was used to study this effect. Increasing the shaft inclination traps air beneath the disk at the high point of rotation; the air is then unable to escape back into the manifold because of the centrifugal force effect. This results in a general increase of the separation curve. This experiment demonstrates the stability of disk separation with respect to time. It is important from a practical standpoint that hub wobble be kept to an absolute minimum in devices which require minimum separation.

G. Effect of Hub Radius, Shrouds, and Environmental Conditions

Minimum-drive hub radii depend upon the elastic properties of the disk material and the buckling force of the viscous torque over the manifold area. Solid and perforated shrouds, positioned on the open or atmospheric side of the disk, serve to control differential pressures across the disk, and may be used to influence separation in the manner of secondary air supply holes or backplate grooves. Maximum separation is limited by flutter when the aerodynamic forces decrease below the normal resonant forces of rotation. To date, environmental tests on existing devices show no decrease of readout signals under conditions in excess of 50 G shock and for vibrations of 10 G's from 0 to 3000 cycles. Excellent temperature vs readback stability exists from 0°C to 100°C for presently tested tapes with new double-backed, elastically neutral tapes, indicating a considerable improvement over the present range.

Fig. 23 is a photomicrograph of a 133-kc sinusoidal recording on one of the mylar disks. The tracks have been made visible by utilizing a powder-pattern technique. This photomicrograph illustrates the actual appearance of recorded data on a 4.25-inch-diameter disk operated at 8000 rpm with a track width of 24 mils and a guard space of 8 mils.

Device Applications

Fig. 24 is a photograph of a flexible-disk memory device designed for use in a satellite. This unit is a complete system having a motor, disk, heads, head selector matrix, read/write amplifiers, and interface circuitry. The volume of the device is 380 cubic inches; the weight is 10 pounds, and it may be mounted upon any axis. The disk is $4\frac{1}{4}$ inches in diameter, with 38 channels capable of storing 1024 bits per channel. The channels are made

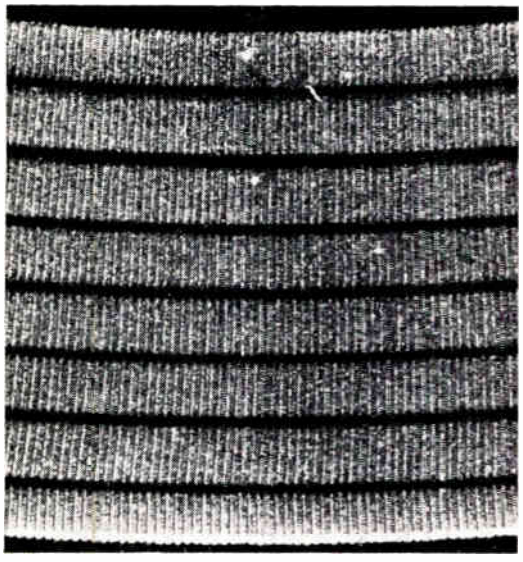


Fig. 23—Photomicrograph of 133-kc recorded sinusoidal signal on a disk made visible by powder-pattern techniques.

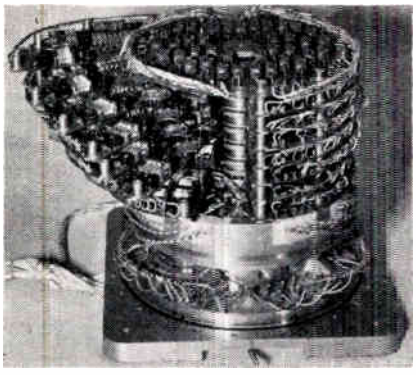


Fig. 24—Photograph of complete satellite memory device with cover removed.

up of 32 general storage tracks, 5 adjustable 32 ± 3-bit recirculating registers, one main clock track, and 3 word-locating tracks. The total power required is 13 watts (non-recording). Approximately 2000 components are contained on 7 stacked, circular printed-circuit boards, each of which is split and hinged for servicing and head adjustment. The memory is designed for continuous operation for 3500 hours in ground, launch, and orbital environment.

A new 100,000-bit capacity memory is illustrated by the photograph of Fig. 25. This unit stores 3000 bits per track with a bit rate from 90 to 400 kc. The unit has 40 channels arranged as follows: 32 general storage tracks, 3 spare tracks, 3 clock and timing tracks, and 2 register tracks having a total of 4 recirculating loops. The register length is 32 bits $\pm$ 3 bits. The disk speed ranges

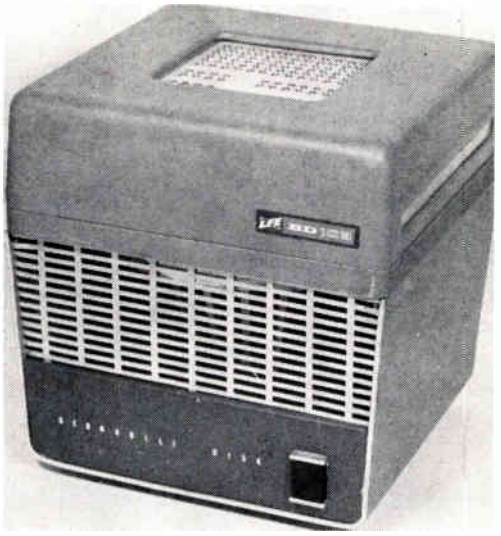


Fig. 25—Photograph of BD-103 100,000-bit memory.

from 1800 to 8000 rpm, and the disk is driven by an induction or a synchronous motor. The size of the unit is 9 inches $\times$ 9 inches $\times$ 5 inches.

The extension of the flexible-disk principle to multiple-disk memories is underway. Large quantities of data may then be stored within a single synchronous unit providing fast access to clocked information. Systems employing both fixed- and servo-positioned recording head installations are presently being designed.

Stable separations are presently being achieved at 300 microinches, and recording densities in excess of 1000 wavelengths per inch have been accomplished under laboratory conditions. The feasibility of extending the flexible-disk technique to video storage at frequencies up to 10 Mc has been shown.

Acknowledgment

The author wishes to thank the Laboratory for Electronics, Inc., for permission to publish this material.

The author wishes to acknowledge the contributions of many people to the work reported here, in particular those of W. J. Gorman, co-inventor of the flexible-disk device, and R. K. Lee, Jr., who devised the optical measuring system. Additional contributors, in part, are R. C. Kelner, director of the Computer Products Division, H. W. Fuller, manager of the Applied Research Laboratory, D. Vakharia, and R. E. Morley, members of the Storage Device Group.

The author wishes to thank Prof. A. H. Shapiro of M.I.T., who first analyzed and derived the equilibrium equations, and Dr. T. Goodman of Allied Research, Inc., who devised and performed the computer solutions of these equations.

Pattern Recognition Using Autocorrelation*

L. P. HORWITZ†, MEMBER, IRE, AND G. L. SHELTON, JR.†

Summary—**A class of techniques for character recognition is described. These techniques are characterized by the property that the only parameters of the input which are used are those which are independent of the position of the character; that is, these techniques are registration invariant.**

In Section I of this paper, we describe the registration invariant mathematical formalism which underlies these techniques, and in Section II we describe in more detail the physical realization of several recognition schemes based on these concepts. Some results from our computer simulation of these procedures are given.

Introduction

DURING the past year, considerable progress has been made in optical data processing and character recognition. Some theoretical techniques have been developed which seem appropriate for handling at least a few aspects of the problem, and several machines have been proposed as physical realizations of the prescribed mathematical operations.

Since the theoretical techniques that have been worked out have played an important role in the experimental program, they will be described in some detail in Section I of this paper. The basic idea underlying these techniques is that of registration invariance; *i.e.*, all patterns are described in such a way that shifting translationally in any direction does not affect any observed parameter. This mode of description has strong implications for the engineering side of the situation; a machine designed to deal with information in this form does not have to search in a character field for the precise location of the character. There are, of course, other ways of dealing with character misregistration, but the essential point to be made here is that this particular aspect of the problem is dispensed with from the start, and an appropriate mathematical formalism is pointed out by requiring this invariance property. The starting point for the development of these ideas is the construction of a discrete binary representation of the patterns to be recognized. This is done, in principle, by placing a discrete mesh over the character and setting each mesh point to unity if it covers a black part of the character and to zero if it covers white. The patterns are then described by counting specified pairs of ones regardless of their positions in the matrix for all possible kinds of pairs.

In Section II of this paper, several recognition systems will be proposed in some detail as physical realizations of the mathematical operations prescribed in the first part. In particular, if the limiting case of a large number of mesh points is examined (that is, the continuous case), it becomes apparent that one procedure for making decisions within this mathematical framework is equivalent to an optical scheme utilizing diffraction effects proposed by one of the authors (GLS) before the theoretical work was started. This parallel registration invariant optical scheme will be described, and some of the modifications for increasing discrimination which follow from the theoretical analysis will also be discussed. An alternative optical scheme will then be presented which is based on a configuration of Kovásznay and Arman[1] at Johns Hopkins. This device uses geometrical optic effects entirely, and has properties that differ markedly from the diffraction scheme with regard to the modifications that can easily be imposed to aid discrimination. It is possible, for example, to change the nature of the transformation performed by the optical system in such a way that the autocorrelation (two-point combination count) operation is carried out in the vertical direction (for registration invariance in this direction) and an autoconvolution operation is carried out horizontally.

One of the chief disadvantages of such optical schemes for some application areas, however, is the necessity for having available transparent images of the patterns to be detected. Photographic negatives work quite well, but it is desirable in some cases, particularly when batch processing is not feasible, to work directly from the printed document. In addition, the size of the alphabet that can be handled in a parallel optical scheme is limited by the total light energy available from the source; the energy in each channel goes down with the reciprocal of the number of channels. We have therefore considered the design of electronic machines which operate on an electronic input from an optical scanner of some sort.

I. Theory of Pattern Recognition

A. Registration Invariance and Autocorrelation

One of the outstanding engineering problems encountered in the construction of character recognition devices has been the accommodation of character misregistration. The problem has not, of course, been insoluble; prescanning techniques and shifting search modes have been used effectively, but always result in a loss of time or increase in storage. For example, the simplest and most straightforward character recogni-

* Received by the IRE, August 1, 1960; revised manuscript received, October 27, 1960.

† IBM Mohansic Lab. Res. Ctr., Yorktown Heights, N. Y.

[1] L. S. Kovásznay and A. Arman, "Optical autocorrelation measurement of two-dimensional random patterns," *Rev. Sci. Instr.*, vol. 28, pp. 793–797; October, 1957.

tion device consists of placing a mask over the pattern in question which consists of, say, a photographic negative of a known character. The amount of light passing through the mask is an indication of the similarity of the known and unknown characters, if the two are properly lined up. In general, it is impossible to prescribe the exact location of printed characters in advance, so that a search through various positions becomes necessary. Some of the distinct advantages of masking (stability against noise is identical to the use of matched filters or correlation in communication theory) are thereby minimized because of the additional uncertainties introduced.

It has, therefore, been our purpose to develop a description of patterns which is, by construction, independent of the absolute position of a character in a field of observation within translations or shifts. Since any two-dimensional pattern of black and white can be represented to any degree of approximation by an $N\times N$ matrix of zeros and ones for sufficiently large N, it will be adequate for our purposes to consider such binary matrices rather than the source patterns initially. The ones correspond to matrix points falling on black portions of the pattern, and the zeros to matrix points falling on white (see, for example, Fig. 1).

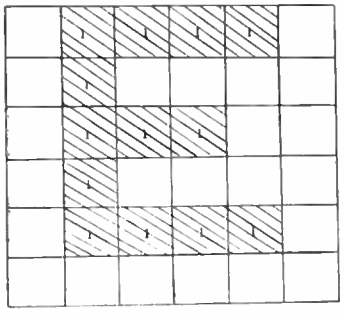


Fig. 1—"Ones" correspond to matrix points falling on the black portion of the pattern, and "zeros" to points off the pattern.

It is convenient to define the function $f(\boldsymbol{r})$, where $\boldsymbol{r}$ is the (x, y) coordinate of a matrix point, as unity on black points, zero on white. The number of pairs of ones with relative separation $\boldsymbol{R}=(\Delta x, \Delta y)$, if known for each $\boldsymbol{R}$, provides a registration invariant description (within a 180° rotation) of the pattern.

This representation has some intuitive appeal in that important geometrical characteristics are not obscured as in the crossing-type schemes or in the single-slit scan bank systems. If the number of pairs of each kind, $D(\boldsymbol{R})$, is plotted as a function of $\boldsymbol{R}=(\Delta x, \Delta y)$, then the resulting surface has information concerning local structure close to $|\boldsymbol{R}|=0$ and gross long-range structure for larger $|\boldsymbol{R}|$.

In order to examine the properties of the function $D(\boldsymbol{R})$ in greater detail, it is necessary to consider its formal expression in terms of $f(\boldsymbol{r})$. The existence of a pair of ones with separation $\boldsymbol{R}$ terminating at the matrix point $\boldsymbol{r}$ is established by the nonvanishing of the product $f(\boldsymbol{r})f(\boldsymbol{r}-\boldsymbol{R})$. Hence, the total number of pairs with separation $\boldsymbol{R}$ is given by

$$D(\boldsymbol{R}) = \sum_{\boldsymbol{r}} f(\boldsymbol{r})f(\boldsymbol{r}-\boldsymbol{R}). \tag{1}$$

Since the vector $\boldsymbol{r}-\boldsymbol{R}$ does not necessarily lie in the $N\times N$ matrix, the computation prescribed by (1) can be carried out only if $f(\boldsymbol{r})$ is defined over a more extensive domain. We therefore think of the pattern $f(\boldsymbol{r})$ defined initially in the first $N\times N$ quadrant of a $2N-1\times 2N-1$ matrix, all other quadrants containing zeros. The structure of the larger matrix is to be repeated periodically over the plane, and the sum in (1) is taken over $-(N-1)\leq x, y\leq(N-1)$. It is clear from (1) that the description $D(\boldsymbol{R})$ is independent of the position of the pattern $f(\boldsymbol{r})$ so long as it is contained in some $N\times N$ matrix within the larger $2N-1\times 2N-1$ matrix; it corresponds, in fact, to the discrete autocorrelation function of $f(\boldsymbol{r})$.

It is interesting to consider the harmonic analysis of $D(\boldsymbol{R})$. To do this, we define the discrete "Fourier transform" of $f(\boldsymbol{r})$:

$$f(\boldsymbol{r}) = \frac{1}{(2N-1)^2}\sum_{\boldsymbol{Q}} \bar{f}(\boldsymbol{Q}) \exp\left\{\frac{2\pi i}{2N-1}(\boldsymbol{r}\cdot\boldsymbol{Q})\right\}, \tag{2}$$

where

$$\bar{f}(\boldsymbol{Q}) = \sum_{\boldsymbol{r}} f(\boldsymbol{r}) \exp\left\{\frac{-2\pi i}{2N-1}(\boldsymbol{r}\cdot\boldsymbol{Q})\right\}. \tag{3}$$

The proof of the consistency of these relationships is a simple exercise resting on the identity

$$\sum_{\boldsymbol{r}} \exp\left\{\frac{2\pi i}{2N-1}(\boldsymbol{Q}-\boldsymbol{Q}')\cdot\boldsymbol{r}\right\} = \begin{cases} 0, \boldsymbol{Q}\neq\boldsymbol{Q}' \bmod \text{periodicity} \\ (2N-1)^2, \boldsymbol{Q}=\boldsymbol{Q}' \bmod \text{periodicity.}\end{cases} \tag{4}$$

All summations are taken over the $2N-1\times 2N-1$ box. Substituting (2) into (1), one finds that

$$D(\boldsymbol{R}) = \frac{1}{(2N-1)^2}\sum_{\boldsymbol{Q}} |\bar{f}(\boldsymbol{Q})|^2 \cdot\exp\left\{\frac{2\pi i}{2N-1}(\boldsymbol{R}\cdot\boldsymbol{Q})\right\}, \tag{5}$$

and comparing this result with (2), we learn that the transform of $D(\boldsymbol{R})$ is given by

$$\bar{D}(\boldsymbol{Q}) = |\bar{f}(\boldsymbol{Q})|^2. \tag{6}$$

B. Optics and a Procedure for Decision

Although $D(\boldsymbol{R})$ can be calculated electronically by techniques such as those which we describe in Section II, the harmonic representation is especially convenient for describing a parallel optical technique suitable for certain areas of application. To see this most simply, we shall pass to the limit of the continuous distribution.

Let

$$N\Delta l = L, \tag{7}$$

where Δl is the spacing between mesh points and L the size of the character field. Let also

$$\begin{aligned} \mathbf{s} &= \mathbf{r}\Delta l \\ \mathbf{S} &= \mathbf{R}\Delta l \end{aligned} \tag{8}$$

and

$$\begin{aligned} F(\mathbf{s}) &= f(\mathbf{r}), \\ \theta(\mathbf{S}) &= (\Delta l)^2 D(\mathbf{R}). \end{aligned} \tag{9}$$

It then follows that, in the limit,

$$\begin{aligned} \theta(\mathbf{S}) &= \int d\tau F(\mathbf{s})F(\mathbf{s}-\mathbf{S}) \\ F(\mathbf{s}) &= \frac{1}{(2L)^2}\sum_{\mathbf{Q}} \bar{F}(\mathbf{Q}) \exp\left\{\frac{\pi i}{L}(\mathbf{s}\cdot\mathbf{Q})\right\} \\ \bar{F}(\mathbf{Q}) &= \int d\tau F(\mathbf{s}) \exp\left\{-\frac{\pi i}{L}(\mathbf{s}\cdot\mathbf{Q})\right\}, \end{aligned} \tag{10}$$

where $\bar{F}(\mathbf{Q}) = \lim\ (\Delta l)^2 \bar{f}(Q)$, and $d\tau$ is the differential of area. The integrals are taken over a $2L \times 2L$ square centered at $\mathbf{s}=0$, and $\mathbf{Q}$ is discretely summed over the entire plane. In this limiting process, the pattern remains stationary, but the number of defining points increases indefinitely. The point function $F(\mathbf{s})$ is piecewise constant at values 0 or 1. The theorem expressed by (6) is now of the form

$$\bar{\theta}(\mathbf{Q}) = |\bar{F}(\mathbf{Q})|^2, \tag{11}$$

a result that can be obtained by multiplying both sides of (6) by $(\Delta l)^4$ and taking the limit. The variable $\mathbf{Q}$ in (11) is still discrete; when $L \to \infty$, the relations applying to the usual Fourier transform are obtained, but it will suffice for our purposes to restrict the discussion to a periodic input pattern. Within such a final trivial limiting process, the function $\bar{\theta}(\mathbf{Q})$ is precisely the intensity pattern spatially displayed by the Fraunhofer diffraction pattern of an optical filter with transmission factor $F(\mathbf{s})$. The physical arrangement for producing this pattern will be discussed in Section II; we wish to concern ourselves here only with some of the mathematical properties of this representation of the input data.

The utility of this optical procedure for obtaining the Fourier transform of the autocorrelation function is most apparent from the point of view of a particular method of making decisions, *i.e.*, of identifying unknown patterns. One procedure for identifying patterns, analogous to the selected-point or region schemes such as that used in the IBM 1210 Sorter-Reader, would be to require the presence of important pairs of points or regions defined in a relative sense (as given in the autocorrelation function). Since there is no uncertainty in the registration of the pattern, this procedure could easily be developed for any given font in a small alphabet application with a careful computer analysis. Since each particular font would require individual analysis, and no particular design of type seems to have an intrinsic and universal interest at present, this technique will not be discussed further here. Instead, we shall consider a procedure which is analogous to the matched filter detection techniques of communication theory or the well-known masking technique used in the early work in character recognition. This method weights all configurations equally, and is in fact a calculation of the cosine of the angle between two multidimensional vectors.[2] For the discrete autocorrelation functions, we define the measure of similarity as

$$S_{AB} = \frac{\sum_{\mathbf{R}} D_A(\mathbf{R})D_B(\mathbf{R})}{\left(\sum_{\mathbf{R}} D_A^2(\mathbf{R})\right)^{1/2}\left(\sum_{\mathbf{R}} D_B^2(\mathbf{R})\right)^{1/2}}, \tag{12}$$

where A and B refer to, say, an unknown and a known character respectively. According to the Schwartz inequality, $0 \leq S_{AB} \leq 1$, and $S_{AB}=1$ only if $D_A(\mathbf{R})$ and $D_B(\mathbf{R})$ are identical. This implies that A and B are either identical or differ only by a 180° rotation or a shift.

With the help of (4) and (5), we find that

$$\sum_{\mathbf{R}} D_A(\mathbf{R})D_B(\mathbf{R}) = \frac{1}{(2N-1)^2}\sum_{\mathbf{Q}} |\bar{f}_A(\mathbf{Q})|^2 |\bar{f}_B(\mathbf{Q})|^2, \tag{13}$$

so that an alternative expression for S_{AB} (computation in the "frequency" domain) is

$$S_{AB} = \frac{\sum_{\mathbf{R}} |\bar{f}_A(\mathbf{Q})|^2 |\bar{f}_B(\mathbf{Q})|^2}{\left(\sum_{\mathbf{R}} |\bar{f}_A(\mathbf{Q})|^4\right)^{1/2}\left(\sum_{\mathbf{R}} |\bar{f}_B(\mathbf{Q})|^4\right)^{1/2}}. \tag{14}$$

If the numerator and denominator are multiplied by $(\Delta l)^8$, the limit $N \to \infty$ can be carried out without changing the value of S_{AB} except for the change due to the approximation of representing the continuous pattern by a discrete finite set of points initially. In the optical realization of this calculation, $|\bar{F}_B(\mathbf{Q})|^2$ corresponds to a filter in the Fraunhofer plane with the transmission factor given by the value of the function at the spatial point corresponding to the wave number integer pair $\mathbf{Q}$. The factor $|\bar{F}_A(\mathbf{Q})|^2$ is obtained from the intensity distribution that is the Fraunhofer diffraction pattern of the unknown character, and the sum is performed by collecting the total amount of light energy transmitted through the filter in a photovoltaic device.

In actual practice, a number of filters $|\bar{F}_B(\mathbf{Q})|^2$ would

[2] We are grateful to Dr. H. H. Goldstine for suggesting this very useful criterion for application here.

be used in parallel or series, each B corresponding to a separate recognition channel. Since the normalization factor

$$\left(\sum_{Q} | \overline{F}_A(Q) |^4 \right)^{-1/2}$$

is the same for all channels, recognition may be accomplished equally well if this factor is deleted from (14) and the maximum voltage over all channels is detected. It therefore remains for us to define the factor

$$\left(\sum_{Q} | \overline{F}_B(Q) |^4 \right)^{-1/2}$$

operationally. This quantity can be represented by an adjustable uniform attenuating filter T_B for each channel. If a uniform collimated light beam impinges upon the filters $| F_B(Q) |^2$ and T_B in series, the transmitted energy density is proportional to

$$| F_B(Q) |^2 T_B.$$

This distribution may then be reflected back through the pair of filters resulting in a total transmitted energy proportional to

$$\left(\sum_{Q} | F_B(Q) |^4 \right) T_B^2. \tag{15}$$

T_B may then be adjusted so that the quantity (15) is the same for each channel, resulting in the appropriate set of normalizing filters.

In order to get a feeling for the kind of discrimination that we would get with a real alphabet, some characters were processed digitally on the basis of (12). The relatively high resolution used insures a reasonable approximation to what the analogous optical results would be, and the results indicate a minimum discrimination of a few per cent (Fig. 2).

We have obtained comparable results in our studies of direct masking (no autocorrelation transform first) with the same alphabet in perfect registration. We have also simulated the effect of noise (Fig. 3) and the procedures of registered masking of the character and filtered autocorrelation functions compare very well in a rough way; the amount of noise that is added can amount to roughly as much as the area of the character before discrimination is lost in either case. We have, therefore, concluded that with respect to noise sensitivity and discrimination, nothing is lost by going to the autocorrelation description, and a great deal is gained in the registration problem. By use of appropriate nonlinear detection techniques, it should be possible to do better against noise, but this is still a subject for investigation.

It has been our desire to improve the discrimination by making distinct autocorrelation functions more nearly orthogonal with the same linear transformation on every pattern. If this linear transformation has the form

$$D'(R) = \sum_{R'} M(R - R')D(R'), \tag{16}$$

then an optical realization in a simple form is assured. Consider, for example, the application of the criterion (12) to functions of the form (16). The numerator of (12) is given by

$$\sum_{RR'R''} D_A(R'')M(R - R'')M(R - R')D_B(R') = \sum_{RR'} D_A(R')L(R' - R)D_B(R), \tag{17}$$

where

$$L(R) = \sum_{R'} M(R')M(R' - R). \tag{18}$$

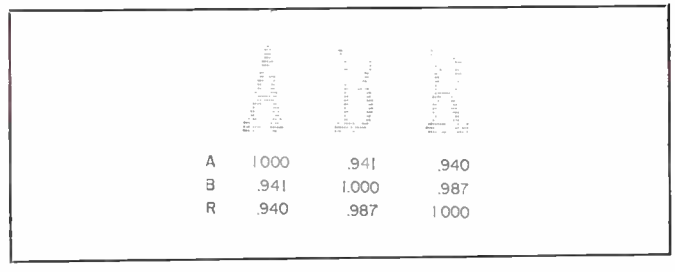
In the wave number representation, (17) can be written as

$$\frac{1}{(2N - 1)^2} \sum_{Q} \overline{D}_A(Q)\overline{D}_B(Q)\overline{L}(Q) = \frac{1}{(2N-1)^2} \sum_{Q} | \overline{f}_A(Q) |^2 | \overline{f}_B(Q) |^2 | \overline{M}(Q) |^2. \tag{19}$$

The normalization can be carried out in the same way as described in connection with (15). It follows from (19) that whatever the form of $M(R)$ (it may contain negative terms), an optical decision procedure can be fabricated with positive transmission filters.

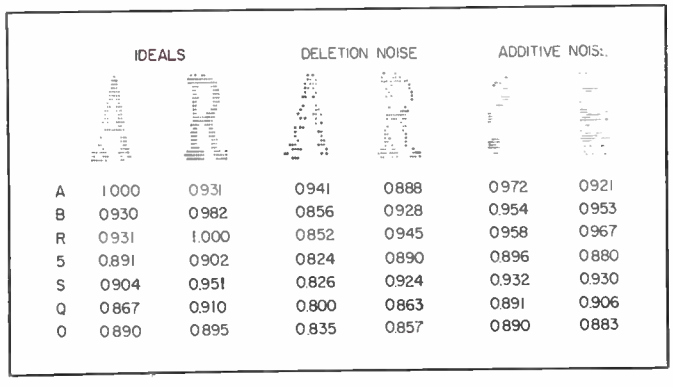
In particular, the use of a transformation of the form

$$M(R) = \begin{pmatrix} & 1 & \\ 1 & 1 & 1 \\ & 1 & \end{pmatrix} \tag{20}$$



A	1.000	.941	.940
B	.941	1.000	.987
R	.940	.987	1.000

Fig. 2—Comparison of autocorrelation functions.



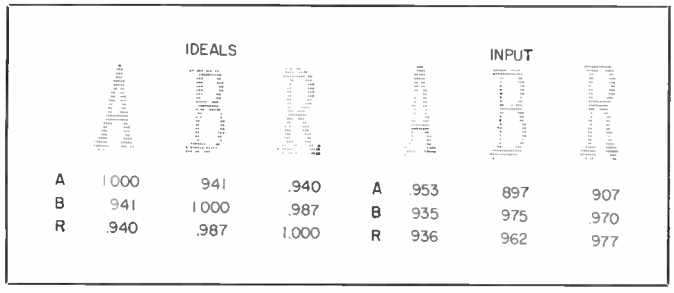
A	1.000	0.931	0.941	0.888	0.972	0.921
B	0.930	0.982	0.856	0.928	0.954	0.953
R	0.931	1.000	0.852	0.945	0.958	0.967
5	0.891	0.902	0.824	0.890	0.896	0.880
S	0.904	0.951	0.826	0.924	0.932	0.930
Q	0.867	0.910	0.800	0.863	0.891	0.906
0	0.890	0.895	0.835	0.857	0.890	0.883

Fig. 3—Comparison of autocorrelation functions with noisy input.

produced good results going across a few printed fonts, but decreased the discrimination within a given fixed font (Fig. 4). On the other hand, the second-difference operation[3] (the opposite of averaging, so to speak)

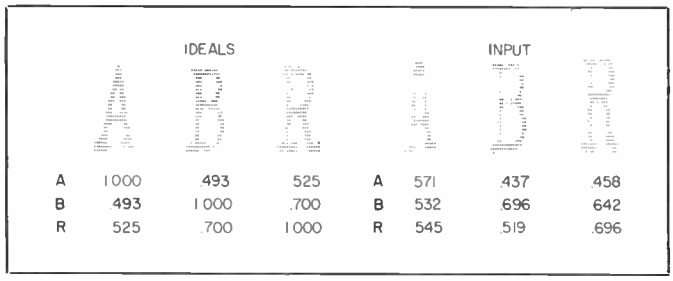
$$M(R) = \begin{bmatrix} & -1 & \\ -1 & 4 & -1 \\ & -1 & \end{bmatrix}, \qquad (21)$$

produced poor results across fonts but increased the discrimination within a given font considerably. Computer simulation showed a discrimination of the order of 20 per cent to 30 per cent in bad cases as compared to 10 per cent with a comparison of autocorrelation functions (Fig. 5). In a test for noise sensitivity, we found the surprising result that the autocorrelation recognition technique with a second-differencing was just as insensitive with respect to the introduction of errors as without second-differencing, but discrimination was considerably improved, even in very noisy situations (Fig. 6).



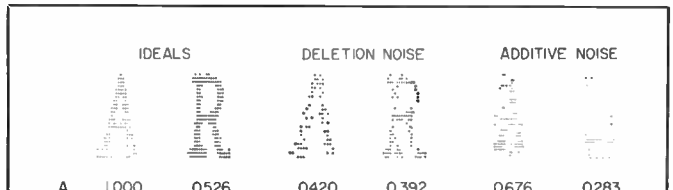
A	1.000	.941	.940	A	.953	.897	.907
B	.941	1.000	.987	B	.935	.975	.970
R	.940	.987	1.000	R	.936	.962	.977

Fig. 4—Comparison of smoothed autocorrelation functions.



A	1.000	.493	.525	A	.571	.437	.458
B	.493	1.000	.700	B	.532	.696	.642
R	.525	.700	1.000	R	.545	.519	.696

Fig. 5—Comparison of second-differenced autocorrelation functions.



A	1.000	0.526	0.420	0.392	0.676	0.283
B	0.494	0.695	0.300	0.450	0.478	0.320
R	0.526	1.000	0.338	0.539	0.507	0.364
5	0.522	0.576	0.305	0.434	0.506	0.256
S	0.515	0.654	0.327	0.451	0.508	0.285
Q	0.528	0.556	0.322	0.395	0.510	0.280
0	0.581	0.587	0.326	0.411	0.523	0.259

Fig. 6—Noise sensitivity for second-differenced autocorrelation functions.

[3] $|\overline{M}(\mathcal{Q})|^2 \propto |\mathcal{Q}|^4$ in the optical analog.

II. Physical Realization

In the first part of this paper, registration invariant counting functions were described based on a binary matrix description of the characters, and it was shown that as the matrix mesh becomes finer and finer the continuous representation of the pair counting function is

$$\theta(S) = \int_{-\infty}^{+\infty} F(s) \cdot F(s - S) d\tau;$$

and since $\theta(S)$ is also given by

$$\theta(S) = \frac{1}{(2\pi)^2} \int_{-\infty}^{+\infty} \bar{\theta}(W) \cos(2\pi W \cdot S) dW \quad \text{where} \quad W = \frac{\mathcal{Q}}{2L}$$

one can either work with the wave number spectrum $\bar{\theta}(W)$ or with the autocorrelation function $\theta(S)$.

A. Wave Number Spectrum Model

The wave number spectrum of a pattern $F(x, y)$ is given by $\overline{F}(W_1W_2) \cdot \overline{F}(W_1W_2)^*$, where $\overline{F}(W_1W_2)$ is the Fourier transform of $F(x, y)$. It is known that the Fraunhofer diffraction pattern of a transmitting aperture is given by the square of the Fourier transform of the aperture;[4] consequently, the wave number spectrum of an input character can be obtained in parallel by a rather simple optical arrangement. Fig. 7 is a schematic of the optical arrangement required to produce the wave number spectrum, and Fig. 8 shows the wave number spectra for a set of numerals. The coordinates of the Fraunhofer plane are wave numbers, and the origin of the coordinate system is always located at the intersection of the optic axis and the Fraunhofer plane. If Cartesian coordinates (μ) and (ν) are set up in the Fraunhofer plane, the transform coordinates W_1 and W_2 are related as follows:

$$W_1 = \frac{2\pi}{\lambda} \frac{\mu}{f_2} \qquad W_2 = \frac{2\pi}{\lambda} \frac{\nu}{f_2}.$$

The size of the diffraction pattern is therefore proportional to the wavelength of the source and the focal length of L_2, and inversely proportional to the size of the aperture. The latter fact can be seen by computing the transform of a simple rectangular slit of height h and width w, which results in

$$I = A_0^2 \frac{\sin^2 W_1 \frac{w}{2}}{W_1^2 \left(\frac{w}{2}\right)^2} \cdot \frac{\sin^2 W_2 \frac{h}{2}}{W_2^2 \left(\frac{h}{2}\right)^2}$$

so that the distance between the origin and the first zero along the W_1 direction is

$$\mu_0 = \frac{\lambda f_2}{w}$$

[4] G. Joos, "Theoretical Physics," Blackie & Son, Ltd., London, Eng., p. 369; 1949.

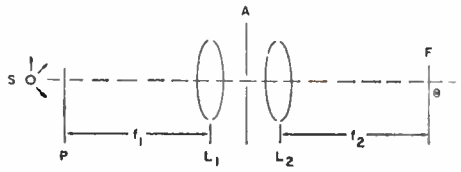


Fig. 7—Schematic of the optical arrangement. s = monochromatic point source; P = pin hole aperture; L_1 = lens, f_1 = focal length of L_1; O = optic axis; A = transmitting aperture of input; L_2 = lens; f_2 = focal length of L_2; F = Fraunhofer plane.

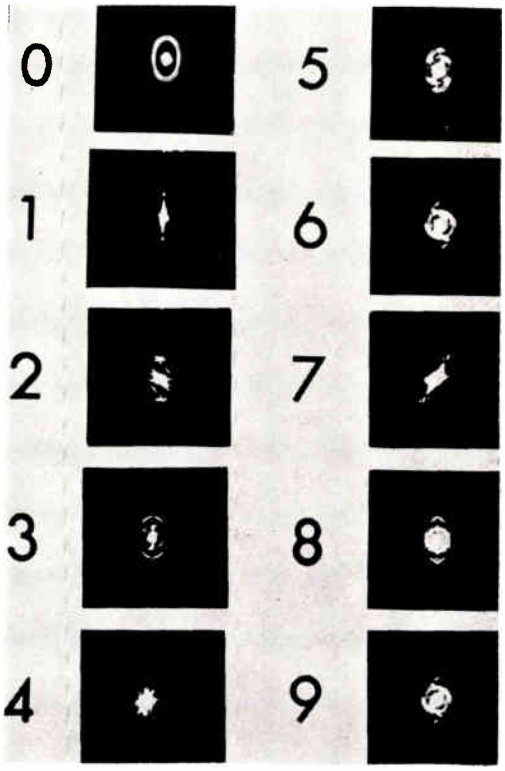


Fig. 8—Wave number spectrum of a set of numerals.

and along the W_2 direction is

$$\nu_0 = \frac{\lambda f_2}{h}.$$

It can be appreciated from the diagram that translations of the aperture A do not alter the Fraunhofer pattern or its location. The Fraunhofer pattern can therefore be considered as a representation of the input character in an exactly known location. Fig. 9 shows schematically a recognition system which compares the Fraunhofer pattern of the input with normalized comparison masks for ideal characters. The comparison masks are obtained by photographing the Fraunhofer patterns for ideal characters, being careful to maintain unity gamma for the photographic procedure. The channel normalization masks are obtained by using a pair of crossed polaroids in each channel to adjust the channel transmission by the method described in Section I. The total light being transmitted through each channel is collected and converted to an electrical signal by a suitable photo-electric detector, and identification is made by determining the channel having the maximum signal.

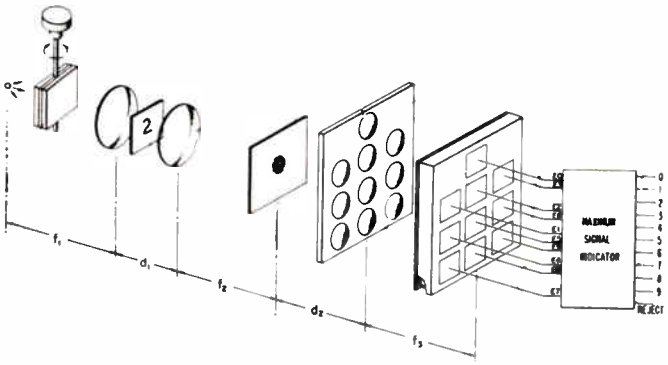


Fig. 9—Schematic of optical recognition procedure using wave number spectrum.

Other linear transformations of the form described in Section I can be carried out in the wave number space either to improve the discrimination or to improve the stability. In particular, the equivalent of the second-difference operation can be realized by inserting a transmission plate in the Fraunhofer plane which has transmission characteristics that vary as the fourth power of the wave number. In this case, the discrimination between characters in a fixed alphabet is improved and, contrary to one's intuitive reasoning, the sensitivity to random noise is essentially unchanged; however, the tolerance to systematic noise is decreased. Systematic noise in this context means the variations between two or more type styles which are very similar.

It was shown earlier that the size of the diffraction pattern was proportional to the wavelength of the source and the focal length of the lens. Accordingly, a convenient search mode can be employed to accommodate similar patterns which differ from each other only by a scale factor. In practice, it is somewhat easier to vary the wavelength by using a polychromatic source and a variable narrow band-pass filter. The band pass of a conventional interference filter can be shifted by inclining the plane of the filter to the direction of a collimated light beam. Other variable wavelength filters are discussed in most standard optic texts. A practical range for scale factor variation achieved in this way is approximately two to one.

A parallel comparison system has been described, but it is clear that the comparisons could be made sequentially if desired. Also, since the Fraunhofer pattern is inversely proportional to the character size, a practical system requires that normal-size characters be reduced to microfilm sizes in order to maintain a reasonable focal distance for lens L_2.

B. Autocorrelation Function Model

Of course, one could construct an autocorrelation function by taking the diffraction pattern of the wave number spectrum of the input, but some method of generating a transparency of the spectrum in real time

would be required. No practical method for doing this is currently known; nonetheless, an experiment of this type was carried out using photographic means to generate the transparencies. Fig. 10 shows the correlation functions for the set of numerals in Fig. 8 that were obtained in this experiment. A spurious multiple line structure is present in these functions which was shown by analysis to be caused by the limited range of the photographic emulsion used to generate the transparencies. The range of the film has the effect of passing the wave number spectrum through a low-pass filter. This situation is quite analogous to the signal obtained by passing a square pulse through a low-pass filter in a communication network. A survey of the available photographic emulsions revealed that no emulsions were available with the required range.

The above experiment was instructive in that it made apparent that the photographic construction of filters, such as the second-difference filters previously discussed, cannot be obtained with sufficient fidelity by a continuously varying photographic transparency. Construction of this type of filter will probably require a mosaic pattern in which the transmission per square is controlled by varying the size and spacing of the mosaic elements.

An optical arrangement illustrated in Fig. 11 will directly produce the autocorrelation function of the input pattern. This arrangement was described by Kovásznay and Arman.[1] It is shown in this article that the intensity distribution in the focal plane of the lens L_1 is given by

$$I(\mu_1'\nu') = \frac{I_0}{A}\int\int f(x,y)\cdot f\left(x+\frac{2d}{F}\mu'_1 y+\frac{2d}{F}\nu'\right)dxdy,$$

where (μ') and (ν') are the coordinates in the focal plane, and (x) and (y) are the coordinates in the character aperture plane. If the following substitutions are introduced,

$$\mu = \frac{2d}{F}\mu', \qquad \nu = \frac{2d}{F}\nu'$$

so that

$$\mu' = \frac{F}{2d}\mu, \qquad \nu' = \frac{F}{2d}\nu,$$

the intensity distribution becomes

$$I\left(\frac{F}{2d}\mu, \frac{F}{2d}\nu\right) = \frac{I_0}{A}\int\int f(x,y)\cdot f(x+\mu_1 y+\nu)dxdy,$$

where the size of autocorrelation function has a magnification factor $(F/2d)$.

In the above method, the peak of the autocorrelation function always appears at the intersection of the optic axis and the focal plane, independent of the location of the character aperture plate. For comparison, a well-known optical arrangement for generating cross correlations is shown in Fig. 12. The intensity distribution in the output plane is the cross correlation of the input character $f(x, y)$ and the reference character $g(x', y')$. If the input character is the same as the reference character, the intensity distribution is the same as the autocorrelation; however, in this arrangement one can see that a movement of the input causes a movement of the output. This point has been brought out to eliminate the confusion that has occurred with regard to these two methods.

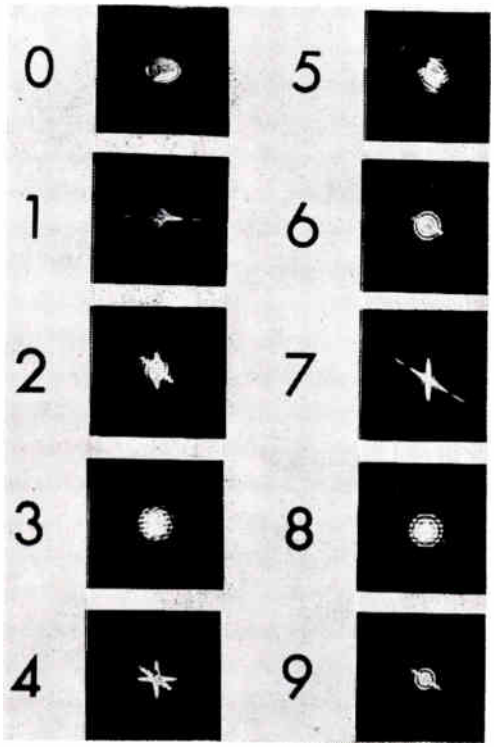


Fig. 10—The autocorrelation functions of a set of numerals generated by taking the Fraunhofer diffraction pattern of the wave number spectrum of the original input patterns.

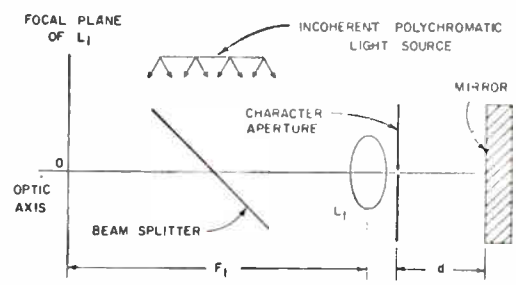


Fig. 11—Optical arrangement to produce directly the autocorrelation function of the input pattern.

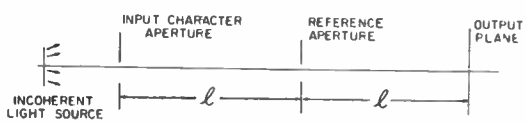


Fig. 12—A well-known optical arrangement for generating cross correlations.

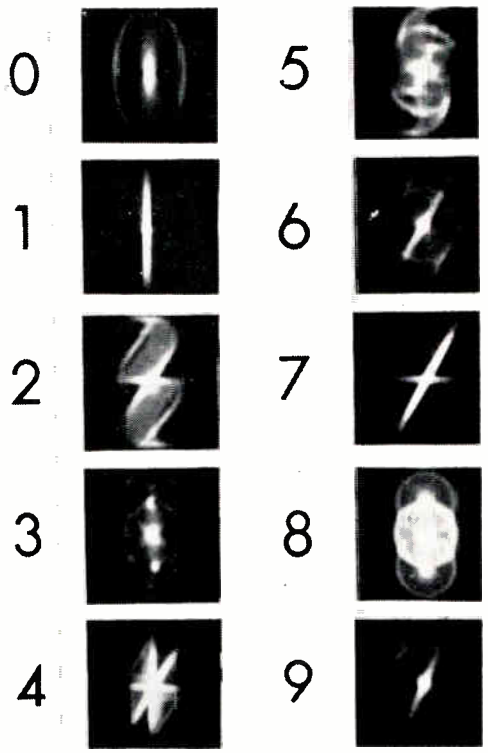


Fig. 13—The autocorrelation functions of a set of numerals generated by the device shown in Fig. 11.

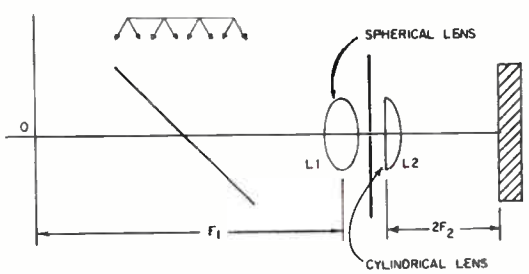


Fig. 14—Autocorrelation function generator modified to eliminate 180° ambiguity problem.

The autocorrelation function can now be used in a recognition system in exactly the same manner that the wave number spectrum was employed. Fig. 13 is a set of autocorrelation functions for the same set of numerals used previously. It was pointed out earlier that there is a 180° ambiguity problem in both the wave number spectrum and the autocorrelation function. The autocorrelation function generator can be modified as shown in Fig. 14 to eliminate this ambiguity. In this arrangement, registration invariance is maintained along the generators of the cylindrical lens, but lost in the normal direction. The intensity in the output plane is the result of autocorrelating in the direction of the generators of the cylinder and convolving in the direction normal to the generators. That is,

$$I(\mu, \nu) = \int\int f(x, y) \cdot f(x - \mu, \nu - y) dx dy$$

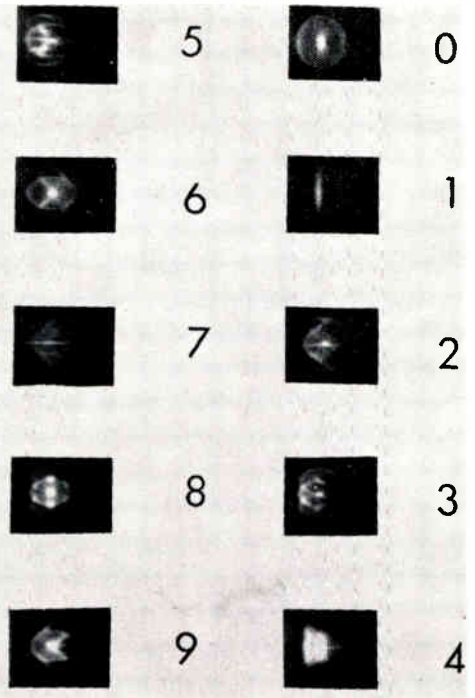


Fig. 15—The autocorrelation functions of a set of numerals generated by the device shown in Fig. 14.

or

$$I(\mu, \nu) = \int\int f(x, y) \cdot f(\mu - x, y - \nu) dx dy.$$

One may regard this physically as being the result of introducing a phase shift on the system which is constant along one coordinate and variable along the other coordinate. The particular arrangement illustrated in Fig. 14 gives the autoconvolution; however, any other phase plate could be introduced, but if registration invariance is to be retained in one dimension, the phase shift in this dimension must be constant. The autoconvolution of the set of numerals is shown in Fig. 15.

The two optical systems that have been described have certain practical limitations. These are:

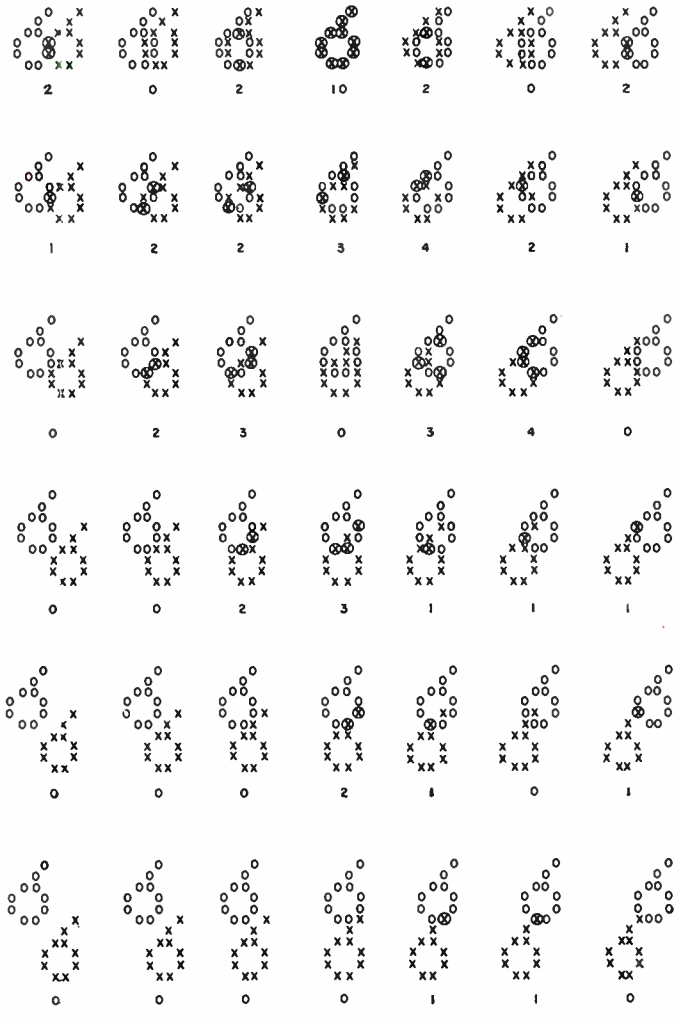
1) The operation of these systems demands thta a transparency of the character be supplied as an input.
2) Low-level light intensities are inherent to both modes of operation.

If the optical realizations are to become applicable to a large class of recognition problems, some practical method of converting, in real time, a projected image of a character from a conventional document to a transmitting input must be developed, and some method of supplying image intensification in either the Fraunhofer plane or the correlation plane must be supplied. Optical pumping techniques in solid-state materials are being investigated as possible means of solving the first problem, and phosphor technology is being investigated as a means of solving the latter problem.

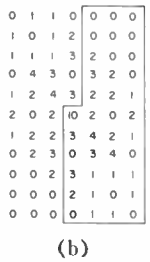
C. Electronic Autocorrelation Model

In view of the outstanding problems in the optical realizations, it became apparent that an electronic realization would be desirable to handle the more general problems. In discussing the electronic realization, a binary matrix representation of the input character will be used, and the sequential digital signals will be those generated by a vertical scan moving from left to right.

The geometrical interpretation of the autocorrelation function is that the value of the autocorrelation function at any specified point is proportional to the number of pairs of occupied points having a given displacement and direction. Physically, this is equivalent to taking the same character on two matrices and shifting one with respect to the other through all possible translations and counting the number of coincidences for each relative translation. Fig. 16(a) illustrates this procedure, and shows one-half of the autocorrelation function. Making use of the symmetric properties of the autocorrelation function, the complete function is constructed and shown in Fig. 16(b).



(a)

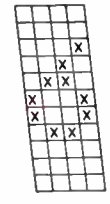


(b)

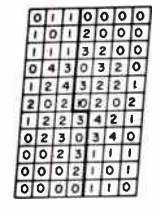
Fig. 16—(a) One-half of the autocorrelation function. (b) The complete function.

It would be desirable to define an operation on the sequential scan pattern which is the equivalent of the two-dimensional shifting operation. If one considers a skewed character matrix, as shown in Fig. 17(a), wrapped around a cylinder such that the rows are parallel to the generators of the cylinder and the upper and lower rows are adjacent members, it becomes clear that the columns of the matrix form a continuous spiral, and that the sequence of bits is the same as that formed by connecting, from left to right, the lower end of one column to the upper end of the adjacent column. A translation of the spiral along the helix retains the spatial relation between the bits, but causes a movement of the pattern both along and around the cylinder. Thus, the pattern may be placed in any desired location on the cylinder by translating the spiral. If two like matrices are wrapped around the cylinder and one held stationary while the other is moved by translating the spiral, the complete two-dimensional shifting operation described previously will be carried out. Fig. 17(b) shows the autocorrelation generated in this way, and the sequence of shifts is described by the spiral of the correlation matrix. After some reflection one can realize that if the maximum character height is N bits tall, the minimum column height must be $(2N-1)$ bits tall to prevent overlaps. The two spirals may now be considered as one-dimensional words which preserve the spatial relations under shifting operations.

The autocorrelation function of an input pattern can therefore be generated by putting the same bit



(a)



(b)

Fig. 17—(a) Two-dimensional shifting operation. (b) Where the sequence of shifts is described by the spiral of the correlation matrix.

pattern in two shift registers and counting the number of coincidences each time one register is shifted with respect to the other. Fig. 18 shows the generation of an autocorrelation function using this method. The result of not having at least $(2N-1)$ column positions is also shown in this figure. This mode of operation is not the most desirable, since there must be at least a full word separation between incoming patterns.

A more useful method, developed by McDermid, Petersen, and Shelton, of obtaining the autocorrelation function is illustrated in Fig. 19. In this structure, the first position in the register is ANDED independently to all other register positions, and the outputs of the ANDS each fed into a counter. Reading from left to right, the counter positions and the equivalent shifts are as follows:

1) Total number of bits in the pattern
2) Unit shift in $+y$ direction
3) 2-unit shift in $+y$ direction
4) 3-unit shift in $+y$ direction
5) 4-unit shift in $+y$ direction
6) 5-unit shift in $+y$ direction
7) 1-unit shift in x direction and 5-unit shift in $-y$ direction
8) 1-unit shift in x direction and 4-unit shift in $-y$ direction
9) And so forth, with every twelfth position corresponding to an additional x shift.

The values in the counters at any particular time represent the autocorrelation function of that part of the word that is in the register. After the last bit of the word moves into the register, the values in the counters become and remain stationary until the first bit in some new word enters the register.

The appropriate time to compare the function in the counters to the comparison functions is that time when the values in the counters become stationary for some specific number of vertical scans. The number chosen would depend on the nominal separation of the input.

The comparison is made by taking the scalar product of the function in the counters with each normalized comparison function. This is equivalent to multiplying each number in the counter by the corresponding comparison number in each comparison channel and summing the products in each channel. The channel having the largest sum identifies the input character. Fig. 19 shows a block diagram of this operation.

Earlier it was noted that two symbols which differ from each other only by a 180° rotation result in an ambiguous result. This ambiguity can be resolved by making use of the partial autocorrelation functions that exist in the counters as the input enters the register. In general, at corresponding times, these partial autocorrelation functions are characteristically different even for the ambiguous case. Fig. 20 is an illustration of the generation of the autocorrelation functions of a six and a nine, and it is clear that the partial functions are significantly different.

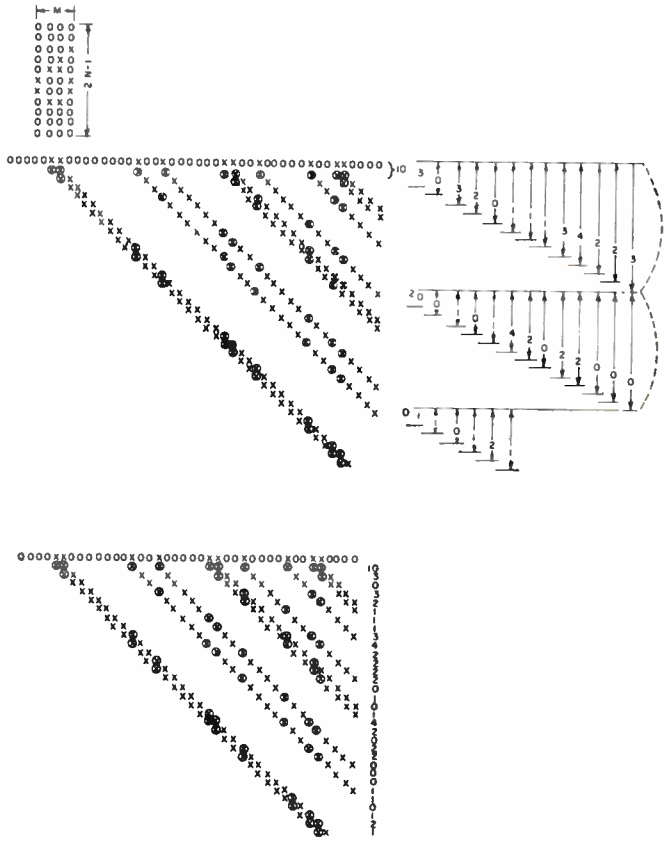


Fig. 18—Generation of an autocorrelation function by putting the same bit pattern in two shift registers and counting the coincidences each time one register is shifted with respect to the other.

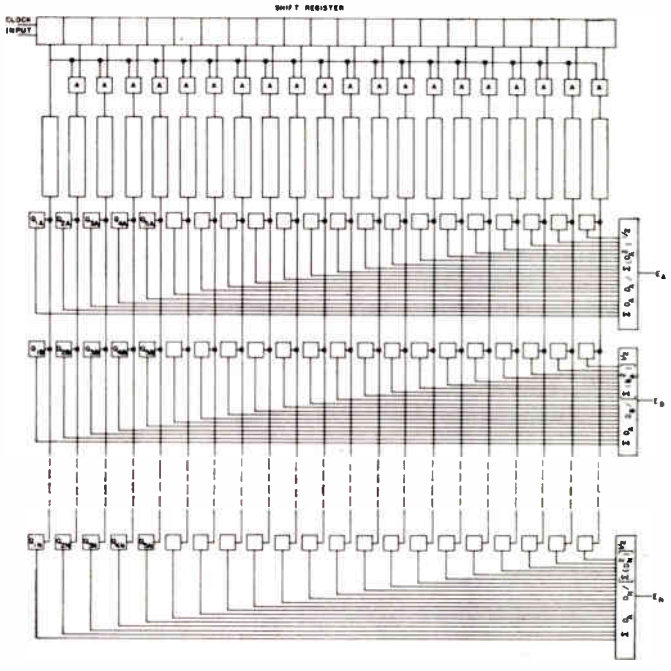


Fig. 19—Block diagram of operation. A = AND; Q_{in} = normalized reference multiplied by counter value; E = Nth channel output voltage.

Fig. 20—Autocorrelation of the numbers six and nine.

Simulated results of the system discussed indicate a good capability to handle printed characters of a large alphabet. A continuous trade between discrimination and stability can be made by use of the M operators described in Section I. Thus, multifont recognition can be realized at the cost of discrimination. There are indications that extensions of the notions described will result in improved multifont recognition and in gains toward the isolation of the character separation problem.

III. Acknowledgment

The authors wish to thank Mrs. L. Selfridge and Miss F. Reilly for carrying out the calculations referred to above.

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Computer Generated Displays*

R. T. LOEWE†, R. L. SISSON†, member, ire, and P. HOROWITZ†, associate member, ire

The need for improved presentation of computer output information is being fulfilled by a surprising variety of developments in display devices and systems. The importance of these developments in computer system design and the current lack of a coherent view of these developments indicates a need for an organized summary. R. L. Sisson and his colleagues were requested to select and summarize an appropriate set of developments, introduced by a statement of the elementary requirements of the viewer. In this paper, which is directed at the specialist and non-specialist alike, the authors adopt the system engineering approach, identifying the functions to be performed in transferring information from computer to display, and describing a variety of equipments and techniques to accomplish the transformation.—*The Guest Editor*

***Summary*—Increased use of computer output for decision-making has led to the need for effective computer-generated displays of symbols and lines in various formats. Two key functions involved in display generation are digital-to-image conversion, and image storage for projection. Symbol generation can be performed by use of logical and electron beam devices to create dot patterns, intensity modulated scans, mixtures of waveforms or shaped electron beams. Lines are generated as dots, line segments, or vectors.**

Large, bright displays are obtained by optically projecting images using CRT, photographic, electrostatic, oil film, or thermoplastic techniques. Many new developments show promise for application in computer-generated displays.

* Received by the IRE, November 2, 1960.
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Introduction

THERE have been many varied and interesting developments in the rapidly growing display field. This paper explains techniques for performing key display functions, in particular, 1) digital-to-image conversion with symbol generation, and 2) generation of large, bright displays. In reviewing this broad field, only basic principles and typical characteristics are given. The reader is referred to the Bibliography and the manufacturers for more detailed explanations and quantitative data.

Conventional electromechanical printers, conventional and storage CRT's, and individual character

readout units will not be discussed, since they are summarized in other literature [1]–[10].

User Requirements

Most data-processing systems divide the data-processing and decision-making activities between man and machine. In order to use human capabilities effectively, information must be communicated from machines to humans in a manner that permits effective human perception and comprehension. Before discussing display techniques, the general requirements which a user imposes on a display are briefly reviewed.

Update Response Time

The time between the entry of new data into a display system and the instant the results are on (or ready for) display is the update response time. In systems which display many classes of information, this time is a function of the priority given new data, the data-input rate and the processing of queues as well as the response time of the display equipment itself. Requirements vary from seconds to hours.

Request Response Time

It is important from an operational and psychological point of view that a display be created soon after the user designates the information he wishes displayed. A request might designate, for instance, the class of information, such as "airplanes, flying over 30,000 feet," and the geographic area. The request response time is considered as the time delay from request until the display appears. This is a function of the display access mechanism as well as of the display generation process.

These response times are determined in part by display writing speed for individual symbols and complete frames, and the time to remove or erase a display.

Resolution

In normal room light, the average human eye can discriminate parallel black lines, separated by intervals equal to the line width, when the line separation subtends about 1.5 minutes of arc at the eye. Thus, the eye has an angular resolving power of 40 optical lines (80 TV lines) per degree. From a fixed position, a user can see a plane display which subtends 50° at the eye. This allows the eye to make out 2000 optical lines of detail on such a display. The eye will be the limiting factor in the amount of usable information that can be presented in a display. In order to perceive further detail, the user must somehow have access to additional displays either on other surfaces or by changing the display (including magnifying portions).

Exact resolution requirements vary with contrast, brightness, "clutter," background "noise" (*e.g.*, maps), nature of use (prolonged study or occasional reference), and viewing angle.

Contrast, Brightness, Ambient Illumination

The display markings should be brighter than the background (or vice versa) or have contrasted color. Preferable contrasts in black and white display are about 30:1. In many systems the viewer will perform other tasks between display viewings, *e.g.*, writing and reading; under these conditions, the room lighting should be ample for normal office use. The display should have an average brightness close to the ambient light level to prevent eyestrain.

Fidelity

The display must allow the user to properly interpret quantitative data (*e.g.*, the distance between items or their relative position). A military ground unit, for example, should not be represented on the wrong side of a river. The necessity for proper interpretation leads to specific requirements for linearity, accuracy and registration. Distortion in a display (*e.g.*, pin cushion distortion in a CRT) must be kept to a level which will not bother the user nor cause concern as to the adequacy of the display. Character spacing and alignment must be reasonably uniform on tabular displays; lines which the user expects to be straight should appear so.

Obviously, the system must be accurate in the sense that the data displayed truly represent the data which were received from the processor. Dropped bits, drift in analog units, etc., may cause as much trouble in a display system as in a computer.

Display and Audience Configuration

Console displays, serving one or several persons, have dimensions of from 5 inches in diameter to about 2 feet by 3 feet. When used by a large group, the display screen dimensions range from a few feet on a side to as much as 20 feet on a side.

The distribution of light issuing from the display surface also is a function of the audience configuration. If the audience can be concentrated along an axis perpendicular to the display surface, directive screens may be used, improving effective brightness. If, however, the audience may be randomly situated in respect to the screen, a screen which issues light of equal intensity in all directions is desirable. The location and activities of the audience often require rear projection to avoid shadows on the screen.

Flicker Rate

The critical-fusion frequency is the frequency of light flashes which appear to the viewer as a continuous light. The critical-fusion frequency is affected by the factors of light intensity, light bandwidth, length of exposure, brightness of surrounding area and the relative lengths of "dark" and "light" cycles.

Symbology

Printouts or displays of data composed of alphanumeric characters in tabular or straight text form are the most common type of computer output for human interpretation. Requirements often exist for displaying

symbols of arbitrary shapes. Symbols provide an extremely efficient means of representing (coding) complex thoughts, objects or events. A simple symbol design often has tremendous mnemonic or associative value. A symbol no more complicated than an alphanumeric character can convey more meaning than many alphanumeric characters. Table I below shows a number of typical symbols and what they might represent; familiarity and use allow immediate interpretation. The number and complexity of symbols depend on the variety of different objects and events that must be indicated. The maximum number of different symbols is limited by the user's memory and the mnemonic value of the symbols. Requirements often exist for changing or adding symbols.

TABLE I
TYPICAL SYMBOLS

SYMBOL	MEANING	SYMBOL	MEANING
A	ALPHABETIC CHARACTER	XX 14	14TH INFANTRY DIVISION
?	QUESTIONABLE SITUATION OR PUNCTUATION MARK		SCHOOL
5	NUMERIC CHARACTER		OILFIELD
	AIRCRAFT		BRIDGE

Line Drawings

Certain varieties of data cannot be described alphanumerically or symbolically in a concise form suitable for human comprehension. These are most effectively shown directly as: lines on graphs, charts, diagrams, maps, line drawings, etc. Examples of data that are best displayed in line drawing form are: isotherms, air lanes, roads, topographic contours, weather fronts, functions of a variable, vehicle courses, satellite tracks, radii of coverage.

A display of area information is occasionally necessary. Examples are: mine fields, fallout hazard areas, swamps, areas of sales responsibility, and areas on charts or graphs. Areas can generally be well represented by lines and symbols; however, shading or color is sometimes more clear.

Formats

The format of a display refers to the positioning of information within the display. A *fixed* format is one in which the location of various elements of data are predetermined and cannot vary. Tabular information is commonly in a fixed format. A *free* format is one in which the position of any element of information is not fixed and may depend on the information itself. The display of aircraft location within an air traffic control system is an example.

Even free format displays generally have a frame of reference, which may be a map, grid lines, a block diagram or flow chart. The variable data are usually superimposed on the particular frame of reference, and some display systems need only a single format or frame of reference. The capabilities of data-processing and storage systems, however, can provide many different types of display data very rapidly, in which case the displays should show the various format headings or reference backgrounds as needed.

Other Requirements

Each display system will have many other requirements regarding methods of coupling to the processor, the use of colors, halftones, dynamic displays, 3D, physical characteristics, economics, flexibility, and reliability. All such requirements should be understood prior to display system selection or design.

With these types of requirements in mind, certain basic display functions can be reviewed.

Display Functions

Fig. 1 shows a consolidation of functional flows for meeting the display requirements of a particular system. Any path from left to right through Fig. 1 is a possible functional flow.

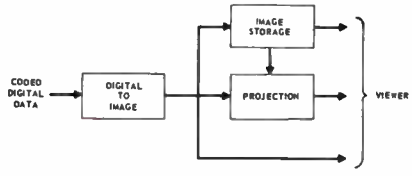

Fig. 1—Typical composite functional flow.

For each functional flow, a system may be designed by proposing implementation of each function with a feasible technique. For each function, generally several techniques exist, so many system configurations can be examined. These functions are, broadly speaking, either of two things. One is conversion between one form of information-carrying media and another. Typical media are: digital pulse sequences, analog signals, electron beam motions, electrostatic charge patterns and modulated optical beams. The second type of function is the conversion of signals representing symbols and lines to the visual images that a human interprets as the symbols and lines. It is assumed that information is provided to the display system in coded digital form which identifies what is to be displayed and where it is to be displayed.

The digital-to-image conversion function, in particular, converts coded digital descriptions of symbols and lines into visual images directly, or via such intermediate media as patterns of electrostatic charges, photochemical changes, or oil film thickness variations. Symbol generation, inherent in most digital-to-image transformations and a vital display function, can be accomplished by many techniques reviewed below. This re-

view also illustrates the various digital-to-image conversion methods.

Symbol Generation

Symbol generation is the process of converting a coded digital description of a symbol to an image of that symbol. Table II summarizes characteristics of representative symbol generation techniques.

One method uses logical circuitry to convert from the digital symbol code to a matrix of wires energized in a pattern forming the symbol image. Symbol shape information is stored in the logical circuit, and the resulting image is in the form of a voltage or current pattern in a matrix of wires. The wires can be energized simultaneously, column by column, row by row, or one by one (scanning). Sensitized paper (*e.g.*, electrography) may be utilized as the visual output.

Electromechanical printing and individual digital readout devices are also symbol generators, but since they are covered adequately in the literature, they are not discussed further here.

There are many methods of deflecting an electron beam to form symbols and characters. Several such methods are illustrated in Figs. 2–7. The electron beam may be directed at a phosphor, a Schlieren medium, or a charged surface (as in electrostatic printing tubes, storage tubes, or scan conversion tubes). Most of these symbol generators can be classified by 1) the manner in which the beam is deflected and intensity-modulated, or shaped, and 2) the manner in which the symbol shape data are stored.

Dot Pattern Methods

The symbols are made up of patterns of individual dots as shown in Figs. 2 and 3. Individual points are exposed by positioning the beam to a given x-y coordinate and unblanking the beam. This is analogous to an electromechanical point plotter. The digital coordinates of each point are converted to analog form to deflect the beam. When the beam has stabilized, it is unblanked. Methods of storing and selecting the dot coordinates for symbols are:

1) Store coordinates of dots digitally in the computer memory or in separate magnetic drum or cores. Feed these digital coordinates to a digital-to-analog converter to obtain deflection signals.
2) Store the dot coordinates in analog form in a resistor network (Fig. 2) [11]. Logical switching circuitry selects the appropriate resistor sequence using the digital symbol identifier and sequentially scans the x and y resistance combinations to get the analog deflection signals.

Scanning Methods

Partial rasters and other scan patterns may be used with appropriate intensity modulation. For a fixed scan pattern, the symbol shape can be stored as intensity signals in: 1) a core array (Figs. 3 and 4), 2) an optical image or stencil (Fig. 5), or 3) a drum.

With core symbol storage, every point of the symbol may be stored (Fig. 3), or just the end points of scanning line segments (Fig. 4) [12], [13]. In Fig. 3 the video intensity signal is obtained from the readout wire as

TABLE II
Symbol Generator Techniques

Method of Forming Symbol	Method of Storing Symbol Data	Resulting Signals	Typical Rate Symbols/Second	Method of Changing Symbols	Typical Units
Dot Pattern	Logic Circuits	Pulses on Wires		Replace Circuits	READ
	Drum, Cores, or Computer Memory	Digital Dot Coordinates	25,000	Rewrite Digital Memory	dd 16
	Resistor Net Plus Logic	Analog Dot Coordinates	25,000 to 75,000	Replace Resistor Cards	DOTitron (Fig. 2)
Scanning	Specially Wired Core Planes	Binary Raster	10,000 to 50,000	Replace Core Planes	SM I, II (Fig. 3) Vidiac (Fig. 4)
	Drum plus Logic	Binary Raster	10,000	Rewrite Digital Memory	FLIDEN
	Image Mask	Binary Raster		Replace Mask	(Fig. 5)
Waveforms or Strokes	Sinusoidal Generators plus Logic	Video x, y, z	25,000	Replace Circuits	(Fig. 6)
	Linear Generators Plus Logic	Video x, y, z	20,000	Replace Circuits	Digitron
	Resistors, Transformers	Analog End Point Coordinates		Replace Circuits	
	Drum or Cores	Digital End Point Coordinates	1,000	Rewrite Digital Memory	Dataview (Fig. 7)
	Image Mask	Video x, y, z		Replace Mask	
Beam Shaping	Image Mask	Shaped Beam	20,000	Replace Tube	Charactron (Fig. 8)

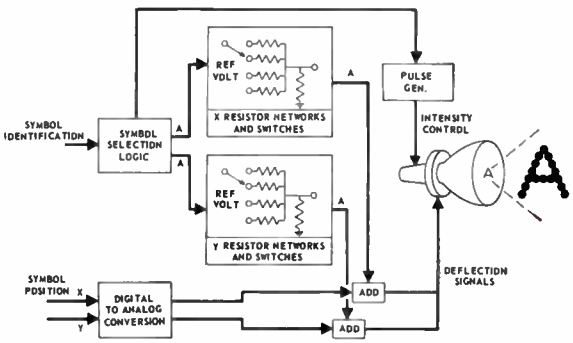

Fig. 2—Dot pattern symbol generation with resistor storage.

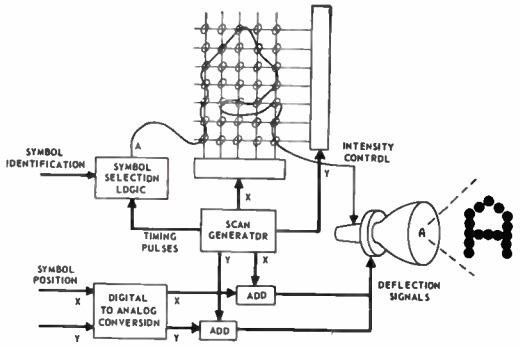

Fig. 3—Dot pattern symbol generation using scanning beam and core storage.

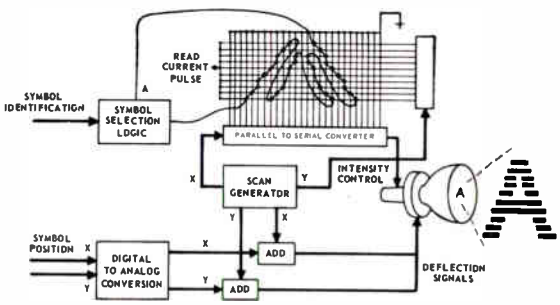

Fig. 4—Scanning symbol generator with core storage.

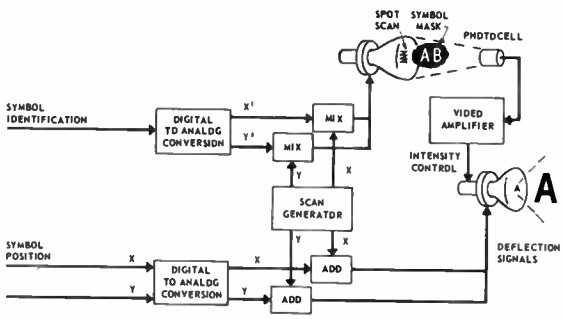

Fig. 5—CRT mask symbol generation.

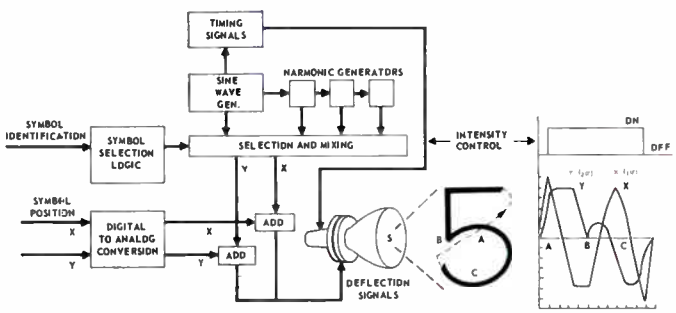

Fig. 6—Symbol generation by analog waveforms.

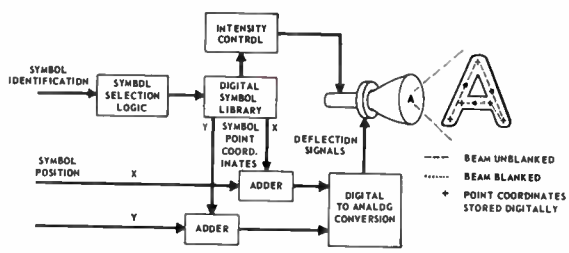

Fig. 7—Line segment end point symbol generation.

the cores are interrogated in a pattern corresponding to the beam scan pattern. The partial raster or scan pattern is superimposed on symbol-position deflection signals. In Fig. 4 the signal from the first core in a line turns the beam on and the second turns it off.

The method shown in Fig. 5 stores symbol shapes on a mask in front of a separate CRT. The video signal is obtained from the photocell as the CRT spot is scanned over the selected symbol in the mask which modulates the light from the spot striking the photocell. Another method replaces the optical system in Fig. 5 by an electrostatic system, in which the mask contains symbols formed of secondary emitting materials. The secondary electron output resulting from scanning the surface forms the intensity signal. The resulting intensity signal is then used to modulate the output electron beam which uses the same scan signals. Gross positioning signals are different for the two beams: in the symbol mask CRT, they select the proper symbol on the mask; in the output CRT, they position the selected symbol properly on the resulting image. Another version of Fig. 5 uses a separate small CRT for each character [14].

Another partial raster method stores shapes as binary rasters, in drums or cores. The scan pattern forms at least seven adjacent horizontal lines. The beam is intensity modulated by pulses along the lines to form the symbols, each composed of a 5×7 array of spots, for example. Conventional logic is used to select and mix the intensity pulses for each symbol or row of symbols.

Waveform Generators

In these methods, three parametric analog waveforms form the x and y deflection and intensity signals for the symbol, using the electron beam much as a pencil is used to draw out characters and symbols. Some of these methods are commonly called "stroke" methods, since

the beam acts much like a pencil. Again the symbol shape data may be stored in several different manners:

1) The symbol shape may be stored in circuitry which includes sine wave and harmonic generators, with clipping, phasing, blanking and the necessary selection logic [15]. To select the proper set of waveforms and blanking signals, a logic network sets up transformer or resistor mixers (as shown in Fig. 6) from the digital symbol identification. This device is often called a Lissajous symbol generator.
2) Waveforms may be generated by mixing positive and negative ramps for x and y and controlling intensity. This forms specific straight strokes with the electron beam. Character descriptions are stored in individual circuit cards which tell when to add or subtract ramps to x and y deflection signals in accordance with timing signals.
3) Symbol shapes can be stored digitally within or external to the computer as coordinates of end points of straight line segments that describe the symbols (Fig. 7). These are selected from the symbol code by logical circuitry and fed to a digital-to-analog converter which drives the deflection circuits. The deflection circuits provide the sweep between the coordinate points. Blanking signals are stored with the point coordinate data. In this method and in the dot pattern method, with digital storage of dot coordinates, storage and logic can be performed in the computer. This may reduce the complexity of external equipment while increasing the computer processing load.
4) Coordinates of end points of line segments describing symbols may also be stored in analog form in resistors or transformers along with logical circuitry for selecting the proper coordinates [16].
5) Waveform data may be stored in image masks (one for x and one for y for each symbol) similar to Fig. 5, except that deflection as well as intensity signals are obtained from the stored image for each symbol. The image is selected by deflection and then followed to form the video waveforms. The curve on the mask may be followed either by a "servo" circuit which keeps the beam on the edge of the mask or by reading the mask with an oscillating sweep and rectifying the output.

In several of the above methods, the linewidth can be determined by superimposing a wobble or small Lissajous of high frequency on the CRT spot.

Beam Shaping

Symbols may be formed by shaping an electron beam. A stencil mask in the electron beam path is the symbol shape storage. Beam deflection selects the proper symbol in the mask and the beam is extruded through it. The resulting shaped beam is then recentered and deflected to the position the symbol is to occupy in the display image. This is the method used in the CHARACTRON Shaped Beam Tube [17], [18] shown in Fig. 8. The Compositron stores symbol shapes on a photoemissive cathode, the desired symbol is selected electrostatically and the electrons are emitted as a shaped beam.

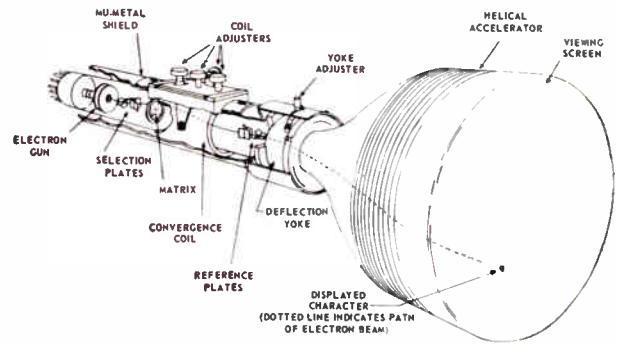

Fig. 8—Charactron-shaped beam tube.

Line Generation

Techniques for generating arbitrary line drawing are not as plentiful as those for symbol generation. There are only two basic types, simultaneous x and y deflections (curve tracing) and dot patterns. Scanning techniques are seldom, if ever, used to generate line images from digital data. Lines are occasionally represented in binary raster form, in data-processing systems, if the line data were initially obtained by scanning images.

One method of generating lines is by selecting enough points to define each line or line segment mathematically. The points must be located close enough to define curves and corners sufficiently accurately to meet requirements. Straight line segments may be drawn between points, as described above under symbol generation (Fig. 7). Another technique which might be termed a vector method describes a starting point and a sequence of direction and distance vectors. Both of these methods can be applied to electron beams, or electromechanical stylii.

Lines can also be generated by defining enough adjacent points to form a continuous line, as in the dot pattern symbol generator method illustrated in Fig. 3. Points need not always be connected, since dotted lines can be quite effective. Coarse lines may also be generating sequences of symbols to form a line.

Cathode-Ray Tubes

The above methods may be used with any of the wide variety of CRT's available [19], [20]: direct view, high-resolution, storage, color, projection, flat tubes, and various special-purpose tubes. Stranix [4] and Allard [7] provide good summaries of special-purpose CRT's. If a CRT is used for direct viewing, it must either be a direct view storage tube [21] or the image must be regenerated frequently enough to avoid objectionable and fatiguing flicker. Since the image must be repeated about 30 times per second, a high symbol generation rate is required. If an image is to contain 1000

characters, the character generation rate would have to be greater than 30,000 per second.

Projection Displays

In recent years many requirements have arisen for displays much larger than can be obtained using direct view CRT's. Several types of projectors have been developed for projecting directly from a CRT [22]. Brightness, however, is reduced proportionally to the increase in area plus any optical inefficiency. This has resulted in development of a wide variety of projection displays designed to provide bright, large-screen, computer-generated displays. The first step in many such devices is to convert from digital-to-image form using an electron beam as described above. The image created by the electron beam is then transferred to and/or stored on a medium suitable for projection. Methods of accomplishing this conversion are discussed next. Table III presents some typical characteristics of image storage media used for projection.

Silver Halide Photography

Conventional photography using silver halide light-sensitive emulsion is, of course, a common method for storage and a common projectable medium. The demand for rapid response for computer displays has been met by development of very rapid photographic processing techniques. Using special films and processing chemicals, along with elevated temperatures and special methods of applying processing chemicals to the film, the complete negative development has been automatically performed in less than four seconds. Rapid photo-processing techniques may be classified by the manner in which the processing chemicals are applied to the film.

The spray-processing method sequentially sprays developer, fixer and wash onto the film within a single processing chamber. Another method forces the three processing liquids sequentially into a very thin chamber adjacent to the film. Entry of one solution forces the preceding one out of the chamber. The use of three sequential baths at three different stations is perhaps closest to conventional processing. One such method uses a saturated sponge-like applicator instead of placing the film directly in contact with the liquids. The monobath technique uses a single solution containing all necessary processing chemicals; these chemicals have response time characteristics such that developing, fixing and washing take place in the proper sequence. This solution may be applied to the film by passing the film over a saturated applicator. Still another method uses a special film backing which contains dry monobath chemicals in contact with the film. After exposure, water is applied to the dry chemicals, and the monobath process proceeds. These automated processes can provide excellent quality results with resolution and contrast rivoling conventional processing. Processing times vary for the different methods from about 3 seconds to about 15 seconds. An automatic color photo-processing system suitable for computer output has been developed which processes the film in about 8 minutes.

Kalfax Photography

This photographic technique uses a diazo material on a film base. Exposure to ultraviolet light creates a latent image of pressure centers in the emulsion. Upon heating above 212°F, the emulsion softens and the pressure centers expand into small gas pockets several microns in diameter. When projected, these small bubbles cause reflection and scattering of light rather than selec-

TABLE III
Typical Characteristics of Image Storage Media Used for Projection

Technique or Media	Resolution Optical Lines per mm	Contrast Ratio	Time to Expose Spot Seconds	Developing Time	Decay Time
Silver Halide Photography Black and white	50–200	1000:1	$10^{-6}-1$	< 5 seconds	Permanent
Color	100			<10 minutes	Permanent
Kalfax	200	25:1[1]	0.5	< 1 second	Permanent[2]
Electrostatic Photoconductor	25–100	1000:1	10^{-4}	0.5–2 seconds	Permanent
Direct charge deposition	10	1000:1	10^{-6}	0.5–2 seconds	Permanent
Schlieren Oil film	1000 TV Lines, Total		10^{-6}	0	0.03–10 seconds
Thermoplastic	100		10^{-6}	0.02 second	Permanent
CRT Phosphors	20–40	30:1[3]	10^{-6}	0	1.5 μsec–0.1 second

Notes:
[1] Contrast ratio in projected image may be 200:1 using proper projector design.
[2] If not subjected to several hour fixing or special processing, may degrade in projector.
[3] For normal viewing, can be several orders of magnitude higher if desired.

tive absorption as in silver halide film. Relatively low contrast in the film may be enhanced to greater than 200:1 contrast in the projected image by proper projector design, so that little of the scattered light is intercepted by the projection lens. Kalfax does not have great enough light sensitivity to be exposed directly from a high-speed CRT trace. It requires considerable ultraviolet light for exposure with peak sensitivity at 385 millimicrons. The development with heat can be accomplished in less than one second. Normally, Kalfax must be fixed for approximately two hours to prevent formation of gas bubbles in the previously unexposed diazo when placed in a projector. Special techniques, however, have been developed to eliminate the need to fix, in some applications.

Electrostatic Techniques

Several methods produce the image in the form of an electrostatic charge pattern as an intermediate step. One method uses a CRT to produce and focus a light image on a uniformly-charged photoconductor. Where the light strikes the photoconductor, the conductivity is increased and the charge is dissipated in that area, leaving a charge pattern on all areas not exposed by the light image. This latent image is made visible by powder development, as described below.

Two photoconducting materials being used in this technique are zinc oxide [23] and vitreous selenium [24]. The zinc oxide can be applied as a coating to a film or other carrier. The selenium photoconductor is a shiny solid convenient for reflective projection. Selenium has higher light sensitivity and resolution than zinc oxide, but its characteristics are destroyed if heated above 125°F. There are methods for transferring the charge pattern from the photoconducting surface to a film or paper base more suitable to certain types of handling and display; however, resolution is slightly degraded in such a process.

Another method applies a charge pattern to a dielectric paper or film directly from closely-spaced wire ends as the medium is pulled past the wires. The resulting charge pattern is then powder developed. The wires may be activated by logical circuitry [25], [26] or by an electron beam in a special type of CRT [4], [27]–[29], as shown in Fig. 9. The special CRT has either a line or mosaic of thin, closely spaced wires extending through the tube face. This allows charges from the electron beam to be applied directly to a carrier in contact with the tube face as shown. The wires are made as thin as 0.001 inch and are spaced 250 or 500 per inch.

The latent image consisting of a charge pattern on a photoconductor, film, or paper material is developed by bringing a charged powder into contact with the charge pattern. The powder adheres to the charged areas forming a visual image. The powder may be brought into contact with the surface by means of a brush, powder cloud, cascade or liquid. The powder image may be erased or transferred to another medium, allowing the initial charged medium to be reused. The powder image may be permanently fixed by application of heat, pressure, or a transparent adhesive. Thermal fixing may be provided by a thermoplastic coating on the medium or by a thermoplastic toner in the powder.

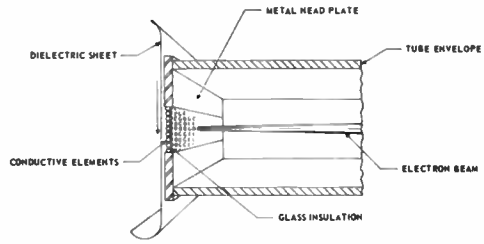

Fig. 9—Electrostatic printing tube.

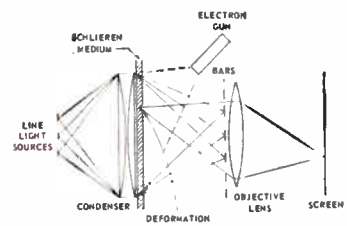

Fig. 10—Functional diagram of a modified Schlieren projection system.

Schlieren Projection

Fig. 10 illustrates a modified Schlieren projection system [22], [30]. This uses variations in the refraction of a light beam caused by a Schlieren medium to create an image. The deformations or ripples are formed in the Schlieren medium by electrostatic forces after the medium is bombarded by an electron beam from a conventional electron gun.

If there were no deformations in the Schlieren medium, the line light sources would all image on the corresponding bars in front of the objective lens and no light would pass through the bars to the screen. Deformations in the Schlieren medium produce varying refraction and cause light from the deformation to pass through the bars. Since the objective lens forms an image of the Schlieren medium on the screen, deformations or ripples in the Schlieren medium appear as light spots on the screen. The Eidophor projector uses a thin oil film as the Schlieren medium [22]. The viscosity of the oil film provides storage times similar to long-persistence phosphors. Thus, the image must be continuously regenerated by the electron beam. A thermoplastic tape may also be used as the Schlieren medium [30]. This tape has a transparent conducting coating covered by a thin coating of thermoplastic material which melts when heated. The electron beam produces a charge pattern on the thermoplastic. This latent image is developed into deformations by melting the thermoplastic. The charges are attracted by the potential, depressing the thermoplastic. The deformations are fixed by cooling, thus freezing the deformations in place and obviating regeneration. The film is reusable after being erased by heating.

Other Projection Techniques

A projection display system has been developed which uses small individual projectors for each symbol. Each projector can select, on instructions from a computer, 1 of 128 symbols from a disk by rotating the disk until the proper symbol is in the light path. The symbol image is positioned on the screen by moving the lens according to position signals received from the computer. Color is provided by placing filters in the light path. The projectors are modular so that a large number may be placed in a bank to allow simultaneous display of many symbols. This technique provides a high brightness and a dynamic capability, and does not require regenerating a complete frame if only one symbol has changed.

The Iconorama projection technique [22] records a line image by scribing a line with a stylus in an opaque metallic coating deposited on a transparent medium. The resulting transparent line is projected in a conventional optical system. The stylus is mounted on a transparent holder and remains in place during projection, providing a dynamic display capability. The stylus is driven by servos as in an x-y plotter. The recording medium must be replaced when the track is completed or when the image is cluttered with old lines. Color is provided by placing a filter in the light path. Multiple projectors can be used simultaneously with the images superimposed on one screen.

Light Generation and Color

Light generators perform either of two functions: 1) they provide a static, uniform light source which is modulated by other devices, such as a photographic transparency; or 2) they provide an extended light source in the shape of the desired image, such as with a CRT or electroluminescent panel. Since light generation is a fundamental function in displays, several basic phenomena are reviewed briefly below. These phenomena can be classified by the source of energy, thermal or radiant, and whether or not the phenomenon exhibits "inertia" (rises and decays slowly) as follows:

Source	No Inertia	Inertia
Thermal	Arcs, glow discharges	Incandescence
Radiant (luminescence)	Fluorescence	Phosphorescence

Incandescence: Many substances emit light when heated, most effectively by passing an electric current through the material or through an adjacent heater. Incandescent lamps react slowly to changes in current because of thermal lags and are not useful as modulated emitters. They are common as projector lamps. Typical lamps produce 800 to 38,000 lumens with efficiencies of 10–20 lumens per watt.

Electric discharge: An electric current passing through a gas will cause it to produce light under proper conditions. These sources range from small glow discharge neon lights producing about 1 lumen per watt to very large arc lamps. Short arc lamps filled with mercury and argon or xenon or just xenon are effective projector sources. Typical lamps provide 1000 to 125,000 lumens at efficiencies of 10 to 50 lumens per watt. The lamps are compact and provide small source dimensions.

Phosphorescence: In this form of luminescence, energy is absorbed by a material and is reradiated over a period of time extending after the input ceases. The sources may be narrow-band light (for example, ultraviolet) or an electron beam. CRT phosphors are of this type. Phosphorescence performs the function of conversion from electron beam to optical form. Phosphors can be activated in very short times—fractions of a microsecond. Persistence varies with type of phosphor from about 1.5 μsec to about 0.1 second. The brightness obtained from phosphors varies over a wide range, depending on the phosphor and accelerating potential. A typical TV tube provides highlight brightness of about 50-foot lamberts while theatre-type projection kinescopes can provide 25,000 foot lamberts.

Fluorescence: Some materials will emit light at a given frequency when subjected to an alternating electric field—*electroluminescence*—or to light of another frequency—*photoluminescence*. The most important effect for display systems is electroluminescence (EL) [31]. In its usual form, an EL "phosphor" powder is embedded in an insulator and placed between two electrodes, one of which is transparent. Upon application of an alternating electric field, light is emitted from the phosphor. The brightness increases with voltage and frequency, 2500 foot lamberts having been achieved while 2.5 foot lamberts are produced at 110 volts, 60 cps. Efficiencies of about 10 lumens per watt have been achieved. Conventional fluorescent lamps provide about 65 lumens per watt.

Brightness: The brightness of a projected display depends on the intensity of the source, the light efficiency of the optics, and any modulation medium (e.g., film), the size of the projected image, and the screen gain (directivity). One of the highest intensity projector lamps available has an intensity of 70,000 candles. The light efficiency of a typical projector is about 5 per cent. This light intensity and efficiency would provide 3500 lumens in the useful light beam. This, divided by screen area, gives the illuminance on the screen expressed in foot candles. Multiplying by screen gain (typically from 1 to 5) gives the apparent brightness in a certain direction expressed in foot lamberts.

Color: The basic phenomena producing color are: 1) light sources having a spectral distribution producing the effect of color, *e.g.*, monochromatic; 2) selective absorption in which a material absorbs certain wavelengths and either reflects or transmits other wavelengths; 3) interference effects causing certain wavelengths to be reflected while others are transmitted (as in dichroic mirrors which serve as high- or low-pass filters); 4) dispersion caused by an index of refraction which varies with wavelength, as in prisms; and 5) diffraction gratings.

Electroluminescent Panels

There are several types of electroluminescent (EL) storage display panels under development [32], [33] which utilize arrays of small individual cells which emit EL light in the desired pattern. To avoid requiring continuous or repetitive triggering or excitation, each cell is also a storage element. The main differences in the basic types of EL storage display panels are the means of triggering the storage cells and of providing the storage function.

In the Sylvatron EL display panel [34], the basic storage cell is a combination of photoconductor and EL elements, as illustrated in Fig. 11. The cell has two stable states; when the EL element is not emitting light, the potential drop across the photoconductor reduces the potential on the EL element so it cannot emit light. The cell is triggered by applying an external light to the photoconductor element. This reduces the potential across the photoconductor and increases the potential across the EL element, thereby causing light to be emitted, part of which impinges on the photoconductor maintaining this condition. A large panel with many cells may be triggered by a light pattern exposed on the rear of the panel. Such a light pattern may be generated by another EL panel attached to the rear of the storage panel which is excited by a crossed wire grid and has no storage feature.

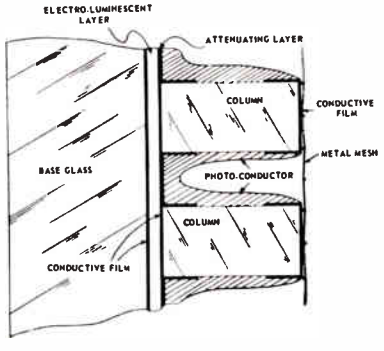

Fig. 11—Portion of electroluminescent photoconductor storage display panel.

In the "ELF" (electroluminescent ferroelectric) display panel [35], [36], each cell consists of a combination of ferroelectric and EL dielectric materials, with semiconductor layers serving as triggering diodes. These elements are combined so that the nonlinearity of the ferroelectric dielectric causes the triggering signal to vary the amount of excitation applied to the EL layer, providing a storage time of about 5 seconds. Storage times of 15 minutes are possible for the screen alone, without the triggering feature. These panels produce a brightness of 10 foot lamberts at 400 cps and 400-volt excitation. A contrast ratio of 50:1 is achieved with a triggering potential of 200 volts. At 400 cps, the life (to half brightness) is about 1000 hours. About 5 gray scale steps can be provided. The resolution is 16 elements per inch, or 256 per square inch. A panel of over four million elements is under development. The writing speed is about 1 element per microsecond.

Miscellaneous Phenomena

There are many phenomena that have various degrees of promise in the display field. Several of these are described below; however, this is not a complete summary. There is considerable development effort in other phenomena, including electrophotography, polarized phosphors [37], image intensifiers [32], [38] and light modulators [39].

A group of chemicals called "Scotophors," which become light absorbing when an electron beam impinges on them, are available. The beam path is thus easily seen in reflected light. This phenomenon is used in "dark trace" devices.

It is possible to cause a thin film of semiconductor material deposited on a transparent base to become transparent when charged by an electron beam. Thus, the thin film can be used to modulate a normal light source in a projection system.

A group of "photochromic" dyes are becoming available which are transparent or colorless in their "normal" state. When exposed to a narrow band of light, *e.g.*, ultraviolet, the materials become visible as colored, relatively opaque areas. The persistence ranges from a fraction of a second to many hours. Photochromic materials may be reused after erasing with light of another wavelength or heat. When properly placed in a light beam, the photochromic film will modulate the beam and result in a colored image.

Somewhat similar to the photochromic dyes are the "electrofluors" [32], [33]. These liquids are observed to fluoresce when a voltage is applied in presence of ultraviolet light, or may appear colored by the subtractive absorption of white light. This activity is caused by an electrolytic reaction in the liquid.

A form of light valve or electro-optical shutter is the "Kerr cell" and its equivalents. In this, a crystal or liquid is contained in a cell which is inserted into a light beam. The transmissivity of this cell is controlled by the electrical potential charge across it. Thus, voltage inputs can modulate the intensity of the beam passing through it. The normal Kerr cell consists of a glass vessel filled with nitrobenzine with two electrodes. An electric field applied between the plates causes the fluid molecules to polarize, changing the transmissivity to polarized light. The polarization is proportional to the square of the voltage applied. The Kerr effect increases as temperature decreases. The Kerr cell will operate at a speed of 10^{-8} seconds.

Conclusions

There are many techniques for accomplishing the basic functions shown in Fig. 1. Various techniques may be combined in many different ways to form display systems meeting a wide variety of requirements. Fig.

12(a) lists several possible alternatives for direct viewing by individuals or small groups. Some systems use magnetic storage for one frame of data. Any of the various symbol generation techniques may then be used with a CRT for display. Instead of magnetic storage for image regeneration, image storage after digital-to-image conversion may be performed using hard copy or display storage tubes (see Fig. 1).

Where large audiences must be accommodated, a projection technique may be used, as is illustrated in Fig. 12(b). The image may be projected directly from a CRT or oil film or it may be projected from one of many types of image storage media.

For any set of requirements for computer-generated displays, there may be a number of feasible functional flows and a number of techniques for each function. Careful analysis of the many possible combinations should lead to a very effective computer-generated display within the present state-of-the-art.

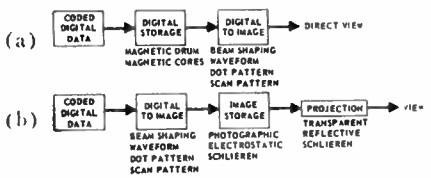

Fig. 12—Several typical functional flows and implementations.

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Digital Data Communication Techniques*

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Reliable digital data transmission is of fundamental importance to the over-all performance of the giant electronic networks now being built, in which digital computers are major elements. J. M. Wier has been commissioned to prepare an introductory paper on the data links in such networks, identifying the major elements of a digital data communication system, and describing and comparing techniques currently employed or being developed for mechanizing these elements, primarily in the domestic commercial installations.—*The Guest Editor*

Summary—**The majority of digital communications are now carried on the teletypewriter networks. New modulation techniques, higher transmission speeds, and more effective error control schemes are being provided in systems now being introduced in the digital communications area. A considerable body of theoretical work has been completed which provides a base for most of the activity in the field; however, application of much of this work, until recently, has often been uneconomical in the current state of the art. This is most notably true in the case of error control and the practical achievement of theoretical channel capacities, but the problem also arises in other areas. The work towards a truly automatic central data processing system has been slow, but a number of projects are now showing the way in this area. These include reservation systems, centralized banking, central inventory control, air traffic control, and, above all, centralized military communications and control systems.**

I. Introduction

WITH the introduction of computers and the promise of the "great tomorrow" to be wrought through the use of the central data processing concept, a good deal of attention has been devoted to the communications requirements of central data processing installations. Actually, the subject of digital communications, even electrical digital communications, obviously has been of some importance for a long time. The dots and dashes of early manual telegraph were clicking out digital messages more than a century ago. Still later, but far before the advent of electronic computers, the automatic punches, printers, readers, and paper tape handling devices of the teletypewriter system were carrying a growing load of commercial and government traffic in record communications. Even today, more messages are carried over the teletypewriter network than on all of the more recently introduced digital communications systems combined.

In the early days of computers, it was recognized that the truly remarkable computational and control abilities of digital computers and data processors could advantageously be concentrated in large central locations in order to integrate the operation of large organizations and systems. This concept is still being pursued today, but a more realistic examination of the entire system has been made so that the problems and costs of such an organization are known as well as the advantages. One of the more important parts of this problem is the communication system which provides the connections to the central system from all of the outlying locations. This paper explores the status of the digital communications field with an eye to using this information to explain "why we are here" and what lies ahead.

A discussion of digital communications naturally centers around the elements which make up such a system: the data source, the modulator, the transmission channel, the demodulator, the data sink, the timing or synchronization unit, and the error control equipment. Each of these elements will be discussed in sufficient detail to give an insight into the current state of the digital communications art. Unfortunately, because of the scope of the problem, some areas and some specific devices are certain to be slighted in a paper of this size. For this, the author apologizes in advance and hopes that such instances are relatively few in number.

II. The Basic Digital Data Communication Problem

As with other forms of communication, the basic problem in digital communication is that of carrying information from one point to another. In this case, however, the information is of a special sort in that only certain discrete forms for the various possible messages are used. Such messages are made up of collections of symbols, each one of which is selected from a finite alphabet of symbols. Since such a message would seem to be simpler to discern at the receiver than one which could assume infinitely many values, digital communication would appear to be simpler than, say, voice or television transmission. To a certain extent, this is true. However, certain complicating factors arise in practice.

First, the usual speech or television signals are already highly redundant by the time that they are presented to the communication channel. This means

* Received by the IRE, October 19, 1960.
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that some of the difficulties of transmission can be ignored because the person listening to the speech or watching the television picture can take over the task of interpolating whenever the system falters momentarily. On the other hand, with digital messages it is often found that this inherent redundancy is missing. The message frequently does not represent the normally redundant speech found on voice connections, but rather some seemingly random collection of symbols. This fact makes it necessary to provide some other way of dealing with transmission difficulties.

Second, largely because of the redundancy present in most nondigital material, the actual rate of information transfer attempted in this case is not such as to push the capacity of the communication channel. On the other hand, since digital material is often not so redundant, the channel is stretched considerably further. As an illustration of this, it has been estimated that the information rate used in voice transmission does not exceed fifty bits per second. In comparison, a digital data transmission rate of a thousand bits per second in the same channel is common and this has been pushed to three thousand bits per second in special cases.

A third complication, somewhat related to the first one, is that no reasonable counterpart of the human receiver is present in many data cases. Thus, whatever cleverness may be necessary to obtain a reasonable copy of the received message must be provided in the form of hardware. For all but the simplest cases, the provision of such built-in ingenuity is quite complex and, consequently, costly.

Nyquist's Analysis

The subject of communications over a digital channel has been investigated theoretically for some time. In the late 1920's Nyquist wrote a now-classic paper on the subject, in which he analyzed a channel used for digital communications [34]. He established a condition which relates the bandwidth of the communication channel to the speed of transmission for so-called distortionless transmission. As most of the digital communication devices currently in use operate in a manner which is described by Nyquist's analysis, it is worthwhile to consider this study for a moment.

Nyquist established that it is possible, subject to a few idealizing assumptions, to transmit two bits per second of digital information for each cycle per second of channel bandwidth, while maintaining at least one position in each bit in the digital waveform at the receiver in a form which is not influenced by other bits in the message. This means that a sampling spike placed at that one undisturbed point could ascertain the bit present with no ambiguity (noise considerations being ignored). Nyquist further showed the conditions under which this sort of operation is possible. In practice it is found to be difficult to realize the conditions laid down by Nyquist because of the difficulties of providing the required channel. This is particularly true for switched connections, for the channel changes from connection to connection so that what constitutes proper channel equalization for one connection may be entirely wrong for another.

For instrumentation reasons, almost all of the digital communication devices known to the author operate in a way which is generically related to the process described by Nyquist. A discrete-valued (usually two-valued) waveform is presented to a transmitting modulator for translation into a form suitable for transmission through the required channel. After transmission, a receiving demodulator reproduces this waveform in the best way that it can and the resulting waveform is then examined in order to ascertain the state which is present. A considerable number of variations on this theme exist, but few of them offer a fundamentally improved approach.

The Shannon Approach

In more recent times Shannon has presented a different point of view [41]. It does not consider the so-called distortionless transmission case, but examines directly how much information it should be possible to pass through an idealized channel when the channel is limited in bandwidth and disturbed by noise. It is shown that for sufficiently long messages, with a random digital content, it is possible to transmit at a rate, C, the channel capacity, in a channel with a bandwidth, W, when the signal-to-random-noise power ratio is S/N. The relation connecting these quantities is

$$C = W \log_2 \left(1 + \frac{S}{N}\right) \text{ bits per second.} \qquad (1)$$

where W is in cps. This transmission may be carried out, in theory, with an arbitrarily small error rate.

Eq. (1) yields the same transmission rate as does Nyquist's analysis (2 bits per second per cps) for a signal-to-noise ratio (SNR) of three. As the SNR is usually considerably higher than this, Shannon's calculation of capacity usually exceeds that found from the Nyquist analysis. Unfortunately, unlike the Nyquist approach, the demonstration of (1) is carried out without indicating a practical means for achieving the given result. Furthermore, it is possible to show that there is no method of reducing the error rate to an arbitrarily low value when the message is of fixed finite length, and still maintaining the given transmission rate. It appears, however, that some considerable gain might be made by investigating the matter more thoroughly. It is to be expected that the required transmission terminals may be very expensive and therefore it may not be practical to carry out such an operation for other than demonstration purposes. This is true since, in many cases, it is less expensive to provide more communication channels than to pay for excessively expensive terminal equipment.

Typical System

Typically, a digital communication system is represented diagrammatically in much the same way as any other form of communication system. Fig. 1 presents this diagram.

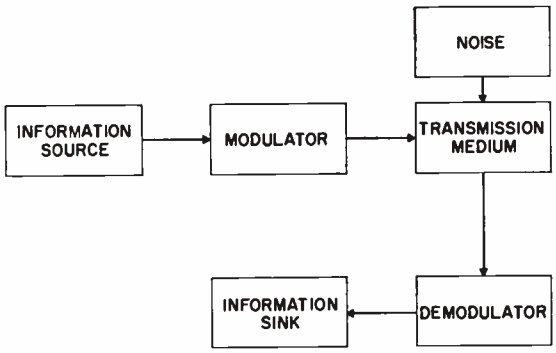

Fig. 1—A typical communication channel.

Information is provided by some source, in this case in digital form. This information is presented to a modulator which translates the digital waveform into a signal wave which will pass through the transmission medium with a minimum of difficulty. Such a translation usually involves the generation of a signal with a frequency spectrum which may be carried easily through the selected communication channel.

The transmission medium carries the signal from the point of origination to its destination. In the process, various noise sources in, and coupled to, the medium cause extraneous interfering signals to be added to the signal wave. In addition, imperfections in the transmission properties of the channel cause the signal wave to leave the transmission medium in a form somewhat distorted from that in which it entered. This distortion usually takes the form of variations in the transmission loss and delay as a function of frequency, although other types of disturbance also occur.

The signals leaving the transmission medium are presented to the receiving demodulator for translation back to the original digital waveform, or an approximation thereto. The demodulator operates on these signals and attempts to ignore the disturbances caused by the passage through the transmission medium, and to reproduce the digital waveform in an undistorted form at its output. The properties of the demodulator which further this end will be discussed later when modulation is considered at greater length.

The information sink is the destination for the digital information. It usually takes the form of some type of recording device such as a printer or magnetic tape unit. However, more sophisticated units such as on-line computers may also be used.

In addition to the major elements of the system, at least two other parts have a prominent effect in practice. These are the timing system and the error control portion. In the more detailed discussion which is to follow, these will be covered as separate sections in addition to the more obvious elements shown in Fig. 1.

III. Modulation and Demodulation

As has been indicated, the function of the modulation system is to translate the digital information to be transmitted into a form which will pass through the communication channel, preferably with the greatest efficiency. The term "greatest efficiency" deserves some further explanation. For the purposes of this discussion, it will be taken to mean that the modulation method used goes as far as it can toward meeting the following list of desirable properties:

1) It must represent sequences of digits as waveforms acceptable to the channel (necessary).
2) It should make possible a high rate of sending information.
3) It should generate waveforms which differ recognizably from the prevailing noise.
4) It should be suitable for a variety of similar, nonideal channels.
5) It should be simple and inexpensive.

We shall consider each of these points in turn in discussing the general modulation problem for digital communication. Further, to be concrete, we shall, at least for this discussion, consider the transmission of a serial sequence of binary symbols.

The most fundamental requirement placed on the modulation system is that it must represent the information to be sent over the channel in some distinguishable way. Thus, to represent a serial sequence of binary digits, a sequence of two-state signals must be produced which will pass recognizably through the channel. Usually this means that the sequence has a certain frequency range in which all of the essential signal components fall. Further any idiosyncracies which the channel may have must not result in ambiguities being introduced into the message. As we shall see later, certain relatively common "side properties" can cause some of the common modulation systems to fail.

In order that a high information rate be achieved, the discrete modulated signals should occupy a short average time. Again restricting ourselves to binary transmission, this means that each of the two binary signals should be designed to be as short as possible, consistent with restrictions enforced by available bandwidth, reasonable demodulator simplicity, and adequate error performance.

In order to operate advantageously in the presence of noise, the difference between the line signals and expected noise should be exploited to the maximum to reject the noise in favor of the signal. The most common ways of doing this are to distinguish the two by differences in their spectra and in their phases. Further improvements are possible when the statistics of the

noise are known, for then the demodulation system may be able to use these statistics to improve the noise rejection ability.

Commonly the available channels which are useful for communication purposes have certain defects which work to decrease their desirability. These defects, among others, are: amplitude and phase distortion as a function of frequency, channel nonlinearities which create cross-modulation products with other channels in the same carrier system, sudden changes of circuit loss due to malfunction, certain types of human interference, small frequency translations and phase jumps. As will be discussed in the individual modulation cases, these difficulties have more importance for some modulation systems than for others.

It is axiomatic that any modulation system should be as simple as possible, consistent with achieving the desired objectives. It is often the case, however, that certain of the properties which are necessary in the ideal system may be compromised somewhat in the interest of economy. Thus, an extremely high transmission rate may not be so important as a saving in the modulator terminal costs. Similarly, a certain amount of noise advantage attainable by some desirable modulation scheme may not make the difference between a system's being satisfactorily useful and its being unusable. In fact both of these properties are seriously compromised in nearly all of the systems which have been built to date.

In discussing the general subject of modulation it is simplest to talk about the modulation for a binary signal. As most of the current systems may be treated in this way directly, very little loss on generality is incurred. Furthermore, other discrete systems usually perform in ways readily deducible from the binary case.

Voltage Level Modulation

Probably the simplest form of modulation for a binary information sequence consists of a simple two-voltage representation in which "ones" are represented by one voltage level and "zeroes" by another. This is, of course, a form which is relatively popular in computer representation. It is also a form which might not be considered as modulation in some senses, but here "modulation" is taken as nearly synonymous with "representation." In any case, this form has one very desirable property: for a given information rate, the bandwidth required for transmission in this form is less than with most other modes of modulation. For the sake of comparing the speed capabilities of the various modulation systems, the bandwidth requirements of this form of signal representation will be taken as standard. Other systems will be compared to it in this property. It is this representation that Nyquist used in establishing the requirement of one cps of bandwidth for each two bits per second of binary data speed.

Unfortunately, for transmission this representation has one serious drawback. Such a representation has a dc component for most messages. Thus the channel for carrying such signals must have the ability to carry dc. All radio circuits and most carrier systems are thus disallowed.

Regardless of this difficulty, such a scheme of transmission was used on early telegraph circuits and is still used, in many cases, on the local loop segments of modern teletypewriter systems. Since this representation requires less channel bandwidth for a given bit rate than most other modulation schemes, its use will probably grow where it can be employed. It is a common form for providing electrical signals to other modulation systems. It is also being used in the wire line transmission of voice by pulse code modulation.

Having disposed of an obvious representation of binary signals, let us forego any discussion of other representations which also require a dc component. This removes a number of pulse systems from further consideration.

Double-Sideband Amplitude Modulation

Most of the modulation systems used in digital communication systems are simple two-state particularizations of standard modulation systems. Perhaps the simplest one of these uses double-sideband amplitude modulation. With such a system, one of the binary states is customarily represented by the presence of a sinusoidal carrier while the other state is represented by its absence. Such a system is characterized by a tolerance to noise which is on the same order as that found in the simple dc representation case. This is particularly true when the obvious and simple envelope detection scheme is used. The performance can be improved by using suitable filters to remove noise outside of the band and by integrating over the duration of each of the binary signal elements. These complications, however, are currently considered better applied to some other form of modulation which stands a better chance of performing well in the presence of noise. Furthermore, since this system represents the binary waveform in each of its two sidebands, it requires twice as much bandwidth as the dc voltage representation. Although this modulation system possesses the above-named disadvantages, it is relatively simple to instrument and was therefore used extensively in early systems. Some of these include early carrier telegraph systems and early IBM card transceivers.

Vestigial Sideband Modulation

One of the obvious ways of improving the abilities of the amplitude modulation system just described calls for the removal of one of the information-carrying sidebands which is present in the double-sideband case. Since all of the essential information is present in each of these sidebands, there is no loss of content in this process. However, some practical difficulties must be considered. In the first place the carrier must be preserved to recover the dc component of the information

envelope. Thus, instead of going to a complete single-sideband system, digital systems of this type use vestigial sideband modulation in which one sideband is retained, a portion of the carrier is kept, and a "vestige" of the other sideband is retained. This is usually done by producing a double-sideband signal and filtering out the unwanted sideband components. The result of these operations is that the signal now takes only about three-fourths of the bandwidth required of a double-sideband system. However, with simple envelope detection, the noise margin has been markedly reduced. This is true because the depth of modulation must be decreased, relative to that of the double-sideband case, in order to avoid excessive distortion of the demodulator output. The effect of this distortion may be reduced in the detection process by using a system of synchronous detection [7]; however, this process is sufficiently complex that no presently announced system utilizes the scheme for digital transmission.

Perhaps the outstanding example of the use of vestigial sideband for digital transmission is the SAGE system [38], [44]. More recently, a highly developed vestigial sideband system has been announced by Rixon Electronics, called the Sebit 25 [50]. Here some of the noise penalties are reduced in importance by careful filtering. Furthermore, special equalization is used to aid in getting maximum channel utilization.

Frequency Modulation

Perhaps the system which yields the next simplest modulation and demodulation equipment (after double-sideband amplitude modulation) is frequency modulation. In this case the two binary states are represented by two different frequencies. Binary signals represented in this way are usually detected by using two frequency-tuned sections, one tuned to each of the two bit-frequencies. The demodulated signals are then averaged over the duration of a bit and the results compared in order to decide which binary state is present. Such a system is somewhat less sensitive to most of the noise forms which exist than the simple double-sideband amplitude modulation (DSBAM) scheme. This follows from the general frequency sensitivity of the detection process which tends to reject frequencies which are not like those of the signal. From an intuitive examination it is apparent that one might expect the FM signals to be more durable, for an FM system has a complementary DSBAM representation of the binary wave about the two binary signal frequencies. In practice, however, to make good use of the bandwidth available, these two frequencies are placed so close together that the lower sideband of the upper frequency overlaps the upper sideband of the lower one.

Carrier telegraph systems using FM have been built by Western Electric, North Electric, Western Union, and Collins Radio, among others. Other FM systems of greater bit rate capability have also been constructed for use in wider channels [47].

Digital transmission using FM has a number of advantages and is a good compromise for many of the less than perfect, but rather good, applications. It is less sensitive to noise, operating as well as a DSBAM system with 3 to 5 db less SNR for white noise when both are utilized at bit rates which tax the channel. The instrumentation has been streamlined until it is not much more complex than an AM system. Furthermore, since the received signals can be amplified and limited at the receiver, a simpler receiving amplifier can usually be used than with AM, which requires a somewhat sophisticated automatic gain control system if it is to operate over a wide range of circuits. If FM has one disadvantage, it is that it requires slightly more bandwidth than DSBAM, although the difference is small indeed in practice.

Phase Modulation

The modulation system which is currently getting the most thorough investigation is probably phase modulation (PM). A two-phase system operates by using one phase of the carrier frequency for one binary state and another phase for the other. These two phases are usually 180° apart. The two phases are generally detected by using a reference signal at the receiver which is of known phase with respect to the incoming signal. This signal is of the same frequency as the incoming carrier and is usually arranged to be exactly in phase with one of the binary signals and 180° out of phase with the other.

The demodulation process is carried out by multiplying the reference signal times the informational signal and integrating over the bit duration. In practice, it is usually arranged for this integration to be carried out over an integral number of cycles of the carrier frequency. This condition causes the integral to be uniform in size for all carrier starting phases. Pure polarity is adequate to distinguish one binary state from the other in the demodulator output using this process.

One of the more useful advantages of this form of demodulation is that it is frequency-sensitive in such a way that the largest output is obtained when the signal is of the same frequency as the reference and of the same phase as, or 180° out of phase with, that reference. Other frequencies are attenuated with respect to this one, and other phases, even of the same frequency, are also attenuated. In fact it may be shown that if purely random signals are put into this process, half of their power is ignored on phase considerations. This is true in addition to the frequency discrimination present. Such a condition means that this demodulation scheme is very good at selecting the signal out of a noise field. Further, it may be shown that such a system yields a smaller noise bandwidth, the longer the period of integration is allowed to be. Thus, an even more improved noise performance can be obtained with such a system if the transmission rate requirements are such as to allow a sufficiently long period of integration.

Thus far only the advantages of phase modulation have been indicated. In practice a number of associated problems arise which must be given special consideration in order to arrive at a working system. The most important of these is that somehow the reference signal must be made available at the receiver. This is usually done by deriving such a carrier from the signal elements in some way. One way of doing this for two-phase binary modulation is to full-wave rectify the signal wave, thus stripping all of the binary modulation off the signal and leaving a collection of unidirectional, half-sinusoidal loops. These have a strong component at the second harmonic of the carrier frequency. This component may be used to drive a circuit which is tuned to the second harmonic and oscillator in phase with this component. By counting down from this signal, a frequency is obtained which is equal to that of the desired reference. This carrier is either in phase of 180° out of phase with what the desired reference should be. Once this ambiguity is resolved and the recovered carrier is locked into the correct phase, such a signal usually holds solidly in this phase as long as the signal is present, provided that the noise is not extremely large for some extended period, an event which is not too likely under most circumstances. A second difficulty exists in phase systems. Where the channel provides small frequency shifts, the reference signal may get out of frequency and phase with the information signal. This causes a degradation in the detection process.

The system described next is less troubled by this difficulty. A second and perhaps more popular way of operating a phase modulation system uses what is called a relative phase system. Typically, a binary "one" is represented by sending a signal of the same phase as that of the previous signal sent, while a binary "zero" is represented by a signal of a phase opposite to that of the previous signal transmitted. These signals are demodulated at the receiver by storing each signal for one bit period for comparison in phase with the next signal element. The same process as that described previously is employed here except that the reference signal is merely a delayed version of the previous signal. No problems of phase ambiguity exist with this system.

Both of these systems have been used and perform very well in the presence of noise. They are both somewhat more complex to instrument than the AM and FM systems. The stored reference system, since it uses a previous signal as a reference, has somewhat more noise difficulty (about 1 db in practice), since the reference also has noise on it. In general, however, both systems perform better than typical AM and PM systems, although the margin is not too large in actual practice. With typical instrumentations the phase systems will operate at the same level of error rate with from 1 to 3 db less SNR than an FM system, and with from 5 to 7 db less than an AM system.

As a final comment, phase systems may be operated with limiting receiving amplifiers, just as is the case with FM. A small noise penalty is ideally paid in the demodulation process itself, but the sometimes difficult problems of automatic gain control present in linear amplifiers are avoided.

Quadrature Phase Modulation

In addition to these modulation systems, a number of more complex ones have also been used recently. Perhaps the most complex of these is the Collins Kineplex system [9].

It has been known for some time that it is possible to phase multiplex two binary channels onto one tone by placing them in phase quadrature. Thus, two bits may be placed in the frequency space which was used for one in the simple binary case. Kineplex equipment further extends the state of the art by placing two binary channels on each of several tones spaced throughout the voice band of a typical telephone circuit. By using a synchronous detection scheme, the demodulation process can both select one phase in each channel from its quadrature mate and also reject the contributions from all of the other tone channels. Thus Kineplex provides a high degree of transmission efficiency, but it is extremely complex to implement.

Another special modulation system which shows some promise as a result of the extreme simplicity of the transmitting circuit is described by Edson and Flavin [10]. With this system two or three frequencies are transmitted at the same time. Each of these frequencies is selected from a different set of four distinct frequencies. Each frequency, at any time, may thus have one of four values and a pair may have any of sixteen state values. With a three-frequency system, sixty-four state values are available. Thus an alphabet of 4^n symbols may be sent during each transmission interval in this way, where n is the number of sets of four frequencies employed.

Summary of Modulation Systems

In summary of the various modulation systems which have been and are being used, a few general comments may be made. Firstly, from the standpoint of simplicity of implementation, the different standard systems may be arrayed in order of increasing complexity as AM, FM, and PM. Their tolerance to noise, in order of increasing tolerance, is identical to this. Finally, as far as bandwidth required for a binary channel of a given speed is concerned, AM and PM take about the same amount of channel while FM requires slightly more than these.

In selecting one of the systems for a given application, two additional general observations seem worth making. First, it is difficult to improve performance in transmission speed and in noise performance simultaneously. Second, for many purposes, many of the technical properties of the modulation system are of no importance, since it is frequently true that only one figure of merit, economy, is of paramount importance. Any

reasonable working system is adequate. This will be further emphasized in the discussion of the noise problem, where it is found that in some applications one modulation system is not, for practical purposes, much more useful in guarding against noise than another.

IV. Noise, Filtering, Error Control, and Coding

As has been previously mentioned, digital communications must be more carefully protected from error than must some other forms of communication. Therefore, more careful consideration is generally given to the subject of accuracy than is the case with other systems.

Noise

Of prime importance in any discussion about error control is the form of the interfering noise which may cause the errors. Generally speaking, noise in the digital communication field is divided into two categories: white noise and impulse noise. Of course, both of these are band-limited in real channels. White noise is characterized by a flat frequency spectrum with equal contributions from all frequencies and with the various components having random phases. For calculation purposes it is generally sufficient to know only its average power and that the noise is "white." On the other hand, the term "impulse noise" is not nearly so definite. Conceptually, impulse noise is made up of a collection of randomly-sized impulses. However, by convention, impulse noise has come to mean the noise which reaches the receiver as a result of the presence of various short disturbances in the communication path.

These two types of noise vary in their importance from one communication medium to another. White noise is of negligible importance on wire circuits, while on radio circuits, particularly during a fade, it may be a most serious source of difficulty. Impulse noise is the greater problem on wire circuits.

Since the exact statistical form of white noise is known, its ideal effect on digital communications is fairly simple to compute. On the other hand, a similarly accurate description of impulse noise is not as yet available. This is partially because not as much data have been taken on it, but it is probably more attributable to the way the noise is categorized. Although it is assumed that all such noises originate as sharp spikes, other short-time phenomena also cause the prime disturbances which appear in the circuit as "impulse noise." The result of this is that accurate statistical descriptions of impulse noise are not available, and, even when they become so, they will probably be so complex that they will be difficult to use.

Even though accurate descriptions are not available, a number of interesting and useful facts are known about the impulse noises in the voice frequency telephone network. In the first place, they have very low average power on the whole. Second, the noise which appears will be correlated with itself over a time at least on the order of the reciprocal of the bandwidth and often for considerably longer than this. Finally, the noise often reaches very large values when it occurs, so that errors are very likely to appear at that time, no matter how good the filtering and detection process.

Error Control

We began discussion of the subject of error control in Section III, and pointed out that the demodulation process can aid in rejecting noise in favor of signals, thus improving the basic error rate.

It is, of course, also possible to remove various parts of the frequency spectrum by using a filter with the proper response. By matching the filter characteristic to the signal spectrum, the signal can be maximally emphasized with respect to the added noise so as to improve the error performance. In practice this is usually done in addition to the other operations which help to improve the error behavior.

The more standard method of protecting a digital information channel against changes made by interfering noises involves the insertion of redundant digits. These digits are added with certain constraints placed on the possible sequences which may appear in the encoded message. Since these constraints are known at the receiver, it is possible to determine there whether a certain class of errors has occurred in transmission. This class of errors may be made as broad as desired, provided a suitable encoding scheme is used. In practice, of course, an attempt is made to make this class similar to that which is caused by the noise in the channel.

For ease of calculation of the additional digits at the transmitting and receiving points, it is desirable that the relations dictating them be as simple as possible without making the process ineffective. Perhaps the simplest sort of constraint which has been used is the parity relation, in which an additional binary digit is added to a binary group so as to make the number of binary "ones" in the augmented group either always odd or always even. Such a system of encoding may be used to detect some odd number of errors in the group. However, the check is ineffective when an even number of errors occurs in a check group.

By suitably designing the encoding scheme it is possible not only to detect the presence of an error, but to isolate and thus correct it. Such a process is described by Hamming, among others [25]. General schemes for using combinations of such checks are given for actual location and correction of an arbitrary number of errors. Such processes require more and more additional binary digits as the scope of the check improves.

A more general form of error correction can be provided by using a table look-up process at both the transmitter and receiver. This process can be used to carry out any type of error correction or detection. However, instrumented in this form, the mechanisms involved will generally be much too complex for economical use. Simpler processes such as the parity check system, the counting of "ones" in a group, and simple arithmetic

operations are more convenient for practical use. Furthermore, the results using these simple systems may be made sufficiently good to make other schemes less necessary.

The effectiveness of an error control system is usually measured in terms of how much the system improves the error rate and reduces the efficiency. Systems which are capable of dealing with large numbers of consecutive errors are also considered as being good. Error detection systems for doing this may be obtained for an inexorbitant investment in circuit complexity. Error correction systems are often completely out of the question because of the presence of long bursts of errors. Thus, there is a tendency in the digital communication field to provide error detection of a very high order and to correct the erroneous material by retransmission. Perhaps this is most frequently done by making use of collections of interlaced parity groups. Such interlaced groups are arranged so that the individual bits of a group are separated by several bits in the message sequence. The intervening bits are members of other check groups. Providing this interlacing process is carried far enough, even completely catastrophic failure will still be detected with a very high probability, for the resulting random sequence of binary digits will be very unlikely to satisfy all of the various parity checks simultaneously.

As a result of tests of transmission over telephone circuits, a number of facts are known about the effectiveness of some of the more common codes when used in telephone circuit applications. Alexander, Gryb and Nast [4] present a good deal of this information. Some of the facts which have been ascertained about such codes are the following. Simple parity checks in which the members of the group being checked are all in sequence in the message are usually ineffective because error bursts cause a high probability of local error correlation. An improvement by a factor of no more than two to four is typical. Similarly, systems of fixed count coding, in which the number of "ones" in a group is always constrained to be the same, are similarly inadequate when the members of the group fall in sequence. These are marginally better than the simple parity check system, however. The recurrent burst-correcting codes originated by Hagelbarger are found to improve the error rate only a little more [24]. Suitably interlaced parity checking can be made as effective as desired, but the complexity of the equipment to instrument the process may rise to rather high levels. It is also true that a number of forms of interlaced code can be made similarly effective. However, the costs again tend to rise.

The foregoing discussion stresses one important point of view. The effectiveness of any coding system in an error environment as mentioned above is not dependent so much upon the actual assignment of values to the various characters involved as upon the arrangement of the parts of the check groups within the message. Thus, the actual selection of these codes has not turned out to be very complex in practice, and for this reason very little practical use has been made of most of the extensive body of theoretical work which has gone on in this field of information theory. (A representative but not complete bibliography on this subject is included among the references.)

As a matter of interest it should be pointed out that the few commercial systems now available for data communication use methods of error control which take at least some of the above facts into account. The IBM 7701 tape-to-tape system uses a combination consisting of a four out of eight fixed count character code (in a noninterlaced form) along with a longitudinal parity check by level in the eight-level code. The later check provides for an interlacing of eight different parity check groups at any time. These codes are used only for detecting errors, not for correcting them. The correction is done by retransmission.

The RCA DaSpan system uses two parity checks per character plus an interlaced parity check over a block. It too detects and retransmits.

The early IBM Card Transceivers used a slightly different system which still takes advantage of knowledge of the error pattern. This system uses a four out of eight coding system. However, it also uses an AM modulator. In such a modulation system, it is very much more likely that errors will occur from the no-carrier state to the carrier state than the other way around. This being so, the probability of a compensating error in the four out of eight system is very low.

Analog Error Control

In addition to the process of coding noted above, there is a method of achieving a similar result, which can be carried out in the channel rather than by using the bits in the digital portion of the system. This method works as indicated in Fig. 2. It will be recognized as a simple frequency multiplex system. The original serial message is collected together into parallel groups of bits (in this case, groups of 5). Each of the bits of a group is now transmitted, in the same band as before, in a nar-

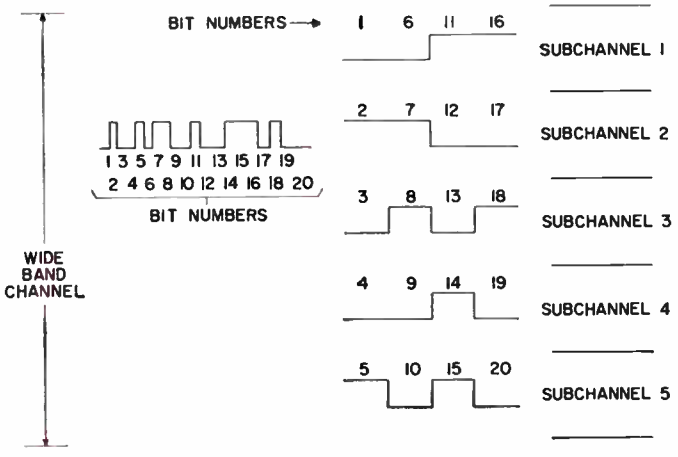

Fig. 2—A frequency-multiplexed data channel.

row subchannel of the total channel. This is done by frequency-dividing the channel into as many subchannels as there are bits in the group. Of course, each one of the bits in the narrower-band channels will now be longer than it would have been in a purely serial channel by a factor which is equal to the number of bits collected into the group. Furthermore, since there is a maximum total channel power limitation in most cases, the instantaneous power in each subchannel is less by about the same factor.

Now, let it be assumed that a burst of impulse noise occurs in the channel carrying these signals. The energy of this interference is divided among the various channels in nearly equal proportion in the typical case. Since the signal power is smaller per channel, the instantaneous SNR is the same as before. However, because the individual signals now last longer than they did before (so much so that they have the same total energy per bit transmitted as when the signal was a serial one), the interfering energy per bit is reduced by a factor equal to the number of subchannels, assuming the original disturbance is not longer than one bit. Thus a larger interfering pulse will be required to cause an error, and, if enough subchannels are used, the likelihood of having error-free transmission becomes quite good. The limiting case of this process is, of course, when an entire message is sent in parallel in this way.

To bring the entire matter of error control into a unified perspective it should be pointed out that the various systems used to reduce errors all have at least one thing in common. They all attempt to minimize the effect of the noise in some way. Filters and modulation do this by selectively removing the noise. Error control does it by attempting to average a lot of good bits, resulting from low-noise transmission, against the relatively few expected bad bits. For this the code groupings must, with a high probability, be arrayed throughout the message so that only a few bad bits fall in any group.

Error Statistics

In order to give a feeling for the expected performance of a digital communication system when used on the telephone network, a number of general conclusions drawn from Alexander, Gryb and Nash [4] seem useful. In stating these facts it should be remembered that, in this area, a good number of qualifications must be applied to all such data. However, the following general comments seem warranted.

1) The tests, which were carried out by using a frequency modulation system, indicated that successful transmission in this mode at up to at least 1200 bits per second can be achieved on the large majority of switched connections by using a compromise equalizer to correct the more usual forms of line distortion.
2) The error rates are better on low loss circuits than on high loss ones, and therefore generally better on shorter circuits.
3) The error rates are such as to require some form of error control where really great accuracy is necessary.
4) With nonzero probability a circuit with a nearly arbitrarily high error rate can be found, but circuits with fewer than one error in 10,000 bits are by far more common. Over half of the circuits yielded fewer than one error in 100,000 bits.
5) Somewhat poorer error rates are achieved at higher transmission rates, but errors are not markedly worse until line distortions nearly destroy transmission by means other than noise.
6) With reasonable error control schemes the undetected error performance can be improved to something on the order of 1 error in 10^9 bits transmitted.

In addition to the simple statistics on error rates, this test program attempted to determine enough about the error distributions to ascertain how various error control schemes would operate. This was done by making a continuous recording of the incidence of errors and no errors, bit by bit. It was found that:

1) Most of the errors are single isolated errors.
2) A sufficient number of multiple errors occur so that single-error control schemes do not improve the error rate by even as much as a factor of 10.
3) Error detection with retransmission is probably more efficient in most cases and is almost certainly less expensive.

From the preceding discussion it may be inferred that some form of error control is to be desired where really accurate transmission is necessary. As yet, however, the problem of providing this control is an economic rather than theoretic difficulty. In order to cope with the localized correlation of errors which is found in practice, it is necessary to provide either some form of interlaced grouping or a rather powerful multiple error correction or detection scheme. Either of these methods requires a good deal of equipment for adequate instrumentation by the methods now used. (By definition, "a good deal of equipment" means that the error control circuitry has several times the complexity of typical modulator-demodulator equipment.)

V. Synchronization

For a data communication system to operate properly, it is necessary that the sending and receiving devices have some agreement as to how fast the information is to be sent. Coordination in this respect is provided by the synchronization equipment. At the transmitter some form of clock times the introduction of the data into the communication channel. At the receiver, a device is present which, either by some form of *a priori* timing knowledge or by examination of the arriving signal wave, times its treatment of the signal

wave so that each data bit is neither lost nor reproduced more than once at the receiver.

Generally, synchronization systems are classified as either synchronous or asynchronous. Synchronous systems provide for a uniform speed of digital transmission so that no more time is taken for one bit than for any other. An asynchronous system may operate with unequal periods for the individual bits.

In the typical system a number of timing periods must be used. Bit timing, character timing, and often block timing must be accurately maintained. A single clock with separate but related timing for bits, characters, and blocks is usually employed.

Synchronous Timing

A system with synchronous timing uses an accurate clock at the transmitter. This clock times the bits, characters, and blocks in their presentation to the line and tells the data source how fast to feed information to the line. At the receiver some means must be found to anticipate just how fast the data will arrive and to record each bit once and only once when it does appear. It is also necessary to arrange for the setting of the character and group limits.

The receiver synchronization system usually adjusts its local timing mechanism to the information appearing in the digital channel by using some information in that channel. Quite frequently this information consists of the location of the individual transitions from "one" to "zero" and vice versa in the message itself.

A narrow-band timing channel has also been used. In this case such information is usually used to pull a local clock into synchronism with the received data. The inertia of the local clock acts as a narrow-band filter to reduce transmission noise in the synchronization channel.

The receiving clock usually takes one of two forms in the synchronous case. It may be an oscillator which is pulled into the proper phase or it may be a ringing circuit of some sort which is shock-excited into operation in the proper phase. Various forms of each of these exist, but most are required to be fairly close in intrinsic operating speed to that of the transmitting clock.

Asynchronous Timing

Asynchronous systems utilize some distinctive line signal to notify the receiver that a data element is arriving at a particular time. Such a system may operate at a constant speed, just as does a synchronous system, but it can be used at a variable rate. The synchronization signal may be any one which is distinguishable from the data portion of the message or which allows for the timing information to be extracted from some property of the data waveform. An example of the latter is the case in which "one" is represented by a positive pulse and "zero" is represented by a negative pulse, there being no pulses for no data. Thus the location of the pulse establishes the synchronization information while its polarity determines what the data are. It should be pointed out, however, that this scheme wastes considerable bandwidth and generally sacrifices noise tolerance.

Start-Stop Timing

A very important use of a combination of asynchronous and synchronous timing systems is found in the start-stop system employed in teletypewriter transmission, in which the sequence of binary states representing a character is always preceded by a stop signal and a start signal. The transition between these is used as the reference timing point for the character, the bits of the character being spaced out after it at equal intervals. Thus, the character timing is asynchronous while the individual bit timing within a character is synchronous.

In the applications requiring character and/or block synchronization in addition to bit synchronization, the required signals are locked together at both the transmitter and the receiver. This may be done by scaling up or down from the primary synchronization signal.

Start Cycle

In general all synchronization systems are compromises between the conflicting demands for a short start cycle and a large tolerance to interference. In order that a receiving synchronization system keep accurate time, it is desirable that the device average its estimate of accurate time over some period of transmission so that local disturbances do not cause sudden jumps out of synchronization. Since asynchronous systems take their timing from a single point in the signaling wave, such systems are quite susceptible to noise interference. These systems, however, start up very rapidly. On the other hand synchronous systems may average their estimates over long periods by using heavy electronic flywheels. These systems, however, require some time to pull into synchronism at the start.

Fig. 3 illustrates a scheme for operating normally with a heavy flywheel and for getting started very rapidly. When the system has been operating for some

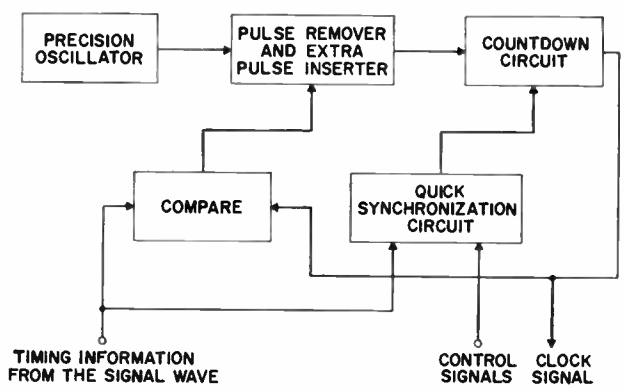

Fig. 3—A high-inertia timing recovery system with a fast-start feature.

time, the oscillator frequency is merely counted down to provide a clock. Slow corrections in clock phase are made by inserting or removing a count pulse at high frequency occasionally when the clock and the signal timing information do not agree. When it is desired to pull rapidly into synchronization, a control signal is sent to the quick-synchronization circuit and the next time a timing point is detected in the signal wave, that circuit clears the countdown circuit counter to zero, thus forcing the clock signal instantly to the latest estimate of correct timing. A number of variations on this general scheme also exist which allow for raising or lowering the inertia of the clock flywheel and so starting at different rates.

Another system for obtaining fast starts and yet having a high-inertia flywheel is described by Edson, Flavin and Perry [11]. Here a high-inertia tuning-fork flywheel is heavily overdriven to get into synchronism rapidly.

VI. Switching

As with other forms of communication there is a need to connect various data terminals together in some flexible way. In the case of much radio communication this is a matter of having the transmitter and the receiver on the same carrier frequency. Of course, many other receivers may also be connected to the transmitter so privacy is scarcely preserved. With fixed-plant communications greater control can be exercised and a more complex switching problem arises.

A considerable amount of work has been done in the switching area within the telephone industry. Some differences exist, however, between switching for voice and switching for data. Some of these differences will be cited and the effect on the switching process will be examined briefly.

Most of the differences between digital data traffic and voice traffic stem from the character of the user. In the voice case a human being is involved, with his normal capacity for interpretation, judgment, and instrument manipulation. In the digital data case the user is often a more or less automatic machine. As such it will do a rather limited repertory of tricks. On the other hand, it will do these tricks with nearly unfailing regularity. It also will not get bored or impatient if it has to wait for a few moments. Furthermore, the machine will be infinitely more businesslike and will get right to the matter of sending the message it holds.

The results of the above are that often the digital message length is shorter than that of a voice message, that special concessions must be made to the machine's lack of ability to recognize audible signals, and that there is less demand for back and forth chit-chat communication than with voice.

Other differences in data traffic stem from the historical situation. Private-line teletypewriter switching systems have existed for some time. These provide certain services that are not common on the telephone network. These services include:

1) Multi-address messages which require a conference-type connection or else the sending of the same message a number of times.
2) The storage of messages in the switching channel for later delivery.
3) The provision of unattended operation.
4) The use of mnemonic addresses.

The various differences existing between voice traffic and data traffic sometimes make necessary certain differences in the engineering of the switching network. The presence of short messages makes it necessary to provide more common control switching equipment for a fixed time-amount of traffic since the setting up of a connection occupies more time relative to the transmission time. Further, the short messages make it desirable that the connections be made rapidly to minimize the waiting time at the transmitter relative to the transmission time.

The general lack of cleverness in the automatic data equipment makes it imperative that the signals in the switching network be intelligible to the data equipment where necessary. Thus, in certain cases, either special signals must be provided or else the current ones must be uniform enough for simple machine-recognition. For example, two signals which are of interest are dial tone and busy indication.

In addition to the services mentioned in connection with teletypewriter switching systems a host of other possibilities are being proposed for computer-like switching devices. Some of the possibilities which have been stressed are:

1) Speed conversion in transit through the network.
2) Code conversion so that different, somewhat incompatible units can communicate.
3) Priority control to take care of important messages.
4) Centralized coding and decoding for error control.
5) Automatic secrecy encoding.
6) Automatic group addressing to set up predetermined conference calls.

This list could be extended a good deal further and could include all of the operations of which computers are capable. The choice of any set of capabilities is largely a matter of the economics involved.

Many of the functions discussed are included in switching systems which are available or proposed. Switching systems with capabilities of this type have been described elsewhere [3], [17], [30]. By utilizing the varied abilities of a computer-like device, extremely versatile systems have been derived. These systems include not only the normal computer functions having to do with internal computation and manipulation, but also provide for on-line attachment of the computer to a communication network. It is to be expected that such devices will have extensive applications in military areas almost immediately. In the commercial area it is

likely that their introduction will proceed more slowly for economic reasons. However, some of the common switching functions will be provided as electronic switching comes into use in the telephone network. In addition, more on-line attachments to connect commercial computers to a communication facility are inevitable.

VII. Channels

The digital communication channel is the most important element of the whole communication system. It determines how much information-carrying capability is present and how simply it can be used.

Perhaps the most important single property of a communication channel is its bandwidth. This quantity is usually dictated more by the transmission properties of the terminal elements than by the nominal propagation medium. Thus, in radio, free space has an almost arbitrarily large bandwidth. Even in wire communications the available bandwidth is often larger than the channel used.

Perhaps the most likely communication channels to be used for data communication (besides the already available telegraph circuits) will be voice circuits selected from the telephone plant. A good deal of information is available on these, but a few general comments seem in order. These will, in general, have a nominal pass band from about 200 cps to perhaps 3000 cps. Variations of considerable magnitude exist about these limits so that this is a most oversimplified view of the situation. The paper by Alexander, Gryb and Nast referred to above is instructive in this regard [4].

The noise to be found in the telephone plant also varies within wide limits. However, the average noise level is generally low, so that white noise is not a problem, but impulse noise can be expected to be noticeable. Such noise can be expected to obliterate the signal in certain cases, and, when this happens, a number of locally correlated errors can be expected to occur.

On the most general circuit it should not be expected that polarities, frequencies, or phases of a transmitted signal will be perfectly reproduced. Certain single-sideband carrier systems allow slight frequency shifts to occur, which result in changes in the above quantities. It is rather unlikely that this frequency shift will exceed 2 cps, although in certain cases of maladjustment the figure may rise above 20 cps. Since certain of the modulation systems are more sensitive than others to these changes (notably phase modulation systems), these facts should be taken into account in choosing a modulation scheme.

In addition to the garden variety voice circuits discussed above which are available in both switched networks and private line versions, other sorts of channels are also obtainable with greater bandwidths. These are available only on a private line basis.

As a rule, private lines are not subject to noise levels as high as those found in the switched network, since they do not pass through the automatic switching equipment which generates much of the impulse noise. The difference is not great, however.

VIII. Information Sources and Sinks; Systems

The only two boxes shown in Fig. 1 which have not as yet been discussed are those labeled "Information Source" and "Information Sink." It is these two portions which are perhaps of most interest to the computer user in that the elements are of the same sort as the devices associated with normal computer installations. As these devices all have the function of providing or absorbing the digital information which goes through the communication channel, the units used in this area either generate, use, or store information.

Some of the devices which may be used as information sources are keyboards, paper tape readers, magnetic tape units, card readers, character recognizers, magnetic core memories, magnetic drums, analog-to-digital converters, pushbuttons, data processors, and dials. At the receiver the required information sink may take as many forms, many of which are the natural complements of the above equipments. These include magnetic units, paper tape punches, magnetic core memories, magnetic drums, digital-to-analog converters, relays, printers, and data processors.

Thus far there have been few installations in which a computer is directly connected to another computer. This situation is partially due to the inherent mismatch in speed between a computer and an ordinary digital data line. Since the computer is generally a much faster unit, the operation of the computer to provide the data to a transmission facility or to absorb the data from a line requires either that the computer slow itself down considerably or that some form of buffering be provided. This latter type of operation is the one which has generally been undertaken. The buffering has been provided by off-line peripheral devices, in most cases, since the real necessity for on-line operation is frequently not pressing. It often is important that certain computer-to-computer data be moved during the same day or even during the same hour, but very seldom is it necessary that this operation have a time scale on the order of milliseconds.

Of course, the most obvious exception to this situation is found in military applications, where the importance of real-time operation is somewhat greater than in commercial uses. The SAGE system is an example of an installation where wasted time defeats the purpose of the system. As the pace of warfare increases with other advances in technology, it is apparent that the emphasis in this area will increase.

A second type of operation in which the real-time value of the digital information to be transmitted is very high appears when the digital communication facility is merely a way of carrying analog data of real-time importance. Such applications often involve telemetering systems. The use of pulse code modulation (among

other pulse schemes) for the transmission of speech over voice facilities also has this requirement built into it.

In the more usual applications the need for a very small time delay is not as pressing as in the systems just described. Thus the various units which are used as information sources and information sinks are usually not computers themselves but the various devices which were listed. They are generally units which can store information in one way or another. The most common devices for this purpose are found in the teletypewriter networks. There the common storage medium is paper tape. Thus at the transmitting terminal the information source is usually a piece of perforated paper tape. The unit actually reading this tape feeds the information to the transmission sections of the system. At the receiving location the information is commonly again placed in a storage medium. Paper tape is the usual choice. This is particularly true if the information is to be used by a machine. If the ultimate destination of the material is a person, then the receiving recorder may be a printer.

It is also possible to transmit to the line directly from a keyboard with a human operator. However, this form of operation is very inefficient in its use of line time since the operator is not capable of the same sort of speed as a tape reader (or the line).

A second system of off-line transmission which is relatively popular is one which transmits from a punched card to another punched card. The IBM Transceiver provides such a service. This system, while very convenient from the standpoint that a typical business may have cards to transmit, is relatively slow, and rather costly. The more recently announced IBM 1001 is considerably less expensive, but its speed capabilities are even less. This defect, however, is not important in many cases.

Perhaps the most promising method of communication which is currently being tried is the magnetic tape to magnetic tape system. To date this has been used in very few locations. The Collins Kinetape system and the IBM 7701 tape-to-tape system are examples of such units. One difficulty as yet not completely solved in such systems is that they are intrinsically expensive. The tape units involved are complex and usually designed to operate at speeds which are much higher than those of the communication facilities to which they are fastened. Thus it has been necessary to devise special tape units or extensive buffering systems to take care of the speed differentials. These systems, however, are almost certain to be very important in the future, for, as more and more computers are installed, magnetic tape is likely to be the major form of bulk storage for the foreseeable future. Thus, transmission from it will be a necessary function.

The discussion thus far in this section has principally emphasized the role of the off-line type of transmission. This is not to imply that the situation will always be the same as it is now. In fact there are already a considerable number of applications in addition to the military ones in which the direct connection of a computer to another computer or of a computer to other outlying equipment is important.

Centralized Computer Systems

As yet, to the author's knowledge, there are no direct real time computer-to-computer digital communication systems. However, there are a number of applications being very actively pursued in which a number of outlying locations using equipment other than computers are being connected in real time to a computer in an automatic way. Generally these systems can be called data gathering, data distribution, and control systems.

The data gathering systems include ones in which data are sent, often by unsophisticated data terminals, to a central location for storage and processing. A number of forms of system control are possible in this way. Also, such a system may be used to return control data from the central location to operate a scattered network of activities effectively. Obvious examples of such systems handle inventory control for large merchandising organizations. In this way it has been possible to reduce the money invested in large inventories and to use this money for more profitable ventures.

In a typical installation of the above type a central computer may be connected on-line or off-line to a large number of relatively simple data units. These units may, for example, take the form of teletypewriter equipment. In the future it is likely that simple card readers or perhaps pushbuttons will be used. However, to date, no inexpensive receiving device is available for the outlying location which is as economical as the teletypewriter equipment.

Another area where a good deal of activity is now going on is that of reservation systems. This is particularly true of airlines reservation systems, where time is of great importance. In such systems a central computer is used to maintain records of reservations on all of the flights of a given airline for some time in advance. Outlying agent sets are connected to this computer via a wire network on a real-time basis. When a customer appears at one of the outlying locations, the agent may, on a very short time scale, inquire of the computer about the status of any flight; change the reservation status of that customer; sell him a ticket and get immediate confirmation of the sale; inform the computer of the customer's telephone number in case of changed plans and do other similar things.

Another area which is receiving considerable attention is that of air traffic control. With the increasing use and speed of aircraft, the airways are becoming exceedingly congested. The problem met in air traffic control is that of maintaining a real-time picture of the airways situation with an eye to operating it smoothly and, most importantly, safely. By means of a central computer operated in real time, flights may be expeditiously controlled from a single location.

These examples give a flavor for the sorts of problems

that are being placed on centralized computer systems. Others exist also. More will come into being as their economic value increases, as their cost comes down, or as they are newly discovered. Perhaps we may eventually even reach the heights of centralization and control whose arrival by 1960 was predicted a few years ago.

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Arbitrary Boolean Functions of N Variables Realizable in Terms of Threshold Devices*

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Summary—**A method is presented for the logical design of single-stage, combinatorial switching circuits of n variables. This method is applicable to circuits composed of threshold devices, such as magnetic cores, transistors with Kirchhoff adder inputs, parametrons, etc. A study of the constraints imposed by the form of the input portions of the threshold devices leads to the definition of certain classes of functions which are physically realizable in a single device. By the use of this method, arbitrary switching functions of as many as seven variables have been easily designed by hand computations.**

Introduction

It is well known that there are 2^{2^n} possible switching functions of n variables, where each variable can take only the values "1" or "0." Each truth function has 2^n states. For the purpose of designing arbitrary functions, switching circuits for only a small class of these functions need to be cataloged, since it can be shown that this class of circuits, under the symmetry operations of permutations and complementations of the input variables, maps the entire set.

Thus, Aiken[1] lists all vacuum-tube switching circuits for four variables in a table of 402 entries. Two other tables are given which show the transformation of the function under the group of symmetry operations on the input variables, but even for four variables, the process of transforming and classifying an arbitrary function is extremely tedious, while the use of five variables requires a catalog of over one million switching circuits.[2]

The above classification is without regard to the properties of the physical circuit which is used to embody the function. Thus, the same "primitive" set of functions is designed whether the circuit elements are vacuum tubes, magnetic cores, or relays, etc. If the circuit element is a threshold device such as a magnetic core, then certain constraints are introduced into the problem. These constraints define a different class of functions, those which can be embodied in a single input-composite of a threshold device. Such functions will be called consistent with respect to a threshold device. If only the consistent switching circuits need to be designed, and allowing symmetry operations, a table of only 14 entries is required for all four variable functions, and probably no more than 62 for all five variable functions.

The design of an arbitrary n variable function, using threshold devices, is accomplished in the following manner: 1) the truth function is first partitioned so as to separate the ONE bits into a set of functions, each of which is independently consistent; 2) the input composite for each of these functions is designed, perhaps, by referring to a table of consistent switching circuits; and 3) since the partitioning of the function places each of its ONES into one, and only one subset, the outputs of the switching circuits need only to be ORed together to embody the entire function.

It is the purpose of this paper to demonstrate a means of partitioning and designing arbitrary n variable Boolean functions. Although most of the reported work is with reference to magnetic cores, it is presented in terms of the generalized concept of a threshold switching device. For this reason and because they are adequately treated elsewhere,[3] the physical details of magnetic core switching are omitted here.

Threshold Device Logical Element

A threshold device can be brought to either of two distinct states depending upon the magnitude of some physical quantity at its input. Although the threshold of a given device has a distinct magnitude (*i.e.*, in a magnetic core the applied magnetizing force H_i must exceed the coercive force H_c in order to switch), it is preferable to specify a range. That is, if the state is not to change, the strength of the input must be less than a specified quantity; if it is to change, the strength of the input must be greater than another quantity. To use the example of a magnetic core again, if the core is not to switch from negative remanence, the applied magnetizing force $H_i \leq 0$; or if it is to switch $H_i \geq H_o$, where $H_o \geq H_c$ and depends upon the desired speed of switching. In units of H_o: $H_i \leq 0$ implies a "0," $H_i \geq 1$ implies a "1," where "0" and "1" denote respectively the negative and positive remanent states of the core and it is assumed that the core always starts from negative remanence.

The threshold device may be considered to be composed of two separate portions, an input circuit which

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comprises a means of weighting and combining the input variables, and an output stage which indicates by a definite change in state whether or not the combined value of the weighted variables exceeds the threshold. Following Karnaugh,[3] the mathematical description of the input circuit is called the *input composite*. The input variables are denoted by $x_1, x_2, \cdots x_n$ and can take only the values 0 or 1. All variables operate simultaneously in the input composite. The term x_0 is reserved for a unit pulse which, together with its weighting factor, is called the bias.

The effects of the inputs are added algebraically to obtain the net effect on the output stage of the threshold device, and the input composite may, therefore, be represented in the following form:

$$M = q_0N_0x_0 + q_1n_1x_1 + \cdots + q_nN_nx_n. \qquad (1)$$

Here $q_i = \pm 1$ and N_i is a positive integer or zero. In terms of magnetic cores, q_i represents the polarity, N_i the number of turns of the winding, and M the net applied magnetomotive force where x_i represents a constant current pulse.

Now, since the value of M depends on the manner in which the variables x_i are taken as 0 and 1, we define a new quantity in terms of a column matrix which will be called the solution vector, $\boldsymbol{S}$, the terms of which are called the input values.

$$\boldsymbol{S} = \begin{bmatrix} q_0N_0 \\ q_1N_1 \\ \vdots \\ q_nN_n \end{bmatrix}$$

The M above is one term of a vector which is found by multiplying the solution vector by the truth table for n variables, treated as a matrix $\boldsymbol{T}$. The vector $\boldsymbol{M}$ will be called the input composite vector.

$$\boldsymbol{T}\cdot\boldsymbol{S} = \boldsymbol{M}$$

$$\begin{array}{c} x_0\ x_1\ x_2\ x_3 \cdots x_n \\ \begin{bmatrix} 1 & 0 & 0 & 0\cdots 0 \\ 1 & 1 & 0 & 0\cdots 0 \\ 1 & 0 & 1 & 0\cdots 0 \\ 1 & 1 & 1 & 0\cdots 0 \\ 1 & 0 & 0 & 1\cdots 0 \\ 1 & \cdot & \cdot & \cdot\cdots\cdot \\ 1 & \cdot & \cdot & \cdot\cdot\ \ \cdot \\ \cdot & \cdot & \cdot & \cdot\cdot\ \ \cdot \\ \cdot & \cdot & \cdot & \cdot\ \ \cdot\ \ \cdot \\ \cdot & \cdot & \cdot & \cdot\cdot\ \ \cdot \\ 1 & 1 & 1 & 1\cdots\ \ \cdot \end{bmatrix} \end{array} \cdot \begin{bmatrix} q_0N_0 \\ q_1N_1 \\ q_2N_2 \\ \vdots \\ q_nN_n \end{bmatrix}$$

$$= \begin{bmatrix} q_0N_0 \\ q_0N_0 + q_1N_1 \\ q_0N_0 + \quad + q_2N_2 \\ q_0N_0 + q_1N_1 + q_2N_2 \\ q_0N_0 \quad\quad + q_3N_3 \\ \vdots \\ q_0N_0 + q_1N_1 + q_2N_2 + q_3N_3 + \cdots + q_nN_n \end{bmatrix}.$$

The logic function $\boldsymbol{F}$ is evaluated by applying the threshold condition to $\boldsymbol{M}$.

Symmetry Operations

The input circuit of a threshold device is specified by its solution vector. Since it is a physical structure, it is invariant to complementations of and permutations among the input variables. It is easily shown that the effect of the symmetry operations is to permute the rows of the truth table. Consequently, the terms of the input composite vector are likewise permuted without changing their values [see (2)]. One can thus postulate a $2^n \times 2^n$ permutation matrix $\boldsymbol{P}$ which transforms a given $\boldsymbol{M}$ or its corresponding logic function, $\boldsymbol{F}$, to another, $\boldsymbol{F}'$, having the same primitive solution, or switching circuit. Now, since it is desirable to avoid the use of complement drivers, and the necessity for interchanging leads, we transform the solution matrix, $\boldsymbol{S}$, by means of a matrix, $\boldsymbol{C}$, which is defined as follows:

$$\boldsymbol{T}\cdot\boldsymbol{S} = \boldsymbol{M} \qquad (2)$$

$$\boldsymbol{T}\cdot\boldsymbol{C}\cdot\boldsymbol{S} = \boldsymbol{M}' = \boldsymbol{P}\cdot\boldsymbol{T}\cdot\boldsymbol{S} = \boldsymbol{P}\cdot\boldsymbol{M}; \qquad (3)$$

therefore

$$\boldsymbol{T}\cdot\boldsymbol{C} = \boldsymbol{P}\cdot\boldsymbol{T} \qquad (4)$$

premultiplying both sides by $\boldsymbol{T}_t$

$$\boldsymbol{T}_t\cdot\boldsymbol{T}\cdot\boldsymbol{C} = \boldsymbol{T}_t\cdot\boldsymbol{P}\cdot\boldsymbol{T}. \qquad (5)$$

It can be shown by partitioning $\boldsymbol{T}$ and applying induction that $\boldsymbol{T}_t\cdot\boldsymbol{T}$ is nonsingular and thus has an inverse, $(\boldsymbol{T}_t\cdot\boldsymbol{T})^{-1}$ for any number of variables, n. Therefore,

$$\boldsymbol{C} = (\boldsymbol{T}_t\cdot\boldsymbol{T})^{-1}\cdot\boldsymbol{T}_t\cdot\boldsymbol{P}\cdot\boldsymbol{T}. \qquad (6)$$

Only certain $\boldsymbol{P}$ matrices are allowed because, although the transformation, $\boldsymbol{M}' = \boldsymbol{P}\cdot\boldsymbol{M}$, is not unique, only one of the possible $\boldsymbol{P}$ matrices will lead to a product, $\boldsymbol{T}_t\cdot\boldsymbol{P}\cdot\boldsymbol{T}$, which is nonsingular. The properties of the allowed $\boldsymbol{P}$-matrix have not been fully investigated as yet. In any case, we are now in a position to describe $\boldsymbol{C}$ matrices which will perform the symmetry operations on both the solution $\boldsymbol{S}$ and the truth matrix $\boldsymbol{T}$, by (4) above. An example will, perhaps, best bring out the qualities of the $\boldsymbol{C}$ matrix. Given a Boolean function of 3 variables, $F = 10101100$ (the least significant bit is in boldface type), the permutation matrix, $\boldsymbol{P}$, below transforms it to $F' = 00100111$, which has the same

switching circuit and which is listed in a table of basic switching circuits such as that of Aiken.[1]

$$F' = P \cdot F$$

$$\begin{bmatrix}1\\1\\1\\0\\0\\1\\0\\0\end{bmatrix} = \begin{bmatrix}0&0&0&0&0&0&0&1\\0&0&0&1&0&0&0&0\\0&0&0&0&0&1&0&0\\0&1&0&0&0&0&0&0\\0&0&0&0&0&0&1&0\\0&0&1&0&0&0&0&0\\0&0&0&0&1&0&0&0\\1&0&0&0&0&0&0&0\end{bmatrix} \cdot \begin{bmatrix}0\\0\\1\\1\\0\\1\\0\\1\end{bmatrix}. \quad (7)$$

The C matrix is formed by the use of (6)

$$C = (T_t \cdot T)^{-1} \cdot (T_t \cdot P \cdot T).$$

For $n=3$, the product $T_t \cdot T$ and its inverse are:

$$T_t \cdot T = \begin{bmatrix}8&4&4&4\\4&4&2&2\\4&2&4&2\\4&2&2&4\end{bmatrix},$$

$$(T_t \cdot T)^{-1} = \frac{1}{4}\begin{bmatrix}2&-1&-1&-1\\-1&2&0&0\\-1&0&2&0\\-1&0&0&2\end{bmatrix}.$$

Then $T_t \cdot P \cdot T$

$$\begin{bmatrix}1&1&1&1&1&1&1&1\\0&1&0&1&0&1&0&1\\0&0&1&1&0&0&1&1\\0&0&0&0&1&1&1&1\end{bmatrix} \cdot \begin{bmatrix}0&0&0&0&0&0&0&1\\0&0&0&1&0&0&0&0\\0&0&0&0&0&1&0&0\\0&1&0&0&0&0&0&0\\0&0&0&0&0&0&1&0\\0&0&1&0&0&0&0&0\\0&0&0&0&1&0&0&0\\1&0&0&0&0&0&0&0\end{bmatrix} \cdot \begin{bmatrix}1&0&0&0\\1&1&0&0\\1&0&1&0\\1&1&1&0\\1&0&0&1\\1&1&0&1\\1&0&1&1\\1&1&1&1\end{bmatrix}$$

$$= \begin{bmatrix}8&4&4&4\\4&2&2&0\\4&2&0&2\\4&0&2&2\end{bmatrix} \quad (8)$$

$$\frac{1}{4}\begin{bmatrix}2&-1&-1&-1\\-1&2&0&0\\-1&0&2&0\\-1&0&0&2\end{bmatrix} \cdot \begin{bmatrix}8&4&4&4\\4&2&2&0\\4&2&0&2\\4&0&2&2\end{bmatrix} = \begin{bmatrix}1&1&1&1\\0&0&0&-1\\0&0&-1&0\\0&-1&0&0\end{bmatrix}. \quad (9)$$

$(T_t \cdot T)^{-1} \cdot (T_t \cdot P \cdot T) = C$

Since postmultiplying T by C is the same as premultiplying it by P, let us form the product $T \cdot C = T'$ and examine the resulting transformation of the truth matrix

$T \quad C \quad T'$

$$\begin{matrix}x_0&x_1&x_2&x_3\end{matrix}$$

$$\begin{bmatrix}1&0&0&0\\1&1&0&0\\1&0&1&0\\1&1&1&0\\1&0&0&1\\1&1&0&1\\1&0&1&1\\1&1&1&1\end{bmatrix} \cdot \begin{bmatrix}1&1&1&1\\0&0&0&-1\\0&0&-1&0\\0&-1&0&0\end{bmatrix} = \begin{bmatrix}1&1&1&1\\1&1&1&0\\1&1&0&1\\1&1&0&0\\1&0&1&1\\1&0&1&0\\1&0&0&1\\1&0&0&0\end{bmatrix}. \quad (10)$$

Comparing T and T', we see that the effect of the matrix C has been to interchange columns x_1 and x_3 and replace the variables by their complements x_1', x_2', x_3'. Indeed, C is the product of a permutation matrix Π and a complementation matrix K.

$\Pi \quad K \quad C$

$$\begin{bmatrix}1&0&0&0\\0&0&0&1\\0&0&1&0\\0&1&0&0\end{bmatrix} \cdot \begin{bmatrix}1&1&1&1\\0&-1&0&0\\0&0&-1&0\\0&0&0&-1\end{bmatrix} = \begin{bmatrix}1&1&1&1\\0&0&0&-1\\0&0&-1&0\\0&-1&0&0\end{bmatrix}. \quad (11)$$

Thus, to complement any variable x_i without recourse to complement drivers, it is replaced by $(x_0 - x_i)$; this corresponds to Karnaugh's theorem.[4]

All possible matrices Π and K for n variables, together with the unit matrix I, form a group which is isomorphic with the group of isometries of an n-dimensional hypercube.[5] For $n=3$, the group contains 48 members, *i.e.*, six permutations, and eight complementations.

We have, thus, shown that if a permutation matrix P can be found which transforms an arbitrary function to another having a known solution (or switching circuit) and if P has the property such that $T_t \cdot P \cdot T$ is nonsingular, then a transformation C can be found which will convert the known solution to the desired one.

[4] *Ibid.*, p. 575.

[5] G. Birkhoff and S. Maclane, "A Survey of Modern Algebra," The Macmillan Co., New York, N. Y., p. 128; 1946.

Consistent Functions

If we examine a truth table for n variables, we see that each span of four rows repeats the truth values for the variables x_1 and x_2. The variable x_3 becomes true in the second span and remains true for the entire span, likewise with x_4 in the third span. In fact, each variable, x_i, $3 \leq i \leq n$, must be constant in any arbitrary span of four rows. Thus, any variations in the values of the terms of the input composite vector within any span of four terms must be due to the variables x_1 and x_2. Within any span, the presence of true variables whose indices are 3 or greater only affect the net bias and establish an average level for that span, as can be seen in Fig. 1. Consequently, it is instructive to study the properties of the set of functions of two variables.

Of the 16 functions of two variables, 14 of them are consistent as defined in the Introduction. With a little reflection, it is possible to write unique, minimal solutions for each of them. These functions are shown in Table I, where the decimal heading indicates the function, *i.e.* ONE is 0001, FIVE is 0101, etc. SIX and NINE, the two alternating symmetric functions (EXCLUSIVE OR and its inverse), cannot be embodied in a single input composite and are, therefore, inconsistent. It is easy to see that this is true by referring to Fig. 1. That is, for function SIX, if both $q_0N_0+q_1N_1 \geq 1$, and $q_0N_0+q_2N_2 \geq 1$ where $q_0N_0 \leq 0$, then surely

$$q_0N_0 \times q_1N_1 + q_2N_2 \geq 1,$$

and similarly for NINE.

As an example of the manner in which solutions of higher-order functions can be built up from the two-variable solutions, compare the solution for function SEVEN with the solution for function ONE. We see that the two are identical if the x_0 input value of the former is reduced by one. If we take the three-variable function $f_3 = 0001,0111$, the first span can be represented by function SEVEN and the second by function ONE. Referring to Fig. 1, in the second span, the net bias term, which is constant throughout the span is $(q_0N_0+q_3N_3)$. If we, therefore, make the input value of x_3, $q_3N_3 = -1$, then the solution for the first span fits the second span and the input composite is $M = 2x_0 - 1x_1 - 1x_2 - 1x_3$. Plotting the successive values of M (the terms of the input composite vector) we get the input composite profile which aids in visualizing the

	x_0	x_1	x_2	x_3	x_4	$\cdots$	x_n	M
Span 1	1	0	0	0	0	$\cdots$	0	q_0N_0
	1	1	0	0	0	$\cdots$	0	$q_0N_0 + q_1N_1$
	1	0	1	0	0	$\cdots$	0	$q_0N_0 + q_2N_2$
	1	1	1	0	0	$\cdots$	0	$q_0N_0 + q_1N_1 + q_2N_2$
Span 2	1	0	0	1	0	$\cdots$	0	$(q_0N_0+q_3N_3)$
	1	1	0	1	0	$\cdots$	0	$(q_0N_0+q_3N_3)+q_1N_1$
	1	0	1	1	0	$\cdots$	0	$(q_0N_0+q_3N_3) + q_2N_2$
	1	1	1	1	0	$\cdots$	0	$(q_0N_0+q_3N_3)+q_1N_1+q_2N_2$
Span 3	1	0	0	0	1	$\cdots$	0	$(q_0N_0+q_4N_4)$
	1	1	0	0	1	$\cdots$	0	$(q_0N_0+q_4N_4)+q_1N_1$
	1	0	1	0	1	$\cdots$	0	$(q_0N_0+q_4N_4) + q_2N_2$
	1	1	1	0	1	$\cdots$	0	$(q_0N_0+q_4N_4)+q_1N_1+q_2N_2$
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
Span 2^{n-2}	1	0	0	1	1	$\cdots$	1	$(q_0N_0+q_nN_n+q_{n-1}N_{n-1} \cdots q_3N_3)$
	1	1	0	1	1	$\cdots$	1	$(q_0N_0+q_nN_n+q_{n-1}N_{n-1} \cdots q_3N_3)+q_1N_1$
	1	0	1	1	1	$\cdots$	1	$(q_0N_0+q_nN_n+q_{n-1}N_{n-1} \cdots q_3N_3) + q_2N_2$
	1	1	1	1	1	$\cdots$	1	$(q_0N_0+q_nN_n+q_{n-1}N_{n-1} \cdots q_3N_3)+q_1N_1+q_2N_2$

Fig. 1—A portion of a truth table for n variables.

TABLE I

Consistent Solutions of Two-Variable Functions

Number	0	1	2	3	4	5	7	8	10	11	12	13	14	15
Function	0	1	0	1	0	1	1	0	0	1	0	1	0	1
	0	0	1	1	0	0	1	0	1	1	0	0	1	1
	0	0	0	0	1	1	1	0	0	0	1	1	1	1
	0	0	0	0	0	0	0	1	1	1	1	1	1	1
Solution	0	1	0	1	0	1	2	−1	0	1	0	1	0	1
	0	−1	1	0	−1	−1	−1	1	1	1	0	−1	1	0
	0	−1	−1	−1	1	0	−1	1	0	−1	1	1	1	0

described process (Fig. 2). Thus we see that the profiles of the minimal solutions of the functions SEVEN and ONE are identical in form, but that the latter is shifted one unit to the left. Likewise, the two spans of the function F are identical in form with the lower span shifted one unit to the left with respect to the upper span, in accordance with the input value of x_3. The function F is, therefore, consistent.

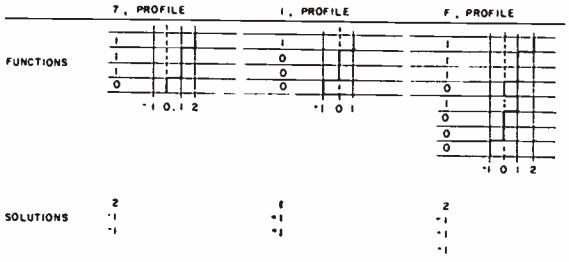


Fig. 2—Function profiles.

Functions such as SEVEN and ONE will be called compatible with one another if both functions can be derived from the same solution merely by a change in the bias. It can be shown that other compatibilities exist if certain equivalent modified two-variable solutions are admitted. The only allowed modifications of the minimal solutions are in the terms N_1 and N_2 of the solution vector. The signs of the terms, q_i, are not allowed to change. The N_i can only be increased, since we start with a minimal solution. Reducing the input value of either variable to zero reduces the order of the solution. Likewise, if the input value of x_i is zero, we cannot alter it without more information, since the value of q_i is not known. We now investigate whether a modified—or nonminimal—solution which may represent a different function can be restored to representing the original function merely by a change in bias.

If a modified two-variable solution is formed from a minimal two-variable solution by increasing the input value N_i of one of the two variables, it can be seen by the first span of Fig. 1 that the value of the input composite for either pair of terms M_1 and M_3 or M_2 and M_3 will be altered without altering the difference between them because the same amount is added to each. Thus, if the truth values of either or both members of one pair of terms change, their truth values can be restored by a compensating change in the bias. This compensating change will not alter the truth values of the unaffected terms for the following reasons: consider first the terms M_1 and M_2.

1) If both terms are greater than one, and if the input value of x_1 or x_2 is altered so as to cause either M_1 or M_2 to become zero or less (the q_i of the variable in question must be -1), then in "restoring" by a bias change, which must be in the positive direction, the previously unaffected term is made more positive so its truth value is unchanged.
2) If both terms were zero or less, by the same reasoning, the truth value of the unaltered term is not affected by restoring.
3) If one term is one or greater and the other is zero or less, the truth values of terms M_1 and M_2 cannot be altered by altering N_1 or N_2 since the signs q_1 and q_2 are opposite. Note that if either N_1 or N_2 is zero, it cannot be altered, since we do not know the value of its q_i.

Now consider the term M_0, the truth value of which is most likely to change with restoring by bias compensation since it depends only on N_0:

1) If $M_0 \leq 0$ and the solution is to be altered so as to cause either M_1 or M_2 to exceed the threshold, it can only be done if the appropriate input value was initially positive. Restoring will, therefore, only make M_0 more negative and will not alter its truth value, f_0.
2) If $M_0 \leq 0$ and either M_1 or M_2 is to be made less than zero, it cannot be done by the allowed alterations, since the appropriate q_i must be initially positive.
3) If $M_0 \geq 1$, the same reasoning shows that the only possible alteration in the term M_1 or M_2 is such as to cause its value to go from one or greater to zero or less, changing its truth value from a "1" to a "0." Therefore, restoring the truth value of the term M_1 or M_2 will not alter the truth value of M_0.

Thus, it has been shown that a minimal two-variable solution which represents one two-variable function can be altered so as to represent a different, though related, function by altering the input value N_i of one or both of the variables, x_1, x_2, or the bias x_0 and then "restored" to representing the original function solely by a change in the bias input value $q_0 N_0$. These related functions, sharing a nonminimal solution, are also compatible.

As an example, let us solve the three-variable function $F = 00010101$. Dividing it into two four-bit spans, noting their minimal, two-variable solutions from Table 1, and generating their profiles, we have Fig. 3. It is readily seen that no possible alteration of the input values of the biases of either two-variable solutions in Fig. 3 can make either function fit the other function. Now, if we add like terms of the solution vectors, or add across the two profiles, we obtain the nonminimal solution and profile shown in the third column of Fig. 3, which still represents the upper span function. The fourth column shows that by adding -1 to the bias, the same solution and profile can also represent the second span of the function F. This indicates, as in the previous example, that the input value of variable x_3, $q_3 N_3 = -1$ and the solution for the function F is as shown in Fig. 4. If the two corresponding terms of two minimal solutions have opposite signs, the order of the solution is reduced and the sum cannot represent either. Such solutions are not compatible.

The 14 consistent, two-variable functions may now be tabulated and classified with respect to their com-

patibility with one another. A convenient way to do so is on the basis of their profiles. Such a tabulation is shown in Fig. 5. The function is written between the values $M=0$ and $M=1$. Where the same profile can represent two functions by shifting, they are displayed accordingly. The letters are arbitrarily assigned for convenient reference. The compatibilities of the minimal functions are shown in Table II. The empty set is called "0," and the filled set I, and they are compatible with all other functions.

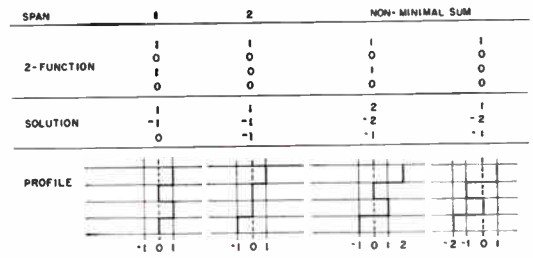


Fig. 3—Sum of minimal profiles.

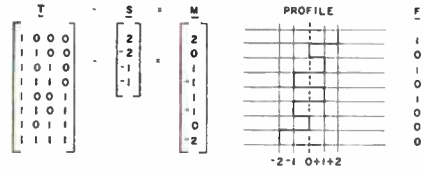


Fig. 4—A consistent three-variable function and solution.

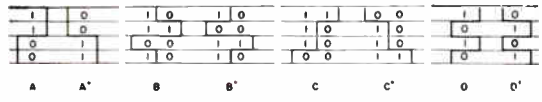


Fig. 5—Consistent minimal profiles.

The Partitioning of Functions

Having examined some of the properties of the minimal, consistent two-variable solutions, we are now in a position to consider a method of partitioning the true terms of an arbitrary n variable truth function into a set of functions each of which is consistent, in accordance with the design procedure laid out in the introduction. It was shown in the discussion of consistent functions that any term to term variations of the M vector within a span of four terms must be due only to variables x_1 and x_2. Thus, if the function is divided into spans of four terms as in Fig. 1, the minimal two-variable solutions for each span considered independently must be compatible with all others, according to the listing in Table II if the function is consistent. Note that compatibility is not transitive; *i.e.*, the fact that B is compatible with A and A with C does not imply that B is compatible with C. By permuting the inputs, any other pair of variables can be made to play the role of x_1 and x_2 in a transformed function. For example, let us consider a truth table for four variables in Fig. 6(a) and permute the rows to produce the table in Fig. 6(b). In the transformed table x_1 and x_2 are held constant and x_3 and x_4 range in each span of four rows. It is easily seen that permuting the columns, x_1 and x_3, and also the columns, x_2 and x_4, will cause the desired permutation of the rows of the truth table. The spans of the transformed function must similarly be compatible with one another if the function is consistent. Likewise, other pairs of columns, that is, x_2, x_4; x_1, x_4; etc. are permuted with x_1 and x_2 in such a manner that the remaining columns remain in numerical order. For example, see the following column orderings. (The rows represent the column headings.)

1 2 3 4
3 4 1 2
2 4 1 3
1 4 2 3
2 3 1 4
1 3 2 4.

TABLE II
Compatibilities of Minimal Two-Variable Solutions

Function	A	B	C	D	A'	B'	C'	D'
Compatible Functions	B C	A D'	A D	B' C	B' C'	A' D	A' D'	B C'

State	x_0	x_1	x_2	x_3	x_4
0	1	0	0	0	0
1	1	1	0	0	0
2	1	0	1	0	0
3	1	1	1	0	0
4	1	0	0	1	0
5	1	1	0	1	0
6	1	0	1	1	0
7	1	1	1	1	0
8	1	0	0	0	1
9	1	1	0	0	1
10	1	0	1	0	1
11	1	1	1	0	1
12	1	0	0	1	1
13	1	1	0	1	1
14	1	0	1	1	1
15	1	1	1	1	1

(a)

State	x_0	x_1	x_2	x_3	x_4
0	1	0	0	0	0
4	1	0	0	1	0
8	1	0	0	0	1
12	1	0	0	1	1
1	1	1	0	0	0
5	1	1	0	1	0
9	1	1	0	0	1
13	1	1	0	1	1
2	1	0	1	0	0
6	1	0	1	1	0
10	1	0	1	0	1
14	1	0	1	1	1
3	1	1	1	0	0
7	1	1	1	1	0
11	1	1	1	0	1
15	1	1	1	1	1

(b)

Fig. 6—(a) Four-variable truth table. (b) Transformed truth table.

Each column permutation and test for compatibility is referred to as a sieve. The function which passes through all sieves, obviously, must be consistent.[6] The partitioning algorithm follows: at each sieve, if necessary, some true terms of the function are removed until a function is developed which will pass all sieves. This is called the first partitioning. The remaining true terms are subjected to the same sieving process which repeats until all true terms are classified. A five-variable example is given in Appendix I.

Certain ones of the permutations of the terms of the function can be attained easily by the following technique which will be demonstrated for a five-variable function. We will allow the decimal representation of the state (row) of the truth table to stand for the truth value of that state. Thus, 0 is the truth value of the function for 100000 row of the truth table, 3 stands for the truth value of the row 111000, etc. We break the function into quarters and write them as rows from right to left of a rectangular array.

7	6	5	4	3	2	1	0	
15	14	13	12	11	10	9	8	first sieve.
23	22	21	20	19	18	17	16	
31	30	29	28	27	26	25	24	
S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1	

Now, taking the columns from right to left in order, each column is a span of the transformed function. The letter designation of the minimal solutions, S_i, $1 \leq i \leq 8$, for each span obtained from Fig. 5, is affixed at the bottom of the appropriate column. For the second sieve, the function is broken at the middle, and each half divided into quarters as follows:

lower half				upper half				
19	18	17	16	3	2	1	0	
23	22	21	20	7	6	5	4	
27	26	25	24	11	10	9	8	second sieve.
31	30	29	28	15	14	13	12	
S_8'	S_7'	S_6'	S_5'	S_4'	S_3'	S_2'	S_1'	
lower half				upper half				
28	24	20	16	12	8	4	0	
29	25	21	17	13	9	5	1	
30	26	22	18	14	10	6	2	third sieve.
31	27	23	19	15	11	7	3	
S_8''	S_7''	S_6''	S_5''	S_4''	S_3''	S_2''	S_1''	

It is often the case that the three sieves shown above are sufficient to partition the function, as in the example in Appendix I. In general, however, all sieves must be applied, and there are $n(n-1)/2$ such orderings. The conditions which allow a reduction in the number of sieves is under investigation.

[6] There are reasons for accepting the sufficiency as well as the necessity of the above condition which have not as yet been formalized into a rigorous proof.

Input Composite Design

Having attained a partition of the function, it now remains to find solutions for each of the subfunctions. This can be done by applying the results of the foregoing discussion of nonminimal two-variable solutions or by recourse to a table of consistent switching circuits, or primitive solutions. In either case, the function is transformed by symmetry operations so as to move all ONES toward the least significant bit end of the function and cluster as closely as possible. To show that this can always be done, consider a solution having any arbitrary entries, q_iN_i, $0 \leq i \leq n$. It is in primitive form if all positive q_iN_i (excluding q_0N_0) are complemented so as to make all q_i except q_0 negative, and the negative terms are arranged in ascending order in absolute value as in Fig. 7. Since only the bias can be positive, the ONES must be clustered at the least significant bit end. Transforming the function is a trial and error process. Recourse can be had to tables such as supplied by Aiken[1] or, with some practice, the transformations for any symmetry operations become obvious. For example, interchanging x_1 and x_2 permutes the terms of the pairs: 1, 2; 5, 6; 9, 10; 13, 14; etc. of the truth table.

$$S = \begin{bmatrix} -1 \\ 2 \\ -3 \\ 1 \\ -2 \\ 1 \end{bmatrix} \qquad S_p = \begin{bmatrix} 3 \\ -1 \\ -1 \\ -2 \\ -2 \\ -3 \end{bmatrix}$$

(a) (b)

$F_a = 0010 \quad 0000 \quad 0011 \quad 0010 \quad 0000 \quad 0000 \quad 0010 \quad 0010$
$F_b = 0000 \quad 0000 \quad 0000 \quad 0000 \quad 0000 \quad 0001 \quad 0001 \quad 1111$

Fig. 7—(a) Switching circuit. (b) Primitive form.

Complementing x_1 permutes the terms of the pairs: 0, 1; 2, 3; 4, 5; etc. In addition to the symmetry operations, the inverse—or complement—of the function and the suppression of variable x_i are allowed. The inverse operation on the solution is equivalent to subtracting the given function from one which is true in every term. Thus, the solution in Fig. 7(a) is inverted by the matrix subtraction:

$$1 - F_a = F_a'$$

$$\begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} - \begin{bmatrix} -1 \\ 2 \\ -3 \\ 1 \\ -2 \\ 1 \end{bmatrix} = \begin{bmatrix} 2 \\ 2 \\ 3 \\ -1 \\ 2 \\ -1 \end{bmatrix}. \qquad (12)$$

If the number of ONES is greater than 2^{n-1}, it is advantageous to invert before proceeding. Suppression is illustrated by referring to the function F_b in Fig. 7. It is noted that the 16 bits in the most significant bit end of the function are all ZERO. This implies that the input value of the variable, x_5, which is true for the entire latter half of the function, is strongly enough negative to over-ride the most positive combination of other inputs and the bias. The ZEROS in the latter half of the function can, therefore, be dropped, reducing the function to one of four variables if a notation is made that variable x_5 is to be suppressed.

If the solution is to be derived without the use of a table of switching circuits, the transformations of the function need not proceed entirely to the primitive form. Remembering that a consistent function can have at most only two different compatible, minimal, two-variable solutions in its spans (aside from 0 and I), the representative minimal solutions or their profiles are added across to obtain a composite, nonminimal, two-variable solution which by changes only in the bias can be made to represent all spans. The input values of the bias and of the variables, x_i, $3 \leq i \leq n$ are then be transformed by symmetry operations until it coincides with a previously tabulated function. If it cannot be made to coincide, it is itself tabulated as a basic function. Furthermore, the selection of those functions which are consistent as defined in this paper requires that the solutions for all the basic functions be found. Such a task becomes almost impossible even with the largest computers for more than four variables.

Admitting the operation of inverting, for four variables it is only necessary to catalog 14 consistent functions. Classifying them according to the number of true bits, we have Table III. The binomial coefficient $\binom{k}{m}$ stands for k true bits out of $m = 2^n$ states of the truth table. The above solutions were extracted from a table of all four variable combinational linear-input switching circuits derived by R. C. Minnick by means of the Simplex algorithm of linear programming, using the Burroughs 220 computer. Since the form of the primitive solution of the switching circuit is known, it should be possible to construct the entire set of primitives for any number of variables without reference to the functions themselves. This possibility is presently being studied.

TABLE III

PRIMITIVE SOLUTIONS OF CONSISTENT, FOUR-VARIABLE FUNCTIONS

	$\binom{1}{16}$	$\binom{2}{16}$	$\binom{3}{16}$	$\binom{4}{16}$		$\binom{5}{16}$		$\binom{6}{16}$		$\binom{7}{16}$		$\binom{8}{16}$		
Solution	1	1	2	1	2	3	2	2	3	3	4	1	3	2
	−1	0	−1	0	−1	−1	−1	0	−1	−1	−1	0	−1	0
	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−2	0	−1	−1
	−1	−1	−2	−1	−1	−2	−1	−1	−2	−1	−2	0	−1	−1
	−1	−1	−2	−1	−2	−3	−1	−2	−2	−3	−3	−1	−2	−1
Function	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	0	0	0	1	0	1	0	1	1	1	1	1	1	1
	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	1	0	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	1	0	1	1	0
	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	0	0	0	0	0	0	1	0	1	0	1	0	1	1
	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0

chosen so as to accommodate the ONE densities of the successive spans. An example is given in Appendix II where the solution of subfunction A of the function partitioned in Appendix I is derived.

The labor of designing the solution for the reduced and transformed function could be avoided if there were tables of switching circuits for consistent functions available. The table of all switching circuits for four-variable functions such as given by Aiken[1] is arrived at by an exhaustive process requiring that each function

DISCUSSION

The work reported here stems from earlier work on the design of combinatorial magnetic logic by means of an automatic computer, programmed with the Simplex algorithm.[7] The Simplex procedure essentially solves a

[7] R. C. Minnick, "Synthesis of Linear-Input Logic by the Simplex Method," presented at the Sixth Annual Symp. on Computers and Data Processing of the Denver Res. Inst., Denver, Colo.; July 30, 1959.

set of linear inequalities corresponding to the constraints imposed by the form of the linear input circuit of a threshold device. Since each state of the truth table is considered an independent inequality and the number of states equals 2^n, the capacity of even the largest computers is very soon taxed with an increasing number of variables.

It is the aim of the reported work to reduce the required computations, while retaining the Simplex approach, to a point where functions of seven or eight variables can easily be managed by hand computations, or perhaps ten variables if the method itself can be programmed for an automatic computer.

Appendix I

Partitioning of a Five-Variable Function

State	F	Consistent Functions					
		A	B	C	D	E	F
0	1	0	0	1	0	0	0
1	0	0	0	0	0	0	0
2	0	0	0	0			
3	1	1	0	0			
4	1	0	0	1			
5	1	1		0			
6	0	0		0			
7	1	1		0			
8	0	0		0			
9	0	0		0			
10	0	0			0		
11	0	0			0		
12	1	0			1		
13	1	1			0		
14	1	0			1		
15	1	1			0		
16	0	0			0	0	
17	1	0			0	1	
18	0	0				0	
19	0	0				0	
20	0	0					0
21	1	1	0				0
22	1	0	0				1
23	1	1	0				0
24	0	0	0				
25	1	0	1				
26	1	0	1				
27	1	0	1				
28	0	0	0				
29	0	0	0				
30	0	0	0	0	0	0	0
31	1	1	0	0	0	0	0

First Partition

√	√	√	√					√	
1	0	1	1	1	0	0	1		
1	*I*	1	1	0	0	0	0		
1	*I*	1	0	0	0	*I*	0		first sieve
1	0	0	0	*I*	*I*	*I*	0		
I	*B*	*C*	*A*	*C*	*C′*	*A′*	*C*		
	B′			*C′*					solutions

The checked columns have compatible solutions. The true bits of the EXCLUSIVE-OR functions in columns 2 and 5 are treated as separate functions. The lower bit of column 5, representing a C' solution is stricken out.

0	0	0	0	1	0	0	1	
1	0	1	0	1	0	1	1	
0	0	0	0	0	0	0	0	second sieve
1	0	0	0	1	0	1	1	
D′	0	*B*	0	*B*	0	*D′*	*B*	solutions

All columns compatible, all bits pass second sieve.

0	0	0	0	*I*	0	*I*	*I*	
0	0	1	0	1	0	1	0	
0	0	0	0	0	0	0	0	third sieve
1	0	1	0	1	0	1	1	
C′	0	*D′*	0	*B*	0	*B*	*C*	
							C′	solutions
C′	0	*D′*	0	*D′*	0	*D′*	*C′*	

Striking out the bits in the first row converts the solutions to those shown below the line, all of which are compatible.

Taking the columns of the third sieve in order from the right, the first partition results in the function marked A, which is consistent. Its solution is:

$$S = \begin{bmatrix} -3 \\ 3 \\ 1 \\ 2 \\ -1 \\ -1 \end{bmatrix}.$$

The successive partitionings proceed in a similar manner.

Appendix II

Design of Subfunction A in Appendix I

M_6	A	Permute x_1,x_5 $\widehat{1,5}$	Complement x_5 $5'$	Suppress x_5 $\bar{5}$	Complement x_3 $3'$	Permute x_3,x_4 $\widehat{3,4}$	Complement x_2 $2'$	Span Label
−3	0	0	0	0	1	1	1	
0	0	0	0	0	1	1	1	
−2	0	0	1	1	1	1	1	I
1	1	0	0	0	1	1	1	
−1	0	0	1	1	0	1	1	
2	1	0	1	1	0	0	1	
0	0	0	1	1	1	1	1	C
3	1	0	1	1	0	1	0	
−4	0	0	0	0	1	0	1	
−1	0	0	0	0	0	0	0	
−3	0	0	0	0	1	1	0	C
0	0	0	0	0	1	0	0	
−2	0	0	1	1	0	0	0	
1	1	0	0	0	0	0	0	
−1	0	0	1	1	0	0	0	O
2	1	0	1	1	0	0	0	
−4	0	0	0					
−1	0	0	0					
−3	0	1	0					
0	0	0	0					
−2	0	1	0					
1	1	1	0					
−1	0	1	0					
2	1	1	0					
−5	0	0	0					
−2	0	0	0					
−4	0	0	0					
−1	0	0	0					
−3	0	1	0					
0	0	0	0					
−2	0	1	0					
1	1	1	0					

The solution of the reduced and transformed function is composed only of the minimal solution C which is:

$$S_0 = \begin{bmatrix} 2 \\ -1 \\ -1 \end{bmatrix}.$$

The input value of the bias x_0 is taken equal to $+3$ in order to make the first span an I function. Adjusting for the second span requires that x_3 have the input value of -1. The variable x_4 which controls the third and fourth spans has the value of -2. The primitive solution is, therefore:

$$S = \begin{bmatrix} 3 \\ -1 \\ -1 \\ -1 \\ -2 \end{bmatrix}.$$

To transform the solution, the above transformations are applied in reverse order:

$$S \quad \begin{bmatrix} 3 \\ -1 \\ -1 \\ -1 \\ -2 \end{bmatrix} \qquad 2' \cdot S = S_1 \quad \begin{bmatrix} 2 \\ -1 \\ 1 \\ -1 \\ -2 \end{bmatrix} \qquad \widehat{3,4} \cdot S_1 = S_2 \quad \begin{bmatrix} 2 \\ -1 \\ 1 \\ -2 \\ -1 \end{bmatrix} \qquad 3' \cdot S_2 = S_3 \quad \begin{bmatrix} 0 \\ -1 \\ 1 \\ 2 \\ -1 \end{bmatrix}$$

$$\bar{5} \rightarrow S_4 \quad \begin{bmatrix} 0 \\ -1 \\ 1 \\ 2 \\ -1 \\ -3 \end{bmatrix} \qquad 5' \cdot S_4 = S_5 \quad \begin{bmatrix} -3 \\ -1 \\ 1 \\ 2 \\ -1 \\ 3 \end{bmatrix} \qquad \widehat{1,\bar{5}} \cdot S_5 = S_6 \quad \begin{bmatrix} -3 \\ 3 \\ 1 \\ 2 \\ -1 \\ -1 \end{bmatrix}.$$

The desired solution is S_6, which is evaluated in the column M_6.

CORRECTION

A. W. Straiton and C. W. Tolbert, authors of "Anomalies in the Absorption of Radio Waves by Atmospheric Gases," which appeared on pages 898–903 of the May, 1960, issue of PROCEEDINGS, have requested that Table I of their paper be corrected as follows.

TABLE I

WATER VAPOR AND OXYGEN LOSSES AT 12,000 TO 14,000 FEET ELEVATION

Wavelength (mm)	Attenuation in db/km	
	Water vapor (1 g/m³)	Oxygen
8.6	0.003	—
4.3	0.01	0.22
2.15	0.12	—

Flow Table Logic*

P. R. LOW†, MEMBER, IRE AND G. A. MALEY†

Summary—**Micro-miniature systems have been proposed which will use packing densities on the order of 10^6 active elements per cubic foot. The interconnecting of these elements has been of great concern to the authors. With these packing densities in mind, the authors have suggested that a complete new theory of machine organization be found. One such method is suggested, whereby rather large sequential circuits are implemented directly from their flow table representations. This method does require more active elements, but the interconnection problem is greatly reduced.**

Introduction

MUCH has been written in the last few years about the device aspects of micro-miniature systems. The possibility of having anywhere from 10^6 [1] to 10^{12} [2] active elements per cubic foot has been indicated. The problem of interconnecting these elements has, understandably, concerned most of the authors. It has become increasingly apparent that the solution to this problem will not be obtained by miniaturizing the wiring. In fact, there is general agreement that if one is to utilize packing densities of this magnitude, a new look should be taken at the logic and organization of a computer system. Such a reexamination might lead to a new system of logic and, perhaps, a complete new theory of machine organization. This paper represents the results of one such study. This study was originally concerned with the combinatorial problems found in computer systems. As the work progressed, however, it appeared that more could be gained by extending the investigation to sequential problems. The ultimate objective was to treat a computer as a single sequential circuit. If this goal were achieved, one might be able to design a computer that made extensive use of regular patterns of similar components (a prime requirement of any system using micro-miniature devices). While the progress in this direction has been rather modest, there is the thought that the concept presented here, after suitable modification and extension, may contribute to the efficient utilization of the so-called batch-fabricated devices.

In any attempt to evaluate a new idea, a measure of some sort must be established. With this aim in mind, the first section of this paper is devoted to a brief review of one of the existing techniques for sequential circuit design. The authors' techniques will then be discussed and implemented, and finally the two methods will be compared, with particular emphasis on the potential application for batch-fabricated devices.

Synthesis of Sequential Circuits

By definition, a sequential circuit is one in which the present output is a function not only of the present inputs, but also the past history of these inputs. Dr. D. R. Huffman[3] has suggested that a chart, called a "flow table," be used to record these past input conditions and that this chart be used to define the operation of the desired circuitry. The vertical columns of this chart are labelled to indicate all possible input conditions. The horizontal rows are labelled to indicate all possible conditions of the memory elements within the circuitry.

For the purpose of illustration, we shall explain the use of this chart in terms of relay technology. A relay may be thought of as being in one of two distinct conditions: stable or unstable. The stable condition of a relay may be defined as a state of equilibrium. The circuit may be energized with the armature attracted to the coil or the relay may be de-energized with the armature held away from the coil by spring action. In either case, the armature is stabilized and will not move as long as the input to the relay coil is unchanged. These conditions of stability will be displayed on the chart as circled numbers. The unstable conditions of the relay will be shown as uncircled numbers on the chart and will be used to indicate a state of nonequilibrium. The relay coil may be energized with the armature not yet seated against the coil or the coil may be de-energized with the armature still in the energized position. It is quite clear that the relay cannot remain in an unstable condition for any extended period of time. This concept of stability and nonstability may now be extended to include a group of interconnected relays. If any relay in the group is nonstable, then the state represented by the group is considered unstable. Therefore, only if all relays are stable will we consider the group to be stable. A circled number will, therefore, indicate a stable group of relays where the group may have one or more relays. An uncircled number will be used to indicate the nonstable condition of a group.

It is possible now to explain the operation of a sequential circuit by indicating on a flow table the movement of the operating point between stable conditions and nonstable conditions. As an example, we shall design a circuit that will operate as described by the timing chart in Fig. 1. The reader will recognize that this

* Received by the IRE, August 2, 1960.
† IBM Corp., Poughkeepsie, N. Y.
[1] R. Norman, J. Lost and I. Haas, "Solid State Micrologic Elements," presented at *1960 Internatl. Solid State Circuits Conf.*; February, 1960.
[2] D. A. Buck and K. R. Shoulders, "An Approach to Micro-Miniature Printed Systems," presented at *Eastern Joint Computer Conf.*, December, 1958.
[3] D. A. Huffman, The Synthesis of Sequential Switching Circuits," Ph.D. dissertation, Elec. Engrg. Dept., Mass. Inst. Tech., Cambridge, Mass.; 1953.

timing chart represents the waveforms found in a four-stage ring or a binary trigger.

The design of a sequential circuit can be broken down into four steps.

1) Translate the statement of the problem into the primitive flow table.
2) Assign circuit conditions to each row in the table.
3) Determine energization required for each unstable state.
4) Write the equation from the Karnaugh Map and simplify, if possible.

1) From this timing diagram we are able to determine that the required circuitry must have four stable states. Stable states (1) and (3) occur when the input is down while (2) and (4) occur while the input is up. From the timing diagram we are also able to determine that the circuitry should move from (1) to (2) to (3) to (4) and back to (1) as the input is raised and lowered. This movement is shown on the flow table in Fig. 2(a).

Let us assume the input is down and the circuitry is in stable state (1). As the input is raised the operating point moves horizontally from (1) to (2). The circuitry is now in a nonstable condition and will move to stable state (2). As the input is lowered, the operating point moves horizontally to (3) and then vertically to (3). This procedure, first, of moving the operating point horizontally by changing the input conditions, then having the circuitry seeking a stable point by moving the operating point vertically, will completely define the operation of the logic configuration.

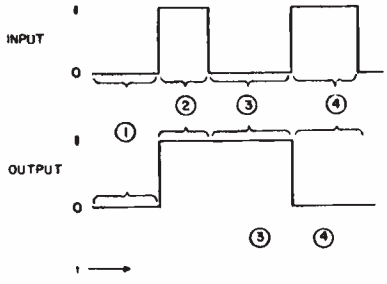


Fig. 1.

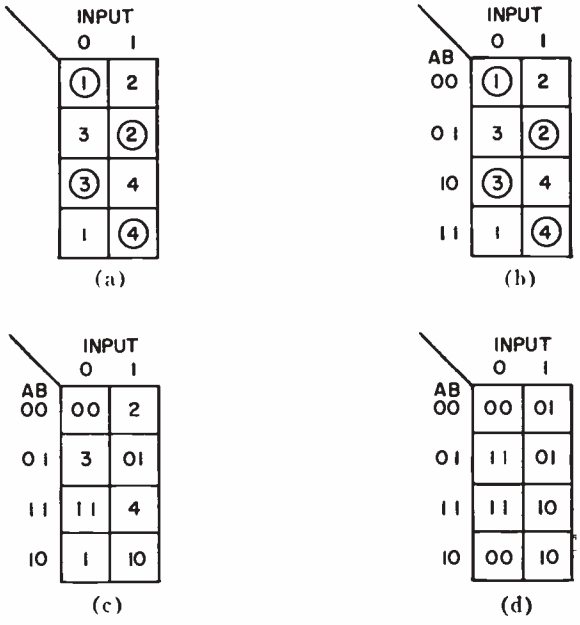


Fig. 2.

2) The next major step in the design of a sequential circuit is that of assigning relay conditions to each row of the table. Since our example has four rows, two relays will be required, *i.e.*, 2-binary bits required to code 4 states. This assignment problem is very complicated and will drastically affect the resulting logic configuration in any problem of reasonable size [see Fig. 2(b)].

3) Since the stable states will require an excitation equal to the conditions of the relays, all stable states are replaced with binary numbers located to the left of the table. In Fig. 2(c) note that the binary numbers in the flow table refer to the excitation applied to the relays, whereas the binary numbers in the left column refer to the actual condition of these relays. When the excitation and the condition are the same, the relays are stable. Similarly, when they are not the same, the relays are unstable.

Nonstable states are now replaced by the energization required to move them to the desired stable states [see Fig. 2(d)].

4) At this point we have obtained a Karnaugh Map of a two-output problem.

$$T_1 = \bar{I}B + IA$$
$$T_2 = \bar{I}B + I\bar{A}.$$

T_1 is actually the input to the coil of relay A, while T_2 is the input to relay B, and I is the input to the circuit.

These equations may be rewritten as

$$T_1 = \bar{I}AB + IA + AB$$
$$T_2 = \bar{I}AB + I\bar{A} + \bar{A}B.$$

These two equations may be implemented as illustrated by Caldwell.[4] The resulting circuit appears in Fig. 3.

While the procedure given here has been greatly oversimplified, it is hoped that the reader has gained some insight into the technique developed by Dr. Huffman. Such questions as hazards, race conditions, and output matrices have purposely been deleted, but must be included to produce a useful circuit.

Flow Table Logic

The technique to be presented here replaces steps 2), 3), and 4) discussed above. It should be noted that this represents the major portion of the problem. Thus the elimination of these steps will drastically reduce the labor involved in sequential circuit design. There is

[4] S. H. Caldwell, "Switching Circuits and Logical Design," J. Wiley & Sons, Inc., New York, N. Y.; 1958.

an additional and perhaps more significant advantage. The circuit designed using Flow Table Logic is extremely regular. This should be a definite advantage when used to design circuits for the so-called micro-miniature, or molecular electronic, systems.

The basic configuration consists of a grid of conductors having insulated crossings. For visualization purposes, the vertical conductors can be related to the columns in a Huffman flow table and the horizontal conductors can be related to the rows of the flow table. Two types of active elements are used. One is a device with the characteristics shown in Fig. 4(a), which will be called a "conditional latch" in this discussion. The second is a transfer element. It is used as an "AND" circuit, as shown in Fig. 4(b). The conditional latch is placed at the intersection of a column and a row in a position corresponding to the position of the stable state in the flow table. The conditional latch is connected to a row in such a way that its output is fed along the entire length of the horizontal connector in that row [see Fig. 4(c)]. Thus the information from the latch is transmitted to all other elements connected on this row. The function of the transfer element is to transfer a logical "1" from the horizontal buss vertically to a particular latch. In all cases the latch is located in the same column as its corresponding transfer point.

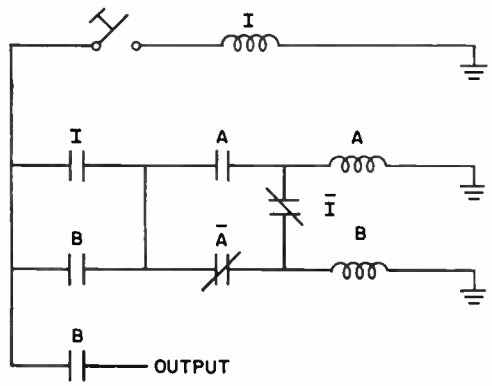


Fig. 3.

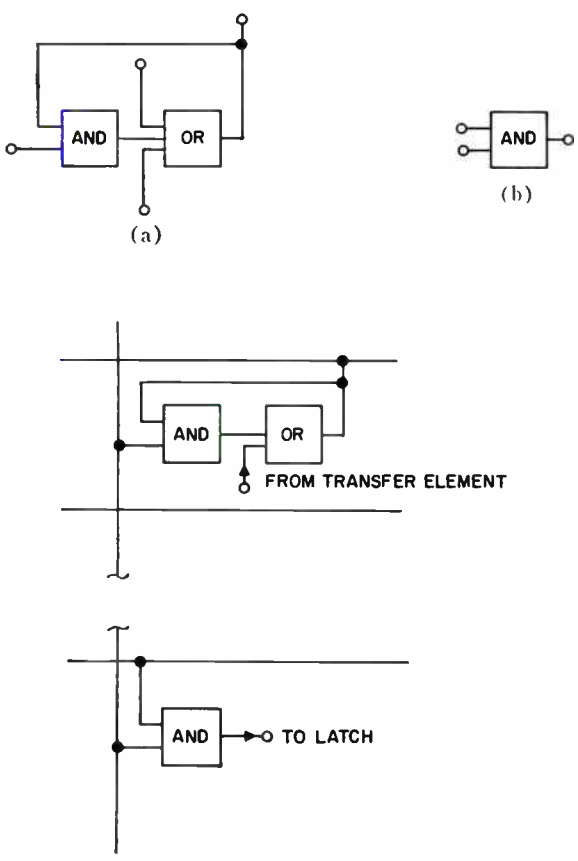
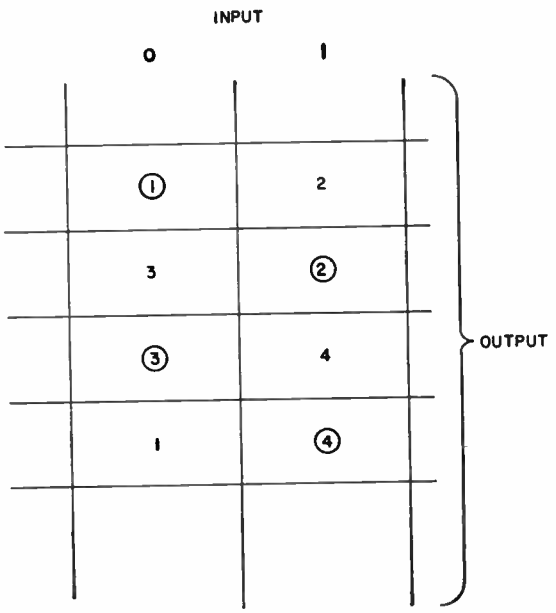


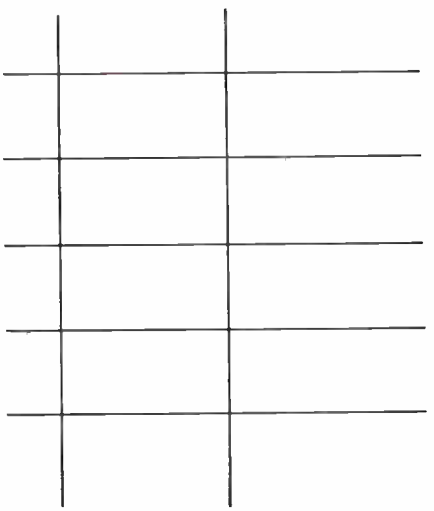
Fig. 4.—(a) Conditional latch. (b) Transfer element.

To understand the operation of the flow table, let us take as an example the problem worked out in the previous section with the conventional approach of Caldwell[4] and solve it by using the Flow Table Logic technique. The matrix of conductors is set up with a horizontal conductor for each row and a vertical conductor for each column in the flow table. Storage or latch circuits are then connected at points in the matrix of the conductors in a position which corresponds to the stable states in the flow table. For example, stable state ① in Fig. 5(a) is represented by latch 1 in Fig. 5(c), stable state ② by latch 2, and so forth. Next, the unstable or transfer elements must be connected. The transfer points correspond in position and in function to the unstable states in the flow table. The final step is to wire the output of each unstable state to its corresponding stable state, as shown in Fig. 5(d). One should note in passing that these wirings or conductor patterns proceed only along vertical columns, never crossing a column, thus simplifying the design of a circuit and the package to house it. Having constructed the circuit, let us now attempt to gain some understanding of its operation by tracing the switching of the circuits involved. We will then see that it does perform the function stipulated in the problem and that suitable outputs can be made available to drive other similar circuits or perhaps combinatorial logic. The input is supplied in the form of electrical signals on the vertical conductors. In this case, there would be two inputs corresponding to a normal and complemented drive for the ring problem to be solved. If the circuit is to perform as expected, the outputs as indicated by lines A, B, C, and D should come up in turn, last for 1 clock period, and then drop. The waveform shown in Fig. 1 can be obtained by the combination of lines A and D to form one output and B and C the complement.

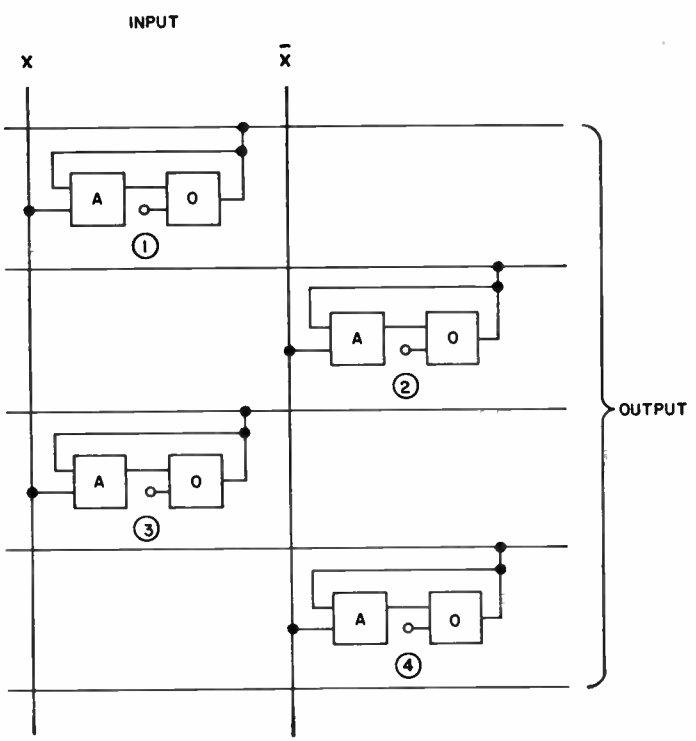
In order to start the problem let us assume that line X is plus, and that stable state ① is the "1" state. The output of the OR circuit is plus, conditioning one of the inputs of the AND circuit. The X line energizes the other input of the AND circuit, causing its output to be plus. The circuit will remain in this state regardless of the state of the other inputs to the OR circuit. In addition, note that the output of the latch driving hori-



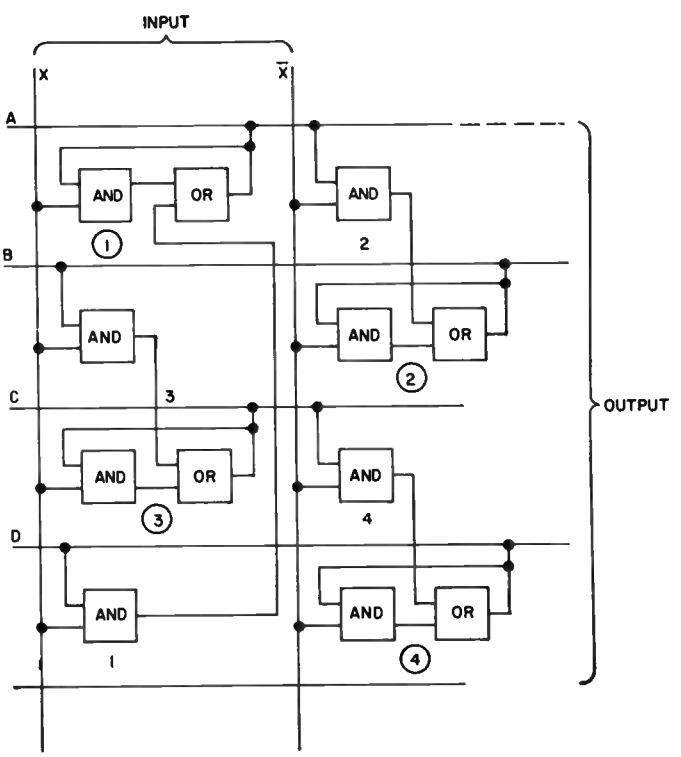
(a)



(b)



(c)



(d)

Fig. 5.

zontal row A is plus. This conditions one leg of the AND circuit representing unstable state 2 (and incidentally any other circuits which might be connected to this buss). When the input is switched from X to $\overline{X}$, the other leg of the AND circuit representing unstable state 2 is conditioned, thus giving us a positive output. This is fed to the OR circuit of stable state ②, causing its output to go positive. This then conditions one leg of the AND circuit in stable state ②. Since the other input is driven by the $\overline{X}$ bus, the output goes up, and stable state ② is now in a "1" condition. Row B is plus and the ring has stepped from position A to position B. Note that with the removal of the signal from the X line one leg of the AND circuit in stable state ① goes to "0," and the signal on line A returns to its "0" level. When the input is returned to the X line, the AND circuit in unstable state 3 will go to the "1" state since row B has been up, conditioning the other leg of this AND circuit. This, in fashion similar to above, will set stable state ③ and the C buss to the "1" state. The removal of the signal from the $\overline{X}$ line deconditions the AND circuit in stable state ② and this circuit resets. Note that when the signal was applied to the X line stable state ① did not go on, since the other input to the AND circuit was at the "0" level. The fourth step in the counting action, that of returning the signal to the $\overline{X}$ line for the second time, will transfer the "1" from stable state ③ to unstable 4 and then to stable state ④, thus bringing up the D line. The removal of the X pulse for the second time deconditions stable state ③ and line C drops to the "0" level. This now completes the full cycle of the ring and return of the input again to the X line will set stable state ① on and will reset stable state ④.

This technique, while simple in concept, has a problem which should be noted at this point. It has been assumed that the output from a stable state remains at plus level long enough to transfer the information through the unstable state to the next stable state. To insure that this is done, one of two precautions must be taken. The first would be to insert a temporary storage or delay element as shown in Fig. 6. This would insure that the output to the horizontal bus remained up (at the positive level) for a certain period of time after the input line to that stable state had been removed. It then should have a delay equal to that of the AND circuit in the unstable state plus that of the OR circuit in the stable state. The alternative precaution would be to insure that the X line remained up for a short period of time after the $\overline{X}$ line was brought up. The danger here is that a race condition may result wherein stable state ① transfers to stable state ②, but since the X line has remained up, stable state ② may transfer back to stable state ③. This in itself would be no problem unless stable state ③ could then transfer to stable state ④ before the X line dropped. If this condition were not avoided, it would be possible to have two "1's" or two stable states on at the same time.

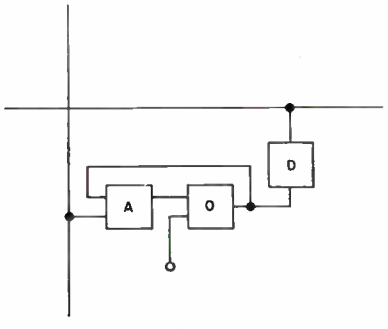


Fig. 6.

As one might expect, certain technologies or switching circuit techniques lend themselves to Flow Table Logic implementation better than others. For the purpose of this paper, we shall discuss one embodiment, although this is by no means the only one that exists. One of the interesting developments in recent years to come to the attention of computer designers is that of optoelectronics. Two embodiments of this technology, Neon-Photoconductor (Neon-PC) and Electroluminescent-Photoconductor circuitry (EL-PC), are ideally suited to the implementation of Flow Table Logic. In the interest of simplicity we shall confine ourselves to the Neon-PC version, keeping in mind that one can make a one-for-one substitution with EL-PC elements. In fact, the planar nature of the flow table design is ideally suited to the packaging potential of EL-PC elements.

A Neon-PC storage element and transfer element are shown in Fig. 7. Note that these two elements are identical except for a single connection, that of one terminal of the PC. This will certainly simplify fabrication of any system employing these devices. The Neon-PC flow table solution to the problem previously presented diagramatically with AND and OR circuits appears in Fig. 8. Let us once again trace through the operation of the ring or counter circuit. The input signals will be considered to be positive voltages sufficient to maintain the Neon-PC storage element in an "on" state (note that the negative resistance of the neon itself is *not* used), provided that it has been set that way by a suitable input signal. Assuming now that stable state ① is in the "1" or illuminated condition and that the input has been applied to the X row, we find that the photoconductor PS1 is in the low resistance state, neon NS1 is "on," and buss A is at some small positive potential above ground. As the input signal is transferred from line X to line Y, neon NS1 will be extinguished (it will not be de-ionized instantly, but the light will go out in a very short period of time). Photoconductor PS1, however, will remain in the low resistance state for a certain period of time, allowing neon NU2 to fire. The conduction path for this state is indicated by the dotted line in Fig. 8. The output of neon NU2 will then lower the resistance of photoconductor PU2, which will in turn cause neon NS2 to fire. This will reduce the resistance of photoconductor PS2 and

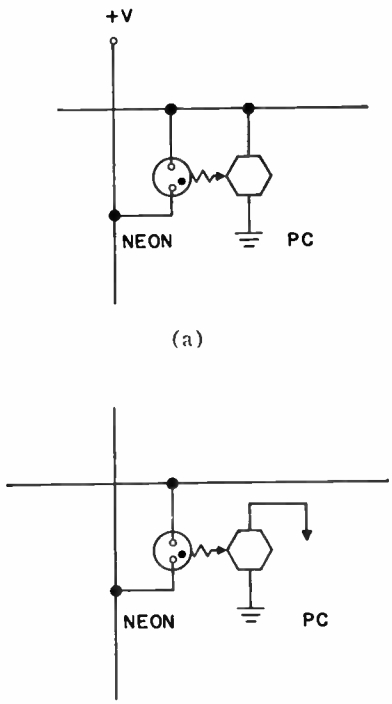


Fig. 7.—(a) Neon-PC storage element.
(b) Neon-PC transfer element.

thus maintain the current in NS2 by means of the optical feedback. During this time, photoconductor PS1 is decaying to its dark or high resistance level, and neon NU2, having no path through which it may conduct, is extinguished. However, the transfer of the bit from stable state ① to stable state ② has been accomplished. The return of the voltage to the X line will proceed, in a similar fashion, to fire neon NU3, lower the resistance of photoconductor PU3, fire neon NS3, and finally energize photoconductor PS3. The operation then continues, with alternate applications of input to the X and Y terminals, to advance the "on" or illuminated state through the Flow Table Logic circuit. It is possible to design the photoconductor in such a way that its turn-on or rise time is considerably shorter than its turn-off or fall time, thus providing the delay required for reliable flow table operation.

In an attempt to illustrate further the simplicity and regularity of the Flow Table circuit, a combination lock was designed using first the conventional technique and then the Flow Table system. The primitive flow table for this problem is shown in Fig. 9. The lock was designed to open only if the inputs 1, 2, 3, 4 were selected in that sequence. Any deviation from this sequence was to disable the lock.

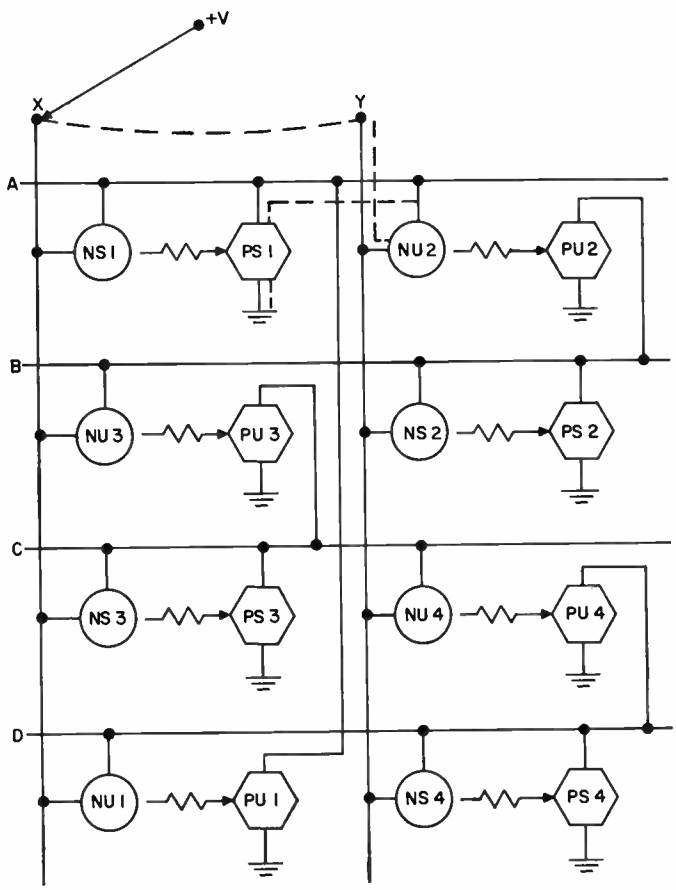


Fig. 8.

$\bar{1}\bar{2}\bar{3}\bar{4}$	1	2	3	4	
①	2	13	14	15	
3	②				
③	12	4	14	15	
5		④			
⑤	12	13	6	15	
7			⑥		
⑦	12	13	14	8	
⑨				⑧	
⑪	⑫	⑬	⑭	⑮	

Fig. 9.

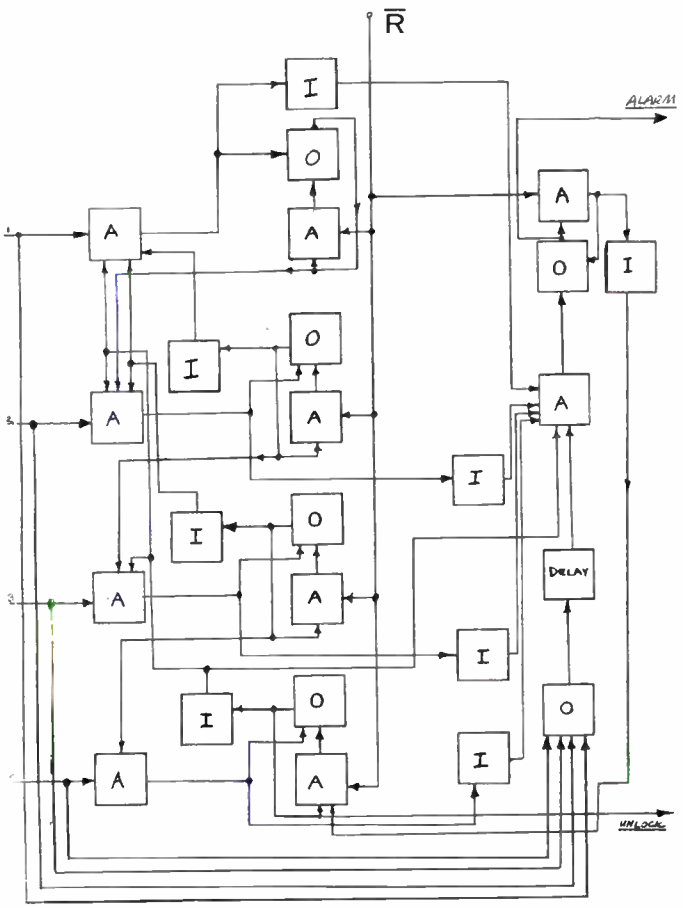


Fig. 10.

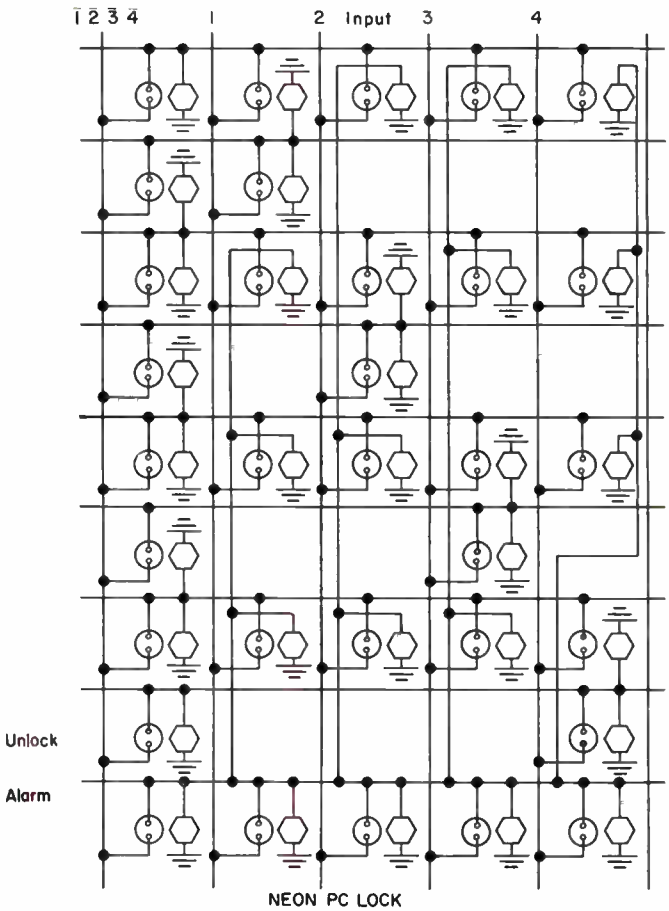


Fig. 11.

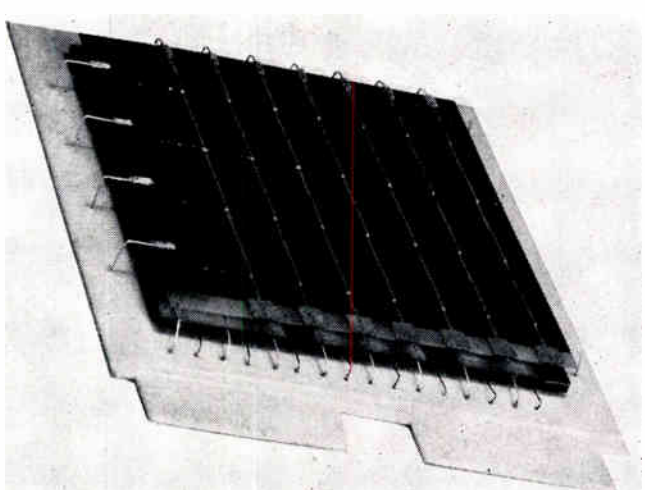


Fig. 12.

The conventional solution to the problem is shown in Fig. 10. A few moments of study will indicate that it does in fact perform the required operation. The Flow Table Logic solution is shown in Fig. 11. Again the problem is easily checked for correct performance.

The simplicity of the wiring and the regularity of the circuit are quite apparent. Such an approach should certainly prove valuable when batch-fabricated devices become a reaility. As was stated earlier, when applied to one such technology (EL-PC) the design and fabrication of circuits is greatly simplified. An early model of an EL-PC combination lock is shown in Fig. 12.

Conclusion

The Flow Table Logic technique for circuit design presented here was intended for use with batch-fabricated (or perhaps micro-miniature) devices, hence the emphasis on simplicity and regularity. These are obtained in some cases at the expense of actual component count. The exchange was felt to be acceptable, however, since minimizing the number of active elements is not guarantee of minimum cost. An interesting point that should be considered is the logical delay associated with circuits designed by the Flow Table Logic technique. The circuit can go from one state to any other state in approximately two logical delays. Thus one has not sacrificed speed in the quest for regularity. The ease of circuit design should also be an advantage of this technique.

As is true in most developments, there are some problem areas that still require investigation. The coding of the input lines and, in fact, the coding of the states of the flow table are far from optimum. Only further work can reveal whether this can be improved without sacrificing the simplicity of the circuit. In addition, the necessary delay required is not found in all technologies and thus must be carefully considered in the solution of a problem.

Acknowledgment

The material presented represents the efforts of the authors plus that of R. J. Domenico. In addition, the authors are indebted to E. J. Skiko, J. Earle, and R. Robelen for many helpful discussions. The EL-PC combination lock was constructed by Dr. J. A. O'Connell and B. Narken.

Cyclic Codes for Error Detection*

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***Summary*—Cyclic codes are defined and described from a new viewpoint involving polynomials. The basic properties of Hamming and Fire codes are derived. The potentialities of these codes for error detection and the equipment required for implementing error detection systems using cyclic codes are described in detail.**

Introduction

Of the many developments in the area of error-detection and error-correcting codes during the past three years, probably the most important have pertained to cyclic codes. Since their introduction by Prange,[1] very attractive burst-error correcting cyclic codes have been found by Abramson,[2,3] Fire,[4] Melas,[5] and Reiger.[6] Cyclic codes for correcting random errors have been found by Prange,[1] Green and San Soucie,[7,8] Bose and Ray-Chaudhuri,[9] and Melas.[10] Encoding and

* Received by the IRE, August 1, 1960; revised manuscript received October 28, 1960.

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[1] E. Prange, "Cyclic Error-Correcting Codes in Two Symbols," Air Force Cambridge Research Center, Bedford, Mass., Tech. Note AFCRC-TN-57-103, September, 1957; "Some Cyclic Error-Correcting Codes with Simple Decoding Algorithms," Tech. Note AFCRC-TN-58-156, April, 1958; "The Role of Coset Equivalence in the Analysis and Decoding of Group Codes," Tech. Note AFCRC-TR-59-164; June, 1959.

[2] N. M. Abramson, "A Class of Systematic Codes for Non-Independent Errors," Electronics Res. Lab., Stanford University, Stanford, Calif., Tech. Rept. No. 51; December, 1958.

[3] N. M. Abramson, "Error Correcting Codes from Linear Sequential Networks," presented at the Fourth London Symp. on Information Theory, London, Eng.; August, 1960.

[4] P. Fire, "A Class of Multiple-Error-Correcting Binary Codes for Non-Independent Errors," Sylvania Electric Products, Inc., Mountain View, Calif., Rept. No. RSL-E-2; March, 1959.

[5] C. M. Melas, "A new group of codes for correction for dependent errors in data transmission," *IBM J. Res. Dev.*, vol. 4, pp. 58–65; January, 1960.

[6] S. H. Reiger, "Codes for the correction of clustered errors," IRE Trans. on Information Theory, vol. IT-6, pp. 16–21; March, 1960.

[7] J. H. Green, Jr., and R. L. San Soucie, "An error-correcting encoder and decoder of high efficiency," Proc. IRE, vol. 46, pp. 1744–1755; October, 1958.

[8] N. Zeiler, "On a Variation of the First Order Reed-Muller Codes," M.I.T. Lincoln Lab., Lexington, Mass., pp. 34–80; October, 1958.

[9] R. C. Bose and D. K. Ray-Chaudhuri, "A class of error-correcting binary group codes," *Information and Control*, vol. 3, pp. 68–79, March, 1960; "Further results on error correcting binary group codes," *Information and Control;* to be published.

[10] C. M. Melas, "A cyclic code for double error correction," *IBM J. Res. Dev.*, vol. 4, pp. 364–366; July, 1960.

error correcting procedures for these codes are relatively easily implemented using shift-registers with feedback connections.[11,12]

The first function of this paper is to introduce cyclic codes from a new viewpoint requiring only elementary mathematics and to derive the basic properties of Hamming and Fire codes. Second, the potentialities of cyclic codes for error detection and the equipment required for implementing error detection systems using cyclic codes are described in detail.

Polynomial Representation of Binary Information

We will be concerned with coding a message of k binary digits by appending $n-k$ binary digits as a check and transmitting the k information digits and then the $n-k$ check digits. It is convenient to think of the binary digits as coefficients of a polynomial in the dummy variable X. For example, a message 110101 is represented by the polynomial $1+X+X^3+X^5$. The polynomial is written low-order-to-high-order because these polynomials will be transmitted serially, high-order first, and it is conventional to indicate signal flow as occurring from left to right.

These polynomials will be treated according to the laws of ordinary algebra with one exception. Addition is to be done modulo two:

$$1X^a + 1X^a = 0X^a \qquad 1X^a + 0X^a = 1X^a = 0X^a + 1X^a$$
$$0X^a + 0X^a = 0X^a \qquad -1X^a = 1X^a.$$

For example:

addition

$$\begin{array}{r} 1+X \qquad +X^3+X^4 \\ X+X^2 \qquad +X^4 \\ \hline 1+X+X^2 \qquad +X^4 \\ X \qquad +X^3+X^4 \end{array}$$

multiplication

$$\begin{array}{r} 1+X \qquad +X^3+X^4 \\ 1+X \\ \hline 1+X \qquad +X^3+X^4 \\ X+X^2 \qquad +X^4+X^5 \\ \hline 1 \qquad +X^2+X^3 \qquad +X^5 \end{array}$$

In addition to the associative, distributive, and commutative properties of polynomials under this kind of algebra, we have, as in ordinary algebra, unique factorization; that is, every polynomial can be factored into prime or irreducible factors in only one way.[13]

Algebraic Description of Cyclic Codes

A cyclic code is defined in terms of a generator polynomial $P(X)$ of degree $n-k$. A polynomial of degree less than n is a code polynomial, *i.e.*, acceptable for transmission, if and only if it is divisble by the generator polynomial $P(X)$.[14] With this definition, the sum of two code polynomials is also a code polynomial, for if $F_1(X)$ and $F_2(X)$ are polynomials of degree less than n, which are divisible by $P(X)$, then $F_1(X)+F_2(X)$ is also of degree less than n and divisible by $P(X)$. Therefore, these codes are a special case of group codes, as studied by Slepian.[15]

If $P(X)$ has X as a factor, then every code polynomial has X as a factor and, therefore, has its zero-order coefficient equal to zero. Since such a symbol would be useless, we will consider only codes for which $P(X)$ is not divisible by X.

Code polynomials can be formed by simply multiplying any polynomial of degree less than k by $P(X)$. The following method has the advantage, however, that it results in a code polynomial in which the high-order coefficients are message symbols and the low-order coefficients are check symbols. To encode a message polynomial $G(X)$, we divide $X^{n-k}G(X)$ by $P(X)$ and then add the remainder $R(X)$ resulting from this division to $X^{n-k}G(X)$ to form the code polynomial:

$$X^{n-k}G(X) = Q(X)P(X) + R(X),$$

where $Q(X)$ is the quotient and $R(X)$ the remainder resulting from dividing $X^{n-k}G(X)$ by $P(X)$. Since in modulo two arithmetic, addition and subtraction are the same,

$$F(X) = X^{n-k}G(X) + R(X) = Q(X)P(X),$$

which is a multiple of $P(X)$ and, therefore, a code polynomial. Furthermore, $R(X)$ has degree less than $n-k$, and $X^{n-k}G(X)$ has zero coefficients in the $n-k$ low-order terms. Thus the k highest-order coefficients of $F(X)$ are the same as the coefficients of $G(X)$, which are the message symbols. The low order $n-k$ coefficients of $F(X)$ are the coefficients of $R(X)$, and these are the check symbols.

Example: Consider a code for which $n=15$, $k=10$, and $n-k=5$ which uses the generator polynomial $P(X)=1+X^2+X^4+X^5$. To encode the message 1010010001 corresponding to the polynomial $G(X)=1+X^2+X^5+X^9$, we divide $X^5G(X)$ by $P(X)$ and find the remainder. By long division it can be found that

$$X^5 + X^7 + X^{10} + X^{14} = (1 + X^2 + X^4 + X^5) \cdot (1 + X + X^2 + X^3 + X^7 + X^8 + X^9) + (1 + X).$$

The code polynomial is formed by adding the remainder $(1+X)$ to $X^5G(X)$:

[11] J. E. Meggitt, "Error correcting codes for correcting bursts of errors," *IBM J. Res. Dev.*, vol. 4, pp. 329–334; July, 1960.

[12] W. W. Peterson, "Error Correcting and Error Detecting Codes," Technology Press, Cambridge, Mass., to be published.

[13] See, for example, R. D. Carmichael, "Introduction to the Theory of Groups of Finite Order," Dover Publications, Inc., New York, N. Y., p. 256; 1956.

[14] According to the usual definition, a cyclic code is a group code with the added property that the cyclic shift of a code vector is also a code vector. Codes obtained by making a number of the leading information symbols identically zero and dropping them are called shortened cyclic codes. The codes described in this paper are cyclic codes if X^m-1 is evenly divisible by $P(X)$, and otherwise are shortened cyclic codes. See Prange, footnote 1, and Peterson, footnote 12.

[15] D. Slepian, "A class of binary signaling alphabets," *Bell Sys. Tech. J.*, vol. 35, pp. 203–234; January, 1956.

$$F(X) = (1 + X) + (X^5 + X^7 + X^{10} + X^{14})$$
$$\underbrace{1\ 1\ 0\ 0\ 0}_{\text{check symbols}}\ \underbrace{1\ 0\ 1\ 0\ 0\ 1\ 0\ 0\ 0\ 1}_{\text{information symbols}}.$$

Principles of Error Detection and Error Correction

An encoded message containing errors can be represented by

$$H(X) = F(X) + E(X)$$

where $F(X)$ is the correct encoded message and $E(X)$ is a polynomial which has a nonzero term in each erroneous position. Because the addition is modulo two, $F(X)+E(X)$ is the true encoded message with the erroneous positions changed.

If the received message $H(X)$ is not divisible by $P(X)$, then clearly an error has occurred. If, on the other hand, $H(X)$ is divisible by $P(X)$, then $H(X)$ is a code polynomial and we must accept it as the one which was transmitted, even though errors may have occurred. Since $F(X)$ was constructed so that it is divisible by $P(X)$, $H(X)$ is divisible by $P(X)$ if and only if $E(X)$ is also. Therefore, an error pattern $E(X)$ is detectable if and only if it is not evenly divisible by $P(X)$. To insure an effective check, the generator polynomial $P(X)$ must be chosen so that no error pattern $E(X)$ which we wish to detect is divisible by $P(X)$.

To detect errors, we divide the received, possibly erroneous, message $H(X)$ by $P(X)$ and test the remainder. If the remainder is nonzero, an error has been detected. If the remainder is zero, either no error or an undetectable error has occurred.

Example:

$$\begin{aligned} F(X) &= 1 + X + X^5 + X^7 + X^{10} + X^{14} \\ &= 1\ 1\ 0\ 0\ 0\ 1\ 0\ 1\ 0\ 0\ 1\ 0\ 0\ 0\ 1, \\ E(X) &= X^3 + X^6 + X^7 \\ &= 0\ 0\ 0\ 1\ 0\ 0\ 1\ 1\ 0\ 0\ 0\ 0\ 0\ 0\ 0, \\ H(X) &= F(X) + E(X) \\ &= 1 + X + X^3 + X^5 + X^6 + X^{10} + X^{14} \\ &= 1\ 1\ 0\ 1\ 0\ 1\ 1\ 0\ 0\ 0\ 1\ 0\ 0\ 0\ 1. \end{aligned}$$

This $F(X)$ was taken from the previous example. The remainder after $H(X)$ is divided by $P(X)=1+X^2+X^4+X^5$ is $X^2+X^3+X^4$, and the fact that this is not zero shows that an error must have occurred. The same remainder occurs if $E(X)$ is divided by $P(X)$, since $F(X)$ is divisible by $P(X)$.

The ability of a code to correct errors is related to its ability to detect errors. For example, any code which detects all double errors is capable of correcting any single error. This can be seen by noting that if only a single error occurs, we can try to correct it by trying to change each symbol. A polynomial with one error and one symbol changed can be a code polynomial only if the erroneous symbol is the one which was changed, since all other combinations are equivalent to double errors and, therefore, are detectable. Similarly, a code which detects all combinations of $2t$ errors can correct any combination of t errors, since if t or fewer errors occur, changing all combinations of t or fewer positions results in a code polynomial only if all the erroneous positions are changed. The same argument shows that any code capable of detecting any two error bursts of length b or less can correct any single burst of length b or less. Finally, the converse of these statements is also true; any t-error correcting code can detect any combination of $2t$ errors and any code capable of correcting any single burst of length b can be used instead to detect any combination of two bursts of length b.

Detection of Single Errors

Theorem 1: A cyclic code generated by any polynomial $P(X)$ with more than one term detects all single errors.

Proof: A single error in the ith position of an encoded message (counting from the left and numbering the leftmost position zero) corresponds to an error polynomial X^i. To assure detection of single errors, it is necessary only to require that $P(X)$ does not divide X^i evenly. Certainly no polynomial with more than one term divides X^i evenly. Q.E.D.

The simplest polynomial with more than one term is $1+X$:

Theorem 2: Every polynomial divisible by $1+X$ has an even number of terms.

Proof: Let $F(X)=X^a+X^b+X^c+\cdots=(1+X)Q(X)$. Substituting $X=1$ gives

$$F(1) = 1 + 1 + 1 + \cdots = (1 + 1)Q(1) = 0.$$

There is one "1" in $F(1)$ for each term, and since the sum is zero, there must be an even number of terms. Q.E.D.

It follows that the code generated by $P(X)=1+X$ detects not only any single error, but also any odd number of errors. In fact, the check symbol must simply be an over-all parity check, chosen to make the number of ones in the code polynomial even.

Any polynomial of the form $1+X^c$ contains a factor $1+X$ since $1+X^c=(1+X)(X^{c-1}+X^{c-2}+\cdots+1)$. Therefore, if $P(X)$ contains a factor $1+X^c$, any odd number of errors will be detected.

Double and Triple Error Detecting Codes (Hamming Codes)

A polynomial $P(X)$ is said to belong to an exponent e if e is the least positive integer such that $P(X)$ evenly divides $X^e-1(=X^e+1 \bmod 2)$.

Theorem 3: A code generated by the polynomial $P(X)$ detects all single and double errors if the length n of the code is no greater than the exponent e to which $P(X)$ belongs.

Proof: Detection of all double errors requires that

$P(X)$ does not evenly divide X^i+X^j for any $i, j<n$. We can factor X^i+X^j (assuming $i<j$) to $X^i(1+X^{j-i})$. It is sufficient to require that $P(X)$ should not divide $1+X^{j-i}$, since $P(X)$ is assumed not to be divisible by X. But $j-i<n\leqq e$, and therefore, since $P(X)$ belongs to the exponent e, $P(X)$ cannot divide $1+X^{j-i}$. Thus the code will detect double errors. Since $P(X)$ is not divisible by X and certainly could not be just the constant 1, it must have more than one term, and will, by Theorem 1, detect single errors also. Q.E.D.

It can be shown that for any m there exists at least one polynomial $P(X)$ of degree m that belongs to $e=2^m-1$. This is the maximum possible value of e. Polynomials with this property (usually called primitive polynomials) are always irreducible. A few such polynomials are listed in Appendix II, and more extensive tables are available.[12,16] Thus for any m there is a double-error detecting code of length $n=2^m-1$ generated by a polynomial $P(X)$ of degree m, which therefore, has m check symbols and 2^m-1-m information symbols. These codes can be shown to be completely equivalent to Hamming single-error correcting codes.[2,3,12,17]

Theorem 4: A code generated by $P(X)=(1+X)P_1(X)$ detects all single, double, and triple errors if the length n of the code is no greater than the exponent e to which $P_1(X)$ belongs.

Proof: The single and triple errors are detected by the presence of the factor $1+X$, as is shown by Theorem 2, and double errors are detected because $P_1(X)$ belongs to the exponent $e\geqq n$, exactly as in Theorem 3. Q.E.D.

Codes of maximum length result if $P_1(X)$ is a primitive polynomial, and these codes are equivalent to Hamming single-error correcting, double-error detecting codes.[1,2,15]

Detection of a Burst-Error

A burst-error of length b will be defined as any pattern of errors for which the number of symbols between the first and last errors, including these errors, is b.

Example:

$$\text{The } E(X) = X^3 + X^6 + X^7$$
$$= 0\ 0\ 0\ 1\ 0\ 0\ 1\ 1\ 0\ 0\ 0\ 0\ 0\ 0\ 0$$

of the previous example is a burst of length 5.

Theorem 5: Any cyclic code generated by a polynomial of degree $n-k$ detects any burst-error of length $n-k$ or less.

Proof: Clearly, any burst-error polynomial can be factored into the form $E(X)=X^iE_1(X)$ where $E_1(X)$ is of degree $b-1$. This burst can be detected if $P(X)$ does not evenly divide $E(X)$. Since $P(X)$ is assumed not to have X as a factor, it could divide $E(X)$ only if it could divide $E_1(X)$. But if $b\leqq n-k$, $P(X)$ is of higher degree than $E_1(X)$ and, therefore, certainly could not divide $E_1(X)$. Q.E.D.

A high percentage of longer bursts are detected as well.

Theorem 6: The fraction of bursts of length $b>n-k$ that are undetected is

$$2^{-(n-k)} \text{ if } b > n-k+1, \quad 2^{-(n-k-1)} \text{ if } b = n-k+1.$$

Proof: The error pattern is $E(X)=X^iE_1(X)$ where $E_1(X)$ has degree $b-1$. Since $E_1(X)$ has terms X^0 and X^{b-1}, there are $b-2$ terms X^j, where $0<j<b-1$, that can have either zero or one coefficients, and so there are 2^{b-2} distinct polynomials $E_1(X)$.

The error is undetected if and only if $E_1(X)$ has $P(X)$ as a factor.

$$E_1(X) = P(X)Q(X).$$

Since $P(X)$ has degree $n-k$, $Q(X)$ must have degree $b-1-(n-k)$. If $b-1=n-k$, then $Q(X)=1$, and there is only one $E_1(X)$ which results in one undetected error, namely $E_1(X)=P(X)$. The ratio of the number of undetected bursts to the total number of bursts is, therefore, $1/2^{b-2}=2^{-(n-k-1)}$ for this case. If $b-1>n-k$, $Q(X)$ has terms X^0 and $X^{b-1-(n-k)}$ and has $b-2-(n-k)$ arbitrary coefficients. There are, therefore, $2^{b-2-(n-k)}$ choices of $Q(X)$ which give undetectable error patterns. The ratio for this case is $2^{b-2-(n-k)}/2^{b-2}=2^{-(n-k)}$. Q.E.D.

Detection of Two Bursts of Errors (Abramson and Fire Codes)

Theorem 7: The cyclic code generated by $P(X)=(1+X)P_1(X)$ detects any combination of two burst-errors of length two or less if the length of the code, n, is no greater than e, the exponent to which $P_1(X)$ belongs.

Proof: There are four types of error patterns.

1) $E(X) = X^i + X^j$
2) $E(X) = (X^i + X^{i+1}) + X^j$
3) $E(X) = X^i + (X^j + X^{j+1})$
4) $E(X) = (X^i + X^{i+1}) + (X^j + X^{j+1})$

2) and 3) have odd numbers of errors and so they are detected by the $1+X$ factor in $P(X)$. For 4), $E(X)=(1+X)(X^i+X^j)$. The $1+X$ factor is cancelled by the $1+X$ factor in $P(X)$ so we will require for both 1) and 4) that X^i+X^j is not evenly divisible by $P_1(X)$. X^i+X^j is not evenly divisible by $P_1(X)$ as is shown in the proof of Theorem 3. Q.E.D.

These codes are equivalent to the Abramson codes, which correct single and double adjacent errors.[2,3] They are also the same as the Hamming single-error correcting, double-error detecting codes of Theorem 6.

Theorem 8: The cyclic code generated by

$$P(X) = (X^c + 1)P_1(X)$$

will detect any combination of two bursts

[16] A. A. Albert, "Fundamental Concepts of Higher Algebra," University of Chicago Press, Chicago, Ill.; 1956. This book contains a table of irreducible polynomials giving the exponent e to which they belong (see p. 161).

[17] N. M. Abramson, "A note on single error correcting binary codes," IRE Trans. on Information Theory, vol. IT-6, pp. 502–503; September, 1960.

$$E(X) = X^{i}E_1(X) + X^{j}E_2(X),$$

provided $c+1$ is equal to or greater than the sum of the lengths of the bursts, $P_1(X)$ is irreducible and of degree at least as great as the length of the shorter burst, and provided the length of the code is no greater than the least common multiple of c and the exponent e to which $P_1(X)$ belongs.

The proof, which is elementary but rather long, is given in Appendix IV. These are Fire codes.[4,12]

Other Cyclic Codes

There are several important cyclic codes which have not been discussed. Burst-error correcting codes have been treated also by Melas,[5] Meggitt,[11] and Reiger.[6] Codes for correcting independent random errors have been discovered by Melas.[10] Prange,[1] and Bose and Chaudhuri.[9,12,18] Any of these codes can also be used for error detection. The Bose-Chaudhuri codes are particularly important. For any choice of m and t there exists a Bose-Chaudhuri code of length 2^m-1 which is capable of correcting any combination of t errors (or alternatively, detecting any combination of $2t$ errors) and which requires a generator polynomial of degree no greater than mt. The description of the structure of these codes and the methods for choosing the polynomials is beyond the scope of this paper.

Implementation

Thus far, an algebraic method has been given for encoding and decoding to detect various types of errors. Briefly, to encode a message, $G(X)$, $n-k$ zeros are annexed (*i.e.*, the multiplication $X^{n-k}G(X)$ is performed) and then $X^{n-k}G(X)$ is divided by a polynomial $P(X)$ of degree $n-k$. The remainder is then subtracted from $X^{n-k}G(X)$. (It replaces the $n-k$ zeroes.) This encoded message is divisible by $P(X)$, but we have shown that if $P(X)$ is properly chosen, the message will not be evenly divisible if it contains detectable errors. The only nontrivial manipulation to be performed for both encoding and error detection is division by a fixed polynomial, $P(X)$.

The following is an example of division under addition modulo two:

$$\begin{array}{r} 1X^3+1X^2+0X+1 \\ 1X^2+0X+1\overline{)\,1X^5+1X^4+1X^3+0X^2+1X+0} \\ \underline{1X^5+0X^4+1X^3} \\ 1X^4+0X^3+0X^2+1X+0 \\ \underline{1X^4+0X^3+1X^2} \\ 0X^3+1X^2+1X+0 \\ \underline{1X^2+0X+1} \\ 1X+1 \end{array}.$$

We now repeat this division employing only the coefficients of the polynomials:

$$\begin{array}{r} 1\,1\,0\,1 \\ 1\,0\,1\overline{)\,1\,1\,1\,0\,1\,0} \\ \underline{1\,0\,1} \\ 1\,0\,0\,1\,0 \\ \underline{1\,0\,1} \\ 0\,1\,1\,0 \\ \underline{1\,0\,1} \\ 1\,1 \end{array}.$$

It can be seen that modulo two arithmetic has simplified the division considerably. Furthermore, we do not require the quotient, so the division to find the remainder can be described as follows:

1) Align the coefficient of the highest degree term of the divisor and the coefficient of the highest degree term of the dividend and subtract (the same as addition).
2) Align the coefficient of the highest degree term of the divisor and the coefficient of the highest degree term of the difference and subtract again.
3) Repeat the process until the difference has lower degree than the divisor. The difference is the remainder.

The hardware to implement this algorithm is a shift register and a collection of modulo two adders. (A modulo two adder is equivalent to the logical operation EXCLUSIVE OR). The number of shift register positions is equal to the degree of the divisor, $P(X)$, and the dividend is shifted through high order first and left to right. As the first one (the coefficient of the high-order term of the dividend) shifts off the end we subtract the divisor by the following procedure:

1) In the subtraction the high-order terms of the divisor and the dividend always cancel. As the high-order term of the dividend is shifted off the end of the register, this part of the subtraction is done automatically.
2) Modulo two adders are placed so that when a *one* shifts off the end of the register, the divisor (except the high-order term which has been taken care of) is subtracted from the contents of the register. The register then contains a difference that is shifted until another *one* comes off the end and then the process is repeated. This continues until the entire dividend is shifted into the register.

Fig. 1 gives a register that performs a division by $1+X^2+X^4+X^5$. Note that if alignment of divisor and dividend is considered to be accomplished when the high-order term of the dividend shifts off the end, then the divisor is automatically subtracted.

[18] W. W. Peterson, "Encoding and error-correction procedures for the Bose-Chaudhuri codes," IRE Trans. on Information Theory, vol. IT-6, pp. 459–470; September, 1960.

The shift register shown in Fig. 1 has, if used for encoding, one drawback that can be overcome by a slight modification. Recall that when encoding a message polynomial, $G(X)$, we calculate the remainder of the division of $X^{n-k}G(X)$ by $P(X)$. The straightforward procedure is to shift the message followed by $n-k$ zeroes into the register. When the last *zero* is in the register we obtain the remainder. Because this remainder replaces the $n-k$ zeros to form the encoded message, it is necessary to delay the message $n-k$ shift times so that the remainder can be gated in from the encoder register at the proper time.

An example of this method of encoding is given in Fig. 2. Initially, the gate G_1 is open and the gate G_2 is shorted, allowing the remainder on dividing $X^{n-k}G(X)$ to be calculated. After the message plus $n-k$ *zeros* is shifted in, G_1 is shorted and G_2 is opened. This allows the remainder which is now in the register to replace the $n-k$ zeros in the output. Error detection with this circuit requires that gate G_1 be open and gate G_2 be shorted. After $H(X)$ has been shifted in, the register contains the remainder. If this is nonzero, an error has occurred.

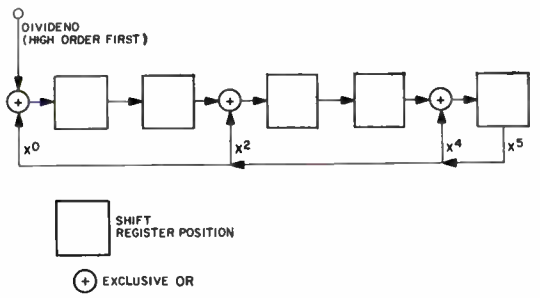

Fig. 1—A shift register for dividing by $1+X^2+X^4+X^5$.

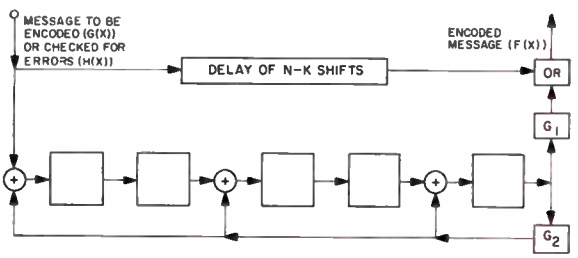

Fig. 2—One method of encoding on detecting errors. (In this example, $P(X)=1+X^2+X^4+X^5$.)

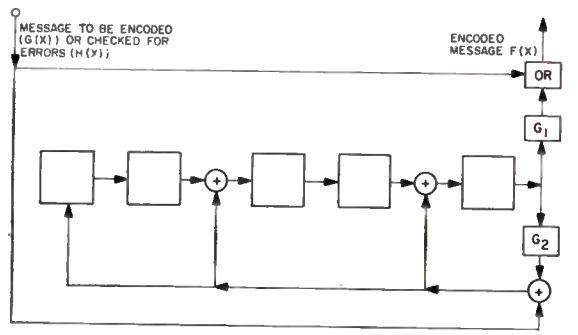

Fig. 3—A more efficient circuit for encoding and error detection. (In this example, $P(X)=1+X^2+X^4+X^5$.)

The delay of $n-k$ shifts can be avoided if Fig. 2 is modified to give the circuit of Fig. 3. In Fig. 3, instead of shifting the polynomial into the low-order end of the register, it is treated as if it were shifting out of the high-order end. This is equivalent to advancing every term in the polynomial by $n-k$ positions, or multiplying by X^{n-k}. Now in encoding, as soon as $G(X)$ has been completely shifted into the register, the register contains the remainder on dividing $X^{n-k}G(X)$ by $P(X)$. Then gate G_1 is shorted, gate G_2 is opened, and the remainder follows the undelayed $G(X)$ out of the encoder to form $F(X)$.

To minimize hardware, it is desirable to use the same register for both encoding and error detection, but if the circuit of Fig. 3 is used for error detection we will get the remainder on dividing $X^{n-k}H(X)$ by $P(X)$ instead of the remainder on dividing $H(X)$ by $P(X)$. It turns out that this makes no difference, for if $H(X)$ is evenly divisible by $P(X)$ then obviously $H(X)X^{n-k}$ is evenly divisible, and if $H(X)$ is not evenly divisible by $P(X)$ then $H(X)X^{n-k}$ will not be evenly divisible either, provided the divisor $P(X)$ does not have a factor X. Any useful $P(X)$ will satisfy this restriction. The circuit of Fig. 3 can, then, be used for both encoding and error detection.

Error correction is by its nature a much more difficult task than error detection. It can be shown that each different correctable error pattern must give a different remainder after division by $P(X)$. Therefore, error correction can be done as follows:

1) Divide the received message $H(X)=F(X)+E(X)$ by $P(X)$ to obtain the remainder.
2) Obtain the $E(X)$ corresponding to the remainder from a table or by some calculation.
3) Subtract $E(X)$ from $H(X)$ to obtain the correct transmitted message $F(X)$.

Both the encoding and step 1 of the decoding are the same for error correction as for error detection. The error-correction equipment is more complex in that it requires equipment for the table look-up or computation of step 2, and it requires that the entire received message $H(X)$ be stored temporarily while the remainder is being calculated and $E(X)$ is being determined. The calculation required in step 2 can be done simply with a shift register for burst-error or single-error correcting codes, but is quite complex for codes that correct multiple random errors. Details of error-correction procedures are beyond the scope of this paper, but can be found in references.[11,12,17]

Conclusion

A simple presentation of cyclic codes has been given in terms of polynomials. The attractive features of these codes for error detection, both their high efficiency and the ease of implementation, have been emphasized.

Appendix I

Notation

k = number of binary digits in the message before encoding,
n = number of binary digits in the encoded message,
$n-k$ = number of check digits,
b = length of a burst of errors,
$G(X)$ = message polynomial (of degree $k-1$),
$P(X)$ = generator polynomial (of degree $n-k$),
$R(X)$ = remainder on dividing $X^{n-k}G(X)$ by $P(X)$, $R(X)$ is of degree less than $n-k$,
$F(X)$ = encoded message polynomial, $F(X)=X^{n-k}G(X)-R(X)$,
$E(X)$ = error polynomial,
$H(X)$ = received encoded message polynomial, $H(X)=F(X)+E(X)$.

Appendix II

A Short Table of Primitive Polynomials

Primitive Polynomial	e
$1+X$	1
$1+X+X^2$	3
$1+X+X^3$	7
$1+X+X^4$	15
$1+X^2+X^5$	31
$1+X+X^6$	63
$1+X^3+X^7$	127
$1+X^2+X^3+X^4+X^8$	255
$1+X^4+X^9$	511
$1+X^3+X^{10}$	1023
$1+X^2+X^{11}$	2047
$1+X+X^4+X^6+X^{12}$	4095
$1+X+X^3+X^4+X^{13}$	8191
$1+X+X^6+X^{10}+X^{14}$	16383
$1+X^{14}+X^{15}$	32767

Appendix III

Data for Some Representative Codes

Detection Capabilities	k_{max}	$n-k$	$P(X)$	Reference
Any odd number of errors	any value	1	$1+X$	Theorem 2
Two errors, a burst of length 4 or less, 88 per cent of the bursts of length 5, 94 per cent of longer bursts*	11	4	$1+X+X^4$	Theorems 3, 5, 6
Two errors, a burst of 9 or less, 99.6 per cent of the bursts of length 10, 99.8 per cent of longer bursts	502	9	$1+X^4+X^9$	Theorems 3, 5, 6
Two bursts of length 2 or less, any odd number of errors, a burst of 5 or less, 93.8 per cent of the bursts of length 6, 96.9 per cent of longer bursts†	10	5	$(1+X+X^4)(1+X)=1+X^2+X^4+X^5$	Theorems 2, 5, 6, 7
Two bursts of combined length 12 or less, any odd number of errors, a burst of 22 or less, 99.99996 per cent of the bursts of length 23, 99.99998 per cent of longer bursts	22495	22	$(1+X^2+X^{11})(1+X^{11})=1+X^2+X^{13}+X^{22}$	Theorems 2, 5, 6, 8
Any combination of 6 or fewer errors, a burst of length 11 or less, 99.9 per cent of bursts of length 12, 99.95 per cent of longer bursts	12	11	$1+X^2+X^4+X^5+X^6+X^{10}+X^{11}$	Theorems 5, 6, and footnote 1
Any combination of 7 or fewer errors, any odd number of errors, a burst of length 31 or less, all but about 1 in 10^9 of longer bursts	992	31	$(1+X)(1+X^3+X^{10})(1+X+X^2+X^3+X^{10})(1+X^2+X^3+X^8+X^{10})$	Theorems 2, 5, 6, and footnotes 9, 12, 18

* *Note:* $1+X+X^4$ belongs to $e=15$ and $11+4=15$.
† *Note:* This is the code used in all examples.

Appendix IV

Proof of Theorem 8

The error polynomial has the form:

$$E(X) = X^i[E_1(X) + X^{j-i}E_2(X)].$$

$E_1(X)$ has degree b_1-1 and $E_2(X)$ has degree b_2-1.

The generator polynomial $P(X)$ cannot have a factor X so we need only consider the factor of $E(X)$ in brackets. Let $j-i=d$, assume $E'(X)=E_1(X)+X^dE_2(X)$ is divisible by X^c+1, and let $d=cq+r$ with $r<c$.

Then,

$$\begin{aligned} E'(X) &= E_1(X) + X^{cq+r}E_2(X) \\ &= E_1(X) + X^rE_2(X) + [X^rE_2(X)]\cdot[X^{cq}+1]. \quad (1) \end{aligned}$$

Now $X^{cq}+1$ contains a factor X^c+1 for

$$\begin{aligned} X^{cq}+1 = (X^c+1)(&X^{c(q-1)} + X^{c(q-2)} \\ &+ X^{c(q-3)} + \cdots + X^0). \end{aligned}$$

Hence the rightmost term in (1) is divisible by X^c+1. $E'(X)$ was assumed divisible by X^c+1 and so from (1), $E_1(X)+X^rE_2(X)$ must be divisible by X^c+1. Using this result, we can let

$$\begin{aligned} E_1(X) + X^rE_2(X) &= [X^c+1][Q(X)] \\ E_1(X) + X^rE_2(X) &= Q(X) + X^cQ(X). \quad (2) \end{aligned}$$

We will assume that $Q(X)\neq 0$. Let the degree of $Q(X)$ be h. The degree of the right-hand side of (2) is $c+h$ and the degree of the left-hand side is either b_1-1 or $r+b_2-1$. Then, for (2) to be true we must have either $c+h=b_1-1$ or $c+h=r+b_2-1$. Since it was assumed that $c\geqq b_1+b_2-1$ we must have the second relation.

$$c + h = r + b_2 - 1.$$

Again using $c\geqq b_1+b_2-1$ we have

$$b_1 + b_2 - 1 + h \leqq r + b_2 - 1 \quad \text{or} \quad b_1 + h \leqq r.$$

From this, $b_1\leqq r$ or $b_1-1<r$ and as $b_1\neq 0$, $h<r$.

Applying these results to (2), we see that both $E_1(X)$ and $Q(X)$ are of lower degree than any of the terms in $X^rE_2(X)$. It follows then, given the assumption that $Q(X)\neq 0$, that

$$X^rE_2(X) = X^cQ(X). \quad (3)$$

As $E_2(X)$ always contains an X^0 term, the lowest order term in $X^rE_2(X)$ is of degree r. The lowest order term in $X^cQ(X)$ is of degree at least c but $r<c$ so (3) can never be satisfied. Therefore, the only solution of (2) is with $Q(X)=0$ giving $E_1(X)+X^rE_2(X)=0$.

As $E_1(X)$ always contains an X^0 term, $r=0$ and $E_1(X)=E_2(X)$. Substituting in (1) gives

$$E'(X) = E_2(X)[X^{cq}+1].$$

This is the form of the error polynomial if it is evenly divisible by X^c+1. It is sufficient to show that this polynomial is not evenly divisible by $P_1(X)$ to guarantee that $E(X)$ is never evenly divisible by $P(X)=P_1(X)$, $[X^c+1]$. $P_1(X)$ is irreducible, so to divide $E'(X)=E_2(X)[X^{cq}+1]$ it must divide one of the factors. For this special case, $E_1(X)=E_2(X)$ so $b_1=b_2$, and since both bursts have the same length, this is the length of the shorter burst. It was specified that $P_1(X)$ is of degree no less than the length of the shorter burst so it is of higher degree than $E_2(X)$ and cannot divide $E_2(X)$.

It remains to show that $P_1(X)$ does not evenly divide $X^{cq}+1$. Make the substitution $cq=ue+v$ where e is the exponent to which $P_1(X)$ belongs and $v<e$. Now $v\neq 0$ because cq is less than or equal to the length of the message and the length of the message is less than or equal to the least common multiple of c and e. Since cq is a multiple of c, it cannot be a multiple of e.

$$\begin{aligned} X^{cq} + 1 &= X^{ue+v} + 1 \\ X^{cq} + 1 &= X^v + 1 + X^v(X^{ue} + 1). \end{aligned}$$

As was shown previously, $X^{ue}+1$ is divisible by X^e+1. Furthermore, $P_1(X)$, by definition, divides X^e+1; therefore, $P_1(X)$ divides $X^{ue}+1$. However, X^e+1 is the lowest degree polynomial of this form that $P_1(X)$ divides, so $P_1(X)$ does not divide X^v+1. As $v\neq 0$, we have shown that $P_1(X)$ does not divide $X^{cq}+1$, completing the proof.

Statistical Analysis of Logic Circuit Performance in Digital Systems*

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Summary—**A digital system usually contains large numbers of relatively few basic circuit configurations. The over-all performance of such a system is largely limited by the characteristics of these building block circuits. If these characteristics (speed, logical gain, noise margin) are treated on a statistical basis as opposed to a worst case approach, substantial improvements in logical design flexibility may be attained.**

This paper reviews methods for combining statistical distributions of a set of parameters to obtain the distributions of the performance characteristics. Both algebraic and numerical (Monte Carlo) methods are considered. Transistor Resistor Logic circuits are then analyzed in more detail. Resultant distributions of propagation delays and logical gain are obtained as functions of circuit parameter distributions, logical configuration and temperature. Comparisons with worst-case design figures are made to indicate the extent to which statistical techniques improve predicted performance. In addition, some new circuit configurations, proved usable by statistical analysis, are shown to lead to greater economy and reliability.

I. Introduction

TODAY'S digital systems may be considered as a type of hierarchy in which the components are placed into circuit configurations, circuits are assembled into groups of subsystems, and the subsystems are in turn organized into the final system. Even though these groupings are not always clearly defined, the over-all performance of the system is of necessity dependent on the characteristics of its subgroupings all the way down to the smallest component. Variations in these characteristics are inevitable because of the tolerances in basic materials, manufacturing processes, and environmental conditions such as temperature and humidity. Such variations must be considered in the design of a system to assure reliable system performance under all conditions. The simplest method for such consideration is to assume that the worst limits in the variations occur in all the characteristics simultaneously. However, this worst case prediction is pessimistic[1] and may degrade the expected performance to a point where there is a need for certain redundant elements that could actually increase the cost and reduce the reliability of a system beyond the limits that would have been obtained had these variations been treated on a statistical basis.

This paper treats the problem of obtaining the statistical distribution of the response or output of some circuit as a function of the distributions of individual component parameter variations. The approach taken is that of an engineering solution to the problem, rather than a rigorous statistical treatment. The paper is divided into three major parts.

Section II is a brief survey of the methods of analysis for the combination of frequency curves.[2] It includes an algebraic method based on a Taylor series expansion which is suitable for hand calculation, and a numerical method,[3] namely the Monte Carlo approach, which is suitable for machine computation. Examples of the applications of both methods are given.

Section III is concerned with the applications of these methods to transistor resistor logic circuits.[4–6] Speed, noise margin, and logical gain distributions are derived.

Section IV discusses how these results may be used by logic and system designers, and the effect of the statistical analysis on system reliability and cost figures.

II. Methods for the Combination of Frequency Curves

When dealing with parameters that are specified as distributions rather than as discrete values, we are concerned with the probability of a given sample, chosen at random from the distribution, falling within certain imposed limits.

For example, the commonly occurring normal distribution has associated probabilities as shown in Table I. This distribution is completely defined by two numbers—the standard deviation σ, and the mean value. Since the distribution is symmetrical about the mean value, the probability of the sample falling outside of just one of the limits is half the value shown in the table. Other types of distributions are characterized by additional factors such as skewness and flatness. The construction of similar tables for such distributions is, in general, likely to be formidable.

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† Bell Telephone Labs., Inc., Murray Hill, N. J.

‡ International Electric Corp., Paramus, N. J. Formerly with Bell Telephone Labs., Inc., Murray Hill, N. J.

[1] F. E. Oreste, "Circuit Design Techniques for High Reliability," presented at the Sixth Natl. Symp. on Reliability and Quality Control, Washington, D. C.; January 11–13, 1960.

[2] R. I. Wilkinson, "The Combination of Frequency Curves," unpublished notes.

[3] L. Hellerman and M. P. Racite, "Reliability techniques for electronic circuit design," IRE TRANS. ON RELIABILITY AND QUALITY CONTROL, No. RQC-14, pp. 9–16; September, 1958.

[4] W. D. Rowe, "The transistor NOR circuit," 1957 IRE WESCON CONVENTION RECORD, pt. 4, pp. 231–246.

[5] Q. W. Simkins, "Transistor Resistor Logic," presented at the Solid-State Circuits Conference, Philadelphia, Pa.; February 20, 1958.

[6] T. R. Finch, "Transistor resistor logic circuits for digital data systems," *Proc. WJCC*, pp. 17–22; 1958.

TABLE I
NORMAL DISTRIBUTION OF VALUES OF PARAMETER x WITH STANDARD DEVIATION σ

n	Probable Occurrence of $x \geq n\sigma$ or $x \leq -n\sigma$
1.0	0.317
2.0	4.55×10^{-2}
3.0	2.70×10^{-3}
3.5	4.65×10^{-4}
4.0	6.34×10^{-5}
5.0	5.73×10^{-7}
6.0	2.00×10^{-9}

A. *Algebraic Combination of Frequency Curves*

If a given characteristic is a function of a number of parameters

$$y = f(x_1, x_2, \cdots x_n) \tag{1}$$

where the x_i are uncorrelated parameters with distributions that vary from their average values ($\bar{x}_i$), by quantities Δx_i, then y can be expanded into a Taylor series around the mean values of these parameters.

$$y = f(\bar{x}_1, \bar{x}_2, \cdots \bar{x}_n) + f_{x_1}\Delta x_1 + f_{x_2}\Delta x_2 + \cdots + f_{x_n}\Delta x_n \tag{2}$$
$$+ \frac{1}{2!}\left[f_{x_1x_1}\Delta^2 x_1 + f_{x_1x_2}\Delta x_1\Delta x_2 + \cdots + f_{x_nx_n}\Delta^2 x_n\right]$$
$$+ \cdots .$$

For sufficiently small Δx_i or higher derivatives of f, the higher order terms may be neglected, so that

$$y \doteq \bar{y} + \sum_i f_{x_i}\Delta x_i. \tag{3}$$

We can obtain a mean value and standard deviation of the characteristic as shown in (4) and (5), respectively.

$$\bar{y} = f(\bar{x}_1, \bar{x}_2, \cdots \bar{x}_n) \tag{4}$$

$$\sigma_y = \sqrt{f_{x_1}^2\sigma_{x_1}^2 + f_{x_2}^2\sigma_{x_2}^2 + \cdots + f_{x_n}^2\sigma_{x_n}^2}. \tag{5}$$

The partial derivatives in (5) may be thought of as weighting factors which determine the contribution of the variations of each parameter to the resultant standard deviation of y. Eq. (5) may be rewritten in terms of the tolerances of the individual parameters:

$$T_y = \sqrt{f_{x_1}^2T_{x_1}^2 + f_{x_2}^2T_{x_2}^2 + \cdots + f_{x_n}^2T_{x_n}^2} \tag{6}$$

where all the tolerances T_i are known with the same degree of certainty. For example, we might say that only 0.3 per cent of all 10 K, 10 per cent, resistors fall outside the limits 9 K to 11 K.

Two special cases exist in the application of (6). When the function y consists entirely of the algebraic addition of the parameters $x_1, x_2, \cdots, x_n$, the partial derivatives in (6) take on the value 1, permitting us to add directly the squares of the individual tolerances. Similarly, in (5), we may add the variances directly. When the function y is defined entirely as a product of terms, squares of the tolerances may be added directly if we now consider the tolerances to be percentages rather than absolute magnitudes.

The application of (4)–(6) is limited by the approximations that have been made in deriving them. Substantial errors occur when the function y has significant higher-order derivatives in the region of interest, when the variation in the parameters, Δx_n, is large (except if the higher order derivatives are zero), or when the distributions of the parameters are skewed and cannot be described entirely by their mean value and standard deviation. In the latter case, the equations still hold but do not give a complete description of the distributions.

These equations have been applied to the simple voltage divider circuit shown in Fig. 1 with the following results: The tolerance on the output voltage E_0 is ± 11.3 per cent at the 3σ point. From Table I, this implies that approximately three out of every 1000 samples will fall outside of these limits. Calculations of the worst case limits (± 17.6 per cent) indicate that they occur at the $\pm 4.7\sigma$ points. This corresponds to approximately two failures per million samples. In other words, even though the parameters R_1, R_2, E_i have a probability of 0.3 per cent of falling outside their tolerance limits, the output voltage will fall outside its worst-case tolerance limits with a probability of only 0.0002 per cent. Thus, as is true, in general, for worst case calculations involving several parameters, the characteristic calculated has a considerably stricter definition of "tolerance" than that used in characterizing the components.

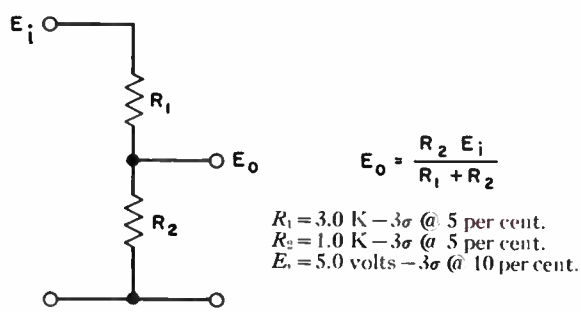


Fig. 1—Voltage divider.

B. *Numerical Techniques for the Combination of Frequency Curves*

As the problems become more complex, numerical techniques frequently become the most useful tool in their solution. In statistical problems, the so-called Monte Carlo technique has been widely used. In this technique, random number generators are used to simulate the distribution of each of the parameters in the problem. The problem is then solved for the desired function a large number of times, each time picking a set of parameters at random from simulated distributions that have been set up for each of the parameters.

These results can then be plotted as a histogram to give a distribution of the desired output characteristic.

The method for generating the simulated distribution of the parameters on a digital computer is shown in Fig. 2. The manufacturer generally specifies the distribution of a parameter by a table such as the one shown in the figure (distribution of current gain in a transistor taken from a typical data sheet). In addition, the manufacturer gives estimates on the expected degradation of the parameters due to aging. From these data an expected distribution of the parameter at end of life can be obtained as shown in line 2 [Beta (EOL)].

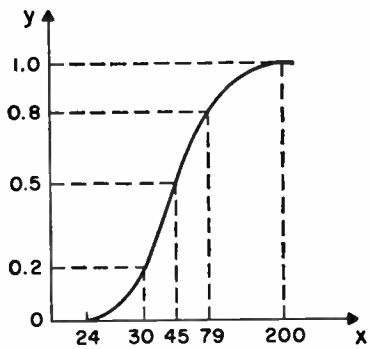


Fig. 2—Generation of arbitrary cumulative distributions.

$$x = a + by + cy^2 + dy^3 + ey^4.$$

Thus the parameter x (Beta in this specific case) is a function of five sets of coordinates, x_1y_1, x_2y_2, $\cdots$, x_5y_5. These five sets of coordinates may then be used to evaluate the five constants in a fourth-order polynomial that can be written to approximate this cumulative distribution.

Manufacturers' Data:	Min	20 Per Cent	50 Per Cent	80 Per Cent	Max
Beta (Initial)	32	39	58	99	200
Beta (EOL)	24	30	45	79	200

Computer subroutines are available which will generate uniformly distributed pseudo-random numbers between the limits of 0 and 1 with a periodicity of $10^{9.9}$. By using such a set of random numbers, y, to evaluate the polynomial

$$x = a + by + cy^2 + dy^3 + ey^4, \qquad (7)$$

the desired characteristic x will then have the distribution specified by the manufacturer. For example, in Fig. 2, the manufacturer says that at end of life 30 per cent of all units will have a Beta between 30 and 45. Thirty per cent of the uniform numbers generated will lie between the values of 0.2 and 0.5. Therefore, 30 per cent of the values of x that are computed will lie between the values of 30 and 45. By this technique, then, it is possible to set up as many polynomials as there are types of parameters in the problem under investigation, so that a set of universes with essentially infinite populations is available from which parameters for the successive solutions to the problem can be chosen.

The accuracy of the sampling process is limited by the number of trials that are performed.[7] Table II shows the limitations imposed on the accuracy by the sample size. Three trends are evident:

1) To increase the degree of certainty of the result, the number of trials must be increased.
2) To increase the accuracy of the result, the number of trials must be increased.
3) As we consider a smaller and smaller section of the tail of the distribution, the number of trials must be increased in order to maintain the same degree of certainty and accuracy.

TABLE II
SAMPLING ERRORS

Degree of Certainty (Per Cent)	To An Accuracy Of (Per Cent)	Number of Trials		
		For Median	For 10th Percentile	For 5th Percentile
90	2	6700		
	10	251	2355	
	20			1750
	50		80	
95	2	9551		
	10		3400	
	20	90		2250
	50		120	
99	10	651	5900	
	20			3650
	50		220	

For example, with 251 or more trials we can be 90 per cent sure that the median of our sample is within 10 per cent of the true median of the entire population, whereas, to be 90 per cent sure that between 9 and 11 per cent of all samples will fall below the measured tenth percentile point, 2355 trials must be performed. Since the extreme limits of the distribution generally are of primary concern to statistical circuit analysis, some sort of extrapolation technique must be developed in order that the number of trials required for reasonable accuracy does not become excessive.

As an example of the application of the Monte Carlo technique, consider the voltage divider problem of Fig. 1. Fig. 3 shows the cumulative distribution of input voltage based on 1000 samples of the polynomial approximation defined at the median, $\pm 1\sigma$ and $\pm 3\sigma$ points, compared to the true normal distribution assumed in the algebraic solution. The latter is a straight line on the probability scale graph shown. As expected, the sample of 1000 trials approximates the true median most closely, the $\pm 1\sigma$ points with somewhat less ac-

[7] M. Sobel and M. J. Huyett, "Nonparametric definition of the representativeness of a sample—with tables," *Bell Sys. Tech. J.*, vol. 37, pp. 135–161; January, 1958.

curacy, and the $\pm 3\sigma$ point with relatively poor accuracy. The sample, of course, does not follow the normal distribution in between these points, but rather the shape of the polynomial.

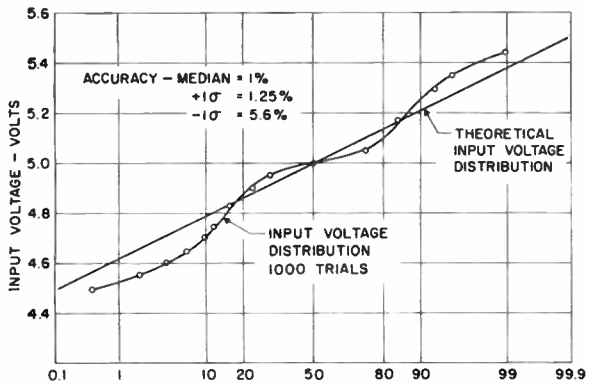


Fig. 3—Voltage divider—input voltage distribution.

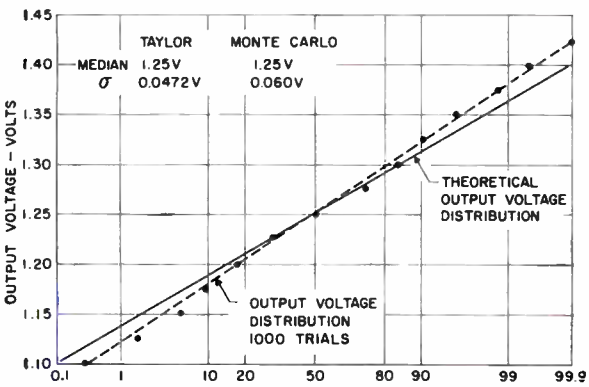


Fig. 4—Voltage divider—output voltage distribution.

Using this same technique to obtain distributions for R_1 and R_2, a cumulative distribution for the resultant E_0 based on 1000 trials is shown in Fig. 4. For comparison, the distribution predicted by the Taylor series analysis is also plotted on the same set of axes. The numerical technique does not give an exactly normal distribution, but one which may be approximated by a normal distribution (the dashed line). A comparison of the two results shows the same mean value for the output voltage, and a larger standard deviation for the numerical technique, due primarily to the conservative approximation of the near normal distribution. This corresponds to a probability of exceeding worst case limits of 0.01 per cent, compared to the 0.0002 per cent for the algebraic calculations, where, as before, the input parameters exceed their tolerance limits 0.3 per cent of the time.

III. Statistical Analysis of Transistor Resistor Logic (TRL) Circuits

In digital systems employing the building block philosophy, the characteristics of the individual gating elements constitute one of the major limitations on the over-all performance of the system. For each element, some specification must be set for its logical gain capabilities, propagation delay, noise margin, and reliability. An improvement in any one or more of these specifications can frequently be used to advantage in improving system reliability, reducing cost, or otherwise improving performance.

Because of the many variables involved in each TRL gating element, it is a particularly good candidate for a thorough statistical analysis of its performance characteristics. The performance characteristics of the TRL gate (Fig. 5) are substantially affected by its surrounding environment and, of course, by its own circuit parameters. Important variables include the type of driving circuits (TRL gates with different fan-outs, high fan-out drivers and other types of driving sources), the fan-in and fan-out of the stage under consideration, and the loads on the gate. The logical gain is defined as the sum of fan-out and fan-in (the highest fan-out of any driving stage plus the fan-in allowable at the driven stage). Propagation delay is defined as the time it takes for an input to affect the output of a stage (between the 50 per cent point of the input waveform and the 50 per cent point of the output waveform). The noise margin is defined as the maximum allowable input which will cause no change at the output. Reliability is based on the failure rates of the components[8] that compose the individual gating circuits.

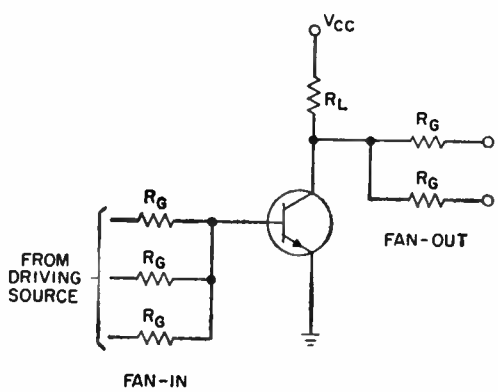


Fig. 5—Transistor resistor logic gate. $V_{cc}=12$ volts, $R_L=2.37$ K, $R_G=4.64$ K.

DC and transient-response analysis of TRL circuits has been covered in the literature.[9,10] The type of statistical analysis proposed in this paper requires mathematical models, the inaccuracies of which are much less than the spread of the expected distributions, and which are based on component parameters normally specified by the manufacturer. In view of this require-

[8] C. A. Krohn, "Reliability analysis techniques," Proc. IRE, vol. 48, pp. 179–192; February, 1960.

[9] M. W. Marcovitz and E. Seif, "Analytical design of resistor coupled transistor logical circuits," IRE Trans. on Electronic Computers, vol. EC-7, pp. 109–119; June, 1958.

[10] W. J. Dunnet, E. P. Auger, and A. C. Scott, "Analysis of TRL circuit propagation delay," *Proc. EJCC*, pp. 99–108; 1958.

ment, the propagation delay model that has been used[11] is based on a ramp input applied to a transistor equivalent circuit comprising the usual dc and small signal parameters. The resultant equations contain many parameters and are rather complicated functions which, under certain conditions, become transcendental and require iterative methods of solution. Therefore, because of the nature of the equations and the many types of parameter distributions that may occur, the numerical technique is clearly the most effective method for this analysis.

A. A Monte Carlo Computer Program for TRL

The block diagram of a computer program which calculates distributions of the desired characteristics is shown in Fig. 6. A group of input cards sets up the problem in terms of:

1) Logical configuration—type of input drive, fan-out, fan-in;
2) Logical state—number of active inputs driving the stage on and off;
3) Circuit parameters—distributions for all transistor parameters, resistors and voltages;
4) Miscellaneous constants;
5) Distribution mode—number of trials to be run, type of analysis (dc only, or dc and transient), definition of intervals for printing out histogram of desired characteristic.

Polynomials are computed for each different type of parameter. The program then examines the logical configuration and determines the total number of parameters N, contributing to the circuit response. This number will be more than the number of defined polynomials, since some types of parameters are used more than once. For example, the same nominal resistance is always calculated by the same polynomial, but may appear in several places in the circuit. This polynomial will thus be evaluated several times using different random arguments. The program now goes into a loop and performs K trials. N uniformly distributed numbers are generated and are used to evaluate the polynomials to obtain the N necessary parameters. Using this set of parameters, a dc analysis is performed and the result (noise margin, and overdrive ratio—$\beta I_b/I_c$) is stored. Also, a transient response analysis may be performed, and the resulting rise times, storage times, fall times, turn-on times, and turn-off times are stored in their respective distribution intervals. After this process has been repeated K times, the resultant distributions are printed out.

Typically, a circuit may contain 25 different types of parameters, a total of $N=50$ parameters, and with 1000 trials, have a running time on an IBM 704 computer of

[11] E. Nussbaum, "Analysis of propagation delay in TRL gates assuming ramp inputs," unpublished.

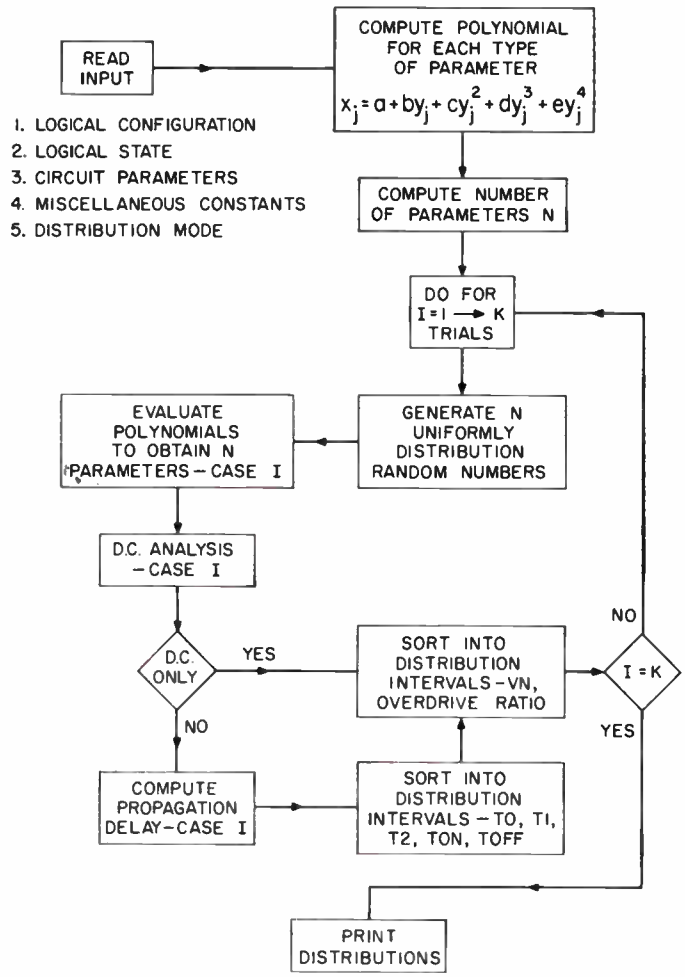


Fig. 6—Flow diagram—Monte Carlo analysis of TRL.

Case A—dc analysis only—0.08 hour.
Case B—dc and transient analysis—0.12 hour to 0.16 hour, depending on the degree to which transcendental equations are involved in the solution.

B. Results of Statistical Analysis

Distributions of turn-on and turn-off times are shown in Fig. 7, for the logical configuration indicated, in the TRL circuit of Fig. 5 using a double diffused *n-p-n* silicon switching transistor. A comparison is made between results obtained when using parameter distributions as specified by the manufacturer, and parameter distributions assumed to be uniform between the extreme limits specified by the manufacturer. For both turn-on and turn-off times, the two assumptions give essentially the same median and, as might be expected, indicate that the use of manufacturer's actual distribution results in a smaller standard deviation of the characteristics.

Fig. 8, which is a plot of the distribution of the overdrive ratio, points up two new characteristics. 1) The median derived from the actual distribution is consid-

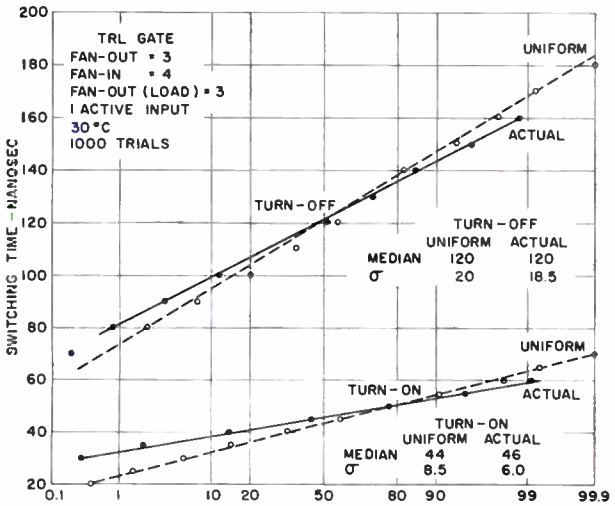


Fig. 7—TRL—propagation delay—turn-on and turn-off.

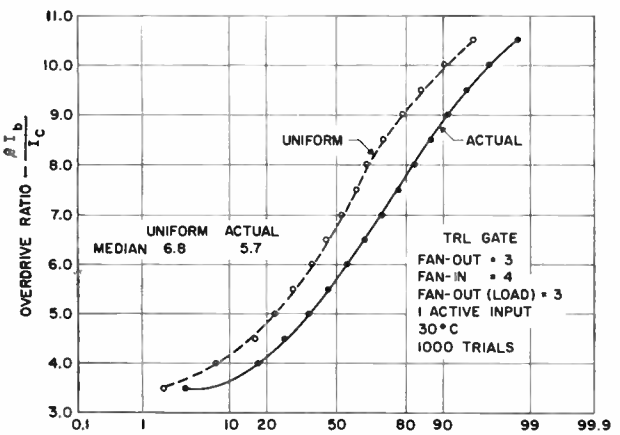


Fig. 8—TRL—overdrive ratio—$\beta I_b/I_c$.

erably lower (more pessimistic) than that derived from the uniform distribution. Thus, although at first it might appear that a uniform distribution is the most pessimistic assumption that one need make statistically, it may happen that because of serious skewing of some important parameters (in this case β), actual distributions may give substantially different results, even for the median. 2) The distributions are very definitely not normal, and no approximation of the standard deviation can be made from this curve.

Fortunately, however, the reciprocal of overdrive ratio ($I_c/\beta I_b$—Fig. 9) has an approximately normal distribution over the important lower half of its range. The median value is 0.173, and for this half of the distribution the standard deviation is 0.082. Failure occurs when the reciprocal of overdrive ratio is greater than one, so that the distribution indicates that the point of failure is approximately 10σ away from the median.

By using actual manufacturers' parameter distributions, and the reciprocal technique where necessary, families of distribution curves for propagation delay and overdrive ratio have been obtained for the TRL

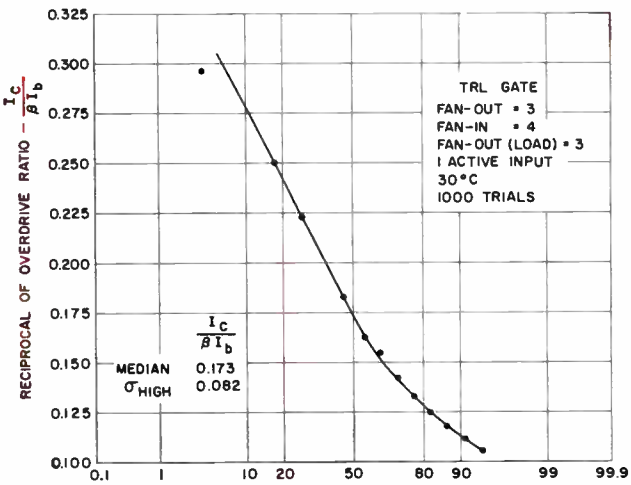


Fig. 9—TRL—reciprocal of overdrive ratio—I_c/BI_b.

gate of Fig. 5 by the Monte Carlo technique just described (Figs. 10–12). Curves for different temperatures are obtained by modifying input parameter distributions by use of appropriate temperature coefficients. Similar curves can be obtained for all the different logical configurations (fan-in and fan-out) and logical states (number of active inputs). Variations in the median and standard deviations are tabulated in the figures. Particularly significant is the fact that a calculation of the worst-case delay indicates that it falls at the 8σ point of the distribution (Fig. 10).

The computer program is also capable of determining correlation between turn-on and turn-off times of the same stage. The importance of this consideration will be discussed in Section IV. The scatter diagram of Fig. 13 indicates that no correlation exists for the turn-on and turn-off times of the circuit configuration referred to in Fig. 10.

IV. Application of Results

In order to determine reasonable bounds on the distribution of some performance characteristic, it is necessary to determine the inherent reliability of the circuit, based upon the failure rate of the components of which it is composed. Fig. 14(a) shows the well-known curve of the failure rate of electronic equipment over a period of time.[8] It assumes that, except for the early burn-in period and eventual wear-out region, equipment functions with a relatively constant rate of failure during its operating life. Typical failure rates for components of which such equipment is composed are shown. A transistor rating of 200 fits (failures in 10^9 hours) implies that a transistor will fail 200 times in 10^9 hours if it is replaced after each failure by a new transistor in that same location, or alternatively, that over a period of 10^5 hours (approximately 10 or 11 years) in a system composed of 100 transistors, probably two will fail. Similarly, probably one out of 1000 resistors would fail in a ten-year test. These failures are due to catastrophic fail-

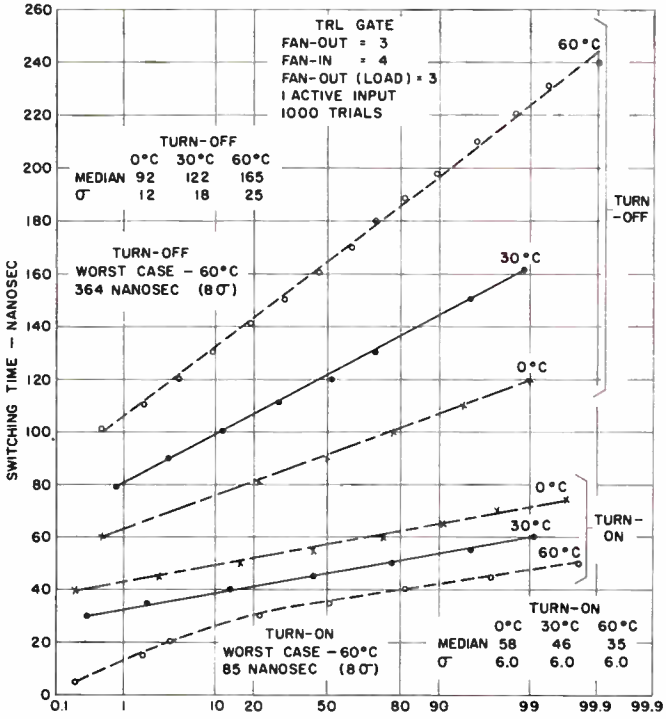


Fig. 10—TRL—propagation delay distributions vs temperature.

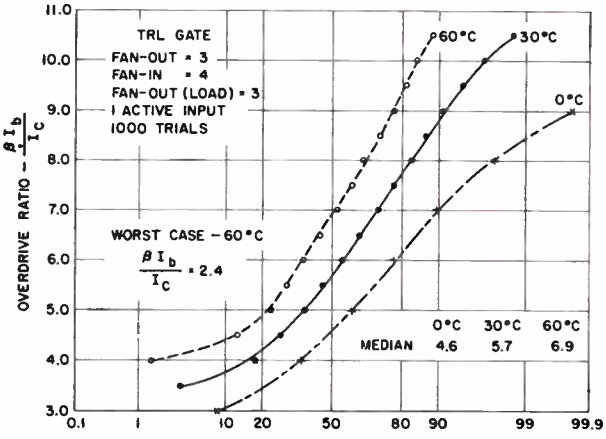


Fig. 11—TRL—overdrive ratio distributions vs temperature.

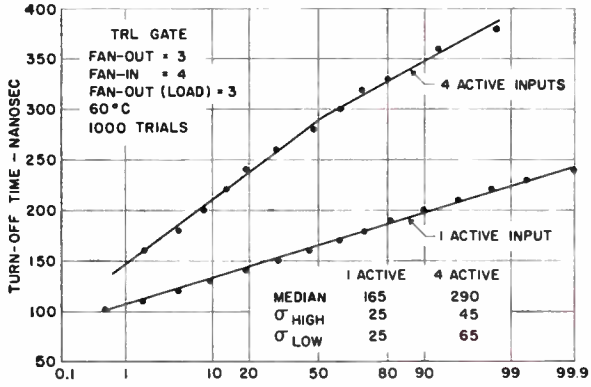


Fig. 12—TRL—propagation delay distributions vs number of active inputs.

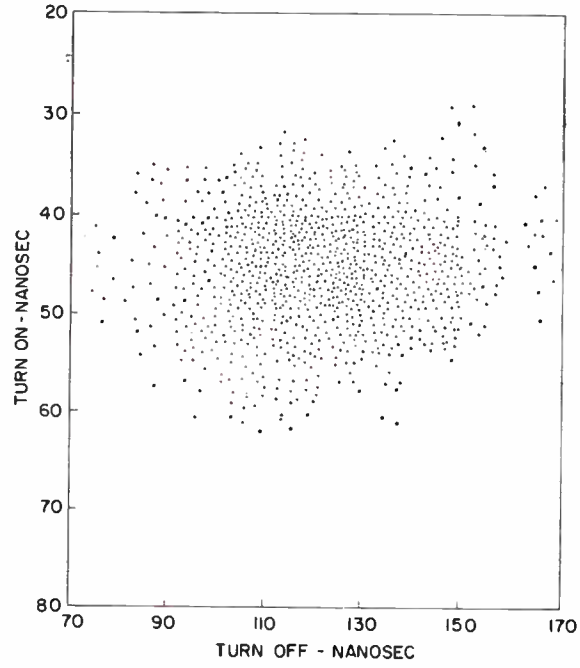
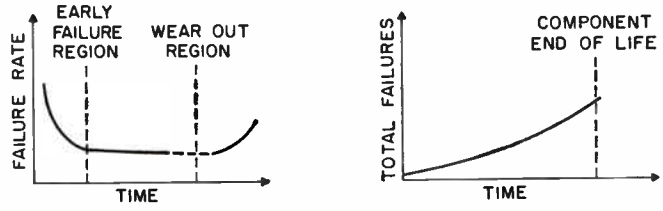


Fig. 13—TRL—turn-on and turn-off correlation.



Failure Rate of Electronic Equipment (Based on Component Failure Rate) Typical Figures—

	Failures /10^9 hours	Failures /10^5 hours
Transistor	200	2×10^{-2}
Resistor	10	1×10^{-3}

(a)

Failures Due to Aging of Parameters (Based on Statistical Circuit Analysis) Typical Figures—
End of Life = 10^5 Hours
$3\sigma = 3\times10^{-3}$
$4\sigma = 7\times10^{-6}$
$5\sigma = 6\times10^{-7}$

(b)

Fig. 14—Failure rates. (a) Component failures. (b) Aging failures.

ures in the components and occasional extremely wide swings out of tolerance. Present-day data on these failure mechanisms are still quite crude, although very recent work in this field shows promise.[12]

In deriving the distributions of the various characteristics in Section III, the parameter distributions used were those that might be expected at the end of life of the component. Compared to the initial parameter distributions, end-of-life parameter distributions generally have larger deviations and occasionally have shifts in their mean value. If the parameter distributions were time stationary, circuits could be designed to have some specified number of failures upon first use,

[12] B. T. Howard and G. A. Dodson, "High Stress Aging to Failure of Semiconductor Devices," to be presented at the Seventh Natl. Symp. on Reliability and Quality Control, Philadelphia, Pa.; January, 1961.

and after these faulty circuits had been weeded out, the rest would be expected to have no more failures. However, it is because of this aging in the parameters that, for any given specification limit set on the distribution of a characteristic, more and more samples will exceed the limit as the distribution spreads out with time [Fig. 14(b)]. An end-of-life time period of the order of 10^5 hours is generally about the minimum to be expected from solid-state components used in electronic computers. This would then indicate that, if a circuit is designed to have its specification limits at the 3σ point of its EOL distribution, over a period of 10^5 hours, three out of 1000 such circuits are likely to exceed these limits (see Table I). Estimates of end-of-life distributions, and indeed time to end-of-life, are generally based on accelerated aging tests, and are therefore of necessity only approximate.

Using this concept of reliability, three examples of the application of the distributions derived in Section III are given below.

Example A—Propagation Delay

Five TRL stages are placed in cascade. Each has a fan-in of 4, a fan-out of 3, and only one input per stage changes at any given time. If the first stage is turned off by the output of some preceding TRL stage, what is the delay until the last stage turns off?

Since the cascaded stages turn alternately on and off, the total delay through the five stages is given by

$$T_D = 3T_{OFF} + 2T_{ON}. \tag{8}$$

This is, then, a linear combination of five distributions, and the special cases of (4) and (5) (the additive case) may be applied.

$$\overline{T}_D = 3\overline{T}_{OFF} + 2\overline{T}_{ON} \tag{9}$$

$$\sigma_D = \sqrt{3\sigma_{OFF}^2 + 2\sigma_{ON}^2}. \tag{10}$$

Using the data from Fig. 10, the mean delay times and their associated standard deviations are predicted (see Table III).

TABLE III

Temperature	0°C	30°C	60°C
$\overline{T}_D$	392	458	565
σ_D	22.5	32.3	44.1
$3\sigma(1.4\times10^{-3}$ fail/10^5 hours$)-T_D$	460	555	697
$4\sigma(3.2\times10^{-5}$ fail/10^5 hours$)-T_D$	482	587	741
$5\sigma(2.0\times10^{-7}$ fail/10^5 hours$)-T_D$	505	620	786

All times in nanoseconds.
Worst case T_D at 60°C = 1260 nanoseconds.

This table indicates that after 10 years, only 14 out of 10,000 such circuits would have total delays exceeding 697 nanoseconds at 60°C (compared to a worst case calculation figure of 1260 nanoseconds).

The typical component failure rates given in Fig. 14(a) show that during the same ten-year period, this five-stage circuit will have 1250 failures in 10,000 such configurations caused by component failures alone.

It is therefore evident that by setting a specification limit of 700 nanoseconds on this propagation delay through the five stages, instead of the 1.26 μsec predicted by a worst-case analysis, no measurable change has occurred in the reliability of the circuit, and the usable performance has been improved by almost 50 per cent.

Example B—Pulse Shrinkage

A negative going clock pulse is applied to a gate, and, under the control of some logic circuits, eventually sets a flip-flop. The minimum pulse width allowable in setting the flip-flop is $W_0 = 0.3$ μsec. The clock pulse has a width of $W_c = 1.0$ μsec. Through how many cascaded stages of logic n may the clock pulse pass? Each logic stage is assumed to have the characteristic shown in Fig. 10.

The width of the output pulse is

$$W_0 = W_c - [(T_{OFF_1} - T_{ON_1}) + (T_{ON_2} - T_{OFF_2}) \cdots + (T_{OFF_n} - T_{ON_n})]. \tag{11}$$

On a worst-case basis, two solutions are obtained for the maximum usable number of stages n:

$$n \leq \frac{[2(W_c - W_0) + (T_{ONmax} + T_{ONmin}) - (T_{OFFmax} + T_{OFFmin})]}{T_{ONmax} - T_{ONmin} + T_{OFFmax} - T_{OFFmin}} \quad (n = \text{odd integer}) \tag{12}$$

$$n \leq \frac{2(W_c - W_0)}{T_{ONmax} - T_{ONmin} + T_{OFFmax} - T_{OFFmin}} \quad (n = \text{even integer}). \tag{13}$$

Since the worst-case maximum and minimum points fall at the 8σ points of the distribution of Fig. 10, the value of n for 30°C is 3.2, so that, at most, 3 stages may be cascaded.

On a statistical basis, considering the $m\sigma$ point on the distribution, it follows that

$$n \leq \left(\frac{W_c - W_0}{m(\sigma_{ON} + \sigma_{OFF})}\right)^2 \quad (n = \text{ even integer}) \tag{14}$$

and

$$n \leq \left(\frac{W_c - W_0 + \overline{T_{ON}} - \overline{T_{OFF}}}{m(\sigma_{ON} + \sigma_{OFF})}\right)^2 \quad (n = \text{ odd integer} \gg 1), \tag{15}$$

where T_{ON} and T_{OFF} are uncorrelated. This condition has been satisfied as shown in Fig. 13.

For the 5σ point of pulse shrinkage, which has been shown to give reasonable reliability, the value of n for

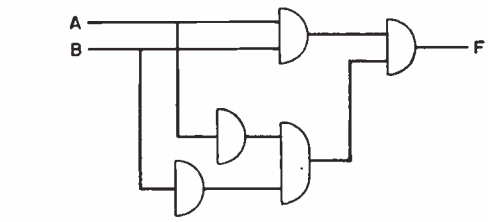
30°C is 26.7, so that up to 25 stages may be cascaded. This indicates about an 8:1 improvement in predicted performance, as regards the number of stages.

Example C—New Circuits

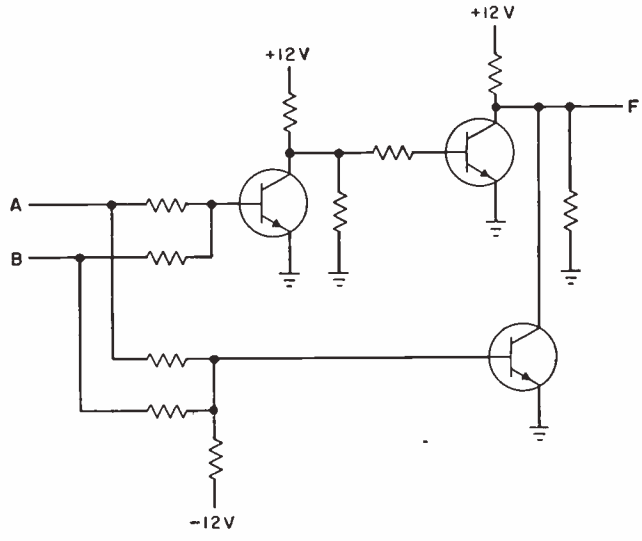
Statistical analysis may lead simultaneously to improved reliability and reduced cost through the introduction of apparently marginal circuits (Fig. 15).

A comparator circuit is needed that is to produce a ground on match, that is, the output F is to be 0 when inputs A and B are either both 0 or both 1. Using the standard TRL building block approach (Fig. 5), in which all gating elements meet worst-case design requirements, the circuit of Fig. 15(a) is obtained. Based on previously used component reliability figures, the circuit has a failure rate of 0.12 per cent per 1000 hours of operation and uses 5 transistors and 18 resistors. In Fig. 15(b), three TRL gates are replaced by a two-input TRL AND gate, that is, an output appears only when both inputs are activated. When analyzed statistically, this gate, while not meeting worst-case design margins, will have a failure rate of only 0.00003 per cent per 1000 hours of operation, based on a 150-mv noise margin requirement. The circuit failure rate for this "marginal" circuit, based on component reliability figures, is 0.069 per cent for 1000 hours of operation and the cost is 3 transistors and 9 resistors. The statistical analysis has thus achieved an improvement in reliability of almost 50 per cent and a similar reduction in cost.

In a similar manner, statistical analysis may be used to increase fan-in and fan-out specifications for the circuit and to design majority gates which find numerous uses in logical design.[13]



(a)



(b)

Fig. 15—TRL comparator—ground on match. $F=[A'B'+AB]'$.

V. Conclusion

Statistical analysis of circuit performance allows improvement of the specifications that are set up for the performance, and, occasionally, even permits the use of circuits that have been previously discarded as inoperable with proper margins when analyzed on a worst-case basis. Even in relatively complex circuits, the algebraic method of analysis, together with some simplifying assumptions, can frequently be used to give a first-order approximation of the degree of improvement that a thorough numerical statistical analysis would produce.

The techniques shown here have used up some, but not all, of the excess margin that was placed in the circuit specification by a worst-case analysis. This remaining conservatism in design (keeping tolerance failure rates two and three orders of magnitude below catastrophic component failure rates) is primarily a result of the present limited knowledge of end-of-life distribution data on components, and of component failure rates. In addition, it should be re-emphasized that, when failure probabilities as small as say 1 in 10^6 are being computed, the extrapolation techniques are likely to lead to large errors. The assumed normal or other exact mathematical distributions are good models near the mean, but become progressively uncertain for small probabilities. To a lesser degree, the curve fitting errors involved in the calculations and the accuracy of the mathematical model of the transistor also represent limitations. These techniques should, however, become more powerful as our understanding of component aging and failure mechanisms improves.

As a last word, it might be noted that these statistical techniques might find application in other tolerance limited logic circuits such as DCTL using silicon transistors, and some of the new Esaki diode logic circuits.

VI. Acknowledgment

The authors would like to thank R. E. Drummond for his work on the random number generator subroutine.

[13] R. Lindaman, "A theorem for deriving majority-logic networks within an augmented Boolean algebra," IRE Trans. on Electronic Computers, vol. EC-9, pp. 338–342; September, 1960.

Transient Analysis of Cryotron Networks by Computer Simulation*

MUNRO K. HAYNES†, MEMBER, IRE

Summary—A general method is derived for transient analysis of complicated nonlinear dynamical systems by use of a digital computer programmed to perform tensor transformations and numerical integration. Tensor methods, adapted from Kron's techniques, are used for converting circuit data into a form for transient simulation by numerical integration.

An IBM 704 program has been written for simulation of cryotron networks. This simulator has been used to study switching speeds of cross-latched cryotron flip-flops; five-stage, free-running, ring circuits; and a three-bit, self-timing, self-checking, binary, parallel adder. The adder circuit contains 233 circuit elements, including 93 cryotrons arranged in 55 meshes. Results of these studies are included.

Introduction

PRESENT computer-design standardization philosophy leads to the choice of a limited number of small basic circuits (building blocks, or logical blocks) based on a given group of components, the exhaustive testing of these blocks to ensure adequate margins for all possible operating conditions, and the release of these standard circuits for use by logical designers. The expectations are that all desired machine functions can then be accomplished by the interconnection of these standard circuits, and that the final assemblage will be practicably operable, barring logical errors, with reasonable margins. Such an approach is well justified when such interconnections can be readily made, when they can be readily altered to accommodate changes or correct errors, and when they have little effect (or at least effects easily allowed for) on the speed, timing, or margins of the assembled machine units.

Since it will be impractical in a superconducting-film machine to make more connections than are necessary, impossible to change a completed evaporated plate, and expensive to redesign masks for modified plates; and since the properties of the connecting lines will be large factors in determining the speed of operation, a new approach to circuit testing, approval, and standardization is necessary. It is especially necessary since many hundreds of superconductor elements will have to be fabricated at once on a single plate in order to achieve the desired reductions in size, operation times, and cost. It is important, therefore, to be able to test marginally and debug assemblages of elements by computer simulation before they are committed to physical realization in hardware.

Since the manual labor of writing the differential equations for simulation of such large networks would be prohibitive, it is desirable that the machine perform this task from a tabular description of the network elements and connections which can be readily generated manually. This may be readily accomplished in a routine manner by the use of tensor methods, which are mathematical tools for systematizing the formulation and machine solution of network problems. These tools are based on the invariance of fundamental physical laws with respect to coordinate systems, and involve the mechanization of transformations to and from Lagrangian generalized coordinates in such fashion as to make easy the formulation and solution of large networks. Further refinements could allow the machine to generate the network description itself from the Boolean equations describing the system, or from a logical block-diagram-connection table.

Tensor methods of network analysis have been well developed and expounded by Gabriel Kron.[1] A simpler exposition of those sections of Kron's work needed for only stationary networks has been written by Le Corbeiller.[2] These references fully cover the analysis of linearized networks.

In order to solve for the transient behavior of networks containing nonlinear elements, the method of simulation is by solution of the simultaneous differential equations by means of numerical integration by a digital computer. Kron's method, therefore, has been adapted for finding the values of the quantities which are to be integrated, and for performing the routine tensor operations involved in setting up the system of equations from the input data. The mesh method, in which the currents are independent variables, is used herein since cryotrons are current-operated devices. The junction-network method, however, could be used by analogy for other nonlinear elements if desired.

Since this method depends on direct treatment of the differential and integral operators, p and $1/p$, some restrictions are required on the format of the "impedance" matrix $[Z]$ and of the "mesh-connection" matrix $[C]$, in order to insure that certain transformed matrices are nonsingular.

Mesh Method

The starting point for this analysis consists of three

* Received by the IRE, August 2, 1960. This work was supported by the Bureau of Ships, Dept. of the Navy.

† IBM Corp., Poughkeepsie, N. Y.

[1] G. Kron, "Tensor Analysis of Networks," John Wiley and Sons, Inc., New York, N. Y.; 1939.

[2] P. Le Corbeiller, "Matrix Analysis of Electric Networks," John Wiley and Sons, Inc., New York, N. Y.; 1950.

primitive matrices: the primitive inductance matrix $[L]$, the primitive resistance matrix $[R]$, and the primitive elastance matrix $[S]$. For physically realizable passive electrical networks, the $[R]$ and $[S]$ matrices are diagonal, and the $[L]$ matrix is symmetrical when it is not diagonal. The method, however, would apply even if mutual resistances or capacitances, or unilateral linear couplings, were included. Let us designate the primitive element matrix $[Z]$, composed from the $[L]$, $[R]$, and $[S]$ matrices as follows:

$$Z = \begin{bmatrix} L & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & S \end{bmatrix}.$$

This differs from the usual primitive impedance matrix in that the operators p and $1/p$ have been omitted and the inductive, resistive, and capacitive elements have been grouped into submatrices.

The next step is to choose the set of independent mesh currents forming the mesh-current matrix $[i']$. The choice of the mesh currents determines the transformation matrix $[C]$, such that $[i]=[C]\ [i']$, where $[i]$ is the primitive element current matrix

$$[i] = \begin{bmatrix} i_L \\ i_R \\ i_S \end{bmatrix}.$$

The values of the matrix $[i]$ are generally the unknown response currents which are to be determined. To insure nonsingularity of transformed matrices, the mesh currents must be chosen in such an order that

$$[i] = [C][i'] = \begin{bmatrix} i_L \\ i_R \\ i_S \end{bmatrix} = \begin{bmatrix} C_1 & 0 & 0 \\ C_2 & C_3 & 0 \\ C_4 & C_5 & C_6 \end{bmatrix} \begin{bmatrix} i_1' \\ i_2' \\ i_3' \end{bmatrix},$$

where the submatrix $[i_1']$ contains all the assumed mesh currents which flow through inductances, the submatrix $[i_2']$ contains all those which flow through resistances and capacitances only, and $[i_3']$ contains those which flow only through capacitances.

The network is assumed to be driven by constant-voltage generators connected in series with elements of the primitive networks such that $[e]$ is the primitive element EMF matrix,

$$[e] = \begin{bmatrix} e_L \\ e_R \\ e_S \end{bmatrix}.$$

These values are assumed to be either known or computable.

The network equation in the mesh-impedance form, including the operators p and $1/p$, is then

$$[e'] = [C_t] \begin{bmatrix} pL & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & \frac{1}{p} S \end{bmatrix} [C][i'],$$

where $[e']=[C_t]\ [e]$, and $[C_t]$ is the transpose of $[C]$. Replacing the operators p and $1/p$ by their operations, and partitioning, we obtain

$$[C_t] \begin{bmatrix} e_L \\ e_R \\ e_S \end{bmatrix} = [C_t][Z] \left[\begin{array}{ccc|ccc} C_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & C_3 & 0 & C_2 & 0 & 0 \\ 0 & 0 & C_6 & 0 & C_5 & C_4 \end{array}\right] \left[\begin{array}{c} \frac{di_1'}{dt} \\ i_2' \\ \int i_3' dt \\ \hline i_1' \\ \int i_2' dt \\ \int i_1' dt \end{array}\right].$$

The equation may then be solved for

$$\begin{bmatrix} \frac{di_1'}{dt} \\ i_2' \\ \int i_3' dt \end{bmatrix} = \begin{bmatrix} C_t Z \begin{bmatrix} C_1 & 0 & 0 \\ 0 & C_3 & 0 \\ 0 & 0 & C_6 \end{bmatrix} \end{bmatrix} - 1$$

$$\times \left[\begin{array}{c} C_t Z \begin{bmatrix} 0 & 0 & 0 \\ -C_2 & 0 & 0 \\ 0 & -C_5 & -C_4 \end{bmatrix} \end{array} \middle| \begin{array}{c} C_t \end{array}\right] \left[\begin{array}{c} i_1' \\ \int i_2' dt \\ \int i_1' dt \\ \hline e_L \\ e_R \\ e_S \end{array}\right],$$

and the nonsingularity of the matrix to be inverted has been assured by the imposed restrictions.

At any point in time t_n in the simulation process, the values of i_1', $\int i_2' dt$, and $\int i_1' dt$ are known from the integration process, and the values of the e_L, e_R, e_S either are known as a function of time or are calculable from known values. By the preceding equation, the values of the di_1'/dt, i_2', and $\int i_3' dt$ can be calculated, and the numerical integration process

$$\int \begin{bmatrix} \frac{di_1'}{dt} \\ i_2' \\ i_1' \end{bmatrix} dt = \begin{bmatrix} i_1' \\ \int i_2' dt \\ \int i_1' dt \end{bmatrix}$$

determines the values of the i_1', $\int i_2'dt$, and $\int i_1'dt$ at the next point in time, t_{n+1}. Further details of the numerical-integration process are outside the scope of this paper.[3,4] The unknown values of currents flowing through the elements at t_{n+1} can then be determined. The node-pair voltages $[E_S]$ across the capacitors are related to the currents $[i_S]$ by $[E_S]=[S]\ [i_S]$, and therefore

$$\begin{bmatrix} i_L \\ i_R \\ E_S \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & C_3 & 0 \\ 0 & 0 & SC_6 \end{bmatrix} \begin{bmatrix} \dfrac{di_1'}{dt} \\ i_2' \\ \int i_3'dt \end{bmatrix} + \begin{bmatrix} C_1 & 0 & 0 \\ C_2 & 0 & 0 \\ 0 & SC_5 & SC_4 \end{bmatrix} \begin{bmatrix} i_1' \\ \int i_2'dt \\ \int i_1'dt \end{bmatrix}.$$

This completes the method of solution of all-mesh (or, by analogy, all-junction) networks. The method can be generalized (see Appendix to this paper) to cover the mixed method,[5] which allows both voltage and current generators, and both unknown mesh currents and unknown node-pair voltages. For simpler cases, where one or more types of element or types of mesh are not present, the corresponding segments of the preceding matrices are omitted, and the equations take on simpler forms.

Cryotron-Circuit Representation

A lumped-constant L-R network is an adequate representation for cryotron circuits presently contemplated. The circuit capacitances can be ignored where the normal gate resistances are an order of magnitude less than the transmission-line characteristic impedances. Assuming no capacitances, and asserting that no all-resistive meshes are necessary, the transformation matrix $[C]$ becomes

$$[C] = \begin{bmatrix} C_1 \\ C_2 \end{bmatrix}, \quad \text{and} \quad [Z] = \begin{bmatrix} L & 0 \\ 0 & R \end{bmatrix}.$$

The equations then become

$$\begin{bmatrix} \dfrac{di_1'}{dt} \end{bmatrix} = \left[C_t Z \begin{bmatrix} C_1 \\ 0 \end{bmatrix} \right]^{-1} \times \left[C_t Z \begin{bmatrix} 0 \\ -C_2 \end{bmatrix} \middle| C_t \right] \left[\begin{array}{c} i_1' \\ \hline e_L \\ e_R \end{array} \right],$$

$$[i_1'] = \int \left[\frac{di_1'}{dt} \right] dt, \quad \text{and} \quad \begin{bmatrix} i_L \\ i_R \end{bmatrix} = \begin{bmatrix} C_1 \\ C_2 \end{bmatrix} [i_1'].$$

A critical factor in simulation of nonlinear elements is the method of representation chosen for them. We have represented here superconducting-film elements as inductances having zero resistance. The normal resistance of a gate, which appears under influence of control current, is represented by a voltage generator, in $[e_L]$, in series with the gate element. If the magnitude of the control current exceeds the threshold value, the generator voltage is set equal to the product of the gate current and the normal gate resistance. If the magnitude of the control current is less than threshold, the gate is superconducting and the generator voltage is set to zero.

No allowances are made for transition times of the gates, thermal effects, Silsbee effect, variation of normal gate resistance with currents, nor for variation of threshold with gate currents. More sophisticated representations could no doubt be included in the programming. This representation focuses attention on the stored magnetic-field energy about the inductive elements and its dissipation in the normal gate elements during switching operations.

Circuit-Description Data

A program for simulation of L-R cryotron networks by this method on the IBM-704 has been completely written, tested, and debugged. The program has been so written as to permit a maximum of convenience possible to the user, both in the amount and form of circuit description data to be inserted, and in the form of available data output possible with a printer. The user must furnish five kinds of input data, on standard SHARE SAP decimal format cards, to describe the circuit: 1) the circuit dimensions, 2) the primitive element matrix $[Z]$, 3) the transposed transformation matrix $[C_t]$, 4) a tabular description of the cryotrons, and 5) a tabular description of any pulse generators connected to the circuit.

The dimensions of the circuit include: 1) the number of true resistive elements in the circuit, 2) the number of inductive elements in the circuit, including the cryotron gates and controls, 3) the total number of circuit elements, and 4) the number of independent meshes in the circuit. The number of such meshes equals the total number of circuit elements minus the number of nodes, plus the number of separable parts.

The primitive element matrix $[Z]$ is entered as a list of the self-inductance values and the resistance values, followed by any mutual-inductance values with their identification.

The transposed transformation matrix $[C_t]$ is entered in a simple form as a list of which of the circuit elements are traversed, and in which direction, by each of the chosen mesh currents.

The cryotron table contains four items for each cryotron: 1) the identity of the inductive element which

[3] H. M. Gurk and M. Rubinoff, "Numerical solution of differential equations," *Proc. EJCC*, Philadelphia, Pa., pp. 58–63; 1954.
[4] The subroutine used is a version of the IBM 704 SHARE program PK NIDE, rewritten for maximum speed and for greater ease of use in matrix operations.
[5] Le Corbeiller, *op. cit.*, p. 79.

is the gate, 2) the identity of the inductive element which is the control, 3) the normal resistance of the gate, and 4) the threshold current value for the control.

The pulse-generator table contains five items for each generator: 1) the identity of the inductive element with which the generator is in series, 2) the voltage value when on (zero is assumed when off), 3) the turn-on time, 4) the turn-off time, and 5) the period after which the pulse cycle repeats.

The program operates in a compiling mode, thus needing only reloading, not reassembly, for any changes in input data or circuit dimensions. The program converts the input data to binary, rearranges it in the form for fastest computation, performs the necessary tensor transformations involved in generating the derivative program, and does all the set-up work for solving the differential equations.

When all these compilations and transformations have been done, the program starts simulation of the circuit by integration of the differential equations. At intervals specified, the program will print the values of time and the mesh currents, and also the currents through any elements designated by a control list. The program also gives a plotted output on the on-line printer (SHARE Subroutine WH0020) of the currents through any six elements designated by a control list. The plotted output is much like a six-beam oscilloscope trace, enabling the user to know quickly what the computer is doing and to modify input data accordingly.

The Cross-Latched Flip-Flop

Detailed switching-speed studies have been made of the cross-latched cryotron flip-flop by use of this simulation program. As shown in Fig. 1, the flip-flop circuit consists of the two cross-latching gate elements, L_2 and L_5, controlled, respectively, by control elements L_3 and L_4. Input to the flip-flop is effected by switching either gate element L_6, or gate element L_8, by current in the corresponding control driven by pulse input source E_{14}, or E_{15}. Output loads are simulated by L_{16} and L_{17}, driven by gate elements L_{11} and L_{12} which in turn are controlled by elements L_{10} and L_{13} in the flip-flop.

The dc supply current I_S is furnished by the power source E_1. The following circuit inductances have been assumed: gate element $= 10^{-12}$H, control element $= 10^{-11}$H, the inductance of interconnecting leads equal to that of gate elements of equal length. The resistance of a gate in the normal state has been assumed to be 1 milliohm, and the critical control-current threshold (above which the associated gate becomes normal) has been assumed to be 140 milliamps. The supply-current lead inductance L_1 has been chosen large enough (2 millihenries) to insure reasonable stability of the supply current and also to simulate the connecting lead for the dc power from outside the dewar into the cryotron flip-flop. The magnitude of the input-pulse-source inductances L_{14} and L_{15} has been chosen arbitrarily as 2 microhenries, which in combination with the resistor values R_2 and R_3 determines the input-pulse rise time of 40 millimicroseconds. This value was chosen in order to obtain input-pulse rise times reasonably comparable to those found in an over-all circuit environment of similar flip-flops.

The output-circuit-load inductances L_{16} and L_{17} were assumed to have values equal to that of a single control element plus the equivalent to five lengths of connecting leads. This is designed to simulate the input to another similar circuit located in close proximity to the flip-flop. The switching times quoted herein do not include the rise-time effects in the input-pulse circuits, but rather are measured from the first instant at which the input gates L_6 or L_8 become resistive in response to the input pulse.

The possible intermediate states of the flip-flop during transition may be most readily plotted as in Fig. 2, wherein we have shown the current I_2 in gate L_2 as a function of I_3, the current in L_3. Since the total supply current I_S will be constant during any transition, the possible states of the flip-flop during transition are described by a straight-line locus of slope minus 1 such as the lines E, F, G, or H in Fig. 2. The critical thresholds for the cross-latching elements, as well as for the output cryotrons, are shown as the dotted lines A and B. The additional dashed lines C and D, having slopes of plus 1 and plus 2, respectively, represent loci of intermediate terminal values during the transition process.

Let us assume that the circuit starts with initial conditions of supply current $= I_3 = 240$ milliamperes,

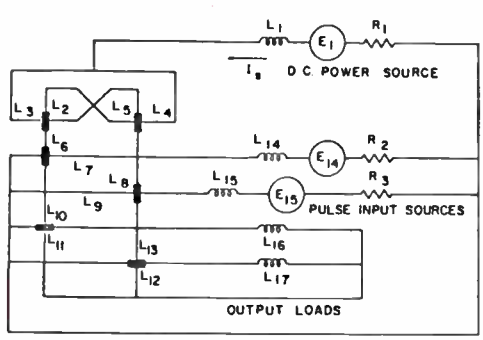


Fig. 1—Cross-latched cryotron flip-flop.

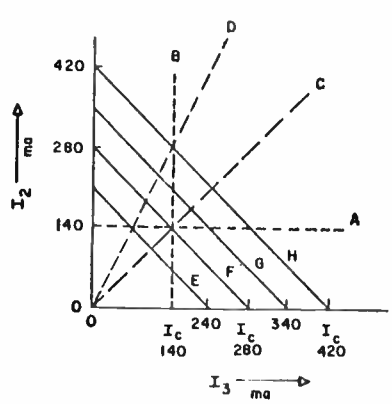


Fig. 2—Flip-flop transition paths.

and $I_2=0$. This is the intersection of line E with the horizontal axis in Fig. 2. At the moment that the current I_9 in L_9 exceeds 140 milliamps, a resistance of one milliohm will appear in gate element L_8. Since now elements L_2 and L_8 are both resistive and of equal value, the supply current will tend to divide evenly. The circuit will then describe an exponential transition from its initial state along line E toward its intersection with line C. Line C represents the locus of points of equal distribution of current on the two sides of the flip-flop. At a point in time 44 millimicroseconds after the beginning of this transient, the circuit will have reached the intersection of line E with line B, representing the fact that the control current I_3 affecting gate element L_2 is no longer greater than the critical-control threshold.

At this point gate L_2 will cease to be resistive, and will revert to the superconducting state. From this point the circuit will move exponentially along line E toward its intersection with the vertical axis, since there is now the 1-milliohm resistance of L_8 in one side of the flip-flop and zero resistance in the other side. However, at a point in time 60 millimicroseconds after the initiation of the original transient the circuit will have progressed to the intersection of line E, with line A, representing the fact that control current L_4 is now greater than the critical-threshold value. At this point, gate element L_5 becomes resistive. Since there are two resistive gate elements in one side and no resistance in the other side, the circuit now moves at twice its previous rate toward the final equilibrium value at the intersection of line E with the vertical axis.

This transition point at 60 millimicroseconds also represents the point where the current in control element L_{10} exceeds the threshold, and causes gate element L_{11} to become resistive, thereby initiating the transient in the output load circuit. At a later time, in this case 89 millimicroseconds from the beginning of the transition, the output current I_{17} will rise to the critical current threshold value, and will then initiate the transient in the circuit coupled to it.

The transition times determined from the simulation output, corresponding to Fig. 2, are plotted in Fig. 3 as a function of supply current I_S. It will be noted from these curves that the transition times become very large when the supply current is in the neighborhood

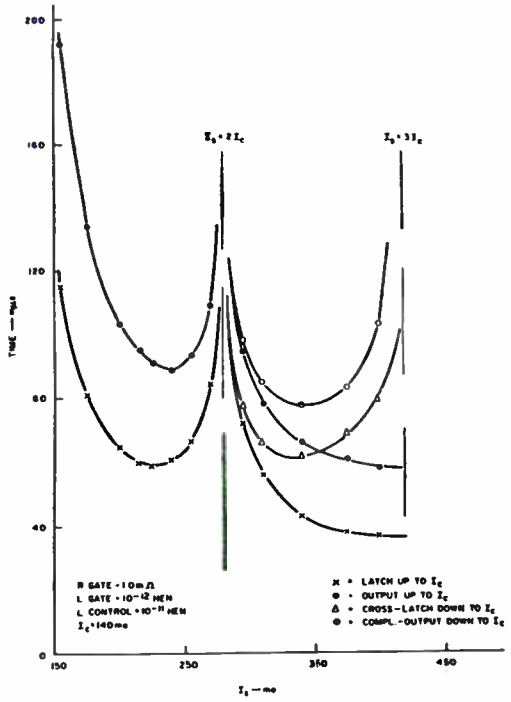


Fig. 3—Cross-latched flip-flop switching times vs supply current.

```
      DEC 20,17,3,5        NPGL
      DEC 2E-3
      DEC 1E-12
      DEC 1E-11
      DEC 1E-11
      DEC 2E-12
      DEC 2E-12
      DEC 1.1E-11
      DEC 2E-12
      DEC 1.1E-11
      DEC 1E-11
      DEC 2E-12
      DEC 1E-12
      DEC 1.1E-11
      DEC 4E-5,4E-5
      DEC 1.5E-11
      DEC 1.5E-11
      DEC 1E3
      DEC 1E3
      DEC 1E3
      OCT 0
      TRA 2,4
      DEC +1,+2,+4,+6,+10,+17,+12,+18, CT
      DEC +2,+4,+5,+10,-13,-8,-5,-3,
      DEC -14,+7,+19,
      DEC +16,+11,-12,-17,
      DEC +15,+9,+20,
      TRA 2,4              LAST CARD
      DEC 2,3,.001,.14     CRY DESC.
      DEC 5,4,.001,.14
      DEC 6,7,.001,.14
      DEC 8,9,.001,.14
      DEC 11,10,.001,.14
      DEC 12,13,.001,.14,
      TRA 2,4
      DEC 1
      DEC 375.0
      DEC -1.0,1E10,1E30
      DEC 14
      DEC 375.0
      DEC 300E-9,600E-9,600E-9
      DEC 15
      DEC 375.0
      DEC 0,300E-9,600E-9
      OCT 7
      TRA 2,4
      DEC 1,2,3,7,9,16,17  IPRT
      OCT 0
      TRA 2,4
      DEC 2,3,7,9,16,17,0              IPLOT
      TRA 2,4
      DEC ,,,,,,           IMIX
      TRA 2,4
      DEC .375,.375,.375,.375,.375,.375
      TRA 2,4
      DEC .375,-.375,.375,.375,0
1059  DEC 2E-9
1060  OCT 1
      TRA 2,4
```

Fig. 4—Input data cards for cross-latched flip-flop, $I_S=375$ ma.

either of I_C, $2I_C$, or $3I_C$.

If, for example, the supply current were 280 milliamps (equal to $2I_C$ as in the case of line F, Fig. 2), the transition path is along line F toward the intersection with line C as the limit of the exponential. The circuit will therefore approach the intersection with line C at an extremely low rate, and the time to reach the intersection with line A or line B (for values of I_S in the neighborhood of 280) will be extremely long. A similar situation results in the case of $I_S=3I_C$, as shown in line H of Fig. 2.

For values of I_S greater than $3I_C$, the circuit will be unable to complete a transition to the opposite stable state. Once the circuit has reached intersection with line D, this will be an equilibrium point, as long as the input currents are maintained. The circuit will therefore never reach the intersection with line B, which is required before the cross-latching operation can be completed.

A listing of the input data cards for the case $I_S=375$ ma is shown in Fig. 4, and the corresponding output plot from the computer is shown in Fig. 5. This run required about two minutes of IBM 704 computer time.

It will be noted from Fig. 2 that for supply currents greater than $2I_C$, the circuit transition will be through a region where both sides of the flip-flop and both sides of the output circuit will have current levels greater than threshold. As a result, the circuit switching time for these cases is best measured by the time to the last transition point, that is, when the complementary current level drops below threshold. This occurs at the intersection with line B, Fig. 2. The corresponding times are plotted as triangles in Fig. 3. The fastest circuit-operation speeds are obtained in a region of supply currents near 340 milliamps, or at $I_S \simeq 2.4\ I_C$. However, the circuit power dissipation for this case will be very much greater than for the other maximum-speed region which occurs at near 240-milliamps supply current, or at $I_S \simeq 1.71\ I_C$.

The next case of interest to be studied is the one where input to the flip-flop is controlled by two gates in parallel on each side, rather than by one as in the previous case. The parallel-gate situation arises where it is desired to obtain a logical AND condition as a means of controlling the input to the flip-flop. This situation is easily simulated by considering the effective input gate resistance to be 0.5 milliohm.

The possible paths of operation may be plotted as in Fig. 6, and the calculated switching times are shown in Fig. 7. The circuit transition proceeds exponentially from the intersection of the line (such as line E) with the horizontal axis upward toward the intersection with line C, whose slope is $+1/2$. When the intersection with line B is reached, the transition of gate L_2 occurs.

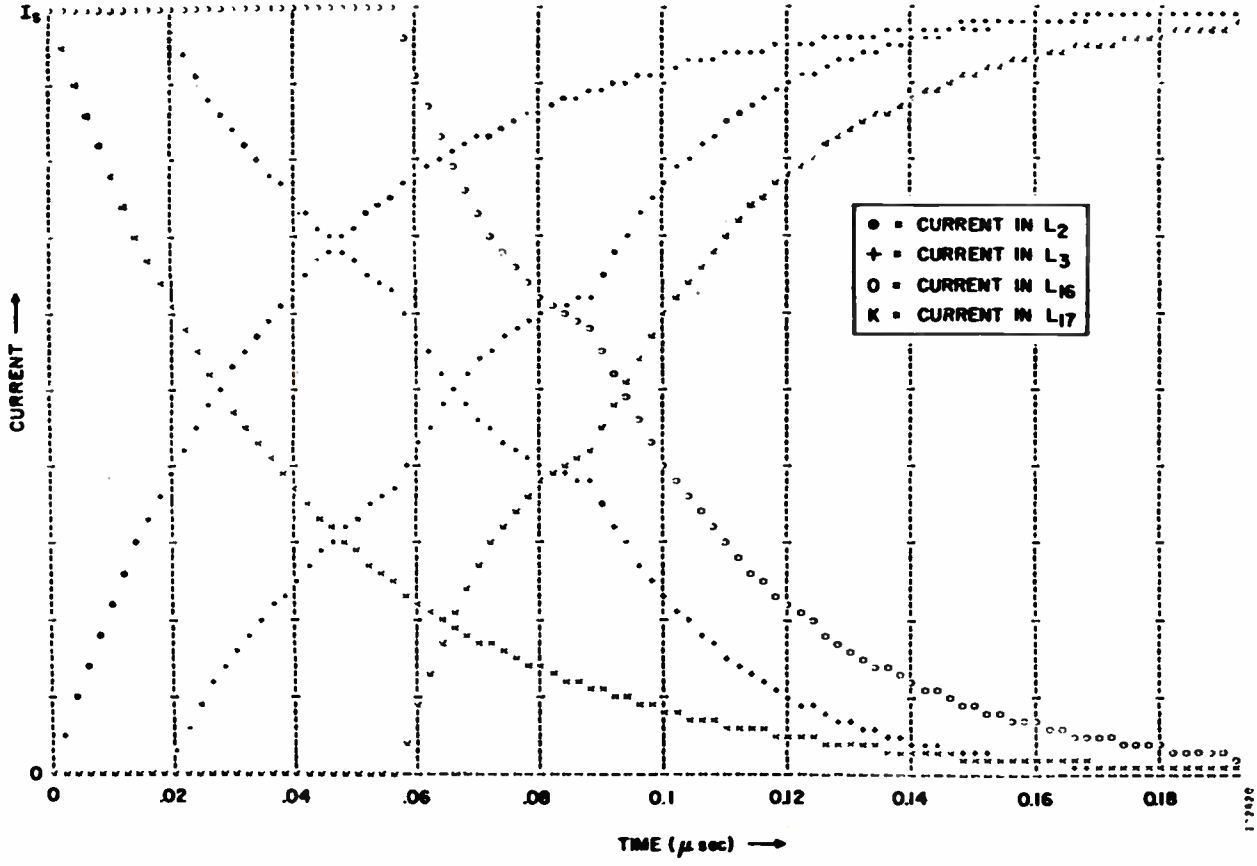


Fig. 5—Computer output plot for cross-latched flip-flop, $I_S=375$ ma.

Thereafter, the circuit approaches the intersection, with the vertical axis as the limit of the exponential. However, if the supply current were to be 1.5 times I_C, as shown in line D of Fig. 6, the circuit would approach the intersection with lines B and C exponentially with a very large resultant switching time.

For supply current values greater than 1.5 I_C the intersection with line C becomes a temporary equilibrium point, and transition to the other permanently stable state never occurs (as in cases $>3I_C$, past line H of Fig. 2). It is seen from Fig. 7 that the price for parallel input gates to the flip-flop is a very large increase in switching time and also a drastic reduction in the circuit tolerance to variations in the supply current.

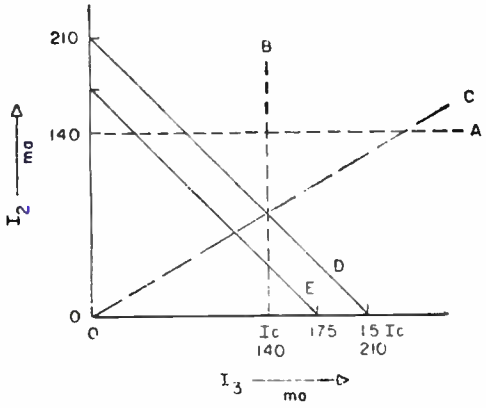


Fig. 6—Flip-flop transition paths with parallel input gates.

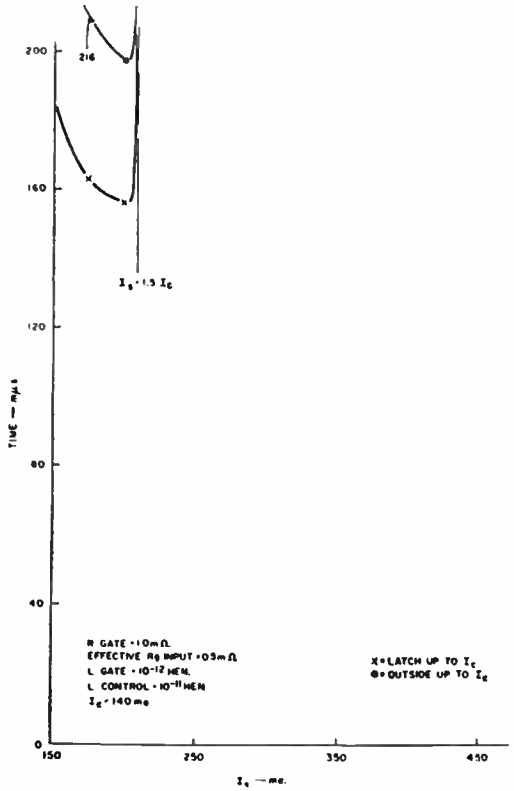


Fig. 7—Cross-latched flip-flop switching times vs supply currents: two gates, parallel input.

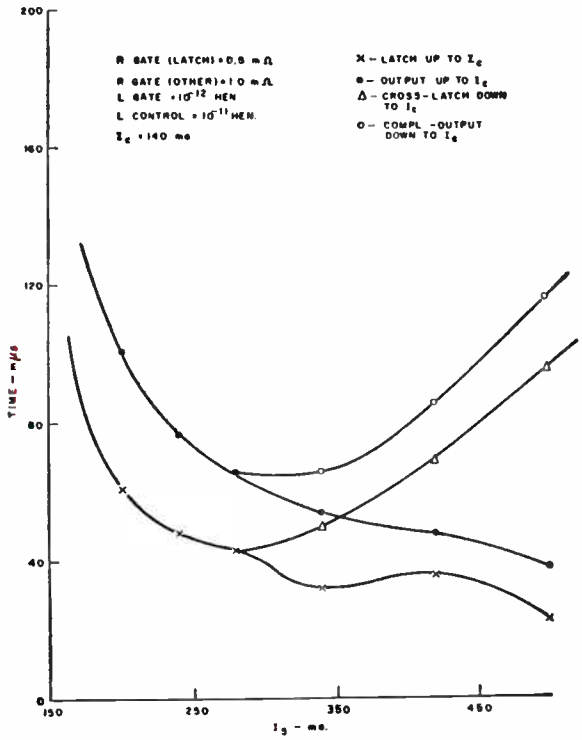


Fig. 8—Cross-latched flip-flop switching times vs supply current.

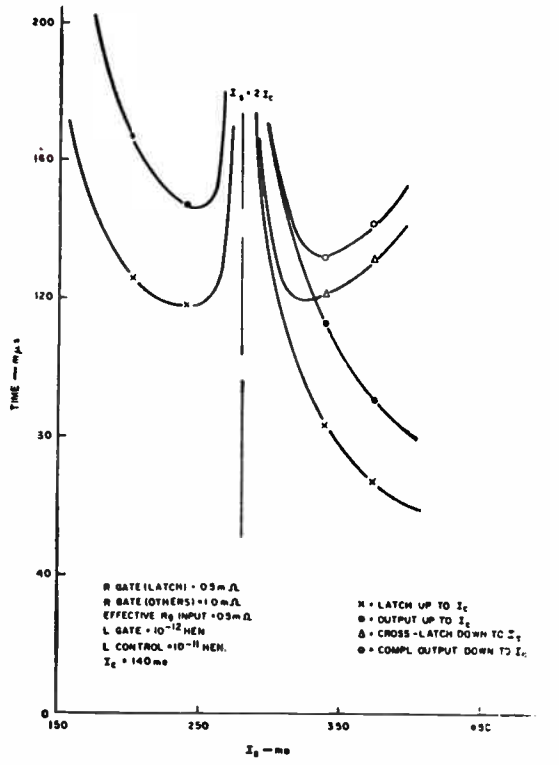


Fig. 9—Cross-latched flip-flop switching times vs supply currents: two gates, parallel input to flip-flop.

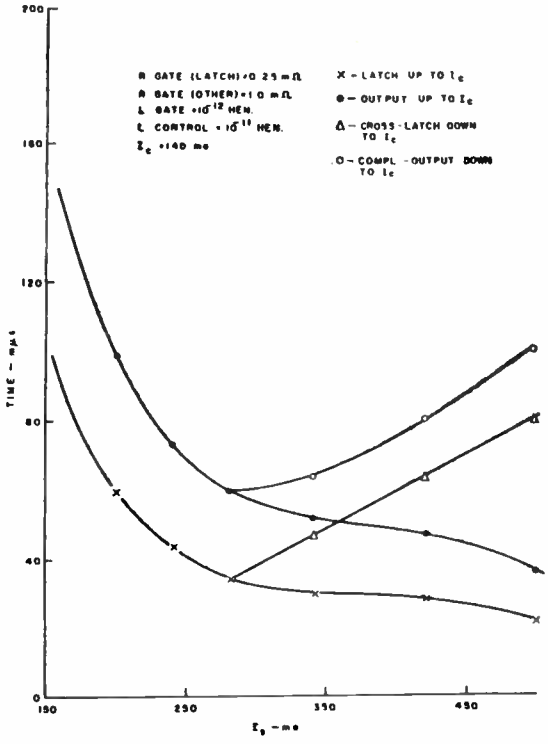


Fig. 10—Cross-latched flip-flop switching times vs supply current.

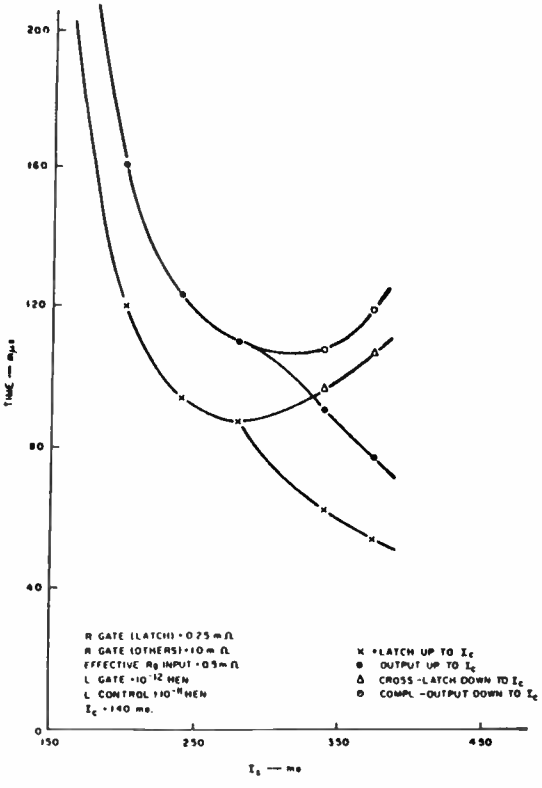


Fig. 11—Cross-latched flip-flop switching times vs supply current: two gates, parallel input to flip-flop.

Circuit operation can be much improved by lowering the value of the cross-latching gate resistances. This may be seen from the data of Fig. 8 wherein the normal resistance of the cross-latch gates has been reduced to 0.5 milliohm. This is the case of single input gates to the flip-flop and is therefore analogous to Fig. 3, except for the change in the latching gate resistances. It will be noted that there is a considerable improvement in switching speed, as well as a greater range of tolerance to variation in supply currents. This improvement may be extended to the case of parallel gates on the input to the flip-flop, as shown in Fig. 9. As may be seen, a considerable price is paid for the use of the parallel-gate AND-circuit input. However, tolerable operation can still be achieved, as shown by these data.

Further circuit improvement can be obtained by reducing the latching gate resistances still further. Circuit speeds are shown for the case of cross-latch gate resistances equal to 0.25 milliohm in Figs. 10 and 11, for single and parallel inputs to the flip-flop, respectively. From Fig. 11 we see that, by using latching gate resistances of one-fourth the resistance of the input gates, it is possible to achieve parallel-gate-input AND circuits in the flip-flop with but small losses in circuit operation speeds, and with reasonably wide margins for supply-current variations. These considerations indicate that where cross-latching gates are required as a precautionary measure, their gate resistances should be no more than one-fourth that of the input gates, especially if AND-circuit inputs are desired.

The Five-Stage Free-Running Ring Circuit

The second circuit to be studied by this simulation technique is the five-stage free-running ring circuit shown in Fig. 12. Such circuits have been operated at Arthur D. Little Corp.,[6] and by A. E. Brennemann of IBM.

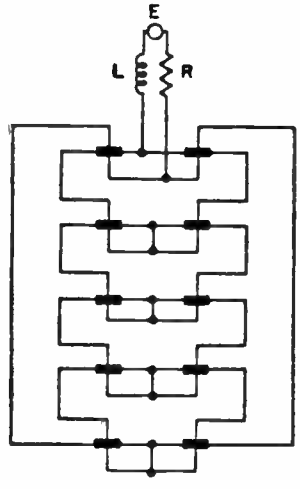


Fig. 12—Five-stage free-running ring circuit.

[6] A. E. Slade, "Thin film cryotrons; Part II—Cryotron characteristics and circuit applications," Proc. IRE, vol. 48, pp. 1514–1575; September, 1960.

No cross-latching is employed in this circuit, which consists of five storage loops coupled in cascade in such a way as to form a loop which may be unstable for certain values of the supply current.

For this circuit, the gate resistances in the normal state have been assumed to be 3 milliohms. The circuit inductances have been calculated from the layout. The gate inductances are 1.5×10^{-12}H, the control inductances 9.2×10^{-12}H, and the inductance of connecting leads equals that of gate elements of equal length. The critical control current threshold has been assumed to be 500 milliamperes.

For values of supply current less than I_C, this circuit will always be stable. For values of supply current greater than I_C and less than $2I_C$, the circuit is capable of existing either in a stable or an unstable mode, depending upon the initial conditions. If the supply current is increased from zero so that the current in each of the loops divides equally between the two possible paths, then all of the cryotrons will remain in the superconducting state and no oscillations will be observed, as long as the supply current remains below twice threshold and no other disturbances occur. If, however, the current in one of the loops is caused to divide, by some external means not shown, so that the current in one side of the loop exceeds threshold, then the circuit will be set into a free-running oscillatory condition which will persist until some external change forces it into another state.

For values of supply current greater than twice threshold, the circuit is also stable, provided an initial condition of current distribution can be achieved which exceeds threshold on both sides of each of the five circuit loops. However, a free-running oscillatory condition can also be achieved for supply currents greater than twice threshold under certain conditions. Once disturbed into an oscillatory mode by some external force, the circuit will continue to oscillate, provided the settling time for the transient in each of the circuit loops is reasonably short compared to its propagation time around the complete five-stage circuit. The interstage delay times, as caused by threshold phenomena, decrease with increasing values of supply current. Similarly, the transient propagation time around the ring decreases with increasing supply current. These variations are shown in the calculated data of Fig. 13. As the supply current is raised beyond the $2I_C$ value, a critical value of supply current will eventually be approached at which the propagating oscillatory mode is attenuated and the circuit goes into a stable equilibrium condition, regardless of its initial state. For the circuit constants chosen, this critical value is approximately 1400 milliamps, at which value the oscillatory condition decays slowly to the stable condition. At supply current values of 1500 milliamps or more, the oscillatory condition decays rapidly to the stable state in the course of a few cycles of propagation.

Fig. 14 illustrates the decay from oscillatory state to stable equilibrium at $I_S=1400$ ma, as reproduced from the output plot from the computer.

Three-Bit Self-Timing Self-Checking Binary Adder

Simulation tests have been run on the three-bit adder shown in Fig. 15. This adder contains 233 circuit elements when the pulse generator sources are included, of which 186 are gates and controls of the 93 cryotrons. The circuit requires 55 independent meshes for its solution. Circuit inductances were calculated from a standard grid spacing of 1/16 inch and assumed values of 24×10^{-12} henries per inch for the inductance per unit length of the gates and connecting lines, and 147×10^{-12} henries per inch for the controls. The normal gate resistances were assumed to be 2×10^{-3} ohms. Within these assumptions, the smallest possible shorted-line flip-flop on this standard grid would have a circuit L/R time constant of 10.6 mμsec. The threshold control current I_C was assumed to be 0.200 ampere, and simulation runs were made for supply current I_S values of 0.400 and 0.500 amperes. The adder inputs were assumed to be driven by current-pulse-generator sources of 10^8 ohms internal impedance, with sufficient series inductance to yield input circuit time constants of 30 mμsec. All times given are measured from the point where the rising input current first reaches the threshold value.

For the balanced case $I_s=2I_c=0.400$ ampere, and with the combination of inputs which gives the shortest possible carry, the delay until the last sum output reached 50 per cent was 93 mμsec, and the delay until the end-of-add output reached 50 per cent was 225 mμsec. When overdriven at $I_S=0.500$ amperes, the corresponding times were 81 mμsec and 200 mμsec, respectively.

Tests were also run for a combination of inputs so chosen as to give the longest possible carry situation. For the balanced case $I_S=0.400$ ampere, the delay until the last sum output reached 50 per cent was 268 mμsec, and that until the end-of-add reached 50 per cent was 345 mμsec, or an average carry delay per stage of about 60 mμsec. The carry delay is not uniform from stage to stage, and is dependent on the total number of stages in the adder. When overdriven at $I_S=0.500$ ampere, for the same case of longest possible carry, the corresponding times were 291 mμsec, and 390 mμsec, respectively. This is an average carry delay of 95 mμsec, around 50 per cent longer than for the balanced case, thus demonstrating that speed improvements cannot always be achieved by overdriving on the supply current.

The computer output plot for the longest carry situation and $I_S=0.500$ ampere is shown in Fig. 16. This run required 15 minutes of IBM 704 time for compilation and 45 minutes for simulation.

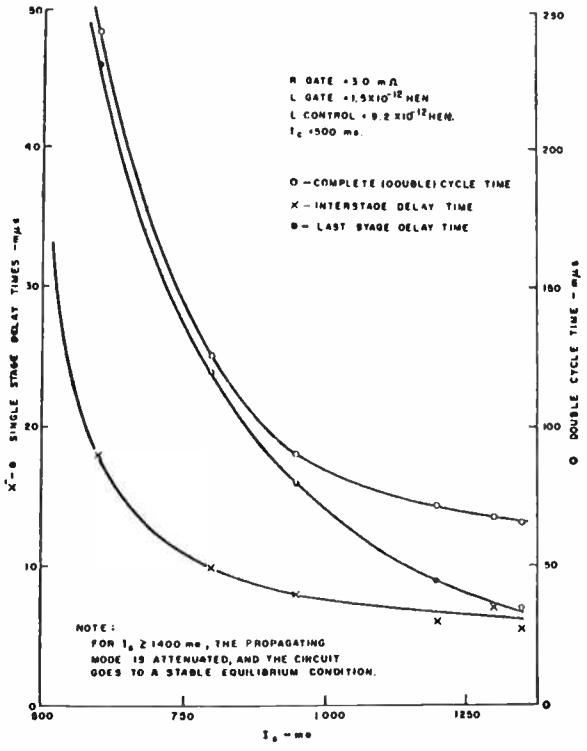


Fig. 13—Five-stage free-running ring circuit cycle and stage delay times vs supply current.

Conclusion

It is possible to study transient responses of complicated nonlinear dynamical systems in a routine manner by use of a digital computer programmed to perform tensorial transformations, threshold discrimination, and numerical integration. Such a program has been written for lumped inductive-resistive circuits consisting of cryotrons, and has proven a useful tool for study of such circuits under marginal conditions.

Appendix

The method of solving mesh networks for transients can be generalized to cover the mixed method, or Kron's "orthogonal network." The transformation tensor becomes

$$[C] = \begin{bmatrix} C_1 & 0 & 0 & C_7 \\ C_2 & C_3 & 0 & C_8 \\ C_4 & C_5 & C_6 & C_9 \end{bmatrix},$$

so that

$$\begin{bmatrix} i_L \\ i_R \\ i_S \end{bmatrix} = \begin{bmatrix} C_1 & 0 & 0 & C_7 \\ C_2 & C_3 & 0 & C_8 \\ C_4 & C_5 & C_6 & C_9 \end{bmatrix} \begin{bmatrix} i_1' \\ i_2' \\ i_3' \\ i_4' \end{bmatrix}.$$

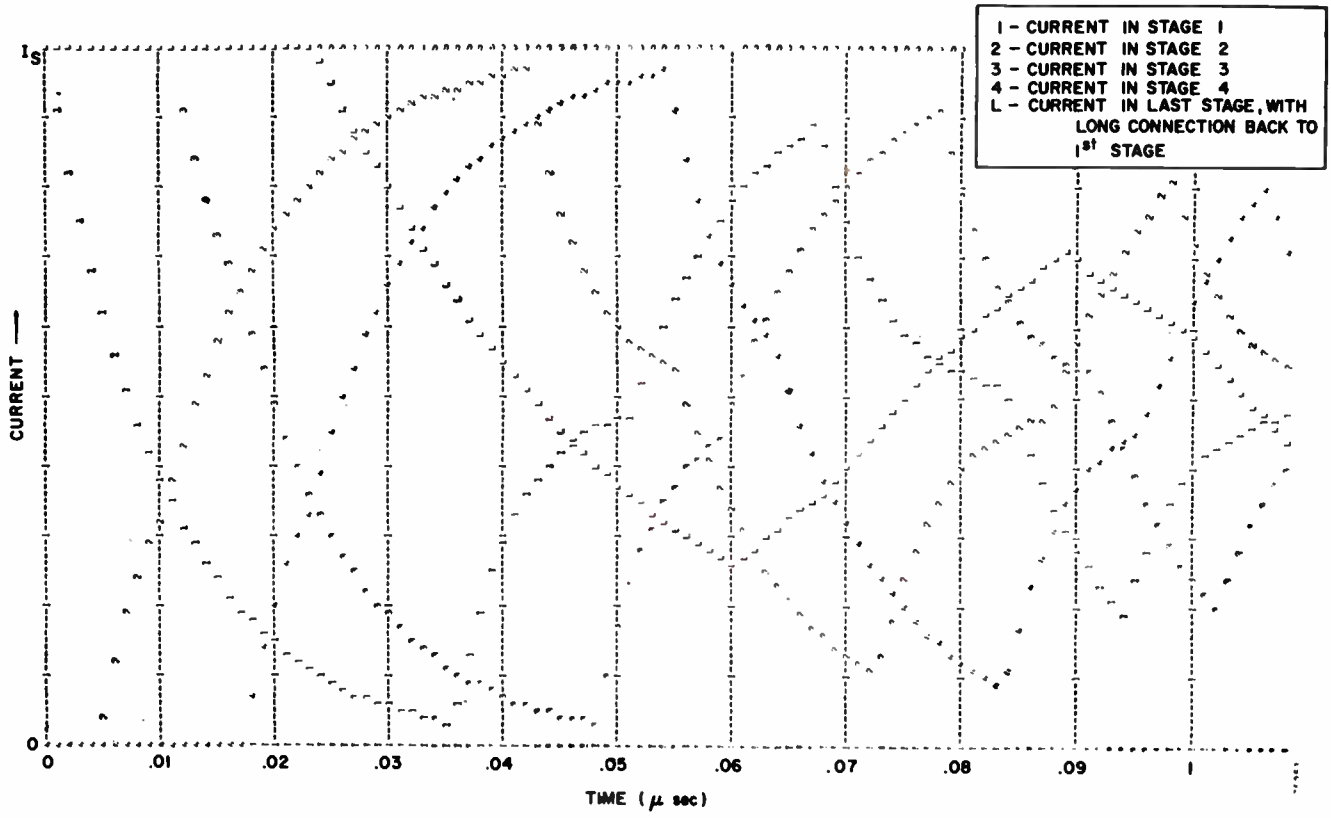


Fig. 14—Computer output plot for five-stage ring, $I_S = 1400$ ma.

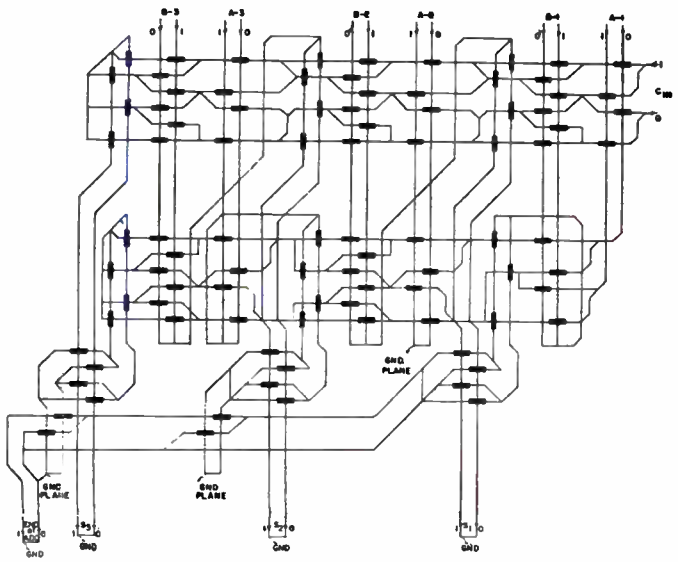


Fig. 15—Three-bit adder.

The equation of voltage is then of the form

$$\begin{bmatrix} E_1' \\ E_2' \\ E_3' \\ E_4' \end{bmatrix} + [C_t] \begin{bmatrix} e_L \\ e_R \\ e_S \end{bmatrix}$$

$$= [C_t] \begin{bmatrix} pL & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & \frac{1}{p}S \end{bmatrix} [C] \left(\begin{bmatrix} i_1' \\ i_2' \\ i_3' \\ i_4' \end{bmatrix} + [C]^{-1} \begin{bmatrix} I_L \\ I_R \\ I_S \end{bmatrix} \right).$$

All the $[E_1']$, $[E_2']$, $[E_3']$ (on mesh axes) are known (or zero). The $[E_4']$ (on junction pair axes) are the added unknown junction-pair voltage variables. All the $[i_1']$, $[i_2']$, $[i_3']$ (on mesh axes) are unknown mesh variables as before. The $[i_4']$ are the added known (or zero) impressed currents on junction-pair axes. The $[I_L]$, $[I_R]$, $[I_S]$ are known currents impressed across the actual

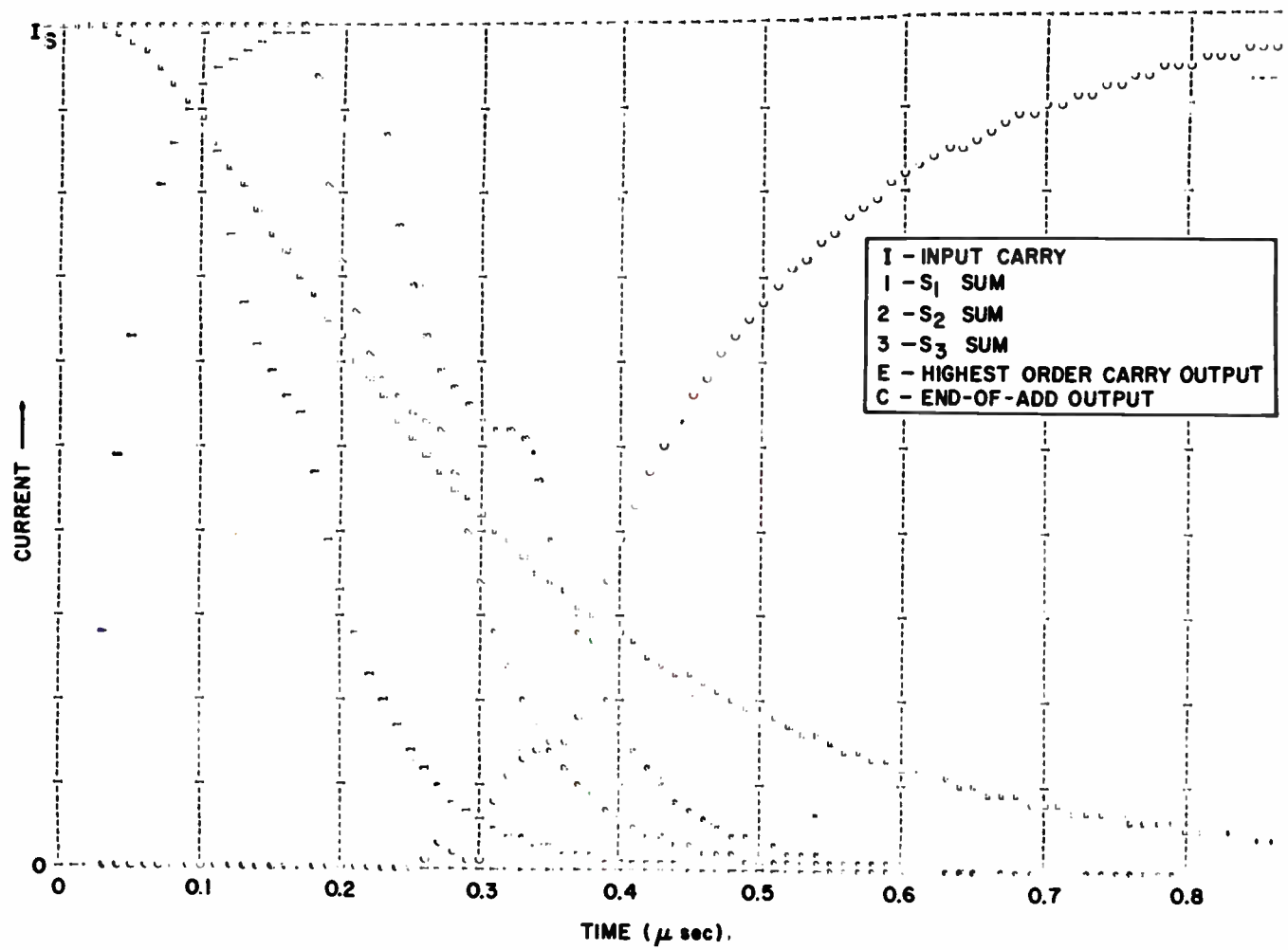


Fig. 16—Computer output plot for three-bit adder, $I_S = 500$ ma.

L, R, and S circuit elements. In general, $[C]$ must be square and nonsingular. A few reasonable restrictions, however, simplify the problem greatly. The inverse of $[C]$ is needed to find

$$\begin{bmatrix} I_1' \\ I_2' \\ I_3' \\ I_4' \end{bmatrix} = [C]^{-1} \begin{bmatrix} I_L \\ I_R \\ I_S \end{bmatrix}.$$

If it is assumed that the junction-pair axes are so chosen, in setting up $[C]$, that all of the nonzero elements of $[I']$ are along junction-pair axes (requiring that a junction-pair axis be chosen across each actual element across which a current source is impressed, then $[C]^{-1}$ is not required, $[C]$ need not be square, the $[I_1']$, $[I_2']$, $[I_3']$ are all zero, and the $[I_4']$ are known without calculation.

The equation of voltage then can be partitioned into mesh and junction-pair sections for solution, as follows:

$$\begin{bmatrix} E_1' \\ E_2' \\ E_3' \\ \text{---} \\ E_4' \end{bmatrix} + \begin{bmatrix} C_{mt} \\ \text{---} \\ C_{jt} \end{bmatrix} \begin{bmatrix} e_L \\ e_R \\ e_S \end{bmatrix}$$

$$= \begin{bmatrix} C_{mt} \\ \text{---} \\ C_{jt} \end{bmatrix} [Z] \left[\begin{array}{ccc|ccccc} C_1 & 0 & 0 & 0 & 0 & 0 & C_7 & 0 & 0 \\ 0 & C_3 & 0 & C_2 & 0 & 0 & 0 & C_8 & 0 \\ 0 & 0 & C_6 & 0 & C_5 & C_4 & 0 & 0 & C_9 \end{array}\right]$$

$$\times \begin{bmatrix} \dfrac{di_1'}{dt} \\ i_2' \\ \int i_3' dt \\ \text{---} \\ i_1' \\ \int i_2' dt \\ \int i_1' dt \\ \dfrac{d(I_4' + i_4')}{dt} \\ (I_4' + i_4') \\ \int (I_4' + i_4') dt \end{bmatrix}$$

where

$$[C_t] = \begin{bmatrix} C_{mt} \\ \text{---} \\ C_{jt} \end{bmatrix} = \begin{bmatrix} C_{1t} & C_{2t} & C_{4t} \\ 0 & C_{3t} & C_{5t} \\ 0 & 0 & C_{6t} \\ \text{---} & \text{---} & \text{---} \\ C_{7t} & C_{8t} & C_{9t} \end{bmatrix}.$$

The unknown variables which are to be integrated are found by

$$\begin{bmatrix} \dfrac{di_1'}{dt} \\ i_2' \\ i_3' dt \end{bmatrix} = \left[C_{mt} Z \begin{bmatrix} C_1 & 0 & 0 \\ 0 & C_3 & 0 \\ 0 & 0 & C_6 \end{bmatrix} \right]^{-1}$$

$$\times \left[\begin{bmatrix} E_1' \\ E_2' \\ E_3' \end{bmatrix} + \left[C_{mt} Z \begin{bmatrix} 0 & 0 & 0 & -C_7 & 0 & 0 \\ -C_2 & 0 & 0 & 0 & -C_8 & 0 \\ 0 & -C_5 & -C_4 & 0 & 0 & -C_9 \end{bmatrix} \middle| C_{mt} \right] \times \begin{bmatrix} i_1' \\ \int i_2' dt \\ \int i_1' dt \\ \dfrac{d(I_4' + i_4')}{dt} \\ \int (I_4' + i_4') \\ (I_4' + i_4') dt \\ \text{---} \\ e_L \\ e_R \\ e_S \end{bmatrix} \right].$$

The unknown variables $[E_4']$ are found by

$$[E_4'] = \left[\begin{array}{c|c|c} & \left[\begin{array}{ccc|ccc} C_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & C_3 & 0 & C_2 & 0 & 0 \\ 0 & 0 & C_6 & 0 & C_5 & C_4 \end{array}\right. & \left.\begin{array}{ccc} C_7 & 0 & 0 \\ 0 & C_8 & 0 \\ 0 & 0 & C_9 \end{array}\right] \\ C_{jt}Z & & [-C_{jt}] \end{array}\right] \times \begin{bmatrix} \dfrac{di_1'}{dt} \\ i_2' \\ \int i_3'dt \\ \hline i_1' \\ \int i_2'dt \\ \int i_1'dt \\ \dfrac{d(I_4' + i_4')}{dt} \\ (I_4' + i_4') \\ \int (I_4' + i_4')dt \\ \hline e_L \\ e_R \\ e_S \end{bmatrix}$$

and unknown element currents and voltages may be found by

$$\begin{bmatrix} i_L \\ i_R \\ E_S \end{bmatrix} = \left[\begin{array}{ccc|ccc|ccc} 0 & 0 & 0 & C_1 & 0 & 0 & 0 & C_7 & 0 \\ 0 & C_3 & 0 & C_2 & 0 & 0 & 0 & C_8 & 0 \\ 0 & 0 & SC_6 & 0 & SC_5 & SC_4 & 0 & 0 & SC_9 \end{array}\right] \times \begin{bmatrix} \dfrac{di_1'}{dt} \\ i_2' \\ \int i_3'dt \\ \hline i_1' \\ \int i_2'dt \\ \int i_1'dt \\ \dfrac{d(I_4' + i_4')}{dt} \\ (I_4' + i_4') \\ \int (I_4' + i_4')dt \end{bmatrix}.$$

As they stand, these equations require that the derivative of $[I_4'+i_4']$ be known at all times. Since few cases will arise where the derivative is known and is nonzero, it is appropriate to require that $[C_7]$ be zero, and to simplify by omitting the terms involving the derivative of $[I_4'+i_4']$.

An analogous set of equations for orthogonal junction networks can be readily derived.

High-Density Digital Magnetic Recording Techniques*

A. S. HOAGLAND†, SENIOR MEMBER, IRE, AND G. C. BACON†

One of the best papers published in the PGEC TRANSACTIONS in the past year is reprinted here to round out an important aspect of storage techniques, that of digital magnetic recording as employed on magnetic drums, discs, and tapes. This useful paper also provides an excellent example of the use of a digital computer as a tool in engineering design. It will be of value to those involved in telemetry recording and magnetic recording in general.—*The Guest Editor*

***Summary*—The merit of any high-density detection method is ultimately dependent on the "resolution" characteristic of the magnetic recording components. Justification of readback waveform synthesis through "single pulse" superposition is given. A comprehensive, yet general readback simulation program is described which will automatically, for any characteristic pulse, simulate all possible readback signal patterns and test them for specified reading logic as a function of bit density. Amplitude, phase, peak, etc., sensing are compared and the influence of parameter variation on performance indicated. Good correlation with experiment has been realized and has greatly reduced time at the bench. The significance of pulse waveform is clearly revealed and this study has provided a guide to head design (ring and probe), permitting the optimization of a total recording system for high-density storage.**

INTRODUCTION

MAGNETIC recording of data involves the storage and processing of binary information, utilizing two states which are capable of being differentiated. For convenience, consider nonreturn-to-zero (NRZ) recording in which the storage surface is continuously saturated during writing, in one direction for a "1" and in the opposite sense for a "0." A particular input is then composed of a succession of alternating step changes in writing current. Reading involves a derivative-type action, as indicated schematically below. Eq. 1 illustrates the over-all transfer process from input to output. The surface co-ordinate is x, and $\bar{x}$ represents the variable indicating the position of the specified surface magnetization relative to the magnetic head.

$$\underbrace{i(t) \rightarrow M(x)}_{\text{writing}} \cdots \underbrace{\phi_h(\bar{x}) \rightarrow vN d\phi_h/d\bar{x}}_{\text{reading}} = e(\bar{x}) = e(vt), \quad (1)$$

where

$M(x)$ = distribution of magnetization recorded in the storage surface,
$\phi_h(x)$ = reading coil flux as a function of surface position,
e = open-circuit readback voltage,
N = number of turns on the reading coil,
v = surface velocity, and
t = time.

Hence, $e(vt)$ is a pulse-like signal for a step change in $i(t)$,[1] and the surface velocity appears as a scaling factor in both time and amplitude for the output signal. An output voltage signal is then associated with each change in the direction of saturation or reversal in writing current.

Consider the output signals for arbitrary input patterns consisting of sequences of alternating step-like changes in writing current. On readback, the magnetic field present, caused by the recorded magnetization of the surface, is extremely weak and, hence, the magnetic head will behave very nearly as a linear element. Writing definition, corresponding to the width of a saturation transition region, is much less than the corresponding reading resolution because of the nonlinear surface saturation characteristic.[1] Therefore, adjacent changes in surface state will not modify one another even with considerable pulse crowding. These considerations imply that the principle of superposition may be usefully applied to the over-all input-output transfer process in investigating high density recording with the use of the characteristic step function output response. The width and waveform of this characteristic step function pulse response, $e(x)$, are thus extremely important. Such responses will be shown as functions of x, or distance, as in this manner they are most meaningful. Since the surface magnetization will consist inherently of an alternating train of magnetization reversals, the readback waveform may be regarded as an alternating pulse sequence. As indicated in the foregoing, the velocity enters only as a scaling factor between distance and time. Accordingly, bit density considerations may be derived directly from this type of analysis.

This superposition concept, as applied to digital magnetic recording, has been experimentally confirmed. As an example, Fig. 1 shows a readback waveform resulting from a given sequence of magnetization reversals along with the characteristic pulse of the system. Also shown is the signal waveform resulting from graphical superposition using $e(x)$. It is seen that the correspondence

* Reprinted from IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-9, pp. 2–11; March, 1960.
† IBM Research Laboratory, San Jose, Calif.

[1] A. S. Hoagland, "Magnetic data recording theory: Head design," *Commun. and Electronics*, vol. 27, pp. 506–512; November, 1956.

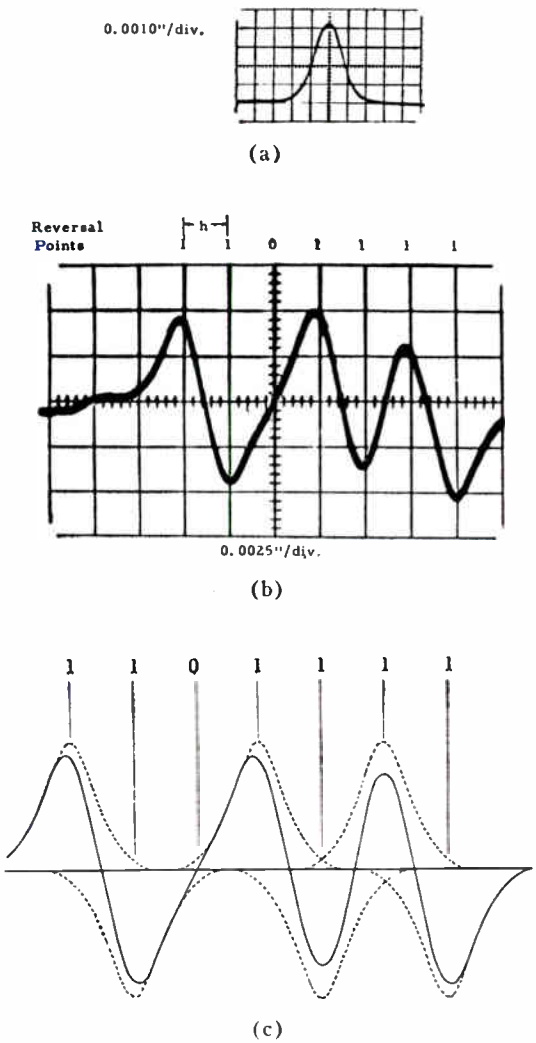


Fig. 1—Comparison of experimental and superimposed waveforms (1 = magnetization reversal). (a) Characteristic pulse $e(x)$. (b) Readback waveform. (c) Waveform resulting from superposition.

is quite good. The minimum separation of magnetization reversals, h_{min}, at which the use of superposition to predict output waveforms begins to break down, may be experimentally ascertained by noting the alternation density at which a marked deviation between the actual readback waveform and that obtained from graphical superposition commences. This point occurs beyond the present operating limits for bit density (set by pulse crowding) with currently employed detection techniques. Hence, the superposition concept is a powerful tool for the exploration of high-density recording. Actual factors causing perturbations of the recording system may be included and the over-all detection characteristics then examined.

The principle of superposition is employed, using $e(x)$, to synthesize the readback waveform for arbitrary binary sequences. Then, to study the density potential of various recording methods, each decoding procedure must be tested against all possible waveforms that could arise in a bit interval at each recording density; this examination must be continued as the density is increased until no error-free run is possible. The number of unique readback waveforms that may be encountered in a bit cell is a function of the degree of intersymbol interference, or pulse crowding, that may arise. For example, until h is chosen less than λ, the characteristic pulse basewidth, only one basic bit cell waveform will arise. If the waveform synthesis procedure includes all possible waveform patterns which result when up to three adjacent bits on both sides of a given bit can produce pulse response interference with the signal of the given bit, *i.e.*, XXX-XXX, then this procedure insures that the "worst" case will be considered with this degree of potential intersymbol interference. This degree of bit interaction was used in the work reported here. The choice of three adjacent bits corresponds to a range for n (where n is the numbering of adjacent bit cells) of from -3 to $+3$ based on the expectation that the actual feasible density limits encountered for the detection techniques studies would not lie beyond the corresponding permissible range of "total" recording pattern simulation. Needless to say, this latter condition did exist. Note that if $e(x)$ has a basewidth of λ, then with $n=3$ the corresponding waveform synthesis is valid until a pulse in an $n=4$ cell would interfere with the test cell. Thus, a maximum density of $7/\lambda$ alternations per inch can be simulated. This is three and one-half times the density at which recorded amplitude modulation, due to pulse crowding, commences to appear. If the density limit obtained with a given recording technique were to exceed $7/\lambda$ then the restriction on n_{max} would have to be modified to include provision for more extensive near-neighbor interaction.

The most common method of recording digital data is the NRZ method where either "1," "0," or a binary sequence change is represented by a step like reversal in current. Considered here is the version (NRZI) where the current is switched in direction each time a "1" is to be recorded. An output pulse is then associated with each recorded "1." We will first indicate the basic simulation method for two sensing schemes, amplitude sensing and peak sensing. These techniques enjoy considerable popularity as well as providing an illustration of the approach for two conceptually different methods to information detection, being predicted as they are on two entirely different signal waveform characteristics.

The simulation of waveform synthesis and the decoding process may be done on a digital computer. For the work here an IBM 650 computer program was developed wherein 40 points were used to represent a characteristic pulse signal. In addition, some very important operating considerations will be covered and the general utility of the program with respect to these practical aspects of recording will be demonstrated.

Amplitude Sensing

With NRZI recording the most common and direct method of detection is amplitude sensing where a "1" is indicated by the presence of a pulse and a "0" by the

absence of a pulse. This detection method is inherently relatively insensitive to base-line "noise." Of particular interest then is: what is the maximum storage density to which such a detection means can correctly operate? An error will result when, at sample time, $|e(0)| > e_T$ or $|e(1)| < e_T$. Here e_T is a preset discrimination level; $e(0)$ is the output amplitude from a recorded "0;" and $e(1)$ is the amplitude from a recorded "1." It should be apparent that in providing an equal margin of protection against the two ways in which an error could arise, e_T may vary as a function of density.

An answer can be given fairly directly to the above question if the characteristic pulse is symmetrical and an impulse strobe is assumed. Let ρ represent the pulse width from the pulse peak to the point on either side at which the pulse amplitude is equal to $\frac{1}{3}$ the magnitude of the pulse peak.

Now first consider an isolated "1" in a binary sequence. Then at a density equal to $1/\rho$ the adjacent "0's" will provide a sample pulse signal equal to $\frac{1}{3}$ where the maximum signal amplitude of the waveform is considered normalized to "1." This situation represents the worst case (largest amplitude) that pertains to the detection of a "0" among all possible binary patterns. Then recalling that the pulse sequence must alternate, consider the central bit in an adjacent group of 3 "1"'s surrounded by zeros. The pulses corresponding to the outer "1's" then subtract from the central pulse. Now at the density $1/\rho$ the signal level at sample time for the central bit is equal to $1-2(\frac{1}{3})=\frac{1}{3}$. This particular binary pattern again corresponds to the worst case for the detection of a "1."

Thus, at a density equal to $1/\rho$ we are at the limit of amplitude discrimination detection and hence $1/\rho$ is the maximum possible density that could be expected with amplitude sensing. For example, for a triangular pulse of base width equal to λ,

$$\rho = \lambda/3 \tag{2}$$

or the maximum theoretical storage density is equal to

$$(bpi)_{\max} = 3/\lambda. \tag{3}$$

For this characteristic pulse model the limiting bit density with amplitude sensing is equal to the magnetization alternation density at which the roll-off curve (output amplitude vs magnetization alternation density) has dropped to $\frac{1}{3}$ of the maximum signal. The limitation here arises specifically from pulse crowding and sensing is predicated on the acceptance of considerable intersymbol interference.

Now in actual practice one must contend with considerable departures from this "first-order" model. Then the computer program outlined below provides a flexible means to attack the general detection question with a high level of sophistication.

Upon readback, with amplitude detection, the signal waveform is strobed at the center of each bit cell (external clocking is assumed) and the sample value is compared with a preset discrimination level. For this work the strobe width is kept at $\frac{1}{5}$ of the *bit interval*. If the magnitude of the strobed signal sample is greater than this discrimination level, the sensing decision logic establishes the bit as a "1;" if the signal amplitude is less than this threshold level, a "0." The simulation program incorporates the requirement that the readback waveform sample exceed the "1" sense level for the full width of the strobe before the presence of a "1" is indicated. This serves as a criterion to provide for a reliability in actual circuit implementation.

There are limits at any given bit density between which this discrimination level must be set to allow the proper identification of each strobed sample. If this level is below an established lower limit, some "0's" will be interpreted as "1's;" if it is above an upper limit, some "1's" will be detected as "0's." As the program considers "cell" signal waveforms arising from all possible patterns produced by varying the states of the 3 adjacent bit intervals on each side of the test bit, the determination of the upper and lower sensing level limits at any density involves the examination of all possible seven-bit code patterns.

With the center bit assumed written as a "1" the strobed signal amplitudes of this cell are used to determine the upper sensing level limit; if this test bit is a "0," the strobe samples are used to determine the lower amplitude threshold limit. Thus, for a given density, the upper limit would be the lowest-amplitude "1" signal obtained while the lower limit is equal to the maximum-amplitude strobed "0" signal. Fig. 2 shows the curves

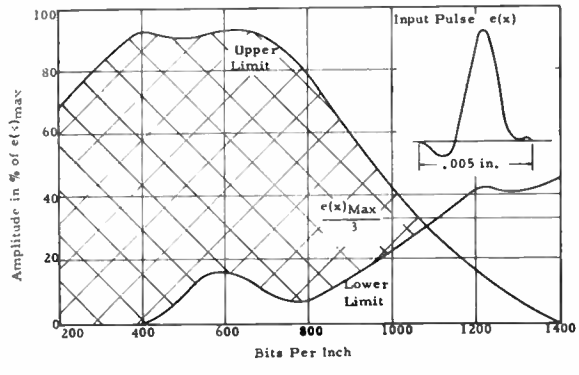


Fig. 2—Amplitude sensing level limit curves.

displaying these limits as a function of bit density with the characteristic pulse from which these curves were constructed. The crosshatched area shows the region in which the amplitude sensing level must be placed for error-free detection. Obviously, this recording system would start to give errors with some patterns at 1075 bits per inch, at which point the sensing level limits intersect. A reduction in density below this figure (down to about 700 bpi) will permit an increasingly greater tolerance for variation in the sense level setting. One can note the effect of the overshoot and the asymmetry

of this particular characteristic pulse on the sensing level limit curves (as well as on the patterns that caused the amplitude threshold limits at various densities). These limiting patterns are tabulated in Table 1. In particular, note in Fig. 2 the rises in the lower sense limit at 600 and 1200 bpi due to the presence of pulses (which, again, possess overshoot) in the adjacent cells. The fall in the upper sensing level limit at low bit densities is due to the strobe intersecting the characteristic pulse away from its peak, since the strobe width is related to the bit interval rather than the pulse width.

This basic waveform synthesis and detection routine may now be extended by any further reading logic that one may wish to apply to the basic detection scheme, *i.e.*, logical correction,[2] self-clocking,[3] etc. In addition, the NRZI coding scheme may be modified to represent a phase modulation scheme.[4] Here NRZ type recording is assumed with a positive pulse representing a "0" and a negative pulse representing a "1," as shown in Fig. 3. If two or more "1's" are to be written consecutively, the inherent alternating characters of the magnetization results in a signal output pulse of opposite polarity between the resulting "1" pulses. These "extraneous" pulses need not be sampled as they contain no new information, but nevertheless they will cause greater pulse crowding at any particular density and thus modify the strobed signal values. The same statements apply to a sequence of "0's."

The computer program allows a rapid comparison of the relative advantages of the NRZ and phase modulation schemes. Intuitively one sees that with phase modulation only the polarity of the sampled waveform need be considered; thus, the lower sense level limit is "0." Using the same characteristic pulse as in Fig. 2, the upper sense level limit as a function of bit (not pulse) density is shown in Fig. 4. The difference of the sense level limits of the NRZ scheme of Fig. 3 is plotted along with this, as this is an analogous measure of the signal amplitude tolerance of the sensing level setting. As might be expected, the phase modulation curve falls off at just over half the density given by the NRZ difference curve. In other words, the fact that the lower sense level can be near "0" does not compensate for the increased pulse crowding. This comparison does not, of course, take account of possible advantages of the redundant pulses for error detection or self clocking.

Further extensions of the basic amplitude sensing routine and uses of the sensing level limit curves will be shown later. In order to make subsequent relative comparisons of the influence of parameter variation on both amplitude and peak detection techniques, the peak sensing simulation program will first be described.

TABLE 1
TEST PATTERNS THAT CAUSED THE SENSING LEVEL LIMITS OF FIG. 2

Bit Density (bpi)	Upper Pattern Test Position ↓	Lower Pattern Test Position ↓
300	0001000	1110111
450	0011000	0010100
600	0011000	0010100
750	0111110	0110010
900	0111110	1010010
1050	1011110	1000110

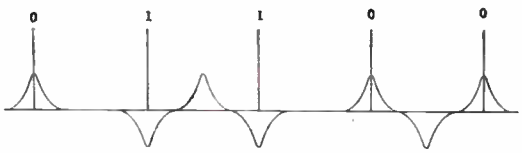


Fig. 3—Phase modulation readback signal (low density).

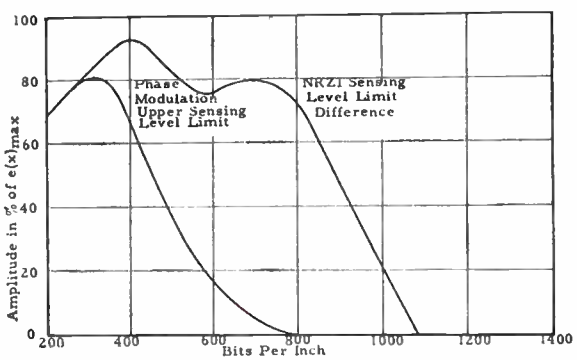


Fig. 4—NRZI amplitude and phase modulation comparison.

PEAK SENSING

The recorded step response typically results in an output pulse with a very high degree of symmetry about the peak. Then the peak, being centrally located, possesses the greatest degree of isolation (among all the sections comprising the waveform) with respect to intersymbol interference. Therefore the technique which intuitively seems obvious as a means to extend density in the face of pulse crowding is peak sensing. Inherently this method provides insensitivity to amplitude variation since it does not directly exploit this waveform feature.

In peak sensing, the detection problems are somewhat different as it is necessary to determine if a signal peak[5] of proper character occurred within a prescribed bit interval. Thus the readback waveform must be examined throughout the entire bit interval for the presence of such a signal peak.

Specific knowledge of the character of the actual in-

[2] A. S. Hoagland, "A logical reading system for nonreturn-to-zero magnetic recording," IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-4, pp. 93–95; September, 1955.
[3] L. D. Seader, "A self-clocking system for information transfer," *IBM J. Res. Dev.*, vol. 1, pp. 181–184; April, 1957.
[4] F. C. Williams, T. Kilburn, and G. B. Thomas, "Universal high-speed digital computers: a magnetic store," *Proc. IEE*, pt. 2, vol. 99, pp. 94–106; April, 1952.
[5] More precisely, points where the derivative of the signal changes sign.

tended peak detector is required to meaningfully simulate this detection method. In practice, it would be undesirable to have a detector that would respond to every signal peak of the readback waveform, as the system would then be susceptible to all noise peaks and baseline ripple. In the work presented here, the detector represented in Fig. 5 was simulated. The low-pass filter network is merely for impulse-type noise elimination and does not cut off any significant part of the signal frequency spectrum. Hence, it is not involved in the detection simulation program since such noise is not generated and inserted in the computer signal waveform synthesis. The specific detector circuit treated requires that the computer program output representing the simulated differentiator *change polarity* and achieve a certain minimum magnitude before indicating the existence of a peak, as shown in Fig. 5.

From the discussion of the computer simulation of amplitude sensing, it is easy to see how the same general procedure applies here. All possible seven bit patterns are again generated and the waveform in the center bit cell is examined for the above characteristics of detectability. As an "acceptable" peak is located, its spatial position within the bit cell is recorded as an output along with the associated bit pattern and bit density. If a signal peak should have been located in a bit cell but no peak is detected, or vice versa, a failure indication is noted.

If the system is externally clocked (*i.e.*, if the bounds of the bit interval are defined independently of the recorded information) the above type of failure completely determines the upper bit density limit. However, if due to timing variations self-clocking must be employed, a somewhat modified failure criterion must be used. Fig. 6 shows the type of self-clocking used in which the clock is rephased each time a peak is detected. If, as previously defined, the bit interval is h (*i.e.*, the maximum clock rate $= 1/h$), an error will occur for two successive "1's" written mh apart (m is an integer) if the distance between the two resulting readback peaks, d_m, is not within the range

$$(m - \tfrac{1}{2})h < d_m < (m + \tfrac{1}{2})h. \qquad (4)$$

("0" peak shift is understood to imply $d_m = mh$). If the lower limit is exceeded, a "0" will be omitted in the readback binary pattern while a peak separation greater than the given upper limit will cause an extra "0" to be inserted in the decoded information.

It is now a relatively simple matter to scan the output list of peak locations within the test bit cell at a given density and determine the maximum magnitude of peak shift. Since the concern about peak shift with self-clocking relates to the relative separation between *successive pulses* it is necessary to determine the net shift by considering the effect on each pulse (treated as the test cell) within the context of the same code pattern. It became readily apparent that for a great variety of pulses

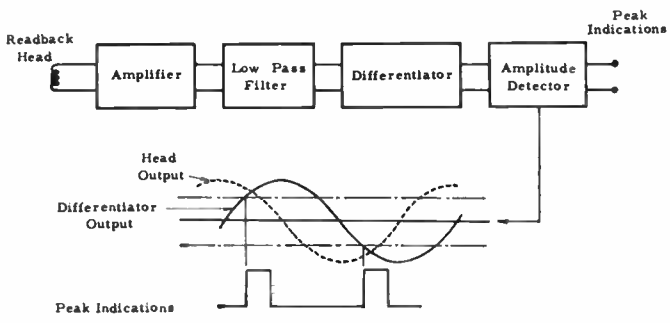


Fig. 5—Block diagram of peak detector.

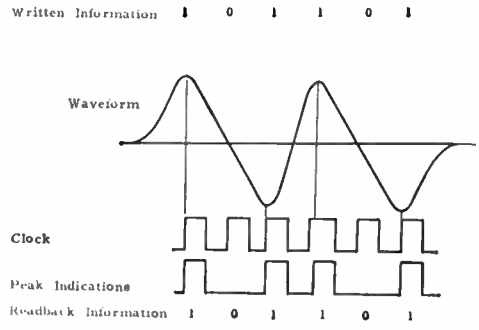


Fig. 6—Self-clocking logic.

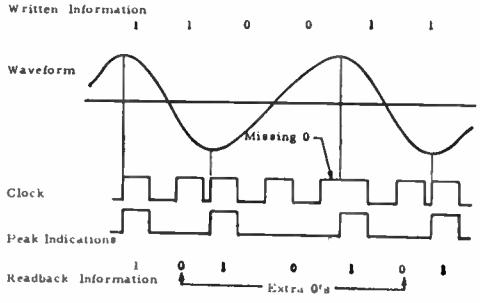


Fig. 7—Self-clocking failure situation.

with little or no overshoot[6] one particular pattern configuration always gave a failure as early, if not earlier, than any others. Fig. 7 shows this pattern and two ways that it may cause an error. In both cases the readback failure is caused by the shift of the readback peaks of two adjacent ones surrounded by "0's".

One might initially suppose that a possible way to circumvent this problem and hence have a means to obtain a higher density would be to deliberately write the two "1's" (*i.e.*, current reversals) closer together than the reference clock period, since this worst case can be recognized prior to recording. Experiment and graphical superposition show that this concept is not fruitful. Typically, a curve like that of Fig. 8 is obtained. For a bit interval greater than h_0 (see Fig. 8) there is negligible

[6] In general, characteristic pulses with significant overshoot cannot be used in a peak sensing system. If the detector indicates a peak when reading the overshoot, the system will automatically fail. For high-density recording, the detector would need sufficient dynamic range to sense all but the smallest "unwanted peaks."

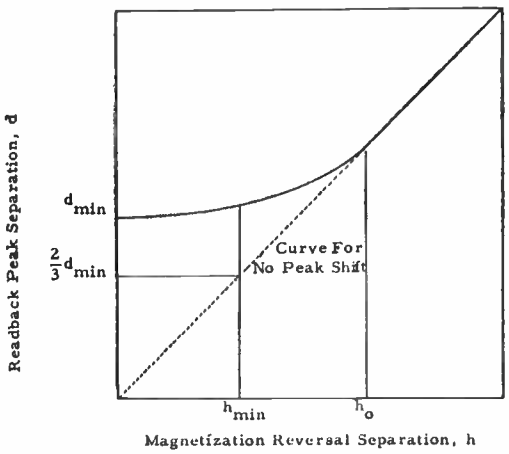


Fig. 8—Peak shift vs h for 00011000 pattern, where bpi $= 1/h$.

peak shift. However, as h is reduced (increasing the bit density) the peak separation rapidly approaches a fixed value d_{min}. In fact, from (4),

$$h_{min} = \left(\frac{1}{1.5}\right) d_{min} = \left(\frac{2}{3}\right) d_{min}. \qquad (5)$$

Recall that $\text{bpi}_{max} = (h_{min})^{-1}$ so that $(\text{bpi})_{max} = 1.5/d_{min}$. Predictated on the superposition concept, d_{min} can be readily interpreted as follows. Note that the readback waveform representing two successive "1's" is obtained from the subtraction of the characteristic pulse, shifted by the distance h, from itself. In effect, one is approximating differentiation of the characteristic pulse through taking finite differences with interval h. In the limit as h goes to 0, then the peaks of the readback waveform approach a separation equal to the distance between the steepest slopes of the characteristic pulse, *i.e.*, the separation of the dipulse peaks of $\dot{e}(x)$, where $\dot{e}(x) = de(x)/dx$. To minimize peak shift, these inflection points should be as near each other as possible; or in general one would like to have cusp-shaped characteristic pulses to complement most fully a peak sensing detection system.

A convenient way of representing the peak sensing density resolution allowed by a given characteristic pulse is to plot the percentage peak shift, $100\ (d_i - h)/h$ (where d_i is the peak separation arising from two adjacent ones), against bit density for the worst-case pattern group. This can be done quite rapidly by the computer. If the characteristics of the peak sensing circuit are reasonably simple, this is easily done graphically. Fig. 9 shows a characteristic pulse and the curve that results. On this same plot is shown a curve that was experimentally obtained from the recording unit that provided this characteristic pulse. The agreement between these two curves again confirms the engineering validity of the superposition approach to recording techniques analysis.

Consider the relative timing aspects of self- and externally-clocked systems that use peak sensing. With external clocking a peak may be anywhere within its appropriate bit interval. Thus for the worst case situation cited above, the peaks could be separated a maximum distance of 2 bit cells, while with self-clocking 1.5 bit intervals is the maximum separation that can be tolerated. Thus if the accuracy of the external clocking is perfect, self-clocking decreases the bit density potential by a factor of $\frac{3}{4}$. It is of interest to note that for an idealized triangular pulse it can be analytically shown (with self-clocking restrictions) that the limiting density due to peak shift is $3/\lambda$, or the same as obtained for this idealized pulse with externally clocked amplitude detection. This fact will point up the significance of considering operating factors (see below) in order properly to get an evaluation of detection methods.

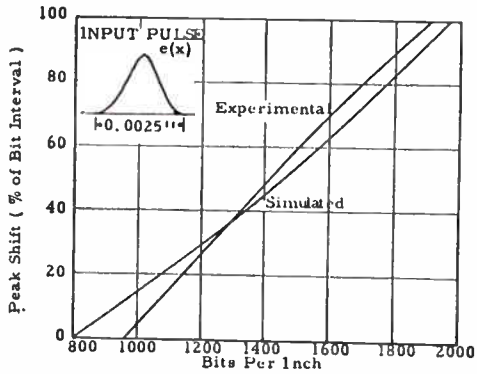


Fig. 9—Peak shift vs bit density.

Operational Considerations

The amplitude and peak sensing simulation procedures that have been described are basic tools whose extension to demonstrate the introduction of practical operating factors and parameter variations into a recording system analysis will now be described. As the over-all goal is the optimization of a recording system the limitations imposed by these factors must be understood.

Amplitude Perturbations

Most applications here of the computer programs exploit the linear characteristic of the readback model. For example, if the amplitude of the characteristic pulse is changed, the sensing level curves of Fig. 2 will be scaled by the same factor. This has direct application with amplitude sensing in the specification of manufacturing tolerances for the output of heads used in a memory where a group will feed the same detector, such as the heads of a drum that are individually selected and connected to a common read amplifier by some switching network. If the assumption is made that the characteristic pulse waveform of each head differs from any other only by a constant scaling factor, then each head will have sensing level limit curves that differ from those of the others by this scale factor. The object is now to determine the two composite sensing level limit curves as these alone are relevant to the single detector. The composite curves wanted are, of course, the highest

lower limit curve and the lowest upper limit curve. Assume that the curves of Fig. 2 correspond to the head with the highest signal output. Then the lower limit curve here will be the lower limit curve of the composite set. The upper limit curve is that associated with the head of lowest output voltage. If, for a margin of reliability, we demand that the composite sensing level limit curves provide a threshold detection level range of at least 25 per cent of e_{max} at the operating density, the ratio of allowable head output variation may be obtained. That is, we can find the factor that must multiply the upper sensing level limit curve of Fig. 2 to cause the difference between the composite sensing level limits to be 25 per cent of e_{max} (at the selected operating density). If we record at a density of 800 bpi, using Fig. 2, this factor may be shown to be 0.41. Any lower ratio of lowest to highest head output would cause the sensing level limit difference to be less than 25 per cent of e_{max}. It should be noted that this same analysis can be used to determine the effects of small head-to-surface variations in which only the amplitude and not the general shape of the characteristic signal pulse is changed.

A problem very similar to the above arises when considering positioning tolerances for an access mechanism that moves a single magnetic head to cover a multiplicity of tracks (again assuming amplitude detection). As a head gives an output proportional to the width of the track that it is reading, any movement off-track gives a proportional decrease in the output from that track. Using this relation it is possible to show how the sensing level limit curves are modified as a function of the maximum access positioning error $2P$. In Fig. 10 it may be

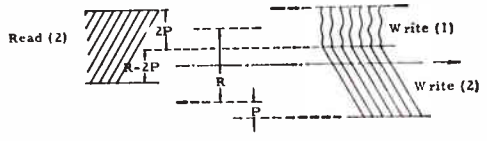


Fig. 10—Track misregistration problem.

seen how the "worst case" situation arises. The head of track width R first writes at a distance P to the right of a reference or true track centerline. The head is now considered on a later access motion to be located at a distance P to the left of this reference axis and new information recorded on the track. The worst case arises when the head is repositioned to read this track again but is assumed located off-track to the right again by the maximum distance P from the centerline. Here the smallest width of the desired (most recently written) information and the greatest width of the undesired or outdated information is read. The sensing level limit difference Δ will now be lowered by two factors. First Δ is reduced by the ratio of the last recorded path width (that is actually being covered by the head) to the head width. As is seen in Fig. 10, this fraction is $R-2P/R$. At the same time an uncrowded output pulse from the outdated recorded path provides the greatest potential additional decrease of Δ. The worst case corresponds to a pulse being previously recorded at the same track cell as the test bit but of the opposite polarity. Let the maximum upper sensing level limit of a single characteristic pulse be C (recall that the sense level limit is based on a finite width strobe). Then for the above worst case the upper sensing level limit will be reduced by a term equal to $(2P/R)C$ due to this factor. Likewise the lower sensing level limit can be increased by $(2P/R)C$ under worst case conditions. The expression for the resultant minimum difference $\bar{\Delta}$ may be written

$$\bar{\Delta} = \Delta \frac{(R - 2P)}{R} - \left|\frac{4P}{R}\right| C. \tag{6}$$

Of, if $\bar{\Delta}$ is specified, the maximum positioning error may be determined, *i.e.*,

$$P = \frac{R(\Delta - \bar{\Delta})}{2\Delta + 4C}. \tag{7}$$

Assume that we are using the recording system characterized by Fig. 2 and that a minimum $\bar{\Delta}$ of 25 per cent of e_{max} is required. If we are operating at 800 bpi, it is seen that Δ is 70 per cent and C is 90 per cent of the characteristic pulse peak. Eq. (6) then gives a maximum tolerable positioning error of $0.09R$.

As $C \geqq \Delta$, the maximum permissible value for P is obtained when $C=\Delta$ and $\bar{\Delta}=0$, *i.e.*,

$$P_{max} = \frac{R\Delta}{2\Delta + 4\Delta} = \frac{R}{6} = 0.167R. \tag{8}$$

Thus the allowable value of $0.09R$, while small, is not too far from the maximum positioning tolerance value.

In general, if there is an unwanted signal of a type that adds linearly to the readback waveform it may be dealt with in an analogous manner. Many times the worst case situations of the composite signal are obvious and through manipulations as simple as those above, direct evaluations may be made. If this is not the case it is still reasonably easy to have the computer automatically test all pertinent cases.

When peak sensing is to be employed, unwanted signals of the type described above pose a different problem. If the unwanted signal, by itself, will cause the detector to indicate a peak, then a detection failure will certainly result. The effects of any lesser disturbing noise signal must be superimposed on the signal waveform and the composite waveform examined. It is usually a computer problem to find worst cases as the resultant waveform must be examined in more detail than is the case with amplitude sensing. In a system in which the main perturbation is a variation in the readback waveform amplitude, peak sensing performance is only slightly affected, as the position of the signal peaks is unchanged. In this respect it is considerably superior to amplitude sensing.

Clock Timing

Another operating condition quite readily handled by the programs is that of clock timing. All systems must tolerate a certain degree of clocking inaccuracy. When an external or fixed clock reference is used, some sacrifice in bit density must be accepted in order to tolerate timing variations; if the timing inaccuracy is potentially extreme, one is forced to employ self-clocking (with a likely restraint on code combinations to maintain proper circuit-surface synchronization).

The peak sensing computer routine is readily adaptable to this problem, since the indicated peak position within the bit interval is the program output. Thus it is simply necessary to determine the amount that the boundaries of the bit cell must be shifted to cause failure in the worst case. One half of this is the maximum allowable clock variation, as the total error has contributions from both reading and writing.

The externally-clocked amplitude sensing case is quite rapidly studied through a slight modification of the sensing level limit program. Again, all seven-bit waveforms are constructed with the clock in the proper position. In the simulation of detection the strobe is moved both to the right and to the left in small increments. At each clock (*i.e.*, strobe) position, the upper and lower sensing level limits are noted, using all possible patterns. From these values composite sensing level limit curves as a function of clock shift are obtained for the density in question, If, for reliability, it is required that the sensing limits be separated by at least 25 per cent of e_{max}, the above curve will establish the maximum allowable clock shift. Using the characteristic pulse of Fig. 2, plots of this maximum allowable shift are shown in Fig. 11, below, for both phase modulation and NRZ

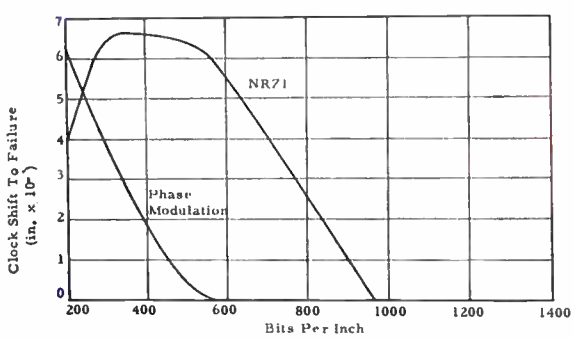


Fig. 11—Clock shift with amplitude detection.

coding. The lower pulse crowding of the NRZ method is seen to be a favorable factor with respect to this problem.

The above applications have dealt with operational effects upon a system with a given characteristic pulse. Now we will look at the characteristic pulse itself to determine how it is related to the recording structure and hence the relation of head design to density.

Head Design

Through a reciprocity argument[1] a relation between $e(\bar{x})$ and $M(x)$ can be derived. In brief, if low-level excitation of the recording head produces a field distribution $H(x)$, then, based on the principle of reciprocity, the layer magnetization $M(x)$ at a depth y in the magnetic surface will produce a reading coil voltage $u(\bar{x})$ where

$$u(\bar{x}) = KvN \int_{-\infty}^{\infty} H(x) \frac{\partial M(x - \bar{x})dx}{\partial \bar{x}} . \qquad (9)$$

Here K is a constant and M and H are vectors combined by a scalar or dot product operation. If a ring-type head (or horizontal recording) is assumed, the significant component of the magnetization is in the x direction. Then, taking $M = M_x$ and for $M_x(x)$ a step function, the derivative of magnetization is an impulse and the above integral yields

$$u(\bar{x}) = u_x(\bar{x}) \propto H_x(\bar{x}); \qquad (10)$$

$u(\bar{x})$, the output signal waveform, is then proportional to $H_x(\bar{x})$.

Eq. (9) may be interpreted as analogous to a "scanning" process in which $H(x)$ is scanned by the distance derivative of the surface magnetization. When $M = M_x$ and demagnetization transition has a finite slope, $H_x(x)$ is scanned by a pulse-like magnetization function of finite width and the resultant $u(x)$ will have a broader and flatter waveform than $H_x(x)$.

For most practical cases, $u(\bar{x})$ closely resembles $H_x(x)$ for a ring head and $u(\bar{x})$ resembles $H_y(x)$ for a vertical probe-type head.[7] Thus, it is useful to have a method for determining $H_x(x)$ and $H_y(x)$ for a given recording environment. A rapid way to get estimates for these sensitivity or weighting functions, *i.e.*, H_x and H_y, is to use an electrolytic tank. Here an analogy is made between permeability and conductivity, and between H and E (electric field). For this purpose, the magnetic head is most easily regarded as possessing an infinite permeability. There is no concern about local saturation effects since this analog is to apply to read-back analysis where very weak fields exist. The head is satisfactorily represented by a highly conducting boundary.

The saturated surface will not have a permeability significantly different from air and both can then be adequately represented by the electrolyte in the tank. Thus, with the simulated head structure electrically excited, $H_x(x)$ and $H_y(x)$ can be found at any corresponding depth y in the "magnetic" surface. The total head "out-signal," $e(\bar{x})$, assuming a step change in M_x, is the contribution from the entire surface, *i.e.*,

$$e(\bar{x}) = \int_{\text{over } d} H_x(x, y)dy. \qquad (11)$$

[7] W. Farrand, "An air-floating disk magnetic memory," 1957 WESCON Convention Record, pt. 4, pp. 227–230.

Here d is the surface thickness. This integral can be approximated by summing the contributions from several depths throughout the surface.

Then the characteristic pulse is determined by the head sensitivity function and the surface magnetization through the integral relation of (9). It is also evident that if the magnetization reversal is essentially step-like, the characteristic pulse very closely resembles the "mean" sensitivity function. This sensitivity function is easily obtained from an electrolytic tank or similar field analog, thus allowing a quick determination of the density limitation implications of a given head design. The above relationship allows one to predict the relative density performance of various head designs before construction is undertaken, thus being a considerable aid in guiding head design efforts.

Of particular interest, the above approach allows a quick relative differentiation between the properties of ring and vertical probe type structures. At the same head-to-surface spacing and with the same magnetic coating thickness, the dimensions of representative head types are chosen to each yield a sensitivity function of approximately basewidth, λ. Two such sensitivity functions for experimentally achievable designs are shown in Fig. 12 along with the corresponding recording geometry. Notice that the vertical probe head yields a sensitivity function with a flatter top and steeper sides than the ring head. This waveform dissimilarity between the ring and probe structures causes a pronounced difference in their sensing level limit and peak shift curves. The sensing level limit curves of Fig. 13 reflect the effects of the average slope of the sides of these readback pulses. When, for the probe head, the upper sensing level limit starts to fall at about 1000 bpi it falls very rapidly as the steep sides of the signal pulse would indicate (and similarly for the rise of the lower sensing level limit). The ring head, however, yields curves that fall off much more slowly and as a result would allow higher recording densities with amplitude detection than this probe head although their pulse widths are the same. The curves of peak shift shown in Fig. 14 demonstrate that peak sensing is even more critically dependent upon characteristic pulse shape. Intuitively, this is substantiated by noting that the much sharper peak of the ring head sensitivity function will be distinguishable under greater pulse crowding than could be expected from the flatter top of the sensitivity function possessed by the probe head.

Surface Magnetization

The effects of a finite slope for the surface magnetization can now be estimated. The integral of (9) was solved graphically for a uniform magnetization reversal of $\lambda/5$ for both the ring and probe head discussed previously. This magnetization transition width places an

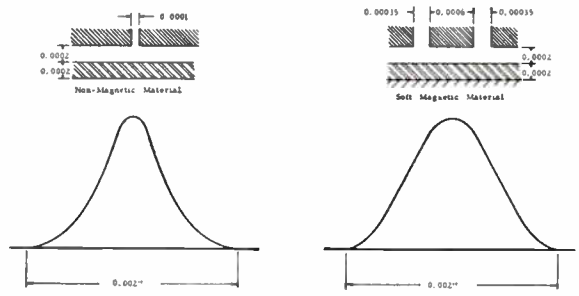


Fig. 12—Sensitivity functions.

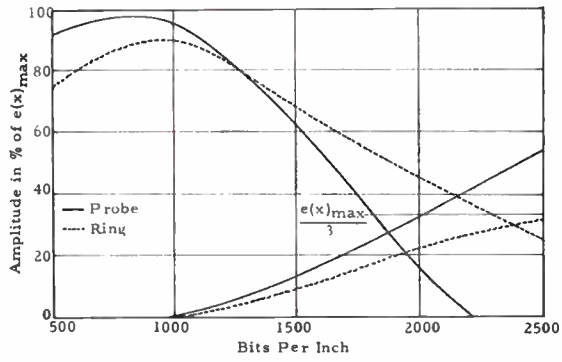


Fig. 13—Amplitude sensing level limit curves.

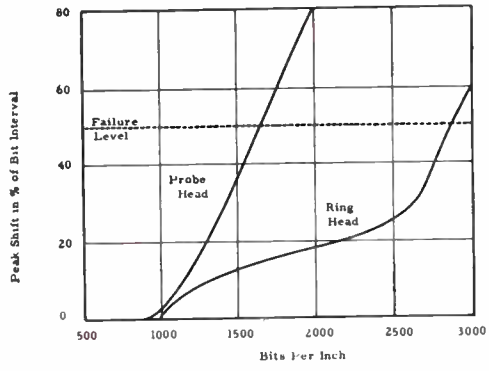


Fig. 14—Ring and probe peak shift characteristics.

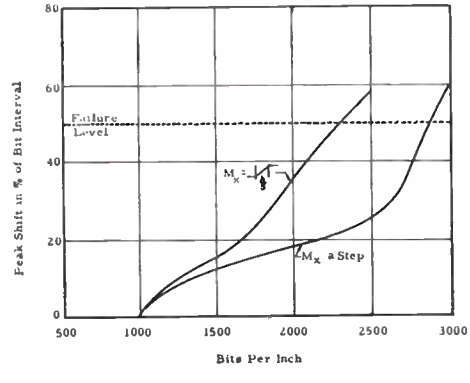


Fig. 15—Effect of M_x upon ring peak shift characteristics.

expected upper bound on the applicability of superposition at $h_{min}=\lambda/5$; for $\lambda=0.002$ inch, the maximum bit density that can be anticipated as susceptible to superposition simulation is 2500 bpi. The results of considering a finite magnetization change were characteristic pulse waveforms with broader bases and flatter peaks than those of the original sensitivity functions, as would be expected. The characteristic pulse of the probe is only very slightly modified, while that of the ring is considerably changed. Neither the sensing level limit curves nor the peak shift curve was perceptably modified for the probe head. Likewise, the sensing level limit curves for the ring head were essentially the same. However, the peak shift of the ring head was considerably increased due mainly to the difference in the shape of the peak of the pulse. This increase in peak shift may be seen in Fig. 15.

Thus when peak sensing is to be used in conjunction with a ring-type head, efforts to obtain a magnetic surface that will sustain a narrower magnetization reversal may be worthwhile, this being indicated by the waveform difference between the characteristic pulse and the sensitivity function. Use of the sensitivity function itself in examining bit density limits corresponds to assuming an ideal surface, since true step changes in magnetization are assumed. Hence, curves obtained in this manner indicate the range of potential gain that may result from improvements in the magnetic surface or in writing for a given detection technique. The data here are for a 200 microinch head-to-surface spacing. Closer spacing would tend to increase the significance of the surface in the over-all recording process.

Conclusions

The purpose of this paper has been to demonstrate the considerable amount of information relative to magnetic recording system performance that can be derived from the utilization of the characteristic pulse waveform. Both theory and experiment have demonstrated that the utilization of the superposition concept is valid beyond the range of recording bit density that is achievable for the detection techniques and head designs here. The waveform superposition synthesis has been advantageously simulated on a digital computer along with detection techniques and operational effects.

It is significant to note that the detection methods studied are very sensitive to the exact shape of the characteristic pulse. The pulse base-width λ is only one parameter characterizing this waveform, and as was shown in the comparison of ring and probe heads, it is not necessarily the most important. It was further shown that these pulse shape factors are more critical in peak sensing than in amplitude sensing. Hence this work has provided a means to interrelate head design and recording techniques to achieve over-all recording system optimization. Further, such analyses have given insight into the role of the magnetic surface in setting performance.

The computer programs will very suitably predict recording system performance, and have greatly reduced exploratory bench work. The study here, while highlighting the nature and features of digital recording is primarily a valuable "tool" since, in itself, the simulation analysis does not directly produce new detection principles.

A New Active-Passive Network Simulator for Transient Field Problems*

WALTER J. KARPLUS†, MEMBER, IRE

Summary—**The computer system described in this paper represents a hydridization of analog and digital techniques. A wide variety of problems characterized by partial differential equations are simulated by means of a network consisting only of positive and negative resistors. No reactors are used, the negative resistors being realized with the aid of dc amplifiers. Unlike conventional analog methods, the time as well as the space variables are approximated by finite-difference expressions; thus the solution proceeds step-wise in time as on a digital computer. Only implicit difference equations are instrumented, so that there is no danger of computational instability no matter how large the time increment. Among the field problems treated by this computer are problems characterized by the diffusion equation, the wave equation, the biharmonic (beam) equation, and various modified forms of these equations.**

THE solution of problems characterized by partial differential equations constitutes a challenge both for the digital and the analog computer. The discrete-space-discrete-time (DSDT) computer described in this paper is the result of a hybridization of analog and digital techniques. It is a general purpose device in that it is designed to be applicable to the simulation of fields governed by a wide variety of partial differential equations occurring in engineering practice, but particularly to those in which the dependent variable varies nonperiodically with time.

Probably the most widely occurring time-dependent partial differential equation is the diffusion equation

$$\nabla^2\phi = K\frac{\partial\phi}{\partial t}, \tag{1}$$

where ϕ is a potential function; for example, the temperature in a transient heat transfer problem, ∇^2 is the Laplacian operator, and K is a field parameter and corresponds to the reciprocal of the thermal-diffusivity in heat transfer problems. If the field is nonuniform, (1) is written as

$$\nabla(\sigma\nabla\phi) = K\frac{\partial\phi}{\partial t}, \tag{2}$$

where σ is a function of the space variables of the problem.

Occasionally, in problems governed by (1), physical mass transfer phenomena are superimposed upon the diffusion process. This is the case in the study of heat transfer in moving liquids, and in the study of the atmospheric diffusion of particles in the presence of winds. Eq. (1) may then be modified according to

$$\nabla^2\phi - u\frac{\partial\phi}{\partial x} - v\frac{\partial\phi}{\partial y} - w\frac{\partial\phi}{\partial z} = K\frac{\partial\phi}{\partial t}, \tag{3}$$

in which u, v, and w represent the transport velocity in the x, y, and z directions, respectively. If sources of energy or excitation are distributed within the field in a continuous manner, as is the case in the study of heat transfer in a nuclear reactor, (1) is modified as

$$\nabla^2\phi = K\frac{\partial\phi}{\partial t} + m, \tag{4}$$

where m may be a function of the space variables, of time, or of the field potential.

A second class of partial differential equations which recur frequently in engineering work is exemplified by the wave equation

$$\nabla^2\phi = K\frac{\partial^2\phi}{\partial t^2}, \tag{5}$$

so that the parameter K is associated with the velocity with which a disturbance is propagated throughout the field. In the presence of dissipation, as well as energy storage, (5) becomes

$$\nabla^2\phi = K_1\frac{\partial^2\phi}{\partial t^2} + K_2\frac{\partial\phi}{\partial t} + K_3\phi, \tag{6}$$

where K_1, K_2, and K_3 are field parameters and may be functions of position.

In the area of structural analysis, the basic equation governing the vibration of elastic members is known as the biharmonic equation

$$\nabla^4\phi = K\frac{\partial^2\phi}{\partial t^2}, \tag{7}$$

where ∇^4 is termed the biharmonic operator.

All the above equations may be formulated in whichever coordinate system appears most suitable to the field geometry, the Cartesian, cylindrical, and spherical coordinate systems being the most widely used. The field simulator described below is capable of handling field problems governed by (1)–(7) in any suitable coordinate system and in as many as three space variables. In order to simplify the explanation of the system operation, the following discussion emphasizes the simulation of problems formulated in one Cartesian dimension

* Received by the IRE, June 7, 1960. A portion of this paper was presented at the Congress of the Internatl. Federation of Automatic Control, Moscow, Russia, July 2, 1960.

† Dept. of Engrg., University of California, Los Angeles.

x. That is,

$$\nabla^2\phi = \frac{\partial^2\phi}{\partial x^2}, \qquad \nabla^4\phi = \frac{\partial^4\phi}{\partial x^4}, \tag{8}$$

The extension of the method of two- and three-dimensional fields is subsequently indicated briefly.

Problems of the type described above are known as "initial value problems." Typically, in problems governed by (1)–(7), the potential along the field boundary, or the potential gradient at the field boundary, is given for all time $t>0$, and the kinetic and/or potential energy stored everywhere within the field at time $t=0$ is specified. In addition, transient excitations may be present within the field or at the field boundaries. The problem is to determine the potentials within the field for times $t>0$.

Presently-Available Techniques for Solving Transient Field Problems

The solution of partial differential equations can be effected by one of two general techniques: analytical or numerical. Analytical methods are generally limited in their application to problems in which the geometry of the field is simple and in which the field parameters are linear and constant in time. For this reason much emphasis has been placed in recent years on automatic computer methods for obtaining numerical solutions. The treatment of field problems by automatic computer techniques is considered in great detail by Karplus[1] and by Richtmyer.[2] These methods can be classified into two broad categories: digital and analog.

In the digital approach, all independent variables of the problem are approximated by finite-difference expressions, and the solution is obtained in a step-wise fashion in the time domain. The manner in which the partial differential equation is approximated has an important consequence. If a so-called explicit approximation is made the calculations required at each time increment are relatively simple, but the difficulty of "computational instability" arises. Unless the time increment is smaller than a critical value, round-off errors made in the course of a calculation will accumulate as the calculation proceeds until the error terms overshadow the solution, making it worthless. Use of explicit approximations, therefore, makes it necessary to use relatively short time increments, which in turn leads to lengthy computer runs. Implicit approximations obviate the instability problem; on the other hand, they make it necessary to solve large sets of simultaneous equations at each step in time. Too often, this leads to uneconomically long solution times, particularly in the case of nonlinear problems.

In conventional analog techniques, only the space variables are approximated by finite-difference expressions. No stability problem exists, and solutions are obtained rapidly. On the other hand, problems with nonlinear and time-varying parameters are very difficult to treat. Furthermore a large assortment of expensive electrical network components, including inductors, capacitors, and transformers, are required for many of the equations mentioned above.

The DSDT computer described in this paper represents a hybridization of analog and digital techniques. Electrical voltages are proportional to field potentials just as in the case of the analog network analyzers, but the time variable, as well as the space variables, is approximated by finite-difference expressions, as in digital computers. Implicit approximations are used exclusively so that no danger of instability exists. At the same time, the network solves the simultaneous equations at each node automatically and instantaneously, so that no cumbersome series of calculations is required. The DSDT computer represents an extension of a method originally suggested by Liebmann.[3] While Liebmann's method was limited to the solution of (1), the DSDT computer can handle *all* of (1)–(7), as well as numerous other modified forms. In addition, the internal circuits of the DSDT computer differ radically from Liebmann's model.

Principle of Operation

The first step in the solution of field problems by the DSDT method is to define a finite-difference grid. For a one-dimensional system, such a grid will have two coordinates: distance x and time t, as shown in Fig. 1. Net

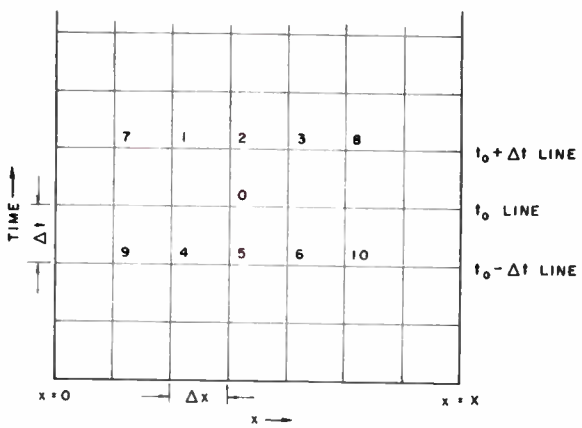


Fig. 1—Finite-difference grid.

intervals Δx and Δt are selected in such a manner that the truncation error resulting from the finite-difference approximation falls within a specified tolerance. In general, the x coordinate will be bounded at $x=0$ and $x=X$, while the t variable will start at 0 and proceed to in-

[1] W. J. Karplus, "Analog Simulation: Solution of Field Problems," McGraw-Hill Book Co., Inc., New York, N. Y., 434 pp.; 1958.

[2] R. D. Richtmyer, "Difference Methods for Initial-Value Problems," Interscience Publishers, Inc., New York, N. Y.; 1957.

[3] G. Liebmann, "A new electrical analog method for the solution of transient heat conductor problems," *Trans. ASME*, vol. 78, pp. 655–665; 1956.

finity. Every point in the finite-difference grid refers to the field potential at some specific x and at some specific instant of time.

A typical point within the finite-difference grid is now selected arbitrarily and denoted by the subscript 0. The field potentials occurring at this point and neighboring points at a time Δt *later* than t_0 are denoted by subscripts 1, 2, 3, 7 and 8, while the field potentials at the point in question and at neighboring points which occurred at a time Δt *earlier* than t_0 are denoted by 4, 5, 6, 9, and 10. To obtain the finite-difference expression, the partial derivatives of (1)–(7) are expressed in terms of the potentials at points 0 through 10. Not all these points are required for all the equations. For example, the diffusion equation (1) requires only points 0 through 3; the wave equation (5) requires points 0 through 6; only the biharmonic equation, (7), require all 11 points.

Diffusion Equation

In problems governed by the diffusion equation, one initial condition is required for each point in the field. Typically, then, we are given the field potentials at a time t_0 and are asked to determine the potentials at time $t_0+\Delta t$. Referring to the coordinate grid shown in Fig. 1, the two partial derivatives in (1) may be approximated by

$$\frac{\partial^2\phi}{\partial x^2} \cong \frac{\phi_1+\phi_3-2\phi_2}{\Delta x^2} = \frac{1}{\Delta x^2}((\phi_1-\phi_0)+(\phi_3-\phi_0)-2(\phi_2-\phi_0)),$$

$$\frac{\partial\phi}{\partial t} \cong \frac{\phi_2-\phi_0}{\Delta t}, \tag{9}$$

so that the finite-difference approximation for the one-dimensional diffusion equation becomes

$$\frac{\partial^2\phi}{\partial x^2}-K\frac{\partial\phi}{\partial t} = \frac{\phi_1-\phi_0}{\Delta x^2}-2\left(\frac{\phi_2-\phi_0}{\Delta x^2}\right)+\frac{\phi_3-\phi_0}{\Delta x^2}-\frac{K}{\Delta t}(\phi_2-\phi_0)=0$$

$$\cong \frac{\phi_1-\phi_0}{\Delta x^2}-\left[\frac{2}{\Delta x^2}+\frac{K}{\Delta t}\right](\phi_2-\phi_0)+\frac{\phi_3-\phi_0}{\Delta x^2}=0. \tag{10}$$

In this equation, the potential ϕ_0, corresponding to the field potential at time t_0, is known, while the potentials ϕ_1, ϕ_2, and ϕ_3 are to be determined. Eq. (10) is therefore an implicit equation and, as shown by Karplus,[1] is stable for all values of Δt.

In order to design the analog circuit, we regard each of the potentials ϕ in (10) as an electrical voltage; (10) then has the form of a Kirchhoff current law equation, and the coefficient of each term is identified as an electrical conductor. The electrical circuit for which (10) is a current law equation is shown in Fig. 2. Note that two of the resistors are positive, while the sign of one of the resistors is negative.

Fig. 2 represents the circuit for a typical node. To solve a one-dimensional field problem, such a circuit must be constructed for each field point along the x coordinate, and these circuits suitably interconnected. A portion of such a circuit is shown in Fig. 3. Variable dc sources are attached to each node in the $(t_0+\Delta t)$ line. These feed-in voltage supplies are adjusted such that each of the nodes in line t_0 assumes the potentials specified for them. The magnitudes of the feed-in sources in line $(t_0+\Delta t)$ are then recorded and correspond to the field potentials at time $(t_0+\Delta t)$. These values now become initial conditions for the next time increment, and the feed-in supplies are all readjusted in such a manner that the node potentials in line t_0 assume the values measured in line $(t_0+\Delta t)$ during the preceding time interval. The voltages now appearing at the feed-in voltage supplies are the field potentials at time $(t_0+2\Delta t)$. These values now become the initial conditions for the next time increment. The process is repeated until the desired time interval has been traversed.

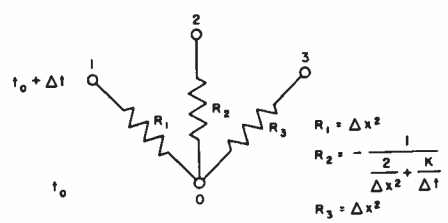


Fig. 2—Typical node for diffusion equation.

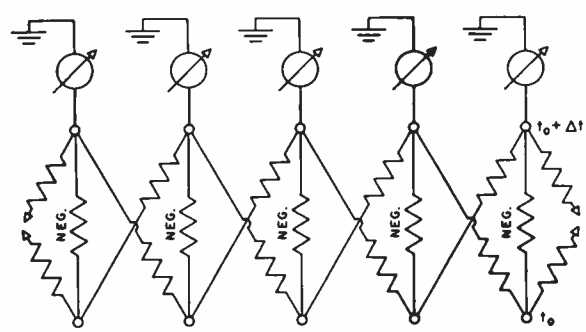


Fig. 3—Portion of network analog for diffusion equation.

Clearly, an adjustment of any one of the feed-in voltage supplies affects to some extent the potential at every network node. Were it necessary to perform this adjustment sequentially and manually, an iterative method would have to be employed, and the adjustments could become very time-consuming. As described in the next section, active circuits are employed to effect this adjustment automatically and instantaneously, so that all voltage supplies assume their correct values at once, and no trial-and-error adjusting is necessary.

The use of the above method makes it possible to simulate moving coordinate problems governed by (3). In approximating that equation by finite-difference expressions and regarding the finite-difference equation as an electrical node equation, we find that the electrical resistors in the forward and backward directions must be given different magnitudes. Such problems cannot be handled by Liebmann's method[3] without the use of inconvenient multiplication factors. Using the DSDT computer, it is only necessary to give the resistors R_1 and R_2 in Fig. 2 different magnitudes. This is possible because separate resistors are used at each node as forward and backward resistances in the x direction.

Wave Equation

In problems governed by (5) and (6), the potential and the first derivative of the potential are specified as initial conditions for the problem. These two values determine, in effect, approximately the value of the potential everywhere within the field at a time Δt after the initial instant. With reference to the finite-difference grid shown in Fig. 1, the potentials at line $(t_0-\Delta t)$ and at line t_0 are known, and the potentials in line $(t_0+\Delta t)$ are to be determined. To obtain an *unconditionally stable implicit approximation* of (5), the second space derivative at grid point 0 is approximated by taking the second derivative at point 2 and point 5, and by averaging the two values:

$$\left.\frac{\partial^2\phi}{\partial x^2}\right|_2 \cong \frac{\phi_1-\phi_2}{\Delta x^2}+\frac{\phi_3-\phi_2}{\Delta x^2}$$

$$=\frac{\phi_1-\phi_0}{\Delta x^2}-2\frac{\phi_2-\phi_0}{\Delta x^2}+\frac{\phi_3-\phi_0}{\Delta x^2},$$

$$\left.\frac{\partial^2\phi}{\partial x^2}\right|_5 \cong \frac{\phi_4-\phi_5}{\Delta x^2}+\frac{\phi_6-\phi_5}{\Delta x^2}$$

$$=\frac{\phi_4-\phi_0}{\Delta x^2}-2\frac{\phi_5-\phi_0}{\Delta x^2}+\frac{\phi_6-\phi_0}{\Delta x^2}; \quad (11)$$

$$\left.\frac{\partial^2\phi}{\partial x^2}\right|_0 \cong \frac{1}{2}\left[\left.\frac{\partial^2\phi}{\partial x^2}\right|_2+\left.\frac{\partial^2\phi}{\partial x^2}\right|_5\right]$$

$$\cong \frac{\phi_1-\phi_0}{2\Delta x^2}-\frac{\phi_2-\phi_0}{\Delta x^2}+\frac{\phi_3-\phi_0}{\Delta x^2}$$

$$+\frac{\phi_4-\phi_0}{2\Delta x^2}-\frac{\phi_5-\phi_0}{\Delta x^2}+\frac{\phi_6-\phi_0}{2\Delta x^2}.$$

The time derivative is approximated as

$$\left.\frac{\partial^2\phi}{\partial t^2}\right|_0 \cong \frac{\phi_2-\phi_0}{\Delta t^2}+\frac{\phi_5-\phi_0}{\Delta t^2}. \quad (12)$$

The over-all approximation for the wave equation, upon rearrangement, becomes

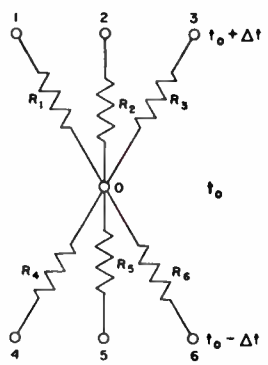
$$\frac{\partial^2\phi}{\partial x^2}-K\frac{\partial^2\phi}{\partial t^2}$$

$$\cong \frac{\phi_1-\phi_0}{2\Delta x^2}-\left(\frac{1}{\Delta x^2}+\frac{K}{\Delta t^2}\right)(\phi_2-\phi_0)+\frac{\phi_3-\phi_0}{2\Delta x^2}$$

$$+\frac{\phi_4-\phi_0}{2\Delta x^2}-\left(\frac{1}{\Delta x^2}+\frac{K}{\Delta t^2}\right)(\phi_5-\phi_0)$$

$$+\frac{\phi_6-\phi_0}{2\Delta x^2}=0. \quad (13)$$

Eq. (13) is regarded as a current law equation pertinent to node 0, with adjacent nodes 1 through 6; the electric analog circuits for the typical node is then of the form shown in Fig. 4. Note that the circuit in this case includes two negative resistors, R_2 and R_5. If the typical node circuits corresponding to each node along the x coordinate are interconnected with adjacent node circuits, the one-dimensional analog circuit shown in Fig. 5 results. Note that two variable dc voltage sources act as feed-in supplies at each node.



$R_1 = R_3 = R_4 = R_6 = \Delta x^2$

$R_2 = R_5 = -(\Delta t^2\Delta x^2)/(2K\Delta x^2+2\Delta t^2)$

Fig. 4—Typical node for wave equation.

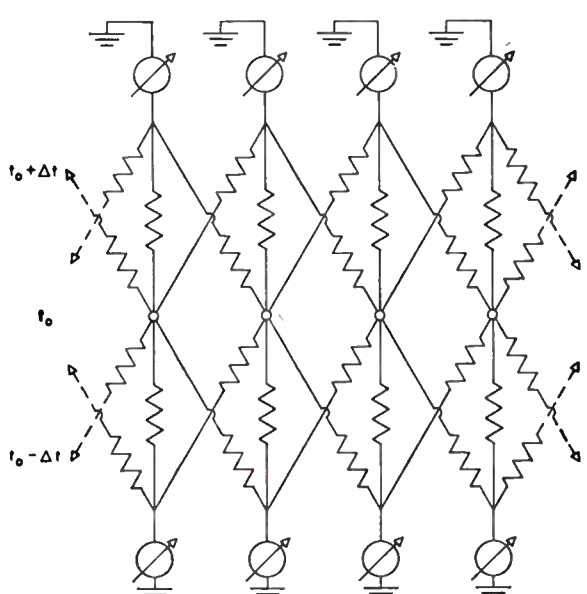


Fig. 5—Portion of network analog for wave equation.

The feed-in voltage supplies energizing the network nodes in line $(t_0-\Delta t)$ are adjusted to the values specified for these potentials. The variable voltage supplies attached to the nodes in line $(t_0+\Delta t)$ are then adjusted until the node potentials in line t_0 assume the magnitudes specified for them. The node voltages in line $(t_0+\Delta t)$ now represent the solution to that step in the problem, *i.e.*, the field potentials at time $(t_0+\Delta t)$. For the next time interval, the potentials now existing in line $(t_0+\Delta t)$ and line t_0 become the initial conditions of the problem; that is, the feed-in voltage supplies in line $(t_0-\Delta t)$ are now given values corresponding to the potentials existing during the preceding measuring interval in line t_0; similarly, the voltage supplies in line $(t_0+\Delta t)$ are readjusted until the node potentials measured in line t_0 assume a value corresponding to the potentials that existed in line $(t_0+\Delta t)$ during the preceding measuring interval. The potentials now existing in the upper line $(t_0+\Delta t)$ correspond to the field potentials at a time $(t_0+2\Delta t)$. These values are recorded and the procedures repeated again and again until a sufficiently large time period has been traversed.

As in the case of the diffusion equation, it is apparent that were it necessary to perform the adjustments of the feed-in voltage supplies in line $(t_0+\Delta t)$ manually and sequentially, the adjustment process might well become inconveniently time-consuming. The electronic analog computer circuit described in the next section performs this adjustment automatically and instantaneously, so that all feed-in voltage supplies assume their correct values at once. As in the case of the diffusion equation, the specified boundary potentials, which may be transients, are applied by separate voltage supplies to those nodes which are immediately adjacent to the field boundaries.

Biharmonic Equation

The treatment of the biharmonic equation (7) is quite similar to the treatment of the wave equation described above. In this case, it is the fourth derivative of ϕ with respect to x which is approximated at lines $(t_0+\Delta t)$ and $(t_0-\Delta t)$, and averaged to provide the fourth space derivative at node 0. The second time derivative is obtained exactly as before; therefore,

$$\left.\frac{\partial^4\phi}{\partial x^4}\right|_2 \cong \frac{1}{\Delta x^4}[\phi_7 - 4\phi_1 + 6\phi_2 - 4\phi_3 + \phi_8],$$

$$\left.\frac{\partial^4\phi}{\partial x^4}\right|_5 \cong \frac{1}{\Delta x^4}[\phi_9 - 4\phi_4 + 6\phi_5 - 4\phi_6 + \phi_{10}],$$

$$\left.\frac{\partial^4\phi}{\partial x^4}\right|_0 \cong \frac{1}{2\Delta x^4}[-4(\phi_1-\phi_0) + 6(\phi_2-\phi_0) - 4(\phi_3-\phi_0) - 4(\phi_4-\phi_0) + 6(\phi_5-\phi_0) - 4(\phi_6-\phi_0) + (\phi_7-\phi_0) + (\phi_8-\phi_0) + (\phi_9-\phi_0) + (\phi_{10}-\phi_0)],$$

$$\left.\frac{\partial^2\phi}{\partial t^2}\right|_0 \cong \frac{\phi_2-\phi_0}{\Delta t^2} + \frac{\phi_5-\phi_0}{\Delta t^2}, \qquad (14)$$

so that the finite-difference approximation of (8) becomes

$$\frac{\partial^4\phi}{\partial x^4} - K\frac{\partial^2\phi}{\partial t^2} \cong -\frac{2}{\Delta x^4}(\phi_1+\phi_0) + \left[\frac{3}{\Delta x^4} - \frac{K}{\Delta t^2}\right](\phi_2-\phi_0) - \frac{2}{\Delta x^4}(\phi_3-\phi_0) - \frac{2}{\Delta x^4}(\phi_4-\phi_0) + \left[\frac{3}{\Delta x^4} - \frac{K}{\Delta t^2}\right](\phi_5-\phi_0) - \frac{2}{\Delta x^4}(\phi_6-\phi_0) + \frac{2}{2\Delta x^4}(\phi_7-\phi_0) + \frac{1}{2\Delta x^4}(\phi_8-\phi_0) + \frac{1}{2\Delta x^4}(\phi_9-\phi_0) + \frac{1}{2\Delta x^4}(\phi_{10}-\phi_0) = 0. \qquad (15)$$

This is again an implicit formulation which is *unconditionally stable* for all values of Δt. A typical node whose current law equation has the same form as (15) is shown in Fig. 6. A portion of a one-dimensional simulating circuit for (7) is shown in Fig. 7.

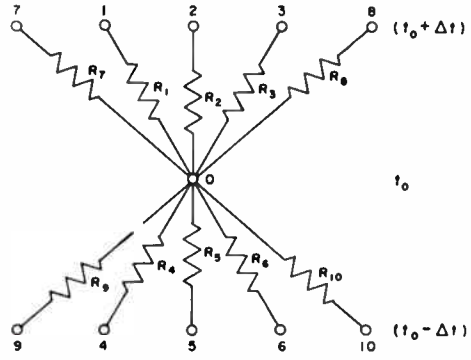


Fig. 6—Typical node for biharmonic equation.

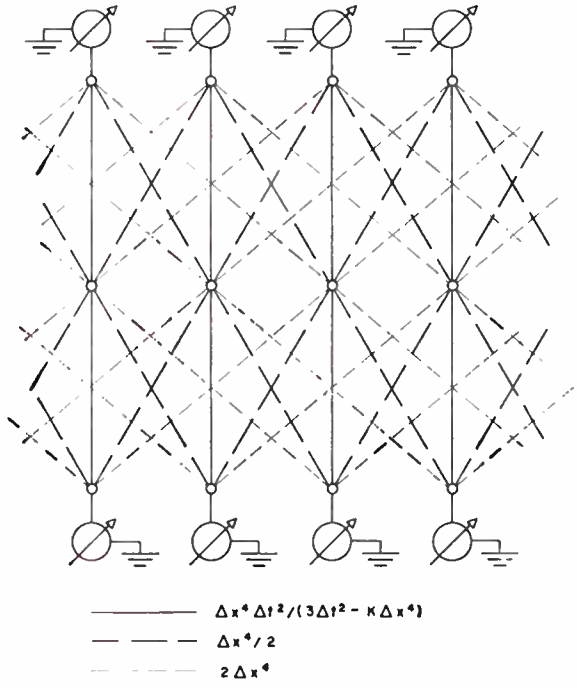


Fig. 7—Portion of network analog for biharmonic equation (line segments represent resistors).

The operation of this circuit is exactly identical to that described for the wave equation above. Two initial conditions corresponding to the potentials in line t_0 and line $(t_0-\Delta t)$ are available for each step of the computation. The voltage supplies in line $(t_0-\Delta t)$ are adjusted to the specified values, and the voltage supplies in line $(t_0+\Delta t)$ are adjusted to make the potentials in line t_0 equal the specified magnitudes.

Modified Forms of the Basic Equations

The presence of a constant term (or a term depending upon time or space position), as in (4), is included as such in the finite-difference expansion. In the electric analog, this term is identified as a current into or out of node 0, depending upon the sign of the term. The analog circuit is then modified by including a source of appropriate magnitude which supplies a current into or out of node 0 of each node unit.

The presence of terms of the type $k\phi$, as in (6), effects a modification in the pertinent basic circuit in that a resistor (which may be positive or negative, depending upon the polarity of the additional term) is connected from node 0 to ground. If a first derivative as well as a second time-derivative is present, as in the case of (6) or in the case of a transient problem governed by the biharmonic equation in which damping as well as vibration occurs, the two time derivatives are approximated by

$$K_1\frac{\partial^2\phi}{\partial t^2}+K_2\frac{\partial\phi}{\partial t}$$
$$\cong\frac{K_1}{\Delta t^2}(\phi_2-\phi_0)+\frac{K_1}{\Delta t^2}(\phi_5-\phi_0)+\frac{K_2}{\Delta t}(\phi_2-\phi_0)$$
$$=\left(\frac{K_1}{\Delta t^2}+\frac{K_2}{\Delta t}\right)(\phi_2-\phi_0)+\frac{K_1}{\Delta t^2}(\phi_5-\phi_0). \qquad (16)$$

If terms of this type are included in (13) and (15), resistors R_2 and R_5 are no longer equal to each other, but the over-all method of simulation and operation remains essentially unchanged.

Two- and Three-Dimensional Fields

For the sake of simplicity, the above discussion has been limited to field problems containing only one independent space variable. The extension of this method to problems formulated in two and three space dimensions is very straightforward. The Laplacian operator in (1)–(6) then becomes, for two and three dimensions, respectively,

$$\nabla^2\phi=\frac{\partial^2\phi}{\partial x^2}+\frac{\partial^2\phi}{\partial y^2} \qquad \nabla^2\phi=\frac{\partial^2\phi}{\partial x^2}+\frac{\partial^2\phi}{\partial y^2}+\frac{\partial^2\phi}{\partial z^2}. \qquad (17)$$

The finite-difference grid of Fig. 1 is then modified to extend in three or four directions (space variables plus time variable). The second derivatives with respect to y and z are approximated by finite-difference expressions similar to those of (11). Eq. (13), in the case of the simple wave equation, is then modified by the addition of these terms. Such an analog circuit for a typical node then has positive and negative resistors extending to 10 or 14 adjacent grid points for two- and three-dimensional problems, respectively. The method of solution remains essentially unchanged. Similar extensions can be effected for the treatment of the biharmonic equation and the diffusion equation.

Time-Varying and Nonlinear Parameters

The variation of field parameters with time is readily accommodated on the DSDT computer. Since the solution proceeds in discrete time steps, it is a simple matter to vary the network resistors after each step, in accordance with the variation of the field parameters. The magnitudes of the positive and negative network resistors at a specific node reflect the magnitudes of the field parameters in the corresponding vicinity of the field. These resistors are then adjusted in a stepwise manner as the computation progresses.

Nonlinearities in the field parameters are reflected in the analog by nonlinearities in the network resistors. Such nonlinearities can be accommodated without undue difficulty by making corresponding adjustments in the network resistors after each step in the computation.

Electronic Circuit for Typical Node

The main difference between the DSDT computer and the conventional resistance network analyzers, including Liebmann's transient heat transfer analyzer, is that some of the resistors at each node have negative magnitudes and that the voltage supplies in the $(t_0+\Delta t)$ line are all adjusted simultaneously to make the potentials in the t_0 line equal to their specified values. Both of these tasks can be handled by dc amplifier techniques.

The governing equation for a negative resistor $(-R)$ connecting a node of potential V_a to a second node of potential V_0 is

$$i=-\frac{V_a-V_0}{R}, \qquad (18)$$

where i is the current *into* node 0. The purpose of the electronic circuit is to force this same current into node 0, using a positive resistor instead of a negative one. If a positive resistor of magnitude R terminates at node 0, there must be applied at its other end a voltage V_x such that

$$i=-\frac{V_a-V_0}{R}=\frac{V_x-V_0}{R}, \qquad (19)$$

or solving for V_x,

$$V_x=2V_0-V_a. \qquad (20)$$

This voltage V_x is generated using a summing circuit of the type shown in Fig. 8. The triangle represents a dc

amplifier similar to that used in conventional analog computer installations. It is characterized by a flat-frequency response down to dc, an open-loop gain in excess of 10,000 and a negative output for positive input (as indicated by the minus sign in its right-hand corner). The input-output relationship for the circuit is

$$e_0 = -R_f\left(\frac{e_1}{R_1}+\frac{e_2}{R_2}+\cdots\frac{e_n}{R_n}\right). \qquad (21)$$

To simulate a negative resistor, the circuit is applied as shown in Fig. 9(a). If more than one negative resistor terminates on the node, all negative resistors can be simulated by a single positive resistor and one operational summing circuit. Fig. 9(b) illustrates the realization of two negative resistors, while Fig. 9(c) shows how four negative resistors terminating on a node can be synthesized. It should be noted that, regardless of the number of negative resistors terminating on a node, only one electronic amplifier is required.

The automatic adjustment of the feed-in voltage supplies is accomplished using a dc amplifier without a feedback resistor as shown in Fig. 10. In this case, the amplifier has a positive output for positive input. The $+V_0$ input comes directly from the 0 node of the network, while the $-V_0$ input comes from a separate voltage supply. This feed-in voltage is set to the value desired of V_0. Since the amplifier has a very high gain, the action of the circuit forces the voltage at point S to be very nearly 0. That is, the amplifier output automatically assumes a voltage such that a current flows from node 2 into node 0 causing the voltage at node 0 to assume its specified magnitude. This happens automatically and almost instantaneously for all node circuits.

Typical node circuits for the treatment of the diffusion equation, the wave equation, and the biharmonic equation are shown in Fig. 11. A separate node circuit is used for each space increment. Separate supplies are employed to provide the specified boundary potentials.

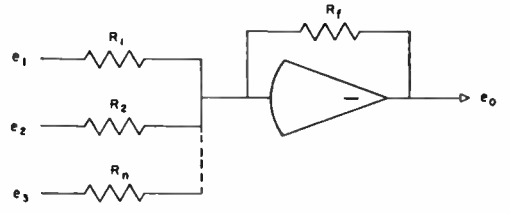


Fig. 8—Electronic summing circuit.

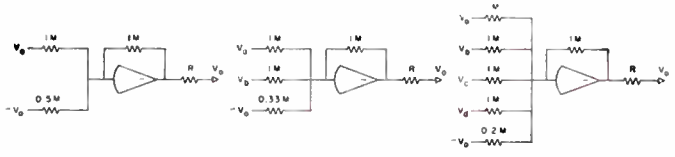


Fig. 9—Negative resistors.

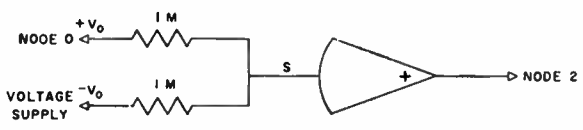
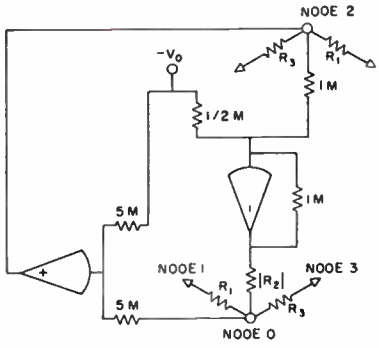


Fig. 10—Automatic feed-in voltage adjusting circuit.

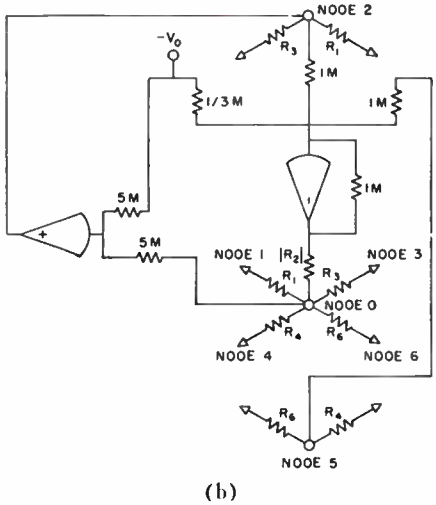
Design of Practical Node Module

Node Module Schematic

The computer system is designed on a modular basis. The node circuits for each node of the finite-difference net are contained in a separate electronic unit; these units are then interconnected using removable patch



(a)



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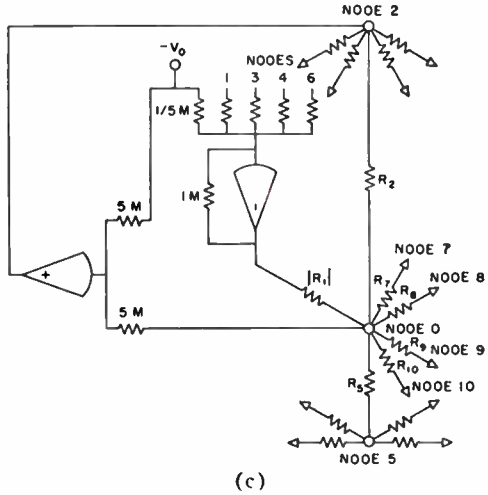

(c)

Fig. 11—Typical node circuits including electronic elements.

cords. In addition to the node units, the system includes units for the application of boundary potentials and several regulated dc voltage supplies. A simplified circuit of a typical node unit is shown in Fig. 12. The circuit is seen to contain three dc operational amplifiers, two with negative outputs and one with a positive output for positive input. Three center-tapped 5000-ohm potentiometers are employed to sense the voltage at node 2 and to apply the required voltages to node 0 and node 5. After each step in the computation, the selector switch is rotated one step, and the functions of the three potentiometers are changed.

Thus, in the position shown, potentiometer 2 is set to produce the required $+V_0$ input to amplifier 3, potentiometer 3 is set to the specified voltage at node V_5, and potentiometer 1 is balanced manually until its voltage is equal to the voltage existing at node 2. This balancing is accomplished with the aid of the meter M, and the push-button arrangement. After all node units have been balanced in this manner by closing the push-button and adjusting the potentiometers, the selector switch is rotated one step in a clockwise direction. Potentiometer 1 then furnishes the input $+V_0$, and potentiometer 2 furnishes the input to V_5. Potentiometer 3 is then employed to balance and read the potential existing at node 2. In this way, each step of the computing operation requires only the adjustment of one potentiometer at each node.

Amplifier 1 acts as the automatic servo to force the voltage at node 2 to assume the required value. Amplifier 2 simulates the required negative resistors and can assume the function of 1, 2, or 4 negative resistors as required by the problem. Amplifier 3 acts as a sign changer. These amplifiers are simple dc amplifiers of the commercially available type. They are fashioned as plug-in units and differ from the type used in electric analog equipment only in that the required high-frequency response in this case is far less severe; they need be accurate only at dc.

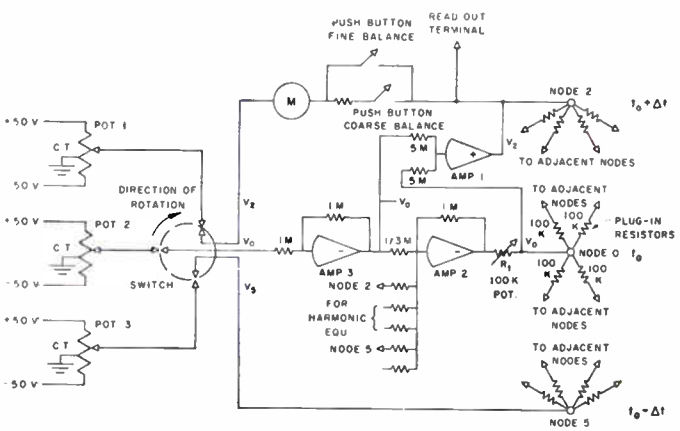

Fig. 12—Simplified schematic of node module.

Physical Layout

The typical node module includes an electronic chassis, a front panel and a rear panel. On the front panel are mounted all potentiometers, the selector switch, the meter M, the amplifier overload indicators, and the amplifier balancing controls. The rear panel contains, in addition to the power supply socket through which the required dc and filament voltages are applied, a number of female plug-in connectors. These are internally connected to the various node points V_2, V_5, and V_0, as well as to the network resistors. The modules are interconnected by means of patch cords. The chassis itself contains the three amplifiers mounted in vertical positions and plugging into separate octal sockets, as well as the network resistors. For maximum flexibility, these precision resistors are attached to plug-in connectors and can be readily removed from the circuit or exchanged for resistors of different values. Plug-in connectors are also employed to permit modification of the topology of the circuit as required for different types of the basic equations.

Method of Operation

The operation of the circuit proceeds as follows:

1) The amplifiers of each node unit are balanced (unless the amplifiers have been provided with a chopper-stabilizer).

2) The node units are interconnected using patch cords, as determined by the finite-difference approximation method described above.

3) Initial conditions as specified are applied by means of potentiometers 2 and 3 of each node circuit.

4) Boundary conditions are applied to the units in the immediate vicinity of the field boundary. Separate potentiometers and voltage supplies are used for this purpose.

5) Potentiometer 1 in each node circuit is balanced in turn. When all node circuits have been balanced in this fashion, the voltages at node 2 of each circuit represent the field potentials at time $(t_0+\Delta t)$ and are recorded. This may be done manually using a separate voltmeter, or it may be accomplished automatically using a stepping switch which samples each of the required nodes. An analog-digital converter, printer and tape punch are provided to permit the QSDT computer to be used in conjunction with digital computers.

6) The selector switch at each node circuit is rotated one step in a clockwise direction.

7) Potentiometer 2 of each node circuit is now balanced using the push-buttons and meter M. The voltages now existing at node 2 are recorded. This procedure is repeated over as many time increments as necessary.

Algebraic Function Calculations Using Potential Analog Pairs*

MERLE L. MORGAN†, MEMBER, IRE

Summary—**A new potential analog method is developed, in which both the magnitude and the angle of functions of a complex variable are calculated from their pole-zero plots. The method is based on a pair of "factor analog" voltage distributions in a complex plane, on which voltage measurements at the zeros and poles of the function are used for the calculation.**

Introduction

When electric current flows in a uniform layer or sheet of resistive material, the voltage contours and the current streamlines obey the same geometric laws as the real and imaginary components of analytic functions of a complex variable. Various investigators have used this principle to evaluate rational algebraic functions by placing current sources and sinks at the zeros and poles of the function.[1–7] The voltage measured at the point representing any value of the complex variable was then proportional to the real component of the logarithm of the function—the log magnitude. Unfortunately, there was no practical way to set up a similar analog voltage distribution for the imaginary component—the angle of the function.

A new approach was needed if the complete solution was to be found by potential analog methods. The new approach proved to be surprisingly simple. The key to the problem was the use of the theorem of reciprocity—the interchanging of current input and voltage output points in the analog. In the old method, the voltage distribution was the analog of the whole function, and varied with the location of the zeros and poles of the function. In the new method, the voltage distribution is the analog of the general factor type, with measurements at the zeros and poles. In the factor analog, the distribution moves with the value chosen for the variable, but its shape remains fixed, depending only on the form of the equation, not on the zero and pole locations. This simplification makes possible the construction of a pair of analogs to represent both components. A general investigation of this new analog computing technique was made the subject of a doctoral thesis.[8]

Algebraic Functions of a Complex Variable

The kind of functions to be discussed are those which can be expressed in either of the two equivalent forms

$$F = K_1 s^{n_0}(s - s_1)^{n_1}(s - s_2)^{n_2}(s - s_3)^{n_3} \cdots = K_1 s^{n_0} \prod_i (s - s_i)^{n_i} \tag{1}$$

or

$$F = K_2 s^{n_0}\left(1 - \frac{s}{s_1}\right)^{n_1}\left(1 - \frac{s}{s_2}\right)^{n_2}\left(1 - \frac{s}{s_3}\right)^{n_3} \cdots = K_2 s^{n_0} \prod_i \left(1 - \frac{s}{s_i}\right)^{n_i}. \tag{2}$$

F, K, s and the s_i's may be complex and each exponent can be either positive or negative. The symbol $\prod$ indicates a product of factors, in a manner similar to the common use of the symbol Σ to indicate a summation of terms.

Note that (2) can be obtained from (1) by dividing each factor $(s-s_i)^{n_i}$ by $(-s_i)^{n_i}$ to obtain $(1-s/s_i)^{n_i}$. Therefore

$$K_2 = K_1 \prod_i (-s_i)^{n_i}. \tag{3}$$

Taking the logarithm of both sides of (1) and (2) and separating real and imaginary parts, each equation is replaced by a pair of equations. Using the nomenclature defined in Figs. 1 and 2, (1) becomes

$$\log |F, = \log |K_1| + n_0 \log |s| \sum_i n_i \log |s - s_i| \tag{1a}$$

and

$$\angle F = \angle K_1 + n_0 \angle s + \sum_i n_i \angle (s - s_i) \tag{1b}$$

* Received by the IRE, August 29, 1960.

† Electro Scientific Industries Inc., Portland, Ore.

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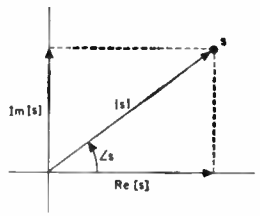


$s = \text{Re}[s] + j\,\text{Im}[s]$

where $j = \sqrt{-1}$

Re [s] = the real component of s

Im [s] = the imaginary component of s

or $s = |s|\,\epsilon^{j\angle s}$

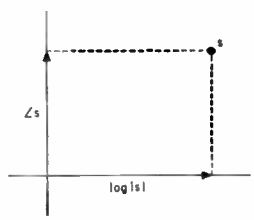
where $j = \sqrt{-1}$

ϵ = the base of natural logarithms = 2.718 ···

|s| = the magnitude of s

∠s = the angle of s

Fig. 1—The s plane.



$\log_\epsilon s = \log_\epsilon |s| + j\angle s_{\text{radians}}$

where $j = \sqrt{-1}$

$\log_\epsilon$ = the natural logarithm

|s| = the magnitude of s

∠s = the angle of s

Fig. 2—The log s plane.

and (2) becomes

$$\log |F| = \log |K_2, + n_0 \log |s| + \sum_i n_i \log \left|1 - \frac{s}{s_i}\right| \qquad (2a)$$

and

$$\angle F = \angle K_2 + n_0 \angle s + \sum_i n_i \angle \left(1 - \frac{s}{s_i}\right). \qquad (2b)$$

In these magnitude and angle equations, the product of factors has been converted to a sum of terms and the value of each term is real, not complex. These equations therefore form the basis of practically every analog method for evaluating (1) or (2), whether the analog is graphical, mechanical or electrical. The antilogarithm of the magnitude equation is sometimes taken to express the magnitude of the product as the product of the magnitudes of the factors. The angle of the product, however, is always equal to the sum of the angles of the factors.

If all the exponents in an algebraic function are integers, the function is said to be rational. A rational algebraic function is often written in the form

$$F = \frac{a_0 + a_1 s + a_2 s^2 + \cdots + a_c s^c}{b_0 + b_1 s + b_2 s^2 + \cdots + b_d s^d}. \qquad (4)$$

This function can be expressed in the form of either (1) or (2) by factoring the numerator and the denominator. The numerator yields factors with positive exponents and the denominator factors with negative exponents. Note that (1) and (2) have been written so that if s is equal to one of the s_i's, the factor is equal to zero. When a function given in the form of (4) is to be expressed as (1) or (2), the s_i values are the roots of the equations formed by setting the numerator and the denominator each equal to zero. The K value is determined by inspection:

$$K_1 = \frac{a_c}{b_d} \qquad (5)$$

or

$$K_2 = \frac{a_0}{b_0}. \qquad (6)$$

In factors with positive exponents, the s_i values are called zeros of the function, since the function is equal to zero at these values of s. In factors with negative exponents, the s_i values are called poles, since the function becomes infinite at these values. The exponent on the factor is called the order of the zero or pole. If the coefficients in (4) are real, complex zeros and poles will occur only in conjugate pairs—with equal real parts, but with imaginary parts of opposite signs.

In the factor analog method, the exponents need not be integers and the zeros and poles need not occur in conjugate pairs. When there are factors with fractional exponents, their s_i's are called branch points. In this article the treatment of a branch point is the same as that of a zero or pole, and a branch point will therefore be thought of as a fractional-order zero or pole. Since the factor analog method handles any function in the form of (1) or (2), it will even include certain transcendental functions when they can be written as an infinite product series in this form, from which a finite number of factors can be used for calculation.

Coordinate Systems for Complex Quantities

Any complex quantity can be specified by either of two pairs of components—its real and imaginary parts, or its magnitude and angle. The relationship between these components is given in Fig. 1.

A real number is simply a complex number whose imaginary part is zero. The real part can be either positive or negative. In terms of magnitude and angle, a positive real number is a complex number whose angle is 0°; a negative number is one whose angle is 180°.

A complex quantity can be represented as a point in any two-dimensional coordinate system. The most common coordinate system for a complex variable, for ex-

ample, s, is the one shown in Fig. 1. It is called the s plane, because its rectangular (Cartesian) coordinates are Re $[s]$ and Im $[s]$. Its polar coordinates are $|s|$ and $\angle s$.

Other coordinate systems may be named by a function of the variable defining them. For example, in the log s plane, the rectangular coordinates are Re [log s] and Im [log s]. These are log $|s|$ and $\angle s$ respectively, shown in Fig. 2. It is possible to make graph paper for any coordinate system using either the contours of Re $[s]$ and Im $[s]$ or the contours of $|s|$ and $\angle s$. These graph papers for the s plane and the log s plane are shown in Fig. 3.

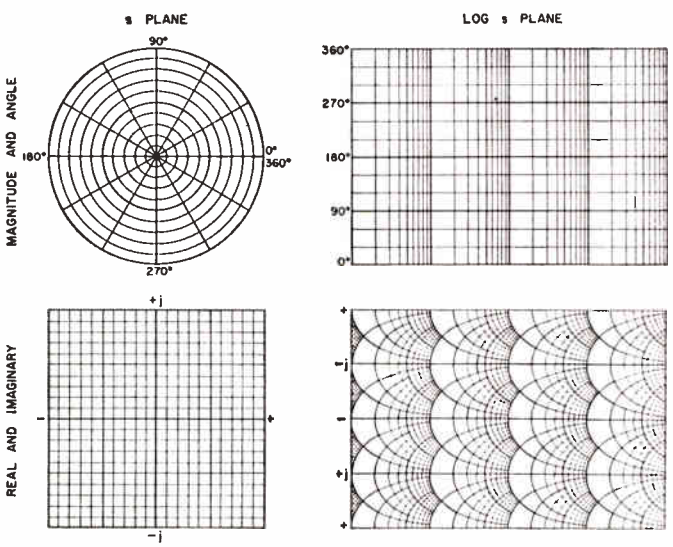


Fig. 3—Coordinate systems.

Angle values differing by 360° represent the same value of the variable; therefore in the log s plane any 360° strip is sufficient for the representation of all values of s. The log s plane possesses a great advantage over the s plane in plotting over a wide range of values. In the s plane, small values of s may be too near the origin to be plotted accurately, while large values may be off the plot. In the log s plane, many decades can be included with the same relative plotting accuracy for all values, and the decimal point can be shifted as desired, as on a slide rule.

A transformation from one coordinate system to another is said to be conformal wherever the function relating them is analytic. In potential analogs in uniform sheet materials, conformal transformations have the extremely useful characteristic that if a set of boundary conditions produces the analog of a function in one coordinate system, the same conditions at the transformed boundaries in any conformal transformation of the coordinate system will produce the analog of the same function.

A change in scale is a conformal transformation if both coordinates are changed in the same proportion. In the s plane, for example, any scale can be chosen, but both Re $[s]$ and Im $[s]$ must be measured in the same units. The log s plane is a conformal transformation of the s plane (everywhere except at $s=0$ and $s=\infty$) if the natural logarithm of magnitude and radians of angle are plotted to the same scale.

Since neither natural logarithms nor radians are convenient units for practical plotting, it is customary to use a logarithmic scale marked directly in decimal values for $|s|$ and a linear scale marked in degrees for $\angle s$. Such semilogarithmic graph paper is a conformal transformation of the s plane only if the proper scale ratio is used. On the logarithmic scale, the usual unit of distance is the decade, commonly called a "cycle" in graph paper. Since log $10=2.303$, and 2.303 radians $=131.9°$, one decade must equal 131.9°. The log s graph papers in Fig. 3 are drawn in this scale ratio. Most general-purpose semilogarithmic graph papers do not meet this criterion, but there is one type which is very nearly correct. Graph paper with 3 decades in 10 inches by 10 lines per half inch fits the conformal transformation requirement within about 1 per cent when each line represents 2°. Log-log graph paper is also available to the same scale, and semilogarithmic paper is available with the same logarithmic scale but with 12 lines per inch, providing 40 lines per decade for decibel plotting equivalent to log-log plotting.

A conformal transformation need not be on a plane surface. One interesting transformation is the conversion of a strip of the log s plane into a circular cylinder by splicing together the sides of the strip. The resulting "log s cylinder" has a logarithmic $|s|$ calibration along its length, and $\angle s$ corresponds to the angular position about the axis of the cylinder.

The Principle of Dual Analogs

In the simple complex plane or any conformal transformation of it, the contours of the real and imaginary components of an analytic function obey the same geometric laws as the voltage contours and current streamlines in a uniform resistive sheet. If the voltage at every point on the boundaries of a uniform sheet can be made proportional to either the real or the imaginary component of an analytic function, then the voltage everywhere on the sheet will be proportional to the same component of the function. The boundaries of such a sheet usually consist of conducting boundaries (electrodes) along equipotential lines, and insulating boundaries (cut edges) along current streamlines.

If the voltage distribution representing one component of a function can be set up on a uniform resistive sheet by means of electrodes along the outer border of the sheet, it is always possible to set up another sheet with the electrodes and cut edges interchanged, on which the voltage everywhere is proportional to the other component of the same function. Such a pair of sheets with voltage and current functions interchanged will be called dual sheets, since their functional relation is the same as that of dual networks.

If a voltage field contains an isolated current source or sink within the area, its dual must have a circulation of current around the same point. Such a circulation is possible if the point is connected to the outer boundary by a "conducting cut"—a cut faced with a pair of strip electrodes separated by a thin insulating barrier. This conducting cut must, of course, lie along an equipotential line in the required distribution.

The New Analog Method

In the direct analog method of evaluating the magnitude of a function F, the voltage is proportional to $\log |F|$, which is Re [$\log F$]. The voltage on a dual sheet would therefore represent Im [$\log F$], which is $\angle F$. But since the magnitude analog contains current sinks and sources at all the zeros and poles of the function, the angle analog would require conducting cuts connecting all the zeros and poles along lines which were current streamlines in the magnitude analog. Such an analog is not practical. In the first place, a sheet with different conducting cuts would be required for each problem. More important, the locations of the current streamlines in the magnitude analog are not known—their determination is the purpose of the angle analog.

If dual analogs are to be useful in a practical computer, the voltage distribution must be simpler. A simplification is suggested by a combination of the reciprocity theorem and the superposition theorem. In the magnitude analog for the whole function, superimposed currents at the zeros and poles proportional to their orders produce a voltage at any point s proportional to $\log |F|$. According to these theorems, the same results will be obtained if a single current flows to the point s and the voltages at the zeros and poles are multiplied by their respective orders and added together in a "summing voltmeter" circuit. The summing voltmeter input from each zero or pole will represent the corresponding term in the log magnitude equation; each measurement on the analog therefore represents one factor in the original equation.

Factor Analogs in the s Plane

In the s plane, any value of s appears at only one point. Therefore, the magnitude analog for the new method will be produced by a radial current flow to this point from infinity, as shown at the upper left in Fig. 4. The equipotential lines are circles, shown as dotted lines. The dual of this field, with streamlines and equipotentials interchanged, is shown to the right. The most important characteristic of these voltage distributions is that they remain the same size and shape as the center moves about in the coordinate system. The practical analog can therefore be a fixed portion of the infinite field terminated at any convenient equipotentials and streamlines. The boundaries of the practical magnitude sheet will consist of a small circular electrode at point s and a larger concentric circular outer electrode. The angle sheet will have a small hole at point s, a concentric outer edge, and strip electrodes along a conducting cut on any radial line. These sheets will be constructed as rigid pieces of resistive sheet material with permanently attached electrodes connected to fixed power supply voltages. They can then be placed in the coordinate system with their centers at the desired value of s.

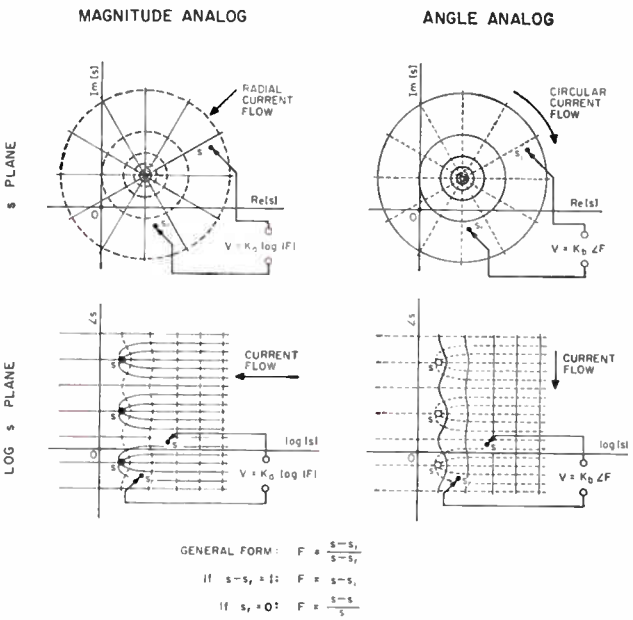


Fig. 4—Factor analogs. Case 1.

The function represented by the voltage at each point s_i will depend on the reference point s_r relative to which the voltages are measured. In the distributions in Fig. 4, the voltage will be proportional to the log magnitude or the angle respectively of the function $(s-s_i)/(s-s_r)$. In the s plane, the logical choice of reference point is one unit to the left of the center of the sheet, so that $s-s_r=1$ and the function reduces to $(s-s_i)$, the factor form of (1).

Factor Analogs in the Log s Plane

Although the pair of factor analogs in the s plane are perfectly satisfactory for a practical computer design, it is even more useful to take advantage of the conformal transformation to the log s plane. The lower half of Fig. 4 shows the log s transformation of the same distributions. Although the shape of the field has been changed, it remains constant as the value of s moves about, and a fixed portion can therefore be used in a practical analog. In the log s plane point s is repeated every multiple of 360°. In the magnitude analog each of these points is a sink for current flowing from $s=\infty$; in the angle analog, current flows around each of these points, so the angle sheet must be split by a conducting cut between each point s and the outer edge of the sheet.

In the log s plane, the reference point $s_r = s - 1$ is not practical, as it is no longer a constant distance or direction from s. Here the best available choice is $s_r = 0$, approximated at any point far enough to the left of s that $s_r \ll s$. The voltage at s_i relative to the left end of the sheet therefore represents the function $(s - s_i)/s$, which must be multiplied by s to convert it to the factor form of (1). This can be done by connecting the left end of the magnitude sheet to a voltage proportional to $\log |s|$ and the left end of the angle sheet to a voltage proportional to $\angle s$, to add these voltages to the values measured relative to the left end of the sheets. The voltage at each point s_i will then represent the function $(s - s_i)$, the factor form of (1).

In the log s plane, the analogs of another function also remain fixed in size and shape as s varies. In Fig. 4, if s is replaced by $1/s$, or $\log s$ by $-\log s$, the distributions and functions of Fig. 5 are obtained. In the log s plane, the fields have been rotated 180°. In this case the choice $s_r = \infty$, approximated at any point far enough to the right that $s_r \gg s$, immediately yields the function $(1 - s/s_i)$, the factor form of (2). Note that the analogs in Fig. 5 would not remain fixed in size in the s plane, nor those in Fig. 4 in the $1/s$ plane; in the log s plane, both analogs satisfy this requirement. Thus, in addition to its inherent plotting advantages, the use of the log s plane in the factor analog method permits the calculation of problems given in the form of either (1) or (2).

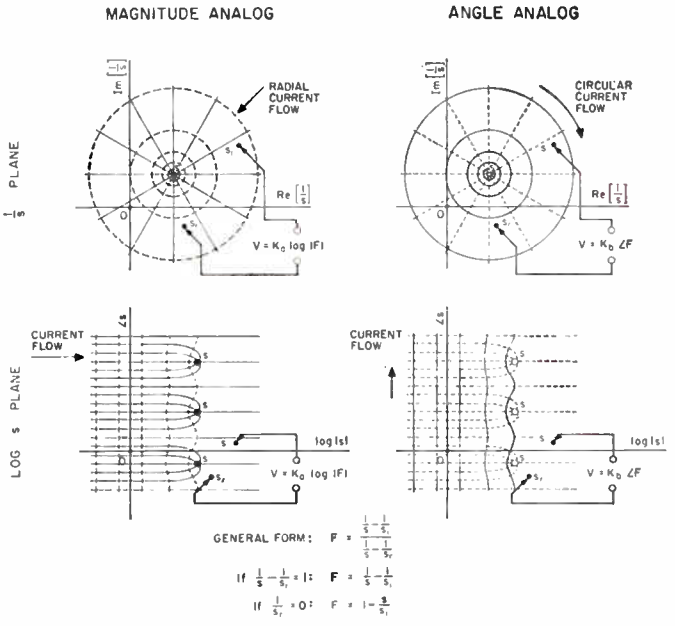


Fig. 5—Factor analogs. Case 2.

Any equipotentials and streamlines in the infinite analog field can be used as sheet boundaries. For either pair of distributions in the log s plane, the simplest sheet shape is a rectangle with its top and bottom sides passing either through points s or midway between them and long enough that the ends of the rectangle will not measurably distort the field. A sheet length of 6 or 8 decades (3 or 4 decades each side of s) will be sufficient to make the distortion negligible. If the electrodes in the magnitude sheet and the holes in the angle sheet at the points s are made small enough, they can be constructed as circles concentric with point s. On the angle sheet, although only one conducting cut is required from each point s to the outer edge, it will be more practical to cut the sheet completely apart along the straight equipotential line through s. After the electrodes have been applied to the edges of the resistive material, the pieces can be mounted side by side with a thin insulating barrier between the adjacent electrodes. The pair of electrodes on one side of s will then be shorted together in the external circuit and the voltage applied between the other pair.

Computing with Factor Analogs

In computing with factor analogs, two computing circuits are required—one for the magnitude equation and one for the angle equation. In the log s plane, the selection of factor form will be accomplished by a change in the electrode voltages applied to the sheets—the rest of the circuit will be the same for both factor forms. The basic circuits for the sheet connections are shown in Fig. 6. Although dc voltages are shown in these diagrams, ac may be used.

The circuits of Fig. 6 provide only the basic voltages representing the log magnitude and the angle of s and of each basic factor $(s - s_i)$ or $(1 - s/s_i)$. These voltages must be multiplied by their corresponding n_i values and added together. The simplest way to accomplish this is to apply each voltage to a small admittance (conductance or capacitance) proportional to n_i and to combine the resulting currents. Since all the admittances will be positive, a differential current measuring circuit must be used, with currents from numerator factors (zeros) entering one input and those from denominator factors (poles) the other input. The factor s^{n_0} can be handled similarly, applying the $\log |s|$ and $\angle s$ potentiometer voltages to admittances proportional to n_0 and connecting the currents to the plus or minus inputs of the measuring circuit as required by the sign of n_0. Currents proportional to $\log |K|$ and $\angle K$ can be supplied by potentiometers with dials directly calibrated in $|K|$ and $\angle K$. The K dial settings will represent either K_1 or K_2, depending upon which analog voltage distribution has been used.

The net current in either circuit represents the right-hand side of the magnitude or angle equation. Although it would be possible to read these currents directly on a pair of meters with appropriate scales for $|F|$ and $\angle F$, it is better for most applications to provide another pair of potentiometers supplying currents calibrated as $|F|$ and $\angle F$. The magnitude or angle equation is then satisfied when the $|F|$ or $\angle F$ dial is adjusted so that its current exactly balances the net current representing the right hand side of the equation. This operation is

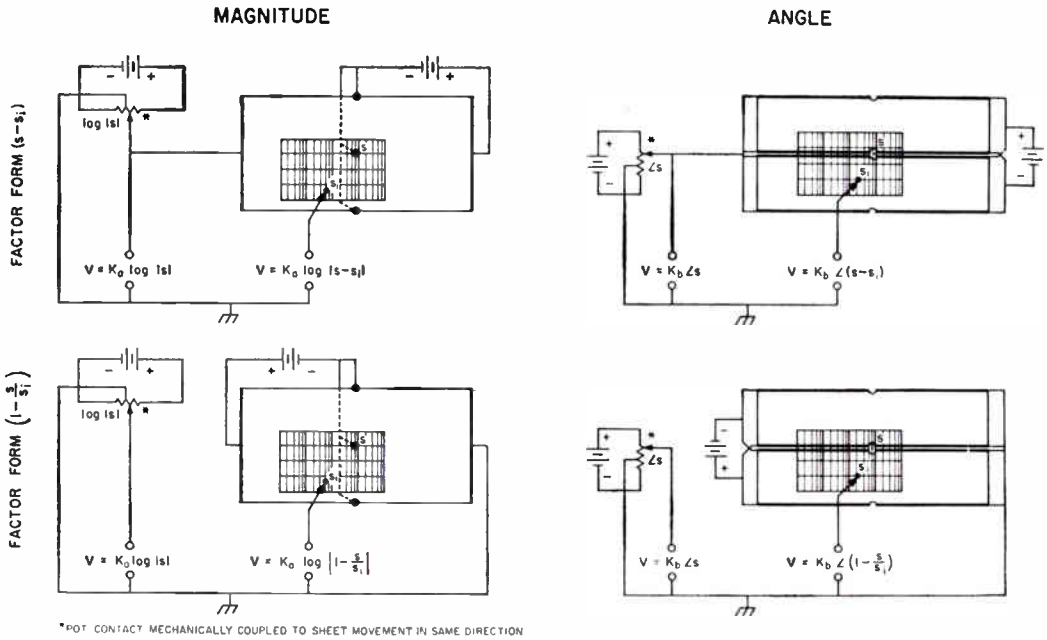


Fig. 6—Basic factor analog circuits in the log s plane.

comparable to that of balancing a bridge. The solution is independent of voltage variations so long as all voltages vary proportionally, and the current measuring circuit need not be calibrated since it serves only as a null detector.

The use of a null balance to indicate the equality of values set for the two sides of the equation is a distinct advantage in one of the most important applications—the determination of the roots (the values of s) satisfying the equation when the value of F is given. Such problems are solved by tracing a locus of solutions of the angle equation, and then retracing the curves to find the points exhibiting the specified magnitude value. In the null balance method the locus is easily traced by marking either manually or automatically the points where a balance is obtained.

For factor analog computation in any coordinate system, contacts touching an analog sheet will be placed at positions corresponding to the zeros and poles s_i of a function, and the sheet moved relative to these contacts to place its center at various values of the variable s. The portion of the infinite field chosen for the actual sheet must be large enough to cover all the zero and pole contacts over the whole range of movement. The sheet dimensions must therefore equal the sum of the s movement range and the s_i contact range. In the log s plane, the width of the sheet must be the sum of the $\angle s$ movement and the $\angle s_i$ contact range; each of these will normally be 360°, requiring a 720° sheet width. The length of sheet will equal the sum of the number of decades of movement and the number of decades in which contacts may be placed.

In the log s plane, the sheets must move in translation only; therefore the motion should be constrained by a mechanism comparable to a drafting machine. This motion can be calibrated with a logarithmic $|s|$ scale and a linear $\angle s$ scale and coupled to linear potentiometers to provide voltages proportional to log $|s|$ and $\angle s$. The s scales also serve to calibrate the positions of the zero and pole contacts. Relative to the contacts, the position of the center of the sheet represents the value of s indicated. When a contact is to be placed at any point s_i, its position can be located by moving the sheet to the setting $s = s_i$ and placing the contact at the center of the sheet. Note that it is the relative motion between the sheet and the zero and pole contacts which is calibrated; although s changes have been referred to as sheet movements, it may be more practical in actual equipment to mount the sheet stationary and move a frame carrying the contacts.

Although the $|s|$ and $\angle s$ scales on the moving frame provide the basic calibration for s and the s_i's, it will be helpful to couple this motion to a stylus for tracing and plotting s values on graph paper. At the stylus, s values can be read either as $|s|$ and $\angle s$ or as Re $[s]$ and Im $[s]$, depending upon the type of graph paper chosen. If the zeros and poles of a function have been plotted in advance, the contacts representing them can be placed in the coordinate frame without reading the $s = s_i$ values, simply by moving the stylus to each zero or pole on the plot and placing a contact at the center of the sheet. And the final use of the stylus mechanism, of course, is the plotting of points or curves representing the solution of a problem.

Applications

Algebraic functions of a complex variable occur in many practical engineering problems as a result of the widespread use of transforms for converting differential equations into algebraic equations. Examples of such

transform methods are equations involving the complex frequency $j\omega$, the Laplace transform, the Fourier transform, the D operator, and the z and w transforms used in analyzing sampled-data systems. Through the use of such a transform, a differential equation is converted into an algebraic equation involving a different variable and having a much easier solution. Once the solution is found, the inverse transform may be used to put the answer in terms of the original variable, if desired. Often, the characteristics of the transform solution can be interpreted directly, as in frequency response plots and root locus plots.

The factor analog principle makes possible for the first time a complete computer using pole-zero plots and potential analog pairs. The ESIAC® algebraic computer[9] shown in Fig. 7 is based on this principle. The ESIAC has proved to be of great value in a variety of amplifier and network calculations, and especially in feedback control system design.[10] Among the most popular applications are root locus plotting, frequency response plotting, polynomial factoring and residue evaluation. Exponential functions encountered in problems with dead time or transport lag are easily approximated, and nonlinear problems can frequently be handled by the describing function method.

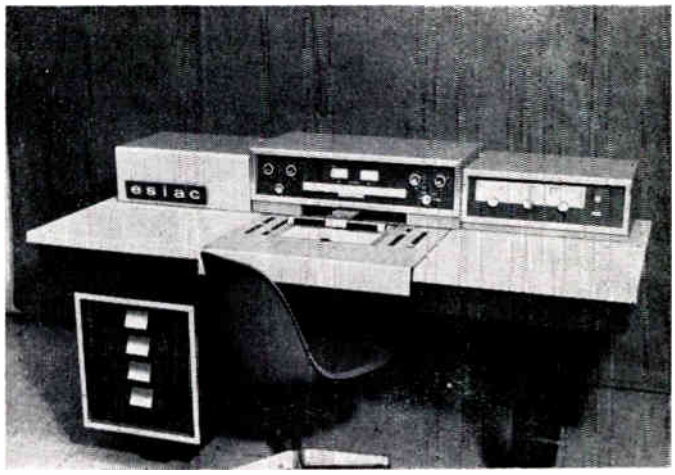


Fig. 7—The ESIAC.

The versatility of factor analog computation is further enhanced by the fact that it can be used with irrational functions containing factors with fractional exponents. In general, a factor analog computer can be looked upon as a two-dimensional slide rule for the complex plane; when the logarithmic plane is used, as in the ESIAC, the analogy to a slide rule is particularly obvious. Such complex plane calculations are useful in any problem in which a differential equation is represented by an algebraic transform, and it is hoped that investigators in other fields may be stimulated to report other applications.

[9] ®Trademark registered by Electro Scientific Industries, Portland, Ore.

[10] M. L. Morgan, "A new computer for algebraic functions of a complex variable," to be published in *Proc. First Congr. Internatl. Fed. of Automatic Control (Moscow, USSR, 1960)* by Butterworth Scientific Publications, London, Eng.

The Evolution of Programming Systems*

WILLIAM ORCHARD-HAYS†

Since many readers are employing the stored program digital computer, the problem of computer programming is of widespread interest. Developments in this discipline are numerous and exciting, as the programmers increasingly employ the computer to do its own coding. Programmers are developing hierarchies of programming systems and are moving to higher levels of abstraction and sophistication. W. Orchard-Hays has been asked to block out and explain major types of programs and programming systems, and to spell out the path of future developments in this engrossing work. In addition to the general reader, many computer engineers will find this useful reading, for it may well stimulate thoughts on improved machine organization.—*The Guest Editor*

***Summary*—In spite of a host of uncoordinated, and largely incompatible, developments in the programming field, a number of standard forms and principles are beginning to emerge. Many of the basic ideas, though known and applied in the very early days of electronic computing, have been carried to a high degree of implementation in the last few years. The tendency to overemphasize particular operational features is giving way to a healthier view that a variety of techniques are available and each has its place. They can be brought together into a special system as required for the purpose at hand, both economically and quickly, as soon as certain current efforts are brought to fruition. Unless this is done soon, the rapid advances in hardware capabilities would appear to be reaching the point of diminishing returns.**

Introduction

In the special issue of these Proceedings for October, 1953, there appeared a number of articles on the nature of digital computers and computer programming. In this paper, an attempt is made to survey and summarize programming developments since that time. In detail, this would be a nearly impossible task but, from an over-all view in retrospect, certain definite trends can be rather clearly discerned.

The matter of programming for digital computers will be approached as a body of knowledge and techniques; principles, practices, standards, developments.

To those unfamiliar with this field, it should be explained that digital computer hardware systems only provide a sort of universe within which to work; in and of themselves they can handle no problems at all. The processes carried out, the monitoring of these processes, the controls provided, and, in general, the whole application of a computer to real problems is entirely dependent on the program or system of programs provided for the machine within the limits inherent in the hardware, of course. The preparation of these programs, *i.e.*, computer programming, is a long and tedious process and usually involves the understanding and use of several "languages": machine code, symbolic code, more abstract computer languages, and the jargon associated with the particular problem at hand.

On rereading the October, 1953 issue, one is struck with the currency of the subject matter. In addressing himself to the question "Can Machines Think?,"[1] Wilkes correctly and clearly points out that it is the complexity of the program, rather than the machine, which produces features which so impress the layman. This fact is still not well understood by many nontechnical people who are nevertheless greatly concerned today with the application of computers in their business or agency. Thomas' discussion of programming fundamentals is essentially the same as that still used in introductory courses in programming.[2] And the theme of programming techniques influencing the design of computers, which Drs. Hopper and Mauchley developed, is even more germane now than then.[3] Their remark that "the development of (programming techniques might) have as profound an influence on computer design as would be produced by an entirely new type of memory or switching element" has proven to be an accurate prophecy, if anything, conservative. A case in point is the IBM 7090 which, though transistorized and physically a new design, is logically identical to the IBM 709 which is five to six times slower. On the other hand, many of the newer computers incorporate features which were clearly inspired by programming practices, the Honeywell 800 being one good example.

But if computer design has been favorably influenced by programming requirements, the converse can hardly be claimed. Most of the programming principles and techniques invoked today were not only known and discussed, but in use seven years ago. Only in the past two years or so has there begun to develop anything like a

* Received by the IRE, October 27, 1960.
† C-E-I-R, Inc., Houston, Tex.

[1] M. V. Wilkes, "Can machines think?," Proc. IRE, vol. 41, pp. 1230–1234; October, 1953.
[2] W. H. Thomas, "Fundamentals of digital computer programming," Proc. IRE, vol. 41, pp. 1245–1249; October, 1953.
[3] G. M. Hopper and J. W. Mauchly, "Influence of programming techniques on the design of computers," Proc. IRE, vol. 41, pp. 1250–1254; October, 1953.

widespread appreciation of the formidable problems facing us in the further exploitation of today's powerful hardware systems. It will be revealing to trace the genesis and development of certain rather distinct coding philosophies, to see why they have found acceptance and where, in some cases, they have fallen short.

Preparation and Use of Computer Routines

The preparation of a routine involves several steps, usually about as follows, with variations due to specific circumstances or individual work habits.

1) Analysis of the problem or orientation by an analyst.
2) Evaluation of different mathematical or logical techniques, different logical procedures within the computer, and available canned routines pertinent to the problem.
3) Detailed flow-charting of the logical and arithmetic processes to be carried out and, usually, over-all allocation of high speed storage and auxiliary units.
4) Writing of code in a suitable "language" and transcribing it to a suitable medium, *e.g.*, punched cards.
5) Assembly or compilation of the handwritten code to translate, organize and record it into the form of machine code which can actually be recognized and executed by the hardware.
6) Testing and "debugging" of the routine with synthetic or hand-computed test cases.
7) Final cleanup of the code, documentation, operating instructions, etc.

The assembly or compilation of step 5) is nearly always done by the machine itself through the use of a pre-existing routine. This latter routine is usually very elaborate, and enormous amounts of effort have been devoted to devising good "assemblers" and "compilers." Steps 3), 4), 6), 7) and, in part, 2), are built around the "language," philosophy and conventions of the assembler or compiler used in 5).

In using a checked out routine for productive work, there is also a series of steps of which the following are fairly typical: 1) collection, editing and transcribing of data and parameters; 2) loading of the routine and data into the computer; 3) processing of the data by the computer; 4) transcribing of output; 5) checking and evaluation of results. Here again, steps 2), 3) and 4) are carried out by the computer, with peripheral equipment often involved in 1) and 4). Since steps 5) and 6) of the routine preparation process involve this last process, with the assembler here the "productive" routine, and since both kinds of procedures must be carried out in great variety throughout the day at any one computer installation, there is often a severe planning, scheduling and operational problem. Furthermore, the debugging process is complicated and requires communication with the assembly and output functions to be effective. This whole complex can be further complicated by the development and use of elaborate, specialized systems which engender many difficulties related to the problem, the data, and training of the user, quite apart from the programming or machine "bugs."

It is, of course, taken for granted today that elaborate "processors," *i.e.*, programs for constructing programs, will be provided for any but the smallest machines. The vast majority of people doing programming today never have occasion to work on these processors; they only use them. Indeed, to many, understanding a "machine" is in reality understanding one or more programming systems for the machine, with scarcely a thought for the processor which vivifies the system, much less for the machine itself. This is the result of extensive efforts to provide "automatic coding" which constitutes perhaps the greatest single programming development during the past few years. Processors differ greatly in basic philosophy, however, and a discussion of the different types is tantamount to a discussion of developments in programming.

The word most commonly used for a processor is "compiler" but it is used in so many different senses that it is becoming ambiguous, like "data processing" and "systems." In the present pliable state of the programming field, it is difficult to enforce the original intent and understanding of the terms used. In spite of this, three terms, which are often used interchangeably, need to be distinguished, namely: assemblers, compilers, automatic programming systems. Certain types of compilers have developed around earlier assemblers, and "automatic programming system" is often applied to any routine which converts handwritten code to machine code. The Communications of the ACM, for example, lists 118 processors for 25 different machines under "Automatic Programming Systems," but it is like adding apples and oranges.[4] Surely it is not very meaningful to consider, within the same set, a very elementary assembler like DUAL-607 for the IBM 701 with the FORTRAN compiler for the 704. It is not merely size, age or universality which makes the difference. The very early Douglas Aircraft assembler for the IBM 701 can be compared in many ways to the fairly recent SCAT compiler for the 709. The equally early EASY FOX system for the RAND Corporation's JOHNNIAC was the result of a quite modest project accomplished mainly by Clifford Shaw of RAND's staff, but it incorporated a degree of sophistication rarely equalled to this time in some respects. It will be useful, therefore, to make certain definitions in the sequel merely for the sake of a common starting point, and with no intent of implying or suggesting their universal acceptance.

[4] Even this list is incomplete, not even mentioning SOS for the IBM 709, for example. But it is, in itself, evidence of the growth of the programming field. There are 28 different processors listed for the IBM 650 alone. Each of these is in use, presumably, by at least one entire staff.

Assemblers

The definition of an assembler used by the SHARE organization[5] is enlightening:

> *Assembler*—A computer program which operates upon symbolic input to produce machine instructions, carrying out some or all of the following functions:
>
> 1) translation of symbolic operation codes;
> 2) allocation of storage, to the extent at least of assigning storage locations to successive instructions and of utilizing symbolic addresses so defined;
> 3) computation of absolute or relocatable addresses from symbolic addresses;
> 4) generation of sequences of symbolic instructions by the insertion of parameters supplied for each case into macro definitions;
> 5) insertion of library routines.
>
> An assembler differs from a compiler chiefly in that it does not make use of information on the over-all logical structure of the program, but evaluates each symbolic instruction as though it stood alone or in the immediate context of a few preceding instructions. There is in general a one-to-one correspondence between the symbolic instructions written by the programmer and the machine instructions produced by the assembler.

Assemblers as defined above were in general use at least as early as late 1953. By 1955 they had reached a high degree of elegance for "machine language coding" and have not changed markedly since insofar as the language acceptable to them and the running times are concerned. A good assembly program is now considered the minimum essential "software" for any computer. While there are still a few types of machines for which sizeable routines may be coded directly in basic machine language, the IBM 650 being a notable example, this is impractical for the binary machines and certainly contrary to the overwhelming majority of current opinion and practice.

Anyone who has not written or modified an assembler can scarcely appreciate the logical complexity of even this basic tool. The above definition suggests that these assemblers consist of several parts for distinct functions and that compilers incorporate additional, higher level functions. In general, this is so. The design, programming and use of assemblers and compilers has exerted the greatest single influence on the programming art. The reason is not hard to find. Programming an assembler is programming for programming's sake with no extraneous considerations of mathematical algorithms, statistical estimates, numerical analyses and so on. The best programming talent had been employed on them and their design has decreed the *modus operandi* of production programming staffs.

All this is not to say that the tools thus provided have been received without criticism. Today, many consider a machine language assembler an archaic tool,[6] to be resorted to only when more sophisticated processors prove inadequate or grossly inefficient. Indeed, a sufficient number of such exceptional cases has on several occasions led to the creation of a new type of processor. The more important such developments will provide the basis for the remainder of the present discussion.

Organizational Compilers

The earliest type of compiler and one which is still important may be referred to as an organizational compiler. Essentially they organize existing library routines, new hand-written code, and generated blocks of instructions into a new over-all program. This may be done either according to a predefined structure or by means of pseudo instructions provided to the compiler. A compiler as discussed by Drs. Hopper and Mauchley in the 1953 paper[3] was essentially of this kind. Regardless of efficiencies or inefficiencies in the resulting machine program, the primary purpose of such a compiler is to simplify the procedure for getting new programs put together in a workable form. The effort required to create compatible and matching routines and to combine these into an over-all program using a basic assembler is often very considerable. The leg work and tedious details often consume more of the programmer's time than the actual planning and coding of the routines.

In the past few years such organizational compilers have reached a high degree of complexity and have tended to become merged in operating systems, which are discussed later. The SHARE Operating System (SOS)[7] for the IBM 709 and 7090, for example, compiles symbolic code written in SCAT language (symbolic compiler, assembler, translator), yet the actual compilation process is not handled by any single routine. Organizational compilers are a very important tool in the programming field and give every indication of continuing to be so. A recent development is the system maintenance compiler which is discussed later.

Mathematical Formula Compilers

Another type of processor is the mathematical formula compiler which translates mathematical formulas and logical statements, together with necessary input/output and control instructions, into a machine language program. Although such compilers were suggested many years ago, the major credit for their de-

[5] SHARE is a cooperative organization composed of users of the IBM 700 series machines. Members disseminate their computer programs to the other members, maintain programs, etc.

[6] An opinion to which there are many dissenters, including the author. However, it is certainly true that the cost of many jobs today would be prohibitive if done with a basic assembler.

[7] I. D. Greenwald, and M. Kane, "The SHARE 709 system; programming and modification," *J. ACM*, vol. 6, pp. 128–133; April, 1959.

velopment must go to the group working at IBM under J. W. Backus who created the FORTRAN processor. This has probably been the greatest single programming achievement to date and undoubtedly more people have been introduced to the use of large scientific computers through FORTRAN than in any other way. The FORTRAN project was begun in the summer of 1954 and has never really ended. Although versions of the system have been available since late 1956, there are current plans for redoing the whole system to take advantage of the features of the IBM 7090.

Quoting from a paper prepared by Backus and his associates,[8] "Its purpose was to reduce by a large factor the task of preparing scientific problems for IBM's next large computer, the 704. If it were possible for the 704 to code problems for itself and produce as good programs as human coders (but without the errors), it was clear that large benefits could be achieved. For it was known that about 2/3 of the cost of solving most scientific and engineering problems on large computers was that of problem preparation. Furthermore, more than 90 per cent of the elapsed time for a problem was usually devoted to planning, writing and debugging the program. In many cases the development of a general plan for solving a problem was a small job in comparison to the task of devising and coding machine procedures to carry out the plan. The goal of the FORTRAN project was to enable the programmer to specify a numerical procedure using a concise language like that of mathematics and obtain automatically from this specification an efficient 704 program to carry out the procedure. It was expected that such a system would reduce the coding and debugging task to less than one-fifth of the job it had been."

How well FORTRAN has accomplished its purpose can perhaps best be judged from the fact that there are now entire programming staffs which use virtually nothing but the FORTRAN system. The original 704 version consumed 18 man years of effort and an unknown number of machine hours. That, however, was only the initial cost. Certainly well over twice this amount of effort has been devoted by now to the 704 alone. The system has progressed through a series of versions not only for the 704 but also for the 709, 7090, 705 and restricted versions for the 650. The language has become so popular, in fact, that other manufacturers have found it necessary to develop processors for their own machines which accept source programs written in the FORTRAN language.

FORTRAN has not been the only such project, of course. One of the lesser known efforts, also started in 1954, was the PACT 1 compiler (Project for the Advancement of Coding Techniques).[9] This project was a cooperative venture of IBM 701 users in the Los Angeles area and a working processor was available by late 1955. The PACT 1 compiler allowed better control of the machine in some ways than does FORTRAN and it was later reprogrammed for the 704 and called PACT 1–A. The origin of the SHARE organization can be traced to these efforts by the Los Angeles group but for some reason PACT 1 never achieved widespread acceptance, probably because it was more programmer oriented than FORTRAN. Since there has been a continual shortage of experienced programmers over the years and since FORTRAN is easier to explain to the mathematician, engineer and physical scientist than other source languages, it has helped very greatly in promoting the profitable use of large scale computers and has thus gained a large number of devotees.

Another reason for the popularity of FORTRAN is that the processor is also an organizational compiler. A correctly written source program presented to the FORTRAN processor will be converted, completely and automatically, to a package of routines ready for loading and execution. Nothing further need be done but remove the cards from the punch stacker and place them in the read hopper to be ready to go.[10] This foresight exercised by the designers of FORTRAN has paid off in efficient over-all operation and in avoiding the discouragements so often caused by trivial card handling and procedural errors. It has had one major disadvantage, however, in that being so complete it has tended to be incompatible with other processors and programs. Considerable effort has been expended in trying to overcome this difficulty but the incorporation of FORTRAN compiled programs into other systems which have developed since is still unsatisfactory or impractical in most cases.

Another compiler deserving special mention is IT or "internal translator" built for the IBM 650 by Dr. A. J. Perlis and his associates at Carnegie Institute of Technology.[11] The excellent planning which went into IT was somewhat nullified by the stringent limitations of the 650 itself. The result was that the notations used for programming in IT are somewhat unnatural. The compiler translated from this language into a standard assembly language for the 650. Later a restricted version of FORTRAN called FORTRANSIT was developed for the 650 which required a 3-stage translation, FORTRAN to IT, and IT to assembly language. However, in spite of the cumbersome nature of this amalgamated processor, IT itself represented a real pioneering effort in automatic programming and the original version was actually in operation earlier than FORTRAN on the 704. It is reported that Perlis is now designing another automatic programming system for a newer and much more adequate computer.

[8] J. W. Backus, "The FORTRAN automatic coding system," limited publication.

[9] C. L. Baker, "The PACT I coding system for the IBM type 701," *J. ACM*, vol. 3, pp. 272–278; October, 1956.

[10] Versions now exist which permit automatic "load and go" operation using magnetic tape.

[11] A. J. Perlis, J. W. Smith, and H. R. Zoeren, "Internal Translator (IT)—A Compiler for the 650," Carnegie Inst. of Tech., Computation Center, Pittsburgh, Pa.

The success with algebraic language compilers has led to an international effort to define a universal algorithmic language called ALGOL. A number of committees and subcommittees have been actively working on this project since 1958 or earlier.[12,13] The reader should refer to the references for further details. However, two facets of the total effort warrant explicit mention here. First, it was recognized that three language levels would be required: a reference language, a publication language and several hardware representations. The reference language represents the results of a widespread scientific effort at unifying computational techniques. It will be unique and will be the basic reference for the other levels. The publication language recognizes variations in printing and writing practices. Second, the development of any particular so-called ALGOL compiler may or may not be adequate to handling complete ALGOL statements and may or may not include extraneous devices. Furthermore, source programs written for one such hardware representation may not necessarily be compatible with another one.

An effort such as ALGOL is a huge undertaking and one which is certainly promising. One should not expect, however, to find universal compatibility in the near future. In fact, it is not clear that ALGOL even takes into account many of the problems which are brought about by the use of large scale computers and certainly particular machine processors will leave much to be desired for the immediate future.

Data Processing Systems

In the past three years or so a number of systems especially designed for data processing applications have been developed. These likewise involve a type of compiler or, in some cases, what might more properly be called generators. The distinction between a compiler and a generator is somewhat hard to maintain. Roughly, however, a generator creates blocks of code according to some fixed plan specialized by the use of parameters, whereas a compiler creates code from more detailed instructions within a much wider and more flexible framework. Compilers and even assemblers make use of generators as subroutines. On the other hand, elaborate generators, as under discussion here, may actually use compilers to augment the scope of the system.

One data processing system put into production in 1957 has had tremendous impact on large scientific machines in the last two to three years. It was developed for the IBM 702 at General Electric's Hanford Atomic Products Operation. The results of this effort were called "generalized routines,"[14] a term which does not seem to convey very well the sophistication and power of the concept. There were three major parts: a file maintenance routine, a sort routine, and a report generator. These were not routines in the ordinary sense of the word but rather generators which specialized predefined structures for a particular job. The concept is thus somewhat of a cross between that of a compiler and that of an interpretive system. The experience with these routines on the 702 at the Hanford installation was so gratifying that follow-on projects were undertaken not only by that group but by other installations as well. The 702, which was not noted for its speed, generated routines so quickly that no attempt was made to save them. It was actually easier to regenerate than to write out and reload the object program. Basically these routines were designed to operate on standard files using a limited number of standard operations but with options for inserting special hand written code to handle "unusual" situations.

The coding concept used here was quite different from ordinary machine language coding or from the source language of a formula translation compiler. Essentially the idea was to describe the desired results and to let the generator create the necessary code to accomplish this, working from well defined premises regarding the nature of the data formats, etc. This might be called "inductive programming" as opposed to more usual "deductive programming." The input forms to the report generator were particularly clever. They consisted of page layout sheets, designed in such a way that they could be interpreted as coding forms and keypunched a line at a time. In this way the programmer could draw a picture of the desired report and have the necessary code to create this report generated for him automatically. Another set of forms specified the source of the data which was to be inserted in the report. Similarly, in coding the manipulation of fields within records within files, the essential information was specified by means of directories.[15]

With these generated routines it was actually possible to specify the selection of information from a file, the format of a report, the necessary operations for transforming or sorting the selected data to go into the report and to have the necessary input key punched and the entire job done all in an afternoon. These routines were quite widely discussed and led to two other sizeable projects. One of these was the writing of the SURGE compiler[16] for the IBM 704 as a cooperative effort of several users of that machine. The other was the creation, by GE Hanford and others, of the 9PAC system for the IBM 709 which is now in productive use

[12] A. J. Perlis and K. Sameson, "Preliminary report—international algebraic language," *Commun. ACM*, vol. 1, pp. 8–10; December, 1958.

[13] P. Naur, ed., "Report on the algorithmic language ALGOL 60," *Commun. ACM*, vol. 6, pp. 299–312; May, 1960.

[14] W. C. McGee, "Generalization: key to successful electronic data processing," *J. ACM*, vol. 6, pp. 1–23; January, 1959.

[15] The GE Hanford people call these dictionaries. However, more properly, a dictionary is a list of possible entries in a field together with their meaning in some other coding system. The directories, on the other hand, describe the layout of a record within a file. A directory is itself a file with a record for each field of the record which it describes.

[16] SURGE manual prepared by North American Aviation, Inc., Columbus, Ohio, 1959; available to IBM 704 users through the SHARE Distribution Agency.

in many installations and is maintained by IBM. The SURGE compiler was modified for the 709 and a more elaborate modification is underway for the IBM 7090. Many of those who worked on the original SURGE program later helped in the design and writing of the FACT system for the Honeywell 800,[17] undoubtedly the most ambitious single data processing compiler undertaken to date.

There is no question that the basic notions in these routines are correct and that much future work will be based on them. Some of the limitations which these systems have had to date are the awkwardness of incorporating special routines or handling nonstandard files, the difficulty of designing fully integrated data processing runs and the generally somewhat piecemeal approach to related but different computing problems, such as file maintenance and sorting. Much progress is being made, however. A system nearing completion for the IBM 7090 overcomes the above objections. Out of this approach a few basic principles have begun to emerge and it seems reasonable to expect that something approaching a data processing discipline will eventually evolve.[18]

Information Storage and Retrieval Systems

For a number of years, information storage and retrieval systems of varying degrees of elegance have been programmed. These are similar to data processing systems except that the emphasis is on the continued use of a large file rather than the day by day maintenance of many files. Such systems may include either an interpretive input routine or a compiler of some kind to convert data selection statements into the appropriate machine code to interrogate the files. These statements consist of descriptors of various selection criteria combined with Boolean operators. In such systems it is also necessary to allow for the handling and sorting of variable length records or several classes of records, some of which may be subsidiary to others. When such work was first undertaken, it appeared to be enormously complicated. But some recent programs have proven that the generality required in the information formats, when once planned, actually leads to simplifications in some of the more standard operations. For example, a variable length, variable way sort-merge program was thought to be almost impossible a few years ago but such programs are now in operation and are surprisingly fast. Progress with the Boolean selection compilers has not been as great but this has resulted not so much from an inability to define them as from a reluctance of interested parties to pay the fairly sizeable costs. Since much of this can be simulated either by machine language coding or by hand and punched card machine procedures, it has been felt that the practicality of large information storage files needed to be proven before too much expense was incurred in the systems.

Actually a number of systems have been in use over the past several years which handle one or more aspects of the information retrieval problem quite well. Perhaps the earliest one was programmed for the IBM 701 at the Naval Ordinance Test Station at China Lake under the direction of Bruce Oldfield. Several organizations and government agencies have looked into this general area and IBM has a department of their Data Processing Division devoted to information retrieval problems.[19] This subject is so broad that it quickly carries one far afield from computer programming. However, attempts to handle these problems have helped to clarify concepts and standardize approaches to data file problems in the programming field itself.

Simulators

A simulator is a program which effectively converts an actual physical computer into a different computing device, simulating the actions of the latter by means of routines written for the former.[20] The simulated machine may be real or imagined. In a broad sense almost any routine might be considered a simulator but there is a more explicit meaning usually implied by the term. One of the more useful forms of simulators is one which simulates one actual machine, or at least the programming language for that machine, on another actual machine. The simulated machine may be either an earlier computer or a more advanced one than the machine doing the simulation. For example, the assembler for a new machine is usually written in terms of its own language and first assembled, itself, on an earlier machine for which a simulation program has been written. On the other hand, it is often desirable, when switching from one physical system to a newer model, to have a simulator on the new machine which will execute important programs which have been running on the older one. Both these uses of simulators have become quite widespread.

[17] "FACT," Honeywell Electronic Data Processing," Minneapolis-Honeywell DATAmatic Div., Wellesley Hills, Mass.; 1960.

[18] In this author's opinion, experience with such routines is likely to lead to far-reaching results as new perspectives are gained by widely dispersed users. For another related approach to data processing problems, the interested reader should obtain a copy of the report: "COBOL, *CO*mmon *B*usiness *O*riented *L*anguage," Dept. of Defense, Washington, D. C.; April, 1960. This is an effort similar in scope to ALGOL and aimed at similar goals for data processing as opposed to mathematical algorithms.

[19] GE's Flight Propulsion Division has an elaborate literature searching system on an IBM 704 near Cincinnati, Ohio. GE's Large Steam Turbine Generator Department at Schenectady, N. Y., has also done considerable work on storage patterns and symbolic notation. The Systems Development Corporation in Santa Monica, Calif., did an extensive study on the organization, retrieval and sorting of information. C-E-I-R, Inc. has likewise studied a number of such problems and has one partial system in operation on the 7090 with work continuing.

[20] A more general meaning of the term is that of a system of programs to simulate some physical complex such as a refinery, a network of factories and transportation links, maneuvers of armed forces, and such like. A similar but less grandiose meaning is sometimes implied also, as the simulation of a distillation tower, simulation of a job shop, or simulation of a bombing run. This has to do with the application of computers and programming techniques, however, rather than with programming systems *per se*.

These simulators are essentially interpretive routines, and, as might be expected, result in slow effective speeds. Usually a simulator is slower than the simulated machine, even when run on a physically faster machine. An exception is the simulation of the IBM 650 on the 704 which was programmed by at least two installations.[21] In both cases, a 650 program runs considerably faster on the 704 than on the 650. Remington Rand, St. Paul, Minn., also simulated the IBM 650 on their 1103A with similar results.

Simulators are important in the development of new machines and new systems for new machines. Their value as a stop-gap measure to guarantee operation of old programs on new equipment has, in the author's opinion, been greatly overrated. When the decision is made to upgrade equipment, a parallel decision should be made to upgrade the programs. Otherwise, the result may be to spend more money to accomplish the same old jobs less efficiently.

Specialized Service Systems

Some types of problems are so widely encountered and consume so much machine time that it has been found advantageous to design special systems for their solution and to continue improvements over a period of several years. Several examples could be cited but perhaps one of the best for illustrative purposes are systems for linear programming (LP) computations. This operations research technique was developed over a decade ago in studying Air Force planning and scheduling problems. It leads to a mathematical model consisting of a large number of linear restraint equations in an even larger number of variables, plus a linear functional to be minimized. From an analytical viewpoint, such models find application in a great variety of situations but what concerns us here are the mathematical and data handling problems to which such models lead.

The simplex method for solving the central mathematical problem has proven to be the most practical and flexible way to handle the calculations. After experience with some early machine procedures and routines, a project to develop LP computing techniques was begun in late 1952 at The RAND Corporation. Numerical techniques for LP computations developed steadily in the following years, at RAND and elsewhere. During 1958 C-E-I-R, Inc., complete reworked, elaborated and systematized the RAND codes to allow the handling of 511 order systems in any number of variables, automatically by means of a card controlled system. The system itself, called SCROL, is kept on magnetic tape and has its own supervisory program which completely controls all components of the computer. This system has been in wide use for some two years and led to the sponsorship of an even more elaborate system for the IBM 7090, called LP/90, which has been recently completed at C-E-I-R.

In the meantime, extensions to the original simplex method had been developed into everyday analytical tools and the whole kit of LP techniques had become virtually another mathematical discipline. The growth in model sizes and analytical refinements paralleled the increased size and speed of computers for the simple reason that LP finds practical application only by use of modern computing equipment.

The experience gained over a period of seven or eight years in continually refining, extending and using these programs has led to advances in computer programming method. For example, the difficulties encountered in constructing the 704 SCROL system led to the design of a system compiler from the sole purpose of constructing the LP/90 system. (This concept is discussed further below.) Also the difficulties of running large problems on a service basis, often by mail, has led to improved organization of input editing routines, operational instructions, and the whole gamut of computing practices. For example, a fairly standardized data specification language and an LP operational language have evolved and show signs of continuing development. Such efforts are far removed from the original intent of the RAND project of merely solving models with large systems of equations in reasonable running times.

The LP systems are perhaps an extreme example of specialization but certainly not unique. A similar thing, for example, has happened with systems designed to handle large sets of differential equations, information retrieval problems, classical data processing procedures and others. The important thing with respect to the evolution of programming systems is that these specialized service systems provide counterpoint to the development of pure operating and programming systems. The latter often tend to treat the use of a computer as an end in itself whereas, of course, it is merely the means to more worthwhile goals.

List Processors

It has long been apparent to programmers of assemblers, compilers and similar programs that one of the basic problems in the use of computers is the manipulation of lists of information. Frequently these lists are arranged in echelons of abstraction starting perhaps with textual input and receding into pure symbolism and code. Also the entries in such lists may sometimes be lists themselves or may refer to indexed entries in other lists. The organization of such lists and the programs to create and manipulate them lead to difficult logical processes, not to speak of notational difficulties. The storage allocation problem is also very difficult since the length of lists is usually a function of the input, both in quantity and logical complexity. Nevertheless, several programs have been written to deal with such purely logistic processes.

[21] "Simulation programs—machine language," *Commun. ACM*, vol. 1, p. 6; November, 1958.

One effort of particular note is that of Newell, Shaw and Simon who have programmed a heuristic theorem proving system for the propositional calculus.[22] They made use of a programmed associative memory (NSS memory). The storage register of an NSS memory contains either the gross data for the information process, called data words, or information that serves to associate storages of data in the lists, called location words. A list is the fundamental assemblage of information and each register of an NSS memory is an element of at least one list. If nothing else, it is in a list of available storage. The interpretation of a particular data word depends on the list containing it, its location in the list or an identifying tag in the location word associated with it. Location words supply the links between units of information in a list. The interested reader should refer to the references for further details on this sophisticated approach to information processing.

The concepts invoked by Newell, Shaw and Simon have evidentally had a considerable influence on the design of computers.[23] It may well be that this purely abstract approach to information processing may have a more profound effect on future hardware systems and programming techniques than almost any other current effort. The importance of such studies is probably challenged only by the investigation of problems connected with time-sharing techniques, which are discussed briefly below.

Operating Systems

In contrast to specialized service systems, and often at odds with them, are general operating systems. The design of operating systems is addressed directly to the problem of human error and confusion which can easily arise in today's complicated computing center. The variety of tasks and their diverse input requirements; the different procedural approaches used by programmers; the necessity for mounting and dismounting various tape reels, loading and unloading card machines, manipulating consoles, etc., etc., which are a part of the machine operator's everyday work schedule, can all lead to gross inefficiencies in the utilization of extremely expensive equipment. It is bad enough to pay hundreds of dollars an hour for machine time and to match this cost or more with program preparation and checkout, without incurring additional expense and delay because of mistakes, misunderstandings or clumsiness on the part of the human dispatchers and operators. Furthermore, the programming job is often made unnecessarily difficult by continual duplication of effort because of a lack of standardization of basic service routines, library subroutines and procedures. The development of operating systems is the result of attempts to simplify and streamline the actual use of computing equipment.

It is difficult to pinpoint the origin of operating systems.[24] Almost any elaborate set of routines have similar features. As presently understood, however, an operating system implies a primary magnetic tape-to-tape operation of the central computer with programmable or preplanned operating instructions. The machine operator is supposed to carry out only standard general instructions plus special instructions printed out by the computer under control of a supervisory program. Standard emergency procedures are often added for use in case of a breakdown of the system. The comprehensiveness of such an approach leads to some particularly knotty problems in programming the system itself. Gross inefficiencies can also arise if great care is not exercised in the design and implementation of the control programs. The general concept has proven to be worthwhile, however, and large computers are now almost sure to be operated under one or more such systems. Some installation heads contend that an operating system is really such only if *all* work run on the computer is under its control. Where workloads are more varied, installations may be willing to use different systems for different types of jobs. A more recent concept, and probably the most useful in the long run, is that of a family of systems, all similar enough to allow operator familiarity with their common philosophy, but specialized to different purposes for the sake of machine efficiency.

A number of terms have come into use for parts of an operating system. The term "supervisory program" has already appeared above. The supervisor is the program which maintains ultimate control of the machine at all times and to which control reverts when a routine finishes its function or when an unexpected stop or "trap" occurs. Terms which are used more or less synonymously with "supervisor" are "executive routine," "monitor," "master control routine." However, these are also used in narrower or different senses and "supervisor" would appear to be preferable.[25]

The concept of a program "trap" is now in wide use for a variety of purposes. A trap may be actuated by the hardware or by conditions imposed by the design of the operating system. Frequently it is a combination of the two. Traps are a special form of conditional breakpoint and are an outgrowth of the old idea of switch controlled halts or jumps (transfers of control). For example, some machines have been designed so that particular instructions were effective "no operations" unless a manual

[22] A. Newell, J. C. Shaw, and H. A. Simon, "Programming of the logic theory machine," *Proc. WJCC*, pp. 218–240; December, 1958.

[23] G. A. Blaauw, "Indexing and control word techniques," *IBM J. Res. & Dev.*, July, 1959.

[24] One of the earliest operating systems of the type known today was on the IBM 704 at General Motors Res. Labs. See J. Strong, "The problem of programming communication with changing machines—a proposed solution," *Commun. ACM*, vol. 1, pp. 12–18; August, 1958.

[25] "Executive Routine" is used for a program which controls loading and relocation of routines and in some cases makes use of instructions which are not divulged to the general programmer. Effectively it is part of the machine. "Monitor" is often used for a routine for input/output scheduling and control, especially for machines with simultaneous input-output-compute and I/O "trap" features. "Master control" is an old term originally applied to the highest level of a subroutine hierarchy. It is thus more applications than system oriented.

switch were set in which case they became halts or jumps.[26] As computer hardware became more elaborate, a number of internal triggers which could be program tested became commonplace. Since these are usually set only by unexpected or unpredictable occurrences, and since the execution time and number of instructions for testing them can become burdensome, it has been found advantageous to have these triggers cause an automatic transfer of control to a known location, with the location from which the transfer occurred, and its cause, recorded in other standard locations. This is known as a trap. Some trapping features can also be enabled or inhibited under program control. Certain simple forms of trapping can be program simulated. For example, if a routine loading program initially fills storage with transfer instructions to a standard location, and if the executed program ever transfers control to a location which has not been filled, a simulated trap to the standard location will occur. In general, however, a true trapping feature must have hardware provisions to be effective. Trapping is a good example of the influence of programming developments on machine design.

In "buffered" machines, *i.e.*, those with a simultaneous Input/Output/compute feature, a data transmission trap is essential to effective use of buffering. Otherwise, every program using Input/Output must test frequently for the availability of a data channel. This is self-defeating. On the other hand, automatic traps whenever a data channel becomes available can lead to inordinately complex logic unless the I/O transmission control is centralized in the system of programs. This is the function of I/O Monitors which have already become a critical part of every sizeable system of programs for buffered machines.

Two other important parts of operating systems are input and output translators. Both present difficult problems but those for input are the most severe. In actuality, it appears that there is no complete solution to the general problem of input translation, at least in a practical sense.[27] Limited or specialized translators of some kind are usually provided however.

The philosophy of a complete operating system is usually somewhat as follows: symbolic code in its original form as transcribed from coding sheets, usually onto punched cards, is acceptable as an input and can be compiled by the processor provided in the system to produce either machine code or some condensed form of symbolic or relocatable code which can be quickly absolutized for execution. On a later run, this condensed form of code is also an acceptable input, perhaps with modifications allowed at loading time. Numerical or even alphabetic input data is also allowable. To be truly effective, an operating system should also permit several jobs to be stacked for continuous processing. Thus the complete set of inputs to a particular run may involve a large amount of data of various kinds and in various stages of refinement. The compiler or assembler is itself considered one form of input translator and a package of data card scanning, conversion and packing routines, another. Since a great deal of processing is required before a program is ready to be executed, it is usual to do all this processing (compilation, data translation, modification, etc.) on one pass of the input and to prepare a mediary input tape containing the material for all the jobs to be processed in a refined form. This mediary tape is then played back and the jobs run in succession, producing output which is commonly stacked on a mediary output tape. At the end of all the jobs the mediary output tape is played back and the final output for printing or punching prepared by processing it. All this is further complicated by the necessity for master data files or special inputs and outputs for various jobs which are handled by the object program during the execution phase, that is, separately from the regular input or the final output.

The difficulty with the input translator is in providing communication between 1) the compiler which assigns absolute locations and sets up linkage to the scanning and conversion routines within the symbolic code, 2) the symbolic code itself which, at execution time, will call for certain data to be loaded into certain locations, and 3) the input translation routines which must convert the input and stack it in such a way that its eventual location can be determined. In specialized systems this difficulty can be overcome by fixed rules and conventions regarding the nature and type of data acceptable. In a general system this is difficult to do without severely restricting the flexibility of the whole complex.

There is somewhat the inverse problem connected with output translation but it is less severe since the generation of the output is a function of the executed program. At worst, it is necessary to carry large amounts of control information through the system in order to allow ultimate preparation of elaborate reports. In the case of input, however, control information is really not available at the time when it is needed. For jobs involving large files of data and heavy report requirements, this whole situation is alleviated by the use of data processing program systems.

The function of an I/O Monitor is to act as a universal Input/Output control which recognizes pseudo commands and then executes the necessary machine commands to carry these out, keeping track of the status of all such commands from request to completion. Presumably, if the Input/Output controls for computers were built properly the I/O Monitor would exist in the hardware. Some of the newer machines seem to be tend-

[26] There are several variations of this. In some machines any instruction can be so flagged with a special bit or digit in the word; in others, a particular address can be preset with dials so that any reference to that address within a program causes a special action, etc.

[27] This is within the scope of operating systems as meant here. A general solution is possible in a wider context but the practicality still depends on the use to which a particular computer is usually put.

ing in this direction; however, it is difficult to build the full generality required for all types of work. But machine designers and system programmers have a great deal yet to learn about the problems of buffered machines. These machines, which have been in use now for nearly two years, have opened up a whole new world of concepts which we have hardly begun to explore.

As an example of the kind of difficulty which has arisen, consider the IBM 709 which is a typical buffered machine. This machine can be equipped with up to six data transmission channels, all of which can be loading or unloading high speed storage while computing is going on in the arithmetic unit, which also refers to storage. It is sufficient to consider only two channels. A channel may be activated by selecting a unit, such as a magnetic tape, attached to it. To insure that transmission of data has been completed before the program makes use of it, instructions are provided which effectively delay until channel transmission is complete. The program can, of course, use some of this time for internal calculations and, in fact, this is the whole purpose of buffering. Suppose now that one channel has been thus activated and that subsequently the second channel is activated (Fig. 1). Suppose further that the

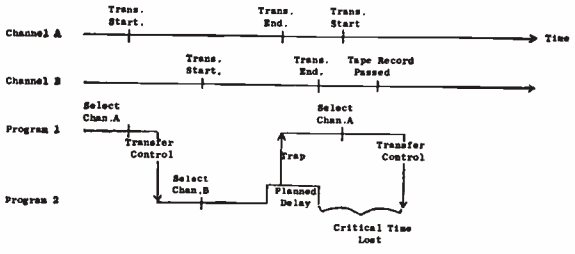


Fig. 1

internal operation must ultimately be delayed until the second channel has completed its function. Now if the machine is also equipped with a data channel trap and the first channel completes transmission during the time that the delay is occurring for the second channel, the program will be interrupted and control transferred to a system routine which proceeds with waiting instructions for the first channel. By the time this has been completed and control is returned to the delay instruction, the second channel may have completed its assigned work and passed the point in time at which additional commands are acceptable for the desired purpose. It is clear that, if the two channels are being controlled by separate programs which were not written in conjunction with one another, complete confusion can result. The only way out of the dilemma is to centralize all the physical I/O transmission commands and have the normal routines make I/O requests in some interpretive scheme. Even more difficulties can arise when one channel can handle tapes of different speeds and/or densities so that timing loops cannot rely on completion of logically preceding operations without explicitly testing for it. It has been found, for example, that some I/O loops which operate perfectly on the IBM 709 will not operate correctly on an IBM 7090 using tape units of mixed speeds. Such considerations are considerably more subtle than those to which programmers have been accustomed in the past.

Still another feature provided by some operating systems is a subsystem for debugging. Many schemes have been devised over the past decade, both in hardware and in programs, to assist the programmer in checking out his routines. None of these have been completely satisfactory though perhaps it is foolish to expect an ideal method. The heart of the problem is that the routines being checked out have to be modified themselves in order for information concerning their progress to be output. Three forms of debugging routines have long been in use. The oldest, simplest and one which is still widely used is the memory dump. A skilled programmer can make effective use of such a service routine but, if employed without careful planning, a memory dump routine can produce a very extravagent amount of printed material. In any event, a memory dump provides static information after the fact. By the time it is used, the important information may have already been destroyed in high speed storage.

In order to give dynamic information, tracing programs were written many years ago for several machines. They are in effect simulators which simulate the computer on itself. Although complete information on the progress of a program can be obtained (except in certain special cases involving input and output), they effectively reduce the speed of computers manyfold and have been all but abandoned for this reason. Besides, they do not lend themselves to use in conjunction with another elaborate system.

A compromise between these two is the "snap" tracer which has been used quite effectively. A snap tracer usually consists of three parts; a set-up routine used either in conjunction with or as a replacement for a load program; the snap routine itself which outputs the required areas of storage, unedited, during execution of the program being tested; and an output translator which edits the snap information and prepares it for printing in a readable format. The method used is somewhat as follows: before actually loading a routine, special snap instructions are loaded which specify at which points in a program information is desired and the location in storage where this information will be found. These snap instructions are then retained in tables during the actual loading of the routine. After the routine is loaded, the appropriate instructions in the program are replaced by transfers to the snap routine which is left in memory with the program to be tested. This is a form of program induced trap. When the traps occur, the requested information is output to a scratch tape. At completion of the run, the output translator takes over and edits the scratch tape to a form suitable

for printing. Here again there are three difficulties. First, there must be room in memory for the snap routine itself; second, the inserted transfers for the traps must not occur at logically inconsistent points in the program under test and, third, it must be possible to operate the snap routine within the over-all operation of the system of programs in use. The last point involves more than mere memory allocation. For example, since operating systems are designed for continuous automatic running, it may be next to impossible to interrupt the system for operation of the snap routines.

Since the snap tracer has proven to be the most effective debugging tool in spite of the above limitations (and the additional one that they usually refer to everything in terms of absolute locations) the notion has been elaborated and incorporated within operating systems so that snap instructions can be coded in-line at the time the program is written. Since an operating system requires room for its own various programs, it is then necessary only to allocate additional storage at the outset for the snap routine and to make the formats of the output compatible with the system's output translator. By making the snap instructions processable by the system compiler, debugging can be done at the symbolic level rather than at the absolute level.

Tremendous amounts of manpower have been employed on operating systems in the past few years. Some of the results have been excellent; some have been disappointing. The basic idea, however, has been employed in a variety of special applications and it is now an established technique which will undoubtedly continue to be used and improved in the future.

Dual Master-Operating Systems

When C-E-I-R undertook to program the LP/90 system referred to above, a survey of the compilers and operating systems available for the IBM 7090 failed to disclose one that seemed adequate to all the requirements. The basic idea of an operating system was a necessity but the demands of LP on both machine time and machine components was so great that the inefficiencies of existing systems could not be tolerated. There have been similar disappointing experiences in writing other large specialized systems and thus it was decided to take a whole new approach to the systems concept. What was felt to be needed was a good machine language compiler together with a library of coordinated routines, which could be readily updated, plus a good operating system which would make the execution of LP runs efficient and easy to control. It should be recognized that the LP routines themselves compile data and allocate memory on the basis of the size of the immediate problem and that these runs vary from job to job, depending upon the analysis desired. A careful review of the requirements for compiling and for execution of the routines showed that these two functions were different enough that combining them into one grand operating system introduced needless complexity and inefficiency. At the same time, however, the LP routines need to reflect the latest changes in the library without unnecessarily complicated systems maintenance procedures.

The result of all these considerations was a dual system consisting of a master system which was self updating and an operating system which is a by-product of a compile run. The whole complex which finally evolved is illustrated in Fig. 2. The modification of the

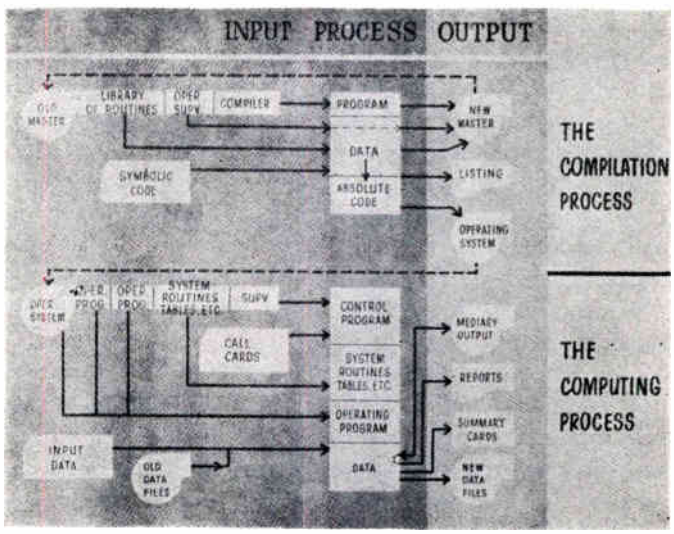


Fig. 2

master system is treated much like a file maintenance run. The compiler contains a master control which reproduces the compiler onto a new master and also relays a copy of the operating supervisor both to the new master and to the new operating system. The library of routines, symbol tables, communications regions, etc. which are also on the master tape, are then read in and modified as required by new symbolic code which is treated like a detail tape. As the library is processed it is written out onto the new master in condensed symbolic form and onto the new operating system in absolute form. At the completion of the compile run the new operating system is then ready for use. It is controlled by the supervisor and is activated by call cards by which the operating system can be programmed for a particular run. This operating system will then be the standard one in use until such time as further modifications or additions are desired in the system. Then a new compile run will be made, producing a new operating tape.

There is nothing unique to LP about the master system except for the particular operating supervisor which is carried. This same idea has been carried over into a more elaborate general system which is nearing completion at C-E-I-R. Experience to date indicates that this general philosophy is a very useful one and it is expected that much further work will be done along the same lines.

The organization of the routines within this system is also of interest. There are two classes of routines called systems routines and agendum routines. The former are routines which are felt to be universally useful and which are kept in core at all times during execution. The agendum routines are individual master programs which can be brought into storage by call cards and which overlay one another.[28] It has been found that a third class of routines are required in a general system. These may be called modular routines and they are never put into absolute form until they are called for by an agendum routine (during the compilation process). The modular routines are thus essentially relocatable library routines although the original symbolism is retained in tables on the master system. It appears that these three classes of routines are sufficient for very general requirements. Modular routines may also be prepared by preprocessors which translate a data processing language or other forms of coding into input acceptable to the compiler. In this way references can be made anywhere in an agendum routine or in modular routines at the symbolic level.

One advantage that has resulted from this classification of routines in a more dynamically useful debug subsystem. In addition to systems routines and modular routines, ordinary subroutines within an agendum routine can be linked via a transfer vector. Since the convenience and power of using this hierarchy tends to promote well designed programs, it is sufficient in most cases to restrict debugging traps to entries into various routines. This is readily controllable through the transfer vector and paths through the program can be defined by sequences. Hence a debug system can be a part of the operating supervisor and still allow tracing at a limited symbolic level. No change need be made in any vital part of a program and debugging instructions can be prepared at any time for use on an operating run. Although the printed output may not be as completely symbolized as would be the case if the debug instructions were processed by the compiler, it is nevertheless very flexible and convenient. Since the programmer presumably has a well annotated program listing available during checkout, the lack of complete symbolic references can be dismissed as an unnecessary luxury. The important thing is that it is possible to interrupt the progress of a complicated system at almost any critical point by easily prepared call cards.

It is hoped and expected that further experience with systems of this type in the near future will disclose still other advantages and capabilities. It already seems evident that the separation into master and operating systems unravels a lot of the logical maze in which other over-all systems have bogged down.

[28] The word agendum was chosen since the specification of a series of these routines determines the agenda for a particular run.

Processor Compilers

A notion that has been considered for the past several years is that of a compiler for writing compilers. While it is true that assembly programs are commonly written in their own language and that compilers are sometimes written in a subset of their own language, so far a true compiler or generator for writing compilers has not been achieved. The SHARE UNCOL Committee[24] which has received considerable publicity, has undertaken much study along this line but their interest has been primarily in a processor which could prepare compilers for different machines. If one is willing to restrict himself to a single machine or close family of machines then it appears that the dual system described above may be extendable for this purpose. It should be noted that in treating a master system as a self-updating file, families of master systems are created automatically. In fact, one of the additional burdens imposed by the dual system concept is in keeping track of these various trees of systems. As described above, such a master system does not work on its own compiler but only on its own library. However, there appears to be no logical difficulty in extending this idea backwards so that the compiler can act as a generator on itself. This would lead ultimately to some minimal compiler or generator from which all other compilers, within a fairly wide scope could be derived. Perhaps once this were done the problem of changing from one machine to another or of preprocessing different source languages might become more tractable. In any event, this appears to be a fruitful source of study and development in the immediate future.

Emerging Techniques and Principles

Other special system developments could be discussed but enough has already been covered to allow certain general statements to be made.

First, it appears to this writer that the experiences of the past several years have well established or reemphasized the following principles:

1) The introduction of new ideas and new applications is an inherent part of Electronic Data Processing (EDP) technology, both in the manufacture and in the use of equipment. Some of these new ideas and applications have far-reaching logical implications. Programming analysts need to anticipate this and devise techniques which are adaptable. No worthwhile job is ever really finished.
2) Since the handling of information involves the generation and manipulation of information about information, data handling requirements can grow without limit unless carefully constrained. The constraining force must be personal and organizational discipline, which implies a willingness to work within well-defined rules and procedures.

3) Nothing can be mechanized which cannot be precisely defined and this definition must be simple enough to allow familiarity to be achieved. It is a delusion to suppose that a complicated machine can be made more usable by superimposing a system which is even more complicated to use.
4) A wide variety of skills are involved in present-day EDP applications, thus multiplying the problems of communication between people. Since we are dealing with complex man-machine systems we must provide for quick and easy communication if their use is to be profitable.

If these seem slightly antithetical, it only emphasizes the challenge facing system designers.

Second, the following types of routines and techniques have proven their worth and are sure to be developed further: operating supervisors, central I/O monitors, data file directories, pictorially coded report generators, formula translation precompilers, sophisticated organizational compilers and specialized applications languages.

Third, two observations seem in order about changing attitudes.

1) The notion that a universal processor can be developed even in one field is being abandoned. It is beginning to be realized that "languages" develop around applications and that it should be possible to integrate such languages into suitable processors and operating systems. The idea, for example, that a data processing language can be limited to 16 kinds of statements, or 24 or 50 or any other fixed number, is beginning to appear absurd.
2) Although experience with omnibus processors has been disappointing in some cases, new processors are continually needed and ways must be found to make their preparation easier. There is considerable current analysis of the logically distinct parts of these complex programs which, it is hoped, will soon lead to more standardized systems work, as opposed to standard systems.

Finally, it appears that two major areas need to be carefully re-examined. One has to do with reprogramming, which has become a bugaboo. Too often the expense of newer equipment is justified without adequate thought being given to the problem of conversion of existing procedures. Ways are then sought to get by with a minimum of effort from the programming staff. Often this leads to the use of generally available routines which may be quite unsuitable to the job at hand and can lead to the continuing of inefficient procedures, simply at added expense. If sufficient effort is devoted to the preparation of a suitable processor and if the staff is properly educated both in its use and in the over-all job to be done, then the use of the new equipment can be made truly profitable.

The other area is the use of buffered machines and systems built on the input-compute-output philosophy. It is unfortunately true that some procedures do not lend themselves well to buffering and that the running time of others may be independent of internal computing speeds. Unless standardized techniques can be developed to make the use of highly sophisticated equipment easier, then the computing field is in danger of experiencing a severe technological lag. The new concepts and logical complexities which current time sharing equipment is posing are different in kind from those which programmers have grown accustomed to. Whole systems concepts can be invalidated in going from a sequential machine to one with functions overlapped in time. Some of the equipment about to come out time share not only the input and output but the actual execution of instructions. The fact that this newer equipment can be programmed fail-safe is beside the point. There is little purpose in paying more money for more complex equipment only to gear it down to speeds which make its operation more costly than its predecessor. With regard to program systems, it is beginning to be evident that input and output are inseparable twins and that the compute phase should be a subroutine to an over-all data handling system rather than an interposed phase on a coordinate level. From a systems view, mere arithmetic is of minor importance.

One emerging philosophy that appears to be very promising is that of a large central computer with relatively inexpensive satellite equipment tied to it. Although long range transmission equipment is on the way which will facilitate this, the real problem is one of over-all systems organization. Even now the delays induced by remote use of a computer may be minor compared to the procedural delays which occur right within the computing center. All of the systems skill and experience gained in the past few years need to be brought to bear on this problem to insure the continued development of the computing field.

Advanced Computer Applications*

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Since new applications of computers are cropping up at a remarkable rate, many readers may not be aware of some of the new and interesting jobs this machinery is performing. W. F. Bauer and his associates have been asked to survey this huge field of activity and select several applications felt to be significant, describing these briefly in such a form as to be useful reading for the nonspecialist.—*The Guest Editor.*

Summary—**This paper views applications which hold a promise of becoming important commercially, as well as many which are simply interesting and unusual.**

A number of important applications are appearing such as language translation, the computer as an aid in medical diagnosis and applications in the fields of education, music and history. Applications in government vary from a proposed simulation of emergency duties of the President of the United States to the evaluation by computers of bids for government contracts. Other applications include computer control of railroads, steamships and space vehicle tracking. Computers in communications are being used in speech compression and message switching. Computers in automobile traffic control show promise. Industrial process control on a large scale is also promising.

In addition to a general applications survey, this report describes four application areas in some detail: communications, automobile traffiic control, language translation, and industrial process control.

Introduction

THE digital computer is an information handling device which does not directly reflect, in most cases, the application to which it is applied. It is this universality, unparalleled in modern technology, which gives the computer such a broad base of application.

There is special challenge, therefore, in writing a paper on computer applications. We cannot hope to cover every application which would lie within every definition. For these reasons, it is necessary to spend a few paragraphs discussing what is meant herein by "applications."

We shall omit, for the most part, applications commonly referred to as "scientific" and "business" in which there is intrinsic interest in the mathematical equations, or in which there is mechanization of the standard data processes. These were among the first computer applications and therefore tend to be less new and less unusual.

We shall not discuss computer techniques (programming, mathematics, problem formulation, etc.) except as they are important or peculiar to the application. Nor shall we discuss applications of the computer to recreational games such as bridge, checkers, or chess since the principal value of such applications is the development of techniques (such is covered in this issue by Minsky[1]).

It seems extremely difficult to classify applications, and only a rough classification will be attempted herein. Rather, we shall present a potpourri of interesting applications which have been called to our attention through search of literature and discussions with prominent people in the field. In addition to brief sketches of many applications, we shall provide some detail in the areas of automobile traffic control, communication systems, language translation, and industrial process control. These, we feel, are of considerable interest and importance.

We shall deal only with applications of the stored-program digital computer. We will not attempt to cover the many applications of computer components in the implementation of various systems of instrumentation, etc.

It is our opinion that an application becomes a good candidate for discussion within our framework if it has a degree of newness and importance in the field. Unusual applications which hold a future promise of becoming important commercially are especially interesting. In fact, it appears that the most important contribution of a paper on interesting applications is to point to new and rapidly developing areas of application which will be important in the computer field, will have influence and impact on other disciplines, and will have some weight on the national economic and technical scene.

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[1] M. Minsky, "Steps toward artificial intelligence," this issue, pp. 8–31.

Literature and the Arts

Although computers are usually associated with precisely formulated endeavors of our culture, such as the sciences, they are now used successfully in literature and the arts. Although the applications are not numerous, several are interesting and show signs of commercial importance.

Language translation is an unusual application in this area. Since it promises to be an extremely important application, we have devoted a special section to this subject.

Although computers are in use in almost every large college and university, they are not used as direct tools in the education process. We know of no use of computers as a direct educational tool on a practical day-by-day basis. However, in a research project called "The Automated Teaching Project" (a),[2] the computer directs the display of instructional material from slide projectors and determines sequences of diagnostic questions. The student can indicate answers by means of typewriter input, and the computer, in turn, can tell the student how correctly questions are answered. It is clear that teaching machines will come into greater use; the digital computer is obviously well suited to this application.

The computer is sometimes used as a supporting tool in the education process. At Purdue University, for example, computers have been used in scheduling classes [1]. Starting with the students' total schedule requirements, the computer investigates all of the schedule combinations, and purportedly arrives economically at a schedule which fits the students' needs and a collection of schedules which are generally error-free. A similar kind of project (b) employs a computer program to prepare time tables for Toronto high schools. The input is a set of classes and a list of teachers who are to teach given subjects to these classes. The computer prepares the timetable, which takes into account a great many restrictions and indicates the time and place for teachers to meet these classes.

Perhaps some day the digital computer will be used to teach children reading, writing and arithmetic. A step in this general direction has been taken in the preparation of computer programs for correcting spelling errors [2]. In this application, the computer checks the spelling with correctly spelled associated words which are stored in its memory.

Important strides have been made in various training applications. The general purpose aspects of the digital computer make it ideal for use as a control element in training devices where an environment or action is being simulated. A good example of this is the use of the digital computer as the control element in an operational flight trainer [3]. Although the computers used in such trainers have been traditionally analog, the flexibility of the digital computer in changing from one airplane model to another in the flight trainer makes it attractive for this use.

Computers have served literature and history. Scholars have used computers to prepare Bible and poetry concordances in the detailed study of literary works. Also, the computer has been of considerable value in analyzing the Dead Sea Scrolls [4]. Historians will undoubtedly find additional applications of this type.

In the musical arts, the computer has been used in a facetious way to play simple tunes by amplifying certain internal signals, mostly as a public relations stunt [5], [6]. However, more serious applications of the computer in music are appearing. The computer can analyze a musical score, perform such manipulations as changing keys, and can write original compositions. These areas are explained by Hiller and Isaacson [8] in their book on experimental music. Also, in England a project is underway for applying computers to the problems of change-ringing on church bells [7].

Of considerable interest is the use of the computer to design weaving patterns. Fig. 1 shows an example of a pattern generated from random numbers (c), described as "four harness overshot, wove as drawn, with a half repeat length of 20 blocks." The pattern was recorded

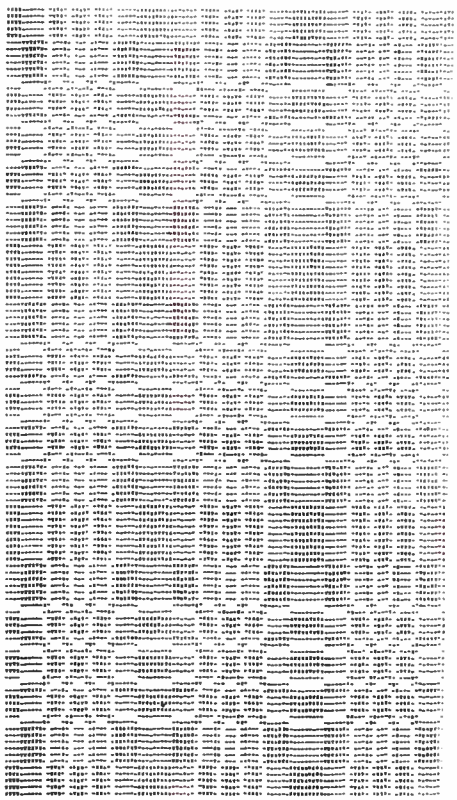

Fig. 1.

[2] Letters in parentheses refer to the Reference at the end of this paper. This Reference is a list of people from whom information can be obtained concerning the application mentioned. We are indebted to these people for calling the applications to our attention.

from a high-speed printer and photographically reduced. Some would say that computers have now turned "full circle": one of the earliest known applications of punched-card-like devices was the storage of "programs" for weaving patterns in the Jacquard loom, over a century and a half ago.

Applications in Medicine

One of the most promising applications of the future is in medicine. It is clear that the computer will be used for every day medical practice. One of the most obvious uses of the electronic computer in medicine is that of evaluation of statistics and retrieval of information as a diagnostic aid. In order to attain fruitful use of the computer, much statistical data must be developed, and considerable operations research must be performed on the use of such data in medical diagnosis [9]. Recently a comprehensive seminar [10] was devoted to storage and information retrieval techniques in medicine. Also, a report by Crumb and Rupe [11] indicates some of the problems and techniques in diagnosis. One research firm is sponsoring a research effort called "Project Medic"(a) to study methods for relieving the practicing physician of many routine tasks of collecting, storing and retrieving patient data.

Another use of computers in medicine is in specialized applications in which signals collected from electronic measuring devices are analyzed in detail. Examples of these are the analysis of electroencephalograms for the diagnosis and understanding of brain diseases or symptoms which show up in the brain. Work has been done by Stark (i) on detailed analysis of neuromuscular actions, such as the examinations of the iris of the human eye as a servo system. Also, the National Bureau of Standards has performed some research [12] in a technique for analyzing electrocardiograms. In this application, the data is recorded as an analog signal and converted to digital. The aim of this application is to improve procedures in diagnosing heart ailments by means of a detailed digital analysis of the heart beat cycle.

Business and Government

Since 1960 is an election year and since the cold war continues, new and unusual applications in politics and government are of interest. A paper has been written [14] on the unusual operations of simulating the emergency duties of the President of the United States. Such possibilities of using a computer come to mind since the number of facts on which to base decisions on incipient war is increasing, and the length of time in which to make these decisions is getting shorter. Computers are being used for election forecasting [15], [16], and perhaps some day the forecast may be so accurate and so fast that it will in itself affect the election outcome, in view of the time differential between the east and west coasts.

To help the U. S. Navy carry out the function of monitoring one of its large programs, the Polaris submarine intercontinental ballistic missile project, program evaluation review technique, (PERT) was developed [17]. In this application, the computer is used as an aid in evaluating the progress of the many contractors in the Polaris program to determine milestone slippages and complex interactions between various phases of this large-scale project. In a similar area, there has been a project [18] to have a computer evaluate proposals from industrial concerns, and select the best bidder. In this application, procurement bids are evaluated involving multiple bidders, the prices of the bid, quantities, and delivery schedules.

We have seen many applications of computers in the area in which scientific techniques are of a direct concern in business activities. Examples are the use of the computer in civil engineering [19], [20] operations such as the analysis of cut and fill operations in highway construction.

Computers will have a profound effect on our economy in optimizing designs in various activities dealing with discrete items (vehicles, telephone trunks, chemical formulas, etc.), which occur in large numbers of combinations and which must be examined and enumerated in manifold ways. An example of an application to one of these combinatorial problems is the assignment of telephone facilities [21], where there is a complex problem of matching available trunk lines to desired subscriber service. Computers have also been used extensively in the study of automobile traffic [22]–[24], as in the analysis of traffic origin and destination data, forecasting of future traffic patterns, and simulation of traffic on existing or planned facilities. The farmer has found computers useful for selection of corn hybrids [25].

Nor has the lawyer neglected the possibilities of computer use (e); some legal applications are in the areas of patent search, statute search, and decision search. Also, architects have used the computer in the design of buildings [26].

An interesting application in the chemical field is the computer analysis of chemical structures [27], [28]. With topological classification of structures of organic chemical compounds, similarities and other relationships between compounds can be left to the computer, thus enabling decisions concerning commercial chemical compounds for various purposes to be reached faster and more economically. Another application is in analysis of sociological structures (a). In this application, the computer is programmed to operate in ways directly analogous to the operation of large social groups. It is stated in describing this application that

"at intermediate nodes in a command pyramid of a group, simulated individuals and coalitions of these can make personal demands for specific policies for success in status and for monetary rewards."

We have been told (g) of a computer program to generate combinations of keys for manufacture. This involves the generation of all possible combinations of keys subject to certain rules such as the width and height of adjacent tumblers. In similar vein, at the National Bureau of Standards (f) the large number of signal wires in the PILOT computer were given reference names by a computer program. This required the generation of pronounceable four-letter words by the computer.

The gambling industry too has made use of computers in some of the most unusual applications about which we have heard. Computers have been used for some years to compute the division of the pari mutuel pool at the close of the race in Los Angeles. In Las Vegas, a computer is on public display and in use at a gambling casino for the entertainment of, and perhaps practical use of, patrons (k). The computer is used for public relations and as a showpiece but also performs some practical business accounting for the casino. Its more purely entertaining applications provide the patrons with horoscope information and the determination of the movie star who would be the most appropriate mate for the patron, in view of his looks, personality, etc. But the more "practical" applications consist in determining the probabilities in black jack for winning or losing in certain combinations and for the strategies of "standing," "splitting," and "down and double," in each case depending on the dealer's "up card" and the gambler's count. Also, the patron can determine the odds of certain combinations in roulette and craps.

The most personally consequential unusual computer application is one in which salary recommendations in an organization were made by the computer. In this application (d) the computer was presented various facts about professional employees and was programmed to answer questions on salary, including the amount of the next raise.

On-Line Applications

The "on-line" applications which we have in mind here are those in which the computer is closely related or directly tied to a processing activity and performing work which is related to demands occurring in real-time. Included as a special case of this are real-time applications and control applications. We use the phrase "on-line" instead of "real-time" since there seems to be an applications area which does not fall into the real-time definition. For example, the control of an airplane is definitely a real-time problem but the calculation of the raw materials mix for making concrete, which is performed whenever necessary, is not, in a strict sense, "real-time."

The first on-line applications were military in nature. The SAGE System (29), which was very ambitious for its time, was one of the first such applications while other, more specialized, computers [30], [31] were developed for airborne applications and for ground based missile guidance. In modern weapon systems and in missile guidance, airborne or ground based, there are almost no exceptions to the use of the computer as the central control element. The use of computers in military systems is expanding. The U. S. Army has a plan for using computers at all levels of the field army [39] from the Company up to the Army level, and is developing computers and communications systems for this purpose. In military applications, generally, the computer is being used for intelligence, attack warning data processing, and for the command and control of military operations. In fact, the usage of computers for these purposes has reached such a high level that many responsible people [36] have been worried about the "destruction of civilized existence by computer controls."

One of the most interesting and important applications is that of the control of industrial processes. In recognition of the importance of this general topic, we have devoted a section below to this purpose.

Air transportation makes several uses of computers. The application of computer techniques in airline reservation systems is not particularly new. However, this is a growing field, and in some cases [32] general purpose computers have been designated for this task. Computers have been used experimentally in air traffic control [33], [34] and an extensive development program is under way for computers which will handle data for flight plans, for processing data for possible flight plan conflicts, to aid human airways monitors in the solution of special traffic problems which arise, and for the data handling problems which arise in terminal area traffic control. As another example of the use of computers in the airplane industry generally, we have mentioned above the application of computers in flight training devices.

In a related field, general purpose computer techniques are being used to check out complex electronic systems. A computer has been developed [40] for the purpose of examining internal signals and the general electronic status of a missile guidance electronic system. The use of such computers to check the status of complex equipments automatically will undoubtedly become commonplace in the years to come.

An important and new application of computers is in the control of commercial vehicles used for the surface transportation of persons and goods. Automobile traffic control by computers is very new, and we have devoted

a special section to it below. In London, there has been a project for the control of trains through prepunched tape [38]. In Russia a special-purpose digital computer has been built for train control [37]. Metropolitan rapid transit vehicles are considered a likely candidate for computer control. Also, we have heard (h) of a project which will soon result in digital computer control of ships passing through the Panama Canal. In this application, the computer determines the spacing of the ships and computes velocity commands which are transmitted to the ships. The capacity of the Canal is thereby increased significantly.

The control of industrial instruments is recognized as an interesting application. Starting from a research project at MIT [41], machine tool control by computers is becoming widespread. The use of computers for the control of instruments generally is broadening. For example, a project is under way (j) for the real-time computer control of television equipment during a broadcast.

Computers are being used in unusual ways in space technology. Computers have been used for many years for data reduction and for the scientific study of ballistic and space vehicle systems. Also, computers are important as control elements in these systems. When Sputnik I and the first American satellites began circling overhead, computers were used to precisely determine their orbits [42]. A more unusual application is in real-time tracking of space vehicles, since frequently a control function is performed in the firing of retro-rockets, the switching of instruments, etc. The Air Force, for example, has an elaborate scheme for obtaining data from tracking stations throughout the world and processing it in real-time during a space probe shot [43]. Data are received from tracking stations currently tracking, elaborate computations are performed to refine the knowledge of the orbit, corrections for time and distance are made, and the positions are transmitted to stations which cannot currently "see" the vehicle because of horizon limitations. The refined orbit data are also used to determine such control functions as the firing of retro-rockets, and to provide the injection of the vehicle into a special orbit. This system has been used on Air Force probes Pioneer I, II and IV.

The preceding paragraphs have briefly described a variety of advanced computer applications. The following four sections will treat, in somewhat more detail, applications in communications, automobile traffic control, language translation, and process control.

Computers in Communications

Several advanced applications of computers are developing in the field of communications. This applications area will probably prove to be one of the biggest commercial areas in the coming years. Computer equipment is finding use in the preparation of data in special ways for transmission over communications facilities and the processing of messages to provide the routine "housekeeping" operations or the control operations of a complex communications network.

Although mostly in the experimental stage at this time, the compression of human speech by digital techniques is a new and important application. The process is essentially one of performing an analog-to-digital conversion of recorded speech sounds. Several techniques are employed, one being the counting of zero crossings. Since the information content in human speech is low compared to the nominal information rate implied by the bandwidth used in human speech to produce the sounds, it is theoretically possible to compress the bandwidth through digital encoding. Following this compression, the resulting digital signal is sent over a less expensive communications facility, that is, one which handles the lower bandwidth. The signals are then reconstructed at the receiving end for the formation of an analog speech pattern which can be recognized by the human ear. One research effort in this area is an example of the application of a stored program computer [45]. The future will probably see specialized devices designed and built for this speech compression purpose.

A similar application in communications is the compression of English language words by computers prior to transmission, again with the purpose of lowering required communication information rates and bandwidths. This technique is based on the redundancy of letter combinations in the English language (a "q" is always followed by a "u"). A stored program digital computer encodes the words and removes the redundancies (l). The words are transmitted, and reconstructed at the receiving end. The encoding process consists essentially of making a dictionary which lists the economic bit pattern for the representation of words. The reverse process is performed at the receiving end.

A fascinating application of computers in communications is in switching in complex networks. Two different applications or processes must be distinguished: message switching and circuit switching. Circuit switching is the simpler problem and is solved adequately by the cross bar switch of the modern telephone exchange. Although there are some problems in routing in the commercial telephone business, current designs are relatively straight forward, and there is no need for complex computer applications.

Message switching requirements are developing rapidly in government and military communications systems like UNICOM, 480L and ComLogNet. The requirements now being recognized in these systems will be seen in the future in commercial communication sys-

tems. Indeed, the commercial facilities may be shared extensively with the military facility.

Message switching makes use of control information which accompanies the message. At the switch point, the computer decodes the control information and causes appropriate action to be taken. One of the big advantages of the application of the stored program digital computer is immediately apparent: flexibility is obtained through being able to change the function of the computer as procedures change, simply by changing the stored program of the computer.

Communication systems of the future and systems now under design for the military require that a great amount of control information accompany the message: the routing of the message, priorities, security classifications, format, message source, and addressees. Typically, 100 characters of a 250 character message are devoted to this kind of control information. Furthermore, many functions need to be performed: error detection, error correction and translation from one format to another. Future commercial communications schemes may require that all this information be handled. Furthermore, there will probably be need to perform an accounting of the use of the communications facility by the various customers. A stored program computer is, of course, ideal to handle all of these jobs.

A computer is being built for the purpose of message switching in a communications system [44]. This computer is being built for the SAC Control System under Air Force Project 465L. The computer is multi-sequenced, having 256 control counters which enable the rapid time-sharing of the computer among 256 independent programs. The design follows to a great extent the design of the TX-2 computer development at MIT, which has a smaller number of control counters. In the communications computer, the 256 control counters correspond to activities on 256 communications channels. As a character is presented on any one of the channels, the sequence currently being processed is interrupted and control is transferred to the appropriate sequence counter among the 256. After the complete message is assembled by successive interruptions and transfers of control, the message is operated upon and the appropriate switch action is taken.

The marriage of communications and digital computers is a very natural one. Communications have been serving computers in many ways such as providing remote input sources and inter-connecting computers. Now computers will serve communications as an integral and indispensable part of complex communications systems.

Automobile Traffic Control

While special-purpose analog computers for automobile traffic control have been in use for many years, the use of the stored program digital computer for such purposes is just now coming into being. However, the idea of using a digital computer for traffic control is not new [46].

Digital computer abilities have wide application for traffic control problems. With a digital computer it will be possible to change the mode of operation of traffic signals from time to time, sometimes for instance, operating them in a "fixed-time" mode, and at times perhaps in a "semiactuated-mode" where individual intersections are responsive to side-street traffic. Different intersections may be operated in different modes if appropriate. The entire system can be responsive to traffic demands.

One of the important features is the ability of the digital computer to store a wide variety of programs to take care of special situations. It is entirely feasible to let the computer decide when any special program shall become effective, based on criteria established by the traffic engineer. For example, there should be one or more special programs to handle unusual weather conditions. It would even be possible to have a rain gauge and snow gauge tied to the computer in such a way that the computer can initiate an appropriate program when a given rainfall or snowfall level has been reached. The handling of unusual traffic patterns, such as occur in the vicinity of athletic events, can be an important task for the digital computer. On the day of such an event, for example, the time of the start of the event and the location (if there is more than one location for such events within the area), can be supplied to the computer. The computer, based on stored information of past experience, can set up at the appropriate time the optimum program for handling regular traffic in addition to the traffic going to the athletic event. As soon after the start of the event as the attendance is known, this information can be supplied to the computer for use in establishing the appropriate dispersal program. Progress of the game can also be fed to the computer so that it can estimate closing time and be prepared to handle normal traffic and traffic of the athletic event in the optimum manner.

Eventually it will be possible to program the digital computer to have learning ability and to evaluate experience. In this manner it would be possible to determine if a particular program was especially effective in handling some special situation. If this were the case, information concerning this program can be stored for future information, should a similar situation develop in the future. The handling of traffic around localized disasters such as fires can be an important task.

The Municipality of Metropolitan Toronto (m) is presently engaged in an experimental project to evaluate digital computer traffic control. The equipment at each intersection consists of a standard traffic signal timer to which have been added two relays and a terminal strip. Each approach to the intersection is

provided with a radar-type traffic sensor. Communication between the intersection timer and the central control room is accomplished by telephone lines.

The central control room contains a digital computer plus a communication/monitor unit. For each intersection there is a monitor consisting of six pilot light indicators and a communication module which matches between the telephone lines and a computer. This communication module has a switch which permits the operator to specify whether the computer will take control of this specific intersection, and a pilot light shows whether the computer has taken control. Also provided on the communication module is a counter for each leg of the intersection. These counters provide not only a cumulative visual indication of the count but also an electrical indication which can be scanned by the computer to determine the number of vehicles which have arrived since the last scanning.

The computer presently being used for control is a medium-speed computer with tape units. The computer receives decimal input on 100 leads which include information from the various intersections plus a digital clock which gives the cumulative time to the nearest second. The computer can at the appropriate time switch the control of any intersection from local to central and vice versa. When the computer is serving as a central controller, commands are received at the local intersection timer in the form of pulses to the manual (police) operation circuit.

Subroutines providing various modes of control are stored on tape. Before starting a given run it is necessary to specify to the computer which mode of operation will be used for which intersection and the parameters for the various intersections. The general scheme of operation is to have instructions which will be needed for a particular mode of operation transferred from the tape to the drum.

With the present programs the computer reads the data from each intersection once every two seconds and at the same time emits appropriate control and instructions. To permit the analysis of various modes of operation, traffic data are continuously recorded on tape. The tapes can then be analyzed during periods when the computer is not performing control.

At present (August, 1960) nine intersections are being controlled. It is expected that additional intersections will be connected within the near future.

Language Translation

Among the advanced uses of computers today, the translation of language bears promise of being one of the most useful and interesting [47]–[49].

While present-day language translation efforts have shown remarkable success, they are by no means economical. First-rate professional translation by human beings can be bought at about 1.1¢ per word. Merely to keypunch input for computer translation costs about 2.3¢ per word. Thus, it is probable that machine translation can begin to match costs of human translation only with the development of a successful print reader. Such machines are under development by a number of companies.

Although the details of existing language translation programs vary, the approach generally consists of the following steps:

1) Read a block of input text.
2) Dictionary look-up. This is done on each word where it proves possible. Some translation programs treat punctuation marks as words, others do not. In languages which are highly inflected, dictionary lookup is complicated by the various spellings assignable to the same word. English has shed itself of most of the inflectional baggage once found in Anglo-Saxon, and depends heavily on word order to express meaning. Russian, on the other hand, may have as many as ten forms of the same noun, 25 of the same adjective, and 50 of the same verb.

   Some translation dictionaries are essentially complete. Others are compromise word sets attended by methods for separation and identification of affixes.
3) Missing words and homographs. Certain words may not be identifiable in the dictionary lookup. For these, a grammar code (identification by part of speech) can sometimes be assigned. In one set of circumstances, this assignment of grammar code is correct about 75% of the time. Many words may still be ambiguous as to part of speech and such homography must be resolved by analyzing the context in which the word appears.
4) Syntactic analysis of the sentence. This may yield clues to the identity of a word not locatable, and enable the ferreting out of its correct or likely equivalent in the target language.

   Syntactic analysis is done by various methods. One of these is called the fulcrum method from its technique of identifying the verb first and then looking in both directions for subject and object.
5) Resolve multiple meaning, choosing correct equivalents. The syntactic analysis is of great aid here.
6) Output the translated text. Machine translations make use of a number of output forms. Some may list a number of target language equivalents for a single source language word. Output listing formats are generally separable into either vertical listing, which may be difficult to read, or text style listing. If the target language is English (as is most often the case in present-day work in this country) this listing will read from left to right, like any familiar text. The vertical listing pro-

vides the opportunity to list many other pieces of information alongside the text.

Machine translation is not elegant in its present state of development, but it often yields a surprisingly complete translation.

While machine translation is not yet able to compete at the going cost per word for human translation, its speed and quantity abilities serve to make it in demand, partly as a result of the present market for translation of Russian technical material.

Process Control

Direct control of manufacturing or treatment processes with digital computers is growing rapidly. Each of these applications, to date, has shown a uniqueness and advancement-of-the-art sufficient to qualify it for mention in this paper. However, to do such applications full justice might require several volumes, so they will be described in general here, and one will be described in some minor particulars.

One vital justification for any computer application is economic. The initial cost of process control computer applications has, so far, been well above that of conventional control systems [50]. However, the initial cost of computer control is seen, in applications made to date, to be amply written-off by returns arising from better process control and supervision.

Choosing a process to which computer control may be well suited is not a simple task. Among the ground rules which may be applied with certainty are the following: The process should have large throughput (in terms of product value); there should be material increase in product value over raw material cost; and there should be a substantial difference between present level of operating efficiency and maximum theoretical efficiency.

When the process has been chosen, equations must be developed which describe what the computer is to do. This is usually the most difficult step in planning a digital control system.

With the major control functions defined, one must specify the auxiliary functions, such as logging progress or pertinent quantities related to the process on some convenient sampling schedule.

Procedures must be carefully set down for conducting tests and checks on the process and on the process instruments (to detect failures in these), and further to monitor for process instabilities or hazardous conditions.

Choice of instruments is commonly the next step in setting up digital process control. Standard instruments may serve even those already in use on the process. In other instances, the design of new instruments is required. Some variables may not be directly measured, in which instance they must be calculated as known functions of measurable variables.

The first full-scale process to be controlled by a digital computer is that of oil refining [51]. The plant under control converts propylene, a byproduct of catalytic and thermal cracking units, to high-octane gasoline. In this installation the computer monitors operation of an 1800-barrel-per-day polymerization unit. Updating of the control loop, including reading the 50 temperature, pressure, and flow recorders, takes five minutes. The loop repeats 24 hours a day.

The computer's speed plus its round-the-clock ability make it economical in this particular installation. Human operators are not completely eliminated in this installation. In event of a noncorrectable off-scale reading, the computer sounds an alarm and prints out on its console typewriter. Hence the man-machine communication abilities of the computer are vital in process control, and will probably remain so.

Several applications of computers to process control in the fields of power, steel, and chemical processes are reported in the literature [52], [53], [54].

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Computers in Automatic Control Systems*

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One of the most significant applications of computer equipment is in automatic feedback control systems. J. G. Truxal has been asked to bring this field of activity into focus by identifying the types of computers employed in the role of active controller, establishing major types of control functions, and carrying the reader to the advanced control systems sometimes considered to be one aspect of the artificial intelligence field. The paper discusses the fundamentals of each type of application in a form that is suitable to the general reader and is a useful summary and comparison for the computer engineer.—*The Guest Editor*

Summary—**Modern automatic feedback-control systems are making increasing use of electronic computers as active controllers. The trend from the use of simple electric circuits and elementary analog devices toward high-speed digital computers (or computers employing both digital and analog devices) is accelerated by 1) the rapidly growing complexity of modern control systems; 2) the increasing importance of self-adaptive control; and 3) the development of optimizing control. Recent applications of computer control include the automatic control of boiler operation in an electric generating station, the adaptive autopilots for piloted aircraft, and the automatic control of load dispatching in electric power distribution.**

THE technology of automatic control experienced its earliest rapid growth during the second World War and the decade following. Throughout this period, control-system design followed closely the feedback-amplifier technology so fully developed by Bode and others; design ordinarily involved the selection of appropriate *electric circuits* for insertion within the feedback system in order to obtain satisfactory performance of the over-all system.

During the last five years, control technology has acquired an entirely new dimension. With the development of high-speed flexible digital computers of attractive size, power consumption, and cost, the control engineer is able to utilize computers as elements of the feedback system. Integration of a computer (whether special-purpose or general-purpose, purely digital or hybrid analog-digital) into the classical controller circuit permits the control-system designer to expand his activities in three important directions:

1) The control of complex systems,
2) Adaptive control,
3) Optimizing control.

The following sections discuss in turn each of these three aspects in an attempt to delineate the class of control problems which become amenable to solution when computers are admitted as control elements, and to discuss the requirements placed on the computer for the control application and the probable future directions of development of this control-computer technology. In each case, examples are cited of current applications of computer-control concepts.

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Control of Complex Systems

During the second World War, interest in automatic control focused on systems for the position control of radar antennas, gun mounts, or aircraft-control surfaces, or on the remote indication of position. During the decade following the war, control technology witnessed the rapid extension of these concepts of electromechanical control to such areas as the automatic positioning of materials in a production line, the measurement and remote indication of instantaneous variables (*e.g.*, temperature or pressure) in an industrial process, and the programmed control of the position of very large mechanical loads (*e.g.*, radio-astronomy antennas or hydraulic presses).

Throughout the early years of the rapid growth of automatic control, the majority of the systems with which the control engineer was concerned could be described by the block diagram of Fig. 1, or by a slight modification or complication of such a diagram. In this configuration, the block G_P represents the process to be controlled: in the antenna-positioning problem, the motor and the antenna load. The output C is measured by the sensor to generate the feedback signal B. The comparator effects a comparison of the input R and B, with the difference constituting the error E. Again, in the antenna-control system, the sensor would be selected to measure C with as great an accuracy as possible (*i.e.*, ideally B equals C). R is the desired antenna position (the target direction if the system is tracking), and E measures the difference between the desired and the actual antenna positions. This error E is modified in the

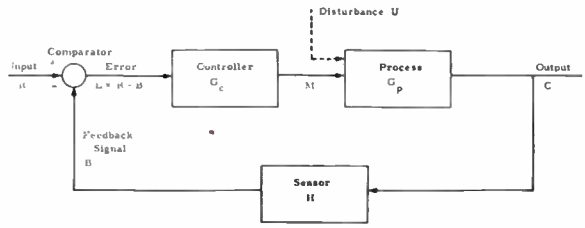


Fig. 1—Classical control system.

controller and then used to actuate the process in such a way as to reduce the instantaneous error toward zero.

Thus, in the very simple configuration depicted in Fig. 1, the designer is required only to select the controller G_C; with this selection, he must satisfy both static and dynamic performance specifications. In the usual case, he must determine an over-all system which simultaneously

1) meets the accuracy requirements with the expected input signals;

2) performs satisfactorily even when the characteristics of G_P change with age, environmental conditions, or signal levels;

3) performs satisfactorily even when disturbances (or unwanted signals), such as U in Fig. 1, enter the system at internal points (*e.g.*, gusts of wind on an antenna, vibration in a mechanical positioning system, or supply-voltage variation in an electrical system).

As a result of these conflicting requirements, design is always a compromise.

The important aspect of such control-system design, however, is the relative simplicity of the problem; essentially the designer seeks only a relation between M and E. If the system is to be linear (and both process and sensor are linear), the designer seeks only the transfer function $M(s)/E(s)$, or $G_C(s)$. If the conflicting specifications described above cannot be satisfied with a linear controller, the designer may have to turn to a nonlinear device. In any event, there is little reason to consider the possibility of incorporating a digital computer as the controller.

Even in the more difficult situation in which the transfer function $G_C(s)$ is to vary, for example, with temperature, in order to compensate for the variations which are anticipated in G_P, the designer is usually able to invent temperature-sensitive electric networks which possess the desired characteristics. As we demand closer control over the functional dependence of $G_C(s)$ on temperature, however, we begin to envision possible advantages of a computer acting as the controller, since with a computer realization it is a relatively simple task to specify the way in which the parameters of G_C vary with an externally measured variable such as temperature. This simplicity is particularly apparent if we utilize an electronic analog computer for the controller, since the analog computer is conventionally programmed to realize the identification of each parameter in the transfer function or differential equation with a single potentiometer or variable resistance in the computer. Thus, the earliest generalization of the controller from an electric circuit toward an electronic computer was implemented in terms of conventional analog-computing elements.

A parallel development of analog-computing controllers was motivated by the need for guidance-control systems for missile applications. The integration required in the recovery of positional information from the output of an accelerometer mounted on a stable platform in a moving vehicle led to the incorporation of mechanical (and later electronic) integrators and associated analog-computing elements for the controller section. Similarly, fire-control computers became more complex as attempts were made to improve the accuracy by including, in the nonlinear differential equations which the analog-computer controller solved, such secondary effects as the predicted motion of the vehicle on which the gun was mounted, and the variation of bullet-muzzle velocity with time.

Thus, by the middle of the 1950's, the technology of automatic control had developed to the point that the designer was attempting to control processes which were exceedingly complex. The complexity of such systems is ordinarily evidenced by either multiple inputs and outputs for the process being controlled, or a complex configuration for the process with severe constraints imposed on the designer's selection of system parameters.

The basic control-system configuration of Fig. 1 is markedly complicated if the process description is extended to include several inputs and outputs. For example, in the automatic control of a boiler for an electric generating station, the outputs (or variables which can be measured) include the steam pressure between the boiler and the turbine, the steam temperature, the rate of steam flow, the water level, etc. There are, likewise, several inputs (or variables which can be adjusted in order to realize the desired operating conditions), including primary fuel input, water input, etc. Thus, the process is described by a block diagram similar to that shown in Fig. 2, with m inputs and n outputs.

In such a system, the task of the controller is, typically, to adjust automatically each of the input variables in order to realize the optimum economy of operation while simultaneously maintaining each of the output variables within the limits prescribed by safety considerations. In addition, the controller in a fully automated system may include automatic scheduling of the start-up operation and automatic control of emergency shut-down procedures. These varied functions demanded of the controller, in particular the requirement of quite different controller operation under different loading conditions and in start-up and shut-down, lead quite naturally to the consideration of a special-purpose computer as the controller. Furthermore, the flexibility required of the controller and the desirability of a logical design for the controller suggest the incorporation of a special-purpose digital computer as the control element.

The nature of the control-system problem is illustrated by the special case in which there are two in-

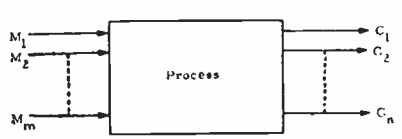


Fig. 2—Multidimensional process.

puts and two outputs for the specified process. In a linear system each of the outputs, C_1 and C_2, is determined in part by each of the two actuating signals:

$$C_1 = G_{11}M_1 + G_{12}M_2 \tag{1}$$

$$C_2 = G_{21}M_1 + G_{22}M_2. \tag{2}$$

If, in addition, there are two input signals R_1 and R_2, the control-system design problem is represented by Fig. 3 where the design problem is the choice of the controller characteristics, *i.e.*, the specific manner in which M_1 and M_2 are related to the measurable signals R_1, R_2, C_1, C_2, M_1, and M_2.

If the over-all system is to be linear (and if the process is linear), M_1 and M_2 are linear functions of the six measurable variables. Because in practical systems neither R nor C may be measurable, it is useful to consider the special case depicted in Fig. 4, in which the variables E_1 and E_2, defined by

$$E_1 = R_1 - L_1C_1 \tag{3}$$

$$E_2 = R_2 - L_2C_2, \tag{4}$$

are used to actuate the controller instead of R_1, R_2, C_1, and C_2, separately. Under this simplifying assumption, the actuating variables are given by

$$M_1 = H_{11}E_1 + H_{12}E_2 \tag{5}$$

$$M_2 = H_{21}E_1 + H_{22}E_2. \tag{6}$$

Inclusion of the variables M_1 and M_2 on the right sides of these equations does not increase the generality, although it may simplify the realization problem when the controller is constructed.

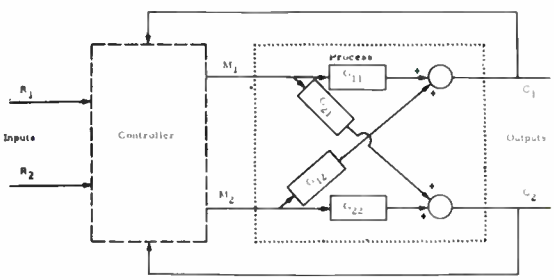


Fig. 3—Two-dimensional design problem.

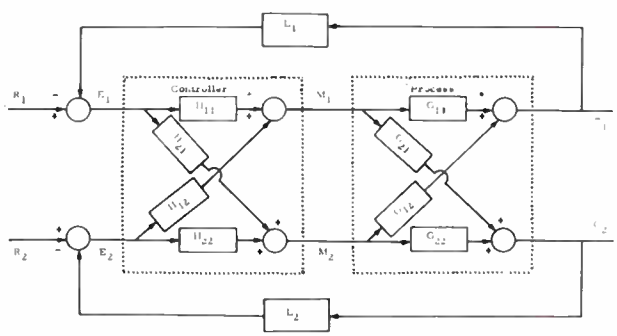


Fig. 4—Simple two-dimensional system.

Once the configuration of Fig. 4 is selected, the conditions under which noninteraction is realized, for example, are readily determined. If C_1 is to depend only upon R_1 and C_2 upon R_2 (the conditions for noninteraction), the two conditions

$$H_{22}G_{12} = -H_{12}G_{11} \tag{7}$$

$$H_{11}G_{21} = -H_{21}G_{22}, \tag{8}$$

with the resulting transfer functions

$$\left.\begin{aligned} T_{11} &= \frac{C_1}{R_1} = \frac{H_{11}\dfrac{\Delta_G}{G_{22}}}{1 + L_1H_{11}\dfrac{\Delta_G}{G_{22}}} \\ \text{where } \Delta_G &= G_{11}G_{22} - G_{12}G_{21} \\ T_{22} &= \frac{C_2}{R_2} = \frac{H_{22}\dfrac{\Delta_G}{G_{11}}}{1 + L_2H_{22}\dfrac{\Delta_G}{G_{11}}} \end{aligned}\right\}, \tag{9}$$

can be determined by direct application of elementary feedback theory: If $R_2 = 0$, C_2 must also be zero. The numerator of C_2/R_1 is evaluated by direct application of Mason's theorem[1] and equated to zero to yield the condition of (8).

Thus, the design procedure for a two-dimensional system breaks down into the following steps, if noninteracting controls are required:

1) The designer is given (or chooses at the outset) the specifications on T_{11} and T_{22}, as well as the transfer functions L_1, L_2, G_{11}, G_{12}, G_{21}, and G_{22}. Hence, Δ_G can be evaluated at once.
2) H_{11} is selected for the appropriate T_{11} according to (9).
3) H_{22} is selected for the appropriate T_{22} on the basis of (9).
4) H_{12} and H_{21} are selected to satisfy (7) and (8).
5) T_{11} and T_{22} are modified (within the performance specifications) until satisfactory and realizable H_{21} and H_{12} functions are obtained.

The five-step design procedure is straightforward in the two-dimensional case considered above as an example, but becomes complicated if the dimensionality of the control system is extended. Of even more importance, the simultaneous realization of the matrix of controller transfer functions by an electric network commonly leads to a complex interconnection of active and passive elements. For the example cited, if the design procedure is to result in *stable* transfer functions H_{jk}, two conditions must be satisfied simultaneously, 1) that $(1/T_{11} - L_1)$ and $(1/T_{22} - L_2)$ must be minimum-

[1] S. J. Mason, "Feedback theory—further properties of signal flow graphs," PROC. IRE, vol. 44, pp. 920–926; July, 1956.

phase transfer functions, and 2) that Δ_G must be a minimum-phase function. In simple cases, this requirement means that the direct coupling terms (G_{11} and G_{22}) must be larger than the cross-coupling terms; in complex cases, the interpretation is more difficult.

The above example has been discussed in detail because it is representative of the direction in which modern control theory is moving as the control engineer works with more complex processes and more stringent specifications. To a very considerable extent, the control engineer of 1960 is no longer concerned with the thoroughly familiar and intensively studied single-loop system of Fig. 1. Rather, the modern control engineer is concerned with extensions and modifications of the basic multidimensional configuration described above.

The two-dimensional design problem represented in Fig. 4 can be complicated, not only by increasing the dimensionality, but also by modifying the specifications. If the system-performance requirements include both the transmissions T_{11} and T_{22} and the sensitivities of these transmissions to changes in the process parameters (*e.g.*, the sensitivity of T_{11} to changes in G_{11})—a natural addition, since the primary purpose for utilizing feedback in the control system is to control such sensitivities—the basic configuration of Fig. 4 is no longer adequate. The designer then turns to the more general linear controller of Fig. 5, and the design procedure is correspondingly complicated with the controller now including the various H_{jk} and the four L_{jk} transfer functions. The requirements on the controller transfer-function matrix have been formulated in order to achieve such characteristics as 1) partial or complete noninteraction, 2) a system in which each of the outputs of significance is completely independent of several of the input functions (*i.e.*, rejecting completely the effects of noise or corrupting signals entering the system at various internal points), or 3) a configuration with specified inter-relationships among the various input and output variables. The general formulation has been presented in detail in the many articles and books by Kulebakin and his associates of the U.S.S.R. Academy of Science.[2]

The complexity of the complete controller for the system of Fig. 5, with the associated difficulty of realizing the eight component transfer functions, is coupled in many practical problems with a critical dependence of the transfer functions on the process parameters. In typical situations the over-all system is conditionally stable (this being the characteristic usually associated with complex systems with stringent specifications on both transmission and sensitivity), with the over-all transfer functions possessing poles close to the imaginary axis of the s plane. Under such circumstances, the controller must be designed so that its parameters depend upon environmental conditions in a manner determined by the process variation with the same conditions. When these demands are imposed on the designer, a flexible computer, or at least a computer including digital techniques, for the purpose of simultaneous realization of the interdependent transfer functions with controllable parameters, is a necessity.

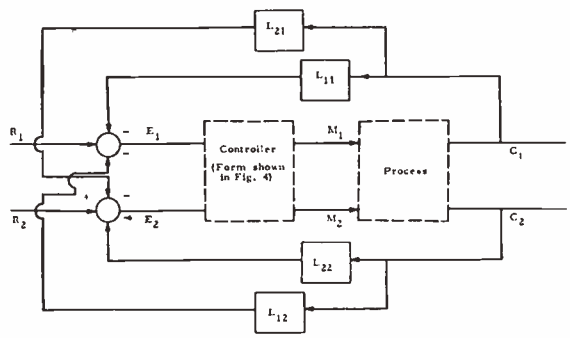


Fig. 5—Two-dimensional system for control of sensitivity as well as transmission.

At the beginning of this section, the problem of boiler control was cited as one example of such multidimensional systems. Another example is the automatic flight control system of a modern piloted aircraft in which the stabilization of the vehicle about the rotational axes directly affects its performance characteristics in the operating modes of fire and missile control, navigation, reconnaissance, bombing, automatic landing, etc. In this situation, with the various, quite different functions which the aircraft must perform, possibly during one flight, the control system must satisfy a set of different specifications dependent upon the particular mission of momentary interest. The incorporation of a digital computer as the central controller permits, with time multiplexing, the simultaneous performance of various functions, and at the same time provides the flexibility required to permit realization of the controller specifications which may differ radically from function to function.

Other examples of the use of digital computers in multidimensional control systems can be drawn from the range of military and industrial applications of control principles. For example, in a rolling mill for the production of sheet steel, the thickness of the output sheet is affected by the various furnaces in which the raw steel slabs are heated as well as by the performance characteristics of the several motor-control units and electric motors used to process the steel and roll the final sheets. Realization of a consistent thickness of the output sheet requires coherent control of each of the motors along the rolling mill. Determination of the proper actuating signals for the various motors is most conveniently carried out in a digital computer, particularly in order to permit the rapid change-over in the

[2] The entire theory of invariance, the focal point for the design of multidimensional systems, is described in detail in the "Proceedings of the Symposium on the Theory of Invariance," Moscow, 1958. (In Russian.) This book plus other basic references are listed in V. S. Kulebakin's paper, "The theory of invariance of regulating and control systems," in *Proc. First IFAC Congress*, Butterworths Scientific Publications, London, Eng., pp. 2095–2100; 1960.

control schedule when a change in output thickness is to be effected or when the characteristics of the input steel slabs change. This application of automation and computer-controlled industrial processes is an awesome example of the potentialities of automatic control, since the steel sheet comes off the rolling mill at 30 miles an hour.

Adaptive Control

The second major area of automatic control technology in which computers have played an important role expanding the horizons of the control engineer is that of adaptive control—automatic control in the presence of gross unpredictable variations in the characteristics of the process, or automatic control of a process for which the dynamic characteristics are largely unknown. Under these conditions, the controller of Fig. 1 must measure the performance characteristics of the system and then generate an actuating signal which results in satisfactory over-all performance.

The early work on adaptive control was largely motivated by research on autopilots for manned aircraft. Stimulated by the need for aircraft control over a flight regime which may correspond to process parameters varying by factors of 10:1 or more, several research groups investigated in detail the feasibility of various schemes for the automatic adjustment of controller parameters as the process parameters vary.[3] While most of the proposed systems involved relatively small modifications of conventional control systems, a radical change was investigated in terms of both computer studies and flight tests by the group under the direction of Aseltine.[4]

The general adaptive control system consists of the blocks indicated in Fig. 6. The dynamic characteristics of the process (or alternatively, of the over-all system) are measured in the identification block. On the basis of the results of this evaluation and of the measured characteristics of the input signal, a decision block determines an appropriate form for the controller characteristics. Finally, the actuation component realizes these desired characteristics, or realizes the actuating signal to drive the process. Thus, the adaptivity involves the elements of *identification*, *decision*, and *actuation*.

The autopilot developed by Aseltine and Anderson, like all practical adaptive systems, is a simplified version of the general configuration of Fig. 6. First, the signal-measurement block is omitted. Further simplification is effected in the decision and actuation elements by designing the controller so that the closed-loop controlled process is described by a second-order system. Then the adaptive loop is designed to hold constant the relative damping ratio of the over-all, second-order system.[5] Thus, the adaptivity is accomplished by measurement of the process dynamics, determination of the relative damping ratio ζ, and automatic correction of the ζ.

The noteworthy element in the adaptive section of the system is the equipment for the measurement of process dynamics. In contrast to the other adaptive autopilots which have been developed in which identification involves only the determination of a single variable (such as the integral of the error between the actual system output and the output of an ideal system), this scheme involves a complete determination of process dynamics in terms of the impulse response. If the process is linear and time-invariant, the impulse response is given by the cross-correlation between the input and output when the input is a white-noise signal. Thus, if low-level white noise is added to the process input, the impulse response can be determined as depicted in Fig. 7, with the cross-correlator calculating the expected value,

$$g_p(\tau) = E[n(t - \tau)c(t)]. \tag{10}$$

In order to simplify the equipment involved in the cross-correlation computations, a special-purpose hybrid (analog and digital) computer is employed. The noise signal utilized in the actual equipment is obtained by the periodic read-out of a noise sample stored as a binary sequence on a magnetic drum. A pseudo-white noise is realized in binary form as a coded sequence of

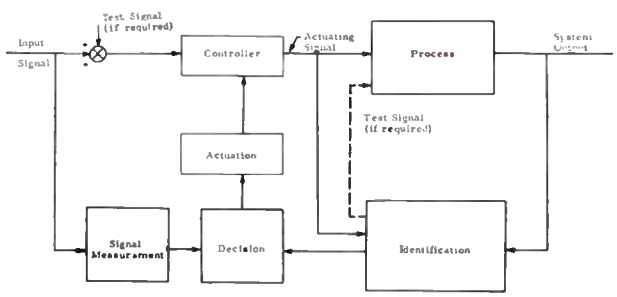


Fig. 6—General adaptive control system.

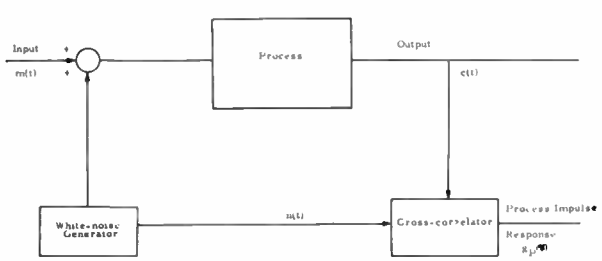


Fig. 7—Identification.

[3] P. C. Gregory, Ed., "Proceedings of the Self-Adaptive Flight Control Systems Symposium," Wright Air Dev. Ctr., Dayton, Ohio, Tech. Rept. 59-49; February, 1959.

[4] "A Study to Determine the Feasibility of a Self-Optimizing Automatic Flight Control System," Aeronutronic Div., Fort Motor Co., Newport Beach, Calif., WADD Tech. Rept. 60-201; June, 1960.

[5] Control of the resonant frequency was also investigated during the research program.

transitions between two possible signal levels.

The cross-correlation expression described by (10) requires three distinct operations: time delay (by an amount of t seconds), multiplication, and averaging. The time delay is realized with a shift register mechanized on the magnetic drum. As a result of the binary (plus or minus) form of the noise signal, multiplication can be effected with an electronic switch. Finally, the averaging operation is carried out by an RC low-pass filter. In the actual equipment, twelve parallel channels are provided (corresponding to different delay factors) in order to permit the simultaneous determination of twelve distinct points on the process impulse response.

Thus, the noise source and cross-correlator are implemented together as a special purpose, analog-digital computer system typical of the application of computing techniques in adaptive system design. In the actual autopilot, the impulse response is then used for the determination of the process relative damping ratio by comparison of the positive and negative areas of $g_p(t)$; suitable controller parameters are adjusted to hold constant the ratios of these two areas. This particular processing of the $g_p(t)$ function is valid only when the system is second-order [since higher-order processes may result in exclusively positive values of $g_p(t)$, even though the system is very close to instability], but the general procedure for process identification is representative of the increasing application of computers in automatic control systems. Indeed, the research program underlying the autopilot development is primarily of interest because of the extensive investigation of the identification problem—an investigation which included studies of the effects of process nonlinearities even though the identification procedure is based upon the assumption of linearity, validity of the impulse-response description of the process dynamics, and presence of noise or unwanted signals (including the primary operating signals of the aircraft control system) during the cross-correlation measurement.

In terms of the current state of the control art, the above autopilot represents an elegant implementation of the principles of adaptivity; by far the majority of adaptive systems which have been constructed and tested employ only partial identification of the process dynamics and represent a modification of conventional control systems in order to incorporate controller parameter changes coherent with the general trend of process-parameter variations.[6] As a result of the relative youth of the concept of adaptive control, most of the past implementations have been in terms of electric circuits with variable parameters controlled by an appropriate function of system performance, as in the on-off autopilot described by Shuck, *et al.*,[3] in which the characteristics of a nonlinear element are controlled by the limit cycle associated with a small-amplitude oscillation. Or, past implementations have been in terms of very simple analog-computing elements, as in the M.I.T. Instrumentation Laboratory autopilot discussed by Whitaker,[3] in which the controller gain is determined by an integral function of the difference between the actual system output and the output of a model.

Thus, the field of adaptive control is still very much in its infancy, still concerned with the control of relatively simple processes using adaptive elements which are designed principally on an intuitive basis or from an understanding of the general characteristics desired in controller operation. As applications of adaptivity increase in the future, we can anticipate the incorporation of more and more complex configurations until digital computers represent the only feasible basis for the design of the controller functions of identification, decision, and actuation.

The boiler-control problem cited briefly in the first part of this paper represents a logical application of the adaptive concept. In this system, the matrix of transfer functions relating the several outputs to the various input signals depends on the loading of the power plant. In order to realize either noninteracting control or optimum boiler dynamic performance (interpreted, for example, in terms of the optimum economy of operation) as the load varies over a range from the maximum value to a small function of the maximum, the transfer-function matrix must be determined at each operating point. Once the process is characterized, the controller system, although complicated, can be realized with a digital-computer implementation.

If the process-matrix variation with plant loading is known at the time of system design (or can be measured once at the start of operation), the computing controller can consist simply of a pre-programmed controller characteristic as a function of the single measured variable, the load. In coal-fired boilers, however, the process matrix changes markedly and unpredictably with time; in any case, the designer frequently finds it impractical to determine *a priori* the process matrix for all loading conditions. Under these circumstances, the advantages of an adaptive controller are apparent.

Thus, adaptive control is useful under either of two conditions: 1) when the process characteristics are unknown and the designer does not know the environmental factors which affect the process dynamics, and 2) when the process characteristics change markedly and unpredictably with time or environmental conditions. Since feedback control is fundamentally utilized for these same reasons, adaptive control represents a logical broadening of the familiar concept of feedback control. The focussing of attention in system design on the various functions represented in Fig. 6 leads to a variety of novel feedback control systems and provides a logical basis for the design of complex systems to meet unusually difficult specifications.

[6] G. R. Cooper and J. E. Gibson, "A Survey of the Philosophy and State of the Art of Adaptive Systems," Purdue Res. Foundation 2358, Lafayette, Ind., Tech. Rept. 1; July 1, 1960.

Optimalizing Control

Closely related to the subject of adaptive control is the field of optimizing control (or "optimalizing control" in the terminology of Draper and Li,[7] who first emphasized the subject as a novel approach to system design). The basic principles of optimizing control are illustrated by the simple configuration depicted in Fig. 8.

In this system, the process to be controlled possesses two output signals, c_1 and c_2, and four inputs, m_1 and m_2, the two actuating signals determined by the controller which is here divided into the computer and optimizer sections, and u_1 and u_2, the two disturbance signals which are not directly measurable and which affect the process outputs in an unknown fashion. The computer, on the basis of the measured values of c_1 and c_2, determines the value of α which measures the quality of system performance; optimum design corresponds to a maximization of the quantity α by the appropriate adjustment of m_1 and m_2. In addition, the computer measures secondary-system variables b_1 and b_2, which are constrained within known bounds for safety purposes. On the basis of the computed values of b_1, b_2, and α for the instantaneous values of u_1 and u_2 which exist, the optimizer determines changes in m_1 and m_2 which result in an increase in the criterion quantity α.

In any reasonably complex system, both the computer and optimizer blocks in Fig. 8 are conveniently realized by special-purpose computers. The operation of the system is illustrated by the one-dimensional characteristic of Fig. 9. For any given value of u_1, α varies with m_1; the task of the optimizer is to seek automatically for that value of m_1, resulting in the maximum possible α for the existing u_1. When u_1 varies, the "seeking" problem changes and a new maximum must be sought.

Even the simple cases of Figs. 8 and 9 indicate certain basic difficulties which arise in the realization of such an optimizing scheme. First, if the α criterion function possesses numerous maxima over the space of m, the automatic-seeking optimizer must include a logical method for the random inspection of the allowable region of the m space in order to avoid the system settling at a low maximum. Second, as we search over the space of m in this nonlinear programming problem, we often reach the boundary of the allowable m region, e.g., m_1 may be constrained to be less than a specified maximum value; the searching technique must therefore involve an instrumented procedure for continuing the search along the boundary. Third, variation of u_1 in Fig. 9 may result in instability, as shown in Fig. 10. For example, we might obtain an initial measurement of $\alpha=2$ with a trial value of $m_1=1$ when $u_1=2$. If, before the next measurement, u_1 changes to the value of unity and an m_1 of 0.9 is tested, the corresponding value of α is decreased to unity. The next logical choice for m_1 would be 1.1, but the proper direction of change of m_1 along the $u_1=1$ curve is just the opposite. In other words, if the time required for a significant change in u_1 is of the same order of magnitude as the time required for one cycle of controller operation, entirely erroneous results may be obtained.

The importance of the various difficulties cited above depends on the nature of the process, on the α function selected (and the nature of its functional dependence on the m and u variables), the form of the constraints, and the type of searching procedure which is implemented. A variety of different searching schemes have

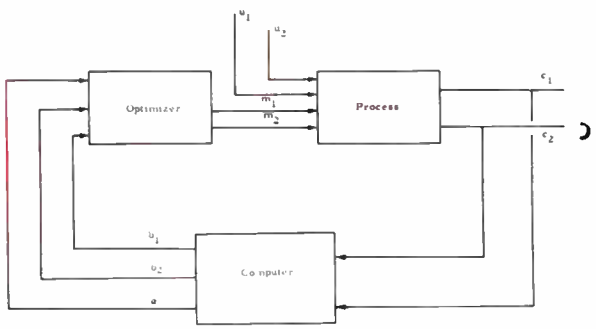


Fig. 8—Simple optimizing configuration.

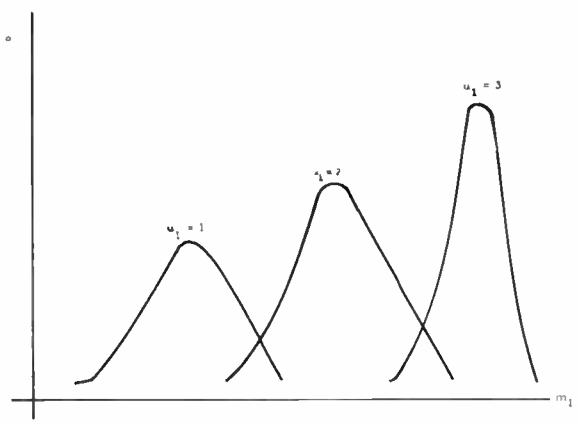


Fig. 9—Typical one-dimensional dependence of α on m_1.

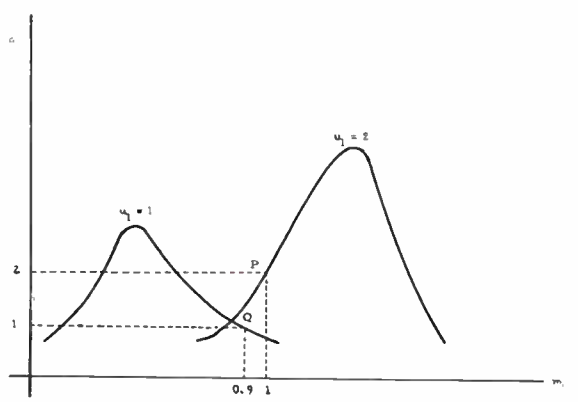


Fig. 10—Effect of u_1 variation.

[7] C. S. Draper and Y. T. Li, "Principles of optimalizing control systems," *Trans. ASME;* 1951.

been investigated by control engineers (as well as by mathematicians, econometricists, and others). The majority of the schemes described in detail in the control literature are closely related to the method of steepest descent or the gradient method or a combination of them. The Fel'dbaum experiments,[8] for example, use analog equipment for the automatic adjustment of twelve variables on the basis of a steepest-descent search until the maximum is approached, at which time operation is switched to search on the basis of the gradient method. Gibson[9] has investigated a searching method based upon successive adjustment of the variables (although the application is for an adaptive system rather than an optimizing controller).

Illustrations of optimizing control can be drawn from a broad range of industrial applications of automatic control. Kirchmayer[10] and others have described optimum control in the load-dispatching problem in the electric utility industry. In this case, the early systems employed analog computers for the determination of the optimum apportionment of the total electric-power load among the various generating stations, but as the specifications are refined and larger systems are encompassed the use of digital computers rapidly becomes desirable and economical.

In another typical example, Lerner[11] describes the automatic optimization of the burning in a flame furnace using a composite fuel mixture. The computer and optimizer measure the intensity of the radiation from the nozzle (with a radiation pyrometer) and adjust the m variables (the ventilating air flow and the flow of the oxygen-air mixture). The "disturbance" signal is the fuel flow.

A final example of the application of optimizing methods is provided by the multiparameter problem in the design of complex control systems.[12] In a wide variety of practical design problems in modern control engineering, the configuration and parameter values are almost entirely prescribed by considerations other than the performance of the control system. For example in missile control, aerodynamic, guidance, and mission considerations determine the control components which can be used and the characteristics of the process to be controlled; the control engineer is frequently left with the "design" problem of selecting specific values for a particular set of system parameters. Furthermore, the ranges allowable for the parameters are also fixed.

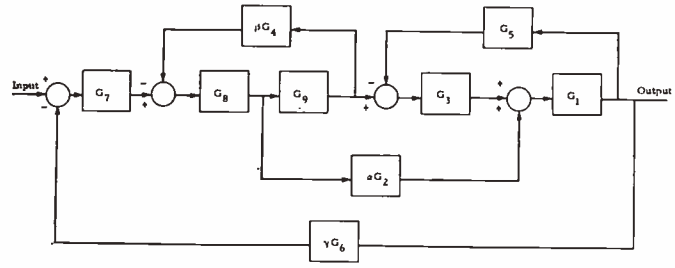


Fig. 11—Multiparameter problem.

A typical problem is illustrated in Fig. 11, where the three parameters to be chosen in design are denoted α, β and γ. Each of the G transfer functions is specified, and the three parameters are to be selected within prescribed ranges; *e.g.*,

$$1 \leq \alpha \leq 10 \quad 1 \leq \beta < 100 \quad 1 \leq \gamma \leq 10. \qquad (11)$$

The design task then involves a search over the three-dimensional (α, β, γ) space within the region defined by (11), for a point at which the operation of the system is an optimum. Although the space coordinates are now parameters rather than signals, we are working here with exactly the same optimization problem described above once the criterion for optimization is selected, *e.g.*, the minimum time required for the response to a step-function excitation, the optimum economy of operation, or the closest control over the quality of the system output product. When the number of adjustable parameters exceeds three, a random or trial-and-error search provides little hope for success within a reasonable time interval, and systematic or planned random search techniques must be employed; computers are essential elements in the system design.

Future Computer-Controlled Systems

The primary applications of computer control in the present state of the field have been described above. Current research work in control engineering points toward the increasing combination of computer and control technologies, particularly in the extension of the concept of adaptive control to more and more elaborate systems. The development of improved realizations of the three functions of identification, decision, and actuation will be based upon the research on the identification problem for both linear and nonlinear systems, the development of decision devices which incorporate increasingly elaborate realizations of the learning mechanism and represent implementation of the basic concepts of such closely related topics as statistical decision theory and pattern recognition, and the invention of novel and improved techniques for actuation. The close relation among the control engineer, the computer engineer, and the communication engineer, is emphasized by the mutual interest in the development of equipment which possesses the many advantages and avoids the disadvantages of the human being in communication and control tasks.

[8] A. A. Fel'dbaum, "An automatic optimizer," *Automat. Telemech.*, Moscow, no. 8; 1958.
[9] J. E. Gibson, "Self-optimizing or adaptive control systems," *Proc. IFAC Congress*, Butterworths Scientific Publications, London, Eng., pp. 147–153; 1960.
[10] L. K. Kirchmayer, "Optimalizing computer control in the electric utility industry," *Proc. IFAC Congress*, Butterworths Scientific Publications, London, Eng., pp. 393–398; 1960.
[11] A. Y. Lerner, "The use of self-adjusting automatic control systems," *Proc. IFAC Congress*, Butterworths Scientific Publications, London, Eng., pp. 1994–1998; 1960.
[12] E. Mishkin and L. Braun, Jr., "Adaptive Control Systems," McGraw-Hill Book Co., Inc., New York, N. Y., ch. 4; 1960.

Digital Computer Equipment for an Advanced Bombing, Navigation and Missile Guidance Subsystem for the B-70 Air Vehicle*

T. B. LEWIS†, MEMBER, IRE

Summary—Transistorized, high-speed, general-purpose digital computing equipment has been designed as the primary airborne real-time calculating element for the advanced bombing, navigation, and missile guidance subsystem intended for use in the B-70 air vehicle.

Because of the critical nature of this application, reliability, maintainability, and flexibility requirements received the utmost consideration in every design phase. Maximum reliability was achieved primarily through the use of a powerful, versatile, parallel main computer section supported by a minimal serial, emergency computer. A new approach to fault location enhances computer maintainability and permits in-flight repair, while flexibility is achieved by means of unique, high-speed input-output processing equipment.

Introduction

WEAPON-system reliability requirements dictated the selection of redundant computing elements; choice of the parallel-serial redundancy approach rather than duplexing identical computer sections was predictated on the space and weight limitations inherent in airborne applications.

During normal operation of the bombing, navigation and missile guidance subsystem, a high-speed parallel computer with both a random access memory and a magnetic drum memory performs all calculations required by the subsystem. If the main computer malfunctions, a moderate-speed, serial, all-drum computer automatically assumes control and generates solutions to a simplified problem. Repair of the main computer is then possible without disturbing the remainder of the subsystem.

An over-all block diagram of the digital computing equipment is shown in Fig. 1. It consists primarily of the parallel main computer, the serial emergency computer, and common input-output equipment. Each computer is composed of a central computer and a high-speed input-output processor. The two computers are capable of intercommunication.

Main Computer

Central Computer

Characteristics of the main computer are listed in Table I (next page). As shown in Table II, the main central computer performs six basic types of operations. Fig. 2 shows a simplified flow diagram of the main central computer.

* Received by the IRE, August 1, 1960.
† Federal Systems Div., IBM Corp., Owego, N. Y.

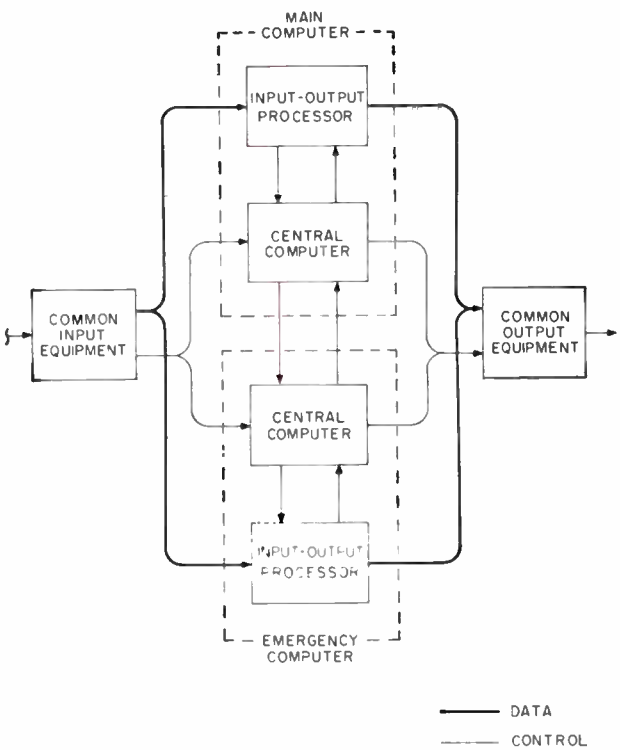


Fig. 1—Block diagram of computer equipment.

In typical single-address operation, one of the two operands required for any given calculation is already contained in the accumulator register; the second operand is determined by the instruction. During arithmetic-type computer operations, matrices decode the address and operation portions of the instruction register. While the second operand is being read from the random-access memory into the memory buffer register, control gates for the particular operation are being energized.

Numerical computations are performed in a parallel arithmetic element consisting of 22 stages. In addition to the memory buffer and accumulator registers, there are an adder-subtracter and a multiplier-quotient (m-q) register.

In general, while one instruction is being executed in the central computer, the succeeding instruction is read from the drum in a four-bit serial by four-bit parallel manner. The timing chart in Fig. 3 illustrates this principle. After an operation has started, the address portion of the instruction being executed is not required, and its place in the instruction register may be

TABLE I
MAIN COMPUTER CHARACTERISTICS

Type of Computer	General-purpose central computer with high-speed input-output processor
Mode of Operation	Parallel arithmetic Serial-parallel program Serial input-output
Internal Number System	Conventional binary
Arithmetic Notation	Fixed point
Word Length	22 bits plus sign and parity
Timing	Synchronous
Clock Rate	166.4 kilopulses per second
Addressing	Single address
Storage	Program—26,624 instructions (drum) Tabular—6656 constants (drum) Data—1024 words (random access)
Arithmetic Speeds	Addition—24 μsec Subtraction—24 μsec Multiplication—264 μsec Division—288 μsec
Number of Operations	14 instrumented
Control Input-Output	96 discrete inputs (contact-sense) 80 discrete outputs (contact-operate)
Data Input-Output	52 variables, processed at rate of 5200 operations per second

TABLE II
MAIN COMPUTER OPERATIONS

Arithmetic	
Addition	ADD
Subtraction	SUB
Multiplication	MUL
Division	DIV
Clear and Add	CAD
Add and Flip	ADF
Random Access Memory	
Store	STO
Scaling	
Shift	SFT
Program Sequencing	
Absolute Transfer	TRA
Conditional Transfer	TRC
Stop	STP
Read Constants	
Read Constants Band	RCB
Input-Output	
Discrete Input-Output	DIO
Serial Input-Output	SIO

taken by the address portion of the next instruction. This method alleviates the need for an additional register to buffer the instruction. Instruction word format is shown in Fig. 4.

Drum Memory

A nickel-cobalt plated magnetic drum contains the program and constants memory. Magnetic drum storage was selected because its nondestructive readout

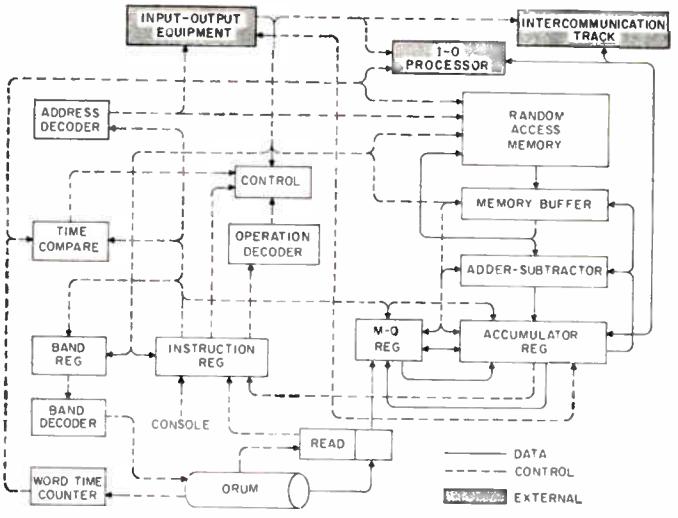


Fig. 2—Flow diagram of main central computer.

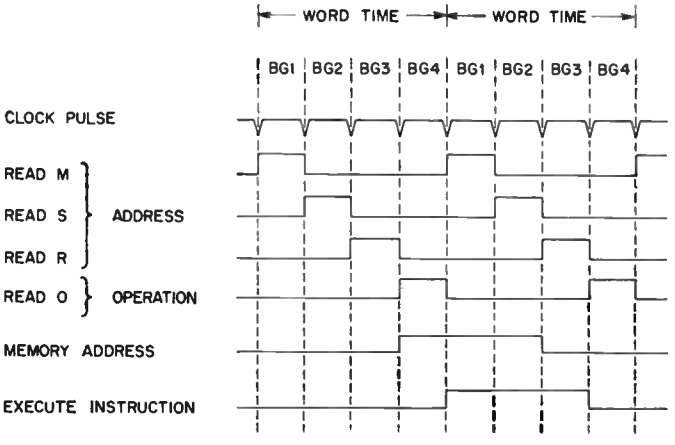


Fig. 3—Main central computer timing.

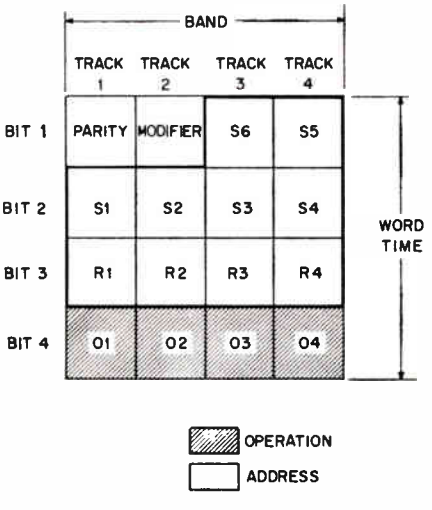


Fig. 4—Main computer instruction word format.

capability was imperative for weapon-system reliability, and because of low bit cost in terms of weight, volume, and power requirements. Air-floated heads permit uniform signal waveforms under severe vibration and shock conditions. Heads are mechanically and automatically lifted from the surface during starting and stopping to eliminate signal deterioration resulting from surface and head wear and to reduce motor starting torque. Biased discrete-spot recording permits reliable read-out with a maximum signal-to-noise ratio. The drum is a hollow cylinder with a diameter of six inches, and a length of twelve inches; it is driven by a synchronous motor, located inside the cylinder, at a nominal speed of 6000 rpm. Track spacing is 0.042 inch; packing density is 176 bits per inch.

Instructions are stored on the magnetic drum in a four-bit serial by four-bit parallel configuration, as shown in Fig. 5. Bits are read into the instruction register at 6-μsec intervals, with a basic clock of 166.4 kilopulses per second. The four serial bits of an instruction, therefore, are read in 24 μsec, the basic word time of the main computer. Instructions are stored sequentially around the drum, thus avoiding search time; however, provision is made for skipping instructions or changing tracks for branching purposes. While one instruction is being executed, the succeeding instruction is read into the instruction register.

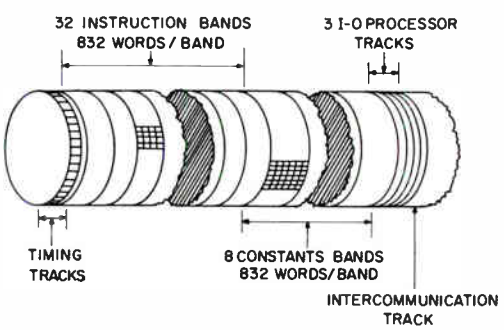


Fig. 5—Main computer drum organization.

Constants are stored on the drum in a four-bit serial by six-bit parallel configuration containing 22 magnitude bits plus sign and parity bits. As with instructions, constants are read from the drum in 24-μsec intervals, or one word time.

Fig. 5 shows how tracks on the magnetic drum are grouped to form bands. During normal operation, drum tracks are nonerasable to prevent accidental destruction of the stored program and constants.

Random Access Memory

Selection of a random access data memory was predicated on the need for high-speed calculations without the delays encountered in searching for operands that are characteristic of drum memories. The full 1024-word memory consists of eight modules, each containing 256 half-words (16 by 16 by 12). The half-word technique permits the use of only 12 memory-sense amplifiers instead of the 24 usually required, with a corresponding reduction in hardware. Sense amplifiers are time-shared to read first the low-order half of a data word. Because the memory circuits are capable of higher speeds than the basic logic circuits, this technique has no effect on the computer's internal organization.

Input-Output Processor

One of the most unique features of the AN/ASQ-28(V) bombing, navigation and missile guidance subsystem computing equipment is the high-speed input-output processor, which performs a number of functions. Originally, this processor was intended to relieve the central computer of calculating servo errors at frequent intervals and of suffering a corresponding loss in instruction storage and computing cycle speed. However, this function was extended to allow the input-output processor to perform additional functions with subsequent savings in hardware and programming. The various tasks handled by the input-output processor are as follows:

1) It calculates servo error signals.
2) It determines first-order clamp for servo loops.
3) It accumulates frequency inputs and outputs.
4) It buffers decimal printer word.
5) It buffers decimal display word.
6) It accepts manual-insert register word.
7) It decodes shaft-to-digital encoder inputs.

In its basic operation, the input-output processor performs the differencing function of a servo loop that is to be positioned as an output of the central computer. Each servo is provided with a v-brush disk converter through which the servo loop provides its feedback signal to the input-output processor. After decoding the v-brush input, the processor differences the signal with the computed value supplied by the central computer, and transmits an error signal to the servo. Each output parameter is sampled in this manner at a frequency of 100 cps, or once every 10 msec, which is one drum revolution.

Fig. 6 shows a simplified block diagram of the high-speed input-output processor. It consists essentially of three drum tracks, the quantity, increment and precesser, a serial adder-subtractor, a serial subtractor, a servo error generator, and a converter v-brush decoder. Drum tracks are subdivided into 52 serial words of 32 bits per word. Addressing of inputs and outputs to be handled by the processor is, therefore, a function of drum position, or word time.

Once each computation cycle of the central computer, a specific output parameter is calculated and transferred serially onto its preselected word position on the quantity track. Thereafter, the processor functions automatically until a new output is calculated by the central computer. As the quantity appears under the read head of the quantity track, the analog-to-digital converter for

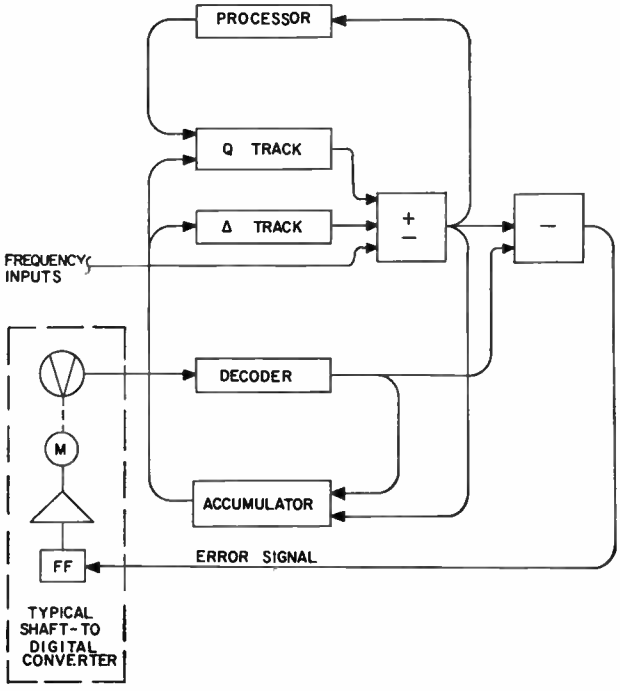


Fig. 6—Block diagram of input-output processor.

the specific quantity is addressed automatically, and its indicated value enters the processor via the v-brush decoder. The calculated quantity from the quantity track and the indicated quantity from the converter are differenced in the subtractor, and the resultant error is transmitted to the servo, where it is stored. The error signal then drives the servo at a constant speed until a new error is calculated one drum revolution (10 msec) later.

Emergency Computer

Central Computer

Like the main computer, the emergency computer consists of a central computer and a high-speed input-output processor. To meet its intended function as a back-up for the main computer, the emergency computer was designed to provide maximum versatility with minimum weight, volume, and power. Because the two computers must communicate with each other, the magnetic drum is common to both, thus avoiding buffering and synchronization problems. For the emergency computer, the drum is used extensively for arithmetic and control registers, by means of revolvers, and for program, constants, and data memory. Considerable hardware savings resulted from this technique.

Table III shows the characteristics of the emergency computer, and a simplified flow diagram of the emergency central computer is shown in Fig. 7. Assuming that there is an instruction contained in the instruction revolver, the word-time section of the next instruction portion is compared with the address reference track until the drum revolves to the position specified by the instruction address. When coincidence occurs, the track address section of the next instruction is transferred from the instruction revolver to the track address

TABLE III
Emergency Computer Characteristics

Type of Computer	General-purpose central computer with high-speed input-output processor
Mode of Operation	Serial
Internal Number System	Conventional binary
Arithmetic Notation	Fixed point
Word Length	23 bits plus sign, parity, and switching
Timing	Synchronous
Clock Rate	166.4 kilopulses per second
Addressing	One-plus-one address
Storage	Program and tabular—3456 instructions and constants Data—384 words
Arithmetic Speeds	Addition—624 μsec Subtraction—624 μsec Multiplication—3.744 msec Division—3.744 msec
Number of Operations	10 instrumented
Control Input-Output	48 discrete inputs (contact-sense) 32 discrete output (contact-operate)
Data Input-Output	32 variables, processed at rate of 3200 operations per second

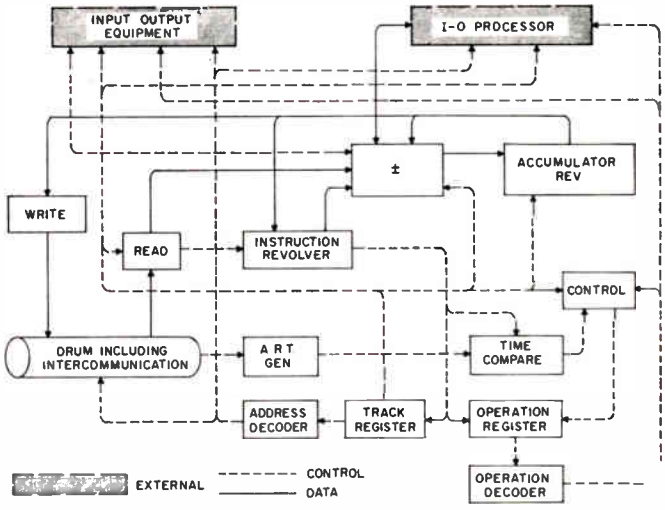


Fig. 7—Block diagram of emergency central computer.

register, and Phase I ends. Having found the correct word time and selected the proper track, the addressed instruction is read into the instruction revolver during Phase II. During Phase III, the word-time section of the address portion of the new instruction now in the instruction revolver is compared with the indication of the address reference track. Again, when coincidence occurs, the track address portion of the operand address is transferred to the track address register, and the operation bits are transferred into the operation register, ending Phase III. The operation is performed during Phase IV.

Five basic types of operations performed by the emergency computer are shown in Table IV.

TABLE IV
EMERGENCY COMPUTER OPERATIONS

Arithmetic	
Addition	ADD
Subtraction	SUB
Multiplication	MUL
Division	DIV
Clear and Add	CAD
Memory	
Store	STO
Scaling	
Shift	SFT
Program Sequencing	
Conditional Transfer	TRC
Input-Output	
Input	INP
Output	OUT

Drum Memory

As shown in Fig. 8, emergency computer instruction words contain 26 bits. In addition to the parity and switching bits, eight bits are used for operand address, four bits for the operation, and twelve bits for the address of the next instruction. In the emergency computer, these 26 bits comprise one word time of 156 μsec. Drum-track organization is shown in Fig. 9. There are 26 tracks of interleaved instructions and/or constants (128 words per track) and two noninterleaved tracks, six data tracks of 64 26-bit words each, plus the intercommunication track, the instruction, accumulator and multiplier-quotient revolvers, and three input-output processor tracks. There is also an address reference track, which performs the function of indicating drum position. The track is divided into 64 word times, and the binary values of drum word time are recorded in the appropriate bit-time positions. This technique is employed instead of a six-stage binary counter, which would require a greater number of components.

Input-Output Processor

Functioning of the input-output processor of the emergency computer is essentially similar to that of the main computer, except that only 32 word positions are available, and addressing is accomplished by the address reference track. Because of the similarity, the emergency computer input-output processor will not be discussed.

INTERCOMMUNICATION

As shown in Fig. 10, intercommunication between the main and emergency central computers is accomplished by a drum track. Pertinent quantities may be transferred from the accumulator of the main central computer by means of a serial input-output (SIO) operation onto the intercommunication track. This track is then addressed by the emergency computer as an additional data track containing certain operands. Information may be written onto the same intercom-

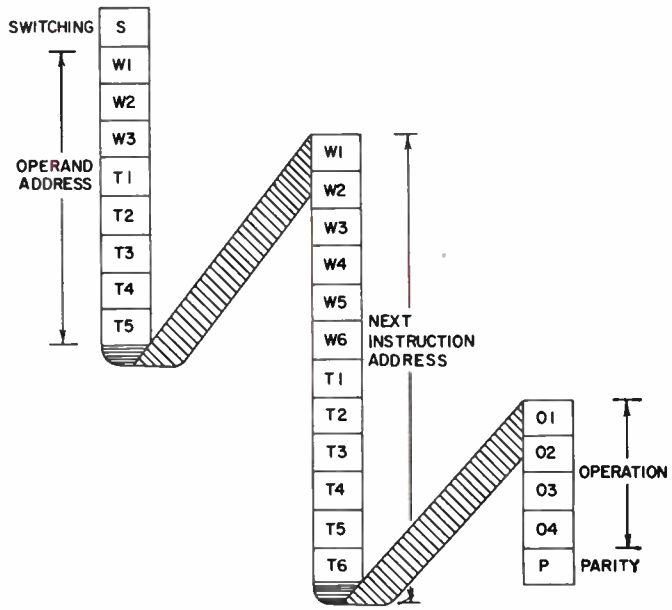


Fig. 8—Emergency computer instruction word format.

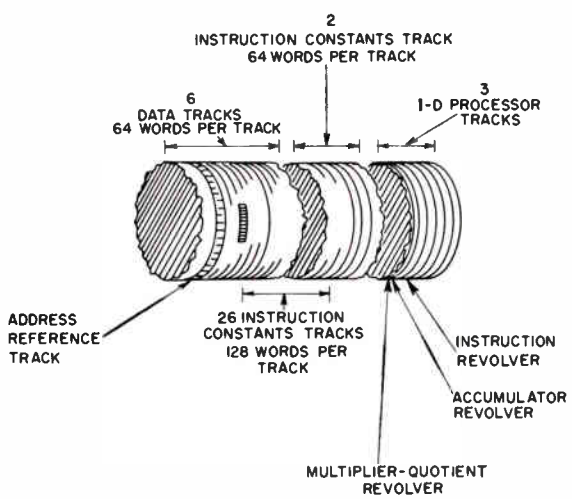


Fig. 9—Emergency computer drum organization.

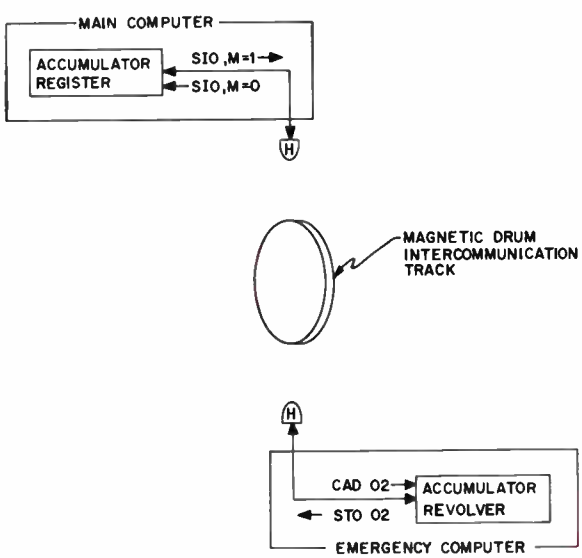


Fig. 10—Intercommunication between computers.

munication track by the emergency computer, using the store (STO) operation which transfers the contents of the accumulator revolver onto the track. These data may then be read into the main computer accumulator register by a serial input-output operation.

Common Input-Output Equipment

Input-output equipment operates externally to both central computers and their input-output processors. This equipment is switched between the main and emergency computers, depending upon which one is in control of the bombing, navigation, and missile guidance subsystem of the B-70 air vehicle. These functions are as follows:

1) It buffers and provides amplification for two decimal display registers of eight characters each.
2) It buffers and provides amplification for decimal printer.
3) It buffers and amplifies discrete control outputs.
4) It gates discrete control inputs.
5) It amplifies shaft-to-digital converter selection signals.
6) It amplifies shaft-to-digital converter v-brush input signals.
7) It accumulates frequency input signals during drum revolutions.
8) It switches control of above functions between main and emergency computers.

Maintainability

Another unique feature of the digital computing equipment is the maintainability which has been designed into both computers to achieve maximum effectiveness and minimum down time. Error checking, through built-in circuitry and programming techniques, and a random error counter, minimizes the effects of random and intermittent errors on system performance. In addition, a new hardware approach to fault isolation, supplemented by simplified diagnostic programs, permits rapid localization of computer failures. Standardization pluggable subassembly packaging permits ready in-flight repair of the computer with a minimum complement of spares.

Circuits

Throughout the digital computing equipment, voltage mode, passive logic circuitry is utilized to perform the maximum logic functions with a minimum of transistors. Circuits employing silicon semiconductors have been designed for ultra-reliable operation over an ambient temperature range from 0° to 100°C. The component listing is shown in Table V.

Transistor usage has been minimized through the use of high-quality metal-film resistors and unique Zener-diode input circuitry. A total of six transistor types are used: the 2N338 and 2N697 types are employed in 90 per cent of the circuitry; the 2N338 is used in low-power circuits to drive loads of less than 12 ma, and the 2N697 is used in medium-power applications where load currents up to 200 ma are required.

TABLE V
Component Usage

	Main Computer, Including I-O Processor	Emergency Computer, Including I-O Processor	Common I-O
Transistors	1697	592	832
Resistors	7274	2540	3647
Diodes	13,076	4395	7265
Capacitors	1927	672	498
Miscellaneous	278	15	23
Total	24,252	8214	12265

TABLE VI
Physical Characteristics

	Weight (pounds)	Volume (feet^3)	Power (watts)
Main computer, including input-output processor	200.6	5.76	494
Emergency computer, including input-output processor	67.8	1.92	216
Common input-output	99.2	2.88	219
Magnetic drum unit	42.0	1.62	
Total	409.6	12.18	929

Packaging

Computer packaging is in accordance with applicable military specifications for airborne electronic equipment. Pairs of printed circuit boards, resin-coated for moisture protection, are mounted into pluggable subassemblies; twelve subassemblies comprise a unit. The main computer, including its random access memory, consists of six units; the emergency computer is contained in two units; three units are required for the input-output equipment for the primary application. The magnetic drum is housed in a separate unit. Physical characteristics are listed in Table VI.

Conclusions

The digital computing equipment described, operating in real time, provides fast, accurate solutions to the bombing, navigation, and missile guidance problems encountered in the B-70 air vehicle. The flexibility, reliability, and maintainability inherent in its design contribute heavily to maximum weapon-system effectiveness with a minimum of support.

Acknowledgment

Development of the digital computer equipment for the bombing, navigation and missile guidance subsystem was performed under contract initially with the U. S. Air Force, Wright Air Development Center, Dayton, Ohio, and subsequently under subcontract with North American Aviation, Inc. The author wishes to thank his colleagues for their assistance in the preparation of this paper.

Digital Simulation in Research on Human Communication*

EDWARD E. DAVID, JR.†

Summary—**Digital simulation is a powerful tool in uncovering the basic properties of new or proposed communications principles, particularly those involving coding of visual or auditory information. Operating on digitalized speech or pictorial signals, a stored program computer can perform processing equivalent to any coding. The output signals so produced can then be made available for subjective evaluation, thereby removing the necessity for premature instrumentation to produce samples for viewing or listening. This technique owes its efficacy to 1) the availability of computers fast enough to accomplish the processing in a reasonable time scale, 2) the existence of high quality translators to implement the flow of continuous signals in and out of the computer, and 3) the creation of compiling programs which allow uninitiated investigators almost immediate access to computer facilities, and which keep programming effort low. Simulation is assuming an increasing role in communications research.**

INTRODUCTION

CHEFS, wine tasters, painters, and musicians have long paid tribute to the fine discriminating powers of the human senses. It is an axiom among these artists that sensory appeal is the criterion of success. Engineers, too, have found that subjective factors play a key role in the evaluation of communication systems transmitting visual or auditory information. The physically measurable properties of such a system, such as its bandwidth and signal-to-noise ratio, are often helpful in making gross judgments, but with few exceptions the final test involves listening or viewing the received signal. Only if physical fidelity criteria are based upon subjective measurement can they substitute for the ear or eye. Indeed, it is the perceptual significance of transmission distortions which is the crucial factor in determining the merit of a communication system.

Therefore, it is not unusual for engineers to carry out intelligibility and quality tests on the systems they create, and to rely on the results to specify their performance. To perform these tests, signal samples must be generated to serve as material for subjective evaluation.

Traditionally, system models are built to generate these samples. In some instances, though, the high costs associated with today's instrumentation preclude building either the system or even a simplified version incorporating its basic principles. This constraint often prevents experimental evaluation of speculative communication concepts. In this and other cases, it may pay to depart from tradition and adopt simulation techniques. The digital computer is an apt tool for simulation. Such a facility can be arranged to accept appropriate inputs and to generate output samples for listening or viewing.

By this means, a stored-program computer, whose function can be changed from the simulation of one model to another by altering the instructions, can greatly facilitate evaluation of communication principles and systems. In addition, this type of simulation has the desirable property of separating defects of principle from those associated with a particular instrumentation.

This technique is useful in another context. In this age of advanced communication, transmission systems are tailored to a relevant class of signals. Signal properties determine design and coding procedures. In establishing these properties, digital computers can analyze signals, thereby serving as specialized measurement equipment. Computers can also generate visual or auditory signals directly from a program without any other input. Here the computer acts as a signal source.

Several investigations using simulation and involving pictorial material and speech have been carried out at the Bell Laboratories. Principally, these investigations concern codings aimed at conserving transmission channel capacity. Closely related are investigations aimed both toward automatic recognition of perceptual attributes of signals, and psychological investigation of perceptual mechanisms. This paper describes briefly some of these studies and the techniques developed for attaining realistic, workable simulations.

INPUT-OUTPUT TRANSLATOR

Since computers deal only with numerical data, one prerequisite to digital processing of speech and pictorial signals is a device to translate between analog and digital domains. Such translators commonly utilize a pulse-code (digital) representation.[1–5] The sampling

* Received by the IRE, July 29, 1960.
† Bell Telephone Labs., Inc., Murray Hill, N. J.

[1] G. L. Schultz, "The use of the IBM-704 in the simulation of speech-recognition systems," *Proc. EJCC*, Washington, D. C., pp. 214–218; December 9–13, 1957.

[2] E. E. David, Jr., M. V. Mathews, and H. S. McDonald, "Description and results of experiments with speech using digital computer simulation," *Proc. NEC*, Chicago, Ill., pp. 766–775; October 13–15, 1958.

[3] E. E. David, Jr., M. V. Mathews, and H. S. McDonald, "A high-speed data translator for computer simulation of speech and television devices," *Proc. WJCC*, San Francisco, Calif., 169–175; March 3–5, 1959.

[4] J. W. Forgie and C. D. Forgie, "Results obtained from a vowel recognition computer program," *J. Acoust. Soc. Am.*, vol. 31, pp. 1480–1489; November, 1959.

[5] J. W. Forgie and G. W. Hughes, "A real-time speech input system for a digital computer," *J. Acoust. Soc. Am.*, vol. 30, p. 668A; July, 1958.

theorem[6] prescribes that input analog signals must be time-sampled at a rate equal to or greater than twice their highest frequency component. Each sample is then coded into a number, usually binary, representing its amplitude to the nearest integer. The resulting succession of numbers might then be introduced directly into a computer except for several complicating factors. Computer input circuits usually require that input data conform to a rigid format specifying data rate, error-check coding, and supervisory marks. Furthermore, inputs rarely accept single digits in sequence, but rather take several digits in parallel usually from a magnetic or punched paper tape or from cards. Finally, because the internal computer memory is of limited size, the data on the tape must be grouped into convenient size blocks, usually called "records." Thus, the translator must convert a continuity of pulse-code samples to discontinuous records. Of course, the translator must work from analog to digital and vice versa.

For example, the IBM-704 computer can take its input from a seven-track magnetic tape. Six of these tracks contain binary data, the other an error-check digit. In each track, there are 200 bits/inch. Recording epochs occur simultaneously in all tracks. Each seven-bit line transverse to the long dimension of the tape constitutes one "character" (200 characters per inch). The number of characters to the record can be determined by the computer program, but the end of the record must be marked by a $\frac{3}{4}$-inch gap on the tape. The end of the data must be signified by a special mark, known as an "end-of-file."

All of these specifications are satisfied by the digital recordings made on the Bell Laboratories translator shown in Fig. 1. In the record mode the analog input signal feeds an analog-digital converter and is sampled at the command of an external sampling pulse. The converter's continuous digital output is grouped by the buffer storage into preset-length records which are then read onto magnetic tape by means of a fast start-stop transport. During playback, the translator reads a discontinuously-recorded tape through the buffer into a continuous stream of samples at a rate determined by an external sampling pulse.

By divorcing the input and output sampling times from the instantaneous recording and playback rates on the tape, the arrangement can accommodate a range of analog bandwidths (proportional to sampling rate) while maintaining the 200 character per inch density on the tape. In addition, the fluctuations in character spacing resulting from "jitter and wow" in the low-inertia digital tape drive are removed during playback so that they do not affect the analog output. The translator can operate at sampling rates as high as 10,000 samples per second with each sample quantized into 2048 levels. (Alternatively, it can supply 20,000 64-level samples per second.) This capability is sufficient to handle signals with a bandwidth of 5000 cps and a signal-to-noise ratio of 60 db. This number of quantizing levels insures that quantizing degradation is negligible compared to effects being studied in the simulation.

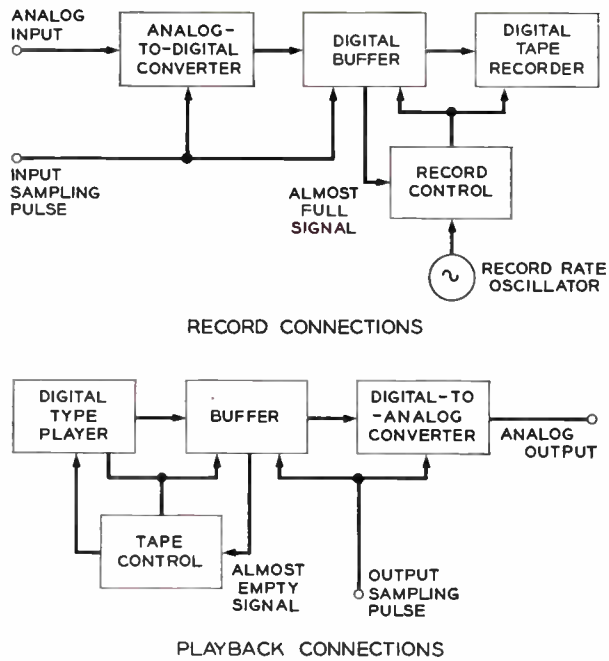


Fig. 1—Block diagram of data translator for computer input-output.

Transducing pictorial material into the computer requires some apparatus in addition to the translator.[7] For this purpose, the translator input is provided by a flying-spot scanner which covers about 1/25 the area of a full television picture in 2.4 seconds. The picture format is then an array of 100×100 picture points. During playback from a digital tape, the picture is displayed on a long-persistence screen, or a 35-mm photograph is made from a short-persistence phosphor. A picture of this size and resolution is sufficient to show those distortions which would be noticeable in a full size picture. Fig. 2 shows a photograph after the material has passed through the computer chain.

There are other pieces of auxiliary equipment which supplement the translator. One is a time-multiplexer which samples up to 24 input signals and presents the samples sequentially to the converter. Alternatively, it can distribute samples from the converter to as many as 20 output channels. This device has been used both to take spectral information from a bank of contiguous band-pass filters and to control a speech synthesizer[8] from computed signals.

[6] B. M. Oliver, J. R. Pierce, and C. E. Shannon, "The philosophy of PCM," PROC. IRE, vol. 36, pp. 1324–1331; November, 1948.

[7] R. E. Graham and J. L. Kelly, Jr., "A computer simulation chain for research on picture coding," 1958 IRE WESCON CONVENTION RECORD, pt. 4, pp. 41–46.

[8] E. E. David, Jr., "Artificial auditory recognition in telephony," *IBM J. Res. and Dev.*, vol. 2, pp. 294–309; October, 1958.

Fig. 2—Picture consisting of 100×100 points after passing through translator.

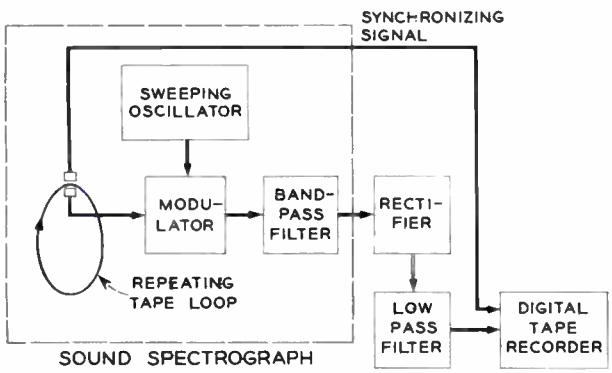


Fig. 3—Spectrograph computer input.

Another useful accessory is the spectrograph[8] input shown in Fig. 3. Here a heterodyne sound analyzer has been adapted for computer input. A repeatedly-scanned loop of tape is successively analyzed at different frequencies by a modulator, oscillator, and band-pass filter. The filter output is rectified, smoothed, and introduced into the converter along with a synchronizing signal which marks the beginning of the loop. Spectral inputs are sometimes preferable to computing the spectrum from the time waveform. Such computations can be overly time consuming.

Since the translator's record and playback sampling rates are independent, any signal may be reproduced slowly enough so that it can be recorded by a pen oscillograph. The translator can in addition supply a timing track which specifies the sample number of each output sample. Thus, the data may be subjected to detailed visual analysis.

These "peripheral" devices, along with other special apparatus built for particular tasks, greatly increase the versatility of the translator.

Sampled-Data Approximations to Continuous Systems

The translator described in the preceding section supplies a quantized and sampled computer input. Thus, any simulated communication system must necessarily operate on a sampled signal. This fact is no constraint on the simulation of systems which themselves process sampled data. The operations incorporated in such systems can be duplicated exactly with a computer. However, this statement is not generally true for systems operating on continuous signals. Fortunately, there are sampled-data near equivalents to continuous systems. Consequently, one important facet of simulation involves formulating such approximations.

Many operations, such as addition, give equivalent results whether applied to continuous signals or their sampled versions. Other operations must be suitably tailored for digital simulation. An example is linear filtering.

Filtering in a continuous system may be expressed by the convolution integral which relates the filter output waveform, $o(t)$, to the input waveform, $i(t)$, and the filter impulse response, $h(t)$. Since in the simulation both input and output must consist of samples, the impulse response, too, must be sampled at the same rate, thereby reducing the convolution integral to a summation. Many impulse responses are not bandlimited and, therefore, cannot be represented in sampled form without error. However, the effect of this error in the convolution computation can be specified. Let $h(t)$ be the impulse response, $H(j\omega)$ its Fourier transform, and W_s the sampling rate of the input; then the mean-square error in the output band $o \leq \omega \leq W_{s/2}$ is

$$\sum = 2 \int_{W_{s/2}}^{\infty} | H(j\omega) I_s(j\omega) |^2 d\omega$$

where $I_s(j\omega)$ is the spectrum of the sampled input. Note that this error is zero if $H(j\omega)$ is limited to the band $o \leq \omega \leq W_{s/2}$. If not, one means for restricting the error substitutes for $H(j\omega)$ another response $H'(j\omega)$ which is nearly equal to $H(j\omega)$ in the interval $o \leq \omega \leq W_{s/2}$, but is smaller outside. For instance, H' might be formed by adding several low-pass sections to H. The procedure carries the disadvantage that it may increase the duration of the impulse response. Another method is to increase the sampling rate until the error falls within the required bound. In this case, also, the amount of data which must be handled is correspondingly increased. However, often the input signal is only nominally bandlimited to W cps and so is sampled at, perhaps, $4W$ times per second. This rate is high enough to accommodate many filters of interest. Nonetheless, care must be taken to avoid the cumulative effects of sampling error in simulating multiblock systems.

Once a sampled-date filter approximation is established, it can be simulated in two ways. One is the "transversal filter," a tapped delay line whose outputs are weighted and summed according to

$$o(t_i) = \sum_{j=-\infty}^{t_i} h'(t_i - t_j) i(t_j)$$

where $o(t_i)$ and $i(t_i)$ are the sampled input and output, and $h'(t_i)$ is the sampled impulse response. Such a filter is shown in Fig. 4(a). One difficulty here is that the impulse response must be truncated to some finite number of values, requiring an additional approximation. In the second method, this is avoided by expressing each

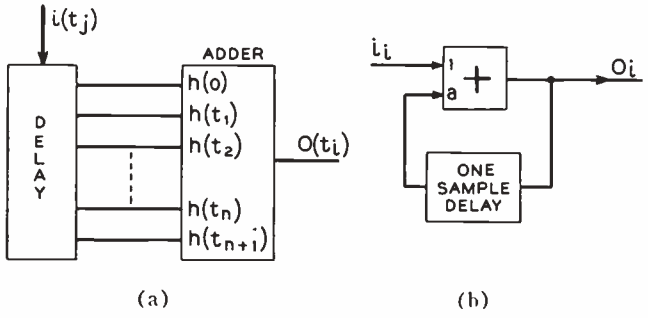


Fig. 4—Two methods of filter simulation. (a) Transversal filter. (b) Accumulator.

sample as a linear difference equation involving the input and previous outputs. The coefficients of this equation must be determined from the desired filter characteristic. An example of this realization for a "leaky" accumulator is shown in Fig. 4(b). The governing difference equation is

$$o_{t_i} = i_{t_i} + a o_{t_{i-1}},$$

where a is a constant less than 1 specifying the rate of decay of the impulse response. Since the quantities making up this equation are quantized (expressed as a finite number of digits), the indicated computation must be carried out with sufficient accuracy to keep the round-off error within bound. For instance, if a were almost 1, round-off errors could cause to output to diverge, yielding an unstable system.

From this discussion, perhaps the reader might guess that the engineer, rather than the professional programmer, is better suited to formulate such problems for simulation. Indeed, this impression has been confirmed in much of our work. Actually, only the use of engineering and programming skills in combination can avoid studies which are either computationally or physically nonsensical.

Computer Requirements and Estimating Running Time

Simulation of communication systems requires processing of large amounts of data. For instance, ten seconds of speech may be represented by 10^5 samples or about 10^6 bits, and all of these samples must be processed. This situation demands a fast computer with a considerable memory capacity if the processing is to be carried out expeditiously. The IBM-704 is such a machine. Its 32,000-word, random-access memory is organized into 36-bit words. Each elementary operation (addition, for instance) requires 12 μsec, while a complex one such as multiplication takes about 240 μsec. Typically, there may be 20 to 100 operations per sample point in a simulation. Assuming an average time of, say, 50 μsec per operation, it takes between 10 and 50 times as long to process a speech sample as it does to speak it. Such time scales are feasible from the economic point of view. Scales of 500–1000 to 1 are usually prohibitively expensive.

Of course, the exact time scale depends upon the complexity of the system to be simulated. The running time can usually be estimated accurately before writing the program by locating those operations which are most time consuming and which must be performed on every data sample.[9] The total number of these operations for each second of processed speech can be found by multiplying the number of signal samples per second by the number of operations per sample. The time scale is then the number of operations multiplied by the time per operation. For example, the number of multiplications per signal sample for a difference-equation filter simulation is one plus the number of poles and zeros in the analog filter characteristic. For a 4-pole filter operating on 10,000 signal samples per second, the time scale on the IBM-704 would be about 12/1.

The total computation time depends, of course, not only on the time scale but also on the duration of the speech sample. Preliminary listening evaluations can be obtained from as little as 10 to 15 seconds of processed speech. This time is sufficient for four or five short sentences each by a different speaker. Such an amount of data permits qualitative judgments of general fidelity and intelligibility. Formal quantitative measurements may require thirty seconds to a minute or more of material. Comparative evaluations of different systems, or the same system with different parameters, is facilitated by the identical digital speech samples which can serve as inputs to all versions.

The computation time and storage requirements for single pictorials can be estimated from the component 10^4 picture points and the operation time per point. Such preliminary estimates of running times can prevent inappropriate uses of simulation, uses in which the results may not be commensurate with the time and effort expended.

Programming

Programming for simulating signal processing systems is not basically different from programming for arithmetic tasks with, perhaps, two exceptions. Simulation often requires a greater number of logical operations. In addition, the amount of processed data is typically very much greater than both the number of computer operations per data point and the computer memory capacity. Therefore, the lion's share of the programming effort lies in shifting data sequentially from one location to another in the machine's memory—a sort of tedious bookkeeping discouraging to all except the most dedicated, and conducive to a high error rate for all except the most meticulous. The problem is most severe when programming in basic machine language. Here, each operation which the machine is to execute must be individually specified. This exacting require-

[9] M. V. Mathews, "The effective use of digital simulation for speech processing," *Proc. Sem. on Speech Compressing and Processing*, AF Cambridge Res. Ctr., vol. 1; September, 1959.

ment implies that basic is the most general machine language. Using it, the expert programmer can tailor the machine's operation precisely to the task at hand, thereby insuring an efficient computation.

Other programming languages, less demanding but also less efficient than basic, have been devised. They permit the programmer to utilize instructions each of which may specify many machine operations. Typically, these instructions are coded in mnemonic form to minimize errors and to facilitate rapid transcription. A program written in these terms is referred to as a "source" program. A compiling program or "compiler" translates the source program into an "object" program in basic machine language. The object program can then be used to process the data in the desired fashion. Compilers do not usually produce a basic program as efficient as an expert programmer might using ingenious short cuts in basic language. The programming economy achieved, however, often offsets this factor. In addition, a compiler catalyzes access to computational facilities. The aspiring user may require as little as a few hours training to use one effectively.

Fortran, the IBM algebraic compiler, has proved useful for certain speech-recognition studies.[10] A compiler conceived especially for signal processing (using the IBM-704) has been written by J. L. Kelly, Jr., C. C. Lochbaum, and V. A. Vyssotsky.[11] A source program in this language is a sampled-data block diagram description. For this reason, the compiler is called BLODI (BLOck DIagram). Its use is best described by an example. The feedback system in Fig. 5(a) is redrawn in a form compatible with BLODI in Fig. 5(b). Input and output boxes have been added and each block has been labeled with an arbitrary letter. In general, any processing system must be converted to a sampled-data equivalent before BLODI can be used. The source program consists of a three-column listing of the blocks. Column 1 contains the block label, Column 2 is a mnemonic specifying the block function, and Column 3 lists the block parameters and the destinations of the block's "output" connections. The order of the listing is immaterial. A BLODI program for Fig. 5(b) might begin with the input:

A INP B/1

The input block is designated A, its function is denoted by INP, and its output goes to input 1 of block B. The code for the subtractor, block B, is

B SUB C.

The quantizer is assumed to have four representative (output) levels and three input decision (transition) levels [see Fig. 5(a)]. These must be listed in Column 3

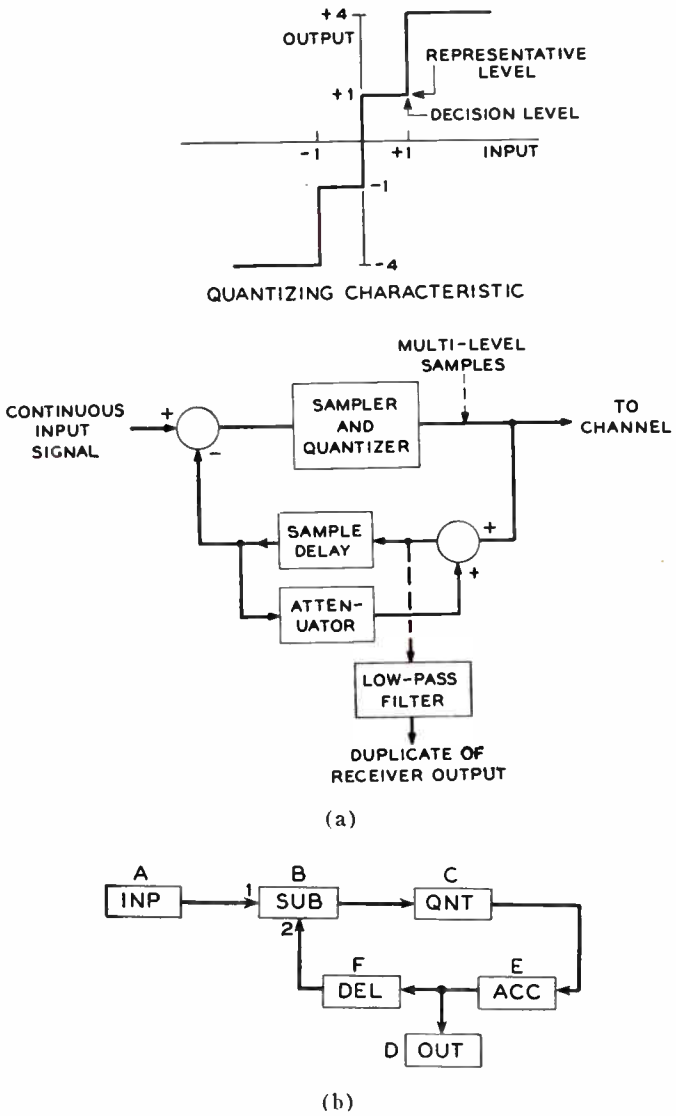


Fig. 5—(a) A differential coder.
(b) Equivalent BLODI diagram.

beginning with the lowest representative level and progressing alternately through all the decision and representative levels. For the quantizing characteristic of Fig. 5,

C QNT −4, −1, −1, 0, +1, +1, +4, E.

Block E is an accumulator with a decay constant, a, and is coded

E ACC a, D, F.

Block F is a delay line with 1 sample delay,

F DEL 1, B/2,

and finally the output is specified,

D OUT −.

These six instructions constitute the source program. From it the compiler prepares a longer object program in which all of the detailed operations and data shuffling

[10] P. B. Denes and M. V. Mathews, "Spoken digit recognition using time-frequency pattern matching," *J. Acoust. Soc. Am.*, vol. 32, pp. 1450–1455; November, 1960.
[11] J. L. Kelly, C. C. Lochbaum, and V. A. Vyssotsky, "A block diagram compiler," *Bell Sys. Tech. J.*, in press.

are automatically programmed.

The internals of BLODI are too extensive to recount here. Clearly, it has available or can compile[12] programs to perform on the signal samples each of the operations specified in Column 2 of the source program. In addition, the compiler establishes the sequence of block operations so that only one output sample from each block need be retained in the computer memory at any time.

BLODI programs generally approach the efficiency of basic language programs, though in some instances they may be only about half as fast. The compiler encompasses a large number of block functions including noise generators, peak and low-level clippers, amplifiers, transversal and difference-equation filters, etc. Other functions can be added by the programmer at will. As many as 800 simple blocks in a single diagram can be compiled. An engineer can learn the formalities of BLODI programming in about two hours. Thus, it affords almost immediate access to a powerful tool for communication research.

To aid in using a computer as a signal generator, Mathews has written a compiler (for the IBM-704) which will produce on command quasi-periodic functions of time of arbitrary waveshape.[13] The basic unit of this compiler is a canonical function generator as shown in Fig. 6. The waveshape is specified by the

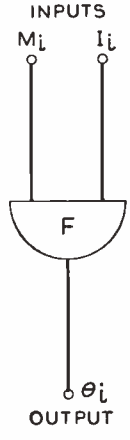


Fig. 6—Canonical generator used in Music Compiler.

function $F(X)$. Its samples, taken at 512 equispaced points (X values), are stored in the computer memory. In generating a wave, samples from this description are printed repetitively on the output tape. The repetition rate is specified by the "scan" parameter, I_i. M_i is a variable scale factor which is used to specify the attack, decay, duration, and location of the wave on the output tape. The ith output sample, θ_i, is related to these parameters by

$$\theta_i = M_i F([X_i] \text{ modulo } 512].$$

Values of X_s are generated according to

$$X_{i+1} = X_i + I_i.$$

Thus X increases progressively in steps of size I_i until it reaches the value 512, then it returns to zero (modulo 512). Thus, if I_i is constant, F is in effect scanned by a linear sweep; each period generated will consist of $512/I$ samples, which at a 10 kc output rate corresponds to $512/I \times 10^{-4}$ seconds.

The output of a basic generator may be printed directly on the computer output tape, or it may supply the input to other unit generators. In this way, groups of generators may be used to form more complex units.

A source program for this compiler begins with a definition of all the unit generators in terms of their F functions and their interconnections. The subsequent portion specifies the intensities, time origins, and repetition frequencies of each waveform segment. This program is well suited for producing musical sounds, and is known as the Music Compiler. It has been used, in addition, for speech production and for the generation of low-frequency control signals.

Compilers, in effect, adapt a general-purpose computer for the solution of particular problem classes. Once such a problem class is defined, it is usually possible to formulate a compiling language which will facilitate programming as well as produce reasonably efficient object programs. Where large numbers of generically similar problems must be solved, such a compiler is practically a necessity.

Studies Utilizing Digital Simulation[14]

Digital simulation has been used for a wide variety of investigations, but perhaps the most interesting concern digital coding of information-bearing signals and duplication of human recognition functions. Also, the computer has been used for generating precisely controlled psychological stimuli. Examples of these studies will be presented in this section.

Digital Coding of Information-Bearing Signals

Digital, or discrete, signals can be transmitted through noisy channels with little or no impairment since such signals can be regenerated exactly, provided the signal-to-noise ratio never falls below a certain threshold value.[6] Information-bearing signals such as speech or the output from a television camera are continuous functions of time. Hence, certain transmission situations require that these be digitally coded. The method most often employed is pulse-code-modulation (PCM). Here, instantaneous amplitude samples of the continuous signal are each represented by a number of

[12] The term "compile" as used here refers to the assembling of a sequence of computer instructions to perform a given function.

[13] M. V. Mathews, "An acoustic compiler for music and psychological stimuli," *Bell Sys. Tech. J.*, in press.

[14] Studies described in this section were carried out on the IBM-704 computer.

binary digits. In order to insure adequate reproduction of the audio or video, the number of digits must often be inconveniently large. This situation arises because PCM codes each sample independently. Thus, novel coding methods tailored to take advantage of dependencies between samples may permit economies.

An important example is the feedback coder in which the difference between the continuous input signal and a replica of the received signal delayed by one sample time is converted into a digital code. A typical coder is shown in Fig. 5(a). The input is bandlimited to W cps and is compared with a reference signal by subtraction. The resulting difference signal is sampled and quantized to produce the discrete code for transmission. The feedback loop accumulates the quantized samples, delays them one sample time, and provides the reference signal. The receiver is an identical accumulator plus a low-pass filter. Thus, the original signal is represented in terms of the difference between its present value and the *previously received* signal value. The terms "delta modulation"[15] and "differential quantization"[16] have been applied to this process. Digital simulation has greatly facilitated comparisons of signals so coded with identical signals pulse-code modulated.

Programming the computer to simulate a differential coder can be done with dispatch using the BLODI compiler. The resulting object program will process a picture in the 100×100 format in about 30 seconds. For speech, the time scale is about 20/1 for those cases in which the computer input sampling rate is sufficiently high. In some delta-modulation systems, the sampling rate may be an important variable. One example is the simple "one-digit" system. Here, the quantizer has only two representative levels; one calling for an increase in the receiver output, the other calling for a decrease. Since the output can change only one "step" per sample, rates much higher than $2W$ may be required to achieve close correspondence between the input and the receiver output. In such cases, the maximum sampling rate afforded by the input-output translator may be insufficient. If so, additional samples may be interpolated by the computer itself. Alternatively, the translator input may be introduced in reduced time scale, achieved, for instance, by a reduced-speed playback of a recording.[2] The effective sampling rate is, thereby, multiplied by the reduction factor. Of course, both methods increase the computing time scale.

The results of this differential coding study illustrate the scope which can be attained with the aid of simulation.[16] Differential quantization has a definite advantage over PCM for transmission of pictorial material. Using the tapered eight-level quantizer (Fig. 7) in the differential coder, pictures such as that in Fig. 8(a) are

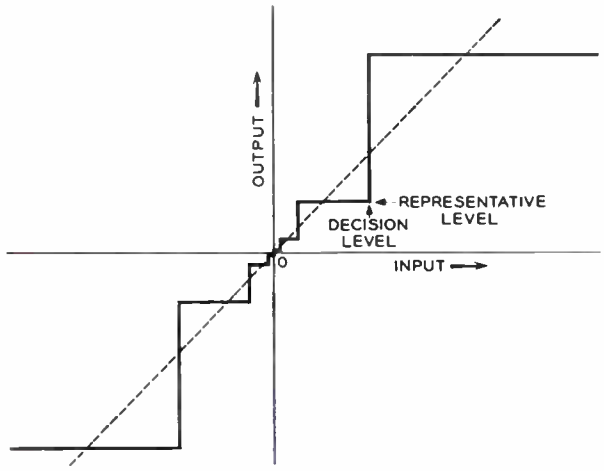
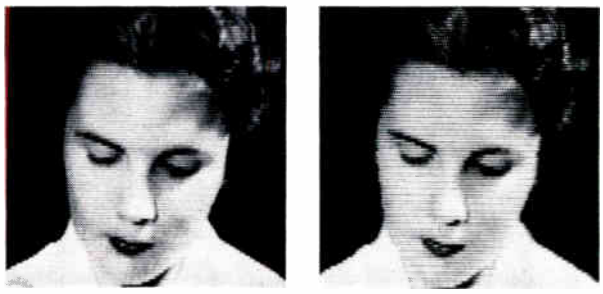


Fig. 7—Quantizing staircase used in differential coding of pictures.



(a) (b)

Fig. 8—Comparison of picture codings. (a) 3-bits/picture point, differential quantizing. (b) 3-bits/picture point, pulse-code modulation.

achieved. Compared to the original, Fig. 2, little difference may be noted except for a slightly ragged contour along the left edge of the face. Since this version of delta-modulation requires three binary digits per picture point, a three-digit PCM representation requires the same total number of pulses per second for transmission. Note the objectionable contouring in the picture so coded, Fig. 8(b).

An analysis of this differential coder indicates that the error (difference between the original and the reproduced picture) is concentrated in areas where the brightness is changing drastically from point-to-point; that is, in areas of fine detail. In regions of constant brightness, the picture is rendered quite faithfully. Subjectively, this distribution of the error is much preferable to the more uniform distribution typical of PCM.

Several refinements of differential coding have been investigated.[16] One makes use of two-dimensional rather than one-dimension differences. It can use as the feedback reference signal either the receiver output delayed by one sample or by one scanning line. A logical test on past picture points determines which interpolation mode gives the best fit at each point of the picture. When coupled with a quantizing staircase which varies according to the instantaneous value of the reference

[15] F. de Jager, "Deltamodulation," *Philips Res. Repts.*, vol. 7, pp. 442–466; 1952.

[16] R. E. Graham, "Predictive quantizing of television signals," 1958 WESCON Convention Record, pt. 4, pp. 147–157.

signal, this scheme considerably improves the reproduced picture.

Another method of digital encoding represents the continuous signal in terms of its extremes (maximums and minimums) and the time between them. The value of such a code for speech and picture transmission has been studied by stimulation. While the results are of interest in themselves, they will not be reviewed here. Interested readers are invited to refer to the appropriate publications.[17,18] Suffice it to say, the simulation technique enables an economic study of this coding, which, while conceptually and computationally simple, would have called for extensive special-purpose equipment.

Recognition of Signal Properties

Many different physical events are regarded as equivalent by the human observer. For instance, specimens of the word "one" as spoken by ten different people will evidence gross acoustical disparities; yet a listener can recognize all versions as symbolizing the intended numeral. Such categorization depends upon abstract properties of the acoustic event, and is closely related to the problems of character recognition, and reduced bandwidth transmission of continuous signals.[8] Paradigms aimed toward machine duplication of human recognition behavior usually involve a group of measurements on the event to be categorized. These are then subjected to appropriate decision logic.

Even such simple distinctions as speech vs silence involve elements of recognition since the noise energy in "silence" is often greater than in some speech sounds.[8] Another significant distinction is that between classes of speech sounds. For instance, a person ordinarily uses two different mechanisms to generate the necessary acoustical energy for speaking. The vocal cords with their quasi-periodic vibrations supply the vowel-like sounds (*voiced* sounds). Turbulent airflow at a constriction appropriately formed in the vocal tract provides the random noise energy associated with sounds such as *s* and *sh* (*unvoiced* sounds). The distinction between these two modes of generation, as well as the identification of silent intervals, is fundamental to both speech bandwidth reduction and speech recognition. For these purposes, these distinctions must be made automatically by a device operating solely on the speech signal itself.

Systematic investigation of such devices using conventional equipment is tedious because observation of the nonrepetitive dynamics is difficult, and input conditions can be reproduced only with great care. Simulation alleviates both of these problems. Computer printouts and tabulations can provide an accurate log of the processed results, while the input speech can be reproduced precisely from a digital recording.

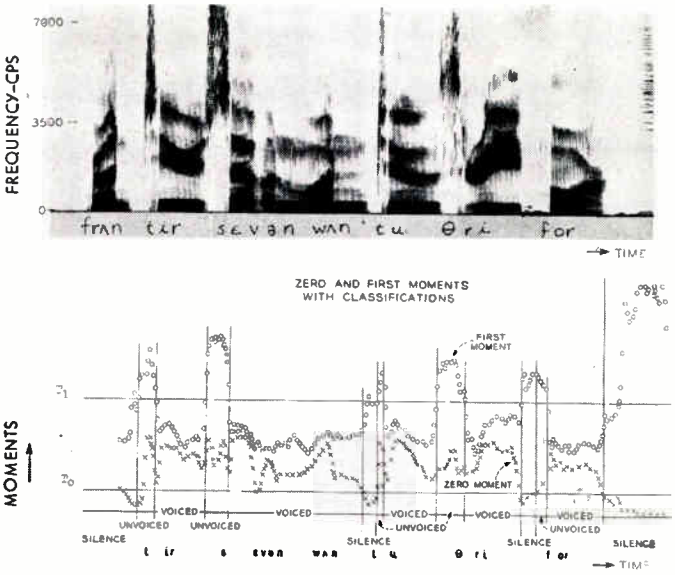


Fig. 9—Operation of voiced, unvoiced, silence recognition on speech spectra data.

One investigation of voiced-unvoiced-silence discrimination utilizes measurements of the normalized zeroth and first moments of the speech wave followed by decision logic.[19] The computer input is taken from the sound spectograph (Fig. 3) which produces a running amplitude spectrum display as shown in Fig. 9. This display specifies the approximate rms value of the speech (indicated by increasing density of marking) at each time-frequency intercept.[8] As this spectral information is taken into the computer, it sums and groups the data into 70 cps by 7-msec blocks. The moments, M_0 and M_1, are computed by:

$$M_0 = \sum_i X_i \qquad M_1 = \frac{\sum_i iX_i}{\sum_i X_i},$$

where the X_i's are the rms speech amplitude values in each block, and the index i runs over the frequency axis. The average moments are computed by summing over the time index j and averaging

$$\overline{M_0} = \frac{1}{n}\sum_j M_0 \qquad \overline{M_1} = \frac{1}{n}\sum_j M_1$$

where the summations include only those n values of M which exceed an arbitrary threshold value. The normalized moments are:

$$M_0' = \frac{M_0}{\overline{M_0}} \qquad M_1' = M_1 - \overline{M_1'}.$$

Values of M_0' and M_1' are plotted beneath the spectrographic display of Fig. 9. One simple decision logic

[17] M. V. Mathews, "Extremal coding for speech transmission," IRE TRANS. ON INFORMATION THEORY, vol. IT-5, pp. 129–136; September, 1959.

[18] B. Julesz, "A method of coding television signals based on edge detection," *Bell Sys. Tech. J.*, vol. 38, pp. 1001–1020; July, 1959.

[19] C. C. Lochbaum, "Segmentation of speech into voiced sounds, unvoiced sounds, and silence," *J. Acoust. Soc. Am.*, vol. 32, p. 914; July, 1960.

examines each moment with respect to a threshold value. Separation of the speech into voiced, unvoiced, and silent intervals is accomplished according to Table I. There is in addition a continuity requirement, namely, intervals must be at least 28 milliseconds in duration, otherwise they are assigned to the same category as the adjacent left-hand segment. The decisions corresponding to this process are marked in Fig. 9. They define quite accurately the appropriate regions of the speech.

TABLE I

	M_0 Below T_0	M_0 Above T_0
M_1 Below T_1	SILENCE	VOICED
M_1 Above T_1	SILENCE	UNVOICED

Programming for this simulation was done in Fortran and the time scale was about 20/1. This study is typical of several speech recognition studies aided by simulation.[20] Others have, however, included spectral analyses of waveform inputs as well as operations directly on spectral input data.[21–23]

In the pictorial realm, the recognition approach has been used to remove additive noise selectively from a picture. This process depends upon analysis of local picture properties, and is called "noise-stripping."[24] Its basic properties are easily established by digital simulation. One basic scheme considers a 3×3 matrix of picture samples spaced at the Nyquist interval ($1/2W$ seconds) along the scanning (horizontal) direction and at the line spacing in the vertical. As shown in Fig. 10, the nine samples can be formed into six subgroups, designated by Roman numerals each of which represents the sum of its three sample values. The "flexure" of the region covered by the matrix is:

$$\Delta_x = \tfrac{1}{6}(\mathrm{I} + \mathrm{III} - 2\mathrm{II})$$

$$\Delta_y = \tfrac{1}{6}(\mathrm{IV} + \mathrm{VI} - 2\mathrm{V}),$$

where Δ_x and Δ_y are the second finite-differences of the picture brightness surface in the x and y directions. These quantities can be compared with a threshold value δ, which is typically a small fraction of the picture brightness range. The outcome of this comparison

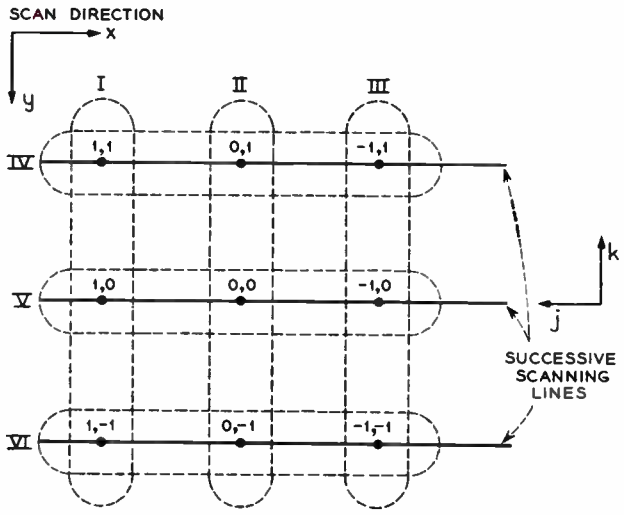


Fig. 10—Picture-point matrix for noise stripping studies.

specifies one of three smoothing modes to be applied to the point in the matrix center. Table II summarizes this process.

TABLE II

Comparison Result	Local Surface Property	Value Substituted for Center Point	Noise Reduction
$\Delta_x < \delta$ $\Delta_y < \delta$	Planar	$\frac{\mathrm{I} + \mathrm{II} + \mathrm{III}}{9}$	10 db
$\Delta_x > \delta$ $\Delta_y < \delta$	Flexure in x Direction	$\frac{\mathrm{II}}{3}$	5 db
$\Delta_x < \delta$ $\Delta_y > \delta$	Flexure in y Direction	$\frac{\mathrm{V}}{3}$	5 db
$\Delta_x > \delta$ $\Delta_y > \delta$	Flexure in Both Directions	Same as original	0 db

For a planar surface, two-dimensional low-pass filtering is used. For a surface flexed in one direction, low-pass filtering in the opposite direction is appropriate. No filtering is applied to a surface flexed in both directions. This and similar transformations on pictures accomplish considerable noise reduction. Typical results from a simulation study are shown in Fig. 11. Simulation is at its best in a study of this kind, a study which is computationally simple with many variations on the original theme to be examined. Each picture requires about 30 seconds of computer time for processing. Thus, many different versions can be run economically.

The Computer as a Signal Generator

Through the medium of the data translator, a computer can be used effectively as a signal generator. From appropriately written output tapes, the translator can produce visual and auditory signals for subjective con-

[20] E. E. David, Jr., M. V. Mathews, and V. A. Vyssotsky, "Recognition of voicing, voice pitch, and formant frequencies with a digital computer," *Proc. Third Internatl. Congress on Acoustics*, Elsevier Publishing Co., Amsterdam, The Netherlands; 1960.

[21] M. V. Mathews, J. E. Miller, and E. E. David, Jr., "Monaural phase effects in speech perception," *Proc. Third Internatl. Congress on Acoustics*, Elsevier Publishing Co., Amsterdam, The Netherlands; 1960.

[22] J. E. Miller, M. V. Mathews, and E. E. David, Jr., "Pitch synchronous analysis of vowel sounds," *J. Acoust. Soc. Am.*, vol. 31, p. 1564A; September, 1959.

[23] J. E. Miller, M. V. Mathews, and E. E. David, Jr., "Pitch synchronous spectral representations of voiced speech," *J. Acoust. Soc. Am.*, vol. 32, p. 913; July, 1960.

[24] R. E. Graham, "A noise-stripping process for picture signals," presented at the SMPTE Conv., New York, N. Y.; October 7, 1959.

(a) (b)

Fig. 11—Typical results from simulation of noise stripping operation. (a) Unprocessed. (b) Processed.

sumption. As reviewed in an earlier section of this paper, the Music Compiler is an effective aid in writing such tapes when quasi-periodic, music-like sounds are desired. Another application is the generation of stimuli for psychological exploration of perceptual mechanisms.

Julesz found this technique quite effective in his investigation of depth perception in vision.[25] The human observer uses many factors, or cues, in his environment to deduce the relative and absolute distance of objects in his field of view. Among them are perspective, familiarity with the known size of objects, interposition,[26] monocular parallax,[27] and binocular parallax.[28] One significant distinction opposes the monocular cues with the binocular of which there is only one. In studying the latter, stimuli with no monocular cues and controlled binocular parallax are required. Of course, natural scenes contain all the cues in varying proportions. In his study of binocular parallax, Julesz solved this problem by having the computer generate his stimuli.

He programmed it to generate rasters of dots whose brightness was a random function of the dot position. In order to see a figure in depth, two such patterns must be presented; one to each eye. If the two are identical, the raster will appear flat when the two fields are fused to a single image in the brain of the viewer. If some sector of the dots in one pattern is shifted horizontally a small distance with respect to the same dots in the other, then the shifted sector will appear to be in a different plane from the background. The separation between this plane and the background depends upon the distance shifted. These computer-generated fields permit the amount of binocular parallax to be controlled accurately. Furthermore, other cues are absent. This convenience permits a systematic investigation of binocular information in depth perception. Stimuli of this type can be generated in less than 30 seconds computer time.

[25] B. Julesz, "Binocular depth perception of computer-generated patterns," *Bell Sys. Tech. J.*, vol. 39, p. 1125; September, 1960.
[26] Objects in front often obscure parts of objects behind.
[27] Near objects seem to move more rapidly than far objects when the observer himself is in motion.
[28] The two eyes see slightly different views of the world.

Concluding Remarks

Computers are proving to be flexible tools in research on human communication. They provide a ready means for uncovering the fundamental properties of any well-thought-out signal processing or coding scheme. This approach owes its efficacy, first, to the high-quality computer input-output translators now available for a range of signals, and, second, to high-speed digital computers which bring significant signal processing tasks within a reasonable time scale. Of equal significance is the creation of compiling programs. These are the "open sesame" to computers for any interested engineer. A well-written compiler requires little training to use effectively, and programming time is often negligible.

However, enthusiasms for simulation studies of communication systems must be tempered by a few caveats. Regardless of the rapid strides toward increased computer speeds and availability, the economics of simulations should not be taken for granted. Some problems will undoubtedly prove to be unsuitable. For instance, the study of apparent (subjective) motion in a sequence of rapidly projected visual images is a strain on present capabilities. Though suitable sequences of picture frames could be processed, the resulting time scale seems excessive. On the assumption of 25 frames per second of viewing time, and one minute of computer processing on each frame, the time scale would be 1500/1. Such an extensive problem should not be undertaken lightly.

A lack of intimacy is voiced by those engineers who like to "feel the knobs" on their experimental equipment. This objection is a very real one since in simulations it may be difficult to gain insight into the workings of a signal processing scheme. Often, a number of hours elapse between the adjustment of a processing parameter and the observation of the corresponding effect. Thus, the valuable interplay between the engineer and his equipment is difficult to establish. This situation promises to be remedied by the current trend toward real-time computer input-output. When generally accessible, this closer coupling between the computer and the engineer holds promise of a near-revolution in experimental communication research.

Problems sometimes arise because computationally

simple operations may defy duplication outside the digital realm. If a coding scheme is shown by simulation to possess desirable properties, then construction of efficient and economic equipment incorporating that coding may be appropriate. If so, the computer program or the principles incorporated in it must be converted into a practical system. Unfortunately, not all programs yield easily to such metamorphosis. Thus, an additional nontrivial step beyond simulation may be required. On the other hand, many simulations concern basic principles drawn from analyses of an existing or proposed system. Here simulation results are often directly applicable without further elaboration.

The judicious use of computers to simulate systems and generate signals which can be evaluated subjectively is catalyzing many areas of research—areas previously hampered by the necessity for excessive amounts of instrumentation. Perceptual research in pattern recognition, signal coding, and sensory psychology are benefiting from a closer association of theory and experiment than heretofore feasible. At some distant time, the terminals of information transmission systems may well turn out to be special-purpose digital computers incorporating the principles established by experiments on general-purpose computers. The speed of digital circuitry within the available technology is increasing at a startling rate. We can confidently look forward to real-time digital processing of speech and pictorial signals.

Acknowledgment

In the preparation of this paper, the author has drawn freely on the work of his colleagues in the Visual and Acoustics Research Department of the Bell Telephone Laboratories. Only through their industry and ingenuity could the simulation techniques described above have come into being. In particular, the contributions of Miss J. E. Miller and Mrs. C. C. Lochbaum, as well as R. E. Graham, B. Julesz, J. L. Kelly, Jr., M. V. Mathews, H. S. McDonald, and V. A. Vyssotsky, are noteworthy. To these and the many other contributors, the author expresses his gratitude.

Correction

In "A Unified Analysis of Range Performance of CW, Pulse, and Pulse Doppler Radar," by J. J. Bussgang, P. Nesbeda, and H. Safran, which appeared on pages 1753–1762 of the October, 1959, issue of Proceedings, Lee E. Davies, of the Stanford Research Institute, has called the following to the attention of the *Editor*.

In (33), on page 1759, the plus sign should be a division sign.

European Electronic Data Processing—A Report on the Industry and the State-of-the-Art*

ISAAC L. AUERBACH†, FELLOW, IRE

To help assure that the U. S. computer engineer has good visibility on the European scene, I. L. Auerbach was asked to undertake the task of surveying the many computer developments in that part of the world. Engineers will find useful information in this paper, in which several of the most promising technical developments have been identified and described briefly, and the characteristics of most of the computers in operation and in development are summarized.

—*The Guest Editor*

Summary—**Information processing activities in Western Europe are developing at an increasingly rapid pace. Newly created companies and many of the established business machine and electronic firms are entering this burgeoning field. A first-hand tour of major industrial and academic groups in Western Europe reveals important progress in equipment design and manufacturing techniques, as well as significant advanced development work.**

The United States is ahead of Western Europe, due primarily to a greater over-all research and development effort. However, there is no national boundary for creative ideas; European laboratories are developing new techniques and products for the world market, ranging from peripheral equipment to complete information processing systems.

The survey of European activities is presented in three parts: an introduction, details of some important technological developments under way, and a detailed review of the characteristics of European computing systems. The technological developments include fixed high-speed memories, magnetic thin films, random-access memories, pattern recognition, learning machines, hydraulic logic, and problem-oriented languages.

I. Introduction

IN a mere fifteen years the electronic digital computer has risen from a laboratory curiosity to a vital element of present-day civilization. The phenomenal growth of the computer industry in the United States has been the subject of many articles, both technical and popular. But too little attention has been given to the work going on in other countries. Indeed, very basic research and development is being conducted everywhere in the world. It is therefore of inestimable value to keep in focus these activities and recognize the magnitude of the ever-growing field.

While virtually every nation today is engaged in some sort of computer activity, the most significant work being done is found in the United States and Western Europe. Several European countries, notably Great Britain, France, Sweden, The Netherlands and Germany, have been active for many years and have well-established research groups and manufacturing concerns. Other nations entered the field more recently and are aggressively forging ahead in basic research and product development.

In an effort to learn first hand just what the Western Europeans are doing in information processing, the author spent seven weeks touring the continent and Great Britain, visiting virtually every major area of computer activity. Through exhaustive interviews, tours of facilities, and examination of equipment the author has prepared this presentation of the technical state of the art in Western Europe.

II. Technological Developments

All over Western Europe important research is being conducted by both commercial and government organizations in advancing the state of the computer art. Some of the work parallels that being done in the United States and elsewhere, while in other cases European groups are pursuing entirely new ideas. Although not all advanced developments are revealed to an outside observer, the author was fortunate in seeing much original and interesting work in process. The items of particular interest are noted below, categorized by technical subject matter, so that the results of several organizations working in the same area may be grouped together.

Fixed High-Speed Memories

There is very interesting development work in Western Europe in the area of fixed high-speed memories, including both technique developments and application studies. Two techniques are receiving particular attention: wired-core memories, and fixed memories using magnetic rods.

Wired-Core Memories: Wired-core memory techniques, well known but little used in the United States, are extremely popular in Western Europe. Almost every modern European computer uses some form of wired-core storage.

In wired-core storage, a wire is threaded through a core matrix in a pattern which represents stored information. Such memories are characterized by nondestructive readout, with higher speed (under 1 μsec

* Received by the IRE, November 2, 1960. The work reported here was sponsored in part by the Office of Naval Research under Contract No. Nonr-3235(00).

† Auerbach Electronics Corporation, Philadelphia, Pa.

switching time is typical) and lower cost than coincident-current memories. Wired-core memories are used to store various fixed or seldom-changed data; *e.g.*, start-up sequences, basic programs for communicating with peripheral equipment, basic subroutines such as standard trigonometric functions, program constants, and, in some cases, entire operating programs. The technique is particularly useful in microprogramming, where the cores control logical gates and the structure of the wired-core matrix defines the logical characteristics of the computer. Industrial control is one of the areas where wired-core techniques have great potential application.

Telefunken in Germany uses E-shaped wired cores in the TR-4, a large-scale, high-speed, solid-state computer. One slot of the E core stores a ONE and the other slot stores a ZERO. A storage capacity of 256 words is achieved with 52 cores and 52 diodes mounted on a single plug-in card threaded with 256 wires. Telefunken claims an access time of 1 μsec with a 30 per cent cost saving over coincident-current systems.

In Holland, N.V. Electrologica uses wired-core storage in the X1 computer. Organized in blocks of 64 words, the storage is used for peripheral equipment subroutines. N.V. Electrologica has automated the assembly of the wired-core matrices with punched paper tape.

Most other European groups are active in wired-core development and application, particularly Elliott Brothers in England who have utilized the technique for both serial and parallel storage in process-control computers.

Fixed Rod Memories: The advantages of wired-core memories are retained and the disadvantage of inflexibility of modification overcome in a new memory development at the University of Manchester in England. Using small magnetic rods inserted in a wire mesh, this 8192-word memory has achieved the highest operating speed of any known memory of equal size being built into a computer anywhere in the world: 0.3 μsec cycle time and 0.15 μsec access time have been achieved in laboratory tests.

The fixed rod memory was developed by Professor T. Kilburn for use in the radically new MUSE computer currently under development. The memory has a capacity of 8192 words of 48 bits each. A smaller version, 256×256, using parts supplied by Manchester, was built at the University of Pisa in Italy and is operating in the C.E.P. computer there.

The fixed rod memory is constructed from a woven mesh of copper wire mounted over a soft plastic. Ferrite rods 1 mm in diameter and 5 mm long are placed in the interstices of the mesh wherever a ONE is to be stored. The woven mesh for a 4096-word memory is 3 feet wide and 8 feet long with $\frac{1}{16}$-inch grid spacing. The mesh, folded in half over the plastic, results in a two-sided frame 3 feet by 4 feet. There are 256×768 loops in the mesh, organized as 256×16 words of 48 bits each.

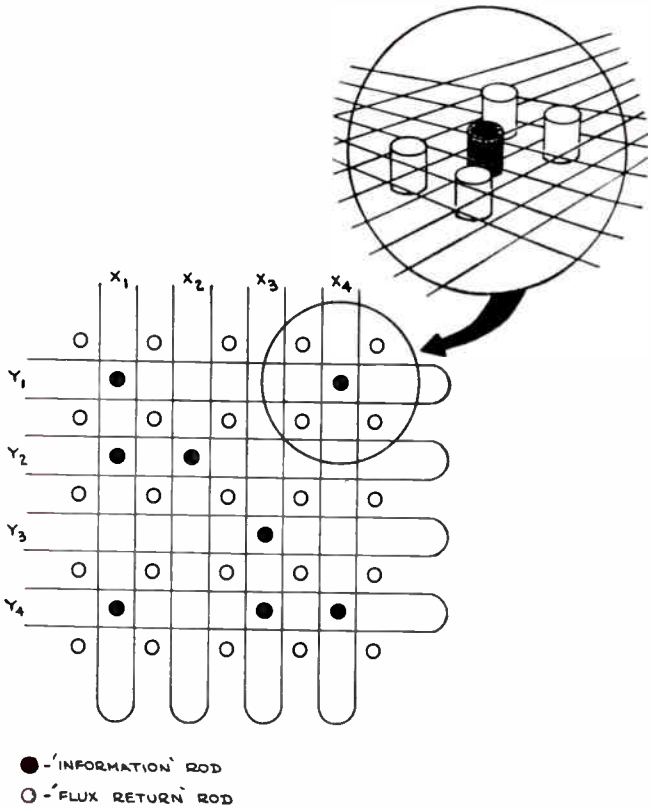


Fig. 1—Kilburn fixed rod memory technique.

The wire mesh is formed into loops (see Fig. 1) by cutting one horizontal and one vertical edge of the mesh. When a ferrite rod is inserted within both a horizontal and vertical loop, it couples these loops and may be detected. To provide a flux return path for the magnetic field and to reduce noise, identical rods are inserted in all of the noncoupled loops.

The memory is organized by switching 48 sense amplifiers to a selected 1-out-of-16 group of 48 loops on the vertical axis. A single driver switched to one of the 256 loops on the horizontal axis provides the interrogation.

Magnetic Thin Films

Research on magnetic thin films is under way in many laboratories throughout Europe. Two of the organizations visited—IBM Zurich, and ICT in England—made some information available about their programs so that a brief review of these programs serves as an indication of the state of the art.

At the IBM Laboratories in Zurich a major program on magnetic thin films is divided between two groups: one engaged in metallurgical methods for depositing and heat-treating ferromagnetic films, and the other concerned with the switching properties of the films and their application in logical devices and memory.

IBM's investigations show that ferromagnetic resonance of a thin film occurs at 1 kMc, which may establish the upper boundary for speed. The possibility of making use of the ferromagnetic resonance in new cir-

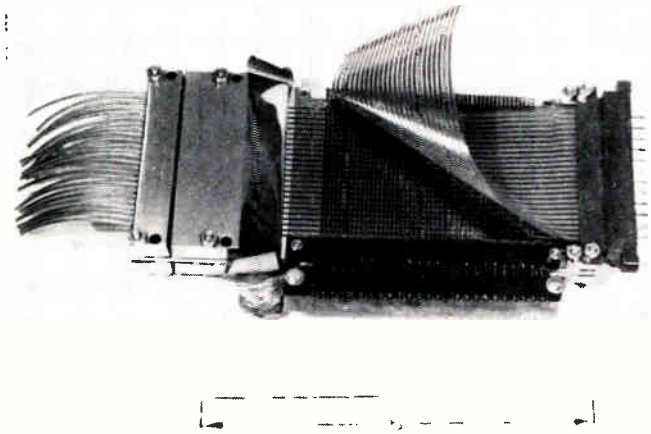


Fig. 2—ICT thin film memory, laboratory model.

cuits is being studied. Experiments have been conducted on nanosecond switching of film 1000 angstroms thick and 1 cm square. Output signals of up to 0.1 volt have been obtained comparable to signal amplitudes derived from small ferrite cores. Memory planes are being tested.

Through microscopic examination of the thin film under polarized light, both the IBM and ICT researchers have been able to observe the domain wall switching and have discovered that the domains "lock up" on impurities.

In England, International Computers and Tabulators Ltd. is active in thin film research. ICT's main emphasis is on improving the reproducibility of the desirable properties of the magnetic thin film, to permit economical manufacture of large-scale memories with cycle times under 100 nanoseconds. Metallurgical research at ICT has produced a new alloy called Gyralloy which is deposited by vacuum evaporation onto an oxidized aluminum substrate. The presence of a conductor so near the film gives a good signal-to-noise ratio and reduces the drive impedance, because magnetic flux cannot penetrate into the conductor in the duration of the selection pulse. ICT claims no harmful damping effect on the magnetic reversal with this arrangement.

An experimental thin film memory assembly built by ICT is shown in Fig. 2. The Gyralloy is deposited on the aluminum substrate in a continuous film—not in spots. An insulating layer is applied over the film; over this are printed circuit copper conductors, which form the read winding. At right angles to the read winding are coils of flat wire, with 10 turns per coil, again at right angles to these coils is a set of conductors embedded in a plastic sheet, for x/y control.

Other European groups engaged in thin film research include Siemens & Halske and the Max Planck Institut fuer Physik in Germany; and Plessey, Mullard Radio Research Laboratory, and the University of Manchester in England.

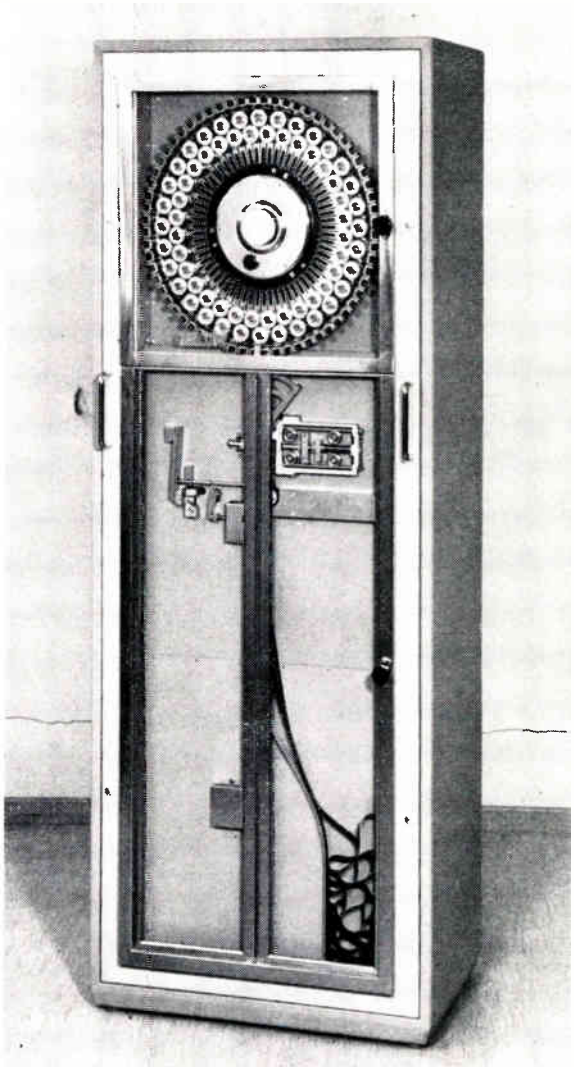


Fig. 3—FACIT ECM 64 Carousel memory.

Random-Access Memories

The problem of providing random access to large quantities of stored data has been attacked many ways in the United States and Europe. Two interesting developments in this area are the Carousel memory developed by Facit in Sweden, and the K-10 memory built by Standard Elektrik Lorenz in Germany.

The Carousel (Fig. 3) permits access to any of over five million stored decimal digits in an average of less than two seconds. It contains 64 small reels of 8-channel magnetic tape mounted in two concentric circles on a wheel. A given reel of tape is read by indexing the wheel so that the selected tape is at the bottom. A weight attached to the end of the tape drops down past an air-gap read/write head to an unwinding bin. Photoelectric sensors control start, stop, and rewind. A fully loaded Carousel wheel can be replaced in about ten seconds.

Standard Elektrik Lorenz' K-10 (Fig. 4) takes a somewhat different approach to the random-access storage problem. It provides a storage capacity equal

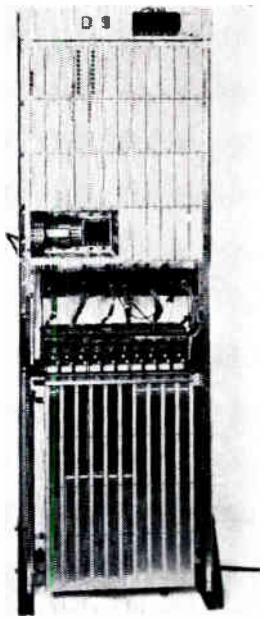


Fig. 4—Standard Elektrik Lorenz K-10 memory.

to that of a standard tape transport with a 1000-meter tape, but with an access time of only 2.5 per cent of a conventional unit. The K-10 has ten bins, each containing 100 meters of tape. Associated with each bin is a read/write head and a drive mechanism. The tapes normally rest with the midpoint over the head, detected photoelectrically. A typical application uses a crossbar switch, four tape control units, and nine K-10's for simultaneous reading or writing on any four of 90 tapes.

Pattern Recognition

The most outstanding development work observed in character recognition in Europe is being conducted at the Technische Hochschule in Karlsruhe, Germany. Solartron in England has produced commercial equipment for character reading. BULL in France, EMI in England, and three German manufacturers are also working in equipment development.

The Karlsruhe approach, sponsored by the German Post Office, is a unique combination of analog and digital techniques. The initial input of a character is straightforward; a flying spot is used to scan the pattern at a rate of 3000 characters per second and the output signal wave is converted to bits indicating black or white areas. The result of a scan is 200 bits (20 vertical by 10 horizontal). A two-dimensional 200-bit shift register stores this image of the original pattern as it develops. The system is currently limited to 14 characters; continued development is expected to increase this number.

The first phase of processing centers the character image. First the character image is transferred from the shift register to an array of 200 flip-flops which in turn feed a resistor matrix. The resistors are so interconnected that there are four output currents: left side, right side, top and bottom. The character is scanned and repeatedly reloaded into the flip-flop array from the shift register with each vertical synchronizing pulse. The character effectively moves from left to right across the array until the left and right currents are equal. This is defined as horizontal centering.

The flip-flops are cross-connected so that vertical shifting of the character image is possible. Then the character is positioned so that the top and bottom currents are equal. This is defined as vertical centering. The horizontal and vertical "centering" places each character image in its unique standard position.

The next phase of processing, which has been thoroughly analyzed but only partially implemented in hardware, is the extraction of salient features from the pattern. Since the currents flowing in the resistors represent the "potential field" (Fig. 5) of the character stored, it is possible to deduce the key shape features of the character from properties of this potential field. For a simple example, a node with a maximum current inflow indicates the end of a line or an isolated point.

An analysis of first and second differentials of current flow at a point indicates the location and curvature of a line. The sign of the first differential indicates whether the character lies to the right or left of the test point. The sign of the second differential indicates whether the line is straight, curved away from or curved towards the test point (see Fig. 6). Note that these currents and differentials are analog, not digital phenomena.

To test the first and second differentials, some novel circuits have been devised. The most novel test uses a differential transformer technique. Leads from adjacent nodes of the resistor matrix are wound around ferrite cores with proper numbers of turns and direction. There are also sense and interrogate windings on the core.

The core is saturated in one direction or the other depending on the sign of the second differential. An interrogate pulse only produces an output for a positive second differential.

The figures to be recognized are described in terms of the location of major straight lines, the direction of curvature in the upper, middle and lower portion of the figure, and the location of line terminals. The present recognition criteria were selected experimentally and wired into the equipment.

Solartron's commercial development is the ERA (Electronic Reading Automation), which converts printed characters to punched cards at the rate of up to 240 characters per second. The accuracy claimed is better than one in 10,000 rejects and one in 1,000,000 errors. Four units represent the necessary equipment for recognition: the scanner, memory, logic, and document handler. The latter provides only for cash register tally rolls, but developments are in process for handling separate documents. One of the Solartron ERA systems

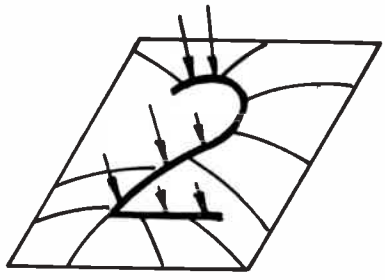


Fig. 5—Two-dimensional potential field for the character "2."

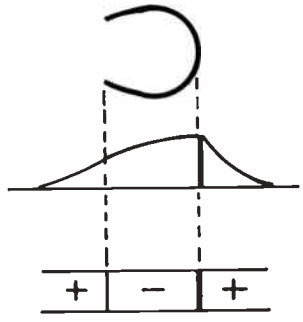


Fig. 6—Determining character shape by analysis of second differential.

was observed undergoing final factory tests in July, 1960.

The ERA is designed to read numerals (0–11), plus some alphabet characters and special signs. (Models are under development for sensing additional characters.) The sensor uses a flying-spot scanner and a photoelectric pickup. Each character is prescanned twice. The first prescan establishes peak white and black levels which are used to clamp the limits to a narrower range than would otherwise be necessary, thus compensating for smudging and other irregularities. The second prescan establishes *x-y* limits to center the character; then a final scan transfers the character information into ferrite core storage. Each character has its own criteria stored within the machine; both acceptance and exclusion criteria are used for identification.

Three of the larger German computer manufacturers (Telefunken, Siemens, and Standard Elektrik Lorenz) have been also working on character recognition equipment, in an effort to receive contracts for equipment to mechanize the German Post Check system and the German Post Office letter sorting problem. Telefunken has a pilot model reader for American Banking Association characters under test.

Electric and Musical Industries (EMI) in England is developing a character reader named FRED (Figure Reading Electronic Device).

Machine Learning

Exploratory work in learning machines, most of it in the early stages, is being pursued by several European groups, notably the Technische Hochschulen in Vienna, Austria, and Karlsruhe, Germany, and Manchester University and Solartron in England. Unfortunately, little information is available on these activities, other than an indication of the general approach each group is taking.

In Vienna, programs are being developed for the MAILUEFTERL computer to create a new type of conditioned reflex automaton. An improved model of Shannon's maze runner has also been developed, with the ability to detect circle-ways, dissolving them into parts of the solution.

The Karlsruhe group has devoted much study to the philosophy of learning machines and has produced excellent articles summarizing the accomplishments in the field. Their work, like that in Vienna, is concerned primarily with conditioned reflexes and is closely related to their developments in character recognition. One approach to the conditioned reflex problem uses the multistep characteristic of ferrite cores in a matrix, with the sensors connected to one axis and the reactors to the other. By repeatedly exposing the sensors to the situation, a conditioned reflex is built up so that, when the reactors are interrogated, a learning-type reaction is obtained. In addition to character recognition, applications of this technique are seen in information retrieval and automatic speech recognition.

At Manchester University, one problem under investigation involves control of a configuration of water tanks in which some drain into others, some drain into a sink, and some are filled from an external source. All flows are controlled by valves, some of which operate randomly, while others are controlled by a learning machine. The machine is told only which tanks are too full or too empty and must try to maintain the proper levels without knowing how the tanks are interconnected or what the valves control. Such a machine may find application in chemical processing.

Another learning problem under study at Manchester involves the memory organization of the MUSE (ATLAS) computer. To achieve, in effect, a huge fast-access memory, MUSE combines a magnetic core memory and a drum memory such that information is transferred between the memories without direction from the programmer. The computer's task is to keep those data which are frequently requested in the immediate-access core memory, with less used data in the drum. When a given block of information is requested, it is read out immediately if in core storage, or transferred from the drum in exchange for an unused block in the core memory. Learning criteria are being developed so the computer can maintain the best compromise of storage locations at all times.

Solartron's association with Rheem Manufacturing Company in the United States has resulted in the development of EUCRATES, an experimental teaching and learning machine. Learning is accomplished by storing the number of hits in correlating a keyboard and a selected light. As the number of hits is increased, the "pupil" part of EUCRATES "learns" the correlation,

and eventually selects the right key. To simulate human behavior, a "forgettery" control is introduced that requires continuous enhancement. The "pupil" learns under control of the "teacher" part of the equipment, or on a trial-and-error basis without outside assistance.

Solartron has also developed a teaching machine, the SAKI (Solartron Automatic Keyboard Instructor) which trains operators in the use of punch-card equipment. It consists of a keyboard, a power supply, and a control unit. On the latter are two indicators, one corresponding to the location of the keys, and the other a card with rows of random numbers and/or letters. In operation, a light shines behind each of the characters on the card, in sequence. The corresponding keyboard indicator is also illuminated, telling the trainee which key to depress. As the proper buttons are depressed, the keyboard indicators grow dimmer and the rate is increased. If errors are made, the rate is reduced and the indicators gradually come back on again.

Hydraulic Logic

One of the most interesting and unusual developments in Europe is the work being done at IBM's Zurich laboratory on hydraulic logic. This is exploratory work aimed at establishing basic techniques rather than building hardware.

This application of hydraulic techniques is quite different from the conventional usage where high power is used to move heavy external loads. In hydraulic logic there is no external load, thus permitting lower pressures and much smaller elements. Miniaturization also permits higher speed, and hydraulic elements compete favorably with relays in this area of performance. Laboratory models of a free-running multivibrator have been operated at 300 cps, and calculations indicate that, with care, 2000 cps operation can be obtained.

Although hydraulic elements can take many forms, the devices built by IBM Zurich use "spool" valves, shown in both schematic and symbolic form in Fig. 7. In this simple building block, three inputs (A, M, and N) and one output (X) are provided. Logical signals in the form of high and low pressure (corresponding to the voltage no-voltage levels in electronic binary logic) are applied to the inputs. A static medium pressure is applied to m. Thus the pressure at A determines the position of the valve, which in turn defines, together with the input at M or N, the pressure at X. If high pressure is regarded as logical ONE and low pressure as logical ZERO, the performance is described as

$$X = MA' + NA.$$

The logical capability of the hydraulic element is thus greater than that of a single transistor.

By providing a feedback path from X to A, a bistable element is created. These simple configurations—the gate and the bistable device—are the basis for all other hydraulic logic elements. Gating networks, shift registers, counters, matrices, and multivibrators have been built and successfully operated. Fig. 8 shows the logical diagram of a scale-of-two counter and a working model of this unit. Fig. 9 shows two multivibrators, with bores of 5 mm and 1 mm, respectively. The larger models are executed in clear plastic to permit direct visual observation of operation using stroboscopes and high-speed photography.

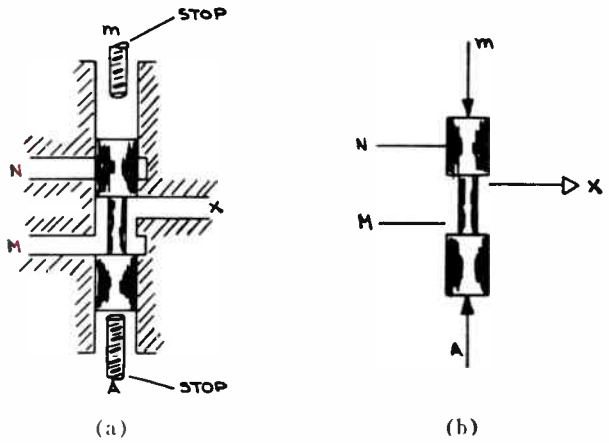


Fig. 7—Basic hydraulic logic element. (a) Schematic, (b) Symbolic.

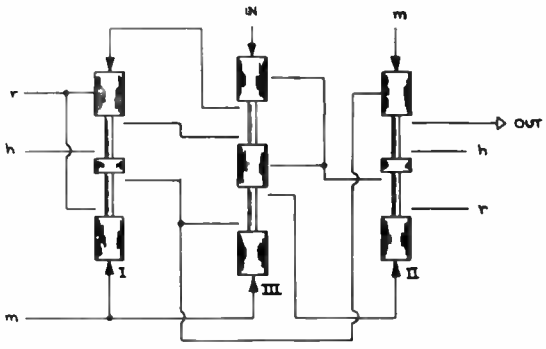
Hydraulic logic presents many serious design problems. In many respects the elements behave like their electronic counterparts, and problems such as transient peaks when a current in an inductive circuit is suddenly stopped are encountered. In addition, many physical effects relating to fluid flow influence the design. Inertia is especially critical in determining response time, and channel (*i.e.*, conductor) lengths must be equal for two parallel-fed elements to operate synchronously.

Despite these problems, the IBM Zurich group has made an impressive start toward realization of practical control and decisioning equipment using hydraulic elements exclusively. They admit that a hydraulic computer is in the far distant future, but point to more immediate potential applications, such as process control and machine tool control. They feel that the high reliability and long life of hydraulic components make the technique especially attractive in such applications.

Other Developments

In addition to the major development efforts described above, several other interesting programs were observed in both computer applications and hardware techniques. In the former area, the work in problem-oriented computer languages is worthy of special mention.

Development of computer languages for simplifying programming is centered around ALGOL (Algorithmic Programming Language). The idea for ALGOL originated in Germany several years ago and is being developed by a cooperative group representing West German and Swiss technical institutes. A preliminary



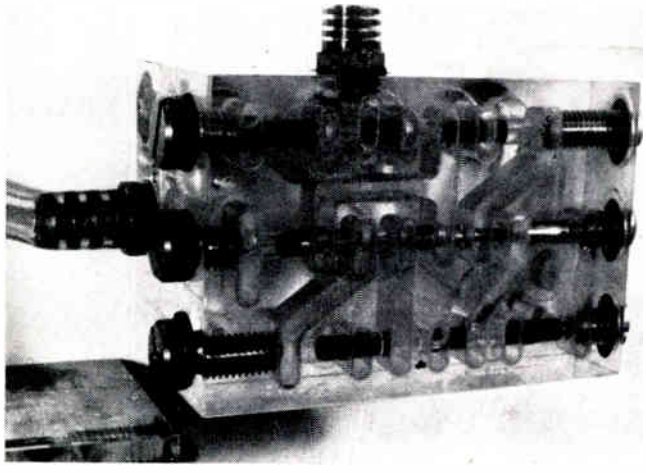


Fig. 8—Hydraulic scale-of-two counter.

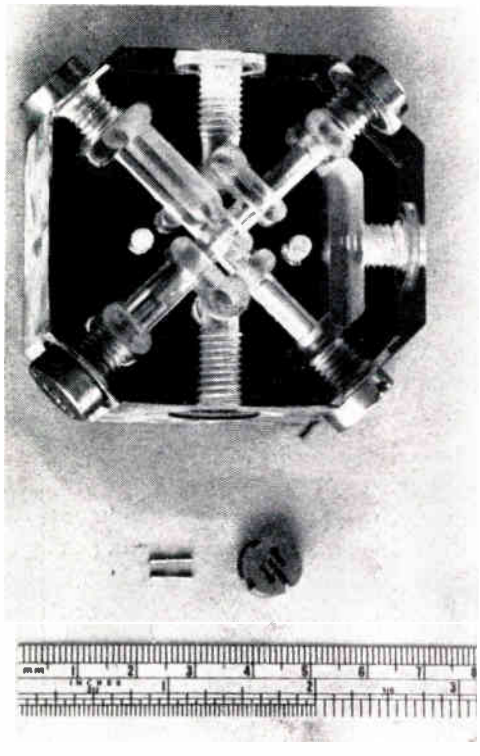


Fig. 9—Hydraulic multivibrators, 1-mm and 5-mm bores.

ALGOL language proposal was approved by GAMM, a German technical society, in 1957. ALGOL conferences in 1958 and 1960 saw the formation of a unified effort to establish a universal computer language. Currently, most computer groups in Europe are working on or have completed ALGOL-60 translators for their computers. Universities are teaching the language and are reporting very good results.

Elliott Brothers have observed an interesting phenomenon that can be used for nondestructive storage with nickel delay lines. A bit of information is stored in a nickel wire by discharging a capacitor through the wire at a fixed point. Bits may be placed every $\frac{1}{2}$ to 1 centimeter along the wire, equivalent to approximately one-microsecond intervals. The discharge applies a permanently stored circular magnetization to the wire. Passing a current pulse through the wire sets up an acoustic wave from each bit stored, so that an acoustic coil transducer mounted on the wire past the current output will receive a sequence of acoustic signals corresponding to the stored discharges in the wire.

III. Computers in Europe

The chart on pages 340–347 presents a comprehensive summary of Western European computers. Included are all current or recent computing systems on which information is available. The chart is mainly devoted to commercially available machines, but a few of the more important one-of-a-kind computers, as well as some systems still in development, are included for reference. The data in the chart were compiled from manufacturers' literature and, in most cases, through direct communication with the manufacturers.

The indexes on which the evaluation of computing systems is based were chosen in the belief that they achieve the most meaningful presentation of information. To clarify the indexes and define the terms used, Table I, on page 339, explains the column headings.

To provide a frame of reference for the computer comparison, the following paragraphs present brief notes on each company and computer represented in the chart.

Great Britain

Computer activity in Great Britain is second only to that in the United States. Several large manufacturers are active in commercial development and production, and British universities continue to play an important role in advanced computer development.

Leo Computers Ltd: Leo Computers Ltd. is a wholly owned subsidiary of J. Lyons and Company Ltd. of London, a pioneer in the application of computers in business. Leo Computers' first effort was LEO I, the oldest computer in the world still in operation. LEO II was introduced in 1957 and was followed by LEO III, an-

nounced in the summer of 1960. This transistorized parallel computer has three distinctive features: basic actions are controlled by microprograms; the computer can be microcoded to operate as a multiradix computer; and two or more different programs can be operated simultaneously under control of a master program.

Ferranti Ltd.: Ferranti Ltd. was one of the earliest companies in Great Britain to enter the computer field, beginning with the MARK I development in collaboration with the University of Manchester in 1951. Since then Ferranti has produced a large family of electronic digital computers, and the company is today at the forefront of technological developments and scientific computation in England.

The ATLAS computer, jointly developed with the University of Manchester, is the most advanced computer being developed in Europe. It features an extremely sophisticated organization and several unusual hardware techniques, including the fixed rod memory described earlier. Ferranti is also building advanced process control computers.

Elliott Brothers: Elliott Brothers, a division of Elliott Automation, entered the general-purpose computer field in the early 1950's, producing several serial scientific machines. The first business data processing machine made by Elliott was the 405 computer, using tube/diode logic, a magnetic tape memory and a 16,000-word magnetic disk memory.

In 1958 Elliott introduced the partly transistorized 802 computer, followed almost immediately by the completely transistorized 803, which is being promoted as a small-scale scientific computer, a small-scale business data processor, or as the computer unit of an on-line industrial data processing system. Elliott recently announced the 503, a large high-speed scientific computer.

EMI Electronics Ltd.: EMI Electronics Ltd., known for its work in analog control systems, entered the general-purpose electronic digital computer field with the EMIDEC 1100, a transistor/magnetic core computer. The 1100 is a two-address binary parallel machine with magnetic core and drum storage.

In 1955 the National Research Development Corporation contracted with EMI Electronics Ltd. to design and develop an advanced data processing system. This system, the EMIDEC 2400, is a very large high-speed data processor comparable to the IBM 7080, with a sophisticated organization of on-line and off-line peripheral equipment. Special features of the 2400 include automatic interunit switching of peripheral units, with an interrupt facility to permit breaking into the normal computing routine for peripheral unit control; elaborate error-checking and time-sharing of computing and input-output functions.

International Computers and Tabulators Ltd. (ICT): ICT was formed in 1959 from the British Tabulating Machine Company, Ltd. (Hollerith) and Powers-Samas Accounting Machines Ltd. Later in 1959, ICT and the General Electric Company Ltd. formed Computer Developments Ltd. as a jointly owned design and coordinating group. The 1301 computer, the first outgrowth of this united effort, is a file processor for medium-size companies. A fully transistor 1 Mc binary-coded-decimal serial-parallel machine, the 1301 has a magnetic core and drum memory.

Standard Telephones and Cables Ltd. (STC): STC's entry into electronic data processing came in 1958, when the first STANTEC ZEBRA was produced, using a logical design developed by the Netherlands Postal and Communications Services. The ZEBRA's unique features include the use of large etched circuit boards for interconnections between the vacuum-tube plug-in modules, extensive use of microprogramming, and the use of all "short" storage registers as instruction modifiers. In addition to the normal machine code, a "simple code" has been designed especially for the unskilled user.

STC is producing the STANTEC COMPUTING SYSTEM, the heart of which is a transistorized and improved version of the STANTEC ZEBRA. In the STANTEC COMPUTING SYSTEM, the magnetic drum is supplemented with ferrite core fast-access storage. Among the peripheral equipment available with the system is the Standard Elektrik Lorenz K-10 Magnetic Tape Unit, described earlier.

English Electric Company Ltd.: In 1947 the National Physical Laboratory at Teddington, England, formed an Electronics Section to undertake the design and construction of an electronic digital computer, designated ACE. In 1952 English Electric Company was given the task of designing an engineered model of the ACE design, with expanded capability. The result was DEUCE (Digital Electronic Universal Computing Engine), a vacuum-tube serial machine with mercury delay storage and magnetic drum back-up storage.

English Electric Company currently has an agreement with RCA to produce a transistorized medium-size data processing system patterned after the RCA 501. The English version, designated the KDP10, is physically and functionally similar to the RCA system and is not included in the chart.

France

Computer activity in France is proceeding at a moderate level, concentrated primarily in a few large, active firms. There is considerable potential for France to continue to be the leading producer of data processing equipment on the Continent, but it is clear that in the future there will be much more serious competition from other countries.

Compagnie des Machines BULL: BULL is the largest data processing manufacturing organization in Europe and ranks among the top four companies in the world. Its most important data processing equipments are the GAMMA 3 and GAMMA 60 computers. The former is a small-scale computer introduced in 1952. When fully equipped, the GAMMA 3 is similar in size to the IBM 650.

The GAMMA 60, BULL's entry into the large-scale solid-state data processing system market, is an advanced machine featuring simultaneous independent processing of several unrelated problems. Its internal structure is based on the concept of autonomous operation of individual elements under control of a central unit which dispatches data and instructions to the elements and serves as a buffer storage for transferred data.

Société D'Electronique et D'Automatisme (SEA): Primarily involved in the design and manufacture of analog computers for the military, SEA expanded into flight simulators and machine tool control. During the past four years the company has produced a series of digital computers for military, scientific and business applications. The computers are used almost entirely within France.

The CAB 500 is a small serial digital scientific computer using magnetic logic elements and transistors, with magnetic drum storage. The SEA 3000 system is a medium-scale data processor designed for scientific and commercial applications. The heart of the system is the SEA 3030 computer, a vacuum-tube, binary computer with ferrite core and drum memory. Successor to the 3000 is the SEA 3900, a fully transistor serial-parallel 2 Mc data processor also intended for general commercial applications. A modified version is available for scientific calculations.

Société Nouvelle D'Electronique (SNE): SNE's parallel binary computer, the KL901, is designed for scientific, statistical, and accounting applications. The vacuum-tube machine uses magnetic-tape and ferrite-core memories. The tape units have 36 tracks, allowing an entire word to be read in parallel.

Italy

The most active computer development work currently being done in Italy is at the University of Pisa and the Olivetti Laboratories near Milan. These two groups are working on both new computers and application problems.

University of Pisa (Centro di Studi sulle Calcolatrici Elettroniche): The University of Pisa's Computer Center is engaged in logical design, computer programming, numerical analysis, and electronic design and construction. The computer development work is among the most advanced observed in Europe. The University's computer, CEP (Calcolatrice Elettronica Pisa), is a 36-bit parallel binary computer with magnetic core and drum memory. The CEP has several interesting and advanced features, including fixed high-speed rod memory for storing microprograms, identical in concept to the fixed memory being built at the University of Manchester (described earlier); and an order structure embodying double address modifiers.

Olivetti: Olivetti is the only major commercial Italian manufacturing company extensively working on data processing equipment. The Olivetti computer product line includes two electronic systems: the ELEA 9003 and the ELEA 6001. The computers are both transistor machines with variable word length. The 9003 is a large system for business applications, while the 6001 is a scientific computer. Both computers operate on a decimal character-by-character basis with memory access time of ten microseconds per character and use threaded-core type microprogramming.

West Germany

The computer industry in Western Germany is quite active on many fronts, despite the country's relatively late start in the field. In the early 1950's the only significant work on computers was being done at the universities and research institutes; not until the past few years did the commercial companies become involved.

Siemens & Halske AG: The SIEMENS 2002 is a transistorized decimal machine, with magnetic-core and drum storage. Input-output equipment includes paper tape, punched card, magnetic tape printer and cathode-ray tube. The machine is designed for both scientific and commercial applications and sales have split evenly between these two uses.

Telefunken: Telefunken specializes in communications, radar, computers and other electronic fields. The Telefunken TR-4, a large-scale transistorized high-speed computer designed for both business and scientific applications, is the fastest computer being built in Germany. It uses two novel fixed memories: a wired ferrite core array, described earlier, and a memory used for microprogramming, consisting of double-sided printed-circuit cards, with diodes inserted wherever connections are desired.

Standard Elektrik Lorenz AG: Standard Elektrik Lorenz is an affiliate of the International Telephone and Telegraph Company. The company's data processing activities include the development of special-purpose systems from elements manufactured by various members of the ITT family. Standard Elektrik Lorenz has developed a transistor general-purpose computer, the ER-56, which uses the K-10 tape unit, described earlier. The ER-56 contains a switching network which can connect the various units in any arrangement desired.

Zuse K.-G.: Zuse started developing computers in 1947 and produced the Z 4, a relay computer, in 1950. An-

TABLE 1

DEFINITION OF EUROPEAN COMPUTER CHART TERMINOLOGY

Term	Definition
Manufacturer and Country	This is the actual manufacturing concern. In some cases the agency responsible for the design or sales of the machine, may be shown in parentheses. Intra-company divisions are shown where appropriate. The country is where the computer is actually built.
Computer Name	This is the name the computer is usually called. For numbered computers, the manufacturer's abbreviation is usually shown along with the number.
Availability—Number on Order	This is the total number of machines for which firm orders have been received, but which have not been installed. The figure is current as of September, 1960.
Availability—Number Installed	This, is the number of completed machines actually installed and operating as of September, 1960.
Availability—Date of First Installation	This is the actual (or anticipated) date of first installation.
Technique—Circuits	Transistor, transistor-diode, transistor-core, vacuum tube.
Word Length	The number of bits (including sign) or digits used in a normal add operation. Parity bits are not included in the count. In variable word length machines, this is the number of digits or characters retrieved from memory on each cycle.
Addresses per Instruction/Instructions per Word	The numerator is the number of full addresses in the instruction used to specify operands. In those machines where an address is included in each instruction to specify the location of the next instruction, the form $x+1$ is used for an x address machine.
Number of Operations: Decoded/Possible	The numerator is the number of operation codes with assigned functions. The denominator is the number of combinations possible of the bits (or digits) used to specify the operation code.
Operation Times	All operation times are in microseconds. The times include memory access for the instruction and the operands. "Subroutine" indicates that a single instruction cannot perform the operation.
Storage—Cycle Time	The minimum time between two consecutive accesses to the same storage unit. This involves the read and restore cycle on core memories.
Storage—Access-Time	The average time to retrieve one word. This is the read cycle only on core memories, and half the time of a drum revolution on drum memories.
Storage—Data Unit Accessed	This is the amount of information transferred out on one call to the memory. This is usually a word, but sometimes it is a character (variable word length machines) on a block of many words (back up drum and memories).
On-Line Input-Output—Speed	The speed of various units is rated as follows: Punch card equipment: Cards per minute. Paper tape equipment: Frames per second. Line printers: Lines per minute. Other units: Characters per second.
On-Line Input-Output—Number of Units	This is the maximum number of units which may be attached to a production model computer without modifying the equipment.
Magnetic Tape—Characters per Second	Alphanumeric character or six-bit groups transferred per second. This is the maximum transfer rate within a block.
Magnetic Tape—Bits per Inch/Inches per Second	Bits per inch on each track.
Magnetic Tape—Number of Units Operating/Total Tape Units	The numerator refers to the number of tape drives which may be reading (or writing) data into the central computer simultaneously. Rewinding, searching or other independent operations are not considered.
Special Features	Any important facts about the computer which are not shown elsewhere on the chart.

EUROPEAN

No.	Manufacturer and Country	Computer Name	Availability			Technique		General Machine Features							Operation Times (Micro-Seconds) (Including Memory Accesses)			
			Number		Date of First Installation	Circuits	Clock Rate	Word Length	Addresses per Instruction / Instructions per Word	Number of Operations Decoded / Possible	Number of Index Registers	Indirect Addressing	Partial and Multiple Word Operations	Internal Checking	Addition (Fixed / Floating)	Multiply (Fixed / Floating)	Control Transfer (Min. / Max.)	Shift Operations (1 Place / Average)
			On Order	Installed														
1	Leo Computers Ltd. Great Britain	LEO III	3	0	1961	Transistor Diode	INA	42 Bits	1 / 2	110 / 140	Up to 12	No	Half Word Operations	Parity	44 / 200–450	300–700 / 600–900	30 / 49	56 / 88
2	Ferranti Ltd. Great Britain	PEGASUS	10	28	1956	Vacuum Tube	333 kc	39 Bits	1 / 2	62 / 64	7	No	Double Word	Parity	300 / Subroutine	1900 / Subroutine	300 / 300	425 / 2750
3	Ferranti Ltd. Great Britain	MERCURY	3	19	1957	Vacuum Tube	1000 kc	10-20-40 Bits	1 / 2	70 / 128	7	No	Double Word	Parity	60 / 180	Subroutine / 300	60 / 60	60 / 300
4	Ferranti Ltd. Great Britain	PERSEUS	0	2	1958	Vacuum Tube	333 kc	72 Bits	1 / 3	63 / 64	7	No	Both	Parity and Complete Arithmetic Check	234 / Subroutine	780 / Subroutine	234 / 3744	234 / 4680
5	Ferranti Ltd. Great Britain	SIRIUS	2	1	1959	Transistor Core	500 kc	10 Decimal Digits	1 / 1	60 / 100	9	No	No	Parity	240 / Subroutine	4000–16,000 / Subroutine	240 / 4000	240 / 1200
6	Ferranti Ltd. Great Britain	ARGUS	0	1	1960	Transistor Diode	500 kc	12 Bits	1 / 1	54 / 64	7	No	Double Word	Parity	20 / Subroutine	100 / Subroutine	20 / 20	20 / 20
7	Ferranti Ltd. Great Britain	ORION	9	0	1961	Transistor Core	500 kc	48 Bits	3 / 1	114 / 128	64	Yes	Both	Parity	36–68 / 60–80	64–184 / 140–160	36 / 68	4 / 48
8	Ferranti Ltd. Great Britain	APOLLO	1	0	1961	Transistor Diode	500 kc	24 Bits	1 / 1	80 / 128	3	No	No	Parity	6 / Subroutine	60 / Subroutine	6 / 12	8 / 30
9	Ferranti Ltd. and Manchester University Great Britain	MUSE (ATLAS)	1	0	1961	Transistor Diode	INA	48 Bits	1 / 1	400 Anticipated / 1024	125	No	Both	Parity	1.1 / 1.1	4 / 4	1 / 2	1 / 12
10	Elliott Brothers Great Britain	803	18	5	1959	Transistor	166.5 kc	39 Bits	1 / 2	60 / 64	4096	No	No	Parity	720 / 720	29,500 / 9360	720 / 720	1440 / 15,480
11	Elliott Brothers Great Britain	503	0	0	1962	Transistor	INA	39 Bits	1 / 2	INA / 64	4096	No	INA	Parity	8 / 8–15	18–28 / 15–25	4	INA

INA—Information not available
* *Maximum internal memory addressing capacity is 1,048,576 words.*

COMPUTERS

Storage						On-Line Input-Output				Magnetic Tape				Special Features	Computer Name
Type of Storage	Number of Words: Minimum System	Number of Words: Maximum System	Number of Words: Module Size	Word Time μsec.	Access Time μsec.	Data Unit Accessed	Type of Unit	Manufacturer	Speed	Number of Units	Manufacturer	Char. per Second	Bits/Inch / Inches/Sec.	Number Operating / Total Tape Units		
Core	1024	32,768	4096	INA	7	Word or Half Word	Tape Reader	Elliott	1000 FPS	32	Ampex (1")	90,000	300 / 150	3 / 24	The computer will generate output layout automatically. A single instruction will follow a table of addressee and editing controls to a perfect output line.	LEO III
							Tape Punch	Teletype	110 FPS	48						
							Card Reader	ICT	600 CPM	16						
							Card Punch	IBM/ CT	250/100 CPM	32						
							Printer	Analex	850 LPM	16	Ampex (½")	45,000	300 / 150	4 / 32		
								ICT	600 LPM							
								IBM	150 LPM							
Nickel Delay Line	55	55	—	126	0	Word	Tape Reader	Ferranti	300 FPS	2	Burroughs or Decca	9,250	123 / 75	2 / 10	7 Accumulators	PEGASUS
							Tape Punch	Teletype	60 FPS	1						
Drum	7168	7168	—	126	8000	Word or 8 Words	Card Reader	Power Samas	200 CPM	1						
							Card Punch	Power Samas	100 CPM	1						
Core	1024	1024	—	10	2	Word	Tape Reader	Ferranti	300 FPS	2	Burroughs	15,000	266 / 60	2 / 8	Division by subroutine only.	MERCURY
Drum	8192	16,384	4096	20	10,000	32 Words	Tape Punch	Creed	33 FPS	1						
							7 Others Optional									
Nickel Delay Line	1024	1024	—	234	234	Word	Tape Reader	Ferranti	200 FPS	2	Burroughs	9,250	123 / 75	4 / 16	Variable radix arithmetic operations	PERSEUS
							Card Reader	Power Samas	300 CPM	1						
							Teleprinter	Creed	10 CPS	1						
Nickel Delay Line	1000	10,000	1000	80	4000	Word	Tape Reader	Ferranti	300 FPS	10	Magnetic Tape Available				—	SIRIUS
							Tape Punch	Teletype	60 FPS	10						
Core	1024	3072	1024	20	2	Word	Custom Specified (Includes Analog-Digital Converters)				Custom Specified				Process control machine with peg board instructions	ARGUS
Drum	0	50,000	50,000	4	12,000	Track										
Core	4096	16,384	4096	12	6	Word	Card Read	ICT	600 CPM	No Limit	Ampex FR 300	90,000	375 / 120	4 / 16	—	ORION
							Card Punch	ICT	100 CPM							
							Printer	ICT	600 LPM							
								BULL	150 LPM							
								Rank	3000 LPM							
Drum	16,384	16,777,216	16,384	200	12,000	Variable	Tape Punch	Creed	300 FPS							
							Tape Reader	Ferranti	1000 FPS							
Core	8000	32,000	4000	6	2	Word	Custom Specified (Includes Analog-Digital Converters)				Custom Specified				Primarily for air traffic control	APOLLO
Core	8192	262,144[a]	4096	2	0.5	Word	Custom Specified			256 Total	Ampex	90,000	375 / 120	8 / 32	Automatic drum-core data transfers. Fixed ferrite slug memory for control operations	MUSE (ATLAS)
Drum	0	1,048,576[a]	24,576	4	6000	512 Wrds										
Core	4096	8192	4096	INA	INA	Word	Tape Reader	Elliott	140 FPS	1	No Magnetic Tape				Serial Computer	803
							Tape Punch	Creed	25 FPS	1						
							Card Reader	Elliott	300 CPM	1						
							Card Punch	IBM	100 CPM	1						
							35 mm mag. Film	Elliott	1.44 msec per Word	1						
							Analog-Digital Converters									
Core	4096	8192	4096	4	INA	Word	Tape Reader	Elliott	1000 FPS	Multiple	Potter	45,000	INA	INA	Programs compatible with 803	503
							Tape Punch	Teletype	100 FPS	Multiple						
							Card Reader	Elliott	400 CPM	Multiple						
							Card Punch	IBM	100 CPM	Multiple						
							Printer	INA	900 LPM	Multiple						

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EUROPEAN

No.	Manufacturer and Country	Computer Name	Availability: Number On Order	Availability: Number Installed	Availability: Date of First Installation	Technique: Circuits	Technique: Clock Rate	General Machine Features: Word Length	Addresses per Instruction / Instructions per Word	Number of Operations Decoded / Possible	Number of Index Registers	Indirect Addressing	Partial and Multiple Word Operations	Internal Checking	Operation Times (Micro-Seconds) (Including Memory Accesses): Addition (Fixed / Floating)	Multiply (Fixed / Floating)	Control Transfer (Min. / Max.)	Shift Operations (1 Place / Average)
12	EMI Electronics Ltd. Great Britain	EMIDEC 1100	15	4	1960	Transistor	100 kc	36 Bits	2 / 1	30 / 32	7	No	Double Word Addition	None	140 / Subroutine	1260 / Subroutine	125 / 225	170 / 340
13	EMI Electronics Ltd. Great Britain	EMIDEC 2400	3	0	1961	Transistor Diode	1000 kc	36 Bits	2 / 1	57 / 64	64	No	Multiword Transfers	Parity	32 / Subroutine	130 / Subroutine	16 / 30	32 / 60
14	ICT Great Britain	ICT 1200 ICT 1201 ICT 1202	21	57	1955	Vacuum Tube	40 kc	40 Bits	1+1 / 1	38 / 64	0	No	Both	No	2500 / Subroutine	20,000 / Subroutine	1250 / 20,000	2500 / 2500
15	Computer Development Ltd. (ICT & GEC) Great Britain	ICT 1301	25	0	1961	Transistor Diode	1000 kc	12 Decimal or Sterling Digits Incl. Sign	1 / 2	51 / 100	0	No	No	2 Parity Bits per Word Check Sum on Drum	27 / Subroutine	2040 / Subroutine	12 / 12	23 / 23
16	Standard Telephones and Cables Great Britain	STAN-TEC ZEBRA	6	32	1957	Vacuum Tube	100 kc	33 Bits	1 / 1	Micro Programmed / 2^{15}	12	No	Multiple Word Operations	Parity	312 / Subroutine	11,000 / Subroutine	INA	INA
17	Standard Telephones and Cables Great Britain	STAN-TEC SYSTEM	10	0	1960	Transistor	128 kc	33 Bits	1 / 1	Micro Programmed / 2^{15}	12	No	Multiple Word Operations	Parity	312 / Subroutine	624 / Subroutine	INA	INA
18	English Electric Great Britain	DEUCE	2	30	1955	Vacuum Tube	1000 kc	32 Bits	2+1 / 1	Not Defined	0	No	Many Double Word Operations	No	64 / Subroutine	2080 / Subroutine	64 / 96	64 / 544
19	English Electric Great Britain	KDF-9	INA	0	1962	Transistor Core Diode	2000 kc	48 Bits	0 or 1 / 2 to 6	292 / INA	16	Yes	Double Word	INA	1 / 7 From Special Working Store	14 / 14	INA	2.5 / 5
20	Compagnie des Machines BULL France	GAMMA 3 ET	25	88	1956	Vacuum Tube-Diode	280 kc	12 Digits (Binary Commands)	1 / 3	INA	0	No	Variable Word Length Up To 12 Digits	INA	850 / Subroutine	11,000 / Subroutine	INA	INA

INA—Information not available
[a] *Maximum internal memory addressing capacity is 1,048,576 words.*

COMPUTERS (*Cont'd*)

Storage							On-Line Input-Output				Magnetic Tape				Special Features	Computer Name
Type of Storage	Number of Words: Minimum System	Number of Words: Maximum System	Number of Words: Module Size	Word Time μsec.	Access Time μsec.	Data Unit Accessed	Type of Unit	Manufacturer	Speed	Number of Units	Manufacturer	Char. per Second	Bits/Inch / Inches/Sec.	Number Operating / Total Tape Units		
Core	1024	4096	—	20	10	Word	Tape Reader	Ferranti	300 FPS	16 Total	Ampex FR 300	20,000	167 / 120	6 / 16	Automatic decimal-binary conversions	EMIDEC 1100
							Tape Punch	Creed	30/300 FPS							
							Card Reader	Elliott	400 CPM							
							Card Punch	ICT	100 CPM							
							Printer	ICT	300 LPM							
Drum	16,384	65,536	16,384	INA	15,000	4 Words										
Core	4096	32,768	4096	10	5	Word	Tape Reader	Elliott	1000 FPS	Multiple	EMI	60,000	300 / 200	5 / 30	Flexible switching of peripheral equipment to on-line or off-line use. Program interrupt.	EMIDEC 2400
							Tape Punch	Creed	300 FPS	Multiple						
							Card Reader	Elliott	400 CPM	Multiple						
Diode-capacitor	64	64	—	4.5	1.5	Word	Card Punch	ICT	100 CPM	Multiple						
							Printer	ICT / Rank	300 LPM / 3000 LPM	6						
Drum	4096	8192	4096	1250	10,000	Word	Card Reader	ICT	100 CPM	1	No Magnetic Tape				Direct transfer from card reader to printer and punch. The same card can be punched in both decimal and binary	ICT 1200 ICT 1201 ICT 1202
							Card Punch	ICT	100 CPM	1						
							Printer	ICT	100 LPM	1						
Core	400	2000	400	12	4	Word	Card Reader	ICT	600 CPM	1	Ampex FR 300	90,000	300 / 150	2 / 8	Automatic error correction on tapes	ICT 1301
							Card Punch	ICT	100 CPM	1						
Drum	12,000	96,000	12,000	52	286	200 Words	Printer	ICT	600 LPM	1	Ampex FR 400	22,500	300 / 75			
Drum	8192	8192	—	312	5000	Word	Tape Reader	Ferranti	200 FPS	1–2	No Magnetic Tape				Microprogrammed computer	STAN-TEC ZEBRA
							Tape Punch	Teletype	50 FPS	1–2						
							Teleprinter	Creed	7 CPS	1–2						
Core	512	8192	512	INA	INA	Word	Tape Reader	Elliott	800 FPS	1–6	ITT K2S	20,000	200 / 100	1 / 64	Up to 8 blocks of core buffer storage with 32 words each are available.	STAN-TEC SYSTEM
							Tape Punch	Teletype	50 FPS	1–6						
								Creed	300 FPS							
							Card Punch	ICT	150 CPM	1						
Drum	8192	8192	—	INA	5000	Word	Card Reader	Elliott	340 CPM	1	Ampex	INA	INA	1 / 64		
							Printer	Rank	3000 LPM	Off Line						
							Teleprinter	Creed	10 CPS	1–2						
Mercury Delay Line	402	626	—	32	.496	Word or Multi-Word	Tape Reader	INA	850 FPS	1 (Optional)	Decca	8000	80 / 100	1 / 8	Serial binary computer	DEUCE
							Tape Punch	INA	30 FPS	1 (Optional)						
Drum	8192	8192	—	INA	15	32 Words	Card Reader	ICT	200 CPM	2						
							Card Punch	ICT	100 CPM	2						
Core	4096	32,768	4096	Main Storage 6 μs Special Wkg Store .5 μs Read 1 μs Write	Main Storage 3 μs Special Wkg Store .5 μs	Word	Printer	Rank	3000 LPM	As Required	English Electric	33,333	333 / 100	8 to 16 / 64	Use of special working storages. Concurrent operation up to 4 programs running on time sharing basis. Time smoothing advance control.	KDF-9
							Tape Reader	INA	1000 FPS							
							Tape Punch	INA	110/300 FPS							
							Card Reader	English Electric	400 CPM							
							Card Punch	English Electric	150 CPM							
							Printer	English Electric	600/900 LPM							
Electro-magnetic Delay Line	71	135	16	172	500	1 Digit	Card Reader	BULL	150 or 300 CPM	1–2	Burroughs	21,500 Digits	200 / 67	1 / 8	—	GAMMA 3 ET
							Card Punch	BULL	150 or 300 CPM	1–2						
Drum	4096	16,384	4096	172	10,000	16 Words	Printer	BULL	150 or 300 LPM	1–2						

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EUROPEAN

No.	Manufacturer and Country	Computer Name	Availability: Number On Order	Availability: Number Installed	Availability: Date of First Installation	Technique: Circuits	Technique: Clock Rate	General Machine Features: Word Length	General Machine Features: Addresses per Instruction / Instructions per Word	General Machine Features: Number of Operations Decoded / Possible	General Machine Features: Number of Index Registers	General Machine Features: Indirect Addressing	General Machine Features: Partial and Multiple Word Operations	General Machine Features: Internal Checking	Operation Times (Micro-Seconds) (Including Memory Accesses): Addition (Fixed / Floating)	Operation Times: Multiply (Fixed / Floating)	Operation Times: Control Transfer (Min. / Max.)	Operation Times: Shift Operations (1 Place / Average)
21	Compagnie des Machines BULL France	GAMMA 60	13	3	1960	Transistor Diode	2700 kc	6 Digits or 24 Bits	1-3 / Undefined	INA	0	Yes	No	Modulo 7 Check On All Operations	100 / INA	250 / INA	INA	INA
22	SEA France	CAB 3030	INA	3	1958	Vacuum Tube Diode	100 kc	30 Bits	2 / 1	31 / 31	1	No	Double Word	Parity	320 / 9600	640 / 5120	INA	320 / 5120
23	Le Matériel Electrique S-W (SEA) France	CAB 500	20	2	1960	Magnetic Switching (Symmag)	220 kc	32 Bits	2 / 1	46 / 64	1	No	Double Word	Parity	308 / Subroutine	Subroutine / Subroutine	INA	308 / 308
24	SEA France	SEA 3900	20	2	INA	Transistor Diode	2000 kc	Variable (2 Characters Per Memory Access)	3 / Undefined	43 / 128	3 (One For Each Address)	No	Data Controlled Word Length	Parity	216 / Subroutine [5 Digit Factors]	5590 / Subroutine	48	Undefined
25	SEA France	CAB 5000	INA	INA	INA	Transistor Diode	2000 kc	42 Bits	2 / 1	31 / INA	3	No	Double Word	2 Parity Bits Per Word	24 / 48	48 / 48	24 / 24	48 / 48
26	SNE France	KL 901	INA	1	1960	Transistor and Vacuum Tube Diode	200 kc	29 Bits	2 / 1	56 / 64	2	Yes	No	Parity	10 / 20	No Operation / 80	10 / 10	10 / 10
27	University of Pisa Italy	C.E.P.	1	0	1960	Vacuum Tube Germanium Diodes and Transistor	Asynchronous	36 Bits	1 / 1	512 / 512	64	No	Double Word	No	15 / 100	135 / 135	10 / 24	10 / 52
28	Olivetti Italy	ELEA 6001	4	INA	1960	Transistor Diode Core	250 kc	Variable Number of Digits	1-3 / Undefined	116 / 256	16	Yes	Data Controlled Word Length	Parity Bit On Each Digit	364 / 2198 [10 Digit Factors]	3804 / 3426	60	Undefined
29	Olivetti Italy	ELEA 9003	6	1	1960	Transistor Diode	100 kc	Variable Number of Characters	1 / Undefined	91 / 256	40	No	Variable Word Length Controlled By Either Instructions Or Data	Parity Bit On Each Character Modulo 3 Check on Arithmetic	200 / Subroutine	1400 / Subroutine	100	Undefined
30	Siemens Halske A G Germany	SIEMENS 2002	22	8	1958	Transistor Diode	200 kc	12 Decimal Digits and Sign	1 / 1	86 / 1000	3	Yes	INA	Illegal Digit Combinations	90 / 450	1260 / 1350	90 / 90	INA
31	Telefunken Germany	TR-4	4	0	1961	Transistor Diode	2000 kc	48 Bits	1 / 2	208 / 256	256	Yes	Half and Double Word Operations	Modulo 3 Check On All Operations	8.5 / 15	30 / 30	7.5	10.5 / 12

INA—Information not available
[a] *Maximum internal memory addressing capacity is 1,048,576 words.*

COMPUTERS (*Cont'd*)

Storage							On-Line Input-Output				Magnetic Tape				Special Features	Computer Name
Type of Storage	Number of Words: Minimum System	Number of Words: Maximum System	Number of Words: Module Size	Word Time μsec.	Access Time μsec.	Data Unit Accessed	Type of Unit	Manufacturer	Speed	Number of Units	Manufacturer	Char. per Second	Bits/Inch / Inches/Sec.	Number Operating / Total Tape Units		
Core	8192	32,768	4096	10	10	Word	Card Reader	BULL	300 CPM	INA	Burroughs	21,500 Digits	200 / 67	10 / 48	—	GAMMA 60
							Card Punch	BULL	300 CPM	INA						
							Printer	BULL	300 LPM	INA						
Drum	25,600	No Limit	25,600	100	10,000	Word	Tape Reader	BULL	300 FPS	INA						
							Tape Punch	BULL	25 FPS	INA						
Core	1024	16,384	1024	320	6	Word	Tape Reader	Ferranti	200 or 400 FPS	2	Potter	8000	140 / 60	1 / 10	—	CAB 3030
							Tape Punch	SEA	45 FPS	2						
Drum	16,384	16,384	—	320	20,000	32 or 128 Words	Printer	Shepard	900 LPM	1						
							Microfilm Printer	SEA	2000 Char/sec	1						
Drum	16,384	16,384	16,384	160	10	Word	Tape Reader	SEA	80 FPS	1 (Optional)	Magnetic Tape Available				—	CAB 500
							Tape Punch	SEA	45 FPS	1 (Optional)						
Shift Register	16	16	16	2.5	2.5	Word	Typewriter	Friden	10 CPS	1						
Core	2048 Characters	4096 Characters	—	INA	6	Char.	Printer	Shepard	900 LPM	No Limit	C.d.C. (French Licensee of Potter)	9000	300 / 60	2 / No Limit	Double recording on magnetic tape	SEA 3900
							Card Reader	Elliott	400 CPM	No Limit						
Drum	40,960 Characters	81,920 Characters	—	INA	15,000	160 Char.	Tape Reader	SEA	450 FPS	No Limit						
							Tape Punch	SEA	45 FPS	No Limit						
Core	4096	32,768	4096	24	6	Word	Tape Reader	SEA	400 FPS	2	C.d.C. (French Licensee of Potter)	9000	300 / 60	2 / 64	Square root operation	CAB 5000
							Tape Punch	SEA	50 FPS	2						
Drum	16,384	131,072	16,384	160	10,000	128 Words	Printer	Shepard	900 LPM	1						
Core	1024	8192 (Total Including Fixed Memory)	1024	10	5	Word	Tape Reader	SNE	1000 FPS	1	SNE	50,000 (10,000 Words)	200 / 50	2 / 8	Square root operation	KL 901
							Tape Punch	Creed	33 FPS	1						
Core	4096	32,768	INA	7	3.5	Word	Tape Reader	Ferranti	300 FPS	2	Ampex	20,000	270 / 75	1 / 8	Fixed ferrite slug memory (256×256 bits) for control. Two index register addresses per instruction. Extra codes.	C.E.P.
Drum	16,384	INA	16,384	39	10,000	Variable	Tape Punch	Teletype	60 FPS	3						
							Printer	BULL	150 LPM	1						
Core	10,000	100,000	10,000	10	6	Digit	Tape Reader	Olivetti	800 FPS	1	Ampex	22,500	300 / 75	1 / 6	Wired in micro subroutines and expandable set of commands.	ELEA 6001
							Tape Punch	Olivetti	50 FPS	1						
							Card Reader	BULL	150 CPM	1						
							Printer	Olivetti	600 LPM	1						
Core	20,000	160,000	20,000	10	10	2 Char.	Tape Reader	Olivetti	800 FPS	10 Total	Ampex	45,000	300 / 150	2 / 20	Three simultaneous program sequences.	ELEA 9003
							Tape Punch	Olivetti	50 FPS							
Drum	0	360,000	120,000	11	10,000	Up to 1920 Char.	Card Reader	BULL	500 CPM							
							Card Punch	BULL	150 CPM							
							Printer	Olivetti	600 LPM							
Core	1000	100,000	—	14	5	Word	Tape Reader	Siemens	200 FPS	1-5	Siemens or Ampex	46,000	200 / 120	INA / 60	Real time input	SIEMENS 2002
							Tape Punch	Siemens	60 FPS	1-5						
							Card Reader	IBM	800 CPM	1-5						
Drum	10,000	2,000,000 Characters	10,000	INA	19,000	INA	Card Punch	IBM	250 CPM	1-5						
							Printer	IBM	1000 LPM	1-5						
								Analex	900 LPM							
Core	8192	28,672	4096	6	2	Word	Tape Reader	Elliott	1000 FPS	64 Total	Telefunken	37,500	375 / 100	8 / 64	Operations usually faster than noted due to overlapping memory accesses	TR-4
								FACIT	500 FPS							
							Tape Punch	FACIT	150 FPS							
Fixed Core	1024	4096	256	1	1	Word	Card Reader	IBM	800 CPM							
								BULL	300 CPM							
							Card Punch	IBM	250 CPM							
								BULL								

Cont'd next page

EUROPEAN

No.	Manufacturer and Country	Computer Name	Availability: Number On Order	Availability: Number Installed	Availability: Date of First Installation	Technique: Circuits	Technique: Clock Rate	General Machine Features: Word Length	Addresses per Instruction / Instructions per Word	Number of Operations Decoded / Possible	Number of Index Registers	Indirect Addressing	Partial and Multiple Word Operations	Internal Checking	Operation Times (Micro-Seconds) (Including Memory Accesses): Addition (Fixed / Floating)	Multiply (Fixed / Floating)	Control Transfer (Min. / Max.)	Shift Operations (1 Place / Average)
32	Standard Elektrik Lorenz Germany	ER-56	12	7	1959	Transistor Diode	100 kc	7 Decimal Digits	1 / 1	82 / 100	9	No	Double Word	2 Out of 5 Code	200 / 1000	500 / 1500	150 / 300	150 / 150
33	Standard Elektrik Lorenz Germany	SEL-B7	1	0	INA	Transistor Diode	100 kc	10 Characters	1 / 1	57 / 100	9	Yes	Partial Word Operations	Parity	90–180 / Subroutine	Subroutine / Subroutine	60 / 60	INA
34	Zuse K.-G. Germany	Z-22R	INA	30	1958	Vacuum Tube	140 kc	38 Bits	1 / 1	Micro Programmed / 2^{18}	21	Yes	Double Word	INA	600 / Subroutine	15,000 / Subroutine	300	INA
35	Zuse K.-G. Germany	Z-23	INA	0	1961	Transistor	150 kc	40 Bits	1 / 1	Micro Programmed / 2^{18}	240	Yes	Double Word	INA	300 / 10,000	13,000 / 20,000	300	INA
36	Zuse K.-G. Germany	Z-31	INA	0	INA	Transistor	53 kc	10 Decimal Digits and Sign	1 / 1	42 / INA	10	Yes	Double Word	2 Out of 5 Code	600 / Subroutine	20,000 / Subroutine	INA	INA
37	N. V. Electrologica Netherlands	X1	16	10	1959	Transistor Diode	500 kc	27 Bits	1 / 1	48 / 64	1	No	No	Parity	64 / Subroutine	500 / Subroutine	36 / 64	48 / 144
38	Philips Netherlands	PASCAL / STEVIN	2	0	1960	Vacuum Tube Transistor Diode	660 kc	42 Bits	1 / 2	57 / 64	8	INA	INA	Parity on Half Word Carry Comparison in Adder	10 / 10–60	70 / 55	4.5 / 7.5	11.5 / 42
39	Facit Sweden	EDB 2 / EDB 3	3	5	1957	Vacuum Tube and Transistor	180 kc	40 Bits	1 / 2	95 / 128	0	No	Half Word Operations	No	45 / Subroutine	290 / Subroutine	22 / INA	45 / 157
40	Regnecentralen Dansk Institut for matematik-Maskina Denmark	GIER	1	0	1961	Transistor Diode	500 kc	40 Bits Plus 2 For Word Indicator	1 / 1	37 / 64	12	Yes	No	No	50 / INA	170 / INA	INA	INA

INA—Information not available
[a] *Maximum internal memory addressing capacity is 1,048,576 words.*

COMPUTERS (*Cont'd*)

Storage							On-Line Input-Output				Magnetic Tape				Special Features	Computer Name
Type of Storage	Number of Words: Minimum System	Number of Words: Maximum System	Number of Words: Module Size	Word Time μsec.	Access Time μsec.	Data Unit Accessed	Type of Unit	Manufacturer	Speed	Number of Units	Manufacturer	Char. per Second	Bits/Inch / Inches/Sec.	Number Operating / Total Tape Units		
Core	200	9000	200/1000	30	5	Word	Tape Reader	Ferranti	400 FPS	23 Total	Ampex	52,500 (Digits)	250 / 150	4 / 16	Control unit simultaneously connects any core storage to any input, output or processing unit. Tape bin storage units.	ER-56
							Tape Punch	Lorenz	50 FPS							
								Creed	300 FPS							
Drum	6000	72,000	6000	INA	10,000	20–200 Words	Card Reader	Elliott	400 CPM		Standard Elektrik	35,000 (Digits)	250 / 100	4 / 16		
							Card Punch	IBM	100 CPM							
							Printer	Shepard	900 LPM							
Core	2000	10,000	2000	10	3	Word	Tape Reader	Lorenz	100 FPS	6	Standard Elektrik	25,000	250 / 100	24 / 48	Reservation system computer with real time input-output facilities and large back up memory using tape bins and drum with independent searching facilities	SEL-B7
								Ferranti	300 FPS							
Drum	9000	180,000	9000	INA	10,000	Word	Tape Punch	Lorenz	50 FPS	6						
							Printer	Shepard	900 LPM	2						
Drum	8192	8192	—	300	5000	Word	Tape Reader	Ferranti	200 FPS	1	No Magnetic Tape				—	Z-22 R
							Tape Punch	Creed	25 FPS	1 (Optional)						
							Typewriter	Siemens	10 CPS	1						
Core	240	8431	256	300	INA	Word	Tape Reader	Ferranti	300 FPS	1	INA				—	Z-23
							Tape Punch	Creed	50 FPS	1						
							Card Reader	INA	300 CPM	INA						
Drum	8192	8192	—	300	5000	Word	Card Punch	INA	150 CPM	INA						
							Printer	Maul	80 CPS	1						
Core	200	10,000	INA	300	INA	Word	Tape Reader	Ferranti	300 FPS	INA	INA				—	Z-31
							Tape Punch	Creed	50 FPS							
							Card Reader	INA	INA							
							Card Punch	INA	INA							
							Printer	Maul	80 CPS							
Core	1216	32,768	512	32	INA	Word	Tape Reader	Ferranti	150 FPS	1+	INA	30,000	200 / 150	2 / 16	Wired core memory for subroutines added in 64 word units. Each 4096 word memory unit has independent input-output connections.	X1
							Tape Punch	Creed	25 FPS	1+						
							Card Reader	BULL	700 CPM	1+						
							Card Punch	BULL	112 CPM	1+						
							Printer	INA	150/600 LPM	1+						
Core	2048	2048	1024	6	3	Word	Tape Reader	Philips Lab.	1200 FPS	1	Ampex	45,000	300 / 150	2 / 16	30 interpretive single address instructions initiating subroutines	PASCAL / STEVIN
							Tape Punch	Teletype	60 FPS	1						
							Card Reader	BULL	150/750 CPM	1						
Drum	16,384	16,384	—	10,000 for Block	0	128 Words	Card Punch	BULL	75/120 CPM	1						
							Printer	BULL	150 LPM	1						
Core	2048	65,536	4096	10	2	Word	Tape Reader	FACIT	500 FPS	8	FACIT	40,000	200 / 200	17 / 64	"Carousel" magnetic tape memory	EDB 2 / EDB 3
							Tape Punch	FACIT	150 FPS	8						
Drum	8192	8192	—	625	10,000	32 Words	Card Reader	INA	700 CPM	8						
							Card Punch	INA	120 CPM	8						
Core	1024	1024	—	10	4	Word	Tape Reader	FACIT	500 FPS	1	No Magnetic Tape				The operation times include indexing and counting. Every operation may be conditional.	G1ER
Drum	12,000	12,000	—	500	500 Block Access	40 Words	Tape Punch	FACIT	150 FPS	1						
							Typewriter	Friden	10 CPS	1						

other more advanced relay computer, the Z 5, appeared in 1953. In 1958 Zuse introduced a vacuum-tube 8192-word magnetic drum computer, the Z 22. This is a medium-scale wired-core microprogrammed computer with extremely flexible programming.

In 1960 the Z 23 and Z 31 were announced. The Z 23 is a solid-state version of the Z 22, with an additional 240-word magnetic core memory. The Z 31 is a new, small, general-purpose solid-state computer with a basic magnetic core memory of 200 words, expandable to 10,000 words. Like the Z 22, it uses paper tape as its input-output medium and a typewriter for printed output.

The Netherlands

Contributions in the information processing field from The Netherlands have been high for the total computer activity in the country. The general emphasis is on the smaller computer systems.

Mathematisch Centrum: The Mathematisch Centrum was founded in 1946 as a government-sponsored nonprofit organization to work in the fields of pure and applied mathematics, statistics and digital computers. It was engaged in early developments of relay and magnetic drum computers, and built the ARMAC (Automatische Rekenmaschine Mathematisch Centrum), completed in June, 1956, and still in operation.

N.V. Electrologica: In 1958, under sponsorship of the Nillmij Insurance Company of Amsterdam, the transistor magnetic-core X 1 computer was designed by the Mathematisch Centrum. To fulfill the demands for additional X 1 computers Nillmij organized a new company—N.V. Electrologica—to make copies of the X 1 and to expand the computer's input-output capabilities. The engineering and fabrication group from the Mathematisch Centrum was transferred to the new company.

N.V. Philips Gloeilampen Fabrieken: The Philips organization, one of the largest electrical component manufacturing companies in the world, has its main research and development laboratories in The Netherlands. To keep abreast of the new applications of components in computers, the company is building two computers—PASCAL and STEVIN—for its own use. They are identical, except for input-output equipment.

Philips is also engaged in the design and construction of an electronic system for air traffic control. In June, 1960, the gigantic digital data transmission system to be used for the United Airlines reservation system in the United States was nearing completion.

Sweden

Scene of some of Europe's earliest computer activity, Sweden is currently active in research, development and production. The work stems from the government's Swedish Board for Computing Machinery (Matematikmaskinnamnden). The Board was active in early computer development. Its BESK computer, completed in 1953, was used as a pattern for the early machines built by FACIT and SAAB, and by the Dansk Institute for Matematikmaskiner in Copenhagen.

FACIT: FACIT Electronic, a subsidiary of FACIT-Atvidabergs, is one of Sweden's major data processing equipment manufacturers. The FACIT EDB computer is an almost exact copy of the BESK computer developed by the Swedish Board. The first machine produced is installed in the data processing center in Stockholm established and maintained by the company, providing computing service on a rental basis. The current model, the EDB 3, incorporates the new FACIT ECM 64 Carousel memory, described earlier.

SAAB: SAAB, well known for its aircraft and automobile production, is also active in digital computation. The company built a BESK-type computer for its own use and has built a transistorized airborne navigation computer. A solid-state commercial computer is in development.

Denmark

In 1953 the Academy of Sciences in Denmark formed a new institute, Regnecentralen (Dansk Institut for Matematikmaskiner), to work in the field of digital computer development and application. The group patterned its first computer, the DASK, after the BESK computer designed by the Swedish Board for Computing Machinery. The DASK was built and put into around-the-clock operation in early 1958.

In connection with computing and consulting work for the Geodetic Institute of Denmark, Regnecentralen was requested to design and build a new computer for the Institute. This computer, GIER, is a transistor parallel computer with magnetic core and drum storage. The computer was planned for considerable programming flexibility and simplicity.

IV. Acknowledgment

The author gratefully acknowledges the assistance received from the many individuals in Europe who supplied him with the information contained in this article. The author assumes full responsibility for the statements made and for the interpretation of any material supplied to him by his associates in Europe.

Special recognition is also given to Franklin Weikel, who was responsible for over-all editing; Mrs. Joyce Finley and Ernest Cohen, who extracted information and compiled the computer comparison tables; Miss Sally Dolly, who cataloged and organized the European material; Miss Hazel Andersen, who transcribed the trip reports dictated in Europe; and Miss Nancy Egmore and Mrs. Gloria Jean White, who typed the manuscript.

Correspondence

Shift of Peak Voltage with Temperature in Tunnel Diodes*

It is the purpose of this note to point out an effect in the static characteristics of tunnel diodes which is as yet unreported.

With decreasing temperature, the peak location moves to a higher voltage. This effect is found to exist in germanium, silicon, and gallium-arsenide tunnel diodes (and probably in other tunnel diodes too). The shift in voltage is not negligible. Shifts from 15 to 70 per cent (of the value at room temperature) have been observed from room temperature to liquid nitrogen temperature. Fig. 1 shows a picture of the peak voltage shift[1] with temperature.

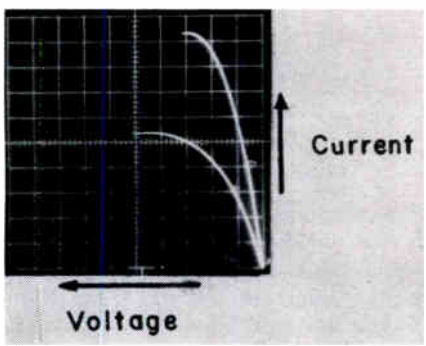

Fig. 1—Experimental result showing the shift of peak voltage of Ge tunnel diode. The upper curve corresponds to room temperature. The lower curve corresponds to liquid nitrogen temperature.

Among the possible contributing factors to this shift are:

1) temperature shift of the Fermi level,
2) change of the tunneling probability with temperature because of the change in both the tunneling barrier height and width, and
3) broadening of the band gap at lower temperatures.

Not all of the above mentioned sources shift the peak to a higher voltage, though the peak shifts because of all these factors combined, and others. Some simple calculations indicate that the effect of each of the above three factors is non-negligible.

Work is under way to gain a better understanding of this phenomenon. It is hoped that more extensive and quantitative discussion of this effect may be published at a later date.

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* Received by the IRE, August 3, 1960. This note presents results of one phase of research sponsored by Rome Air Dev. Center, Griffiths Air Force Base, N. Y., under Contract No. AF 30(602)-2177.

[1] Dr. N. Holonyak, Jr., of G.E. and Dr. T. A. Longo of Sylvania have told the author that they independently observed this same phenomenon.

Optimum Performance of Learning Machines*

Definitions and Basic Principle

It is certainly not easy to give a definition of learning, that can be agreed upon by everybody. However, I think that most people would not like to say that a computer has learned to solve a differential equation, when it has been programmed to do so, but would concede that it is a learning machine, one which can distinguish circles from squares after it has been shown a finite number of circles and squares, *as examples*. In other words, one would like to associate the word "learning" more with the inductive than with the deductive ability of a machine.

Therefore, as a working hypothesis, I propose the following definition of learning: the ability of making correct assignments or statements, *as if* the machine had guessed a rule.

Once the above definition is accepted, so that no rules are given to the learning machine during the learning process, it seems clear that the most any machine can do is to evaluate probabilities, by keeping scores of past successes and failures to make the best guesses on the outcome of future similar situations. The study of learning machines becomes, then, a branch of probability theory (in its wider sense, which includes sequential analysis, the theory of games, etc.) and lends itself to a precise mathematical analysis.

The following basic principle can then be stated: *Every learning machine, no matter how "intelligent," cannot outperform a mathematician, using probability theory at its best, and having the same information.*

The above statement looks trivial, but so does the second principle of thermodynamics. And exactly as in the latter case, we have now an upper limit for the efficiency of any learning machine, to be used as a standard of comparison for evaluating the performance of any actual learning machine.

In the following section an example is discussed, to illustrate how the principle works in specific cases.

The Elementary Perceptron

One type of learning machine—the perceptron—has been discussed by Rosenblatt.[1-4]

* Received by the IRE, August 10, 1960. Work done during the summer of 1960 at Philco Corporation, Philadelphia, Pennsylvania, where the author was visiting as a consultant.

[1] F. Rosenblatt, "The Perceptron—A Theory of Statistical Separability in Cognitive Systems," Cornell Aeronautical Lab., Inc., Cornell University, Ithaca, N. Y., Rept. No. VG-1196-61; January, 1958.

[2] F. Rosenblatt, "Two Theorems of Statistical Separability in the Perceptron," Cornell Aeronautical Lab., Inc., Cornell University, Ithaca, N. Y., Rept. No. VG-1196-62; September, 1958.

[3] R. D. Joseph, "On predicting perceptron performance," 1960 IRE International Convention Record, pt. 2, p. 71.

[4] F. Rosenblatt, Perceptron simulation experiments," Proc. IRE, vol. 48, pp. 301–309; March 1960.

An array of photocells, acting as sensory units (S units) are randomly connected to the so-called associative units (A units). The output of an S unit to an A unit can be positive or negative. The A units are threshold devices that, when active, fire a certain "stored value" into a response unit. The stored value is constantly corrected in each A unit during the training period by a "reinforcement rule," *i.e.*, a feed-back correction which depends on whether the response was correct or not.

Let us examine the operation of the perceptron in the light of the principle formulated in the preceding section. We can easily distinguish two different functions in each A unit, which correspond to the threshold value and to the stored value.

The function of the threshold value is simply to provide the A unit with a binary piece of information on the existence or nonexistence of a given relation. This might be, for example, the information whether the 5th, 8th, 25th, 37th, and 85th S units are excited in greater or lesser number than the 6th, 28th, 33rd, 95th, and 96th S units. Whether this is pertinent information in order to recognize a certain class of patterns is another question. However, if the connections among the S units and the A units are fixed and the threshold is fixed, it is beyond the control of the perceptron to change these pieces of information into other more useful data.

At this point, it is worth noticing one of the best ideas in the perceptron concept: the random connections. This may be expressed in plain words by saying that if you don't know which are the best criteria for a certain purpose—and probably there are no best criteria for a machine of sufficiently wide scope—or if you are afraid that your criteria may be biased, take random criteria. Chances are that with a sufficiently great number of criteria (A units) there will always be enough of them which provide useful information.

Now that we know what information the perceptron can obtain from a stimulus (a bit from each A unit), we can apply our principle and ask the mathematician what data he would like to have to make statistical inferences. He would, of course, ask for frequencies of past events—those which happened during the training period. These frequencies are, therefore, the best values to store, and here is where the second function of the A units comes in. Let us be specific. Assume that we want the perceptron to be able to separate the universe of patterns to be shown to it into the t classes $1, 2, \cdots, r, \cdots, t$. Let N_r be the number of patterns of class r shown during the training period and $n_r(A_k)$ the number of them activating the kth A units; then a mathematician would like to have on record the matrix

$$M_{rk} = \frac{n_r(A_k)}{N_r}. \qquad (1)$$

An unknown pattern X with excitation function $E_X(A_k)$,

$$E_X(A_k) = \begin{cases} +1 \text{ if } A_k \text{ is } \textit{active}, \text{ when the pattern } X \text{ is shown,} \\ 0 \text{ if } A_k \text{ is } \textit{inactive}, \text{ when the pattern } X \text{ is shown,} \end{cases} \quad (2)$$

would then be assigned to that class r of patterns for which the quantity

$$Z_r = \sum_k \left[E_X(A_k) \ln M_{rk} + \{1 - E_X(A_k)\} \ln (1 - M_{rk}) \right] \quad (3)$$

is a maximum. This is the "best bet" according to probability theory, if correlations among different active units A_k, A_l, $\cdots$ for a given stimulus are neglected, this being the case for elementary perceptrons with A units not serially connected.

The learning process—an increased efficiency of the machine as the number of patterns shown during the training period increases—is then simply related to the fact that frequencies tend asymptotically to probabilities.

Without much loss of generality, assume that the number of patterns shown during the training period is the same for all the t classes of patterns: $N_1 = N_2 = \cdots = N_k = \cdots = N_t$. Then from (3) one sees that the optimum performance would be achieved by storing t values in each A unit (or $2t$, if one prefers to store independently both $\ln M_{rk}$ and $\ln (1 - M_{rk})$). In the perceptron discussed so far in the literature, one stores only *one* value in each A unit. Which is the best single function of the t optimal values, what reinforcement rule one has to use, if one wishes to keep the stored values constantly "up to date" during the training period, etc. is then to be decided by comparison with the optimum conditions (1)–(3).

This is, however, only one aspect of the problem. Once we have obtained the optimum requirements, there is no longer a need for looking at perceptrons along the line of the original presentation of Rosenblatt. For example, why look for *one* best function to store in each A unit? Is it really so much simpler to store *one* function than t functions, that one should consider it worthwhile to pay probably a very high price in efficiency for it? Although the present note is not intended to present any particular embodiment, it is not difficult to think of various possibilities for practical solutions.[5]

So far, our principle has been used to improve the memory part of the perceptron. What about the other function of the perceptron which is related to collecting the information from the outside world? Apart from trivial suggestions, such as to increase the number of A units, a straightforward application of our principle leads to the suggestion of *correcting the threshold of each A* unit. Those A units having nearly equal probability of being active for most classes of patterns should change their threshold. This amounts to a change in the binary piece of information provided by the A unit to the perceptron "mind." Since a criterion which activates equally an A unit for most classes of patterns is a bad criterion, nothing is to be lost by changing to a new one (by changing threshold) and possibly one may hit upon a good criterion, which will then tend to be stabilized. Here again, we co not want to discuss particular solutions, although it is not difficult to think of them.[6]

Our principle can also be applied in discussion of the proper balance between the two functions (thresholds and stored values) in order to avoid the mistake of correcting for one, when the performance is poor mainly because of the other.

In short, the principle seems to be a basic one for the design of any perceptron; and conversely, the fact that it can be used in such a case proves that the perceptron is a learning machine, where learning means nothing else than computation of probabilities, according to our definition.

A final remark: If our principle is true, it should apply to the human brain as well, whether it works in a perceptron-like manner, as Rosenblatt suggests, or not. A quantitative measurement of the efficiency of the brain—in relation to an ideal mathematical brain having some specified properties in common with the real one—could then be one of the exciting possibilities of the future.

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I would like to thank C. V. Bocciarelli of Philco Corporation for stimulating discussions, and F. Rosenblatt and R. D. Joseph of the Cornell Aeronautical Laboratory for useful correspondence.

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[5] For example: the threshold of an A unit operates a switch which sends a beam of light of uniform intensity to a region to the left or to the right of a photographic film strip, according to whether or not the A unit is active. Different classes of patterns correspond to different regions along the strip. If an equal number of patterns of each class is shown during the training period, with equal exposure time for each pattern, the density of grains in each region could be made directly proportion to the $\ln M_{rk}$ and $\ln (1 - M_{rk})$ of (3). A whole series of A units could be arranged in a rectangular plate—each vertical strip being an A unit, each horizontal row corresponding to a certain class of patterns.

An unknown pattern would then be recognized by comparing the total amount of plating in the various activated regions of the different horizontal rows. With a small perceptron, one could then even use an interchangeable set of "recorded plates" for special purposes, etc.

[6] In the example of footnote 1, one could change the threshold of those A units, which are more uniformly plated and repeat the training sequence. Note how the correction to the stored values and to the thresholds differs since their function is different.

Shot Noise in Tunnel-Diode Amplifiers*

In the above paper in these PROCEEDINGS, J. J. Tiemann[1] refers to a note by K. K. N. Chang[2] and then comments that "Because of some errors in analysis and interpretation, some of the conclusions in this letter are incorrect." He does not amplify his allegation nor make further reference to it. This is regrettable. Those who know Mr. Tiemann and his contributions to the field may be able to discern and evaluate the corrections he implies that he has made. The general reader is not so fortunate.

I presume that the implicit criticism of the Board of Editors of the PROCEEDINGS who accepted his paper as well as Chang's, is unwitting. It is certainly unjustified.

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[2] K. K. N. Chang, "The optimum noise performance of tunnel-diode amplifiers," PROC. IRE, vol. 48, pp. 107–108; January, 1960.

Experimental Tunnel-Diode Mixer*

Two analyses of the tunnel diode used as a mixer with conversion gain were published simultaneously.[1,2] These analyses predict contradictory performance for this device because of basic differences in 1) the assumed diode I-V characteristic, 2) the effective diode shot noise current, and 3) the conditions necessary for optimum noise factor. Breitzer's more detailed analysis,[2] which was published without supporting experimental data, predicts considerably worse noise performance for this device than that claimed in Chang, *et al.*[1] The purpose of the experimental work summarized in this letter[3,4] was to further investigate the performance of the tunnel-diode mixer, and the result has been substantial agreement with Breitzer's analysis.

Fig. 1 shows the experimental tunnel-diode mixer. Note that two series-resonant traps are provided to reduce otherwise significant spurious responses at the image and intermediate frequencies (100 and 30 Mc). The 1.1 μh choke (self-resonant at 160 Mc) provides a low-resistance dc return that minimizes the effect of rectified local-oscil-

* Received by the IRE, September 19, 1960.

[1] J. J. Tiemann, "Shot noise in tunnel diode amplifiers," PROC. IRE, vol. 48, pp. 1418–1423; August, 1960.

* Received by the IRE, September 30, 1960. The work reported here was conducted under Contract AF 30 (602-1854 with the Air Res. and Dev. Command, Rome Air Dev. Center, Griffiss Air Force Base, N. Y.

[1] K. K. N. Chang, G. E. Heilmeier, and H. J. Prager, "Low-noise tunnel-diode down converter having conversion gain," PROC. IRE, vol. 48, pp. 854–858; May, 1960.

[2] D. I. Breitzer, "Noise figure of tunnel-diode mixer," PROC. IRE, vol. 48, pp. 935–936; May, 1960.

[3] For more details, see J. C. Greene, *et al.*, "Eighth Quarterly Progress Report on Application of Semiconductor Diodes to Low-Noise Amplifiers, Harmonic Generators, and Fast-Acting TR Switches," Airborne Instruments Lab., Melville, N. Y., Rept. No. 4589-I-8; June, 1960.

[4] For more details, see J. C. Greene, *et al.*, "Ninth Quarterly Progress Report on Application of Semiconductor Diodes to Low-Noise Amplifiers, Harmonic Generators and Fast-Acting TR Switches," Airborne Instruments Lab., Melville, N. Y., Rept. No. 4689-I-9; September, 1960.

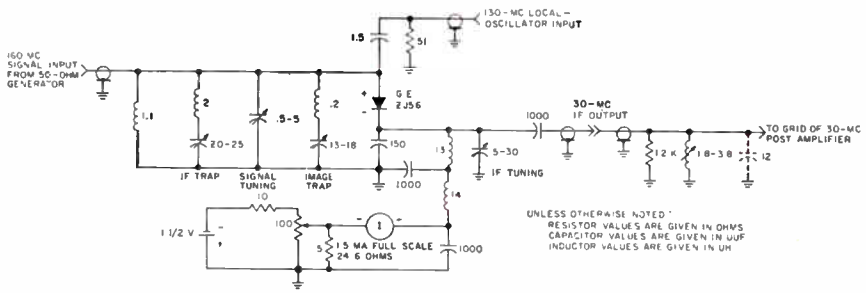

Fig. 1—Experimental tunnel-diode mixer.

TABLE I
PERFORMANCE OF TUNNEL-DIODE MIXER

Operating point	Over-all noise factor (db)				Transducer gain (db)	
	Average current (ma)	Measured	Theoretical (Breitzer)	Theoretical (Chang, *et al.*)	Measured	Theoretical (Breitzer)
1	0.86	13.2	11.8	7.3	4.6	5.4
2	0.70	11.8	9.9	6.5	1.0	3.0

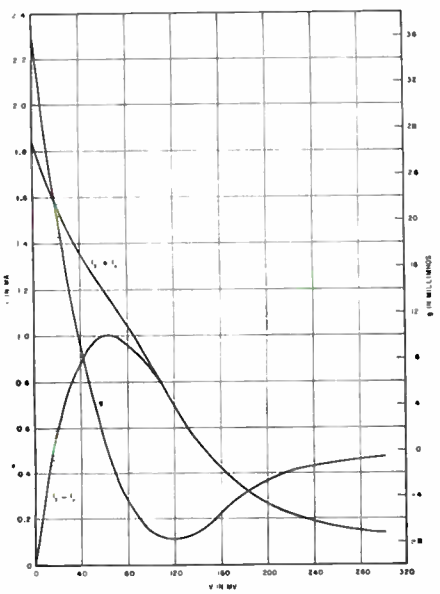

Fig. 2—Currents and small-signal conductance vs voltage for a GE ZJ56 tunnel diode.

lator current on the operating point without loading the signal input circuit.

The damping of the near optimum source resistance of 50 ohms was enough to prevent oscillation, even with large local oscillator amplitudes, when the diode was initially biased at the peak of the I-V curve (a near optimum bias point); this damping also insured a positive IF output conductance. Then two distinct operating points could be obtained by varying the local oscillator drive: 1) maximum transducer gain, and 2) best over-all noise factor. The values of transducer gain and over-all noise factor (which includes the small contribution of a postamplifier having a 2-db noise factor) measured at these operating points are shown in Table I.

Application of Breitzer's analysis to the circuit of Fig. 1 requires a detailed knowledge of the diode characteristics, the local-oscillator drive, and the values of source and load resistances. The diode characteristics are shown in Fig. 2, and include the net current $(i_f - i_r)$, the current for calculating shot noise $(i_f + i_r)$, and the small-signal conductance (g), each plotted versus applied voltage. The first and third were measured in a standard manner, and the second was calculated from the first as by Breitzer. The local-oscillator drive was deduced from precise readings of the average diode current. Thus, assuming the local-oscillator voltage at the diode terminals to be a pure sinusoid, the average current with the local oscillator connected could be correlated with the dc resistance in series with the diode (about 30 ohms) and a Fourier analysis of the $(i_f - i_r)$ characteristic in Fig. 2 to give the peak and average local-oscillator voltage at the diode terminals. Further Fourier analysis of the appropriate curves in Fig. 2 then gave values of parameters g_0, g_1, $I_{0_f} + I_{0_r}$, and $I_{1_f} + I_{1_r}$ to be used in Breitzer's equations. Last, the values of source and load resistances (r_1 and r_2) in Fig. 1 were 50 and 1000 ohms (the former value, though not quite optimum, was used for convenience; the latter value was not critical and includes the IF coil losses). The resultant theoretical values of gain and noise factor are shown in Table I together with appropriate noise factor values obtained from the theory of Chang, *et al.*[1] Following Chang, *et al.*, these latter values were determined by assuming the theoretical gain is the measured gain and including the same small second-stage contribution.

Table I shows fair agreement between the measured values of noise factor and transducer gain and Breitzer's theoretical values. The theoretical noise factor values of Chang, *et al.*, are seen to be quite optimistic.

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Subharmonic Generation with Nonlinear Reactance—A Circuit Analysis*

INTRODUCTION

The use of nonlinear reactive circuits to provide subharmonic generation has been mentioned frequently in the literature. This note presents a circuit analysis of subharmonic generators using nonlinear reactance. The approach is similar to that used successfully in the analysis of harmonic generators.

This analysis proceeds directly from the treatment of frequency multipliers presented by Leeson and Weinreb,[1] and freely uses results and equations derived therein, with the same notations. In order that the terminology of the two analyses will correspond, the output (subharmonic) frequency of the frequency divider to be considered will be denoted ω, and the input, or fundamental, frequency will be denoted $N\omega$ in a divider of order N.

ANALYSIS

From the circuits of Figs. 1 and 2, the circuit models shown in Figs. 3 and 4 are

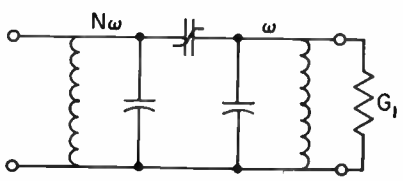

Fig. 1—Parallel tuned divider.

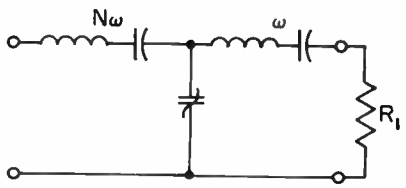

Fig. 2—Series tuned divider.

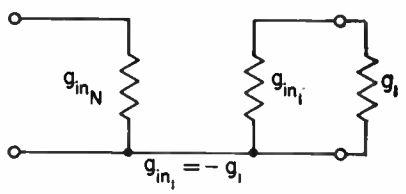

Fig. 3—Equivalent circuit of parallel tuned divider.

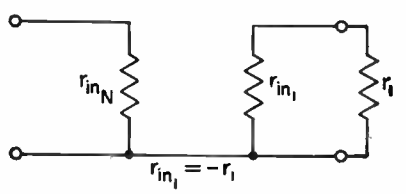

Fig. 4—Equivalent of series tuned divider.

* Received by the IRE, June 7, 1960. This work performed at Hughes Aircraft Co., Culver City, Calif.
[1] D. B. Leeson and S. Weinreb, "Frequency multiplication with nonlinear capacitance—a circuit analysis," PROC. IRE, vol. 47, pp. 2076–2084; December, 1959.

derived. It may be seen that for the proper driving phase, the subharmonic terminals present a negative resistance to the subharmonic load. Thus, the device operates as an oscillator, and in the steady-state situation presents a negative resistance equal to the load resistance.

In the circuit shown in Fig. 1, the circuit equations derived in the reference under the conditions of small-signal operation and ideal filters are used as a starting point. The input and output circuits are assumed to be resonant at $N\omega$ and ω, as shown in Fig. 3. Setting V_1 real for convenience, the equations of interest are

$$q_{1i} = N\alpha_N v_1^{N-1} v_{Ni}, \tag{1}$$

and

$$q_{Nr} = \alpha_N v_1^N. \tag{2}$$

The equations correspond to (18) and (19) of the frequency multiplier analysis, and the notation is the same as in the reference; reactive terms are omitted.

The conductance seen by the load is

$$g_{in_1} = \frac{i_1}{v_1} = \frac{\omega q_{1i}}{v_1} = -N\omega\alpha_N v_1^{N-2} v_{Ni}. \tag{3}$$

For the proper phase of v_N, this conductance is negative. At equilibrium, the load conductance g_l is

$$g_l = -g_{in_1}, \tag{4}$$

where g_{in_1} is the conductance seen by the load.

Solving (2) for v_1, and substituting in (3) and (4) yields the value for v_{Ni},

$$v_{Ni} = \frac{g_l}{N\omega\alpha_N^{2/N}} q_{Nr}^{(2/N-1)}. \tag{5}$$

Thus, the normalized input conductance at the fundamental frequency $N\omega$ is

$$g_{in_N} = \frac{Nq_{Nr}}{v_{Ni}} = \frac{(N\omega)^2\alpha^{2/N}}{g_l} q_N^{(2-2/N)}. \tag{6}$$

The circuit equations corresponding to the model shown in Fig. 4 are

$$v_{1_i} = N\beta_N q_1^{N-1} q_{N_i} \tag{7}$$

and

$$v_{N_r} = \beta_N q_1^N. \tag{8}$$

[Eqs. (7) and (8) above are (30) and (31) in Leeson and Weinreb,[1] with reactive terms omitted.]

The normalized input resistance at the fundamental frequency,

$$r_{in_N} = \frac{v_{Nr}}{N\omega q_{N_i}} = \frac{\beta_N^{2/N}}{\omega^2 r_1} v_N^{(2-2/N)}, \tag{9}$$

is derived by a procedure similar to that used above. Assuming resonant input and output, (6) and (9) are the normalized small-signal input parameters of the subharmonic oscillators of Figs. 1 and 2.

Semiconductor Nonlinear Capacitor

By employing a nonlinear element whose capacitance is of the form

$$C = \frac{C_1}{(\phi + V)^\gamma},$$

the input parameters of the subharmonic oscillator can be "unnormalized" for the circuit of Fig. 1 exactly as in the frequency multiplier analysis to yield

$$G_{in_N} = \omega C_0 \frac{N^2\alpha_N^{2/N}}{(1-\gamma)^2} \frac{\omega C_0}{G_l} \cdot \left\{\frac{I_{in_N}(1-\gamma)}{2\omega C_0 V_0}\right\}^{(2-2/N)}, \tag{10}$$

and for the circuit of Fig. 2 to yield

$$R_{in_N} = \frac{1}{\omega C_0}\left(\frac{1}{\omega C_0 R_l}\right)\beta_N^{2/N}(1-\gamma)^2 \cdot \left\{\frac{V_{in}}{2V_0}\right\}^{(2-2/N)}. \tag{11}$$

Losses

Losses may be handled in the same manner as in the frequency multiplier analysis. The model shown in Fig. 5 is pertinent here.

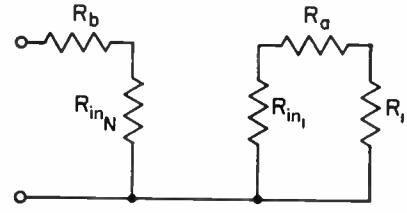

Fig. 5—Equivalent circuit for losses.

The efficiency, or ratio of output to input power, is calculated from

$$\frac{P_{in}}{P_{out}} = \left(1 + \frac{R_b}{R_{in_N}}\right)\left(1 + \frac{R_a}{R_l}\right), \tag{12}$$

where R_a and R_b are, respectively, the equivalent output and input loss resistances, and are composed of filter and varactor losses.

Special Properties

For the interesting case of $N=2$, the input conductance of Fig. 1 becomes

$$G_{in} = \frac{\gamma\omega C_0 I_{in}}{G_l V_0}. \tag{13}$$

Note that the input voltage, $E_{in} = I_{in}/G_{in}$, is equal to a constant, implying that the circuit of Fig. 1 will function as a voltage limiter if the source voltage is sufficiently high to initiate oscillations. This is the phenomenon mentioned by Siegman.[2]

In the dual case shown in Fig. 2, the input resistance R_{in} for $N=2$ is

$$R_{in} = \frac{\gamma V_{in}}{4(\omega C_0)^2 R_l V_0}. \tag{14}$$

Here the input current, $I_{in} = E_{in}/R_{in}$, is a constant if the circuit is oscillating. Numerous uses for this unusual ability to limit voltage or current in this manner should suggest themselves. The voltage limit for the circuit in Fig. 1 is

$$V_2 = \frac{G_l v_0}{\omega C_0 \gamma}. \tag{15}$$

The current I_2 in Fig. 2 limits to the value

$$I_2 = \frac{4(\omega C_0)^2 R_l V_0}{\gamma}. \tag{16}$$

Note that the quantities which are limited are the input voltage or current, rather than the load voltage or current at the subharmonic frequency.

Conclusion

The general method of nonlinear circuit analysis presented in Leeson and Weinreb[1] appears to apply with satisfactory validity to the problem of the subharmonic oscillator or generator employing nonlinear reactance. As in the reference, the normalized results are general in application and, with the proper "unnormalization" procedure, may be applied to the case of a large class of nonlinear elements.

Subharmonic oscillators have already been used in high-frequency computer applications. Other suggested uses include passive count-down circuitry, and the voltage- or current-limiting property of the divide-by-two circuit offers a number of interesting possibilities. The conditions for minimum loss may be determined in much the same manner as in the case of frequency multipliers.

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[2] A. E. Siegman, "Phase distortionless limiting by a parametric method," Proc. IRE, vol. 47, pp. 447–448; March, 1959.

The Cryosistor—A New Low-Temperature Three-Terminal Switch*

Recent publications[1,2] have described impact ionization in germanium at liquid helium temperature, and device applications utilizing the unique voltage-current characteristics of bulk material as a result of this ionization phenomenon. However, these devices pose circuit limitations, because all of their electrodes are ohmic contacts to the germanium bulk. To extend device possibilities utilizing this phenomenon and to provide a tool for investigating the ionization process itself, a three-terminal device has been constructed. In this device, a reverse biased p-n junction is used to control the ionization between two ohmic contacts. A preliminary study of the properties of this structure indicates its promise as a fast monostable or bistable (memory) switch for computer applications; as a pulse amplifier; as a controlled sinusoidal or relaxation oscillator; and also as a unipolar (field effect) transistor after ionization.

Cryosistor Characteristics

The device consists of a thin wafer of germanium with two ohmic contacts (H and

* Received by the IRE, June 10, 1960. This work was supported in part by the Office of Naval Research under Contract Nonr 760(69).

[1] A. L. McWhorter and R. H. Rediker, "The cryosar—a new low-temperature computer component," Proc. IRE, vol. 47, pp. 1207–1213; July, 1959.

[2] M. C. Steele, L. Pensak, and R. D. Gold, "Pulse amplification using impact ionization in germanium," Proc. IRE, vol. 47, pp. 1109–1117; June, 1959.

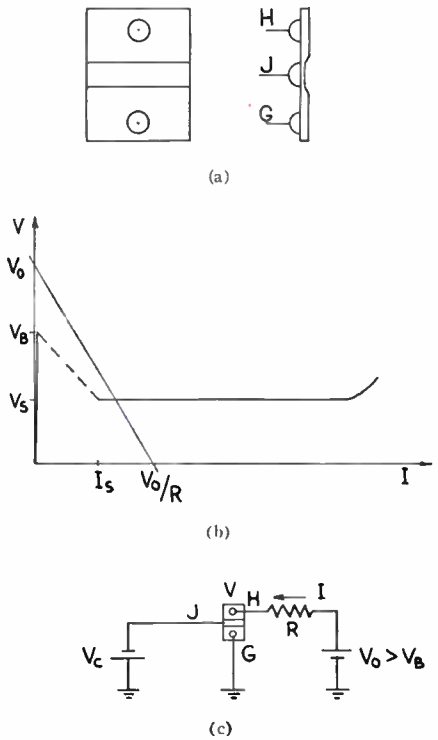

Fig. 1—(a) Top and side views of an experimental cryosistor. The approximate dimensions of the wafer are 90×70×5 mils. The ohmic contacts (H) and (G) to the n-type germanium are lead-antimony; and the long p-n junction J is indium-alloyed. (b) Schematic representation of the voltage-current characteristic existing between points (H) and (G) with no bias applied at (J). Typical values for the cryosistors used are $V_B = 14$ volts, $I_S = 50$ μamp. The resistance before breakdown is about 10^{11} ohms. A typical loadline with reference to Fig. 1(c) is shown. (c) The dc circuit used with a cryosistor, indicating the proper polarities of applied voltages.

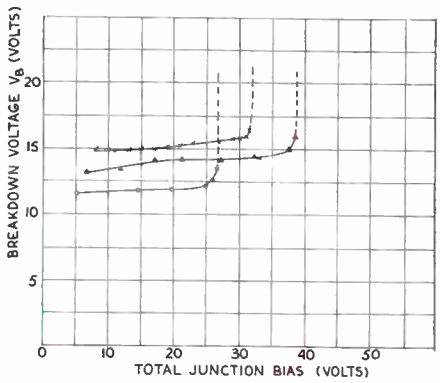

Fig. 2—Breakdown voltage (V_B) as a function of the reverse bias (including the self-bias caused by the drop inside the sample) for three specimens, all made from the same crystal, but of somewhat different dimensions.

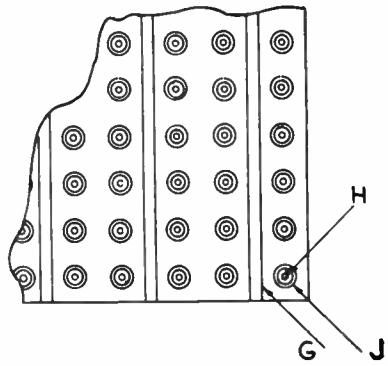

Fig. 3—Top view of a proposed array of memory elements showing common ohmic ground strips (G) and ohmic dots (H) enclosed by ring shaped p-n junctions (J).

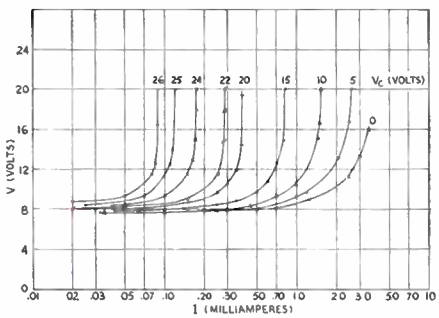

Fig. 4—Voltage-current characteristics between the ohmic contacts after breakdown for different values of reverse junction bias.

G) and an indium-alloyed p-n junction (J), as shown in Fig. 1(a). The material of the wafer in the samples constructed is n-type compensated germanium of the type that has been used in the Lincoln Laboratories' bistable cryosar. Because of the combination of n- and p-type impurities, this germanium exhibits a negative resistance characteristic between the high- and low-resistance states at liquid helium temperature.

With no bias applied at (J), the voltage-current characteristic between (H) and (G) is as shown in Fig. 1(b). When the junction is biased in the reverse direction, the depletion of carriers from the region under the junction reduces the size of the conducting channel. When the bias is sufficient for the depletion layer to reach the opposite surface, conduction between (H) and (G) ceases. This process at ordinary temperatures is the basis of operation of the well-known unipolar transistor.[3,4] In the cryosistor, this process has been found to control the ionization between contacts H and G at liquid helium temperatures. If the bias voltage exceeds a certain value, no ionization occurs even if V_0 [Fig. 1(c)] is appreciably larger than V_B, and as seen from Fig. 2, at less than this critical bias the breakdown voltage increases only slightly with increase of bias. A critically biased cryosistor can thus be used as an amplifier of pulse voltage and power, since small pulses can then permit or prevent ionization of the material.

Owing to the biasing action of the voltage drop between points (J) and (G) and the bistable nature of the material itself, the voltage applied externally to (J) has actually two distinct critical values. With a constant $V_0 > V_B$ [Fig. 1(c)] applied at H, the ionized channel deionizes at a value V_{c_1} as V_c is raised. A subsequent reduction of V_c causes breakdown at a value V_{c_2} which is less than V_{c_1}. The difference between V_{c_1} and V_{c_2} depends upon the dimensions of the device and also upon the voltage-current characteristic of the bulk material. This provides the possibility for bistable switching of the type required in memory devices, providing that the dc bias is placed between the two critical values. Both modes of switching have been investigated, and present results show that bistable switching is possible with pulses of no more than 2×10^{-8} second duration, and that current rise times and decay times in the load are shorter than this amount, depending upon the pulse amplitude and the applied voltages. Shorter times may be possible, but this possibility was not explored (owing to equipment and technique limitations).

In addition to the ionization process itself, which is known to be fast[1] ($< 10^{-8}$ seconds), one of the factors influencing the response time is the capacitance of the p-n junction. In the present experimental devices, this has not been carefully controlled, but it could be reduced by reducing the junction area.

Since the ionization process is very localized, an array of a large number of such elements could be placed on a single wafer of germanium. A possible arrangement is suggested in Fig. 3, where the junction is made in the form of a ring enclosing one of the ohmic contacts to prevent undesired breakdown.

Among the advantages of this device are an isolated (high-impedance) input and the possibility for a convenient nondestructive readout by means of test pulses applied to the output circuit, which will not cause switching.

The Cryosistor as a Means to Study the Ionization Phenomenon

As a second objective, the cryosistor is proposed as an experimental structure for investigating the ionization of germanium at liquid helium temperatures. Recent experiments[5] have revealed the filamentary nature of the breakdown, *i.e.*, while the current before breakdown is distributed through the germanium bulk, after breakdown most of the current is concentrated in an ionized filament of small cross section. The present device provides a conducting channel of variable area, the approximate size of which can be calculated by using Poisson's equation for different values of junction bias. This provides a means for estimating the dimensions of the filament at various current values after breakdown. As the depletion layer and the filament surface come in contact, a rise in the voltage between the ohmic contacts should be observed.

Fig. 4 shows the voltage-current curves after breakdown with the junction bias as a parameter. The gradual rise in voltage with increasing current before the "pinch-off" current may indicate that either the filament or the depletion layer, or most likely both, do not have very sharply defined boundaries, and the calculation of the filament size from present data can yield at best an order-of-magnitude. At the lowest current at which the filament can exist, its diameter is found to lie between 10^{-4} and 10^{-6} cm, which is in the same range as a mean-free path of a free

[3] W. Shockley, "A unipolar field-effect transistor," Proc. IRE, vol. 40, p. 1365; November, 1952.
[4] G. C. Dacey and I. M. Ross, "Unipolar field-effect transistor," Proc. IRE, vol. 48, p. 970; August, 1953.
[5] A. L. McWhorter and R. H. Rediker, private communication.

carrier, and hence not unreasonable. More carefully chosen sample configurations are hoped to improve the accuracy of the method.

An extensive program has been undertaken in an effort to explore the ultimate limitations of the presently described device, as well as related impact ionization devices, to improve our understanding of the ionization phenomenon itself, to investigate the low-temperature characteristics of *p-n* junctions, and to study other materials in which impact ionization is observed at temperatures higher than that of liquid helium.

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Universal Representation of Electromagnetic Parameters in Presence of DC Magnetic Fields*

In a recent paper,[1] it has been shown that, by a suitable normalization of parameters, the electromagnetic properties of a uniform isotropic plasma (assuming the electron collision frequency to be a constant independent of electron velocity) can be universally represented in convenient form; either the dielectric coefficient plane or the complex propagation constant plane. It is the purpose of this note to point out that, by the appropriate choice of the normalizing parameters, the electromagnetic properties of a uniform, anisotropic plasma (*i.e.*, electromagnetic wave propagation in a uniform plasma in the presence of a dc magnetic field) are represented by the same expressions and the curves presented previously[1] can be equally applicable.

For electromagnetic wave propagation along the direction of the dc magnetic field applied to a uniform plasma (longitudinal propagation), the plasma becomes a doubly refracting medium with a dual value of the dielectric coefficient given by[2]

$$K_{\pm} = \left[1 - \frac{\omega_p^2}{\omega^2}\,\frac{1}{(1 \pm \omega_h/\omega)}\cdot\frac{1}{\left(1 + \frac{\nu^2}{\omega^2}\,\frac{1}{(1 \pm \omega_h/\omega)^2}\right)}\right] - j\left[\frac{\omega_p^2}{\omega^2}\,\frac{1}{(1 \pm \omega_h/\omega)}\cdot\frac{\frac{\nu}{\omega}\,\frac{1}{(1 \pm \omega_h/\omega)}}{\left(1 + 1\,\frac{\nu^2}{\omega^2}\,\frac{1}{(1 \pm \omega_h/\omega)^2}\right)}\right].$$

(The notation employed is the same as that given by Bachynski, Johnston, and Shkarofsky[1] and $\omega_h = (e/m)B_0$ is the electron cyclotron frequency.)

The plus sign corresponds to a circularly polarized wave rotating in the same direction, as positive particles (ions) gyrate under the influence of the dc magnetic field, and the minus sign corresponds to a circularly polarized wave rotating in the same direction as the negative particles (electrons).

If now we write

$$N_{\pm} = \frac{\omega_p^2}{\omega^2}\,\frac{1}{(1 \pm \omega_h/\omega)}$$

$$S_{\pm} = \frac{\nu}{\omega}\,\frac{1}{(1 \pm \omega_h/\omega)},$$

then the equation for the dielectric coefficient becomes

$$K_{\pm} = Kr_{\pm} - jKi_{\pm} = \left[1 - \frac{N_{\pm}}{1 + S_{\pm}^2}\right] - j\left[\frac{N_{\pm}S_{\pm}}{1 + S_{\pm}^2}\right].$$

This leads to exactly the same expressions [(7a) and (8a) of footnote 1] for the scattering (S) and density (N) parameters in terms of the real and imaginary parts of the dielectric coefficient of the plasma. Hence, for longitudinal propagation in a plasma in the presence of a dc magnetic field, Figs. 1 and 2 of footnote 1 can be used directly, provided N is taken to represent the new normalizing parameter $N_{\pm}$, and S to represent the new normalizing parameter $S_{\pm}$, when $N_{\pm}$, $S_{\pm}$ are positive. For negative $N_{\pm}$, $S_{\pm}$, which occurs only for the wave rotating in the direction of electron motion at RF frequencies below the electron cyclotron frequency ($\omega < \omega_h$), Figs. 1 and 2 mentioned above,[1] still apply if the curves are reflected about the $Kr = 1$ axis, as shown in Fig. 1 of this note.

Similar comments apply to the normalized collision parameter (C) and normalized RF frequency (F), provided that we redefine them as

$$C_{\pm} = \frac{\nu}{\omega_p}\,\frac{1}{(1 \pm \omega_h/\omega)^{1/2}}$$

$$F_{\pm} = \frac{\omega}{\omega_p}\,(1 \pm \omega_h/\omega)^{1/2}.$$

For electromagnetic wave propagation across the direction of the dc magnetic field (transverse propagation), the dielectric coefficient again has a dual value. When the electric vector E of the electromagnetic field is parallel to the applied dc magnetic field, the dielectric coefficient and propaga-

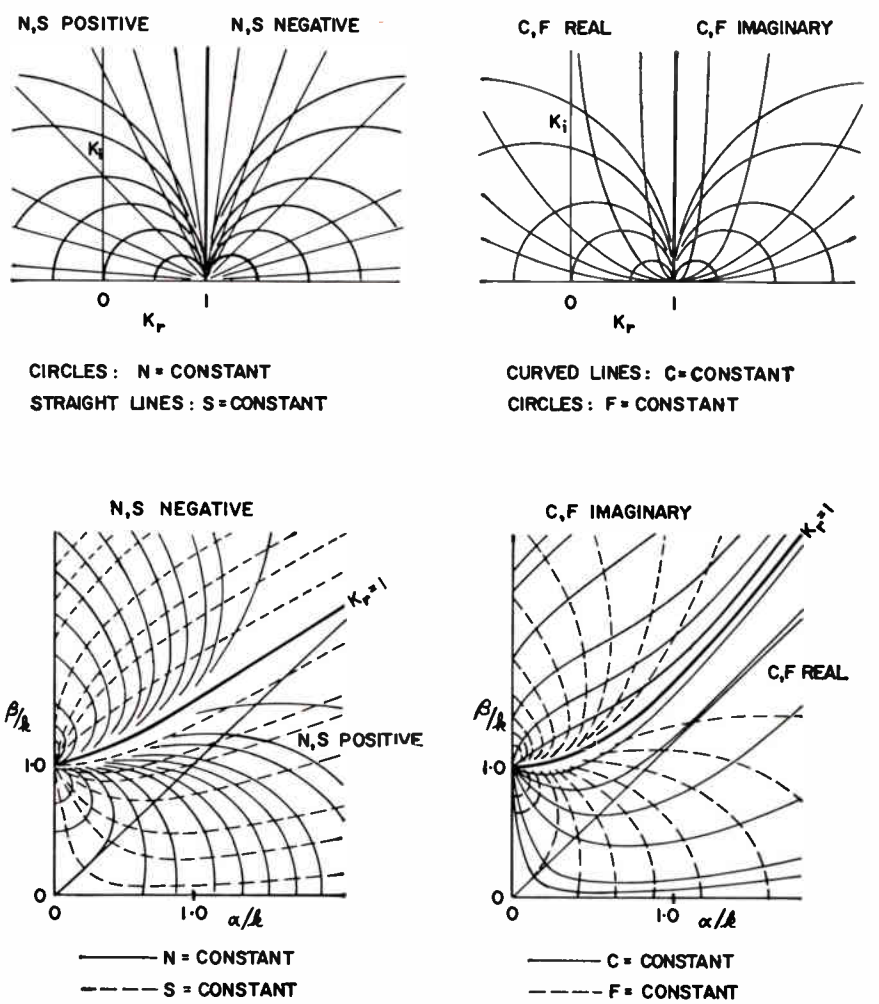

Fig. 1—Universal representation of the electromagnetic properties of a plasma in the complex dielectric coefficient plane and in the propagation constant plane.

* Received by the IRE, July 6, 1960.

[1] M. P. Bachynski, T. W. Johnston, and I. P. Shkarofsky, "Electromagnetic properties of high temperature air," PROC. IRE, vol. 48, pp. 347–356; March, 1960.

[2] M. P. Bachynski, I. P. Shkarofsky and T. W. Johnston, "Plasmas and the Electromagnetic Field," McGraw-Hill Book Co., New York, N. Y.; in press.

tion constants are identical to those in the absence of a magnetic field, so that the representations presented in footnote 1 apply directly. When the magnetic vector of the electromagnetic field H is parallel to the applied dc magnetic field, the above representations are less useful, but nevertheless valid, provided the N and S parameters are taken to be the new normalizing parameters N_x, S_x, given by

$$N_x = \frac{\omega_p^2}{\omega^2} \frac{(1-\omega_p^2/\omega^2)}{1-\dfrac{\omega_b^2+\omega_p^2}{\omega^2}+\dfrac{\nu^2}{\omega^2-\omega_p^2}} \Lambda$$

$$S_x = \frac{\nu}{\omega} \frac{1-\dfrac{\omega_p^2}{\omega^2}+\dfrac{\nu^2+\omega_b^2}{\omega^2-\omega_p^2}}{1-\dfrac{\omega_b^2+\omega_p^2}{\omega^2}+\dfrac{\nu^2}{\omega^2-\omega_p^2}},$$

where

$$\Lambda = \frac{(\omega^2-\omega_b^2-\omega_p^2)^2+\nu^2\omega^2\left[\left(1-\dfrac{\omega_p^2}{\omega^2}+\dfrac{\nu^2+\omega_b^2}{\omega^2-\omega_p^2}\right)^2+\dfrac{2(\omega^2-\omega_b^2-\omega_p^2)}{\omega^2-\omega_p^2}+\left(\dfrac{\nu\omega}{\omega^2-\omega_p^2}\right)^2\right]}{(\omega^2-\omega_b^2-\omega_p^2)^2+\nu^2[\nu^2+\omega^2+\omega_b^2-\omega_p^2+\omega_p^2(\omega_p^2-\omega^2)/\omega^2+(\omega^2+\omega_b^2)]}.$$

For small collision frequencies, the parameter Λ approaches unity.

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Gain Bandwidth Relations in Negative Resistance Amplifiers*

The recent invention of the tunnel diode and the re-emergence of the principles of parametric amplification have resulted in the engineering consideration of negative resistance amplifiers whose voltage gain is proportional to the reflection coefficient ρ, defined at the terminals of the active element as the square root of the ratio, power reflected to power available. Sard[1] and Seidel and Herrman[2] have shown that the gain bandwidth relation for these amplifiers need not be a simple product $\rho_0\Delta\omega = 2/\tau$. They have not, however, given the correct gain bandwidth relation for optimum maximally flat and stable response as a function of circuit complexity N. This letter attempts to give the correct relations for both maximally flat and equal ripple reflection response showing an asymptotic form $\ln \rho_0 \Delta\omega = \pi/\tau$ which agrees with a general gain bandwidth theorem. Stability of, and the effects of, loss in the active networks are considered, and the method of calculating circuit values is shown to rely upon existing tables.

The reflection coefficient defined at the terminals connecting an active element to a passive circuit is the reciprocal of that obtained when the sign of the real part of the active immittance function is reversed.

$$\frac{Z-Z_0^*}{Z+Z_0} \xrightarrow[Z_0 \to -Z_0^*]{} \frac{Z+Z_0}{Z-Z_0^*}. \quad (1)$$

This change allows a wide range of passive network theory to be applied to the active reflection problem. For the ideal tunnel diode representable as a parallel capacitance C_T, and negative conductance $-G_T$, we may immediately adapt Bode's[3] bandwidth theorem to read

$$\int_0^\infty \ln|\rho|\, d\omega = \frac{\pi G_T}{C_T}. \quad (2)$$

The optimum maximally flat active reflection response,

$$\rho\rho^* = \frac{1+(\omega/\omega_B)^{2N}}{\dfrac{1}{\rho_0^2}+(\omega/\omega_B)^{2N}}, \quad (3)$$

is the reciprocal of the passive Butterworth response. The N branch ladder network required to achieve this response, or its bandpass equivalent, is identical to a passive Butterworth network designed to give a reflection response $1/\rho$ with a parallel termination $G_T + i\omega C_T$. The normalized half power bandwidth is

$$\frac{C_T}{G_T}\Delta\omega = \omega_B(\rho_0^2-2)^{-1/2N}$$

$$= 2\sin\frac{\pi}{2N}\left(1-\frac{2}{\rho_0^2}\right)^{-1/2N}(\rho_0^{1/N}-1)^{-1}, \quad (4)$$

which for large N approaches

$$\frac{C_T}{G_T}\Delta\omega = \frac{\pi}{\ln\rho_0}. \quad (5)$$

The gain bandwidth relation (4) is exhibited in Fig. 1 for several values of ρ_0.

In a similar way, the equal ripple requirement leads to reciprocal Tchebycheff response

$$\rho\rho^* = \frac{1+\epsilon^2 T_N^2(\omega/\omega_T)}{\dfrac{1}{\rho_0^2}+\epsilon^2 T_N^2(\omega/\omega_T)}$$

$$T_N(\omega/\omega_T) = \cos\frac{1}{N}\cos^{-1}\frac{\omega}{\omega_T}, \quad (6)$$

with half peak power bandwidth

$$\frac{C_T}{G_T}\Delta\omega = \frac{C_T}{G_T}\omega_T \cosh\frac{1}{N}\cosh^{-1}\frac{1}{\rho_{0\epsilon}}$$

$$= 2\sin\frac{\pi}{2N}$$

$$\cdot \frac{\cosh\dfrac{1}{N}\cosh^{-1}\dfrac{1}{\rho_0}}{\left[\sinh\dfrac{1}{N}\sinh^{-1}\dfrac{1}{\epsilon}-\sinh\dfrac{1}{N}\sinh^{-1}\dfrac{1}{\rho_{0\epsilon}}\right]}. \quad (7)$$

Fig. 2 shows the equal ripple bandwidth for the case $\rho_{max}/\rho_{min} = \sqrt{2}$, and for several values of $\bar{\rho} = (\rho_{max}^2/2 + \rho_{min}^2/2)^{1/2}$.

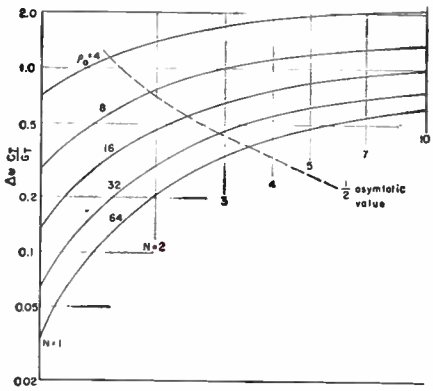

Fig. 1—Normalized half power bandwidth of maximally-flat reflection amplifier.

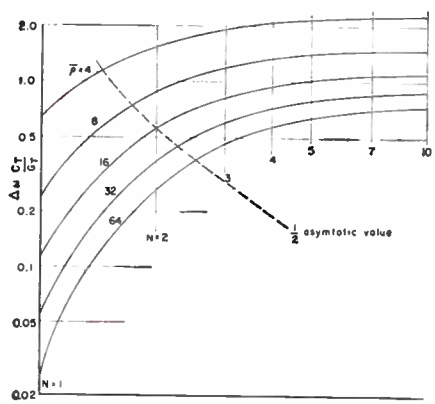

Fig. 2—Normalized bandwidth of ±1.5 db equal-ripple reflection amplifier.

The fact that the above active response characteristics are reciprocal to Butterworth or Tchebycheff reflection characteristics, whose zeros are chosen to be in the left half s plane, guarantees the conditional stability of the active networks. The further requirement that the reflection be stable as the active element is turned on and brought to operating value imposes a restriction upon the maximum reflection coefficient, more severe in the lossless maximally flat case than in all other cases of corresponding ρ_0 and N. Table I shows critical values of ρ_0 for this case.

TABLE I
Critical Values of ρ_0 for Lossless Maximally Flat Reflection Response

N	ρ_0 critical
1	∞
2	∞
3	320
4	90
5	50

* Received by the IRE, March 14, 1960. This research is sponsored by the Office of Naval Research under Contract Nonr 220(13).

[1] E. W. Sard, "Tunnel diode amplifiers with unusually large bandwidth," Proc. IRE, vol. 48, pp. 357–358; March, 1960.

[2] H. Seidel and G. F. Herrman, "Circuit aspects of parametric amplifiers," 1959 IRE WESCON Convention Record, Pt. 2, pp. 83–90.

[3] H. Bode, "Network Analysis and Feedback Amplifier Design," D. Van Nostrand Co., Inc., New York, N. Y., pp. 365–367; 1945.

The maximally flat or equal ripple reflection response can always be obtained at the input terminals of the reflection amplifier, even in the presence of circuit loss. When the network consists of coupled cavities with quality factors Q_0 at the mid-band frequency ω_0, a bandwidth reduction factor

$$\left(1+2\,\frac{\omega_0}{Q_0}\,\frac{C_T}{G_T}N\right)^{-1} \tag{8}$$

corrects (4) and (7).

The reflection coefficient of a time varying capacitor $C_0(1+\eta\cos\omega_p t)$, used as a parametric amplifier, depends critically upon the circuit admittance presented to the active terminals at two frequencies, ω_s and $\omega_i=\omega_p-\omega_s$. This complication is removed when the circuit admittance is derived by equal double band-pass transformation from a low-pass function to be specified. The active reflection coefficient then takes the form

$$\rho_p=\frac{1}{2}\,\frac{Y_{(\omega)}+i\omega C_0+\frac{\eta}{2}\sqrt{\omega(\omega_p-\omega)}}{Y_{(\omega)}+i\omega C_0-\frac{\eta}{2}\sqrt{\omega(\omega_p-\omega)}}, \tag{9}$$

where $Y_{(\omega)}+i\omega C_0$ has nearly equal and symmetric characteristics about two band centers, ω_{s0} and ω_{i0}. For most cases of practical interest, the variation of $\sqrt{\omega_s(\omega_p-\omega_s)}$ is not the ultimate bandwidth limiting factor and may be neglected by writing $\sqrt{\omega_{s0}\omega_{i0}}$.

When $Y_{(\omega)}+i\omega C_0$ is derived by double band-pass transformation of Butterworth or Tchebycheff low-pass network, the parametric amplifier reflection response is related to (3) and (6) by the same transformation. The two equal bandwidths centered on ω_{s0} and ω_{i0} may be found from (4) and (7) by the substitutions

$$\frac{\eta}{4}\sqrt{\omega_{s0}\omega_{i0}}=\frac{G_T}{C_T}$$

and

$$\rho_{\text{parametric}}=\frac{1}{2}\,\rho_{\text{tunnel diode}}. \tag{10}$$

The ultimate gain bandwidth relation for a parametric amplifier is thus deduced.

$$(\ln 2\rho_p)\Delta\omega=\frac{\pi\eta}{4}\sqrt{\omega_{s0}\omega_{i0}}, \tag{11}$$

has a maximum when $\omega_{s0}=\omega_{i0}=\omega_p/2$.

$$(\ln 2\rho_p)\Delta\omega=\frac{\pi\eta}{8}\omega_p. \tag{12}$$

The final point to be expressed here is that the usual series inductance arising from the packaging of the two active devices considered becomes a part of the filter network, and does not affect bandwidth as long as the operating frequency is below the self-resonant frequency of the active element.

Continuing work on the circuit theory of negative resistance amplifiers will include studies of loss and noise performance and synthesis techniques for transmission amplifiers.

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Author's Comment[4]

Aron's article appears to summarize a valuable theoretical contribution on gain-bandwidth performance of N-pole negative-resistance amplifiers (when operated with an ideal circulator only). With regard to designing the filters for such amplifiers, however, I disagree with Aron when he says that existing tables are adequate.

It should be pointed out that similar work for the tunnel diode case, "Optimum Negative-Resistance Amplifiers" by D. C. Youla and L. I. Smilen, was presented at the Polytechnic Institute of Brooklyn's Symposium on Active Networks and Feedback Systems in April, and will be published in Volume X of their *Symposia Series*. Furthermore, in my paper presented at the same Symposium, "Gain-Bandwidth Performance of Maximally Flat Negative-Conductance Amplifiers," the correct gain-bandwidth expression for the maximally flat case [Aron's (4)] was deduced, although not as elegantly as by Aron.

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[4] Received by the IRE, May 26, 1960.

Determination of Probability Density Functions for Sums of Variables by Laplace Transformation*

Let $p_1(x)$ and $p_2(y)$ be, respectively, the probability density functions of two independent random variables x and y; and let $z=x+y$.

Then the probability density function $p_3(z)$ may be found[1] from the relation

$$p_3(z)=\int_{-\infty}^{\infty}p_1(x)p_2(z-x)dx. \tag{1}$$

Alternatively, the characteristic functions corresponding to x and y may be multiplied to find the characteristic function which corresponds to z; $p_3(z)$ is the inverse Fourier transform of this product.[1]

In this note, a method of determining $p_3(z)$ is derived which is analogous to the characteristic function method, but which involves Laplace transformation instead of Fourier transformation. The method is based upon use of (2a) and (2b):

$$p_3(z)=f(z+2a), \tag{2a}$$

$$f(z)=L^{-1}\{(L[p_1(x-a)])(L[p_2(y-a)])\}, \tag{2b}$$

where L and L^{-1} represent direct and inverse Laplace transformation, respectively, and where a is a non-negative real number so chosen that

$$p_1(x-a)=0,\ x<0 \tag{3a}$$

$$p_2(y-a)=0,\ y<0. \tag{3b}$$

The validity of these expressions depends upon the existence of the required Laplace transforms and of a finite value of a which satisfies (3a) and (3b). Provided that these conditions are satisfied, (2a) and (2b) may be derived as follows.

$$\text{Let } p_4(x)=p_1(x-a) \tag{4a}$$

$$p_5(y)=p_2(y-a) \tag{4b}$$

and let

$$f(z)=\int_{-\infty}^{\infty}p_4(\lambda)p_5(z-\lambda)d\lambda. \tag{5}$$

From (1),

$$p_3(z)=\int_{-\infty}^{\infty}p_1(\lambda)p_2(z-\lambda)d\lambda. \tag{6}$$

Also, from (5),

$$f(z)=\int_{-\infty}^{\infty}p_1(\lambda-a)p_2(z-\lambda-a)d\lambda;\ \text{or} \tag{7}$$

$$f(z)=\int_{-\infty}^{\infty}p_1(\lambda-a)p_2(z-2a-[\lambda-a])d(\lambda-a).$$

From (6) and (7),

$$p_3(z-2a)=f(z);\ \text{or}$$

$$p_3(z)=f(z+2a). \tag{2a}$$

Now, the integrand in the expression on the right-hand side of (5) vanishes except when $0\le\lambda\le z$, by virtue of (3a), (3b), (4a), and (4b). Hence, we may write

$$f(z)=\int_0^z p_4(\lambda)p_5(z-\lambda)d\lambda. \tag{8}$$

Then, by Borel's theorem,

$$L[f(z)]=(L[p_4(x)])(L[p_5(y)]); \tag{9}$$

or, finally,

$$f(z)=L^{-1}\{(L[p_1(x-a)])(L[p_2(y-a)])\}. \tag{2b}$$

The formal extension of the present method to determination of the probability density function for the sum of more than two variables is somewhat more unwieldy than is the case with the method of characteristic functions. The value of the method is confined to those cases in which the (direct and inverse) Laplace transforms involved are more easily obtained than are the corresponding Fourier transforms.

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* Received by the IRE, May 27, 1960.

[1] W. R. Bennett, "Methods of solving noise problems," PROC. IRE, vol. 44, pp. 609–638; May, 1956.

Applying the Chordal-Hop Theory of Ionospheric Long-Range Propagation to Echo-Signal Delay*

Regarding measurements of the time taken by a short-wave signal to complete a path around the earth, the literature contains accounts by various research workers. As a comprehensive study on the subject,

* Received by the IRE, June 30, 1960.

Hess used 218 measurements to obtain an average value of 0.13778 second[1-3] for one complete path. This value has been found to be, for the accuracy indicated, independent of frequency, relative magnetic field characteristics, and seasonal and diurnal variations of ionospheric characteristics. Assuming the velocity of light to equal 299,792 km/sec, the above value yields 41,308 km as the distance really travelled by the signal. Its ratio to the distance on the earth's surface amounts to 1.03271, defined as the "Path Factor."

As given by Hess,[3] the above-mentioned series of measurements results in delay values between 0.1376 and 0.1381 second, being equivalent to path factors between 1.0312 and 1.0354. According to Lassen,[4,5] measurements can be taken as representative between 0.1370 and 0.1384 second or path factors 1.027 and 1.037.

Furthermore, Humby, Minnis, and Hitchcock[6] discuss measurements of delays between signals arriving at London via short and long routes resulting in 61–63 msec and 76–78 msec for circuits London–Singapore and London–Colombo, respectively. These values yield path factors between 1.005 and 1.038 for the Singapore circuit, and between 1.013 and 1.039 for the other one.

Attempts to interpret these time-delay readings in terms of the orthodox propagation theory of multiple hops between ionospheric layers and the earth's surface led to theoretical path factors[5] of 1.032 and 1.043 for reflection heights of 200 and 300 km, respectively, at a take-off angle of six degrees.

Continuing his research work on long-distance propagation, the author analyzed such echo-signal delays with the aid of his chordal-hop theory and found an apparently much closer agreement between measurements mentioned and theoretical results according to this theory. In fact, with given ionospheric characteristics, path factors are between 1.0289 and 1.0347 for a take-off angle of six degrees. However, at a take-off angle of four degrees, and under the same ionospheric conditions, values agree almost precisely with those measured by Hess, viz., path factors are between 1.0302 and 1.0359. In a more general sense, it was found that chordal-hop propagation permits path factors between 1.021 and 1.039.

Postulated and proved in 1956 and 1957,[7,8] the chordal-hop theory requires that a *normal*, largely predominant mode of long-range propagation follows a path reflected by ionospheric layers without touching the earth's surface. As its name implies, the ray is supposed to be propagated along the ionosphere by chordal hops with minimum path heights varying from a few kilometers to a hundred and more, because of changes in ionospheric characteristics.

The author's work in this field has yielded very satisfactory results, particularly as far as new approaches to path-attenuation calculations[8,9] and comprehensive propagation analysis[10] are concerned. The successful use of the chordal-hop theory for echo-delay calculations, as described in this note, appears to present another general proof of this propagation concept.

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[1] H. A. Hess, "Untersuchungen an Kurzwellen-Echosignalen," *Z. Naturforschung*, vol. 1, pp. 499–505; September, 1946.
[2] H. A. Hess, "Das Kurzwellenecho," *Funk und Ton* (title changed to *Elektron Rundschau*), vol. 2, pp. 57–65; February, 1948.
[3] H. A. Hess, "Investigations of high-frequency echoes," PROC. IRE, vol. 40, pp. 1065–1068; September, 1952.
[4] H. Lassen, "Die Ausbreitung der Kurzwellen-Echosignale," *Funk und Ton* (title changed to *Elektron. Rundschau*), vol. 2, pp. 420–424; August, 1948.
[5] H. Lassen, in "Antennen und Ausbreitung," by K. Fraenz and H. Lassen, Springer-Verlag, Berlin, Germany, pt. I, p. 118; 1956.
[6] A. M. Humby, C. M. Minnis, and R. J. Hitchcock, "Performance characteristics of high-frequency radiotelegraph circuits," *Proc. IEE*, vol. 102, pt. B, pp. 513–522; July, 1955.
[7] H. J. Albrecht, "Analysis of world-wide ionospheric propagation to and from Australia, 1953–54," *J. Wireless Instr. Austr.*, vol. 24, pp. 2–5; October, 1956.
[8] H. J. Albrecht, "Investigations on great-circle propagation between Eastern Australia and Western Europe," *Geofis. pura e appl.*, vol. 38, pp. 169–180; 1957.
[9] H. J. Albrecht, "Further studies on the chordal-hop theory of ionospheric long-range propagation," *Arch. Meteorol. Geophys. u Bioklimatol.*, Ser. A, vol. 2, pp. 84–92; 1959.
[10] H. J. Albrecht, "Analysis of ionospheric paths in long-range propagation," *Indian J. Meteorol. Geophys.*, vol. 2, pp. 57–63; January, 1960.

Minimization of the Maximum Amplitude in Frequency Multiplexing*

This note deals with the problem of finding the sequence of phases $\phi_1, \cdots, \phi_N$ which minimize

$$\max_{0\le\theta\le1}\left|\sum_{k=1}^{N}\cos(2\pi k\theta+\phi_k)\right|.$$

The problem arises in a variety of contexts, *e.g.*, frequency multiplexing and speech synthesis.

It seems to be very difficult to find a formula for this minimum, or even an algorithm for computing it. However, a practical approximation can be obtained through a few simple manipulations together with certain results from the mathematical literature. We can do this by first proving a universal lower bound, *i.e.*, a lower bound independent of the choice of the phases $\phi_1, \cdots, \phi_N$, and then exhibiting two sequences of sums of the form

$$\sum_{k=1}^{N}\cos(2\pi k\theta+\phi_k)$$

such that

$$\max_{0\le\theta\le1}\left|\sum_{k=1}^{N}\cos(2\pi k\theta+\phi_k)\right|=O(N^{1/2}).$$

The lower bound is given by

$$\max_{0\le\theta\le1}\left|\sum_{k=1}^{N}\cos(2\pi k\theta+\phi_k)\right|\ge N^{1/2}, \quad (1)$$

independently of the choice of the ϕ_k's.

* Received by the IRE, June 27, 1960.

To prove (1), we first find a formula for

$$\int_0^1\left|\sum_{k=1}^{N}\cos(2\pi k\theta+\phi_k)\right|^2d\theta:$$

$$\int_0^1\left|\sum_{k=1}^{N}\cos(2\pi k\theta+\phi_k)\right|^2d\theta$$

$$=\int_0^1\left|\sum_{k=1}^{N}(\cos\phi_k\cos 2\pi k\theta-\sin\phi_k\sin 2\pi k\theta)\right|^2d\theta$$

$$=\sum_{k=1}^{N}(\cos^2\phi_k+\sin^2\phi_k)$$

$$=N. \quad (2)$$

Combining (2) with the following inequality yields (1):

$$\int_0^1\left|\sum_{k=1}^{N}\cos(2\pi k\theta+\phi_k)\right|^2d\theta$$

$$\le\max_{0\le\theta\le1}\left[\left|\sum_{k=1}^{N}\cos(2\pi k\theta+\phi_k)\right|^2\right]$$

$$\le\left[\max_{0\le\theta\le1}\left|\sum_{k=1}^{N}\cos(2\pi k\theta+\phi_k)\right|\right]^2. \quad (3)$$

Of the two sequences of sums which are bounded by a constant multiple of $N^{1/2}$, the first has a smaller constant in the bound but is probably more difficult to use for large values of N. To define the sequence, we consider the two sequences of polynomials determined by the following relations:

$$P_0(x)=Q_0(x)=x, \quad (4)$$

$$P_{r+1}(x)=P_r(x)+x^{2^r}Q_r(x), \quad (5)$$

$$Q_{r+1}(x)=P_r(x)-x^{2^r}Q_r(x). \quad (6)$$

It can be seen that: 1) $\deg(P_r(x))=2^r$, 2) $P_r(x)$ is precisely the first 2^r terms of $P_{r+1}(x)$, 3) each coefficient of $P_r(x)$ is 1 or -1, except for the constant term, which is zero. Thus, $\{\epsilon_k\}_{k=1}^{\infty}$ is a well-determined sequence of 1's and -1's if we define ϵ_k to be the coefficient of x^k in $P_r(x)$ whenever $2^r\ge k$, *i.e.*, the definition of the ϵ_k's requires the subsequent relation to hold

$$P_r(x)=\sum_{k=1}^{2^r}\epsilon_kx^k. \quad (7)$$

From this definition, it can be shown[1] that for all $N\ge1$ we have

$$\left|\sum_{k=1}^{N}\epsilon_ke^{ik\theta}\right|<5N^{1/2}. \quad (8)$$

Since $\epsilon_k=e^{i(1-\epsilon_k)\pi/2}$, (8) clearly implies that we have

$$\max_{0\le\theta\le1}\left|\sum_{k=1}^{N}\cos\left[2\pi k\theta+(1-\epsilon_k)\frac{\pi}{2}\right]\right|<5N^{1/2}. \quad (9)$$

In view of the lower bound (3), the inequality (9) shows that the sums of the form

$$\sum_{k=1}^{N}\cos\left[2\pi k\theta+(1-\epsilon^k)\frac{\pi}{2}\right]$$

[1] For proof of the estimate, see W. Rudin, "Some theorems on Fourier coefficients," *Proc. Amer. Math. Soc.*, vol. 10, pp. 855–859; March, 1959.

have a behavior which is a useful approximation to the desired minimum-maximum behavior.

The second sequence of sums is probably more useful in the case of large N than the one just considered. The generic sum is

$$\sum_{k=1}^{N} \cos (2\pi k\theta + k \log k),$$

and we have, for all $N \geq 1$,

$$\max_{0\leq\theta\leq 1} \left| \sum_{k=1}^{N} \cos (2\pi k\theta + k \log k) \right| < 50\, N^{1/2}, \quad (10)$$

which is a simple consequence of an inequality deduced by Hardy and Littlewood.[2]

Graphs of the sums

$$\sum_{k=1}^{5} \cos (2\pi k\theta + k \log k) \text{ and } \sum_{k=1}^{5} \epsilon_k \cos 2\pi k\theta$$

$$(= \cos 2\pi\theta + \cos 4\pi\theta + \cos 6\pi\theta - \cos 8\pi\theta + \cos 10\pi\theta)$$

are given in Figs. 1 and 2, respectively. It

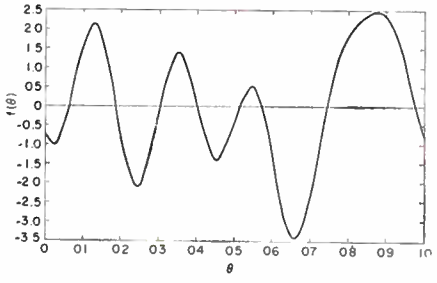

Fig. 1—Graph of $\sum_{k=1}^{5} \cos (2\pi k\theta + k \log k)$.

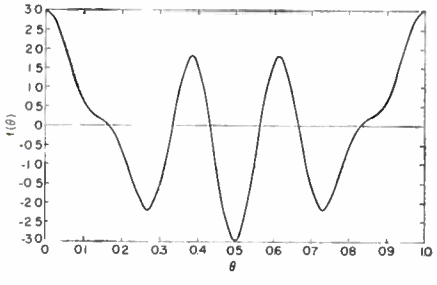

Fig. 2—Graph of $\cos 2\pi\theta + \cos 4\pi\theta + \cos 6\pi\theta - \cos 8\pi\theta + \cos 10\pi\theta$.

should be noticed that their maximum absolute values are 3.4 and 3.0, in that order. Since $3.4 \approx 1.5\sqrt{5}$ and $3.0 \approx 1.4\sqrt{5}$, it appears that the two sequences of sums considered are much better behaved and more useful for small values of N than the estimates (9) and (10) might lead us to believe.

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[2] A. Zygmund, "Trigonometrical Series," Chelsea Publishing Co., New York, N. Y.; 1952; see Theorem 5.32 on p. 118.

The Equivalence of the Taylor-Cauchy and Laurent-Cauchy Transform Analysis with Conventional Methods*

Ku, *et al.*,[1] have described a new transform calculus applicable to a class of nonlinear differential equations. It will be shown that this transform method is identical to well-known elementary techniques for solving differential equations.

Consider their example 1 (in Sec. VII), where the differential equation

$$\frac{df}{dt} + f^2 = 1 \quad (1)$$

is to be solved for $t>0$, with the condition that

$$f(0) = 0. \quad (2)$$

The solution is assumed to be of the form

$$f(t) = a_0 + \frac{a_1}{1!} t + \frac{a_2}{2!} t^2 + \cdots + \frac{a_n}{n!} t^n + \cdots. \quad (3)$$

The coefficients $a_0, a_1, \cdots$, can be determined by substituting (3) into (1), expanding the right-hand side of (1) into a Taylor series, and equating coefficients of similar powers in t. The same result can be obtained by differentiating (1) successively with respect to t. This gives

$$\begin{aligned}
f^{(1)} &= 1 - f^2 \\
f^{(2)} &= -2ff^{(1)} \\
f^{(3)} &= -2(f^{(1)})^2 - 2ff^{(2)} \\
f^{(4)} &= -6f^{(1)}f^{(2)} - 2ff^{(3)} \\
f^{(5)} &= -6(f^{(2)})^2 - 8f^{(1)}f^{(3)} - 2ff^{(4)} \\
f^{(6)} &= -20f^{(2)}f^{(3)} - 10f^{(1)}f^{(4)} - 2ff^{(5)} \\
f^{(7)} &= -20(f^{(3)})^2 - 30f^{(2)}f^{(4)} - 12f^{(1)}f^{(5)} - 2ff^{(6)} \\
&\cdots\cdots\cdots\cdots\cdots\cdots, \quad (4)
\end{aligned}$$

where

$$f^{(n)} = \frac{d^n f(t)}{dt^n}.$$

Substituting $t=0$ into (4) gives, since $a_n = f^{(n)}(0)$,

$$\begin{aligned}
a_1 &= -a_0^2 \\
a_2 &= -2a_0a_1 \\
a_3 &= -2a_1^2 - 2a_0a_2 \\
a_4 &= -6a_1a_2 - 2a_0a_3 \\
a_5 &= 6a_2 - 8a_1a_3 - 2a_0a_4 \\
a_6 &= -20a_2a_3 - 10a_1a_4 \\
a_7 &= -20a_3^2 - 30a_2a_4 - 12a_1a_5 - 2a_0a_6 \\
&\cdots\cdots\cdots\cdots\cdots\cdots. \quad (5)
\end{aligned}$$

Since $a_0=0$, (5) can be solved recursively for the a_n's; the result is

$$\begin{aligned}
a_1 &= 1 \qquad a_4 = 0 \qquad a_7 = -1\cdot(16)\cdot(17) \\
a_2 &= 0 \qquad a_5 = 16 \qquad \cdots\cdots\cdots. \quad (6) \\
a_3 &= -2 \qquad a_6 = 0
\end{aligned}$$

Hence,

$$f(t) = t - \frac{1}{3}t^3 + \frac{2}{15}t^5 - \frac{17}{315}t + \cdots = \tanh t. \quad (7)$$

Consider now their example 2. The problem is to solve the differential equation

$$\frac{d^2f}{dt^2} + (2+f)\frac{df}{dt} + f = -e^{-2t}, \quad (8)$$

subject to the condition

$$\begin{aligned}
f(0) &= a_0 = -1 \\
f^{(1)}(0) &= a_1 = +1. \quad (9)
\end{aligned}$$

Eq. (8) can be differentiated successively with respect to t. This gives

$$\begin{aligned}
f^{(2)} &= -2f^{(1)} - f - ff^{(1)} - e^{-2t} \\
f^{(3)} &= -2f^{(2)} - f^{(1)} - (f^{(1)})^2 - ff^{(2)} + 2e^{-2t} \\
f^{(4)} &= -2f^{(3)} - f^{(2)} - 3f^{(1)}f^{(2)} - ff^{(3)} - 4e^{-2t} \\
&\cdots\cdots\cdots\cdots\cdots\cdots. \quad (10)
\end{aligned}$$

Substituting $t=0$ into (10) gives

$$\begin{aligned}
a_2 &= -2a_1 - a_0 - a_0a_1 - 1 \\
a_3 &= -2a_2 - a_1 - a_1^2 - a_0a_2 + 2 \\
a_4 &= -2a_3 - a_2 - 3a_1a_2 - a_0a_3 - 4. \\
&\cdots\cdots\cdots\cdots\cdots\cdots. \quad (11)
\end{aligned}$$

These equations can be solved recursively for the a_n's. The result is

$$\begin{aligned}
a_0 &= -1 \qquad a_3 = +1 \\
a_1 &= +1 \qquad a_4 = -1 \\
a_2 &= -1 \qquad \cdots\cdots. \quad (12)
\end{aligned}$$

Hence,

$$f(t) = -1 + \frac{t}{1!} - \frac{t^2}{2!} + \frac{t^3}{3!} - \frac{t^4}{4!} + - \cdots = -e^{-t}. \quad (13)$$

This method of solving a differential equation is described by Ince,[2] who considers the method to be, in general, impractical. A closer examination will now reveal that this method is identical to the Cauchy-Taylor transform method. This can be readily seen from (3), which is the Taylor series for $f(t)$. Since t is a mathematical independent variable and need not be restricted to representing time, it can take on complex values. Then a_n can be obtained from the well-known formula

$$\frac{1}{n!} a_n = \frac{1}{2\pi j} \oint_{t=0} \frac{f(t)}{t^{n+1}}\, dt. \quad (14)$$

Using their terminology, (14) represents the Cauchy-Taylor transform of $f(t)$, and (3) the inverse transform. The algebraic equations obtained from the differential equation by this transform are none other than the equations of type (5) and (11). These are obtained by substituting the power series (3) into the differential equation, expanding the right-hand side into a power series, and equating the coefficients of similar powers of t. The symbolism and terminology used completely obscures the elementary and well-known method that is actually being used.

* Received by the IRE, May 24, 1960.

[1] Y. H. Ku, A. A. Wolf and S. H. Dietz, "Taylor-Cauchy transforms for analysis of a class of nonlinear systems," Proc. IRE, vol. 48, pp. 912–922; May, 1960.

[2] E. L. Ince, "Ordinary Differential Equations," Dover Publications, Inc., New York, N. Y., p. 540; first American Edition.

In a companion paper, Ku and Wolf[3] describe the Laurent-Cauchy transform. It will be shown now that this is identical to the z transform.

In its application to physical systems, the z transform can be defined by the Laurent series

$$H(Z) = \sum_{n=0}^{\infty} a_n z^{-n}, \tag{15}$$

where the a_n represents the nth sample of a time function $h(t)$. In the application to solving difference equations it is unnecessary to restrict a_n in this manner. The a_n's may be any sequence of complex numbers, provided that they do not depend upon Z, and that $H(Z)$ is analytic within a suitable domain.

In solving difference equations by this method, the difference equations are first written in terms of suitably defined a_n's. Using z-transform methods, a function $H(Z)$ is determined from which the a_n's can then be found.[4]

Consider their example 1 again. The problem is to solve the equation

$$\frac{dy_{n+1}}{dt} + \frac{a}{n+1} y_n = 0 \quad (n = 0, 1, \cdots) \tag{16}$$

with the condition

$$y_n(0) = \frac{1}{n!}. \tag{17}$$

Following Ku, the Laplace transform of (16) is first taken. This gives

$$(n+1)SY_{n+1} + aY_n = \frac{1}{n!}. \tag{18}$$

If (18) is to be solved by the z-transform method, a generating function $H(Z)$ must be found where

$$H(Z) = \sum_{n=0}^{\infty} Y_n Z^{-n}, \tag{19}$$

and the Y_n's satisfy (18).

To find $H(Z)$, consider first the function

$$F(Z) = \sum_{n=0}^{\infty} (n+1) Y_{n+1} Z^{-n}. \tag{20}$$

From (19) and (20) it is an easy matter to show that

$$F(Z) = -Z^2 \frac{dH}{dZ}. \tag{21}$$

Using the expansion

$$e^{z^{-1}} = \sum_{n=0}^{\infty} \frac{z^{-n}}{n!}, \tag{22}$$

and combining (19)–(22), it is easy to show that (18) is equivalent to

$$-SZ^2 \frac{dH}{dZ} + aH = e^{z^{-1}}. \tag{23}$$

Solving (23) for H gives

$$H = \frac{e^{z^{-1}}}{s+a}. \tag{24}$$

[3] Y. H. Ku and A. A. Wolf, "Laurent-Cauchy transforms for analysis of linear systems described by differential-difference and sum equations," PROC. IRE, vol. 48, pp. 923–931; May, 1960.

[4] D. Cheng, "Analysis of Linear Systems," Addison-Wesley Publishing Co., Inc., Reading, Mass., pp. 313–320; 1959.

Using (22), and comparing it with (19), shows that

$$Y_n = \frac{1}{n!} \frac{1}{(s+a)}. \tag{25}$$

The inverse Laplace transform of (25) gives the final solution

$$y_n = \frac{1}{n!} e^{-at}. \tag{26}$$

Comparing this with their method shows the methods are identical. To see this, consider (19), from which it is easy to obtain

$$Y_n = \frac{1}{2\pi j} \oint H(Z) Z^{n-1} dZ_{z=0}. \tag{27}$$

In their terminology, Y_n is the inverse Laurent-Cauchy transform of $H(Z)$. In the conclusion of their paper it is mentioned that the Laurent-Cauchy transform is identical to the z transform only if the a_n's in (15) are the samples of a time function. The results here clearly show that the methods are completely identical. Merely replacing the symbol $a_n(t)$ by $Y_n(S)$ cannot possibly justify renaming the z transform, and calling it the Laurent-Cauchy transform.

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Author's Comment[5]

The undersigned appreciates the opportunity to reply to the points raised in Mr. Bohn's communication.

From his remarks, it is apparent that he has failed to grasp both the obvious and subtle essentials and differences between the transforms presented in our papers [1],[1] and other methods of analysis [2]–[18], and the resulting significance to the general theory of nonlinear systems [19]–[27]. He presents two points in his letter that appear to be unrelated to one another. We shall consider these separately and show clearly that the conclusions drawn by him about our transforms, on the basis of his examples, are incorrect.

First, consider Bohn's assertion concerning the identity of the Taylor-Cauchy transform, and "well-known" methods of elementary analysis. He builds his argument on two examples and an integral given in his (14). He offers no other rigorous or even a systematic proof of his claim, but he nevertheless concludes that the Taylor-Cauchy transform is identical to an elementary technique in differential equation analysis on the basis that the two methods give the same result. The technique used by him is an elementary aspect of the Fuchsian [10] theory of *linear* differential equations. The method of analysis was first developed systematically by Frobenius [10], [11] in a classic paper published in 1874. The method was rigorously proven only for a class of linear differential equations. Fuchs [12] showed that the method was not applicable, in general, to all linear differential equations. In particular, it failed, under certain conditions, whenever the coefficients in the differential equations were time variant and contained singular points. Occasionally, series solutions could be found by this method, despite the presence of these singularities. The issue as to what singular points were admissible was settled in an important theorem by Fuchs [2], [10], [12].

The question as to whether Frobenius's method could be applied to nonlinear systems in general was not solved by Frobenius, since he found, with the exception of a special class of problems, that the coefficients of the assumed solution were related in a "backward" recurrence relation (among other things). This means that in order to obtain a given coefficient it is necessary to know at least one coefficient which has not yet been determined. Since the higher-order coefficients, in these cases, are found under the convolution sign, it is impossible to reverse this procedure to obtain a forward recurrence relation as it is in the linear case. Another difficulty that arises concerns convergence of the solution and proper generation of the coefficients. It is difficult by this theory to decide what kinds of problems will yield proper and well-behaved recurrence relations. Other difficulties occur when the linear part is time-varying. Consider, for example, the nonlinear integro-differential equation given in (1)

$$Z(D)x(t) + F(x) = g(t), \tag{1}$$

where

$$Z(D) = \sum_{n=N_1}^{N_2} f_n D^n; \quad D^n = d^n/dt^n \tag{2}$$

and

$$F(x) = \sum_{k=0}^{N} a_k x^k. \tag{3}$$

Suppose we use Bohn's method to develop a series solution such as

$$x(t) = \sum_{n=0}^{\infty} h_n t^n. \tag{4}$$

We obtain the recurrence relation (5) as

$$\sum_{m=N_1}^{N_2} f_m h_{n+m} \binom{n+m}{n} n! + \sum_{k=0}^{N} a_k h_n^{(k)} = b_n, \tag{5}$$

where

$$\binom{n+m}{n} = \frac{(n+m!)}{n!\,m!}$$

denote the binomial coefficients, $h_n^{(k)}$ are multifold convolution sums given in [19]–[21], and b_n denote the Taylor coefficients of $g(t)$.

Now (1) is an integro-differential equation so that $N_1 < 0$ (negative). It is then obvious that we have a "backward" recurrence relation. Hence, we are in difficulty, as discussed above. It is easy to compound these difficulties by adding time-varying terms. If repeated differentiation is resorted to, the difficulty may be transferred to the nonlinear part.

Now let us return to the Taylor-Cauchy transform. As stated,[1] this transform arises from the partition theory [19]–[27] whenever the partition is made at the highest linear derivative. We note for contrast that Fro-

[5] Received by the IRE, July 11, 1960.

benius's method is equivalent to a partition at the zeroth-order linear derivative, *i.e.*, the dependent variable. This is, therefore, equivalent to requiring the modified forcing function [19], [20] to equal the response function $x(t)$, a condition which mathematically may not always be possible to achieve. Wolf showed [23] that if the partition is made at some other point, a general transform pair could be generated from the integral sum equations given in (6) and (7),

$$x(\lambda) = \sum_{n=0}^{\infty} C_n Q_n(\lambda) \tag{6}$$

$$C_n = \frac{1}{2\pi j}\int_c x(\lambda)Q_n(\lambda)d\lambda, \tag{7}$$

with certain precautions assumed [19], [20], [23],[1] and where $Q_n(\lambda)$ are the moments of the linear partitioned part in the open interval $(0, \lambda)$, and where n is the order of the moment, and λ denotes a complex variable which is the analytic continuation into a plane of the real variable t along the infinite half line.

Concept of the Partition Theory

The partition theory of nonlinear systems was developed to cope with the difficulties engendered by the Frobenius method, and to develop rigorously a framework to analyze systematically a class of nonlinear systems under certain specified conditions. In [19] and [20], Wolf showed a rigorous mathematical justification for partitioning (1) into

$$Z(D)x(t) = A(t) \tag{8}$$

$$A(t) = g(t) - F(x), \tag{9}$$

where $A(t)$ denotes the modified forcing or auxiliary function, and

$$F(x) = F(x, \dot{x}, \ddot{x}, \cdots). \tag{10}$$

Since (1) can be pictured as a feedback system [19], [20], [23] with a forcing function $g(t)$, a response $x(t)$, a linear forward part and a nonlinear feedback part, it is at once clear that $A(t)$ physically represents the error function. From the partition theory, one can very rigorously deduce the properties of $A(t)$. Thus, the problem of solving (1) is reduced to the solution of (8), which is a linear problem wherever $A(t)$ is deducible. We note, in contradistinction to the method of Frobenius, that no assumptions are directly made concerning the solution expansion; only the modified forcing function is expanded according to certain rules.

From the partition theory, the general solution to (1) is immediately obtainable from the moment theorem [19], [20], [23].

The Moment Theorem: Under certain specified but broad conditions required of the linear, nonlinear and driving functions, the solution of (1) *is the linear combination of all the moments of the folded impulse response of the linear partitioned part* [19], [20].

Since the partitioning procedure allows some or all the linear terms, with the exception of the highest-order derivative, to be transferred to the right member along with the nonlinear terms, the moments will change as a function of the partition selection. This method gives a range of forms to the solution depending upon the number of terms contained in the linear part and, therefore, allows one to select, *a priori*, the form of the solution, to a limited extent. By the uniqueness property of the solution, the several forms, although different, are nevertheless identically equivalent. It may be possible, therefore, to pick the form which most typifies the physical behavior of the system. For example, in an oscillatory system one might want to display the fundamental mode and its possible harmonics.

As discussed in [23], the partition at the highest derivative leads to a power function moment. If the highest-order derivative, *e.g.*, the kth and the $(k-1)$th remain in the partition, the moment function will be an entire nonperiodic function. Continuing in this way one can display both periodic and nonperiodic forms. This is not immediately possible with the method of Frobenius whenever it applies. As a result of these observations, Bohn's contention that the method we presented is identical to the method of analysis he presented, is obviously erroneous. The observations referred to here are proven in [19]–[27].

We now take up the question of obscurity in notation, claimed by Bohn. We dismiss this point by pointing out that the notation used in the partition method, and hence in the Taylor-Cauchy transform, is well established in the literature. We cite as reference Knopp [15], Sylvester [16], and Feller [28], with slight modiffications discussed and adequately explained in [19]–[21].

Comments on the Laurent-Cauchy Transform

We now consider Bohn's second point. Apparently he also missed this point. The transform deals with *sample* functions, while the Laurent-Cauchy transform deals principally with *sequence* functions. The two are different. Let us define them for comparison.

Definitions:

1) *Sample Function* is a collection of discrete points arranged so as to coincide with the corresponding range points of a continuous function having the same domain values and otherwise zero outside these domain values.
2) *Sequence Function* is a collection of continuous functions each different from the other, but having the same domain of definition.

An example of a sequence function $x_0(t), x_1(t), x_2(t), \cdots$ might be

$$x_0(t) = 1 \tag{11}$$

$$x_1(t) = \cos t \tag{12}$$

$$x_2(t) = \cos^2 t \tag{13}$$

$$\cdots\cdots$$

$$x_n(t) = \cos^n t$$

$$\cdots\cdots$$

Evidently this is quite different from the sampled cosine function, namely,

$$x(nt) = \cos nt, \tag{14}$$

where

$$x(nt)\begin{cases} \neq 0; & \text{when } n = 0, 1, 2, \cdots \\ = 0; & \text{otherwise.} \end{cases} \tag{15}$$

In the special case when the discrete variable, n, is related in some fashion to the time variable, t, then, with due precaution, one can view the resulting sequence function as a sample function if in the degenerate case all sequence functions reduce to one function. Hence, the sample function, for this condition, is a subset of the sequence functions. The sample functions, moreover, are a degenerate case of the mutilated functions [29].

Without considering this matter further, it is clear that Bohn is incorrect in his claim that the Laurent-Cauchy transform is identical with the z transform. They are generally different.

Conclusions and Comments

Bohn has given some examples showing that for the particular problems he selected, the Taylor-Cauchy transforms and Laurent-Cauchy transforms give the same results as other methods. This is not surprising. There are many ways of solving problems. What is surprising, however, is that he concludes from this that the methods are identical. By the same token, if one accepts Bohn's argument, the Laplace and Fourier transforms are identical. Similarly, one might also say that the Laplace transform is a trivial disguise of the method of assuming an exponential solution in solving linear differential equations with constant coefficients.

Finally, let us remark that the partition theory, and specifically the Taylor-Cauchy transform, afford one a systematic method of solving a broad class of nonlinear systems. As regards practicality, Dietz [27] developed a useful approximation to the partition theory enabling one to solve very difficult nonlinear problems with a given degree of accuracy and with moderate labor. As stated in [23], there are multitudes of methods in the literature for solving nonlinear problems; each has its realm of particular usefulness. The methods cited here are principally useful for theoretical and systematic studies, and are easily adapted for the case of stochastic inputs [25], [26]. The approximate method of Dietz also makes them very practical.

Appendix

An Example of the "Partition Method"[6]

Given:

$$c'' + k_1c' + k_2c + N(c', c) = r.$$

Three possible ways of partitioning:

$$c'' + k_1c' + k_2c = r - N(c', c) = e_1$$

$$c'' + k_1c' = r - k_2c - N(c', c) = e_2$$

$$c'' = r - k_1c' - k_2c - N(c', c) = e_3.$$

The solution of c is unique no matter which equation is used.

A simple example:

$$c' + c + c^2 = r = u(t) + \tanh t \tag{1}$$

$$c' + c = r - c^2 = u(t) + \tanh t - c^2 = e. \tag{2}$$

[6] Y. H. Ku, to appear in IRE Transactions on Circuit Theory.

Assume that

$$e(t) = \sum_{n=0}^{\infty} a_n t^n. \tag{3}$$

Taking the Laplace transform gives

$$E(s) = \sum_{n=0}^{\infty} a_n \frac{n!}{s^{n+1}}. \tag{4}$$

Taking the Laplace transform of (2) gives, for $c(0+)=0$,

$$(s+1)C(s) = E(s). \tag{5}$$

Substituting (4) in (5) gives

$$C(s) = \sum_{n=0}^{\infty} a_n \frac{n!}{(s+1)s^{n+1}}. \tag{6}$$

Taking the inverse transform of (6) gives

$$c(t) = \sum_{n=0}^{\infty} a_n q_n(t) \qquad t \geqq 0, \tag{7}$$

where $q_n(t)$ is the inverse transform of $n^k/(s+1)s^{n+1}$. For

$$n = 0,\ q_0(t) = 1 - e^{-t}.$$

$$n = 1,\ q_1(t) = t - q_0(t).$$

$$n = k,\ (k > 1),\ q_k(t) = t^k - kq_{k-1}(t).$$

Substituting $e(t)$ from (3) and $c(t)$ and its derivative from (7) into (2), expanding the exponentials in series and equating coefficients for the same power of t give a_n, for $n = 0, 1, 2, \cdots$.

Thus,

$$e(t) = 1 + t - t^2 - \frac{t^3}{3} + \frac{2}{3}t^4 + \frac{2}{15}t^5 - \frac{17}{45}t^6 - \frac{17}{315}t^7 + \frac{62}{315}t^8 + \frac{62}{2835}t^9 - \cdots + (0t) \tag{8}$$

$$c(t) = t - \frac{1}{3}t^3 + \frac{2}{15}t^5 - \frac{17}{315}t^7 + \frac{62}{2835}t^9 - \cdots = \tanh t \quad (t \geqq 0). \tag{9}$$

If we rewrite (2) as

$$c' = e - c = e_1, \tag{10}$$

we get

$$e_1(t) = 1 - t^2 + \frac{2}{3}t^4 - \frac{17}{45}t^6 + \frac{62}{315}t^8 - \cdots = \operatorname{sech}^2 t \quad (t \geqq 0). \tag{11}$$

Integrating and noting $c(0+)=0$ gives

$$c(t) = \tanh t \quad (t \geqq 0). \tag{12}$$

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Rotating Polarization and Periodic Bodies*

In a recent letter,[1] P. J. Allen described a method of generating a rotating polarization, and as a corollary, the measurement of the rotating polarization of a received wave. Since he speaks of a transmitted plane wave, all the rotations are in a plane normal to the direction of propagation. However, by placing the concepts on a firm mathematical basis, a matrix transformation of polarization, the previous effect and more interesting effects of scattering from "periodic" bodies are placed in evidence. The matrix concept was introduced in a series of reports,[2] and employed by the author in the study of scattering from tumbling objects.[3]

Since polarization describes the state of a vector in a plane, it is characterized by two basis vectors. Generally, these are taken to be orthogonally linear, and the vector $\boldsymbol{h}$ is given as $\{h_x, h_y\}$ (also a column matrix); an equally suitable description is in terms of a circular basis, right and left hand circular, $\{h_R, h_L\}$. The components of the vector are complex, having a magnitude and phase, and any polarization may be described in any basis. For example, in the linear basis right circular polarization is given as

$$\left\{\frac{1}{\sqrt{2}}, \frac{e^{j(\pi/2)}}{\sqrt{2}}\right\}.$$

Since the power in the wave is not dependent upon the manner of description, a transformation from one basis to another is accomplished by some unitary transformation. For example, the transformation from an orthogonal linear basis to a circular basis is given by

$$\begin{pmatrix} h_R \\ h_L \end{pmatrix} = \frac{1}{\sqrt{2}}\begin{pmatrix} 1 & e^{j(\pi/2)} \\ 1 & e^{-j(\pi/2)} \end{pmatrix}\begin{pmatrix} h_x \\ h_y \end{pmatrix}.$$

Similarly, it can be shown that a rotation of the coordinate system, or a rotation of the polarization vector in a fixed coordinate system, is given by the standard matrix transformation.

$$\begin{pmatrix} h_{x'} \\ h_{y'} \end{pmatrix} = \begin{pmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{pmatrix}\begin{pmatrix} h_x \\ h_y \end{pmatrix},$$

or in a circular basis

$$\begin{pmatrix} h_{R'} \\ h_{L'} \end{pmatrix} = \begin{pmatrix} e^{-j\theta} & 0 \\ 0 & e^{j\theta} \end{pmatrix}\begin{pmatrix} h_R \\ h_L \end{pmatrix}.$$

From this statement it is apparent that a continuous rotation about the line of sight, $\theta = 2\pi f_r t$, results in a frequency shift in opposite directions on the frequency scale for the two circular components, or vice versa.

Thus, in a more rigorous manner, the results on the generation and measurement of a rotating polarization are displayed. However, a more interesting result is obtained when this is extended to the scattering statement

$$\boldsymbol{h}^s = \boldsymbol{A}\boldsymbol{h}^t,$$

where

$\boldsymbol{h}^s$ is the scattered plane wave vector,
$\boldsymbol{h}^t$ is the transmitted plane wave vector, and
$\boldsymbol{A}$ is the scattering (Jones) matrix.

Furthermore, the scattering body is termed periodic if

$$\boldsymbol{A} = \boldsymbol{A}(t) = \boldsymbol{A}(t + m\tau)(m = 1, 2, \cdots).$$

It is to be noted that periodicity does not imply simply rotation in a plane normal to

* Received by the IRE, June 28, 1960.
[1] P. J. Allen, "Generating a rotating polarization," Proc. IRE, vol. 48, p. 941; May, 1960.
[2] Quar. Prog. Repts. Nos. 389-4, -12, -13, Antenna Lab., The Ohio State University Research Foundation, Columbus, Ohio, 1950–1952.
[3] Group Rept. 47.38, M.I.T. Lincoln Lab., Lexington, Mass.; March, 1960.

the line of sight. Also, it excludes rotation about any axis of revolution of a body. Note that periodicity is not a meaningless postulate. $\boldsymbol{A}$ depends upon the space orientation of the body, and if a body in space, free from all torques, has its spin axis and symmetry axis misaligned, a motion will result that is periodic.

It can be proven that $\boldsymbol{A}(t)$ may be expanded in the matrix series

$$\boldsymbol{A}(t) = \sum_{\nu=-\infty}^{\infty} {}_{c}\boldsymbol{E}_{\tau}^{\nu}(t)\boldsymbol{A}_{\nu},$$

where

$$\boldsymbol{A}_{\nu} = \frac{1}{\tau}\int_{0}^{\tau} {}_{c}\boldsymbol{E}_{\tau}^{-\nu}(t)\boldsymbol{A}(t)dt;$$

and in a circular basis

$${}_{c}\boldsymbol{E}_{\tau}^{\nu}(t) = \begin{pmatrix} e^{-i\nu(2\pi/\tau)t} & 0 \\ 0 & e^{i\nu(2\pi/\tau)t} \end{pmatrix}.$$

Thus, in the scattering statement

$$\boldsymbol{h}^{s} = \boldsymbol{A}(t)\boldsymbol{h}^{i} = \sum_{\nu=-\infty}^{\infty} {}_{c}\boldsymbol{E}_{\tau}^{\nu}(t)\boldsymbol{A}_{\nu}\boldsymbol{h}^{i}.$$

Since $\boldsymbol{A}_{\nu}\boldsymbol{h}' = \boldsymbol{h}'$ some unknown polarization, but expressed in a circular basis, it is evident that periodic bodies produce a line spectrum in each of the polarization components which is related to its period. In particular, simple periodic motions will be described by the positive index in the summation, and hence, the spectrum will be one-sided and in the opposite sense on the frequency scale, for each of the two components of circular polarization basis.

This method may prove useful in the analysis of one aspect of the motion of bodies remote from the observer. The effect to be expected is not affected by normal Doppler nor by Faraday rotations.

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On Phase Distortion in a Ferrimagnetic Limiter*

Siegman[1] has suggested that limiters employing parametric methods of energy conversion should be phase distortionless. Other authors[2–4] have reported on the phase characteristics of diode parametric limiters. The results of data taken on the analogous ferrimagnetic limiter in X band are reported here. The limiter, built in waveguide, employs a garnet slab biased to the region of subsidiary resonance as the nonlinear medium.

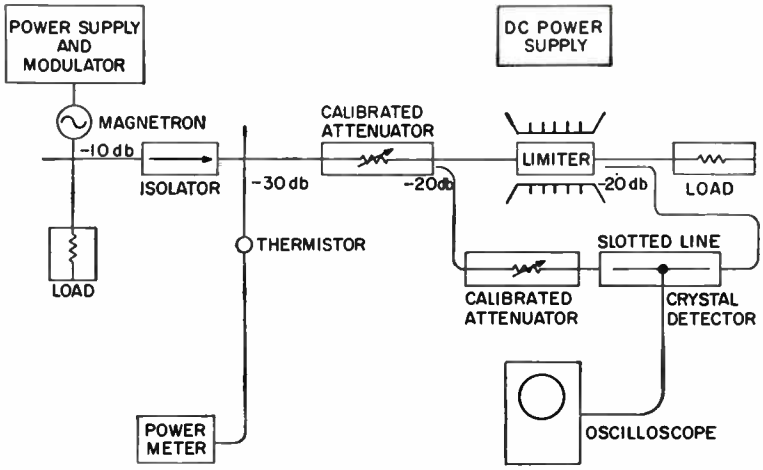

Fig. 1—Experimental arrangement.

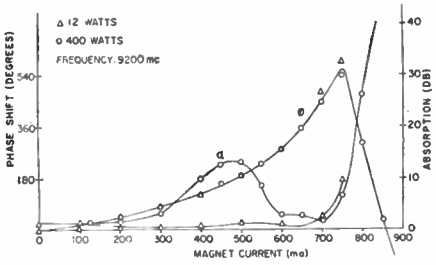

Fig. 2—Phase shift and absorption in the limiter at two power levels.

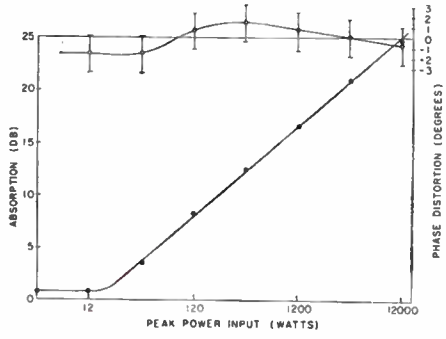

Fig. 3—Phase shift and absorption as a function of input power with the dc magnetic field held constant in the subsidiary resonance.

The experimental arrangement is depicted in Fig. 1. By matching the attenuation in the limiter with attenuation from the calibrated attenuator, a very sharp and deep null can be found on the slotted line section every half wavelength. Any change in phase shift through the limiter is reflected in a shift of the null position, and from the usual guide wavelength relationships the null shift is converted into phase shift.

Data presented in Fig. 2 show the phase shift and absorption in the limiter as a function of magnet current. The absorption peak at a magnet current of 450 ma represents the field (1700 gauss) required for subsidiary resonance, and approximately 900 ma would correspond to the field (3300 gauss) required for main resonance. The data are presented at two power levels. One level at 12 watts is below the limiting threshold, and the other at 400 watts is above the threshold. The difference in absorption between the two power levels in the region of the subsidiary resonance is evident. The data also show that in the same region the phase shift is substantially the same at the two power levels. Data in Fig. 3, which show the phase shift and absorption as a function of input power with the dc magnetic field held constant in the subsidiary resonance, illustrate well that within the limits of the accuracy of the measurements the phase shift through the limiter is constant over a 30-db range of input power.

The data were repeatable to within about three-fourths of a degree for a given depth of penetration of the probe on the slotted line. The smaller penetrations indicated slightly less phase distortion, but due to the reduced amplitude of the detected signal, the noise blanked out the center of the null on the slotted line and reduced the accuracy of the determination of the exact center of the null. An additional source of error was the possible phase distortion in the calibrated attenuator adjacent to the slotted line. The manufacturer states that phase distortion will be less than one degree in the attenuation range of our interest. Then the over-all accuracy of the measurements was calculated to be within 1.8°.

It is interesting to note from Fig. 2 that there should be little or no phase distortion in phase shifters due to high peak power alone.

The author wishes to thank Dr. G. R. Harrison for his helpful discussion of error probability.

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* Received by the IRE, July 8, 1960.

[1] A. E. Siegman, "Phase-distortionless limiting by a parametric method," Proc. IRE, vol. 47, pp. 447–448; March, 1959.

[2] A. A. Wolf, and J. E. Pippin, "A passive parametric limiter," *1960 Internat. Solid State Circuits Conf. Digest of Technical Papers*, pp. 90–91; February, 1960.

[3] A. D. Sutherland and D. E. Countiss, "Parametric phase distortionless L-band limiter," Proc. IRE, vol. 48, pp. 938; May, 1960.

[4] F. A. Olson and G. Wade, "A cavity type parametric circuit as a phase-distortionless limiter," presented at the 1960 PGMTT Symp., Coronado, Calif.; May, 1960.

Correction to "Evidence of Satellite-Induced Ionization Effects Between Hemispheres"*

The first sentence of the above article, which appared on pages 1913–1914 of the November, 1960, issue of PROCEEDINGS, should have read as follows:

While monitoring a remote CW station at The Ohio State University Radio Observatory, Columbus, it has been found that large signal enhancements often occur at times related to the near approach of an artificial earth satellite.

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* Received by the IRE, November 18, 1960.

Multiple Diversity with Nonindependent Fading*

A recent article by Pierce and Stein[1] presented an analytical method for determining multiple diversity system performance in the presence of nonindependent Rayleigh fading. The purpose of this note is to supplement that article with curves calculated for one of the special cases treated in the article. These curves should give a more quantitative idea of the effects of correlated fading on diversity performance.

The calculations have been performed for binary data transmission by frequency shift keying, with predetection maximal ratio combining, bandpass matched filtering, and envelope detection. (This configuration has been extensively analyzed in the independent fading case by Barrow.[2]) The exponential correlation model discussed by Pierce and Stein[1] is assumed. That is, if μ_{jk} is the normalized correlation of the power received on the jth and kth diversity branches, then it is required that $\mu_{jk}=\mu^{|j-k|}$, where μ is the correlation between the adjacent branch fading; furthermore, it is assumed that mean power is the same on all branches.

The following notation is used:

N = number of diversity branches,
S_j = power received in watts in the jth branch during an element $j=1, 2, \cdots, N$,
S_0 = mean power in any branch,
μ = correlation of fading on adjacent branches,
$S=S_1+S_2+\cdots S_N$,
T = reciprocal of element transmission rate, in seconds,
n_0 = noise density in watts/cps.

* Received by the IRE, July 5, 1960.

[1] J. N. Pierce and S. Stein, "Multiple diversity with nonindependent fading," PROC. IRE, vol. 48, p. 89; January, 1960.

[2] B. B. Barrow, "Error probabilities for telegraph signals transmitted on a fading FM carrier," PROC. IRE, vol. 48, pp. 1613–1630; September, 1960.

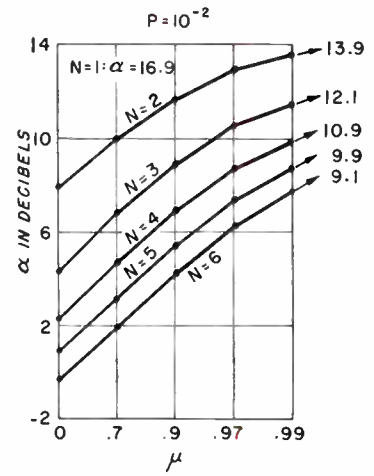

Fig. 1.

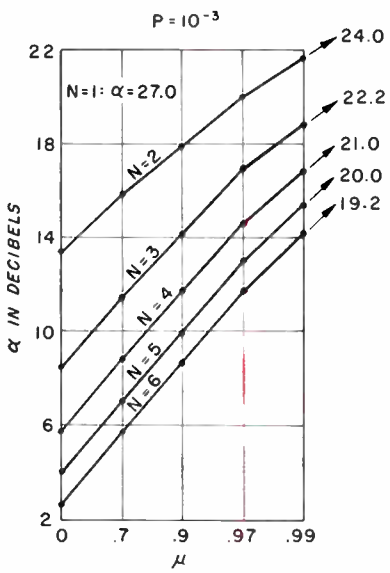

Fig. 2.

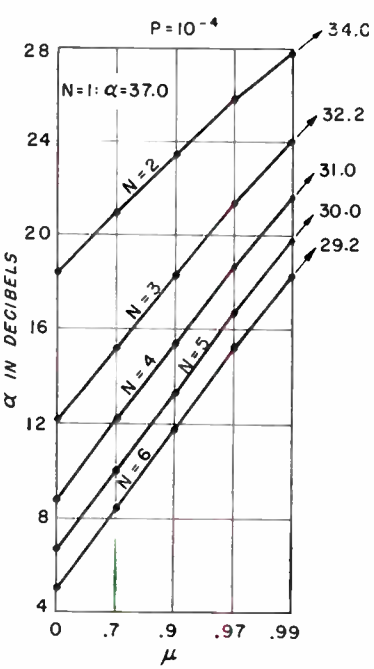

Fig. 3.

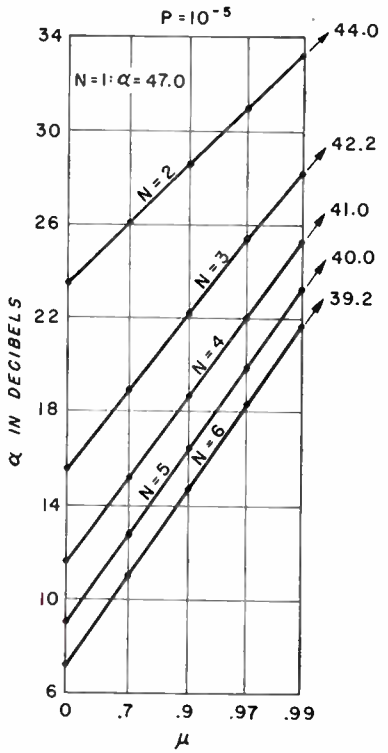

Fig. 4.

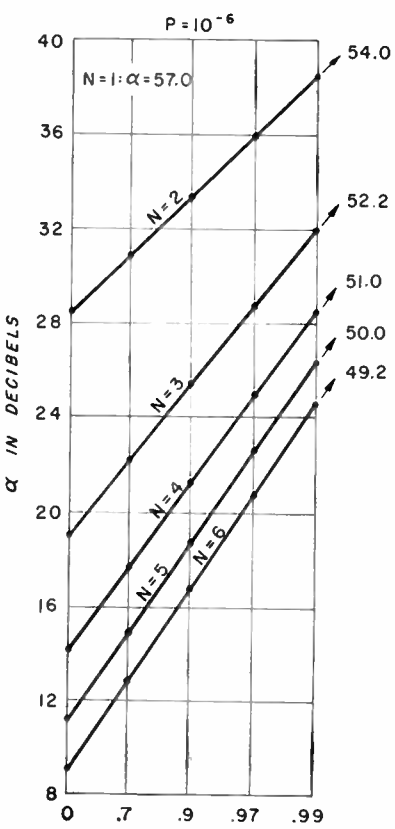

Fig. 5.

The element error rate for a particular set of received powers can be shown to be

$$pr(\text{error} \mid S_1, S_2, \cdots, S_N) = \tfrac{1}{2} \exp(-ST/2n_0). \quad (1)$$

It then follows that

$$pr(\text{error}) = \int_0^\infty pr(\text{error} \mid S) p(S) dS \quad (2)$$

$$= \int_0^\infty \frac{1}{2} \exp(-ST/2n_0) p(S) dS$$

$$= \frac{1}{2} [\mathcal{L} p(S)]_{z=T/2n_0}. \quad (3)$$

In (3), $\mathcal{L}$ is the Laplace transform operator and z is the variable of the transform. Pierce and Stein[1] give this transform as

$$\mathcal{L} p(S) = |I + zL|^{-1}, \quad (4)$$

where the vertical bars indicate determinant, I is the identity matrix, and L is given by

$$L = S_0 \begin{bmatrix} 1 & \mu^{1/2} & \cdots & \mu^{(N-1)/2} \\ \mu^{1/2} & 1 & \cdots & \mu^{(N-2)/2} \\ \mu^{2/2} & \mu^{1/2} & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots \\ \mu^{(N-1)/2} & \mu^{(N-2)/2} & \cdots & 1 \end{bmatrix}. \quad (5)$$

If we define a dimensionless parameter α by

$$\alpha = S_0 T / 2n_0, \quad (6)$$

(3) may be considered to be an equation giving α, and consequently the required transmitter power, as an implicit function of the probability of error.

This implicit equation has been solved numerically for several values of the error rate and for several orders of diversity. The results appear graphically in Figs. 1–5.

Although these curves have been calculated for a specific modulation, combining, and detection configuration, one could expect that much the same behavior as a function of correlation would obtain for other types of transmission and diversity reception.

I would like to thank the Applied Mathematics Section of the Computer and Mathematical Sciences Laboratory, AFCRC, who programmed sections of this work for the Cambridge Computer, and A. M. Pierce of the Communication Sciences Laboratory, AFCRC, who did much of the necessary hand calculation.

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Differential Phase Shifts in Ferrite Dielectric Loaded Coaxial Lines at 2200 Mc*

The theory of differential phase shift $(\beta^+ - \beta^-)$ in ferrite dielectric loaded coaxial lines (see Fig. 1) has been developed by two authors,[1-2] but very little has been reported on the experimental verification of this theory. Button[2] has prepared calculations showing the results which should be expected for a fixed ferrite loading as a function of the dielectric constant and dielectric cross-sectional area of the dielectric mode distorter. His results are shown in Fig. 2.

These calculations were made for a $1\frac{5}{8}$-inch, 50-ohm standard rigid coaxial line at 2000 mc with a ferrite loading factor of 11 per cent and a dc magnetic field biased below ferrimagnetic resonance. We were interested in similar phase shifts for a $\frac{7}{8}$-inch coaxial line, and the measurements reported below were made using standard $\frac{7}{8}$-inch OD 50-ohm rigid coaxial line.

Assuming that the propagating mode in the $\frac{7}{8}$-inch ferrite dielectric loaded coaxial line is the TE mode predicted by Button, the differential phase shift should depend upon the same loading parameters in the manner predicted by Fig. 2. However, it is to be expected that the values of $(\beta^+ - \beta^-)$ will not be as large as the predicted results, because of the degeneration of the TE mode in the $\frac{7}{8}$-inch coaxial line. An explanation of this effect is beyond the scope of this note, and the reader is referred to Sucher[1] and Button.[2] An experimental program was initiated to investigate the differential phase shift and compare the results with those predicted by Fig. 2.

Dielectric mode distorters were machined from Stycast HiK15. The ferrite used was Trans Tech 414, which has $4\pi M_s = 500$ gauss. This value of $4\pi M_s$ avoids low-field magnetic losses at 2200 mc. Fig. 3 shows a curve of experimental differential phase shifts and loss as a function of the dielectric loading factor for various H_{dc} biasing fields. In Fig. 3, the ferrite loading factor is 11 per cent, and the ferrite length is 3 inches. This gave a maximum phase shift of 0.3 radians/cm. Fig. 2 predicts the maximum differential phase shift to be 0.8 radians/cm for the $1\frac{5}{8}$-inch OD coaxial line for $K_c = 15$. The dependence of $(\beta^+ - \beta^-)$ shown in Fig. 3 is similar to that shown in Fig. 2 on the dielectric loading factor for dc magnetic fields below resonance, for this geometry resonance occurs at 560 gauss. The amount of differential phase shift for the $\frac{7}{8}$-inch coaxial line is approximately 60 per cent less than the theoretical differential phase shift for the $1\frac{5}{8}$-inch coaxial line.

An important factor in Fig. 3 is the agreement between the actual behavior and the theoretical behavior. For magnetic fields below resonance, the maximum phase shift occurs for loading factors near 0.25 (90°), as predicted by the theory. Above resonance, the differential phase shift is quite small and relatively constant. The losses associated with all three H_{dc} biasing fields are approximately equal, and we feel that no real significance can be attributed to this fact. Furthermore, we also feel that the losses can be made small by judiciously adjusting the position of the coaxial line in the magnetic field.

For the data reported in Fig. 3, the coaxial line was jigged in the dc magnetic field to keep mechanical position variations to a minimum.

Fig. 4 shows that the differential phase shift and insertion loss can be optimumized by experimental techniques. For the data shown in Fig. 4, the dielectric mode distorter was machined from Stycase HiK9, and its

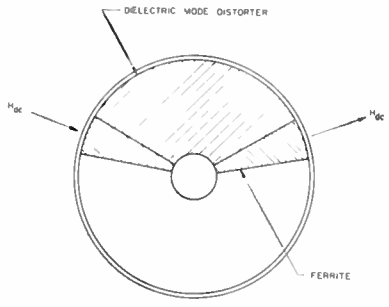

Fig. 1—Coaxial ferrite phase shifter cross section.

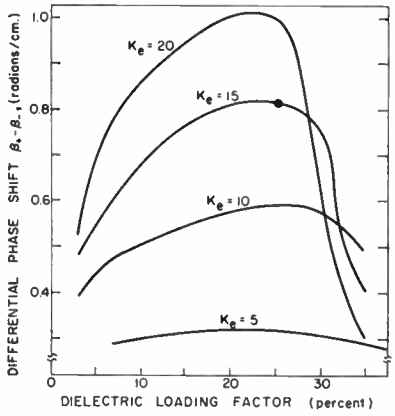

Fig. 2—Differential phase shift as a function of dielectric constant and dielectric loading factor for ferrite dielectric loaded 1-5.8-inch OD 50-ohm coaxial line, the biasing magnetic field below resonance.

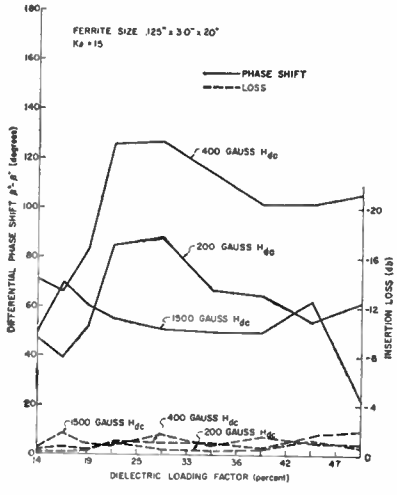

Fig. 3—Differential phase shift and loss as a function of dielectric angle.

* Received by the IRE, July 5, 1960.

[1] M. Sucher, "Application of Ferrite Materials to Microwave Instrumentation," Microwave Res. Inst., Polytechnic Institute of Brooklyn, Brooklyn, N. Y., Rept. No. R-572-57, PIB-500; April 24, 1957.

[2] K. J. Button, "Theory of Nonreciprocal Ferrite Phase Shifters in Dielectric-Loaded Coaxial Lines," M.I.T. Lincoln Lab., Lexington, Mass., TR No. 176; March 7, 1958. Also in *J. Appl. Phys.*, vol. 29, pp. 918–1000; June, 1958.

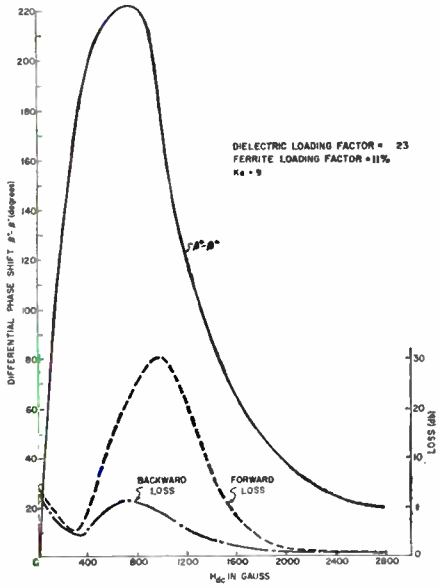

Fig. 4—Differential phase shift and loss as a function of H_{dc}.

dielectric loading factor was 0.23. The differential phase shift is shown as a function of H_{dc}, and values in excess of 180° under 1 db loss were obtained. This illustrates the importance of experimental procedures in the design of ferrite devices. We did not perform the same experiment with a $K_a = 15$ mode distorter, but we feel that even better results could be obtained from further investigation. Other tests relating differential phase shift to ferrite volume were also performed, but the results were degraded from the ones reported above, and are not reported here.

The author wishes to thank Dr. Philip S. Carter, Jr., for his technical assistance and insistence.

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A Broadband Termination for IF Coaxial Lines*

The IF portion of radar receivers is often divided into two or more amplifier chassis, which may be physically separated anywhere from a few inches to tens of feet. The signal is normally transmitted between chassis on a coaxial transmission line with a characteristic impedance of 50 to 100 ohms, and the line is usually driven through a tuned circuit which is loaded by the input impedance of the line. If the line is terminated in its characteristic impedance at all frequencies within the IF pass band, it will present a pure resistive load to the tuned driving circuit throughout the pass band. The driving circuit will then have a predictable frequency response. If the line is improperly terminated for any frequencies in the pass band, it will present an improper impedance to the tuned driving circuit at these frequencies. This will distort the driving-circuit frequency response, and the nature of the distortion will vary with line length.

A simple method of terminating such lines is with a noninductive resistor, having the same value as the characteristic impedance of the line; however, this does not give a perfect termination because the line must be connected to the input circuitry (usually the grid of one or more tubes) which adds a shunt capacitance. This capacitance can be resonated at the center frequency of the pass band by a shunt inductor. Such a circuit is shown in Fig. 1 along with the appropriate circuit equations. This circuit presents a perfect termination at the center frequency only. If its bandwidth is not significantly wider than the over-all amplifier pass band, the mismatch off center frequency within the passband is great enough to cause serious distortion of the driving circuit frequency response.

Circuit theorists[1] have treated the problem of constant input resistance matching networks with minimum insertion loss over a given pass band; however, it is difficult to derive a simple practical network by these techniques without considerable experience. Figs. 2 and 3 show two simple networks, each of which exhibits a constant input resistance at all frequencies, and has one terminal common to both input and output. Since the network of Fig. 2 has a capacitance shunting the output terminals, it would be suitable as a line termination. This termination would prevent distortion of the driving-circuit frequency response for any line length; however, it should be noted from the circuit equations that the network introduces a low-pass characteristic of its own. If the shunt capacitance is sufficiently small, the low-pass cutoff frequency will be well above the amplifier pass band so that the effect in the pass band will be small; however, in this case the simple circuit of Fig. 1 would have sufficient bandwidth.

If the shunt capacitance in the circuit of Fig. 2 is high enough to affect adversely the response in the pass band, the high-pass circuit of Fig. 3 may be cascaded with that of Fig. 2 to give a band-pass response. In both of these circuits the input resistance is equal in value to the circuit resistors at all frequencies; therefore, a resistor in one network can be replaced by the input impedance of the other network. The two circuits are cascaded by replacing the resistor shunting L_2 in Fig. 3 by the input impedance of the circuit of Fig. 2, as shown in Fig. 4. This circuit not only satisfies the basic requirement of a pure resistive line termination in the pass band, but also presents a perfect termination outside the pass band. Improper termination outside the pass band may cause undesired oscillation of the driving circuit.

In the circuit of Fig. 4, the upper cutoff

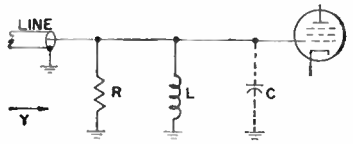

Fig. 1—Simple line termination.
R = characteristic impedance of line, Z_0.
Center frequency, $f_0 = 1/2\pi\sqrt{LC}$.
Bandwidth, $B = 1/2\pi RC$. $Q = 2\pi f_0 RC$.

$$Y = \frac{1}{R}\left[1 + jQ\left(\frac{f}{f_0} - \frac{f_0}{f}\right)\right].$$

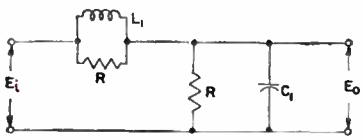

Fig. 2—Low-pass constant-R network.
$Z_1 = R = \sqrt{L_1/C_1}$ at all frequencies.
Cutoff frequency, $f_1 = 1/2\pi\sqrt{L_1C_1} = 1/2\pi RC_1$.

$$\frac{E_0}{E_i} = \frac{1}{1 + j(f/f_1)}.$$

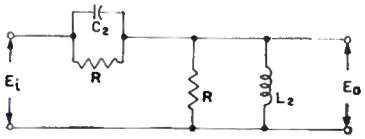

Fig. 3—High-pass constant-R network.
$Z_2 = R = \sqrt{L_2/C_2}$ at all frequencies.
Cutoff frequency, $f_2 = 1/2\pi\sqrt{L_2C_2} = 1/2\pi RC_2$.

$$\frac{E_0}{E_i} = \frac{1}{1 - j(f_2/f)}.$$

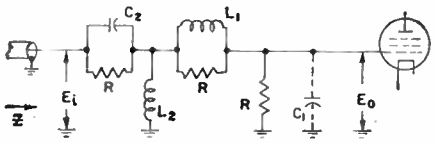

Fig. 4—Band-pass constant-R line termination.
$R = \sqrt{L_1/C_1} = \sqrt{L_2/C_2} = Z_0$ of line.
$f_1 = 1/2\pi RC_1$, $f_2 = 1/2\pi RC_2$.
$Z = (R + jO)$ at all frequencies.
$B = (f_1 + f_2) = (C_1 + C_2)/2\pi RC_1C_2$.

$$\frac{E_0}{E_i} = \frac{1}{(1 + f_2/f_1) + j(f/f_1 - f_2/f)}.$$

frequency, f_1, is determined by the characteristic impedance of the line, Z_0, and the shunt capacitance, C_1. It is desirable to have f_1 as high as possible; therefore, C_1 should consist only of the unavoidable input circuit capacitance. The designer is free to choose the value of the lower cutoff frequency, f_2. It would normally be chosen so that the center signal frequency, f_0, will be either the arithmetic or geometric mean of f_1 and f_2, giving the terminating network a symmetric band-pass characteristic to cascade with the other networks in the amplifier. The bandwidth of the proposed terminating network of Fig. 4 is always greater than the bandwidth of the simple termination of Fig. 1 by the ratio $(f_1+f_2)/f_1$; however, the proposed termination introduces a loss relative to the simple termination of the same ratio. This loss puts a practical upper

* Received by the IRE, March 23, 1960; revised manuscript received, June 1, 1960.

[1] H. J. Carlin, "Gain-bandwidth limitations on equalizers and matching networks," PROC. IRE, vol. 42, pp. 1676–1685; November, 1954.

limit on the value of C_1 which can be accommodated. In the case of geometric symmetry, when $C_1 < 1/(2\pi f_0 Z_0)$, the loss is less than 6 db, but for larger values of C_1 the loss increases as the square of C_1 in the limit.

The proposed circuit gives a perfectly matched broadband line termination for applications where distortion of the driving circuit frequency response is not permissible. Relative to the simple circuit which gives a distorted frequency response that varies with line length, the proposed circuit adds a cascaded band-pass characteristic which is independent of line length. The relative cost of this perfect termination is four additional small components and some attenuation of the signal.

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A Practical Compact UHF Isolator*

The realization of TEM mode solid-state isolators at frequencies below 1000 megacycles has presented a very formidable problem when dealing with conventional isolator structures,[1,2] with only limited success achieved to date.[3] The conventional dielectric loaded coaxial and stripline isolators are shown in Fig. 1(a) and 1(b). It is well known that these isolators utilize the dielectric medium to create a region of circular polarization of the h-vector in the vicinity of the ferrite material.

This note reports a somewhat different structure which offers considerable promise in solving the low-frequency TEM mode isolator problem. A cross-sectional view of the most promising form of this strip transmission line structure thus far devised is depicted in Fig. 1(c). The new structure utilizes only a ferromagnetic material. This material, by virtue of its asymmetrical placement on the center conductor, produces the mode distortion necessary for nonreciprocal wave propagation. This confirms the findings of other workers in the solid-state field.[4]

The material used was yttrium iron garnet, although certain other materials also yielded good operating characteristics. As shown in Fig. 1(c), the garnet was cut in slab form, placed with the broad side flush on the center conductor, and magnetized perpendicular to the broad dimension. Important parameters, such as fundamental ferromagnetic material characteristics (including saturation magnetization, linewidth, material size and shape), as well as degree of asymmetrical loading and applied magnetic field, were investigated in an attempt to obtain optimized operation. The results reported herein were derived from tests on devices operated at low power levels. The characteristics of such devices are quite promising, as evidenced in Figs. 2 and 3, where typical results obtained in two frequency ranges of operation are given.

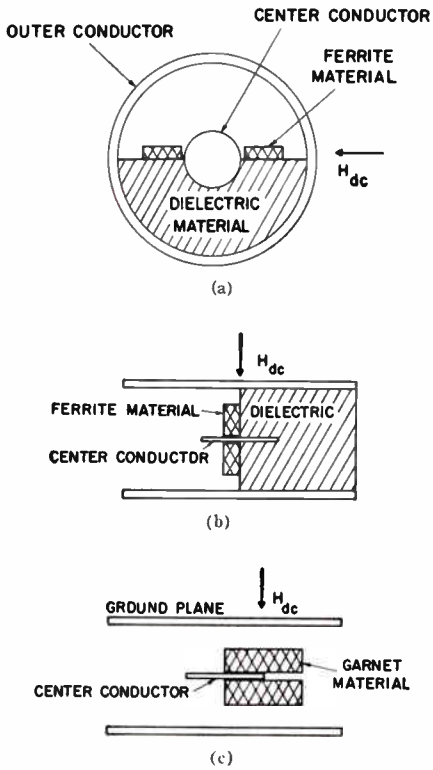

Fig. 1—New and conventional isolator structures.

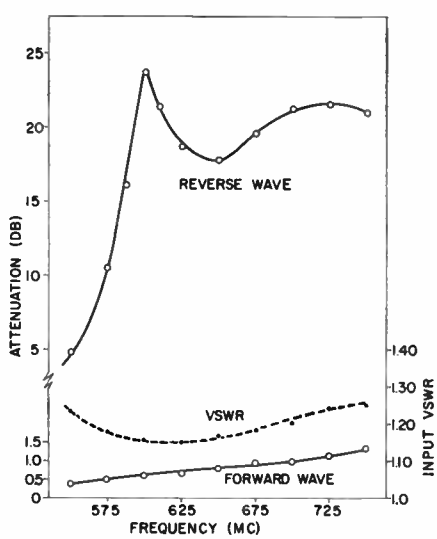

Fig. 2—Electrical performance of a UHF isolator.

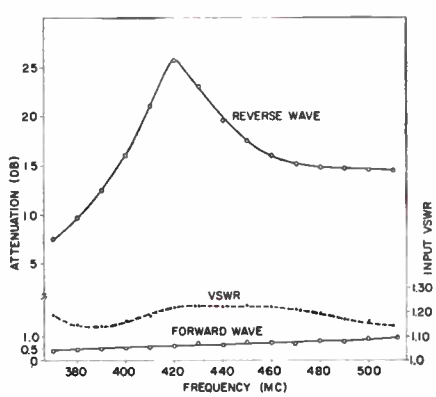

Fig. 3—Electrical performance of a UHF isolator.

Fig. 2 depicts the electrical performance of an isolator which exhibits better than 15-db to 1-db reverse to forward wave attenuation over an 18 per cent bandwidth centered about 640 megacycles. At 600 megacycles, a ratio of approximately 40 to 1 was obtained. In Fig. 3, electrical performance is given for an isolator which exhibits a better than 10-db to 1-db reverse to forward wave attenuation ratio over a bandwidth of 28 per cent. It is significant to note that at 420 megacycles an attenuation ratio of approximately 50 to 1 was obtained.

The input VSWR of each of these isolators is also shown, and is observed to remain below 1.25. It was found that this can, in general, be reduced through the use of conventional matching techniques.

Another unique feature of this device, which almost equals that of its electrical performance, is its physical size. The over-all size of the device, including permanent magnet is $1\frac{1}{2}$ inches $\times 2\frac{1}{4}$ inches $\times 6\frac{1}{2}$ inches. A photograph of the assembled isolator is shown in Fig. 4.

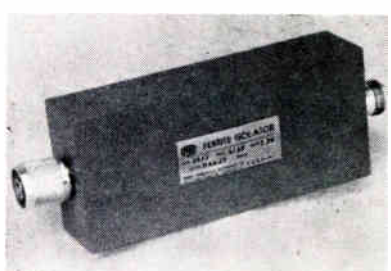

Fig. 4—Typical commercial version of the isolator.

Additional and more complete information relating to lower frequency, higher power and other information pertinent to this new structure will be forthcoming in a future publication.

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* Received by the IRE, July 5, 1960.

[1] B. J. Duncan, L. Swern, K. Tomiyasu, and J. Hannwacker, "Design considerations for broadband ferrite coaxial line isolators," Proc. IRE, vol. 45, pp. 483–490; April, 1957.
[2] S. Weisbaum and H. Seidel, "The field displacement isolator," *Bell Sys. Tech. J.*, vol. 35, pp. 877–898; July, 1956.
[3] B. J. Duncan and G. F. Horner, "Coaxial line isolators at and below 1 kmc," Proc. IRE, vol. 47, pp. 103–104; January, 1959.
[4] H. Seidel and R. C. Fletcher, "Gyromagnetic modes in waveguide partially loaded with ferrite," *Bell Sys. Tech. J.*, vol. 38, pp. 1427–1456; November, 1959.

Spectrum of Exponential Message Lengths*

Consider transmitting serially a sequence of statistically identical, mutually independent messages whose respective mes-

* Received by the IRE, July 25, 1960.

sage lengths are exponentially distributed. This scheme is represented mathematically by

$$s(t)=\lim_{N\to\infty}\sum_{-N}^{N}s_n(t)\left[u_{-1}(t-t_n)-u_{-1}(t-t_{n+1})\right];$$
$$u_{-1}(x)=\text{unit step function} \quad (1)$$

where

$$\langle s_n(t)s_m(t+\tau)\rangle = 0, \qquad n\neq m$$
$$= R_{ss}(\tau), \qquad m=n$$

and

$$\langle s_n(t)\rangle = 0 \qquad \text{for all } n.$$

Further, $(\Delta t)_n=t_{n+1}-t_n$ are mutually independent random variables and possess an exponential distribution of mean $1/\lambda$ where

$$1/\lambda=\lim_{N,T\to\infty}T/N.$$

To determine the spectrum we first compute

$$\sqrt{2\pi}S_T(\omega)\overset{\Delta}{=}\int_{-T}^{T}s(t)e^{j\omega t}dt$$
$$=\sum_{-N}^{N}\int_{t_n}^{t_{n+1}}s_n(t)e^{j\omega t}dt$$
$$\text{for large } N. \quad (2)$$

then

$$2\pi\left|S_T(\omega)\right|^2$$
$$=\sum_{-N}^{N}\sum_{-N}^{N}\int_{t_n}^{t_{n+1}}\int_{t_m}^{t_{m+1}}s_n(t)s_m(\sigma)e^{j\omega(t-\sigma)}dtd\sigma \quad (3)$$

and by the Wiener-Kinchine definition

$$\Phi_{ss}(\omega)\overset{\Delta}{=}\lim_{T\to\infty}\langle\left|S_T(\omega)\right|^2\rangle \quad (4)$$

now;

$$2\pi\langle\left|S_T(\omega)\right|^2\rangle=\sum_{n,m}\int_{-\infty}^{\infty}\cdots\int_{-\infty}^{\infty}dt_np(t_n)$$
$$\cdot\int_{t_n}^{t_{n+1}}\int_{t_m}^{t_{m+1}}\langle s_n(t)s_m(\sigma)\rangle e^{j\omega(t-\sigma)}dtd\sigma,$$
$$2\pi\langle\left|S_T(\omega)\right|^2\rangle=\sum_{n=-N}^{N}\int_{-\infty}^{\infty}\cdots\int_{-\infty}^{\infty}dt_np(t_n)$$
$$\cdot\int_{t_n}^{t_{n+1}}\int_{t_n}^{t_{n+1}}R_{ss}(t-\sigma)e^{j\omega(t-\sigma)}dtd\sigma. \quad (5)$$

By a suitable change in variable it can be shown that

$$\int_{t_n}^{t_{n+1}}\int_{t_n}^{t_{n+1}}R_{ss}(t-\sigma)e^{j\omega(t-\sigma)}dtd\sigma$$
$$=2\int_0^{(\Delta t)_n}\left[(\Delta t)_n-x\right]R_{ss}(x)\cos\omega x dx. \quad (6)$$

Since the t_n points are independent it follows that

$$2\pi\langle\left|S_T(\omega)\right|^2\rangle=2\sum_{-N}^{N}\int_0^{\infty}P(\Delta t_n)$$
$$\cdot\left\{\int_0^{(\Delta t)_n}\left[(\Delta t)_n-x\right]R_{ss}(x)\cos\omega x dx\right\}d(\Delta t)_n$$
$$\text{for large } N. \quad (7)$$

The message lengths are exponentially distributed so that

$$P(\Delta t_n)=\lambda e^{\lambda(\Delta t)_n};\quad \lambda=\lim_{N,T\to\infty}N/T. \quad (8)$$

Inserting $P(\Delta t n)$ into (8) and integrating by parts we have:

$$2\pi\Phi_{ss}(\omega)=\lim_{N,T\to\infty}\frac{1}{2T}\sum_{-N}^{N}\frac{2}{\lambda}\int_0^{\infty}$$
$$\cdot e^{-\lambda\tau}R_{ss}(\tau)\cos\omega\tau d\tau,$$
$$2\pi\Phi_{ss}(\omega)=\int_{-\infty}^{\infty}e^{-\lambda|\tau|}R_{ss}(\tau)e^{j\omega\tau}d\tau \quad (9)$$

and taking the inverse transform we obtain

$$\phi_{ss}(\tau)=R_{ss}(\tau)e^{-\lambda|\tau|}. \quad (10)$$

This represents a more general result than that obtained by James, Nichols and Phillips.[1] An interesting implication of this conclusion is to consider a phase-controlled oscillator whose phase is switched in a Poisson fashion with a uniform phase distribution. If the mean frequency of switch occurrences is λ (much less than sinusoidal frequency), then the resulting spectrum is identical to narrow-band "RC" noise amplitude modulating the oscillator in the suppressed carrier mode.

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[1] H. M. James, N. B. Nichols, and R. S. Phillips, M.I.T. Rad. Lab. Ser., McGraw-Hill Book Co., Inc., New York, N. Y., vol. 25, pp. 301–303; 1947.

Translation of a Historic Paper on Diversity Reception*

In his excellent paper on diversity, Brennan[1] cited the important pioneering work on diversity reception published in 1931 by Beverage, Peterson, and Moore.[2,3] At about the same time that this work was going on at RCA, a similar experimental study of fading and of diversity receiving techniques was being carried out by the PTT of the Netherlands East Indies, as part of an investigation into the possibilities of using short-wave transmission for commercial purposes. The problem was of urgent interest, because there already existed enough telegraph traffic between the Netherlands and the then prosperous colonies to saturate all available channels. Furthermore, scheduled short-wave broadcasts of both voice and music had begun. Severe fading frequently made short-wave reception impossible, however, and radio engineers worked to develop techniques such as AGC and diversity combination to counter the violent fluctuations in received signal strength.

In charge of this work at the Rantja-Ekek receiving station near Bandung, Java, was a young engineer named A. de Haas, and in 1927 and 1928 he published his results in a two-part article in *Radio-Nieuws*.[4] This remarkable paper contains a thorough, qualitative discussion of the fading phenomena, and describes a set of experiments in diversity reception, and the practical diversity combiner to which they led. It may well be the first published work on diversity reception, but because it appeared in a journal that did not circulate widely, it has not received the attention it deserves. The following is a translation of the most important portions.

* * * * * * *

Short-Wave Reception Without Fading

In the beginning of the short-wave era, it was more than once alleged that no fading existed on the ultra-short wavelengths, in contrast with wavelengths of 200 meters and longer. Anyone who has a little practical experience in short-wave reception can contradict this.

It is not even too strong to assert that the development of the short waves for high-speed telegraphy, commercial radiotelephony and facsimile transmission is closely bound up with the possibility of eliminating the fading phenomenon in whole or in part. Whereas fading can sometimes present difficulties even for ordinary telegraphy operation, it often appears to present insurmountable obstacles to high quality telephone reception.

. . . . . .

The fading phenomena may be characterized under several general headings as follows:

1) There are two types of fading: the slow, smoothly varying fading, and the fast (one might say precipitous) fading. Slow fading has, as a rule, a rather regular period, and appears in various degrees of intensity, with "inaudible" during the fade as the worst.

. . . . . .

The writer has never observed any regularity in the occurrence of fast fading, but the investigations are not yet thorough enough to state any firm conclusions about this.

It is more or less obvious to ascribe the slow, periodic fading to changes in the Heaviside layer, while fast fading is probably related to interference between waves arriving out of phase from more than one direction. Whether this hypothesis is correct remains to be seen. . . .

As a rule, both [types of fading] appear together, the one more or less superposed on the other

2) Fading depends upon frequency.

For waves with only a few kHz difference, there appears an important phase difference

* Received by the IRE, June 8, 1960; revised manuscript received July 5, 1960.

[1] D. G. Brennan, "Linear diversity combining techniques," Proc. IRE, vol. 47, pp. 1075–1102; June, 1959.

[2] H. H. Beverage and H. O. Peterson, "Diversity receiving system of RCA Communications, Inc., for radiotelegraphy," Proc. IRE, vol. 19, pp. 531–561; April, 1931.

[3] H. O. Peterson, H. H. Beverage, and J. B. Moore, "Diversity telephone receiving system of RCA Communications, Inc.," Proc. IRE, vol. 19, pp. 562–584; April, 1931.

[4] A. de Haas, "Kortegolf ontvangst zonder fading," *Radio-Nieuws*, vol. 10, pp. 357–364; December, 1927. Pt. II, *ibid.*, vol. 11, pp. 80–88; February, 1928. *Radio-Nieuws* was the monthly journal of the Nederlandsche Vereeniging voor Radio-Telegrafie. It is no longer published. The author of this letter can, however, supply a few photocopies of De Haas's paper, which is written in Dutch.

in the fading. The short-wave transmitters at Kootwijk [Netherlands] give a singular example of this. [These transmitters] signal by means of a frequency shift of, as a rule, several kHz. Although then the fast fading for both frequencies is entirely different, there appears also to exist an easily perceptible phase difference in the slow fading of the two waves, even if the period is rather long, *e.g.*, 10 seconds.

. . . . . .

So far as the connection between fading and frequency is concerned, it may further be observed that, in general, the longest waves show the slowest fading. The 64-meter from KDKA generally exhibits fading with a very slow period of 15 seconds or more. At 25 meters the period is often several seconds, while at 15 meters, it is much shorter still.

. . . . . .

3) Fading depends upon the condition of the atmosphere, or, if you like, upon the state of the layers working for the transmission, both on transmitting and receiving sides.

. . . . . .

To take another example, reception from San Francisco on 29.3 meters can be taking place without noticeable fading, while at the same instant reception from Kootwijk on 29 meters exhibits very deep slow fading. [Note: The receiver on Java was roughly equidistant from Kootwijk and San Francisco.]

. . . . . .

From earlier observations at telegraph stations it was already known that fast fading appears asynchronously at receivers separated by a few tens of meters. And here we have arrived at the principle of the antifading system erected by the author for the government radio service at Rantja-Ekek —fading does not appear in synchronism at different places.

For fast fading this difference can already be noticed if one connects two receivers to antennas that are separated from each other by only a few tens of meters. If one puts a loudspeaker on each receiver and stands so that both give equally strong impressions of loudness on the average, then he marks immediately that the source of sound appears to move to and fro between the two speakers.

The first experiment at Rantja-Ekek was made with two receivers placed about 250 meters apart. It appeared that the rapid fades fell entirely differently, at most once in incidental coincidence, while for the slow fading a considerable phase difference was observed, larger according as the period became shorter. A definite regularity for this phenomenon has nevertheless not yet been found.

This and further investigations were sufficient encouragement to make a test on a larger scale. In the neighboring villages, Pintoe and Rantja-Batok, houses were rented and fitted out as temporary receiving stations. (See Fig. 1.) By means of cables and above-ground landlines, these stations were connected with the so-called Raamkooi, an accommodation for experiments in the immediate neighborhood of the main receiving station, and there the audiofrequency signals were combined (*gemengd* = blended, mixed). The manner in which this was accomplished

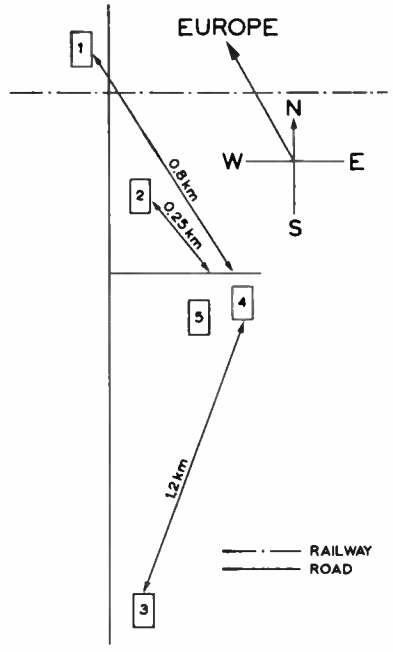

Fig. 1—Layout of the antifading system at Rantja-Ekek, Java. 1) Auxiliary station Ranta-Pintoe. 2) Auxiliary station in high-frequency transmitter building. 3) Auxiliary station Rantja-Batok. 4) Raamkooi. 5) Main receiving station at Rantja-Ekek.

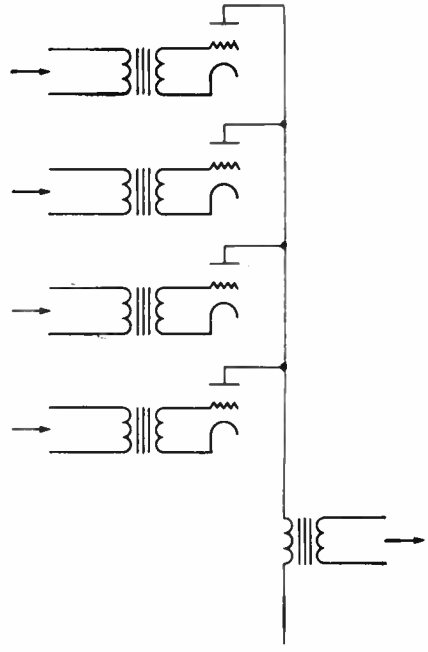

Fig. 2—Schematic diagram of low-frequency combiner-amplifier.

will be described in a following article.

In spite of the incompleteness of the system, following from the provisional nature of the arrangement, the reception achieved can, for practical purposes, be described as fading-free. Only the knowing ear can observe now and then a slight wavering; there is no longer any question of really important fades. Experiments have been carried on for several months with this system, and the promising results have led to a decision to rebuild in final form.

. . . . . .

Part II

There are now two possible methods of combination that present themselves:

1) Each received audio signal is put on a loudspeaker, and the four loudspeakers are placed before one microphone, after which low-frequency amplification follows until the "combined signal" is brought to a sufficiently high level. This method is easily implemented, and it has been justified by experiments, but it is nevertheless not an elegant solution, because a speaker-microphone retransmission system, no matter how well made, is never free of faults.

2) The other, preferable solution is: every auxiliary receiver gets a so-called coupling tube, the anodes of which are connected together in parallel. [See Fig. 2.] A preliminary condition that must be fulfilled is that the mean audio signal strengths from the various stations must be equal. With the loudspeaker-microphone system, this is difficult to control. With the use of coupling tubes it is really very simple. After the audio amplitudes of the various stations have been adjusted to the same mean (adjustment by ear appears to be sufficient), the combined signal becomes available on the common anode impedance of the four tubes, and it may thereafter be passed through a tone control and, finally, through large output tubes [LS5a], to the line.

. . . . . .

[The omitted paragraphs discuss implementation of the system and details of the circuit. Superheterodyne receivers were chosen ("reliable and stable"), and the audio frequency signals were brought via land lines to the central point for combination.]

Although the usefulness of the system was demonstrated immediately in experiment, the following test was made to obtain a more complete insight into its operation.

The incoming signal from each auxiliary station, after regulation to the same mean value, was rectified, and the rectified current presented to a critically damped milliammeter in the plate circuit. It then appeared that with constant modulation (long dash with 500-cps tone), all meters moved independently of each other and asynchronously, while the control meter, measuring after combination, showed slight tremblings, though no important fades were any longer apparent. If this appears, at first, to present immediate justification of the design of the system, it may still be wondered in connection with the fact that the control-meter was *not absolutely* steady, whether the result is really conclusive.

The obvious means of obtaining a more constant average is naturally to install more auxiliary receiving stations. On the other hand it is desired, both for operational reliability and for economic reasons, to hold the number of auxiliary stations as low as possible. The meter fluctuations after combination were in fact relatively weak, and the dominant criterion here is not steadiness on measuring instruments, but "auditory steadiness." Here we are helped by the well known exponential sensitivity of our hearing organ.

It appears, from the test referred to

above, that only with care can the ear detect the insignificant variations in volume, and even then only with a [modulating] signal of constant tone and volume. With speech and music such variations pass entirely unnoticed.

. . . . . .

[The deleted paragraphs discuss the permanent installation that was erected following the tests, as well as the operating procedure and service routine.]

If it is thus possible in the manner discussed to eliminate the fading phenomenon upon reception, another question is now whether the quality of reception is also improved by this system. Naturally this is the case only insofar as the [combined] signal continuously has *that* strength that it exhibits on one single receiver at peak. Thus, if there is very bad fading on one single receiver, the intelligibility index with this installation is greatly raised; still it is self-evident that it can never be better than the intelligibility on a single receiver during the peak strength.

. . . . . .

* * * * * * *

The history of the growth of scientific ideas is full of examples where it was difficult to give proper credit to early investigators because their understanding of the significance of their own work was so incomplete. De Haas did not present such a dilemma to the historian. He clearly understood the important characteristics of short-wave fading, and he seems to have gained this knowledge largely from his own careful observations. These observations led him to experiment with space-diversity reception, and the experiments led, in turn, to a practical space-diversity receiver, which was made part of the permanent short-wave receiving installation of the Netherlands East Indies PTT.

In modern terminology De Haas's combiner was an equal-gain post-detection combiner, and he recognized that with such a combiner the mean signal levels in the various branches had to be approximately equal. He saw also that increasing the order of diversity decreased the effects of the fading for the listener and he correctly adduced the logarithmic characteristic of the human ear to help explain this.

The last sentence of the translation contains a technical error, for the equal-gain combiner can in fact produce an output signal-to-noise ratio better than that in any branch. This comes about because the signals add more or less in phase, while the noise waves in the various branches do not. De Haas can hardly be criticized, however, for failing to take account in 1927 of some of the properties of random waves. It was not until 1954 that Kahn discussed in this context the possible improvement obtainable by combination.[5]

In closing, I would like to thank my colleague W. Metzelaar for his copies of *Radio-Nieuws* and for his many helpful comments on the translation.

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[5] L. R. Kahn, "Ratio squarer," Proc. IRE, vol. 42, p. 1704; November, 1954.

Experimental Proof of Focusing at the Skip Distance by Backscatter Records*

In the above letter, Bibl[1] claims that he has obtained experimental proof of skip-zone focusing from groundscatter observations. Unfortunately, he gives no details about how skip-zone focusing is involved in the groundscatter mechanism. This is a critical point because both Peterson[2] and Dieminger[3] showed that the focusing mechanism which enhances groundscatter is least-time focusing and not skip-zone focusing. Using a parabolic model for the electron density, Peterson calculated the least-time and the skip-zone paths, and showed that they do not coincide. Because the skip-zone and the least-time paths are almost coincident at operating frequencies greater than twice the critical frequency, skip-zone focusing might produce some enhancement; but one cannot exclude the effect of least-time focusing. Thus, in order to use groundscatter echoes to prove anything about skip-zone focusing, one must first eliminate the effects of the primary focusing agent, least-time focusing.

From Bibl's discussion and illustrations, it is not clear what criteria were used to determine whether or not focusing of some sort occurred at a particular time. The mere existence of groundscatter is not a sufficient condition because antenna patterns, ionospheric absorption, equipmental operating parameters, and the critical frequency greatly affect the results. If the broadness of the echo is used as the criterion, then the echo amplitude must be known. Even if the amplitude is known, however, other information is necessary to separate the skip-zone focusing from the least-time focusing effects. Whether this separation is possible is the question here; at present, there does not appear to be any technique for separating them. Thus, it is doubtful that groundscatter can be used directly to prove the existence of skip-zone focusing.

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Author's Comment[4]

H. F. Bates, R. D. Hunsucker, and L. Owren have drawn attention to the existence of two possible focusing effects: least-time focusing, and skip-zone focusing. For short distances (1000 km or less), the skip distance focusing is weak. For long distances ($\approx$2000 km or more), both effects definitely coincide; therefore, I used the expression skip-distance because it is better known and more important. More exact calculations could be arrived at with the formulas for ray propagation in curved coordinates which I published ten years ago in *Revue Scientifique*. It seems to me that for shorter distances the influence of the magnetic field cannot be neglected. In my recent note, I wanted to show that a good focusing effect occurs much more often than is generally believed; this holds true especially under conditions of quiet behavior of the F ionization as in Southern and Southwestern Europe. A small range of focusing, inferior to 50 km for one hop—with clear separation of the two magnetic components—has frequently been observed. Horizontal irregularities of the ionosphere are smaller than might be expected in that zone. On the other hand, the ground scatter point was not found to depend on the geographical situation of the backscattering region; the skip zone variations appeared to be quite regular. Fig. 1 shows a backscatter record to indicate focusing at the skip distance.

To avoid errors, it should be noted that in my letter the expression $1\times F$ backscatter means a one hop with backscatter at the ground, returned by 1 F-hop propagation; $2\times F$ backscatter means 2 hop-F propagation, scattered at its end at the ground and returned in the same manner.

Perhaps eventually it will be possible to use the $2\times F$-ground-backscatter mode and the separation of the two magnetic components for distinguishing between the different focusing effects.

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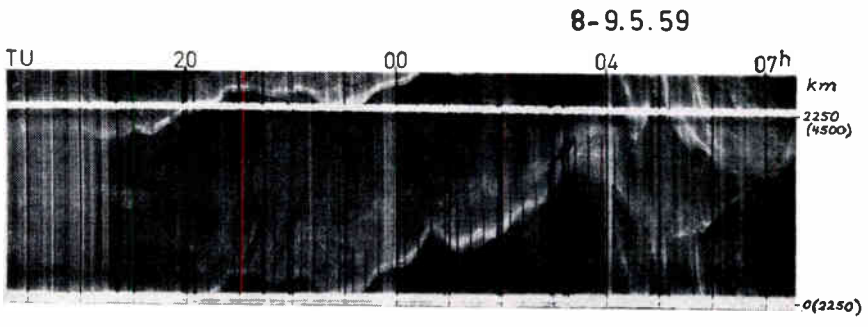

Fig. 1.

* Received by the IRE, June 24, 1960.

[1] K. Bibl., "Experimental proof of focusing at the skip distance by backscatter records," Proc. IRE, vol. 48, pp. 956–957; May, 1960.

[2] A. M. Peterson, "The mechanism of F-layer propagated backscatter echoes," *J. Geophys. Res.*, vol. 56, pp. 221–237; June, 1951.

[3] W. Dieminger, "The scattering of radio waves," *Proc. Phys. Soc.*, vol. B-64, pp. 142–158; February, 1951.

[4] Received by the IRE, July 13, 1960.

A Note on the Radiation Resistance of a Thin Linear Antenna*

The radiation resistance of a thin antenna of length L is given by the well known formula,[1]

$$R_0 = 60 \int_0^{\pi} \frac{\left[\cos\left(\frac{\beta L}{2}\cos\theta\right) - \cos\left(\frac{\beta L}{2}\right)\right]^2}{\sin\theta} d\theta \text{ ohms.}$$

Where $\beta = 2\pi/\lambda$, L = length of the centerfed antenna. Here R_0 is referred to a current maximum.[2] In general, an analytical solution of this integral is not possible. It is the purpose of this note to point out that over a restricted range of values of (L/λ), an approximate but quite useful solution of the problem may be obtained by expanding the numerator of the integrand in a Neumann series which is strongly convergent for small values of L. If we restrict our attention to $L \leq \lambda$, then it is accurate enough to retain up to the fourth order term in the series, thus incurring an error of about 4 per cent when $L = \lambda$.

Thus, within this limit, one obtains on simplification,

$$R_0 = \left[1280 J_2^2\left(\frac{\beta L}{2}\right) + 1755.4 J_4^2\left(\frac{\beta L}{2}\right) - 2048 J_2\left(\frac{\beta L}{2}\right) J_4\left(\frac{\beta L}{2}\right)\right]. \quad (1)$$

When L is appreciably smaller than λ, it is possible to neglect certain terms in (1) to obtain an equation of more compact form.

Thus, when $L \leq \lambda/2$, the term involving $J_4^2(\beta L/2)$ becomes very small, and one obtains,

$$R_0 = 256 J_2\left(\frac{\beta L}{2}\right)\left[5 J_2\left(\frac{\beta L}{2}\right) - 8 J_4\left(\frac{\beta L}{2}\right)\right] \text{ohms.} \quad (2)$$

It may be noted that (2) is accurate to within about 0.3 per cent for $L \leq \lambda/2$. If $L \leq \lambda/4$, then the term involving the product of $J_2(\beta L/2)$ and $J_4(\beta L/2)$ also becomes negligible, and for this, one obtains

$$R_0 = 1280 J_2^2\left(\frac{\beta L}{2}\right) \text{ ohms.} \quad (3)$$

It is easily shown that the error involved in using (3) is 1.2 per cent for $L \leq \lambda/4$ and 7.5 per cent for $\lambda/4 < L < \lambda/2$.

For $L < \lambda/4$, the result is further simplified as[3]

$$R_0 = 1947\left(\frac{L}{\lambda}\right)^4 \text{ohms,} \quad (4)$$

the error thus incurred being within 5 per cent for $L = \lambda/4$.

It is also seen from this equation that for a very short linear antenna, $L < \lambda/4$, there is approximately a 12-db increase in radiated power per octave increase in length, or frequency.

The usefulness of (1) to (4) is illustrated by the results recorded in Table I. In column II from a) to d), the values of R_0 as obtained from these equations are recorded for certain selected values of L as stated in column I. In column II e) are given the more accurate values as obtained from graphical analysis of King, Mimno, and Wing.[2]

TABLE I

I Length = L	II R_0 (ohms), as calculated from a) Eq. (1)	b) Eq. (2)	c) Eq. (3)	d) Eq. (4)	e) From the graph of King, *et al.*
$\lambda/4$	7.9	7.9	7.9	7.6	8
$\lambda/2$	73.1	72.8	79.2	—	73
$2\lambda/3$	131.8	—	—	—	133
$3\lambda/4$	173	—	—	—	179
λ	192	—	—	—	200

It is easily seen that the values given by the approximate method indicated above are in reasonable agreement with those obtained from the graphical method of computation. It should be noted that for $L > \lambda$, the present method of approach becomes too cumbersome and in that range, it would be necessary to use the graphical method.

ACKNOWLEDGMENT

The authors are indebted to Prof. J. N. Bhar, D.Sc., F.N.I., for his interest in the work which was done at the Institute of Radio Physics and Electronics, Calcutta. Thanks are also due to Sri P. K. Sinha Ray for his kind criticism of the work.

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* Received by the IRE, July 15, 1960.

[1] R. W. King, H. R. Mimno, and A. Wing, "Transmission Lines, Wavegnides and Antenna," McGraw-Hill Book Co., Inc., New York, N. Y., p. 120; 1945.

[2] J. D. Kraus, "Antennas," McGraw-Hill Book Co., Inc., New York, N. Y., p. 143; 1950.

[3] L. A. Pipes, "Applied Mathematics for Engineers and Physicists," McGraw-Hill Book Co., Inc., New York, N. Y., p. 310; 1946.

Boolean Functions Realizable with Single Threshold Devices*

Recently Paull and McCluskey[1] discussed the properties of the Boolean functions which can be realized with a single threshold device. Necessary conditions were given in three theorems,[1] Theorems 1 and 2 being the special cases of Theorem 3, which is referred to here as the Paull-McCluskey Theorem.

This note presents a somewhat different approach to the problem with a hope of making some contribution to their excellent discussion. Magnetic cores are also used here as representative threshold devices. An alternate proof of the Paull-McCluskey Theorem is first given and a necessary and sufficient condition for realizability is then stated.

NOTATIONS

A Boolean function $F(x_1, x_2, \cdots, x_n)$, or simply F, of n variables $x_1, x_2, \cdots, x_n$, is a function on the vertices of a n-dimensional cube to 0 and 1. Let $V_1(F)$ and $V_0(F)$ denote, respectively, the sets of vertices where F is 1 and 0, namely $V_1(F) = \{F^{-1}(1)\}$ and $V_0(F) = \{F^{-1}(0)\}$.

Some, but not all, Boolean functions can be realized with a single core. Throughout this paper, the term realizability means realizability with a single core. Without loss of generality let zero and one be the threshold levels of the magnetic core; a current of unity and zero corresponds to the binary states of the input variables. Let there be $n+1$ inputs to a circuit for the production of a Boolean function of n variables. Each of the input variables $x_i (i = 1, 2, \cdots, n)$ is connected to a winding of N_i turns, where the sign of N_i indicates the winding polarity. One winding of N_0 turns is associated with a constant bias.

The following interpretation of realizability is used: A Boolean function $F(x_1, x_2, \cdots, x_n)$ is realizable with a single core (*i.e.*, F is a setting function), if and only if there exist a scalar N_0 and an n-vector $N = (N_1, \cdots, N_n)$ such that for each vertex (or vector) v belonging to $V_1(F)$,

$$N \cdot v \geq 1 - N_0 \quad (1a)$$

and for each vertex v belonging to $V_0(F)$

$$N \cdot v \leq -N_0, \quad (1b)$$

where dot "$\cdot$" denotes the usual scalar product of two vectors.

Eqs. (1a) and (1b) are, respectively, the condition on the magnetomotive force to set and reset the core.

A LEMMA

A necessary condition for realizability can be stated in terms of a sufficient condition for nonrealizability as follows.

Lemma: If there exist $k (k > 0)$ vertices, $v_1, v_2, \cdots, v_k$ belonging to $V_1(F)$ and k vertices $u_1, u_2, \cdots, u_k$ belonging to $V_0(F)$ such that their vector sums are equal, namely

$$\sum_1^k v_i = \sum_1^k u_i, \quad (2)$$

then the Boolean function F is not realizable.

A proof is by contradiction. Suppose F is realizable; then the required N_0 and $N = (N_1, N_2, \cdots, N_n)$ do exist. Eq. (1) implies that

$$N \cdot v_i \geq 1 - N_0$$

* Received by the IRE, July 22, 1960.

[1] M. C. Paull and E. J. McCluskey, Jr., "Boolean functions realizable with single threshold devices," PROC. IRE, vol. 48, pp. 1335–1337; July, 1960.

and

$$N \cdot u_i \leq -N_0 \quad (i = 1, 2, \cdots, k).$$

By summing over i, one has

$$\begin{aligned} N \cdot \sum_1^k v_i &\geq k(1 - N_0); \\ N \cdot \sum_1^k u_i &\leq -kN_0. \end{aligned} \tag{3}$$

Eqs. (2) and (3) lead to a contradiction that

$$-kN_0 \geq N \cdot \sum u_i = N \cdot \sum v_i \geq k - kN_0.$$

This lemma includes the Paull-McCluskey Theorem, as the former, with k equal to two, leads to the latter.

Paull-McCluskey Theorem

This theorem can be equivalently stated as follows. If there exists a pair of residues, R_1 and R_2, which occur in a canonical expansion of F about some number of variables such that neither one residue includes the other nor both residues are equal, then F is not realizable.

The antecedent in the theorem implies the antecedent in the preceding lemma. The former means that both sets $\overline{R}_1 \cap R_2$ and $R_1 \cap \overline{R}_2$ are not empty. This in conjunction with the fact that $V_1 \cup V_0$ includes all vertices of the n cube implies that there exist four distinct vertices v_1, v_2, u_1 and u_2 such that v_1 and v_2 are in $V_1(F)$ and u_1 and u_2 are in $V_0(F)$ and that they are of the following forms:

$$\begin{aligned} v_1 &= (a_1, a_2, \cdots, a_k, a_{k+1}, \cdots, a_n) \\ v_2 &= (b_1, b_2, \cdots, b_k, b_{k+1}, \cdots, b_n) \\ u_1 &= (a_1, a_2, \cdots, a_k, b_{k+1}, \cdots, b_n) \\ u_2 &= (b_1, b_2, \cdots, b_k, a_{k+1}, \cdots, a_n) \end{aligned}$$

where a's and b's are constants of 0 or 1; the indexes $1, 2, \cdots, k$ refer to the variables about which F is expanded; and $(a_{k+1}, \cdots, a_n)$ and $(b_{k+1}, \cdots, b_n)$ belong, respectively, to $R_1 \cap \overline{R}_2$ and $\overline{R}_1 \cap R_2$. Consequently $v_1 + v_2 = u_1 + u_2$. This is the antecedent in the lemma with $k = 2$. F is therefore not realizable.

A Necessary and Sufficient Condition

Consider any Boolean function $F(x_1, \cdots, x_n)$. Let $v_1, v_2, \cdots, v_m$ denote all the vertices in $V_1(F)$ and $v_{m+1}, \cdots, v_{2^n}$ those in $V_0(F)$. A necessary and sufficient condition for realizability is: F is realizable if and only if, for any 2^n non-negative numbers $c_i \geq 0 (1 \leq i \leq 2^n)$, the relations

$$\sum_1^m c_i = \sum_{m+1}^{2^n} c_i$$

and

$$\sum_1^m c_i v_i = \sum_{m+1}^{2^n} c_i v_i \tag{5}$$

imply $c_i = 0$ for all $i = 1, 2, \cdots, 2^n$.

This condition is based on a theorem of Fan.[2]

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[2] K. Fan, "On systems of linear inequalities," in "Annals of Mathematics Studies No. 38," H. W. Kuhn and A. W. Tucker, Eds., Princeton University Press, Princeton, N. J.: 1956.

A 6-Megacycle Cryotron Ring Oscillator*

Better film cryotrons, resulting from improved evaporation techniques, have led to the design and construction of a 6-mc cryotron ring oscillator. Previous ring oscillators constructed at this laboratory have been limited in frequency to 200 kc.[1] The oscillator, shown in Fig. 1, is a three-stage, push-pull ring deposited on a quartz substrate. The controls are lead, 0.006 inch wide, and the gates are tin, 3000 Å thick and 0.062 inch wide. Data for the design of the oscillator were obtained from the measured dc characteristics of similar cryotrons. The significant design values for an operating temperature of 3.45°K are:

critical control current, $I_{crit} = 0.9$ ampere,
current gain, $G = 3$,
incremental current gain, μ, > 5,
gate resistance, $R = 1$ milliohm,
loop inductance, $2L = 4 \times 10^{-11}$ henry,
time constant, $L/R = 20$ μsec.

The measured supply voltage-current curve of the oscillator is shown in Fig. 2. At a, following a small rise in voltage due to the toe of the quenching characteristic, oscillation starts, and the supply voltage rises. Oscillation may now be maintained over a range from b to c. At c, thermal latching occurs, oscillation ceases and the circuit has a constant resistance of $3/2R$. From this curve, the gate resistance is 0.87 milliohm, slightly lower than the design value, and the critical current, as estimated from the range of oscillation, is approximately the design value. The maximum frequency of oscillation observed was 6 mc.

Calculations for a switching analysis of ring oscillators[2] were extended to cover three-stage oscillators, and the results are shown in Figs. 3 and 4. Data obtained from measurements on the oscillator at different operating temperatures are plotted on these graphs. A time constant of 25 μsec (rather than the design value, because of the lower gate resistance) and the design values of critical current were used to normalize the experimental data. The effective μ appears to be between 10 and ∞. A trend toward higher gain at lower temperature is clearly noticeable, and in general, the oscillator conforms well with the switching analysis. A slight drop in frequency at high supply currents was noticed, but this was probably a thermal effect rather than true second mode operation.

In the light of the results obtained with this oscillator, it appears that the discrepancies between circuit analysis and the observed operation of earlier five-stage ring oscillators[2] are readily explainable if these oscillators ran only on the toe of the quenching curve and never utilized the full gate re-

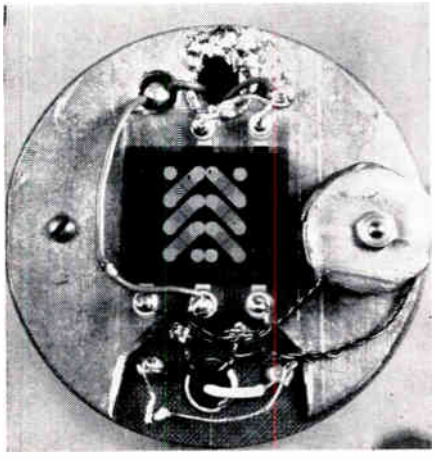

Fig. 1—Three-stage oscillator with output transformer.

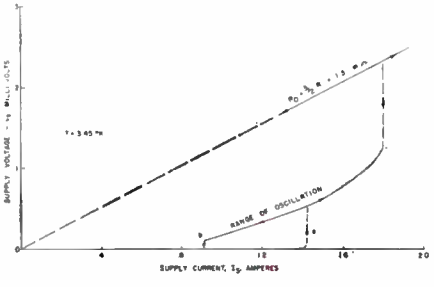

Fig. 2—Supply voltage—supply current characteristic.

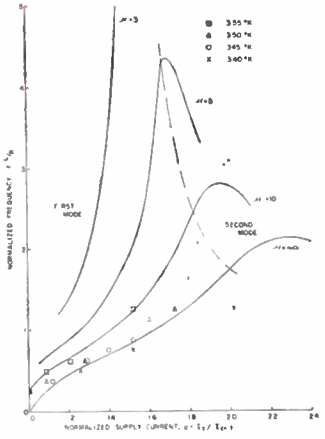

Fig. 3—Frequency vs supply current.

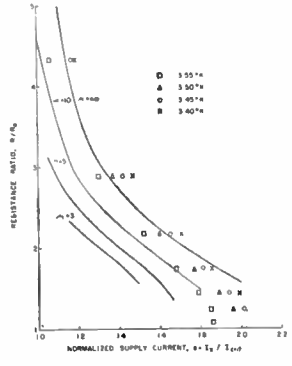

Fig. 4—Resistance ratio vs supply current.

* Received by the IRE, July 27, 1960. This work was supported by the U. S. Dept. of Defense.

[1] A. E. Slade, "Cryotron characteristics and circuit applications," Proc. IRE, vol. 48, pp. 1569–1576; September, 1960.

[2] M. L. Cohen, "An analysis of cryotron ring oscillators," Proc. IRE, vol. 48, pp. 1576–1583; September, 1960.

sistance. In this case, the linear analysis[2] is applicable, and the small toe resistance is compatible with the low frequency of oscillation and the computed circuit inductance.

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Gain Measurements on a Forward Wave Crossed-Field Amplifier*

The dependence of the electronic gain on the peak RF input power has been measured for a forward wave fundamental crossed-field amplifier with emitting sole. The tube is constructed in the normal magnetron cylindrical geometry, except that the RF circuit is nonre-entrant. The active length is 12 sections or approximately $4\frac{1}{2}$ circuit wavelengths. In the interaction region, the electron stream circulates from input to output from which point it drifts in a nonpropagating region for $\frac{1}{4}$ of the circumference and re-enters the input section. The RF circuit employed is a variant of the waveguide coupled slow-wave structures described by Feinstein and Collier.[1] The electronic gain G is defined as $G \equiv P(V)/P(O) = [P_{gen}+P(O)]/P(O) = 1+P_{gen}/P(O)$, where V is the anode to cathode voltage, $P(V)$ is peak output power with voltage on, $P(O)$ is peak output power with voltage off, and $P_{gen} = P(V)-P(O)$. $P(O)$ is related to the peak input power P_i by a constant factor A which is less than unity and accounts for cold loss between input and output. Therefore, $G = 1+P_{gen}/AP_i$; $(G-1) \propto P_{gen}/P_i$. It is interesting to consider the effect of the RF input power under two conditions: 1) constant peak anode-cathode voltage and 2) constant peak anode current. At all times, the magnetic field was constant at 4000 gauss and the frequency set at 9100 Mc. In Fig. 1, the operating voltage V is plotted against P_{gen} with P_i a parameter. The first order effect of an increase in RF input power ΔP_i is to lower by a fixed amount, ΔV, the operating voltage necessary to obtain a given value of P_{gen}. One may view this as a decrease in the extrapolated threshold voltage V_0. Thus, if a constant anode-cathode voltage is maintained, we find an increase in P_{gen} corresponding to an increase in P_i. Fig. 2 displays, on logarithmic paper, curves of P_{gen} vs P_i for several values of constant voltage V. The straight lines indicate a relation $P_{gen} \propto P_i^n$ for V=constant. The exponent n, given by the slopes of these lines, diminishes with increasing voltage. It is apparent that the dependence of P_{gen} on P_i is not very significant in the region of normal high level operation. Now let us consider the relation between G and P_i for constant peak current I. Fig. 3 is a plot, on logarithmic paper, of $G-1$ vs P_i for several values of constant current. The straight lines again indicate a relation $(G-1) \alpha P_i^n$ for I=constant. The slope, which is equal to -1, indicates that $(G-1) \propto P_i^{-1}$ so that P_{gen} is independent of P_i for constant anode current.

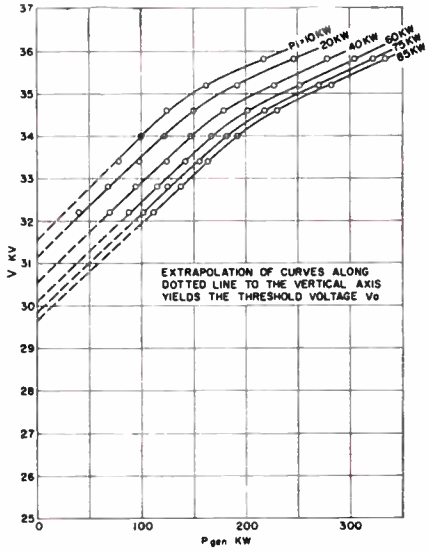

Fig. 1—Voltage vs generated power with peak RF input power as a parameter.

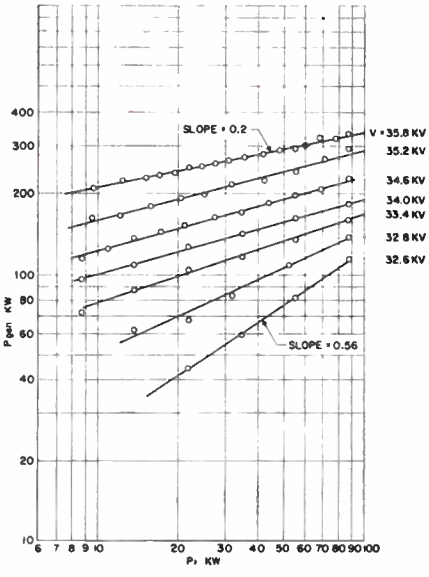

Fig. 2—Peak generated power vs peak RF input power plotted on logarithmic paper. Voltage is a parameter.

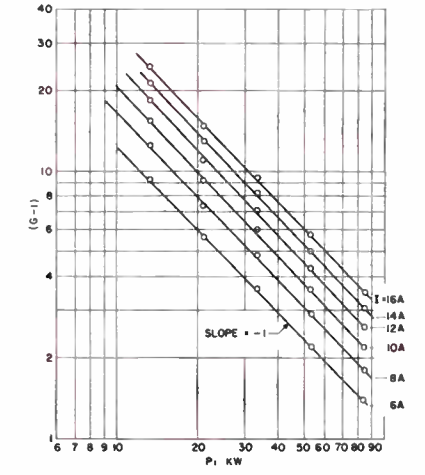

Fig. 3—A plot on logarithmic paper of (electronic gain -1) vs peak RF input power with peak current as the parameter.

We conclude that within the normal high-level operation range, the generated power depends only upon the peak current that can be drawn, the latter determined by the voltage beyond the threshold, $V-V_0$. Since the signal RF fields establish the proper electron spoke formation at the input of the tube, the operating frequency is set by the input frequency and the maximum generated power is limited by the magnitude of P_i. For a given electronic impedance there is a minimum value of P_i required for stability against mode competition. Finally, as shown above, the threshold voltage V_0 is an inverse function of P_i, P_{gen} is independent of P_i, and G is inversely proportional to P_i at constant current.

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The Measurement of Tunnel Diode Junction Capacitance*

It is the purpose of this discussion to consider the limitations and problems encountered in attempting to measure the junction capacitance of tunnel diodes, and to suggest a measurement technique which eliminates most of them.

In the literature,[1] the equivalent circuit shown in Fig. 1 has been analyzed, and it is shown that the apparent capacity looking into the device terminals is

$$C_{apparent} \cong C_{junction} + C_{strays} - L_s g_D^2. \quad (\text{When } \omega \ll g/c).$$

In addition, if a bias resistor suitable for biasing the tunnel diode into the negative-conductance region is used, and the inevitable inductance of the leads coupling the measuring node to the biased device is considered, then the capacitance measured by the bridge is shown to be (see Fig. 2):

$$C_{measured} \cong C_j + C_{strays} - L_{leads}(g_{bias}+g_D)^2 - L_s g_D^2.$$

Since the inductance of the leads to the bridge can easily be the dominant reactance in the circuit, the method described is seen to be subject to large potential errors, even when stringent efforts are made to keep all inductances to the irreducible minimum. Unfortunately, this method is necessary in order to measure the variation of junction capacitance with forward voltage in the

* Received by the IRE, August 3, 1960.
[1] J. Feinstein and R. J. Collier, "A class of waveguide-coupled slow-wave structures," IRE Trans. on Electron Devices, vol. ED-6, pp. 9–17; January, 1959.

* Received by the IRE, June 17, 1960.
[1] U. S. Davidsohn, Y. C. Hwang, and G. B. Ober, "Designing with tunnel diodes," *Electronic Design*; February 3, 17, 1960.

negative-conductance region, and was so described.[1,2]

One further item will be considered before discussing the measurement method to be proposed. From the stability analysis of the equivalent circuit,[1] one finds that for the tunnel diode to be stable in the negative-conductance region, then,

$$\frac{L_s|-g|}{C} < R_s < \frac{1}{|-g|}.$$

In other words, if the circuit inductance cannot be made less than $R_sC/|-g|$, the circuit must oscillate and any capacitance measured bears only a fortuitous resemblance to the actual capacity. (Even in the valley region, the measuring signal will drive the tunnel diode slightly into a region of some negative-conductance for part of the time, and the possibility of oscillations exists.)

Let us consider attempting to increase the bias resistor to the limit of $1/|-g|$ in order to improve the circuit stability. Then L_s *must* be less than C/g_D^2 (or conversely $C_j > L_s g_D^2$) or oscillations will persist and the circuit *cannot* be stabilized. Since the ultimate limits being considered vary as the square of the negative-conductance (a direct function of peak-point current), it is apparent that a test circuit which may be stabilized for a low-current tunnel diode will eventually become unstable for some higher-current device, because of the limitations of a fixed circuit and/or package inductance.

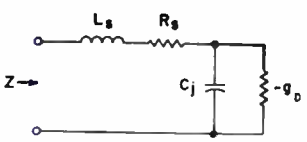

Fig. 1.

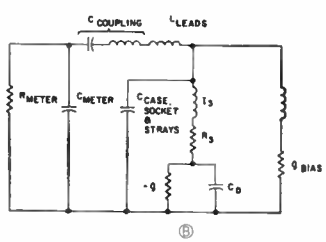

Fig. 2.

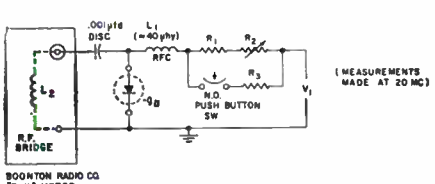

Fig. 3.

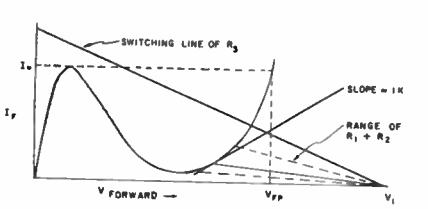

Fig. 4.

With the preceding considerations in mind, we see that the design of a test-circuit for measuring the capacitance of tunnel diodes over a large range of peak-point currents and g/c ratios can be accomplished only by deliberately violating *both* stability criteria simultaneously and forcing stability by using a switching load line to bias the device.

At this point, within the limitations that we will measure the sum of junction and distributed capacity (and can only measure over a small range of voltage around the valley voltage), the technique is very straight-forward and the test circuit shown in Fig. 3 is the result. Fig. 4 shows the region of operation.

Using the results of measurements of capacitance variation with voltage, made using the former method,[1] we can expect that the junction capacitance will vary approximately as

$$C \propto \frac{K}{[V_{\text{Band Gap}} - (V_{\text{Forward}} + V_{\text{Degeneracy}})]^{1/2}},$$

so that the somewhat smaller junction capacitance in the negative-conductance region may be easily calculated. (The case capacitance may be separately measured and subtracted from the measured quantity.)

It cannot be over-emphasized that the measuring signal across the tunnel diode must be kept to less than 10 millivolts to prevent errors resulting from the nonlinearity of the diode characteristics.

The RF choke (L_1) is used to decouple the bias network from the bridge. Since we are switching the tunnel diode, R_3 is used to supply a current somewhat greater than the peak—point current for the particular range of units being measured; R_1 need only be $>1/|-g|$ but is usually made several times this value to prevent oscillation near the valley region. R_2 is used to adjust the intercept point on the device characteristics so that the bridge measures a parallel positive resistance in the order of 1K ohm or greater. (The bridge lead inductance will still reduce the measured capacity somewhat by Lg_D^2, but, if the parallel resistance is 1K ohm or larger, it would require 1 μh of lead inductance to cause an error of 1 $\mu\mu$f in the reading. If care is taken in keeping lead lengths to less than one inch, the resultant error will be less than 0.2 $\mu\mu$f and can be neglected.)

The supply voltage (V_1) is usually in the order of 0.75 v for germanium and 1.5 v for gallium arsenide, and is supplied by one silicon diode, or two in series, as required.

L_2 is used to offset the bridge, if capacitances larger than 20 $\mu\mu$f are to be measured (0.27 μh will offset $\approx$20 $\mu\mu$f at the measuring frequency of 20 mc).

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[2] D. E. Thomas, "Esaki diode characterization," *1960 AIEE Winter General Meeting* (C. P.), February 4, 1960.

A Technique for Cascading Tunnel Diode Amplifiers*

The circuit presented by Chirlian[1] offers an intriguing possibility for cascading amplifier stages using ideal negative resistances. The analysis given for it is not adequate, however, if nonideal negative resistance devices represented by the circuit of Fig. 1 are used instead of the ideal negative resistances. Its inadequacy lies in the fact that it does not consider the problem of maintaining such a nonideal device at a stable operating point in its negative resistance region.

It will be shown here that the simple approach of separating bias and signal considerations leads one to the conclusion that the proposed cascading scheme cannot be used for tunnel-diode-like negative resistance devices. A more general treatment avoiding such a separation is inconclusive except to indicate that the circuit will only be useful at very high frequencies if it is useful at all. The problem of determining the stability of a circuit utilizing more than one nonideal negative resistance device in the ladder structure is vastly more complicated than any considered in this letter.

Let the circuit of Fig. 1 be used as one of the series elements in the ladder structure proposed by Chirlian[1] and assume that the impedances looking "backward" and "forward" along the ladder are ideal positive R's as in the idealized model. Following the simplifying idea of separating bias considerations from signal considerations, we may treat in turn two approximate equivalent circuits. The first is the "bias" equivalent circuit shown in Fig. 2. The second, which is the "signal" equivalent circuit, is shown in Fig. 3.

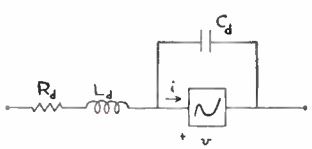

Fig. 1—Nonideal negative resistance model. $1/r = \partial i/\partial v$. r, L_d, and C_d are assumed constant near any possible operating point.

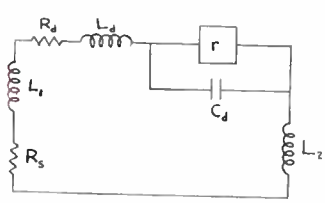

Fig. 2—Bias equivalent circuit. $L_T = L_1 + L_d + L_2$. $R_T = R_s = R_d$.

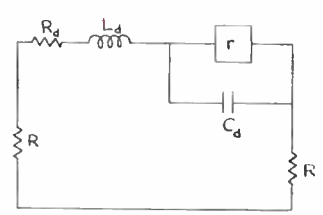

Fig. 3—Signal equivalent circuit. $R_T' = 2R + R_d$.

* Received by the IRE, June 28, 1960.

[1] P. M. Chirlian, "A technique for cascading tunnel diode amplifiers," Proc. IRE, vol. 48, p. 1156; June, 1960.

The natural frequencies of the circuit of Fig. 2 are the roots of:[2]

$$s^2 + \left(\frac{R_T}{L_T} + \frac{1}{rC_d}\right)s + \frac{1}{L_dC_d}\left(\frac{R_T}{r} + 1\right) = 0. \quad (1)$$

To permit a stable operating point for $r<0$, it is necessary that the two roots be either negative real or complex conjugates with a negative real part. The roots of (1) are:

$$s_{1,2} = -\frac{1}{2}\left(\frac{R_T}{L_T} + \frac{1}{rC_d}\right) \pm \sqrt{\left\{\frac{1}{2}\left(\frac{R_T}{L_T} + \frac{1}{rC_d}\right)\right\}^2 - \frac{1}{L_dC_d}\left(\frac{R_T}{r} + 1\right)}. \quad (2)$$

For stability, the following conditions must be fulfilled:

$$\frac{R_T}{|r|} < 1 \quad (3a)$$

$$\frac{R_T}{L_T} - \frac{1}{|r|C_d} > 0. \quad (3b)$$

The two conditions may be combined to give:

$$\frac{L_T}{|r|C_d} < R_T < |r|. \quad (4)$$

It is pertinent to determine the maximum total inductance permissible in the bias circuit, since this will determine, for a given tunnel diode, the minimum frequency at which the bias and signal circuits may be treated independently. Taking as a representative set of parameters those of a 1N2939, ($|r| = 100\ \Omega$, $C_d = 7$ pf, $L_d = 6$ mμh, $R_d = 1\ \Omega$) and assuming that the two external inductances in the bias circuit are equal, we can get some idea of the minimum frequency. It is assumed for now that the amplifier stage is operated at high gain, which means that the characteristic resistance of the ladder, R, is approximately equal to the magnitude of the negative resistance. To permit the maximum possible L for which a stable operating point is possible it is necessary to assume that resistance has been added in the bias loop to bring the total up to approximately the value of the magnitude of the negative resistance. Under these conditions, the maximum permissible total inductance is about 70 mμh and the frequency at which the reactance of half of this inductance equals R is ≈500 mc. This indicates that ordinary lumped circuit techniques will be unusable for such an amplifier stage, but it does not say that operation of the circuit is impossible.

Matters become even worse, however, when the "signal" equivalent circuit is considered. The natural frequencies of the circuit of Fig. 3 are the roots of:

$$s^2 + \left(\frac{R_T'}{L_d} + \frac{1}{rC_d}\right) + \frac{1}{L_dC_d}\left(\frac{R_T'}{r} + 1\right) = 0. \quad (5)$$

These roots are:

$$s_{1,2} = -\frac{1}{2}\left(\frac{R_T'}{L_d} + \frac{1}{rC_d}\right) \pm \sqrt{\left\{\frac{1}{2}\left(\frac{R_T'}{L_d} + \frac{1}{rC_d}\right)\right\}^2 - \frac{1}{L_dC_d}\left(\frac{R_T'}{r} + 1\right)}. \quad (6)$$

[2] W. J. Cunningham, "Introduction to Nonlinear Analysis," McGraw-Hill Book Co., Inc., New York, N. Y., ch. 5; 1958.

This is of the same form as (2) and yields restrictions similar in nature to (3a) and (3b) if a stable operating point is to be maintained:

$$\frac{R_T'}{|r|} < 1 \quad (7a)$$

$$\frac{R_T'}{L_d} - \frac{1}{|r|C_d} > 0. \quad (7b)$$

Referring now to the previous correspondence,[1] we note that the shunt elements in the ladder are given by:

$$-|r_1| = \frac{R(R - |r|)}{-|r|}. \quad (8)$$

(The absolute value signs have been added for consistency within this letter.) If the shunt element is to be negative as proposed, then $R-|r|$ must be positive. *But this violates the stability condition (7a).* It may be concluded from this discussion that (8), which is an essential condition for the realization of the proposed negative resistance ladder, is incompatible with the stable operation of a nonideal negative resistance model of the type of Fig. 1.

It may be argued at this point that the separation of the circuit into a bias and a signal equivalent circuit is questionable and that the foregoing conclusions are not necessarily valid. A complete equivalent circuit (retaining the assumption that the impedances looking up and down the ladder are ideal positive R's) of a typical stage in the proposed cascaded amplifier is given in Fig. 4. The natural frequencies of this circuit are the roots of a fifth-degree polynomial in s:

$$s^5 + \left(\frac{2R}{L_d} + \frac{1}{rC_d}\right)s^4 + \left\{\frac{1}{L_dC_d}\left(\frac{2R}{r} + 1\right) + \frac{2R^2}{LL_d}\right\}s^3 + \left\{\left(1 + \frac{R}{r}\right)\frac{2R}{LL_dC_d} + \frac{R^2R_d}{L^2L_d} + \frac{1}{rL_dC_dC}\right\}s^2 + \left\{\left(\frac{2R}{r} + 1\right)\frac{1}{LCL_dC_d} + \frac{R^2}{L^2L_dC_d}\right\}s + \frac{R}{L^2L_dCC_d} \quad (9)$$

where it has already been assumed that the following conditions hold:

$$\begin{aligned} L_1 &= L_2 = L \\ R_d &\ll R \\ R_d &\ll |r| \\ C_d &\ll C \\ L_d &\ll L. \end{aligned} \quad (10)$$

If there is to be a chance of stability, the coefficient of each power of s in (9) must be positive. Consider, for example, the s^3 term. Assuming R is approximately 100 ohms and using the parameters of the 1N2939, one finds that its coefficient is negative unless L is less than approximately 2×10^{-7} henries. This unfortunately leaves the possibility that the L may not be much less than L_d, as was assumed. This means that a more complicated polynomial must be considered to represent the system and makes impossible any quick conclusions about stability. It does tend to verify the conclusion reached in the simpler previous treatment in this letter that the circuit must be operated at very high frequencies if it is to operate at all.

The conclusions to be drawn from the foregoing discussion are:

1) If one presupposes the existence of a range of frequencies where bias and signal considerations may be separated and assumes attempted operation therein, the proposed cascading scheme cannot be used for nonideal negative resistance devices representable by the circuit of Fig. 1.
2) The more general approach in which bias and signal considerations are not separated offers no quick answer to the stability question.
3) With considerable effort, the fifth-degree polynomial whose roots determine the stability of the circuit of Fig. 4 could be investigated for the presence of roots in the right half plane (after inserting "typical" parameter values if necessary). This seems hardly worthwhile, however, since the circuit of real interest must contain more than one nonideal negative resistance device. This is a situation much more complex than any considered here.

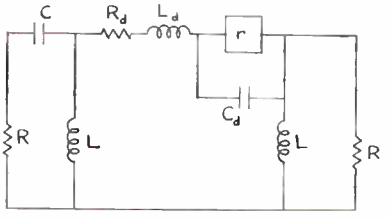

Fig. 4—Complete equivalent circuit for a typical stage.

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Author's Comment[3]

The contents referred to[1] were intended to present a basic procedure for obtaining cascaded amplifiers using tunnel diodes. The idea here was to use an "artificial transmission line" having negative resistance and conductance elements as an amplifier. Such a configuration will produce amplification instead of attenuation. Theoretical tunnel diodes (*i.e.*, negative resistances) were used in this analysis. Harbourt has indicated that when the complete equivalent circuit of the

[3] Received by the IRE, August 5, 1960.

tunnel diode is considered in the analysis the results indicate that oscillation will occur. Actually, as he states, Harbourt's analysis did not consider the complete circuit. The complete circuit must be considered before coming to any definite conclusion. However, it is quite possible that in this case stability will be difficult to obtain. Unfortunately I also have insufficient time, at present, to conduct a study of this problem.

More important is the fact that it can be shown that a stable amplifier can be obtained from the circuit mentioned[1] if some modifications are made. These will now be discussed. If each tunnel diode of Fig. 4(a)[1] is shunted by a small enough resistance, a stable device will result. Let us presume that it was originally unstable. This shunting would shift the poles from the right half of the complex plane into the left half plane. Thus, for appropriate values of the shunting resistances, all the poles will lie in the left half plane and one pair of poles can be as close to the $j\omega$ axis as desired. This produces any desired gain at a given frequency. Of course, if the cascade configuration is to provide an advantage over a single tunnel diode all the pole locations must be controlled with considerable freedom. In addition, the pole location is not the only factor that affects gain. The zero locations and the constant multiplier must also be considered. Thus, this amplifier configuration should be studied to see if arbitrary gains and passband response characteristics can be obtained. In addition, there are several other factors that could be investigated here. For instance, the tunnel diode could be shunted by networks other than simple resistances or the negative resistance of the tunnel diode could be varied by varying the bias.

Another technique, utilizing the artificial transmission line technique, that might prove useful is to modify the bias circuit of Fig. 4(a).[1] For instance, Hines[4] presents another bias circuit. Adoption of other such biasing procedures might reduce the stability problem. However, this must be investigated further before any conclusions can be reached.

It is hoped that this discussion will prove helpful in the realization of cascaded tunnel-diode amplifiers.

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[4] M. E. Hines, "High frequency negative resistance circuit principles for Esaki diode applications," *Bell Sys. Tech. J.*, vol. 39, pp. 477–513; May, 1960.

On the Choice of Constants in the Fourier Transform Pair*

The several definitions of the Fourier transform differ in the choice of constants which are associated with the transform pair.[1] It is the purpose of this note to call attention to the relation between the choice of the constants and the definition and properties of the energy spectral density function and the Laplace transform. In particular, it will be pointed out that the choice of definition and properties of either of the above functions is sufficient to specify the Fourier transform constants in cases where the Fourier transform and either the energy spectral density function or the Laplace transform are used in the same problem. It is noted that one set of frequently used definitions and properties is not self-consistent.

Assume that the Fourier transform pair is defined with arbitrary constants by

$$g(t) = a_1 \int_{-\infty}^{\infty} G(j\omega) e^{j\omega t} d\omega, \tag{1a}$$

$$G(j\omega) = a_2 \int_{-\infty}^{\infty} g(t) e^{-j\omega t} dt. \tag{1b}$$

Solving (1a) for $G(j\omega)$ yields, through a straightforward calculation,

$$G(j\omega) = \frac{1}{2\pi a_1} \int_{-\infty}^{\infty} g(t) e^{-j\omega t} dt \tag{2}$$

for all $g(t)$ for which (1a) and (1b) are appropriate. Comparing (2) with (1b), we may write

$$a_1 a_2 = \frac{1}{2\pi}, \tag{3}$$

which places one restraint on the choice of constants.

We now note that the total energy contained in $g(t)$ is given by

$$\text{energy in } g(t) = \int_{-\infty}^{\infty} |g(t)|^2 dt. \tag{4}$$

Through the use of (1a),

$$\int_{-\infty}^{\infty} |g(t)|^2 dt = \int_{-\infty}^{\infty} g(t) g^*(t) dt$$

$$= \int_{-\infty}^{\infty} g^*(t) a_1 \int_{-\infty}^{\infty} G(j\omega) e^{j\omega t} d\omega dt, \tag{5}$$

where $g^*(t)$ denotes the complex conjugate of $g(t)$. In cases where the order of integration can be interchanged,

$$\int_{-\infty}^{\infty} |g(t)|^2 dt = a_1 \int_{-\infty}^{\infty} G(j\omega) \int_{-\infty}^{\infty} g^*(t) e^{j\omega t} dt d\omega$$

$$= \frac{a_1}{a_2} \int_{-\infty}^{\infty} |G(j\omega)|^2 d\omega.$$

Using the result of (3), we may write

$$\text{energy in } g(t) = \int_{-\infty}^{\infty} |g(t)|^2 dt$$

$$= 2\pi a_1^2 \int_{-\infty}^{\infty} |G(j\omega)|^2 d\omega. \tag{6}$$

If we adopt the usual definition of energy spectral density function,[2]

$$E(\omega) = |G(j\omega)|^2, \tag{7}$$

and further require that the total energy computed in ω be equal to the energy computed in t, *i.e.*,

$$\int_{-\infty}^{\infty} |g(t)|^2 dt = \int_{-\infty}^{\infty} |G(j\omega)|^2 d\omega, \tag{8}$$

then the constant a_1 is clearly fixed at

$$a_1 = \frac{1}{\sqrt{2\pi}}. \tag{9}$$

On the other hand, if we make the standard requirement that the Laplace transform, universally defined as

$$L\{g(t)\} = \int_{-\infty}^{\infty} g(t) e^{-st} dt, \tag{10}$$

shall reduce to the Fourier transform [for suitably restricted $g(t)$] when the real part of s vanishes, then by comparing (10) with (1b) it is clear that

$$a_1 = \frac{1}{2\pi}. \tag{11}$$

We note that in this case the energy relations become

$$\int_{-\infty}^{\infty} |g(t)|^2 dt = \frac{1}{2\pi} \int_{-\infty}^{\infty} |G(j\omega)|^2 d\omega$$

$$= \frac{1}{2\pi} \int_{-\infty}^{\infty} E(\omega) d\omega. \tag{12}$$

Note that if a_1 is chosen as $1/\sqrt{2\pi}$, the Laplace transform does not reduce to the Fourier transform. On the other hand, if a_1 is chosen as $1/2\pi$, the integral over all ω of the energy spectral density (using the usual definition) does not equal the energy computed from the time function.

The following example will illustrate the difficulty that can be encountered. Consider a signal $f_1(t)$ applied to a linear passive network with output $f_2(t)$. Let it be required to compute the output energy by integration of the output energy spectral density function. We can describe the network by its transfer function which is derived through use of the Laplace transform. If we denote this transfer function by $H(s)$, and the spectra of $f_1(t)$ and $f_2(t)$ by $F_1(j\omega)$ and $F_2(j\omega)$, respectively, it is usually accepted that

$$F_2(j\omega) = H(j\omega) F_1(j\omega).$$

Furthermore, the output energy is usually considered to be given by

$$\text{output energy} = \int_{-\infty}^{\infty} |H(j\omega) F_1(j\omega)|^2 d\omega. \tag{13}$$

This expression for output energy is not correct if the Laplace transform is defined in the standard way.

As pointed out above, the standard definition of the Laplace transform forces the choice

$$a_1 = \frac{1}{2\pi}$$

* Received by the IRE, July 15, 1960.

[1] For the more common choices, see the following: R. V. Churchill, "Modern Operational Mathematics in Engineering," McGraw-Hill Book Co., Inc., New York, N. Y., and London, England; 1944. C. R. Wiley, Jr., Advanced Engineering Mathematics," McGraw-Hill Book Co., Inc., New York, N. Y., Toronto, Canada, and London, England; 1951. C. H. Page, "Physical Mathematics," D. Van Nostrand Co., Inc., Princeton, N. J., 1955.

[2] M. Schwartz, "Information Transmission, Modulation and Noise," McGraw-Hill Book Co., Inc., New York, N. Y., Toronto, Canada, and London, England; 1959.

in the Fourier transform pair. Thus from (12) the output energy is given by

$$\text{output energy} = \frac{1}{2\pi}\int_{-\infty}^{\infty} |H(j\omega)F_1(j\omega)|^2 d\omega,$$

and not by (13) above.

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On the Definition of Noise Performance*

Confusion in the literature exists in the representation of noise generated by linear twoports. The problem lies in the use of noise factor (noise figure), the original and still the most common definition of noise performance. A major source of the confusion in the use of noise factor stems from the presence of the standard noise temperature T_0, which is a necessary, though arbitrary, element of the definition. A common mistake is to use standard noise temperature indiscriminately for noise temperature of the input termination and/or of the transducer itself. But even when used correctly, the noise factor of a transducer is not a direct indication of noise generated within it, with the result that a variety of other terms have sprung into use, terms such as excess noise factor,[1] excess noise temperature,[2] and effective noise temperature,[3] because of the inadequacy of this definition. With the advent of low-noise receivers arising from maser and parametric amplification, and space vehicles operating in a variable temperature environment, the use of effective noise temperature is becoming increasingly common. Recently, the IRE adopted[4] a new definition of noise performance, called the "effective input noise temperature," which is free of the sources of confusion inherent in the definition of noise factor. But instead of withdrawing the term noise factor, this term still remains the prevailing IRE standard definition, with effective input noise temperature offered only as an alternative. In fact, the 1959 IRE Standards on Methods of Measuring Noise in Linear Twoports[4] is based exclusively on the use of noise factor as the measure of performance. The purpose of this letter is to point out the failings inherent in the use of noise factor and to make a plea for the universal adoption of effective input noise temperature.

The noise factor of a transducer at any given frequency is defined[5] as the ratio of the output to the amplified input available noise power per unit bandwidth when the input resistance is at the IRE Standard Noise Temperature 200°K. I submit that this is a most unfortunate definition on several counts and one that should be abandoned as soon as possible. First, and foremost, the definition implies a basic misconception as to the mechanism of noise generation by a transducer. By its very form, the term noise *factor* implies that the mechanism of the transducer is a *multiplicative* process and, hence, that the noise property of a transducer is to act as some kind of a noise amplifier whose noise power output is proportional to the noise power input. This implication is strengthened by the fact that noise factor is usually expressed in decibels, implying to the uninitiated that the over-all noise factor of a chain of transducers is the product of noise factors of the individual transducers. Nothing could be further from the truth! Although a transducer does, in fact, amplify the noise input, the noise power contributed by the transducer itself is strictly additive. It is generated independently of the input noise source and added to the power from the noise source. Second is the fact that this definition requires the introduction of a standard noise temperature that is arbitrary and physically meaningless (unless it can be argued that room temperature is meaningful because it is so common). Third, the degradation in signal reproduction caused by noise from the transducer cannot be compared directly to that caused by noise from the input termination because the two representations of noise are different dimensionally; noise factor is dimensionless, being a power ratio that is expressible either as a pure number or in decibels, whereas noise from the input termination is expressed directly in terms of power per unit bandwidth (usually as the temperature of a resistor). And last, calculations involving the use of noise factor are unnecessarily complicated because the noise power introduced by the standard temperature noise source nearly always must be subtracted again.

The newly adopted definition of noise performance,[4] effective input noise temperature, is that temperature of the input termination that would produce the same output noise power from an identical noise-free transducer as would the actual transducer if the temperature of the input were reduced to absolute zero. This definition describes a physically correct interpretation of the source of transducer noise. Furthermore, effective input noise temperature is an absolute measure of noise generated because it is referred directly to a standard temperature of absolute zero instead of being referred to an arbitrarily chosen standard temperature, and is measured in the same units as noise from the input termination. It has the additional advantage of proportionality; a transducer that is twice as noisy as another will have twice its effective input noise temperature.

Effective input noise temperature is a natural definition of noise performance; it appears in all calculations of output noise power at input temperatures different from the arbitrary standard T_0, even when using the noise factor definition:

$$N_{out} = FGkT_0B - GkT_0B + GkT_{in}B.$$

The first two terms together represent noise power generated within the transducer, the first term representing the total power when the input termination is at the standard temperature T_0 and the second term representing the contribution at T_0 from the input termination alone. Combining the first two terms,

$$N_{out} = GkB[(F-1)T_0 + T_{in}].$$

The term $(F-1)T_0$ is, by definition, the effective input noise temperature T_e. This emphasizes once again the artificiality of noise factor as a definition of noise performance. Noise performance of a transducer has significance only when the noise power generated within it is compared with that from the input noise source. Dr. D. O. North, the originator of the term noise factor, was well aware of this essential fact. In a published discussion on the subject of noise factor, he emphasized that "the improvement in performance represented by a reduction in noise factor *cannot be evaluated at all* without the temperature of the input termination for reference"[6] (italics were his).

There is no need for two equivalent definitions of noise performance when one of the two is deceptive and a source of confusion. Noise factor should be abandoned and effective input noise temperature adopted as the universal standard definition.

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* Received by the IRE, May 18, 1960.

[1] C. T. McCoy, "Present and future capabilities of microwave crystal receivers," PROC. IRE, vol. 46, p. 61; January, 1958.

[2] P. D. Strum, "Some aspects of mixer crystal performance," PROC. IRE, vol. 41, p. 883; July, 1953.

[3] J. P. Gordon and L. D. White, "Noise in maser amplifiers—theory and experiment," PROC. IRE, vol. 46, p. 1588; September, 1958.

[4] "IRE standards on methods of measuring noise in linear twoports, 1959," PROC. IRE, vol. 48, pp. 60–68; January, 1960.

[5] "IRE standards on electron tubes: definitions of terms, 1957," PROC. IRE, vol. 45, p. 1000; July, 1957.

[6] D. O. North, Discussion on "Noise figures of radio receivers," PROC. IRE, vol. 33, pp. 125–126; February, 1945.

Comment on "On the Definition of Noise Performance"*

The correspondence from Mr. D. R. Rhodes brings into focus an important controversy which deserves wider discussion in the literature. The fact that the *effective input noise temperature* (T_e) is more suited to some applications than *noise factor* or *noise figure* (F) will be readily admitted by many in the field of extremely low-noise devices or systems. It may well be that the time has come when standards should be written for the measurement of noise by radiometric

* Received by the IRE, June 23, 1960.

techniques. However, there remain a number of applications for which the noise figure concept is adequate and in some ways more desirable than the concept of effective input noise temperature. It would be a disservice to many working with these applications to abandon the definition of noise figure. Thus it can be argued that both definitions should be preserved. At the same time, a wider understanding of the two concepts should be promoted.

It is but a slight burden on the user to acquire a familiarity with both concepts or to convert from one to the other:

$$T_e = (F - 1)290^\circ \text{ K}$$

$$F = 1 + \frac{T_e}{290}.$$

Basically, the two concepts differ in only two respects:

1) *Noise figure* is based on a reference temperature of 290°K (approximately room temperature) while *effective input noise temperature* uses absolute zero as a reference.
2) *Noise figure* includes the noise contribution from the source impedance (at a standard temperature of 290°K) while this noise is excluded in the definition of *effective input noise temperature*. (This is not to say, however, that effective input noise temperature is independent of the input termination. The noise performance of a device, in general, depends on the *impedance* of the source to which it is connected.)

The second item leads to the appearance of a "1" in each of the two formulas above. As Mr. Rhodes points out, the noise from the standard temperature source in some cases is subtracted. Some writers have used the term excess noise figure $(F-1)$ to represent the remaining noise, although effective input noise temperature appears to present certain advantages in some applications.

The quotation which Mr. Rhodes gives from D. O. North that "the improvement in performance represented by a reduction in noise factor *cannot be evaluated at all* without the temperature of the input termination for reference" applies to the effective input noise temperature as well. A 10°K improvement in the effective input noise temperature of a receiving system, although of considerable significance in space communications with low-temperature background noise, would represent a negligible improvement in an application such as a point-to-point ground-based radio relay system where the background noise temperature is of the order of 290°K.

In summary, I feel that there are sufficient applications in which the source is at or near "room temperature" to justify retaining the historically familiar noise figure definition. At the same time, effective input noise temperature is an extremely useful concept for an increasing number of low-noise applications and deserves equal acceptance. The existence in the Standards of two representations of noise performance seems to me desirable since their areas of usefulness differ.

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IRE 7.9

Simplified Cesium Frequency Stabilizer*

Atomic hyperfine transitions have been used by many laboratories in atomic beam frequency standards or optically pumped systems. A simplified frequency standard using the ground state hyperfine splitting of the cesium atom is being constructed by utilizing the direct detection of the microwave emission from an optically pumped cesium cell placed in a suitable cavity. In the simplified energy level diagram (Fig. 1) of the cesium atom, it is seen that if the population of the $F=4$ level of the ground state can be increased over the population of the $F=3$ level, then a net emission at a frequency of 9192.631 mc may be obtained. By suitable filtering and polarizing of the cesium 8521.1Å line used for pumping, and the application of moderate magnetic fields, a very monochromatic stable signal source may be obtained. Although the power is quite low, several schemes could allow the use of the radiation as a very stable frequency standard; for instance, by direct amplification of the signal by a maser and a TWT amplifier. An alternate scheme, whereby a signal of sufficient strength may be obtained, is shown in Fig. 2.

The use of such a system depends upon the detection of the emitted radiation at 9192 mc. Fig. 3 shows the system whereby this signal has been detected.

Light from a 10-watt cesium lamp is passed through a type B1 filter, which rejects the 8943 Å line and passes the 8521Å line after which it is polarized. This polarized light is used to excite a cylindrical resonant cavity ($Q \approx 4000$), operating in the TE_{011} mode at 9192.63 mc, which contains a quartz cell with cesium vapor in it. This cell is made by reducing the pressure to 10^{-7} mm of mercury, inserting a small amount of cesium metal, and then filling it with a mixture of argon and nitrogen gases, which brings the pressure up to the order of 5 mm.

A signal from a 50 cps generator is fed into a ferrite modulator so as to modulate the RF originating in the cavity caused by the cesium transition. The modulated RF passes through two ferrite isolators into a balanced mixer using a type V-201B klystron, tuned to 9162.63 mc by means of a counter, as the local oscillator. The purpose of the isolator is to insure that no modulation of the local oscillator can occur. The 30-mc signal from the balanced mixer is fed into a low-noise, high-gain intermediate frequency amplifier, which in turn feeds a lock-in amplifier of the type described by Strandberg, *et al.*[1] The lock-in amplifier is used with a time constant of 20 seconds, and the receiving system has an available sensitivity of −135 dbm. The power output from the cavity is −120 dbm. No optimization procedures have as yet been carried out.

* Received by the IRE, August 1, 1960.

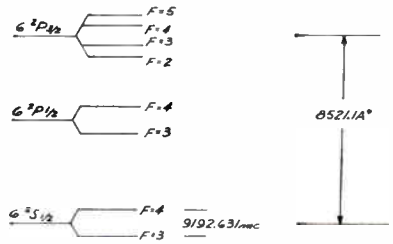

Fig. 1—Energy levels of cesium atom.

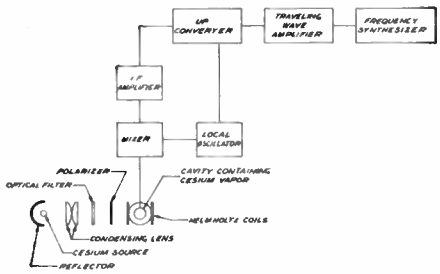

Fig. 2—Proposed stable source.

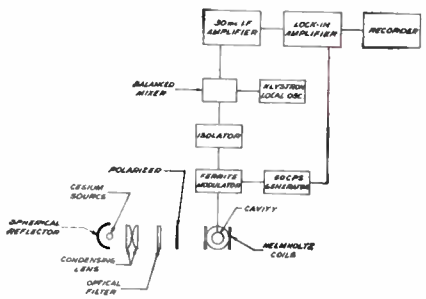

Fig. 3—System used to detect cesium emission.

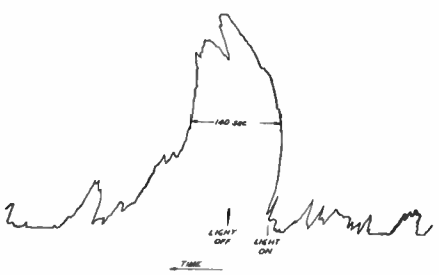

Fig. 4—Recorder trace of cesium emission line.

[1] M. W. P. Strandberg, M. Tinkham, I. H. Solt and C. F. Davis, "Recording magnetic-resonance spectrometer," *Rev. Sci. Instr.*, vol. 27, pp. 596–605; August, 1956.

The output of the lock-in amplifier drives a standard Esterline Angus recording milliammeter.

Thus far, it has not been possible to determine which m_F values are involved in the transition. Since these initial measurements have been made with an unstabilized klystron, all components within the bandwidth of the IF amplifier will be detected. In Fig. 4, a typical recorder trace of the detected signal is shown; the long time constant of the lock-in amplifier accounts for the time required, after turning off the light, for the signal to return to zero. The effect is observed whether one uses the filter and polarizer or not. Since magnetic fields in the vicinity of the cavity will remove or broaden transitions involving $m_F \neq 0$, the radiation observed is believed to be caused by the transition $F=4$, $m_F=0 \rightarrow F=3$, $m_F=0$.

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Further Developments in Tapered Ladder Antennas*

Several types of very broad-band "logarithmically periodic" antennas have been introduced recently, one of which is the tapered ladder.[1] Initial models of this antenna exhibited large impedance variations, but by changing the distributed capacitance across the twin-conductor excitation section we have been able to control the nominal input impedance as well as minimize its variations with change in frequency. This improvement has been achieved by placing a conducting plate structure along the longitudinal axis of the antenna as shown in Fig. 1. The nominal impedance is adjustable between 35 and 100 ohms by variation of the plate structure. The figure shows a 50-ohm model.

Fig. 1—Photograph of 50-ohm tapered ladder.

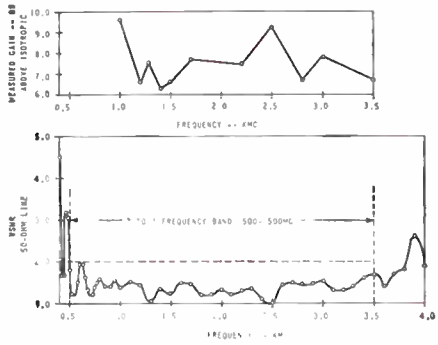

Fig. 2—VSWR and measured gain of 50-ohm tapered ladder.

The VSWR and measured gain of the 50-ohm model are shown in Fig. 2 over a 7:1 frequency band. The E- and H-plane patterns are approximately frequency independent and have half-power beamwidths of 60° and 100°, respectively. This model is excited from a coaxial line placed inside one conductor of the two-wire line.

Since the tapered ladder is symmetrical, it is possible to excite half the structure over a ground plane. A sketch of such an antenna is shown in Fig. 3. E- and H-plane radiation patterns of a working model are shown in Fig. 4. The patterns shown are for the midpoint and extremities of the 600- to 2000-Mc frequency range, and those designated as H-plane are actually conical cuts inclined approximately 10° to the ground plane. The antenna VSWR referred to 50 ohms is less than 1.8:1 over almost a 4:1 frequency band, and its average value is less than 1.4:1.

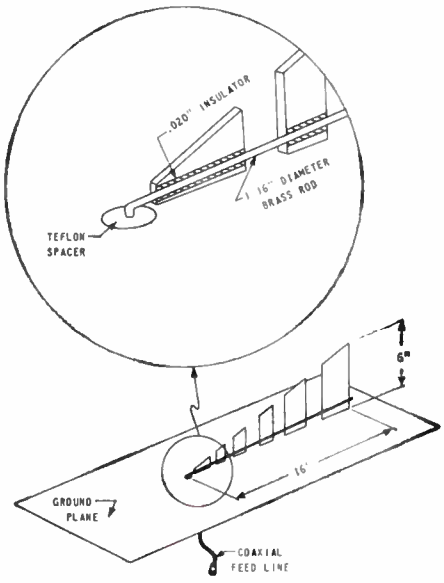

Fig. 3—Sketch of a tapered ladder—ground plane antenna.

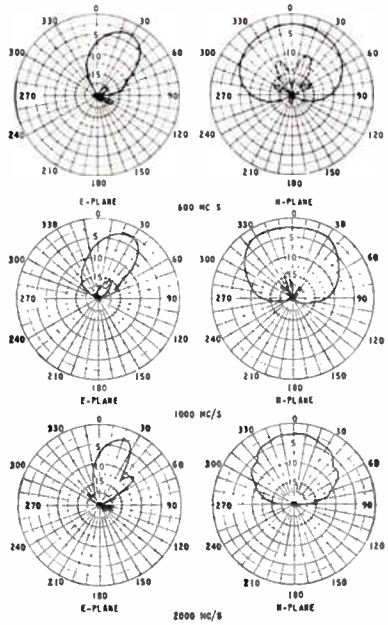

Fig. 4—Radiation patterns of tapered ladder—ground plane antenna at mid-point and near extremities of its frequency range. (Relative power in db.)

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Comments on the History of Parametric Transducers*

With regard to the interesting paper of W. W. Mumford,[1] I would like to give some additional information about the historical development of nonlinear devices in Germany.

In full acknowledgement of the work of L. Kühn, I would like to mention that in 1913,[2] independently from Kühn, I used a nonlinear inductance with iron core in a somewhat different construction and arrangement for the modulation of the high frequency alternator of Goldschmidt.[3] In these experiments the high frequency energy was modulated by speech and music. The work, which was interrupted by World War I, continued in 1920 using a nonlinear inductance for the modulation of the Poulsen arc-transmitter (15 kW). In these experiments a telephony-transmission over the distance of 1700 km (Berlin to Moscow) was reached.

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* Received by the IRE, August 12, 1960. The work described in this letter has been supported by the Signal Corps under Contract DA 36-039 SC-78281.

[1] A. F. Wickersham, Jr., "Recent developments in very broadband end-fire arrays" (Correspondence), Proc. IRE, vol. 48, pp. 794–795; April, 1960.

* Received by the IRE, September 2, 1960.

[1] W. W. Mumford, "Some notes on the history of parametric transducers," Proc. IRE, vol. 48, pp. 848–853; May, 1960.

[2] L. Pungs, German Patents: No. DRP 281440, issued July 15, 1913; No. 58822, issued October 10, 1913.

[3] L. Pungs, "Die Steuerung von Hochfrequenzströmen durch Eisendrosseln mit überlagerter Magnetisierung," *Elektrotech. Z.*, vol. 44, pp. 78–81; January, 1923.

WWV and WWVH Standard Frequency and Time Transmissions*

The frequencies of the National Bureau of Standards radio stations WWV and WWVH are kept in agreement with respect to each other and have been maintained as constant as possible with respect to an improved United States Frequency Standard (USFS) since December 1, 1957.

The nominal broadcast frequencies should, for the purpose of highly accurate scientific measurements, or of establishing high uniformity among frequencies, or for removing unavoidable variations in the broadcast frequencies, be corrected to the value of the USFS, as indicated in the table below.

WWV Frequency
With Respect to U. S. Frequency Standard

1960 October 1600 UT	Parts in 10^{10}*
1	−147
2	−147
3	−146
4	−146
5†	−146
6	−148
7	−148
8	−148
9	−147
10	−148
11	−148
12	−148
13	−148
14	−148
15	−148
16	−148
17	−148
18	−148
19	−148
20	−148
21	−148
22	−148
23	−148
24	−148
25	−148
26	−147
27	−147
28	−147
29†	−146
30	−148
31	−148

* A minus sign indicates that the broadcast frequency was low.
† The method of averaging is such that an adjustment of frequency appears on the day it is made. The frequency was decreased 3×10^{-10} on October 5; and decreased 21×10^{-10} on October 29.

The characteristics of the USFS, and its relation to time scales such as ET and UT2, have been described in a previous issue,[1] to which the reader is referred for a complete discussion.

The WWV and WWVH time signals are also kept in agreement with each other. In addition, they are locked to the nominal frequency of the transmissions and consequently may depart continuously from UT2. Corrections are determined and published by the U. S. Naval Observatory. The broadcast signals are maintained in close agreement with UT2 by properly offsetting the broadcast frequency from the USFS at the beginning of each year when necessary. This new system was commenced on January 1, 1960. A retardation time adjustment of 20 milliseconds was made on December 16, 1959; another retardation adjustment of 5 milliseconds was made at 0000 UT on January 1, 1960.

* Received by the IRE, December 1, 1960.
[1] "National standards of time and frequency in the United States," Proc. IRE, vol. 48, pp. 105–106; January, 1960.

Notice of Time Signal Adjustment WWV/WWVH New Timing Code on WWV

In order to bring the time signals of WWV/WWVH and other stations into closer agreement, a retardation phase adjustment of the time signals radiated by WWV/WWVH is planned at 0000 UT on January 1, 1961. The retardation will be precisely 5 milliseconds.

It is expected that such adjustments in the time signals will be made as infrequently as possible and preferably at the beginning of each calendar year when necessary. The time signals are locked to the broadcast frequency.

In 1961 it is planned to maintain the frequency stable to 1 part in 10^{10} and at the same offset value as before, *i.e.*, −150 parts in 10^{10} with reference to the United States Frequency Standard.

The necessity for offsetting the frequency and for adjustment of the time signals is described in "National Standards of Time and Frequency in the United States," Proc. IRE, vol. 48, pp. 105–106, January, 1960, and "Co-Ordination of Time and Frequency Transmissions," *J. IEE*, vol. 6, no. 65, p. 268; May, 1960.

On January 1, 1961, the National Bureau of Standards will commence a regular broadcast from WWV of a timing code which gives the day, hour, minute, and second (Universal Time), and which is locked in phase to the frequency and time signals. The code is a 36 Binary Digit 100 PPS Code carried on 1000-cps modulation. A complete time frame is 1 second. The code will be broadcast for 1-minute intervals and 10 times per hour. Except at the beginning of each hour, it immediately follows the standard frequencies of 440 cps and 600 cps. The code was broadcast experimentally during the interval April to August, 1960, and is described in "Experimental Timing Code Added to WWV Broadcasts," NBS *Tech. News Bull.*, vol. 44, no. 7, pp. 114–115; July, 1960.

An announcement, "Time Code on WWV," is available on request.

National Bureau of Standards
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Stability Criterion for Amplifier Moving in Space*

The linear network formula for feedback,

$$A(s_1) = \frac{A_i(s_1)}{1 - H(s_2)A_i(s_1)}, \qquad (1)$$

with $s_1 = s_2 = j\omega_1$, and with $H(s_2)A_i(s_1) = 1$ designating the point of instability, can, with $s_1 \neq s_2$, be extended to cover the case when the amplifier of inherent amplification, $A_i(s_1)$, moves in space with the velocity v. The feedback path is then a radiation path with sufficient reflected power to make the stimulance, or negative resistance, compensate for the system loss.[1] To make the formula apply, we must take into account the Doppler frequency shift, and we will find that for $v \ll c$, a linear system is able to repeatedly reach the instability point at a repetition rate dependent upon the Doppler shift $2v/\lambda_1$, where $\lambda_1 = 1/f_1$ and where c is the velocity of light. We may formulate a stability criterion during any brief interval of assumed steady-state condition by means of the straight-forward network transformation

$$H(s_2) \rightarrow R_N(s_2) \rightarrow R_{N\,eq}(s_1) \rightarrow H(s_1)_{eq}. \qquad (2)$$

Here $H(s_2)$ is the feedback transfer function for a feedback path exposed to Doppler shift. It is interpreted as the stimulance $R_N(s_2)$ of return frequency $\omega_2/2\pi$, transformed into the equivalent stimulance $R_{Neq}(s_1)$ of signal frequency $\omega_1/2\pi$. Finally, this stimulance is interpreted as a feedback factor, so that the entire system can be treated as a single frequency system. We may formulate the following criterion: *A linear feedback system, in space, with radiation type feedback and an amplifier moving with a velocity v, very much less than that of light, remains stable when the return frequency differs from the transient generated output frequency by the Doppler shift $2v/\lambda_1$, unless $H(s_2)A_i(s_1) = H(s_1)_{eq}A_i(s_1) = 1$, where $H(s_1)_{eq}$ is defined by the requirement that the corresponding stimulance covers the system loss.* The transformation, (2), implies the insertion of a fictitious frequency converter into the system, to make possible the treatment of Doppler stimulance at signal frequency. If a network element in form of a real frequency converter is inserted, as in Fig. 1,

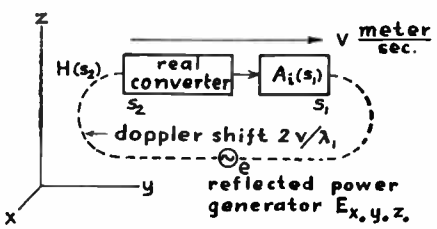

Fig. 1.

so that the return frequency becomes $(f+2v/\lambda_1)-2v/\lambda_1$, the system may oscillate much more readily, and steadily, since the intermittent operation will cease. It follows that a real frequency converter may be preset so as to substantiate oscillations at one specified Doppler shift, $2v/\lambda_1$ only, if and when this shift occurs. This phenomenon may be utilized for the control of missiles.

We may note that the instability point of the entire system above is predicted by linear network theory, including the converter, which accomplishes multiplicative mixing acting as a parametric device.

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* Received by the IRE, August 2, 1960.
[1] H. Stockman, "Communications by means of reflected power," Proc. IRE, vol. 36, pp. 1196–1204; October, 1948.

The Scattering of Short Electromagnetic Pulses by a Conducting Sphere*

In a previous paper, the back-scattered waveform caused by an impulsive incident electromagnetic wave was approximated from elementary considerations of physical optics and Rayleigh scattering, for the case of a perfectly conducting sphere and prolate spheroid.[1] The results were encouraging, but there appeared to be no available solutions for some simple body which could be used as a model for the approximating waveform.

To this end, the diffraction of short electromagnetic pulses by a perfectly conducting sphere was studied. Using calculated values for the phase and amplitude of the scattered field at a number of frequencies, the scattering by a periodic train of short pulses could be determined. Such values were furnished by Cornell Aeronautical Laboratory for the range of ka (circumference in wavelength) from 0.25 to 16.0 in steps of 0.25, at scattering angles from 0° to 180° in steps of 30°. An incident pulse train is obtained by superposition of monochromatic waves at each of these frequencies. The pulse width at base is 0.392τ, where τ is the transit time for the distance of one sphere diameter. The separation of pulses in the periodic train is 12.58τ.

The waveforms obtained for the scattered fields are shown in Fig. 1, together with one member of the incident pulse train. A plan view of the scattered E- or H-field waveform is shown plotted transverse to the direction of propagation, as the associated field vector would point. This yields a sort of "snapshot" of the waveforms in space, with all dimensions to scale, except the distance to the sphere. The concentric circle indicates the locus of points on the waveforms corresponding to virtual reflections at the center of the sphere, and it is seen that the back-scattered waveform, for example, has a peak one diameter in advance of this (corresponding to reflection from the near side of the sphere). The amplitudes of the scattered field waveforms have been normalized by a multiplicative factor of $2(R/a)$, where R is the distance to the center of the sphere, and a is the sphere radius.

In each case, the scattered waveform consists of an initial spike which could be predicted by geometrical optics. This is followed by one or more peaks, corresponding very closely in the E plane to replicas of the incident pulse which have traveled around parts of the spherical surface in the manner predicted by the geometrical theory of diffraction.[2] In the back-scattering hemisphere, it appears that the waveforms shown furnish good approximations to those obtained for an impulsive incident wave; while for the forward hemisphere, shorter pulse lengths (and larger ka values) would be required for additional resolution. The waveforms shown permit good estimates to be obtained for the exponential decay of the geometrically diffracted pulses, as well as the transit time. A complete discussion of the results will be included in a forthcoming paper. One further observation may be of interest. The approximate solution for an impulsive plane wave described in our earlier paper was used to predict the back-scattered waveform for the given pulse train. A comparison of the exact and approximate solutions is given in Fig. 2.

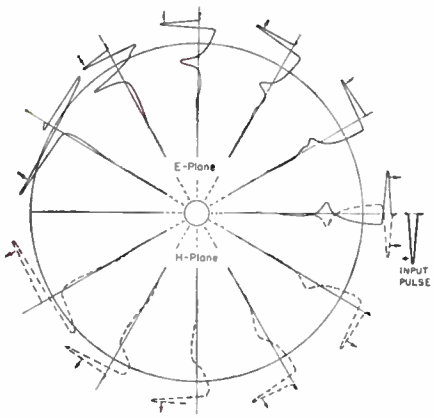

Fig. 1—Scattering of short electromagnetic pulses by a perfectly conducting sphere.

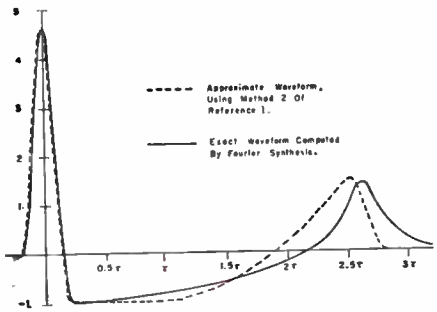

Fig. 2—Back-scattered waveform for a perfectly conducting sphere.

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* Received by the IRE, August 17, 1960.

[1] E. M. Kennaugh and R. L. Cosgriff, "The use of impulse response in electromagnetic scattering problems," 1958 IRE National Convention Record, pt. 1, pp. 72–77.

[2] J. B. Keller, "A geometrical theory of diffraction," *Proc. Symp. in Applied Mathematics*, vol. 8, pp. 27–52, McGraw-Hill Book Co., Inc., New York, N. Y.; 1958.

The Significance of Transients and Steady-State Behavior in Nonlinear Systems*

Wolf's[1] comments on Doba's[2] recent correspondence seem to require clarification. Wolf states that a dormant linear system having a weighting function $k(\tau)$ when excited by an input $g_1(t)$, will produce the response:

$$g_2(t) = \int_0^t k(\tau)g_1(t-\tau)d\tau = \int_0^\infty k(\tau)g_1(t-\tau)d\tau - \int_t^\infty k(\tau)g_1(t-\tau)d\tau, \quad (1)$$

where

$$g_1(t) = 0 \qquad \text{for } t < 0. \quad (2)$$

The first integral, as is well known, represents the total response of the system. The integrals on the right, according to Wolf, represent the steady state (or particular solution) and the transient (or complementary solution), respectively. As Doba insists, however, the final integral of (1) must vanish if (2) is valid since $\tau > t$ in this integral. A restatement of (1) with an alternate expression for $g_1(t)$ will, I believe, avoid this difficulty in interpretation of (1).

Let

$$g_1(t) = g_1'(t)u(t), \quad (3a)$$

where

$$u(t) = \begin{cases} 1, & t \geq 0 \\ 0, & t < 0 \end{cases}; \quad (3b)$$

then

$$g_2(t) = \int_0^\infty k(\tau)g_1'(t-\tau)u(t-\tau)d\tau = \int_0^t k(\tau)g_1'(t-\tau)d\tau = \int_0^\infty k(\tau)g_1'(t-\tau)d\tau - \int_t^\infty k(\tau)g_1'(t-\tau)d\tau. \quad (4)$$

Eq. (4) is a more precise statement than (1) and clearly shows that $g_1'(t)$ rather than $g_1(t)$ should be used in the latter two integrals of (4) and (1). Then, according to Wolf's terminology, the transient term is

$$g_{2T}(t) = \int_t^\infty k(\tau)g_1'(t-\tau)d\tau = \int_{-\infty}^0 k(t-\tau)g_1'(\tau)d\tau \quad (5)$$

and the steady-state term is

$$g_{2SS}(t) = \int_0^\infty k(\tau)g_1'(t-\tau)d\tau = \int_{-\infty}^t k(t-\tau)g_1'(\tau)d\tau. \quad (6)$$

The steady-state term represents the response to $g_1'(t)$ as though it had been applied for all of its past history. The transient term accounts for the fact that $g_1'(t)$ was actually not applied until $t=0$, an effect which ultimately disappears, provided $k(\tau)$ is stable. It should be emphasized that (4) and (5) are valid only for a system initially at rest, since (5) accounts only for the absence of $g_1'(t)$ before $t=0$ and not for the presence of any initial values of g_2 or its derivitives.

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* Received by the IRE, August 19, 1960.

[1] S. Doba, Proc. IRE, vol. 48, August, 1960; p. 1480.

[2] A. A. Wolf, Proc. IRE, vol. 48, August, 1960; pp. 1480–1481.

Photon Propelled Space Vehicles*

In the above paper, a comparison between solar sail and chemical rocket,[1] the former device was put in a rather unfavorable position. I believe this result was due to a damaging assumption made by the authors, and did not do justice to the solar sail. To change a solar sail from a circular orbit around the sun to a spiral orbit, the authors assumed a scheme wherein a velocity increment was supplied by a chemical rocket. Please refer to the authors' Fig. 5.[1] This scheme provides an abrupt change in direction of the vehicle's velocity, and it does so at a heavy payload penalty. To use the solar sail to better advantage, the change-over should be accomplished gradually without outside assistance by proper control of the sail-tilt angle. The mechanics and mathematics of such a maneuver have been studied in detail by Kelley.[2] It is true that, initially, a solar sail has to be boosted into an orbit around earth by rocket power, but henceforth it should need no further assistance to escape earth and to enter into a heliocentric spiral path. In this way, the full performance capability of the solar sail may be developed; and its payload capacity can be shown to be much greater than that of ballistic rockets.[3]

The authors devoted a substantial portion of their paper to a discussion of the case of tangentially applied thrust. This case does not appear to be particularly significant. Here again, the solar sail does not perform at its best when the sail force is tangent to the flight path.[2-4]

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Authors' Comment[5]

We must agree with Dr. Tsu, that better performance capability of the solar sail may be achieved, and that greater payloads will result if the solar sail vehicle is not injected into a logarithmic spiral orbit and the sail is employed to escape from an orbit about the earth or from the earth's orbit. If propulsion alone were the basis for comparison, certainly the solar sail would appear more favorable by our allowing it to replace chemical propulsion in as many functions as possible. However, it must be remembered that schemes of this sort result in greater transfer times, and perhaps more sophisticated guidance systems. These considerations have a strong tendency to subtract weight from the absolute payload, because of added reliability, auxiliary power, and complexity requirements.

Our analysis[1] showed no abrupt changes in velocity. We merely asked what excess speed over escape velocity the vehicle would need so that it could be injected into a logarithmic spiral orbit, and related this excess speed to the burnout velocity. We then compared the solar sail vehicle to a ballistic rocket possessing the same burnout speed.

We again agree with Dr. Tsu that the case of tangentially applied thrust is not particularly significant, but this was pointed out in at least two places in the paper. The special case of the tangential thrust was discussed because we felt the simpler equations allowed a more straightforward presentation of our method.

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* Received by the IRE, June 20, 1960.
[1] D. C. Hock, F. N. McMillan, and A. R. Tanguay, PROC. IRE, vol. 48, pp. 492–496; April, 1960.
[2] H. J. Kelley, "Gradient Theory of Optimal Flight Paths," presented at the Amer. Rocket Soc. Semi-Annual Meeting, Los Angeles, Calif., paper no. 1230-60; May 9–12, 1960.
[3] T. C. Tsu, "Interplanetary travel by solar sail," *Amer. Rocket Soc. J.*, vol. 29, pp. 422–427; June, 1959.
[4] H. S. London, "Some exact solutions of the equations of motion of a solar sail with constant sail setting," *Amer. Rocket Soc. J.*, vol. 30, pp. 198–200; February, 1960.
[5] Received by the IRE, July 11, 1960.

Contributors

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I. Abeyta

After graduation, he went to work for a power and light company in northern New Mexico. In 1951 he joined, as a civilian, the Signal Corps Engineering Laboratories, where he was assigned to the microwave component design and development laboratory. He joined RCA, Camden, N. J., in June, 1957, where he worked as an applications engineer in the field of microwave components until September, when he transferred to the electronic data-processing division. He is presently employed in the advanced development of high-speed computer devices.

Allan H. Anderson (S'55–M'60) was born on October 12, 1935, in Sand Creek, Wis. He received the B.S.E.E. degree from the University of Wisconsin, Madison, in 1957.


A. H. Anderson

He joined the Memory Development Section at the Massachusetts Institute of Technology Lincoln Laboratory, Lexington, in 1957 as a staff associate. In 1959 he received the M.S. degree from M.I.T., Cambridge, and joined Lincoln Laboratory as a full-time staff member.

Mr. Anderson is a member of Eta Kappa Nu, Tau Beta Pi, and Sigma Xi.

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Isaac L. Auerbach (S'46–M'49–SM'52–F'58) was born in Philadelphia, Pa., on October 9, 1921. He received the B.S.E.E. degree from the Drexel Institute of Technology, Philadelphia, in 1943 and the M.S. degree in applied physics from Harvard University, Cambridge, Mass., in 1947.


I. L. Auerbach

He is President and Technical Director of Auerbach Electronics Corporation, Philadelphia, which he founded in 1957 to undertake system engineering, custom equipment development, and product and market planning research in information technology. From 1949 to 1957 he was associated with the Burroughs Research Center where, as Manager of the Special Products Division, he directed the development of the ATLAS ICBM Guidance Computer, the radar target detection equipment for the SAGE air defense system and a number of other military information processing and digital communication systems. He was one of the leaders in applying magnetic cores

and transistors to digital data processing and and was responsible for the design and development of the Static Magnetic Memory System for the ENNIAC computer, the first application of magnetic cores to high-speed coincident selection memory. During his association with the Eckert-Mauchly Division of Remington Rand Univac, he was a member of the original team that designed the BINAC and UNIVAC.

He was scientific advisor to UNESCO on automation and information processing from 1957 to 1960. He was recipient of the Grand Medal of the City of Paris in June, 1959, for his outstanding service in helping to organize the UNESCO-sponsored First International Conference on Information Processing. He is the U. S. Representative of the National Joint Computer Committee (IRE, AIEE, ACM) to the American Standards Association and serves the NJCC as Chairman of the NJCC Standards Coordination Committee.

Mr. Auerbach is a founder and President of the International Federation of Information Processing Societies and the NJCC representative to this federation. He has held numerous posts in the IRE, both on a national and sectional level. He is a member of the AIEE, ACM, Research Society of America, The Franklin Institute, ISA, and Eta Kappa Nu and is a Registered Professional Engineer in the Commonwealth of Pennsylvania.

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Glenn C. Bacon was born on August 24, 1935, in Phoenix, Ariz. He received the B.S.E.E. degree from the University of California, Berkeley, in 1957 and is currently completing work for the M.S. degree at Stanford University, Stanford, Calif.

G. C. Bacon

He joined the IBM Research Laboratory at San Jose, Calif., in June, 1957, as an associate engineer. His initial assignment was in the area of magnetic recording head design for large-scale memories. He is presently concerned with problems in the area of the detection of signals in magnetic recording readback.

Mr. Bacon is a member of Eta Kappa Nu and Tau Beta Pi, and an associate member of Sigma Xi.

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Walter F. Bauer (A'53) was born on March 21, 1924, in Wyandotte, Mich. He received the B.S. degree in 1946, the M.S. degree in 1947, and the Ph.D. degree in 1947 from the University of Michigan, Ann Arbor.

He was a research engineer at the Willow Run Research Center of the University of Michigan and a lecturer in electronic engineering at the University from 1951–1954. At the University of Michigan he worked with the SEAC and MIDAC digital computers, two of the early general-purpose electronic computers in the country, and MIDSAC, one of the first computers for real-time control. Following this, he joined the Ramo-Wooldridge Corporation, Los Angeles, Calif., where he was head of the Digital Computing Center. Later he became director of the Computation and Data Reduction Center of Space Technology Laboratories, Los Angeles. Currently, he is head of the Information Systems Department, Thompson Ramo Wooldridge Corporation, Los Angeles.

W. F. Bauer

Dr. Bauer is a member of Phi Kappa Phi, Sigma Xi, the Society for Industrial and Applied Mathematics, and the ACM.

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Earl R. Beck (S'49–A'52) was born in New Orleans, La., on August 17, 1928. He received the B.S.E.E. and M.S.E.E. degrees in 1949 and 1952, respectively, from Rice University, Houston, Tex.

E. R. Beck

While pursuing his graduate studies he held an Electrical Engineering Department fellowship and served as a laboratory assistant. From 1952 to 1954 he served in the U. S. Marine Corps, and for 15 months of this service he was an instructor at the Marine Corps Institute, Washington, D. C.

Upon completion of this tour of duty, he joined the Research Laboratories Division of the Bendix Corporation, Southfield, Mich. He has been engaged in the investigation and development of components and circuitry for digital systems. He is now supervising a project to develop a high-speed random-access tunnel diode memory system.

Mr. Beck is a member of Tau Beta Pi and Sigma Xi.

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Frank S. Beckman was born on April 10, 1921, in New York, N. Y. He received the B.S. degree in mathematics from the College of the City of New York in 1940, the M.A. degree in 1947 from Columbia University, New York, N. Y., and has currently completed all course requirements towards a Ph.D. in mathematics at Columbia.

F. S. Beckman

He taught engineering college mathematics at Pratt Institute, Brooklyn, N. Y., where he was assistant professor of mathematics until 1951.

Since joining the IBM Corporation, New York, N. Y., in 1951, he has been assistant to the Manager of the Scientific Computing Center in charge of technical computing activities, Product Planning Representative (STRETCH), Manager of the 701-704-709 Applied Programming Group, Manager of Educational Research-Watson Laboratory, and Data-Processing Manager of Watson Laboratory. In May, 1960, he was named Assistant Director of the IBM Systems Research Institute.

Mr. Beckman is a member of the ACM, American Mathematical Association, American Mathematical Society, and the Society for Industrial and Applied Mathematics.

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F. Borgini was born on November 18, 1932 in Mount Clare, Ill. He received the B.S.E.E. degree from the Missouri School of Mines and Metallurgy, Rolla, in 1959, and he is presently studying for the M.S.E.E. degree at Drexel Institute of Technology, Philadelphia, Pa.

F. Borgini

After graduation, he joined RCA's Electronic Data Processing Division, Camden, N. J., where he was involved in the development of a 4-kMc subharmonic phase-locked oscillator for use as a logic element in the development of a carrier computer subsystem.

Mr. Borgini is a member of Eta Kappa Nu.

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Alfred E. Brain was born in Derbyshire, England, in 1922. He received the B.Sc. degree in physics from Sheffield University in 1943.

A. E. Brain

He was then a member of the Radio Department of the Royal Radar Establishment, Farnborough, until 1946. He worked on wide-band video amplifiers at E.M.I. Research Laboratories, Hayes, Middlesex, and received the M.Sc. degree from Sheffield University for a thesis on the application of phase correction networks in 1948. In 1949 he returned to the Physics Department at Sheffield as Ellison Research Fellow, and received the Ph.D. degree for work on the magnetic properties of semiconductors in 1952. After returning to E.M.I. to work on solid-state devices, he joined the Magnetic and Dielectric Devices Group at the Electronics Laboratory of the General Electric Company, Syracuse, N. Y., in 1956. He joined the Applied Physics Laboratory of the Engineering Division, Stanford Research Institute, Menlo Park, Calif., in December, 1958.

Frederick P. Brooks, Jr. (S'54–M'57) was born in Durham, N. C., on April 19, 1931. He received the B.A. degree in physics from Duke University, Durham, in 1953 and the M.S. and Ph.D. degrees from Harvard University, Cambridge, Mass., in 1955 and 1956, respectively, for graduate work in the design and application of computers.

F. P. Brooks, Jr.

From 1956 to 1959, he participated in the planning of the STRETCH and HARVEST computers at the IBM Product Development Laboratory, Poughkeepsie, N. Y. From 1959 to 1960 he studied computer organization theory in the IBM Yorktown Research Center. At present, he is Systems Planning Manager for the IBM Data Systems Division.

Dr. Brooks is a member of the ACM, Phi Beta Kappa, and Sigma Xi.

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David T. Brown (S'58–M'60) was born in Milford, N. H., on April 11, 1936. He received the B.S.E.E. and M.S.E.E. degrees in 1959 from the Massachusetts Institute of Technology, Cambridge.

D. T. Brown

While at M.I.T., he was in the cooperative program of the Department of Electrical Engineering and was employed by the General Electric Company for three industrial assignments. In 1959, he joined the IBM Corporation, Data Systems Division, Product Development Laboratory, Poughkeepsie, N. Y., where he is concerned with improving digital computer reliability by such methods as coding for error control and introducing redundant circuitry to detect or correct faults in a machine.

Mr. Brown is a member of Eta Kappa Nu and Sigma Xi.

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David R. Crosby (A'36–SM'46) was born on October 12, 1911, in Lockport, N. Y. He received the B.S.E.E. degree from Rensselaer Polytechnic Institute, Troy, N. Y., in 1934, and the M.S. degree in communications from Harvard University, Cambridge, Mass., in 1935.

He joined the Radio Corporation of America, Camden, N. J., in 1941, where he was engaged in work on RF transmission lines and antennas, and later on microwave and modulation theory. For the past two years he has been associated with a development group working on high-speed computer devices, particularly in applications for microwave technology. He is presently the leader of a group which is working on the development of millimicrosecond devices for computers. He is also a member of the evening faculty of the South Jersey Division of Rutgers University.

D. R. Crosby

Mr. Crosby is a Registered Professional Engineer in New Jersey, and a member of the AIEE and the American Mathematical Association.

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Thomas S. Crowther (M'58) was born on May 6, 1932, in North Woodstock, N. H. He received the B.S. degree in physics from the University of New Hampshire, Durham, in 1954, and the M.S. degree in physics from the University of Maryland, College Park, in 1960.

T. S. Crowther

From 1954 to 1956 he served as an Electronic Engineering Officer in the U. S. Air Force, stationed at Washington, D. C. From 1956 to 1957 he worked as an electronic engineer in the Department of Defense.

Since 1957, he has been employed at the Massachusetts Institute of Technology, Lincoln Laboratory, Lexington, in the Memory Development Section, and has been engaged in magnetic film production, testing, and evaluation.

Mr. Crowther is a member of Pi Mu Epsilon, Sigma Pi Sigma, and Phi Kappa Phi.

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Edward E. David, Jr. (A'48–M'56–SM'58) was born in Wilmington, N. C., on January 25, 1925. He received the B.E.E. degree from the Georgia Institute of Technology, Atlanta, in 1945, and the D.Sc. degree from the Massachusetts Institute of Technology, Cambridge, in 1950.

E. E. David, Jr.

During the latter period, he was a research assistant at the Research Laboratory of Electronics, working with microwave vacuum tubes and noise theory. He joined Bell Telephone Laboratories, Murray Hill, N. J., in the fall of 1950 and was concerned with communication acoustics and underwater sound. He is presently Director of Visual and Acoustics Research, in which capacity he is concerned with the perception and coding of sensory information and with human information processing.

His book on speech communication, co-authored with J. R. Pierce, entitled "Man's World of Sound," was published in 1958 and, in 1960, a second book, "Waves and the Ear," co-authored with W. A. Van Bergeijk and J. R. Pierce, was published.

Dr. Davis is a member of Sigma Xi and Tau Beta Pi and a Fellow of the Acoustical Society of America.

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Charles V. Freiman (S'54–M'57) was born on June 17, 1932, in New York, N. Y. He received the A.B. degree in 1954 from Columbia College, New York, N. Y., and the B.S. and M.S. degrees in 1955 and 1956, respectively from the school of engineering, Columbia University, New York, N. Y.

C. V. Freiman

From 1956 until 1960, he was employed by Columbia University as instructor in electrical engineering. He is currently at IBM Research Center, Yorktown Heights, N. Y., and is working toward the Eng. D.Sc. degree in electrical engineering at Columbia University.

Mr. Freiman is a member of Tau Beta Pi and Eta Kappa Nu.

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Daniel L. Gerlough (M'49) was born in San Diego, Calif., on May 31, 1916. He received the B.S. degree from California Institute of Technology, Pasadena, in 1937, the M.S.E.E. degree from the University of California, Berkeley, in 1948, and the Ph.D. degree in engineering from the University of California, Los Angeles, in 1955.

D. L. Gerlough

From 1937 to 1947 he held various engineering positions. While a graduate student at the University of California, Berkeley, from 1947 to 1948, he was one of the original members of the group which developed the CALDIC computer. During the period 1948 to 1959 he rose to the rank of Associate Professor in the Department of Engineering, University of California, Los Angeles. He taught electronic courses and was on the staff of the University's Institute of Transportation and Traffic Engineering where he worked with digital techniques in automobile traffic control.

From 1955 to 1959 he was a consultant in data-processing systems for a number of firms in the Los Angeles area. Since 1959 he

has been with the Information Systems Department, Thompson Ramo Wooldridge Corporation, Los Angeles. As Head of the Automobile Traffic Control Section, he devotes his attention to applications of electronic control to traffic problems.

Dr. Gerlough is a member of Sigma Xi, AIEE, ACM, Institute of Traffic Engineers and is a Registered Professional Engineer in the State of California.

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Jackson W. Granholm was born on November 18, 1921, in Tacoma, Wash. He received the B.S. degree in Physics from the University of Washington, Seattle, in 1947.

J. W. Granholm

He was a member of the technical staff, Ramo-Wooldridge Division of Thompson Ramo Wooldridge, Inc., Los Angeles, Calif., from 1959–1960. He held the position of senior group engineer at the Boeing Airplane Company, Seattle, and that of analyst at the General Insurance Company of America in 1954. Presently he is Editor and Publisher of *Computing News* and a consultant in information processing and related matters.

Mr. Granholm is a member of the ACM.

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Joseph K. Hawkins (M'57) was born in Pomona, Calif., on August 15, 1926. He received the B.S.E.E. and M.S.E.E. degrees from Stanford University, Stanford, Calif., in 1952.

J. K. Hawkins

From 1958 to 1959 he worked on information systems for military and civic applications as a data-processing consultant. From 1954 to 1958 he was with Alwac Corporation, Hawthorne, Calif., performing circuit and logical design on general-purpose digital equipment. Since 1959 he has been engaged in research on self-organizing machines at Aeronutronic, a Division of the Ford Motor Company, Newport Beach, Calif.

Mr. Hawkins is a member of Phi Beta Kappa and the AIEE.

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Munro K. Haynes (S'50–A'51–M'58) was born in Elmira, N. Y., on December 10, 1923. He received the B.S. degree in physics from the University of Rochester, Rochester, N. Y., in 1947 and the M.S. and Ph.D. degrees in electrical engineering in 1948 and 1950, respectively, from the University of Illinois, Urbana.

He joined the staff of the International Business Machines Corporation laboratory at Poughkeepsie, N. Y., in 1950, where he initiated the research program on magnetic core storage which led to the present core storage systems. In 1957 he joined the Machine Organization department in IBM Research, and was responsible for the coordination and direction of Phase II of the IBM Lightning Project. He is now serving as technical assistant to the IBM Director of Research.

M. K. Haynes

Dr. Haynes is a member of Sigma Xi and Eta Kappa Nu.

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Terry O. Herndon was born on March 15, 1934, in Syracuse, Kansas. He received the B.S.E.E. degree from Antioch College, Yellow Springs, Ohio, in 1957.

T. O. Herndon

Since 1957 he has been employed in the employed in the Computer Development Group at the Massachusetts Institute of Technology Lincoln Laboratory, Lexington, Mass., where he has been working on the development of high-speed magnetic film memories.

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Albert S. Hoagland (S'50–A'54–SM'57) was born on September 13, 1926, in Berkeley, Calif. He received the B.S. degree in 1947, the M.S. degree in 1948, and the Ph.D. degree in 1954, all in electrical engineering, from the University of California, Berkeley.

A. S. Hoagland

He was project engineer on the California Digital Computer Program, 1948 to 1950. From 1954 to 1956, he was a consultant for IBM and assistant professor at the University of California, teaching senior and graduate courses in switching theory and computers. He joined the staff of the IBM Research Laboratory in San Jose, Calif., in 1956, where he was a senior engineer in charge of file memory research, and is now manager of engineering sciences for the San Jose Research Laboratory. He is a Registered Professional Engineer in the state of California.

Dr. Hoagland is a member of AIEE, Phi Beta Kappa, Sigma Xi, Eta Kappa Nu, and Tau Beta Pi.

Paul Horowitz was born in New York, N. Y., on October 15, 1933. He was an electroencephalography technician for the U. S. Navy from 1951–1954. He received the B.S. degree in psychology from Los Angeles State College, Calif., in 1958, and has also completed special studies in biotechnology at the University of California at Los Angeles and industry-sponsored courses on computer design, systems design, and the SAGE system.

P. Horowitz

From 1959–1960, he was associated with the Ramo-Wooldridge Corporation, Los Angeles, as a human factors specialist for the Information Display Department. In this capacity, he developed operations and human factors analyses required by proposals for display systems. He organized and developed research programs on two-color projection systems, initiated study of stereo projection systems, and organized an encyclopedia on available display techniques. He developed and obtained patent disclosures on two high-speed, real-time projection systems. He was employed by the Systems Development Corporation, Santa Monica, Calif., as a Systems Training Problem Design Assistant from 1958–1959. He participated in the Air Force Systems training program for simulations with IBM 705 and 709 computers, and prepared training exercises for completion by the computers. In 1960, he joined Aeronutronic, a Division of the Ford Motor Company, Newport Beach, Calif., where he is presently engaged in human engineering analysis of information display systems for the ARTOC project.

Mr. Horowitz is affiliated with the Human Factors Society, the American Institute of Industrial Engineers, the IRE Professional Group on Human Factors in Electronics, the IRE Professional Group on Military Electronics and Psi Chi.

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L. P. Horwitz (M'59) was born in New York, N. Y., on October 14, 1930. He received the B.S. degree in engineering science in 1952 from the New York University of Engineering and the M.A. degree in physics and Ph.D. degree in theoretical physics in 1954 and 1957, respectively, from Harvard University, Cambridge, Mass. His thesis topic at Harvard was "Low Energy Applications of Meson Field Theory." He served at Harvard as a Teaching Fellow of natural sciences and physics during this period.

L. P. Horwitz

Several summers between 1952 and 1957 were spent as a staff consultant for Pickard

and Burns Inc., Needham, Mass., where he worked on an optimum bandwidth pulse rise-time study for long-range Loran and an automatic scanning device for plotting contours from aerial diapositives. In 1957 he joined IBM, Yorktown Heights, N. Y., where he developed (with H. H. Goldstine) a procedure for the diagonization of normal matrices and worked on studies of magnetic recording. He has been working in pattern recognition since 1959.

Dr. Horwitz is a member of Sigma Pi Sigma, Sigma Xi, Tau Beta Pi, the American Physical Society, the ACM, and SIAM.

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Edwin A. Irland (M'60) was born in Lewisburg, Pa. on April 29, 1929. He received the B.S.E.E. degree from Bucknell University, Lewisburg, in 1950 and joined the Bell Telephone Laboratories, Murray Hill, N. J., that year. He completed the Laboratories' Communication Development Training Program in 1953, and received the M.S. degree in mathematics from Stevens Institute of Technology, Hoboken, N. J., in 1958.

E. A. Irland

His assignments at Bell Laboratories have included work on automatic message accounting circuits for use in cross-bar telephone offices, development of a digital data transmission system for the Air Force SAGE project, design of data transmission circuits and logic circuits for a time-division electronic private branch telephone exchange, and, most recently, design of semiconductor circuits for use in twistor data storage systems in the Nike-Zeus project.

Mr. Irland is a member of Sigma Pi Sigma, Pi Mu Epsilon, and Tau Beta Pi.

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Vernon C. Kamm (A'54–M'59) was born in Washington, Ill., on March 10, 1929. He received the B.S.E.E. degree from the University of Illinois, Urbana, in 1951 and the M.S.E.E. degree from Wayne State University, Detroit, Mich., in 1960.

V. C. Kamm

From 1951 to 1953 he served in the U. S. Air Force. He worked in the Wayne State University Computation Laboratory from 1953 to 1957, where he was responsible for the operation of an experimental digital computer and supervised the development of a magnetic core memory. In 1957 he joined the Research Laboratories Division of The Bendix Corporation, Southfield, Mich., where he has been engaged in the development of digital data-processing and control systems. He is currently responsible for the development of high-speed logic circuitry employing tunnel diodes.

Mr. Kamm is a member of Tau Beta Pi and Eta Kappa Nu.

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Walter J. Karplus (M'56) was born on April 23, 1927 in Vienna, Austria. He received the B.E.E. degree in 1949 from Cornell University, Ithaca, N. Y., the M.S. degree in 1951 from the University of California, Berkeley, and the Ph.D. degree in 1954 from the University of California at Los Angeles.

W. J. Karplus

Since 1954 he has been a member of the engineering faculty of the University of California and is presently associate professor. He is also active as a consultant to numerous industrial organizations.

Dr. Karplus is the author of two books, "Analog Simulation" and "Analog Methods," and holds a number of patents in the electronics area.

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Herbert R. Kaupp was born on September 26, 1932, in Bristol, Pa. He received the B.S.E.E. degree from the University of Pennsylvania, Philadelphia, in 1959.

H. R. Kaupp

He then joined the Radio Corporation of America, Camden, N. J., where he has been working on the mathematical analysis of circuits for a high-speed computer research and development project. He is at present working towards the M.S.-E.E. degree under the RCA graduate study program at the University of Pennsylvania.

Mr. Kaupp is a member of Eta Kappa Nu, Tau Beta Pi, and Sigma Tau.

❖

Harry T. Larson (A'49–M'55) was born in Berkeley, Calif., on October 16, 1921. He received the B.S.E.E. degree from the University of California, Berkeley, in 1947 and the M.S.E.E. degree from the University of California at Los Angeles in 1952.

H. T. Larson

He served as a radar officer in the Army Air Force in World War II. His work on computers started in 1949 at the National Bureau of Standards at UCLA, on the design of the SWAC general-purpose computer. His activities at Hughes Aircraft and Ramo-Wooldridge Corporation included research in digital computer components, circuit design, business data-processor system design, and application of computers and data processors to new fields. At the Aeronutronic Division of Ford Motor Company, Newport Beach, Calif., his principle activities have been in the design and development of large military control systems and industrial control systems, his current assignment being Manager, Industrial Systems Activity, Computer Products Operations.

Mr. Larson is past Chairman of the PGEC and a member of Tau Beta Pi, Eta Kappa Nu, Sigma Xi, the ACM, and the Institute of Management Sciences.

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William J. Lawless, Jr., was born on April 13, 1919, in Newton, Mass. He received the B.A. degree in mathematical statistics from George Washington University, Washington, D. C., in 1952.

W. J. Lawless, Jr.

He served in the Army during World War II, and was awarded the Legion of Merit. He worked from 1942 to 1953 with the Department of Defense on data-processing machine installations. He then joined IBM Corporation, New York, N. Y., as a technical specialist in Corporate Headquarters Product Planning. From 1954 to 1957, he held various technical management positions, including that of manager of the HARVEST computer systems design. In 1958, he became manager of the IBM Lamb Estate Research Laboratory. He was then Executive Assistant to the Executive Vice President. In January, 1960, he became Director of System and Application Engineering.

Mr. Lawless is a member of Phi Beta Kappa, the AAAS, and the ACM.

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Thomas B. Lewis (M'55) was born in Philadelphia, Pa., on December 7, 1929. He attended Princeton University, Princeton, N. J., on an NROTC Scholarship (Holloway Plan), receiving the B.S.E. degree in basic engineering in 1951.

T. B. Lewis

He was commissioned Ensign in the U. S. Navy upon graduation and served as gunnery officer aboard a destroyer. He then joined IBM, Kingston, N. Y., and was assigned to Development Engineering of the Sage System. He assisted in the logic design of the main drum system, and was later responsible for the logic design of the auxiliary drum system. He was then assigned to Product Engineering as a group leader in computer design. This work included preparation of machine improve-

ment, cost reduction, and factory-service-type engineering changes to early production models of the SAGE drum system. He also participated in production testing of the first model drum system.

He was transferred to the IBM Owego Development Engineering Department in 1957, assigned as Staff Engineer in Computer Development. He conducted a study of computer logic and organization suitable for high-temperature application; he also defined the maintainability design philosophy for the AN/ASQ-28 BNMG Subsystem digital computers and then coordinated the implementation of this philosophy. In 1959, he was assigned as Manager of the Computer Logic Department. In this capacity, he was responsible for laboratory checkout of the main and emergency computers for the AN/ASQ-28 Subsystem, design of computer input-output equipment for the B-70 application, and complete simulation and evaluation of computer logic utilizing an IBM 704 Data-Processing Machine. In 1960, he was promoted to Manager of Computer Development with responsibility for system, electronic, and logic design areas for all computer efforts in Systems Development Engineering at IBM Owego.

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Richard T. Loewe was born in Chicago, Ill., on September 11, 1927. He served as an electronic technician in the U. S. Navy from 1945 to 1946. He received the B.S.E.E. and M.S.E.E. degrees in 1950 and 1951, respectively, from the University of Illinois, Urbana, where he was also a teaching assistant and research assistant.

R. T. Loewe

He was employed at Hughes Aircraft Company, Culver City, Calif., from 1951 to 1954, in the design of operational test equipment for airborne rocket and missile fire control systems. At Autonetics, a Division of North American Aviation, Inc., Downey, Calif., he was engaged in research and development on various data-processing products and was responsible for the initial system design of the instrumentation and data-reduction system for the NAA Trisonic Wind Tunnel. He joined Electronic Control Systems, a Division of Stromberg-Carlson Company, Los Angeles, Calif., in 1957, where he participated in the initial system design of a large-scale electromagnetic reception system (GPERF) and was responsible for a study on intelligence data retrieval. At Aeronutronic, a Division of the Ford Motor Company, Newport Beach, Calif., since 1958, he has served as head of the System Design Section of the Army Tactical Operations Central (ARTOC) project and is currently engaged in advanced system development.

Mr. Loewe is a member of Tau Beta Pi, Eta Kappa Nu, Phi Kappa Phi, and Sigma Tau.

Paul R. Low (M'57) was born on March 16, 1933, in Elizabeth, N. J. He received the B.S.E.E. degree and the M.S. degree in physics in 1954 and 1957, respectively, from the University of Vermont, Burlington.

P. R. Low

In 1957 he joined IBM's Product Development Laboratory, Poughkeepsie, N. Y., where he has worked in the areas of circuit design and semiconductor device development for digital computers. His most recent assignment was evaluating semiconductor devices in an exploratory circuit technology group. He is presently studying for the doctorate degree at Stanford University, Stanford, Calif., under IBM's advanced degree program.

Mr. Low is a member of Tau Beta Pi.

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Olin L. MacSorley (SM'54) was born in Baltimore, Md., on October 23, 1912. He received the B.E.E. degree from the University of Delaware, Newark, in 1935, and the M.S. degree from the University of Pennsylvania, Philadelphia, in 1952.

O. L. MacSorley

From 1935 to 1951 he was employed by RCA, most of his work being associated with the design of communication receivers. In 1951 he joined the International Business Machines Corporation, where he initially worked on the design of the 701 computer. Following this he has been associated with the systems design or circuit design of various projects. His most recent assignment was the logical design of the parallel arithmetic section of the Stretch Computer. He is presently a Senior Engineer in the Data Systems Division of IBM, Poughkeepsie, N. Y.

Mr. MacSorley is a member of Tau Beta Pi and Phi Kappa Phi.

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Gerald A. Maley was born on March 5, 1929, in Buffalo, N. Y. He received the B.S.E.E. degree from the University of Buffalo in 1953.

G. A. Maley

He then joined IBM's Product Development Laboratory, Poughkeepsie, N. Y., where he was engaged in electronic circuit design for data processing systems. He is now in charge of an exploratory logic group studying new devices for use in future computer systems.

He became a member of the Syracuse University faculty in January, 1960.

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Marvin L. Minsky (M'56) was born in New York, N. Y., on August 9, 1927. He received the B.A. degree in mathematics in 1950 from Harvard University, Cambridge, Mass., and the M.A. and Ph.D. degrees in mathematics in 1952 and 1954, respectively, from Princeton University, Princeton, N. J. Up to this time, his chief interests were in topology and in neural-analog theories of brain function. In 1951 (with D. S. Edmonds) he built a machine at Harvard, the SNARC—a random-net reinforcement learning device.

M. L. Minsky

From 1954 to 1957 he was a Lowell Prize Fellow of the Harvard University Society of Fellows, working on the heuristic approach to artificial intelligence and on flying-spot microscopy. In 1957 he joined the staff of the Massachusetts Institute of Technology Lincoln Laboratory, Lexington, and in 1958 he joined the faculty of the M.I.T. Department of Mathematics, the Research Laboratory of Electronics, and in 1960, the M.I.T. Computation Center, Cambridge. Since 1957, he has been working on heuristic programming and on the theory of Turing machines.

Prof. Minsky is a member of the ACM, the American Mathematics Society, the New York Academy of Sciences, and AAAS.

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Merle L. Morgan (S'48–A'54–M'60) was born on May 28, 1919 in Whittier, Calif. He received his engineering training at the California Institute of Technology, Pasadena, where he received the Ph.D. degree in electrical engineering in 1954. He conceived the idea for the ESIAC while a graduate student and wrote his Ph.D. dissertation on this topic. Since that time he has been with Electro Scientific Industries Inc., Portland, Ore., as Director of Research and Engineering.

M. L. Morgan

Dr. Morgan is Secretary-Treasurer of the Portland Section of the IRE, and is also a member of AIEE, the Society for Social Responsibility in Science, Sigma Xi, and Tau Beta Pi.

Eric Nussbaum (S'54–M'57) was born in Vienna, Austria, on April 29, 1934. He attended Columbia University, New York, where he received the B.S.E.E. and M.S.E.E. degrees in 1955 and 1956, respectively.

E. NUSSBAUM

From 1956 to 1959 he was on the staff of General Precision Laboratory, Inc., Pleasantville, N. Y., where he was engaged in development work on special-purpose analog and digital computers for airborn navigation and air traffic control applications. In 1959 he joined Bell Telephone Laboratories, Inc., Murray Hill, N. J., as a member of the Special Systems Development Department where he has been concerned with the development of both semiconductor and magnetic logic circuits.

Mr. Nussbaum is a member of Tau Beta Pi and Eta Kappa Nu.

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William Orchard-Hays was born on September 13, 1918, in Portland, Ore. He received the M.A. degree in mathematics from the University of California at Los Angeles.

W. ORCHARD-HAYS

He worked for six years as a mathematician and programming specialist in the Numerical Analysis Department of the RAND Corporation, Santa Monica, Calif. He developed several early interpretive coding setups for the IBM CPC, some of which were widely used; he was also co-developer of the only stored-program setup for the CPC. He had early experience in computing for many fields, including engineering calculation, statistical and probability analyses, root-finding algorithms, and numerical simulations. He developed computational techniques for linear programming and related problems, carrying a project of development over a period of four years through 10 successive systems for the CPC, IBM Type 701 and JOHNNIAC, and the widely-used system of Type 704 Linear Programming codes, of which he is principal designer and programmer. He has also served as lecturer and instructor on linear programming theory and computing techniques.

He is presently Vice President of C-E-I-R, Inc., Houston, Tex., and Director of the Houston Research Center. His specialties lie in the fields of scientific machine programming, organization of computing machine procedures, and the development of computational techniques for linear programming and related models.

Mr. Orchard-Hays is a member of the SHARE 704 Data Processing Committee, Phi Beta Kappa, Pi Mu Epsilon, and the ACM.

Robert T. Pearson was born on June 14, 1927, in Lynn, Mass. He received the B.S.M.E. degree from Iowa State College of Agriculture and Mechanic Arts, Ames, in 1949, and has also completed several graduate courses at Northeastern University, Boston, Mass.

R. T. PEARSON

He was assistant superintendent of the James Millen Manufacturing Company, producing electronic test equipment and component parts. He then worked for the Towle Manufacturing Company as a project engineer engaged in machine and tool design and development for the automation of silverware manufacturing process. He joined the Laboratory for Electronics, Boston, in 1956 as a development engineer on the DIANA Computer File Drum components and equipment. He has continued as Senior and Project Engineer on the HD File Drums and other information storage projects. He is presently in charge of the design and development of new storage devices. He is co-inventor of the tape disk device and has patents pending on other information storage devices.

Mr. Pearson is a member of ASTE and the Beverley Professional Engineers Associates. He is a Registered Professional Engineer.

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W. Wesley Peterson (S'49–A'52–M'58) was born in Muskegon, Mich., on April 22, 1924. He received the B.A. degree in mathematics, the M.S.E. degree, and the Ph.D. degree in electrical engineering in 1948, 1950, and 1954, respectively, from the University of Michigan, Ann Arbor.

W. W. PETERSON

From 1951 to 1954 he was a research associate in the Engineering Research Institute of the University of Michigan. He was employed by the IBM Engineering Laboratory, Poughkeepsie, N. Y., from 1954 to 1956. In 1956 he joined the faculty of the University of Florida, Gainesville, where he is now an associate professor. He is currently on leave as visiting associate professor of electrical engineering at the Massachusetts Institute of Technology, Cambridge.

Dr. Peterson is a member of the American Mathematical Society and Sigma Xi.

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Jack I. Raffel (S'51–A'55–M'59) was born on April 1, 1930, in New York City. He received the A.B. degree from Columbia College, New York, N. Y., in 1951, and the B.S.E.E. degree from Columbia University in 1952.

From 1952 to 1954 he was a research assistant in the Digital Computer Laboratory at the Massachusetts Institute of Technology, Cambridge, which became part of Lincoln Laboratory, Lexington, Mass. After receiving the M.S. degree in 1954, he continued work on applications of magnetics to storage and switching problems in digital computers, and since 1956 has been working on engineering applications of magnetic films.

J. I. RAFFEL

Mr. Raffel is a member of Tau Beta Pi and Sigma Xi.

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Jan A. Rajchman (SM'46–F'53) was born in London, England, on August 10, 1911. He received the Diploma in electrical engineering and the degree of Doctor of Technical Sciences from the Swiss Institute of Technology, Zurich, Switzerland, in 1934 and 1938, respectively.

J. A. RAJCHMAN

He joined RCA in 1935 and has been engaged in research since 1936, first in Camden, N. J., and from 1942 to the present, in Princeton, N. J. He is presently Associate Director, Systems Research Laboratory, and is directing research in electronic digital computers and data processing, a field in which he has been active since 1939.

He first worked in electron optics and is directly responsible for the development of the electron multiplier tube. Later, he worked on the betatron, for which he became co-recipient of the 1947 Levy Medal of the Franklin Institute. In 1960, he received the Morris Liebman Award for his work on magnetic devices for information processing.

During World War II, he was among the first to apply electronics to computers. After the war, he worked chiefly with memory devices for computers. He developed the selective electrostatic storage tube and the magnetic core memory system that is now standard in modern computers. In the new field of magnetics, he developed a number of switching circuits, the transfluxor, the ferrite aperture plate memory, and transfluxor controlled display panels. He is presently directing research in digital computers involving magnetic, cryoelectric, solid-state, and microwave techniques, as well as system studies.

Dr. Rajchman is a member of the American Physical Society, the ACM, and Sigma Xi. He is listed in "Who's Who in Engineering" and "American Men of Science." He holds more than 60 U. S. patents.

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Glenmore L. Shelton, Jr. was born in Newport News, Va., on September 19, 1924. He received the B.S. degree in marine engineering in 1944 from the National Maritime Academy, King's Point, L. I., N. Y.,

and the B.S. degree in industrial physics in 1951 from Virginia Polytechnic Institute, Blacksburg.

G. L. SHELTON, JR.

He joined the David Taylor Model Basin, Carderock, Md., in 1951 to work on hydrodynamic potential field and vibration problems. In 1952, he joined Hasting's Instrument Company, Hampton, Va., where he was engaged in development work on velocity measuring instruments for both fluids and gases, and on CW navigation equipment including special-purpose real-time computers for tracking and plotting operations. He joined IBM, Yorktown Heights, N. Y., in 1955 as a member of the Component Development Department and was engaged in the development of magnetic transducers and in recording techniques. In 1957, he became a member of the Experimental and Exploratory Machine Department, where he is engaged in the development of methods of character reading by machines.

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Robert C. Sims (A'53–M'58) was born in Franklin, Ky., on October 15, 1928. He received the B.S.E.E. and M.S.E.E. degrees from the Massachusetts Institute of Technology, Cambridge, in 1952.

R. C. SIMS

While attending M.I.T. he was engaged in a cooperative program with the General Electric Company, which included sixteen months of plant assignments at Pittsfield, Mass., and Schenectady, N. Y. While attending graduate school he was employed as a research assistant at the M.I.T. Digital Computer Laboratory, where he worked on the design of magnetic core circuitry for digital logic. Since his graduation he has been with the Research Laboratories Division of The Bendix Corporation, Southfield, Mich. He has participated in a number of projects involving the design and development of systems and subsystems, with particular emphasis on system design. He is now the supervisor of the Digital Research Group of the Computer Development Department.

Mr. Sims is a member of Tau Beta Pi and Eta Kappa Nu.

❖

Roger L. Sisson (S'48–A'50–M'51) was born in Brookline, Mass., on June 24, 1926. He received the B.S.E.E. and M.S.E.E. degrees in 1948 and 1950, respectively, from the Massachusetts Institute of Technology, Cambridge.

He has had ten years' experience in the design of digital computers, in the management of a customer's service group, and in the design of data-processing systems. He first worked on the development of analog and digital computer techniques, the design of data-reduction systems for missile test ranges, and on the development of timing equipment for missile firing applications. He then worked at the National Cash Register Company, Hawthorne, Calif., where he was Manager of Customer Service. From 1952 to 1954, he was a partner of Canning, Sisson and Associates, Los Angeles, Calif., a firm specializing in the design of data-processing systems for commercial applications and many related activities. He joined Aeronutronic, a Division of the Ford Motor Company, Newport Beach, Calif., in 1958, and is presently Assistant Manager of the Military Systems Department, Computer Products Operations.

R. L. SISSON

Mr. Sisson is a member of the ACM, the Institute of Management Sciences, the American Mathematical Association, Tau Beta Pi, Sigma Xi, and Eta Kappa Nu.

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Oscar B. Stram was born in Bridgeport, Conn., on May 15, 1921. He received the B.S. degree in mathematics from Tufts University, Medford, Mass., in 1949, and has done graduate work at the University of Pennsylvania, Philadelphia.

O. B. STRAM

He is presently with Burroughs Corporation Research Center, Paoli, Pa., engaged in research and development of magnetic logical transducers designed for the generation of unique input-output relationships within a single stage. Earlier, he designed a magnetic disk memory system for a small computer system used to demonstrate and prove the applicability of novel computer techniques in advance of the state-of-the-art.

Mr. Stram is a member of RESA, the ACM, and Phi Beta Kappa. He was co-recipient of the 1958 "Best Paper Award" of the IRE Professional Group on Ultrasonics Enginnering for his paper in the August, 1957, issue of that Group's TRANSACTIONS, "A High-Performance Magnetostriction-Sonic Delay Line."

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John G. Truxal (S'47–A'48–SM'54–F'59) was born in Lancaster, Pa., on February 19, 1924. He received the B.A. degree from Dartmouth College, Hanover, N. H., in 1944, and the D.Sc. degree from Massachusetts Institute of Technology, Cambridge, in 1950.

He taught at Purdue University, Lafayette, Ind., and then at the Polytechnic Institute of Brooklyn, N. Y., where he is currently Head of the Electrical Engineering Department.

J. G. TRUXAL

Dr. Truxal is chairman of the American Automatic Control Council Theory Committee and the IRE Professional Group on Education.

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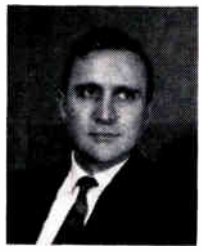
J. M. Wier (A'50–M'55) was born in Amsterdam, Mo., on March 2, 1924. He received the B.S.E.E. and M.S.E.E. degrees from Iowa State College, Ames, in 1949 and 1950, respectively.



J. M. WIER

He was employed in the Digital Computer Laboratory of the University of Illinois, Urbana, from 1950 to 1956 while completing the requirements for the Ph.D. degree at that institution. In 1956 he joined the Bell Telephone Laboratories, Murray Hill, N. J., and since then has worked on problems in data communications and data processing.

He is a member of Tau Beta Pi, Phi Kappa Phi, Pi Mu Epsilon, Eta Kappa Nu, and Sigma Xi.

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Charles E. Young (S'56–M'57) was born in Toledo, Ohio on August 28, 1931. He received the B.S.E.E. degree from the University of Toledo in 1957.

C. E. YOUNG

In 1957 he joined the Bell Telephone Laboratories, Murray Hill, N. J., as a member of the technical staff. There, through the Communications Development Training Program, he obtained the M.E.E. degree from New York University in 1959. He was active in logic design work for the Nike-Zeus Data Communication System. His work also included computer studies of new quartz crystal cuts, semiconductor surface properties, and logic packages for large digital systems. In 1960 he joined the International Electric Corporation, an ITT Associate, in Paramus, N. J. There he has been engaged in engineering management work concerning Project 465-L for the Air Force.

Mr. Young is a member of Tau Beta Pi, Phi Kappa Phi, and Pi Mu Epsilon.

Books

Alternating-Current Circuits, 4th ed., by Russell M. Kerchner and George F. Corcoran

Published (1960) by John Wiley and Sons, Inc., 440 Fourth Ave., N. Y. 16, N. Y. 590 pages+12 index pages+x pages. Illus. 6×9¼. $8.75.

This book is the revised edition of the authors' book of the same title and is designed for "junior electrical engineering students." The book consists of fourteen chapters, with the addition of some new materials such as network topology, duality and concepts of poles and zeros.

The book opens with the analysis of direct current circuits, discussion of sources, superposition, loop currents, node-pair voltages, loop and node equations, resistance and conductance matrices, network topology, identifying a loop current with a "link current" and dual networks. In the second chapter, alternating currents and voltages are introduced, impedance is defined, and real and reactive power is discussed. The third chapter presents the effective and average values of waves including phasor representation. Chapter 4 is devoted to "phasor algebra," including a discussion of the operator j, addition, subtraction, multiplication and division of phasors, and impedances in polar and cartesian forms. In Chapter 5, the sinusoidal analysis of single-phase circuit is discussed in terms of impedance, power factor, resonance, degree of selectivity, Q, circle diagram, efficiency, complex frequency, poles and zeros, reactance theorem, impedance match and maximum power transfer, Thevenin's and Norton's theorems, and delta-wye transformation.

Chapter 6 presents the analysis of complex waves, including Fourier series, graphical methods, effective value and power of nonsinusoidal waves, deviation factor in sine-wave approximation, harmonics, and modulated waves. The discussion is extended to coupled circuits in the following chapter. Magnetically coupled networks such as mutual inductors and transformers are presented. Chapters 8 and 9 present balanced and unbalanced polyphase circuits in terms of generation of polyphase voltages, balanced and unbalanced wye and delta loads, measurement of power, reactive volt-amperes.

In Chapter 10, the study of transmission lines is introduced by way of lumped equivalent circuits, the exact solution of a long line and its physical interpretation, terminal reflection, propagation velocity, determination of transmission line parameters. The following chapter discusses classical filter theory in terms of image impedances, characteristic impedances of T and π sections, filter equations, low- and high-pass sections, constant k-filter, pass- and stop-band filters, m-derived half and full sections.

Chapter 12 describes symmetrical components; topics such as positive, negative and zero phase sequence systems, line-to-line voltages, phase voltages, power, copper loss, the sequence rule, and magnetic coupling between phases are treated. Chapter 13 discusses the methods of the short-circuit calculation, for example, the method of using ohms on a kilovolt base, percentage method, per unit method, including accuracy, three phase and line-to-line and line-to-ground short circuits, and impedances to positive, negative and zero sequence systems.

Finally, the last chapter contains the transient analysis of simple circuits such as RL, RC and RLC circuits, circuit behavior in terms of poles and zeros, iron-clad RL circuit, and finite difference method.

The book contains a massive amount of material: illustrative examples, tables and problems. They must have been accumulated and resulted from the authors' long years of teaching experience. It seems to the reviewer that there are a number of points in the book for which an improvement of the order of presentation and clarification of discussions might be achieved. Some of these are listed below:

1) In Chapter 1, the discussion of the sufficiency of the number of independent loop and node equations is not clear. However, it may be possible to derive the necessary relations by extending the concept of the invariance of the determinants of the "resistance and conductance matrices" of a network.

2) Before presenting the study on transmission lines and filters, it would be desirable to discuss the characterization of a two-terminal-pair network (or two-port network) in order to accelerate and simplify the forthcoming discussions.

3) The book contains four chapters on the subject of power transmission. However, no section on active models, including dependent node-pairs, is found. It may be desirable to include linear active circuit elements such as simple vacuum tubes and transistors. The authors pointed out in their preface that the book is being revised because of "the great advances in electronics." A clear understanding of the differences between the passive and active circuit elements would be essential for a student to grasp the development of electronics.

W. H. Kim
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The Surface Chemistry of Metals and Semiconductors, Harry C. Gatos, Ed., with the assistance of J. W. Faust, Jr., and W. J. LaFleur

Published (1960) by John Wiley and Sons, Inc., 440 Fourth Ave., N. Y. 16, N. Y. 518 pages+4 index pages+bibliography by chapter. Illus. 6×9¼. $12.50.

In recent years, semiconductor devices have decreased in size, and with this trend, the ratio surface/volume has increased considerably. Engineers, physicists and chemists have therefore become more interested in surface phenomena. Literature on surface chemistry is, however, diffuse. Consequently, the appearance of the complete transcript of the Symposium of the Electrochemical Society on the Surface Chemistry of Metals and Semiconductors held in Columbus, Ohio, October 19–21, 1959, is most welcome. The editors had the great task of bringing together the various aspects of the complex problems of surface chemistry, and this volume is a record of their success. Altogether 22 papers are presented under 5 headings, which are: Chemistry and Physics of Surfaces, Imperfections and Surface Behavior, Electrode Behavior of Metals and Semiconductors, Surface Reactions in Liquid Media, and Surface Reactions in Gaseous Media. Many of the papers are reviews and several of these have the merit of critically presenting their subject from specific viewpoints and in that sense they have a high degree of originality. It is impossible to comment here in detail on each paper, but those by Farnsworth on "Clean Surfaces," by Handler on "Electrical Properties of the Surface of Semiconductors," by Cabrera on "The Role of Dislocations in the Reactivity of Solids," by Gilman on "Effects of Dislocations on Dissolution," by Gerischer on "Metal and Semiconductor Electrode Processes," by Dewald on "Experimental Techniques for the Study of Semiconductor Electrodes," by Turner on "Electrolyting Etching of Semiconductors," and by M. Boudart on "Adsorption and Chemisorption" are outstanding presentations in their respective fields.

This well-organized symposium certainly forms a valuable contribution to the subject. Unfortunately, a paper on the important area of adsorption on semiconductors was not included. Everybody interested in the chemistry of metal and semiconductor surfaces should be familiar with this book.

Wolfgang Mehl
RCA Labs.
Princeton, N. J.

Solid State Physics in Electronics and Telecommunications, Vol. 3, Magnetic and Optical Properties, Part I, M. Desirant and J. L. Michiels, Eds.

Published (1960) by the Academic Press Inc. (London) Ltd., 17, Old Queen St., London S.W. 1, England. 557 pages+xvi pages+bibliography by chapter. Illus. 6¼×10. $18.00.

This is the third volume of the Proceedings of the International Conference held in Brussels in June, 1958. It contains thirteen papers on "Ferrites," eight papers on "Properties of Magnetic Materials," twenty-one papers on "Applications of Magnetic Materials," five papers on "Garnets" and also five papers on "Magnetic Resonance." From this global outline of the contents, it is already clear that it is a typical conference report. It contains many excellent papers by leading researchers in the field. The state of the art and topics of current interest have developed and shifted so rapidly, however, that the value of such a report, more than two years after the date of the conference, is greatly diminished. The book is by its very

nature intended for active research workers. They need, however, more up to date accounts of current research. The work prior to 1958 can now be found in many excellent coherent reviews and textbooks. In the field of ferrites, *e.g.*, books have appeared, or will shortly appear, from the hand of many contributors to the 1958 conference, such as Lax, Schlomann, Soohoo, Wijn and others. The field of garnets was of course in its infancy in 1958. The eight papers on "Properties of Magnetic Materials" deal with metallic ferromagnets, and describe such diverse properties as initial permeability, magnetic after-effect, magnetization of powders and domain structure in thin films. The "Applications of Magnetic Materials" deals mostly with ferrites in microwave circuits and computer elements. Especially in high power effects, many new advances have been made since the conference. A paper on parametric amplifiers is included as a surprise topic in this section. The five papers on "Magnetic Resonance" are of course a random selection from this wide field of endeavor. One finds papers on magnetoabsorption in semiconductors, paramagnetic impurities in carbon, paramagnetic resonance and optical spectra in oxides of paramagnetic impurities, and the shape of ferromagnetic resonance lines influenced by inhomogeneous demagnetizing fields. It is surprising that the five papers on masers are not included in this volume. One will find these in volume 4 together with a variety of photoelectric effects. Again, these papers on masers written in 1958 of course do not give an accurate account of the state of the art in 1960.

The general appearance of the book is excellent. The typographical quality and quality of paper and binding is very high. One glance at the tables and drawings in the article by Rottig "Einize Bemerkungen zur Spinellstruktur der Ferrite" will confirm this. The buyer has, of course, to pay a price for this accomplishment. This reviewer can recommend the book, as part of a report on a 1958 conference in a rapidly developing field of research, only for institutional libraries.

N. Bloembergen
Harvard Univ.
Cambridge, Mass.

Noise Reduction, by Leo L. Beranek

Published (1960) by McGraw-Hill Co., Inc., 330 W. 42 St., N. Y. 36, N. Y. 703 pages+31 index pages +x pages+15 appendix pages+bibliography by chapter. Illus. 6¼×9¼. $14.50.

This excellent book on acoustic noise reduction presents a wealth of information based mainly on the broad experience of the consulting firm of Bolt Beranek and Newman, Inc. The 25 chapters in the book, written by 19 experts in the field, are grouped under four main headings: "Sound Waves and Their Measurement," "Fundamentals Underlying Noise Control," "Criteria for Noise and Vibration Control," and "Practical Noise Control."

The first part includes a detailed survey of instruments and techniques for noise measurement. The elementary discussion of the behavior of sound waves in the first part is expanded in the second to a detailed analysis of the behavior of sound outdoors, in enclosures, in solid structures, in porous materials, and in mufflers. Here a wide range of practical data is included with a discussion of the theoretical foundation. This section closes with a brief but fine chapter on "Isolation of Vibrations."

In the third section, one chapter gives an excellent review of the general problem of hearing damage from exposure to intense noise, and the other chapter itemizes a wide variety of criteria for noise. Noise control in ventilation systems, machines, shops, office buildings, homes and transportation is covered in the last section. This survey explains what the problems are in these many areas and what can be done to solve them.

Much more could have been included in a book such as this. For example, it is strange that there is practically nothing on the actual technique of vibration measurement, often the most effective approach to noise reduction. Although vibration pickups, metering systems, and analyzers are described, stroboscopic equipment and its general usefulness in vibration studies are not even mentioned. Furthermore, in the chapter on criteria, a short summary of the recent studies of the effects of noise on work output would have been helpful.

Electronic engineers who are sometimes called upon to solve acoustic noise problems will find this book a useful reference, not only because of the valuable material included, but also because of the extensive references to other work. Most of the chapters are easily grasped by an engineer; and because of his familiarity with electronic instrumentation, decibels, and waves, the electronics engineer will find it particularly easy to use.

Arnold P. G. Peterson
General Radio Co.
West Concord, Mass.

Thermoelectricity, Paul H. Egli, Ed.

Published (1960) by John Wiley and Sons, Inc., 440 Fourth Ave., N. Y. 16, N. Y. 399 pages+6 index pages+x pages, bibliography by chapter. Illus. 6×9¼. $10.00.

Thermoelectricity is making a great impact in several fields of science. In the early stages, obviously "publicity is ahead of technology" but it does hold out the pot of gold justifying payment for very important research which will most certainly lead to creation of valuable new materials. Thermoelectricity offers a great challenge and many attempts are being made to meet this challenge, but guidance is badly needed in the field.

This book, edited by Dr. Egli, is intended to provide the guidance, at least in materials development. In this reviewer's opinion, it does an excellent job and represents not only the latest science but also the considered views of the leading workers in the field.

Most of the chapters in "Thermoelectricity" were originally presented at the Conference on Thermoelectricity sponsored by the Naval Research Laboratory in September, 1958. To improve the continuity and breadth of coverage, other chapters have been added. As might be expected, some repetition and overlapping occurs; more important, different viewpoints are presented, considerably enhancing the value of the book.

The book contains 23 chapters divided into four sections and a conclusion by Dr. Egli. The first section covers "Fundamental Concepts in Thermoelectricity" and serves to introduce the subject and present a broad survey. Section II examines the basic physics of the properties which determine thermoelectric performance. Section III, "Chemical and Physical Properties of Materials at High Temperatures," discusses problems that arise in a program of research on thermoelectricity. Section IV covers "Measurement of Material Properties" and emphasizes thermal conductivity and high temperatures.

This book is highly recommended for scientists and engineers working on thermoelectric materials research and, particularly, for those seriously considering entry into the field.

F. E. Jaumot, Jr.
Delco Radio Div., GMC
Kokomo, Ind.

Optics of the Electromagnetic Spectrum, by Charles L. Andrews

Published (1960) by Prentice-Hall, Inc., Englewood, N. J. 477 pages+9 index pages+x pages+10 appendix pages. Illus. 6¼×9¼. $12.00.

This book is written as a text which might be used on an advanced undergraduate level or graduate level. Its material differs from other texts on either optics or electromagnetic theory in that it concentrates on the microwave field and optics and shows the value of thinking about both domains for the purposes of either one. The availability of microwave theory and experimental techniques has given optical people an excellent opportunity to work with monochromatic sources and to make experiments which either could not be made at all or only with great difficulty with light and optical techniques. Hence there is considerable emphasis on microwave theory and experiments which are usually treated in optics with light as a source.

The Table of Contents reads somewhat like an intercalation of optical topics in a microwave text or conversely. This is not said deprecatingly. In fact, the point of the book is to develop the connections between optics and microwaves and to show how techniques in one can now be used for the other. There is a gradual build-up from simple facts about wave propagation, superposition of waves, standing waves, and interference to diffraction phenomena, dispersion, and polarization. Maxwell's equations are introduced in the latter part of the book, but because most boundary value problems of diffraction theory as well as the problems of propagation in anisotropic media such as crystals are not treatable on the basis of Maxwell's equations, not much is done with these equations. The dominant approach is that of physical optics.

The book can be recommended highly. It starts with simple facts about waves and is developed very carefully. The mathematics is well explained, and the entire treatment is concrete and accompanied by good physical explanations. There are many

good figures and photographs, and suggestions for experimental demonstrations. In fact, the concreteness and understandability of the material is superior to that found in many other excellent books which, unfortunately for many readers, start on too high a level. There is not much doubt, too, that the book is timely. Optical people must surely move in the direction of wave theory as opposed to rigid adherence to geometrical optics and microwave people have much to learn from the optical people, though this material is not made available to them in standard textbooks on electromagnetic theory, and the geometrical optics viewpoint of optics texts ignores important phenomena of wave theory.

The book does not take up the few available exact electromagnetic solutions of diffraction problems or some of the more recent developments in linking Maxwell's equations to geometrical optics and in obtaining asymptotic solutions of Maxwell's equations for diffraction problems. This is not a criticism since the level of the book would preclude serious consideration of these topics. However, perhaps some indication of the more recent theoretical and experimental work would have been desirable.

Morris Kline
New York Univ.
New York, N. Y.

The A.R.R.L. Antenna Book, by the Headquarters Staff of the American Radio Relay League, Inc.

Published (1960) by the American Radio Relay League, Inc., West Hartford 7, Conn. 309 pages+3 index pages+2 bibliography pages. Illus. 6¼×9¼. $2.00.

The purpose of this book is to present available information on antennas useful to amateurs. It is a qualitative treatment written at a low level and rich with practical suggestions and examples. Related subjects on wave propagation and transmission lines round out the treatment.

The theory of wave propagation, antenna fundamentals and transmission lines is supported with useful charts. This general treatment is followed with chapters on directive arrays, long-wire antennas, multiband antennas, antennas for the various amateur bands, construction information, finding directions and mobile antennas.

The authors have written the book as a text using detailed word descriptions with most of the references in a bibliography at the end. This makes for easy reading with explanations that are quite accurate.

The expression "current flow" is redundant since current itself is a flow of electrons. Possibly the authors have used the term "flow" as a crutch in some cases where the expression "current vector" or "direction of current" would better describe the situation.

Also, it appears that "field intensity" is used interchangeably with "field strength." Strictly speaking, intensity should be related to electromagnetic energy transmitted per unit of time in the specified direction through a unit area normal to the direction at the point. Strength should be related to the values of electric E field. Concerning magnetic H fields, it is often referred to as an intensity. Hence, most places in the handbook should use the expression "field strength" rather than "field intensity."

The book is conservative in that only well-known art is presented. There are more sophisticated antenna systems such as frequency independent types which this writer believes should be covered in future editions.

Carl E. Smith
Cleveland Inst. of Electronics
Cleveland, Ohio

Traveling-Wave Engineering, by Richard K. Moore

Published (1960) by McGraw-Hill Book Co., Inc., 330 W. 42 St., N. Y. 36, N. Y. 330 pages+9 index pages+xix pages+bibliography by chapter+16 appendix pages. Illus. 6¼×9¼. $11.00.

This book provides the basis for a long-overdue reorganization of the standard transmission-lines course at many engineering schools of the reviewer's acquaintance. The author has written an introductory textbook on wave motion in a wide variety of media, using the electrical transmission line as the prototype and discussing the other media by means of a well-organized system of analogies. For this reason it will find its widest acceptance among teachers and students of electrical engineering for whom it can provide at very little extra effort a much broader understanding of the principles of wave motion than can be gained from the customary narrowly-oriented course in transmission lines. Thus, the reader learns about waves in acoustic and elastic media and about diffusion processes in thermal conduction and in fluids by direct analogy with the corresponding electric systems. All of the highly-developed techniques of transmission-line analysis are then available for solving the mechanical, acoustical, thermal, or chemical problems in question.

The author has obviously spared no effort to make the treatments consistent from one system to another, and has succeeded remarkably well. The tables of analogies are complete and should make the book useful as a reference to practitioners in the subjects mentioned. The development of the mathematical method is scholarly and accurate. There is a minimum of concern with "hardware" or with standard practice and a maximum of attention to physical processes and analytical procedures.

A few criticisms are in order. The most important from the reviewer's viewpoint concerns the division into separate chapters of the discussions of sinusoidal, steady-state, wave motion and of transient disturbances in media sustaining wave motion. The former is placed first, immediately following the derivation of the transmission line equations. Next comes a chapter in which are derived the wave equations for various nonelectric media. Following that, in Chapter 4, is an excellent discussion of "transient traveling waves." The reviewer feels that the sequence should have been reversed for best understanding by the student; unfortunately, the internal organization of the chapters will make it difficult to teach the subject in any order other than the one prescribed by the author. The other criticisms are minor. Inadequate discussion is given to the factor $\exp(j\omega t)$; on p. 27 it is merely included or "neglected" at will, a process which often leaves the student groping. The treatment of electromagnetic waves other than TEM modes on transmission lines is rather terse and will be understood only with difficulty by students without previous acquaintance with the subject. It is unfortunate that a more complete treatment of water waves, dismissed with a few words despite all their fascinating ramifications, could not have been substituted for the superficial and admittedly qualitative chapter on "Communication and Power Lines."

Despite these few criticisms, the reviewer wholeheartedly recommends Professor Moore's book to electrical engineering teachers interested in giving their students a broad understanding of the physics of waves.

G. W. Swenson, Jr.
Univ. of Illinois
Urbana

Digital Computer and Control Engineering, by Robert S. Ledley

Published (1960) by McGraw-Hill Book Co., Inc., 330 W. 42 St., N. Y. 36, N. Y. 786 pages+28 index pages+xxiv pages+20 appendix pages. Illus. 6¼×9¼. $14.50.

Excellence in textbooks is a rare quality, and this has been particularly true of texts written about the computer art. Fortunately, Professor Ledley has changed this situation and graced the tenth anniversary of modern computers with a textbook of both technical and pedagogical excellence.

The book is intended for the instruction of senior undergraduates or first-year graduate students, and should fill the needs of industrial training programs equally well.

The text is divided into five broad sections which cover every significant facet of computer engineering. Part 1 begins with an excellent introduction to the applications of computers, continues with an exposition of the basic principles and block diagrams, and ends with a very lucid and complete treatment of programming principles, including the description of automatic programming systems and even the ALGOL language. Part 2 deals with the fundamentals of numerical analysis, with the principles of information searching and ordering, and a survey of special-purpose digital computers. Part 3 leads the student from the fundamentals of boolean algebra to a series of systematic procedures for logical design based upon "designation numbers" (a method akin to the Quine-McCluskey, developed by the author) and boolean matrices. Part 4 delves into the structure and design of arithmetic units and digital control circuits. Finally, Part 5 discusses the electronic implementation of digital circuits, including solid-state and magnetic technologies, memories and input-output means.

An interesting feature of the book is that all the principles of computer design and construction are applied to the complete design and construction are applied to the complete design of a simple one-address serial computer, dubbed the Pedagac. As its name implies, this pedagogical aid provides an important element of continuity and helps the student understand the relevance of the material covered to the sequence of design steps involved in building a computer.

A great virtue of the book is that it is thoroughly up to date. The latest developments in the computer field are discussed, including tunnel diodes, magnetic thin films, cryogenics, microwave techniques, and even minimum wiring theory. The references cited are plentiful and modern, too.

In summary then, this is an excellent textbook for the student, and even a worthwhile reference book for the experienced computer engineer. Professor Ledley: a job well done!

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Analogue and Digital Computers, A. C. D. Haley and W. E. Scott, Advisory Eds.

Published (1960) by the Philosophical Library, Inc., 15 E. 40 St., N. Y. 16, N. Y. 303 pages+4 index pages+viii pages+bibliography by chapter. Illus. 5¾×8¾. $15.00.

About half of this 300-page volume is concerned with analog computers and the other half with digital computers. The book is intended to provide an elementary introduction to those fields. It is written for persons with a background in science, particularly electronics, but with no previous knowledge of computers. The book does contain some very lucid explanations of the basic techniques and terms used in computers. It is a useful introduction to the computer field.

The book suffers from the difficulty of freezing on paper a rapidly changing art. The art which the authors portray is the computer field as it existed in the United States about 1955. Most of the references are earlier than 1955 or 1956.

The chapters on analog computers contain analyses of the circuits and engineering and design procedures as well as information on applications. They start with a simple description of electromechanical computing devices, such as differential gears, wheel and disk integrator, etc. Simple interconnection of these devices to form an analog computer is then described. Operational amplifiers and the methods of performing integration, addition, subtraction, multiplication and scale and boundary value setting with them are described. A typical electronic analog computer is constructed using the basic building blocks and analyzed. Elementary discussions of some of the practical problems, such as stability, overload, voltage sources, output impedance, and recording the output, are presented. The design of analog computing circuits based upon vacuum tubes is presented. There is a section on generation of functions and nonlinearities.

The section on digital computers is descriptive in nature, with very little analysis or discussion of design techniques. It starts with a discussion of number representation in digital computers, including such items as binary numbers, arithmetic rules in binary numbers, binary point, etc. Some typical computer circuits, utilizing both vacuum tubes and transistors, are then described. AND-gates, OR-gates, Eccles-Jordan flip-flops, simple adders, direct-coupled transistor logic, and some simple core circuitry are among those presented. The organization of the arithmetic section of a small computer is described in a simple step-by-step manner. There is then a chapter on the various storage means used; mercury delay lines, magnetostrictive delay lines, electrostatic storage tubes, coincident current core storage and magnetic shift registers are discussed. There is then a chapter on input-output equipment, which includes a brief description of cards, punched-paper-tape, and magnetic tape units, and finally a chapter on programming.

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Electronics and Nucleonics Dictionary, by Nelson M. Cooke and John Markus

Published (1960) by McGraw-Hill Book Co., Inc., 330 W. 42 St., N. Y. 36, N. Y. 543 pages. Illus. 6×9. $12.00.

This book is the revised version of the previously widely-accepted dictionary of electronics terminology; however, the revision has been more than a rewrite. Obviously, the book has been revised from beginning to end, with about twice the initial coverage. The addition of nuclear terms is indeed welcome, particularly in view of the increasing correlation between these two fields, and here the electronics engineer will find clear, concise definitions of most of the terms which are common to the nuclear field, and vice versa.

The coverage is very complete and up-to-the-minute, including electronic items such as the tunnel diode, parametric amplifier, mesa transistor, crystron; space terms such as the Van Allen layer, Minuteman, Thor; nuclear terms such as rad, pinch effect, astron, etc.

As illustrated by some of the above examples, one important feature of this dictionary is its use as a style manual, *i.e.*, guide to the proper use of hyphenated words, capitals, trade names, abbreviations, etc. For example, the word "nonlinear" has now dropped its hyphen, in keeping with current usage.

It should be borne in mind that this is a dictionary, not a compendium of legal definitions. The authors state that "each dictionary has been phrased for maximum clarity and conciseness while still retaining the precise meanings set forth in the available formal definitions of the IRE, AIEE, ASA and other official engineering societies." Thus, the reader will note many changes, some minor and some not so minor, from the IRE Standards. If used as intended, however, these departures from vigor are not too serious. (Incidentally, have you ever been uncertain whether it should be "IRE" or "I.R.E."? This book will tell you.)

No work is perfect, and this reviewer cannot avoid pointing out a few random errors or omissions. The illustration for the *n-p-n* transistor uses symbols for the electrode currents which are not in accord with IRE Standards; the decibel (db) is defined but not the decilog; the definition of Professional Engineer makes no mention of licensing, which the NSPE (not included!) will definitely not like! However, if the average reader can find no more fault with this book that the above, he will be forced to your reviewer's conclusion that it is an authoritative, well-conceived and well-executed job.

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Principles of Control Systems Engineering, by Vincent Del Toro and Sidney R. Parker

Published (1960) by McGraw-Hill Book Co., Inc., 330 W. 42 St., N. Y. 36, N. Y. 635 pages+10 index pages+28 appendix pages. Illus. 6¼×9¼. $14.50.

This book is written as a college text for a first course in servomechanisms at the senior or first graduate level. It is clearly written with many problems at the end of each chapter, so it should be useful also for self-study, especially by electrical engineers.

The authors use the conventional approach, starting with Laplace transform theory, and progressing through the time-domain analysis to frequency-domain analysis and synthesis. Considerable detail is then included on linear approximations to transfer functions of typical servomechanism components. The book then continues in the frequency-response technique to study stability and compensation. There follows a perhaps too-long-delayed but very thorough treatment of the root-locus method of analysis and synthesis using the pole-zero concepts.

Outstanding in this book is the thorough treatment of the Nyquist stability criterion and the synthesis of RC networks to be used for compensation. Both topics are very clearly presented.

In the competitive engineering book mart of today, even elementary books must include some flashy new wares for sales appeal, even if as an afterthought of the writers. Here the material never before included in a general text on servomechanisms is a chapter on adaptive control systems. More generally useful are chapters on analog and digital simulation of control systems, for many college students now have computers at their disposal. The chapter on analog simulation is quite complete, including simulation of some nonlinearities in system equations; the digital chapter includes numerical integration methods suitable for simulating transient equations.

This reviewer thoroughly agrees with the authors' statement that "the background provided by the study of this book should serve well as preparation for advanced study . . . of control systems."

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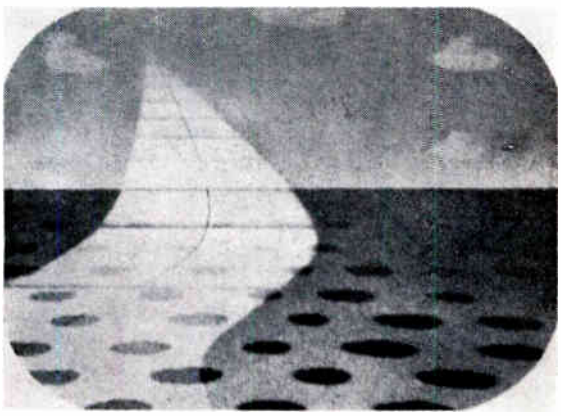
Scanning the Transactions

Artificial electronic displays have been a subject of growing interest in the last few years, especially in connection with the presentation of flight information to pilots of high-speed aircraft. This type of presentation differs from a television or radar display in that the "picture" is generated artificially by electronic circuits. The resulting display gives the pilot an immediate, meaningful picture, albeit an artificial one, of the altitude, speed and attitude of his craft with respect to the world around him. He no longer needs to read a large number of dials, translate the readings into physical quantities, and integrate all these data in his mind. The picture below shows some of the interesting progress that is being made in dynamic artificial display techniques, using standard video display devices. It represents an oscilloscope presentation of a



level-flight display with a programmed flight path around an obstacle. Above the horizon can be seen random clouds, while the lower foreground shows black patches which give texture to the terrain. The curving flight path, with its "tar strips," looks like a highway in the sky. To complete the picture, the tar strips and the terrain patches are made to move continually down the display (*i.e.*, toward the observer) in a manner which gives motion perspective to the whole picture. In addition, the picture can be rotated to show roll, moved up or down to show pitch, moved sideways to show changes in azimuth, and the size and spacing of the picture elements can be varied to show changes in altitude. (G. H. Balding and C. Süsskind, "Generation of artificial electronic displays, with application to integrated flight instrumentation," IRE TRANS. ON AERONAUTICAL AND NAVIGATIONAL ELECTRONICS, September, 1960.)

Communication at optical frequencies is a possibility that has recently intrigued a number of people interested in space communications. The large number of uncrowded communication channels that would become available make this part of the spectrum a very appetizing prize. But even more important, it is far easier to make a highly directed beam in the optical spectrum than it is in the radio spectrum. A study has now been made of the communication potentialities of the spectrum from the infrared through the visible to gamma rays. If the flash of an electrically exploded wire were used as the light source, it appears we could reach Mars from the surface of the Earth at the rate of one bit per second when the planets were at their closest proximity (about 36 million miles). The best wavelength region would be 4000 to 3000 angstroms in the near ultraviolet. With the transmitter located on a satellite, we could send one bit per second for a distance many times the diameter of the solar system in the 2000 to 400 angstrom range. The study does not indicate that we could communicate farther at optical frequencies than at radio frequencies using present techniques. However, the recent development of the optical maser is certain to bring some further improvement to optical communication system capabilities. (C. B. Ellis, "Use of optical frequencies for space communication," IRE TRANS. ON COMMUNICATIONS SYSTEMS, September, 1960.)

The fully automatic power plant appears to be one of the next important goals of the automation era. At last some significant first steps are being taken in this direction. The Louisiana Power and Light Company recently installed an elaborate electronic system for automatically scanning and logging large quantities of operational data at one of its steam electric generating stations. The next step, to be taken later this year, will be to automate a generating unit to the point where it can automatically be brought up from a cold start and put on the line, at which time it will be turned over to the dispatcher for loading. The system will also take the unit off the line upon command and secure it for maintenance. The final step, which now seems only a matter of time, will be to turn over the loading dispatcher's functions to a computer system. When that day comes we will have fully automatic pushbutton power plants with essentially no personnel except those required for maintenance. (J. A. Reine, Jr., "The operational information system and automation of Sterlington steam electric station," IRE TRANS. ON INDUSTRIAL ELECTRONICS, July, 1960.)

Biternary is a new word which we may be seeing more of in the future. Coined from the words binary and ternary, the word describes a promising new type of pulse-code modulation system which is being put into use in military communications systems. Biternary transmission is a method of combining two separate binary pulse trains in order to double the channel capacity of PCM systems without requiring increased bandwidth or transmission facilities. The process of combining two binary signals results in a three-level or ternary composite signal, hence the name biternary. In addition to an interesting name, the new system has some interesting characteristics. It has been found that under the transmission conditions that exist in military PCM systems, biternary transmission combines the assets of a transmission capacity equal to quaternary transmission, a tolerance of interference equal to ternary tranmission, and an inherent error detection capability possessed by no other known PCM transmission method. (A. P. Brogle, "A new transmission method for pulse-code modulation communication systems," IRE TRANS. ON COMMUNICATIONS SYSTEMS, September, 1960.)

For those who think engineering management is still all art and no science, we suggest they consider the following title of a paper in the September issue of the IRE TRANSACTIONS ON ENGINEERING MANAGEMENT: "The Application of Closed-Loop Techniques to Engineering Project Planning." It describes adaptations of methods used for controlling manufacturing processes to the control of research, development and engineering projects. If further evidence is needed, it may be found in another paper in the same issue under the title, "A Generalized Network Approach to Project Activity Sequencing," in which it is shown that when R and D projects are analyzed as networks of interrelated events, it is possible to find the optimal combination of time, technical performance level, and resources for any project.

Abstracts of IRE Transactions

The following issues of TRANSACTIONS have recently been published, and are now available from the Institute of Radio Engineers, Inc., 1 East 79th Street, New York 21, N. Y. at the following prices. The contents of each issue and, where available, abstracts of technical papers are given below.

Publication	Group Members	IRE Members	Libraries and Colleges	Non Members
Vol. ANE-7, No. 3	$2.25	$2.25	$3.25	$4.50
Vol. AP-8, No. 6	2.25	2.25	3.25	4.50
Vol. CT-7, No. 3	2.25	2.25	3.25	4.50
Vol. CS-8, No. 3	1.60	2.40	2.40	4.80
Vol. CP-7, No. 3	2.25	2.25	3.25	4.50
Vol. EM-7, No. 3	1.00	1.50	1.50	3.00
Vol. HFE-1, No. 2	2.25	2.25	3.25	4.50
Vol. IE-7, No. 2	1.40	2.10	2.10	4.20
Vol. MTT-8, No. 6	2.25	2.25	3.25	4.50

Aeronautical and Navigational Electronics

VOL. ANE-7, NO. 3, SEPTEMBER, 1960

The Editor Reports (p. 76)

A Mathematical Analysis of the Performance of the ATC Radar Beacon System—A. Ashely and F. H. Battle, Jr. (p. 77)

The capacity of the Air Traffic Control Radar Beacon System can be evaluated by extensive high-density flight testing, simulation, or mathematical synthesis. Actual flight testing, although desirable, is costly and inflexible. Simulation techniques would be an effective approach to analyzing the system problems, were it not for the cost of the simulator required for this type of work and the delay incurred waiting for the construction and test of the simulator. Use of a mathematical model makes numerous variations of system parameters and equipments feasible at low cost while providing sufficient environmental flexibility. A previous paper described the development and application of such a model for evaluation of traffic-handling capacity in the dense environment of the New York area. Applications of the model and conclusions and recommendations based on the results of its use are presented in this paper.

An Application of Random Process Theory to Gyro Drift Analysis—Robert L. Hammon (p. 84)

Improvements in gyro design within the last decade, particularly various floated gyro developments, make necessary a better understanding of the phenomenon of gyro drift rate. With this knowledge, it should be possible to improve gyro designs still further and to better estimate the error contribution of the gyro to complex vehicle control, guidance and instrument systems.

Generation of Artificial Electronic Displays, with Application to Integrated Flight Instrumentation—G. H. Balding and C. Süsskind (p. 92)

A novel method is described by which complex electronic signals are generated, dynamically varied, mixed, and presented on a standard video (raster-scan) display, without the use of vidicon or similar camera devices. The method is applied to the generation of a "contact-analog" display that provides a stylized representation of the real world to the pilot of an aircraft. This integrated display, which varies continuously as the speed, altitude, or attitude of the aircraft changes, also contains a "flight-path" representation that enables the pilot to maintain a prescribed path.

Wide-Base Doppler Very-High-Frequency Direction Finder—F. Steiner (p. 98)

Although it is quite well known that bearing errors occurring with multipath propagation can be reduced by using wide-base antenna arrays, only systems operating with phase or frequency modulation have come into practical use.

A method of progressively scanning a circular antenna array is described. This scanning which produces a frequency modulation in which the frequency deviation is a function of the bearing information, is accomplished by a rotating capacitive switch, and no vacuum tubes or crystal diodes are employed. Moreover, a special light indicator replaces the usual cathode-ray tube. Designed primarily for the very- and ultra-high frequencies, the equipment is quite simple and of high reliability.

Letter to the Editor (p. 106)

Correction to "Radio Collision-Avoidance Systems for Aircraft"—R. T. Fitzgerald, H. C. Brown, and M. D. Reed (p. 106)

Contributors (p. 107)

Antennas and Propagation

VOL. AP-8, NO. 6, NOVEMBER, 1960

A Theoretical Analysis of Semi-Infinite Conical Antennas—S. Adachi (p. 534)

A theoretical analysis of an antenna consisting of a perfectly conducting semi-infinite cone excited by a thin, linear element directed along its axis is presented. Two different methods are applied; one is a Green's function method, and the other is a mode theory. By the former method, the radiation characteristics of very thin and wide-angle cones excited by a sinusoidal current element are obtained. In the latter method, the linear element at the tip is replaced by a finite cone resulting in a semi-infinite, biconical structure. The variational principle is applied to determine the effective terminating admittance, and thus the input impedance, and the far-zone field. A guided wave which propagates longitudinally on the semi-infinite cone is identified and its properties are discussed.

Electrical Performance of Rigid Ground Radomes—W. Lavrench (p. 548)

The main purpose of a radome is to protect an antenna from the weather. Many designs of radomes can be evolved which will meet the mechanical requirements dictated by such factors as wind and snow load; however, these requirements are not sufficient. The radome must also have certain electrical characteristics in order that operation of the enclosed antennas is not degraded. This paper summarizes the many electrical measurements made on rigid ground radomes to date at the National Research Council to study the effect of the radomes on the performance of radar antennas.

Ground radomes made of thin single-skin, sandwich, and thick foam walls have been studied. Performance of single-skin radomes was found to be adequate for wavelengths of about ten centimeters and longer. In order to obtain maximum transmission, the skins must be thin and the panel joints must be small, few in number, and randomly spaced. Sandwich radomes provide a good design for wavelengths of five to ten centimeters. At wavelengths of three centimeters and shorter, the thick foam wall is believed to be the best solution, because in this construction joints between panels can be made practically invisible to the radiation. Transmission losses as low as one per cent have been measured.

Near-Field Measurements on a Logarithmically Periodic Antenna—R. L. Bell, C. T. Elfving, and R. E. Franks (p. 559)

Near-field measurements on a triangular-tooth log periodic antenna reveal that two waves exist on the structure. A transmission line wave travels from the apex to the "active region" of the antenna and excites currents in the teeth or radiating elements in this region. These currents, in turn, launch a radiated wave which accounts for the far-field pattern characteristics of the antenna. The antenna is shown to exhibit a pronounced degree of increased directivity.

Near-field measurements made through one period of operation show smooth variations of the field distributions with frequency.

Distribution Functions for Monopulse Antenna Difference Patterns—O. R. Price and R. F. Hyneman (p. 567)

Theoretical considerations of monopulse antisymmetrical or difference radiation patterns which have optimum properties in the Dolph-Tchebycheff sense are discussed. An approximate technique for synthesizing such patterns from linear arrays or continuous line sources is given. A highly desirable feature of the method is that the excitation function may be written as a simple modification of a (known) conventional Dolph-Tchebycheff excitation function. In addition, the method is also applicable to the synthesis of other specialized antisymmetrical patterns.

Radiation from a Tapered Surface Wave Antenna—Leopold B. Felson (p. 577)

Utilizing results obtained previously for the propagation of electromagnetic waves along a plane surface having a linear spatial variation of surface admittance, an approximate analysis of the radiation properties of a certain two-dimensional tapered surface wave antenna is carried out. The radiating structure consists of a surface waveguide of finite length having a linear susceptance variation, inserted between a feeding surface waveguide with constant

susceptance, and a perfectly conducting plane. The separate junction effects at the input and output ends of the taper are evaluated approximately for the case where the taper susceptance variation is gradual, and their combined influence on the radiation pattern is discussed.

Near-Field Gain of Aperture Antennas—Alan F. Kay (p. 586)

Formulas for the ratio η of received to transmitted power are examined for microwave aperture antennas at any range.

It is shown that with optimum aperture illuminations the far-field range equation continues to hold fairly well in the near field down to a distance at which it implies that nearly all the transmitted power is received! However, the aperture illuminations with maximum η (nearly 100 per cent) are different from the uniform, constant phase illumination which is optimum in the far-field case. The optimum near-field illuminations not only have the phase variation associated with elliptic rather than parabolic reflectors but they also have some amplitude variations. Some simple illuminations which can be realized practically by lenses and dishes are shown to be sufficiently close to the optimum cases for most practical purposes.

A formula for the power density in the near field of a transmitting aperture is also derived and it is shown how to maximize the power flow through any given area of space by design of the transmitting aperture illumination.

Measured Distribution of the Duration of Fades in Tropospheric Scatter Transmissions—K. F. Wright and J. E. Cole (p. 594)

Results of experimental measurements of fade durations at the output of tropospheric scatter receivers operating at a frequency of 950 Mc are presented. The special test equipment and the test procedures required to perform the measurements are described. The accumulated time the fades are below a reference level is shown. A family of curves representing the number of fades per hour which equal or exceed a given duration, and a family of curves representing the percentage of the total fades that equal or exceed different fade durations are presented. All the data are referenced to fade margin, which is defined as the difference between the received median level and the reference level. This enables the information given in this paper to be readily applied to other systems. A method for computing circuit reliability, based on the results of this paper, is suggested.

An Experimental Investigation of the Fock Approximation for Conducting Cylinders—L. Wetzel and D. B. Brick (p. 599)

The high-frequency current distributions over several conducting elliptic cylinders for normal, plane-wave excitation are measured at a wavelength of 3.2 cm using image-plane techniques. The experimental distributions are compared with the Fock approximation, verifying its validity over a wide range of kR_0 in the neighborhood of the shadow boundary.

Frequency Spectra of Transient Electromagnetic Pulses in a Conducting Media—W. L. Anderson and R. K. Moore (p. 603)

The energy density spectra of transient electromagnetic fields generated by a pulsed ideal dipole source in an infinite conducting medium have been investigated for various distances from the source. A characteristic frequency ω_c, corresponding either to the peak of the spectrum or to its half-width, is defined and shown to vary inversely as the square of distance at large distances. The behavior of ω_c with distance is a measure of the behavior of the pulse energy. Thus, at large distances it appears that the attenuation factor associated with ω_c, $\exp\{-r\sqrt{\omega_c\mu\sigma/2}\}$, is independent of r, due to the constancy of the product $r\sqrt{\omega_c}$. From this point of view, the transient fields do not decrease exponentially as r, but as inverse powers of r.

This should not be construed as meaning that the transient possesses an advantage over CW. The attenuation for monochromatic components of the pulse is the same as for continuous waves of the same frequency and at large distances the energy put into the high frequency components is wasted.

The phenomenon is illustrated by calculations that have been carried out for the case of pulses in sea water.

Reflection Factor of Gradual-Transition Absorbers for Electromagnetic and Acoustic Waves—Klaus Walther (p. 608)

Absorbers for electromagnetic or acoustic waves are described, for which a good impedance match and low reflection factor can be achieved by providing a gradual transition of material constants into the lossy medium. The reflection factor can be calculated by means of a Riccati-differential equation. General conclusions from the WKB-perturbation method can be drawn for absorbers, the layer thickness of which is either very small or very large in comparison to the wavelength. For "thin" layers, wave energy penetrates the whole thickness of the absorber. Suitable average values of the material constants are derived to describe the performance of the panel in this case. For "thick" layers only the initial part of the panel is energized. The asymptotic expressions contain only the material constants of this part. The results are interpreted physically. Numerical solutions of the reflection factor for highly refractive panels with exponentially varying material constants are reported.

A New Sporadic Layer Providing VLF Propagation—J. Ortner, A. Egeland, and B. Hultqvist (p. 621)

During two periods in May and July, 1959, following strong solar flares, the signal strength of receptions at Kiruna of VLF transmissions from Rugby (16 kc) showed no or only slight diurnal variation. It is proposed that the change of the diurnal variation is due to the production by solar protons of an ionized layer very deep in the atmosphere, the electron density of which is sufficient for reflection of very long waves but too low to cause measurable nondeviative absorption in the HF band at geomagnetic latitudes lower than approximately 60°.

Circuit Theory

Vol. CT-7, No. 3, September, 1960

Weissfloch Equivalents for Lossless $2n$-Ports—D. C. Youla (p. 193)

In many applications it is both customary and convenient to describe a $2n$-port M in terms of its transfer scattering matrix T. This representation is particularly apropos when making measurements on an obstacle coupling together n propagating modes in a waveguide.

In this paper canonical forms for T are established for *nonreciprocal* and *reciprocal* lossless $2n$-ports.

A Weissfloch equivalent circuit for the most general lossless $2n$-port (reciprocal or not) is derived and shown to be composed of three lossless $2n$-ports in cascade. The first and third are all-pass networks and the middle one a transformer bank of n uncoupled ideal 2-port transformers. A possible technique for measuring some of the parameters is described.

The Degenerate and Quasi-Degenerate Mode of Parametric Amplification—P. Bura (p. 200)

The analysis of this mode of parametric amplification is based on the theory of linear differential equations with periodically varying coefficients.

A steady-state (particular integral) solution of Matheiu's equation was obtained and expressions for gain, bandwidth and noise figure were derived for varying signal, pump and resonance frequencies. Similar expressions were derived for the lower-sideband or idler response. The gain and bandwidth of the idler response approaches that of the signal as the variation of capacitance is increased. When the fractional capacitance variation becomes equal to $2/Q$, oscillations at half the pump frequency are excited.

Due to the frequency inversion of the idler response, the practical application of the degenerate mode is very limited. In quasi-degenerate mode, when idler and signal responses are sufficiently removed to prevent the intermixing of the sidebands, both the gain and the noise figure deteriorate by approximately 3 db.

Modes in Linear Circuits—C. A. Desoer (p. 211)

The purpose of this review paper is to show that the concept of modes does apply to any linear time invariant circuit. This is accomplished by reducing the network equations to the standard vector form $\dot{y}=Ay+f$. In particular, it is shown that 1) any free oscillation of a linear circuit can be thought of as a superposition of non-interacting modes, 2) in the case of free oscillations, the amount of excitation of each mode can easily be expressed in terms of the initial conditions, 3) any forcing function excites each mode independently, and finally, 4) the resonance phenomenon is easily interpreted and the importance of the proper type of excitation is made obvious. Vector notation is used throughout. Examples of RC, RLC and active circuits are included.

Polynomials of Transfer Functions with Poles Only Satisfying Conditions at the Origin—Marcel J. E. Golay (p. 224)

The Butterworth polynomials, which satisfy amplitude conditions only at the origin, and the Bessel polynomials, which satisfy phase conditions only, are shown to be the extreme cases of a more general class of polynomials, which can be listed in a two-dimensional array, and which satisfy both amplitude and phase conditions. These polynomials are listed up to the seventh order, and a few general formulas are given which permit us to calculate these polynomials along certain lines of the two-dimensional array for any given order.

On the Solution of Networks by Means of the Equicofactor Matrix—G. E. Sharpe and B. Spain (p. 230)

In the solution of electrical networks, there arise matrices with the property that the sum of the elements of every row and of every column equals zero. On the node basis this is a direct consequence of Kirchhoff's current law coupled with the fact that the currents are invariant to a change of all node potentials by the same amount. As a consequence, all the *first* cofactors associated with determinants of such matrices are equal. The authors have named all such matrices *equicofactor matrices* and have based a general discussion of the solution of networks on these matrices. A new sign notation is introduced and problems of admittance-impedance conversion are treated. A proof is given of a theorem—called by the authors *Jeans' theorem*—which relates to the *second* cofactors associated with the determinant of the equicofactor matrix. This theorem is a consequence of the fact that, in the solution of networks, it is immaterial which node (mesh) is taken as reference and which equa-

tion is considered superfluous and suppressed from the given set, since the final answer must be the same.

The theorem also shows that only $(n-1)^2$ coefficients associated with an n-node (n-mesh) network are independent, regardless whether the network be described on an admittance or impedance basis. It is therefore concluded that there is perfect duality between the admittance and impedance description of networks, whatever their complexity.

Ladder Transformer Coupling Networks for Pulse Amplifiers and Hard-Tube Modulators—Thomas R. O'Meara (p. 239)

This paper discusses the problem of synthesizing a two-port network for coupling a pulse amplifier or a hard-tube modulator to a resistive load which may have an associated shunt capacitance. Coupling networks are limited to those capable of absorbing the lumped-parameter reactance equivalents of the high-frequency distributed parameters of a physical transformer. Thus, an important criterion for network performance is the relative ease with which the equivalent network elements of the transformer may be accommodated.

It is shown that one may obtain both decreased rise times and easier transformer accommodation, with step-down networks, by utilizing more complex coupling networks than the usual pulse transformer model. For further improvements, one should consider lowered values of driver impedance.

Step-up networks present a more difficult coupling problem, but appreciable enhancement in waveform and some reduction in rise time may again accrue through the incorporation of supplementary network elements.

Unit Real Functions in Transmission Line Circuit Theory—Leo Young (p. 247)

A new class of functions is introduced which has a direct physical significance in transmission line theory. These are called "unit real" (u. r.) and are derivable by bilinear transformations from positive real (p.r.) functions.

The complex reflection coefficient is a unit real function of the "line vector" $\exp(-2j\theta)$, where θ is the electrical length of a section of line in a resistor-transmisssion line circuit. Just as in lumped constant circuit theory the impedance is a p.r. function of the complex frequency. U.r. and p.r. functions are compared. A new proof and a discussion of Richards' theorem are also presented.

Positive Real Functions of Several Variables and Their Applications to Variable Networks—H. Ozaki and T. Kasami (p. 251)

This paper is concerned with networks containing variable parameters. The concepts of multivariable positive real function, multivariable reactance function, and multivariable positive real matrix are introduced, and it is shown that these concepts are useful for dealing with a wide class of variable parameter networks. Several theorems on these functions are established. Extensions of several conventional procedures of circuit theory are presented for the synthesis of such networks and their limitations are discussed. The last section concludes with a discussion of the approximation problem of networks with one variable parameter.

Terminal and Branch Capacity Matrices of a Communication Net—Wataru Mayeda (p. 261)

A communication net consists of branches representing communication channels with the weight of each branch being a positive real number which represents the capacity of transferring information through the branch (called a "branch capacity"). The terminal capacity between the vertices i and j of a communication net is the capacity of transferring information between the vertices i and j by considering the net as a whole.

To indicate the terminal capacities between all possible pairs of vertices in a net, a terminal capacity matrix is defined. Then the necessary and sufficient conditions for a terminal capacity matrix are given.

To represent the structure of a communication net, a branch capacity matrix is defined. Then the synthesis of a communication net from a given terminal capacity matrix is to obtain a branch capacity matrix from the given terminal capacity matrix.

Extension of Brune's Energy Function Approach to the Study of LLF Networks—Phillip Bello (p. 270)

An effective analytic approach to the study of the fundamental properties of driving point and transfer functions of RLC networks (also designated LLFPB networks) is based upon expressing the network functions in terms of energy functions associated with the network. Using this approach, Brune deduced the well-known necessary conditions on driving point and transfer functions of LLFPB networks. It is the aim of this paper to extend this approach to a class of active non-bilateral RLC networks (designated as LLF networks) generated by augmenting RLC networks through the addition of resistive, capacitive, and inductive multiterminal-pair devices which are not required to be passive or bilateral. In order to derive effectively the properties of LLF networks using the energy function approach, it is desirable to be able to analyze networks whose elements are multiterminal-pair devices. Such a method of analysis is suggested here as a generalization of a method due to Guillemin.

Using the energy function approach, necessary conditions are derived for driving point and transfer functions of several classes of LLF networks. In addition, some of these conditions are shown to be sufficient. Networks are considered which consist of resistors, inductors, and capacitors, both positive and negative, in addition to gyrators and generalized versions of gyrators (to an inductive and capacitive nature).

On the Brune Process for n-Ports—V. Belevitch (p. 280)

The Brune process for n-ports, established by Oono, McMillan, and Tellegen, is derived by an alternative method based on successive series and shunt extractions of passive n-ports containing fictitious complex resistances, which are finally eliminated by a simple equivalence transformation. The method is also applied to nonreciprocal n-ports, thus establishing that such an n-port of degree m is realizable with not more than m reactive elements. For reciprocal n-ports, the new derivation of Brune's process clarifies the physical structure of the reactive $2n$-port generalizing Brune's section and yields explicit formulas for its element values.

A Computational Method for Network Topology—Hitoshi Watanabe (p. 296)

This paper deals with methods for listing all possible trees and multitrees, and for determining the relative signs of tree determinants and multitree determinants, which are necessary for the analysis of networks. A connected linear graph having n elements and all of its possible subgraphs has been studied by mapping on an n-dimensional vector space having n base vectors, and a method for finding out a number of new trees from one tree, or a set of trees, has been derived. Also, a method of computation for determining the relative signs of tree determinants has been developed. These computations can be performed easily and effectively by a digital computer provided with bit-wise logical instructions.

On the Analysis and Synthesis of Single-Element-Kind Networks—E. A. Guillemin (p. 303)

This paper presents a method for the realization of a given nth order node conductance (or capacitance or reciprocal inductance) matrix as an $(n+1)$-node network with all positive elements and no ideal transformers. The first part establishes simple relations between branch conductances and elements in the given matrix which are assumed to be based upon a linear tree. These relations are analogous to the well-known ones pertinent to a so-called "dominant" matrix based upon the starlike tree. In an analysis problem they enable one to compute a single driving-point or transfer impedance with a minimum of computations. The second part of the paper develops a method whereby one can readily determine whether a given G matrix is based upon a tree (the necessary condition for its realization) and find the pertinent geometrical tree configuration when one exists. Once the latter is established, realization is simple and straightforward. The entire process requires no repeated trials and proceeds toward the desired goal with a minimum of effort.

Exact Design of Transistor RC Band-Pass Filters with Prescribed Active Parameter Insensitivity—I. M. Horowitz (p. 313)

The design of low-frequency band-pass filters by means of RC rejection networks in the feedback path of active elements has long been known. The advent of the transistor has renewed interest in this field and has necessitated a more exact synthesis procedure. The reason for this is that in the classical design, the active element is assumed to be an ideal voltage amplifier with infinite input impedance, zero output impedance, and zero reverse transmission. The transistor satisfies the dual ideal assumptions to a considerably lesser degree than the vacuum tube. The sensitivity of the transistor parameters to temperature also requires that more attention be paid to the effect of parameter variations on the filter response.

This paper extends the classical theory in several directions.

1) A synthesis procedure is developed in which the finite input and output impedances and reverse transmission are taken into account.

2) The freedom that exists in the synthesis procedure is used to obtain a design with a least active element. Graphs are presented which provide the values of four of the six required network elements. Two simple equations must be solved for the other two.

3) Expressions are developed for the sensitivity of the filter bandwidth and center frequency to the four low-frequency active parameters. It is presumed that the design specifications include a statement of the extent of active parameter variation and of the tolerances on the filter response. The procedure for satisfying such specifications is an integral part of the design procedure.

An example which includes all of the above features is worked out in detail.

A Frequency-Domain Theory for Parametric Networks—B. J. Leon (p. 321)

This paper presents a frequency-domain method for analyzing the transient and steady-state behavior of a class of linear, variable parameter networks defined as follows:

A "*lumped, linear, parametric network*" (LLPN) consists of a finite number of lumped circuit elements, R's, L's, and C's, whose values vary periodically with time, imbedded in a network of fixed R's, L's, C's, and sources. In any particular LLPN, the frequencies of all the time-variant elements are commensurable. The method of analysis, based upon the theory of linear difference equations, is exact. There are no approximations which restrict the analysis to networks containing sharply tuned filters. For a single sinusoidally varying element, a precise numerical method that is readily performed by a digital computer is pre-

sented. In addition, some interesting properties of single-element linear parametric amplifier networks are presented.

Necessary and Sufficient Conditions for the Existence of ±R, C Networks—B. K. Kinariwala (p. 330)

Necessary and sufficient conditions for the existence of networks containing positive resistors (+R), negative resistors (−R), and positive capacitors (C) are presented. It is shown that the elements of the open-circuit impedance matrices of ±R, C n-ports can have poles only on the real axis of the complex frequency plane and these poles must be simple. The matrices of residues in all the finite poles must be positive semidefinite, and if there are any poles at infinity the matrices of residues in them must be negative semidefinite. These conditions are sufficient as well as necessary. Further, any matrix satisfying the above conditions can be characterized by a passive RC n-port, in a modified frequency variable, with a negative resistor added in series at each of the ports. As a consequence of these conditions, driving-point impedance functions of ±R, C networks can have only simple zeros and poles alternating on the real axis and the residues in all the finite poles must be positive.

Theoretical Bounds on the Performance of Sampled Data Communications Systems—J. J. Spilker, Jr. (p. 335)

A general derivation is given for the minimum mean squared error in the smoothed output of a sampled data communication system. The message which is to be sampled and transmitted is assumed to be a stationary random function of time and is not strictly bandlimited. The results presented here are more general than previous calculations because the message spectrum has an arbitrary cutoff rate, the sampling duration can be finite, and "white" noise is assumed introduced into the system by transmission.

Filtering of the message before sampling is shown to allow a smaller minimum error than without such filtering, even though the error is determined with respect to the original unfiltered message. The transfer function of the optimum presampling filter is derived as well as the corresponding optimum smoothing filter.

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Communications Systems

Vol. CS-8, No. 3, September, 1960

Frontispiece and Guest Editorial (p. 139)

The Comparison of Digital Communication Systems—C. W. Helstrom (p. 141)

Two methods are proposed for comparing the performances of digital communication systems differing in the number of available signals, in bandwidth, in rate of transmission, and in complexity. The systems are ranked on the basis of the probability of correct reception of transmitted messages. The signal durations are adjusted so that the systems have either equal bandwidths or equal rates of transmission. The concept of "strictly comparable systems" is introduced; for these the two methods lead to the same ranking. From one group of strictly comparable systems to another, the reliability of communication tends to decrease as the relative rate of transmission increases or as the bandwidth decreases. A number of systems are graphically compared by these methods, including some to which parity-check coding has been applied. The advantage over binary systems of systems of higher order, in which more than one kind of signal can be transmitted, is illustrated.

Combined Digital Phase and Amplitude Modulation Communication Systems—Charles R. Cahn (p. 150)

The performance of phase modulation communication systems is investigated for the asymptotic case of a high signal-to-noise ratio. A simple and excellent approximation to the probability of error is derived for both coherent and phase-comparison demodulation. In addition, a simple expression is derived for the asymptotic degradation of phase-comparison demodulation.

When the number of bits per sample of the signal is large, a combination of digital amplitude and phase modulation is found to make more efficient use of transmitter power than phase modulation alone. The number of amplitude levels may be optimized for either minimum peak power or minimum average power, using the approximate expressions for probability of error. While an analytical solution can be found for the peak power case, a numerical solution with restriction to powers of two appears preferable, and is necessary for the average power case. Accordingly, tables showing the optimum numbers of levels with this restriction are presented.

A New Transmission Method for Pulse-Code Modulation Communication Systems—A. P. Brogle (p. 155)

This paper presents the results of a study of the basic factors underlying the selection of a preferable method of transmission for pulse-code modulation communications systems. A new method of transmission, called biternary, is described and is compared with quaternary transmission, as a means of doubling the channel capacity of PCM systems without requiring increased bandwidth or transmission facilities. It is found that biternary transmission is more tolerant of the effects of all types of interference than quaternary transmission, and significantly reduces a major problem of quaternary transmission excessive errors, caused by low frequency cutoff effects. The use of biternary transmission is planned in present and future military pulse-code modulation communication systems.

Cozi Oblique Incidence Ionospheric Soundings Using Normal Communication Transmission—L. C. Edwards and D. A. Hedlund (p. 160)

Oblique incidence backscatter soundings have long been used in probing the ionosphere. These have normally employed pulse transmissions and thus have required either special equipment, or special modifications to existing communications equipment for transmission and reception of such signals. A new technique has been developed which allows normal communication or broadcast transmissions to be used for backscatter sounding. It involves a cross correlation performed between the transmitted signal and the returned backscatter signal. The use of re-entrant delay lines as storage devices permits continuous real time cross correlations of relatively long samples of the waveforms. An A-scope presentation of the cross correlation function serves the same purpose as an A-scope display of the backscattered pulse signal. An intensity modulated range-time display of the cross correlation function, very similar to the range-time display commonly employed in ionospheric sounding, can provide a continuous record of skip distance variations. Samples of experimental data obtained using this technique are presented.

Use of Optical Frequencies for Space Communication—Cecil B. Ellis (p. 164)

The spectrum from the infrared through the visible to gamma rays has been surveyed for signalling from Earth or an Earth satellite to a spaceship at planetary distances. The best region for signalling from a satellite vehicle appears to be from 2000 to 400 angstroms. One information bit per second could be sent for a distance many times the diameter of the solar system. If the source is to be on the Earth's surface, the best wavelength region would be 4000 to 3000 angstroms. One could probably then reach the neighborhood of Mars at one bit per second when that planet is closest to the Earth. Greater distances would be possible at slower information rates.

Radio Relaying by Reflection from the Sun—D. J. Blattner (p. 169)

The possibility of using radio reflection from the sun to provide a communication link supplementing that using moon reflections is investigated analytically. Reflection and absorption of an incident signal in the solar atmosphere, and thermal noise radiated by the sun, are considered together with transmitter capabilities to find the operating frequency giving optimum signal-to-noise ratio. The design principles for a receiver which can separate the signal from the noise are indicated. Finally, achievable signaling rates and reliability are estimated.

Fading Loss in Diversity Systems—Martin Brilliant (p. 173)

In a communication system using optimum diversity combining, the mean signal-to-noise ratio of the combined signal is the sum of the mean signal-to-noise ratios of the separate signals. However, the effective signal-to-noise ratio of the combined signal is less than this. The ratio of the mean to effective signal-to-noise ratios of the combined signal is called the fading loss.

The effective signal-to-noise ratio, and hence the fading loss, depends upon the measure of effectiveness used, which in turn depends upon the form of information conveyed by the signal. In a high-quality speech system, the fading loss is shown to depend principally upon the order of diversity (the number of signals combined). In a binary communication system, the fading loss is shown to depend principally upon the mean signal-to-noise ratio of the separate signals. The system design considerations in these two cases are therefore different.

The Design of Wide-Band Scatter Systems—M. O. Felix (p. 177)

The modulation bandwidth that a scatter system can handle is mainly determined by the transmitting and receiving antenna beamwidths. A higher carrier frequency, therefore, permits the use of a smaller antenna. The transmitter power may then be chosen to give an adequate carrier-to-noise ratio.

A method of reducing the differential delay in diversity receivers which extends the modulation band a given scatter system can handle has been developed.

IF amplifiers in wide-band scatter systems are a particularly difficult compromise between performance and ease of maintenance. To date it has not proved possible to use phase equalizers on these circuits, and between 1 and 2 db of threshold must thereby be sacrificed.

IF combining is attractively simple, but even with delay correction, it is doubtful whether the phase can be locked to the required accuracy at low carrier-to-noise ratios. The base-band combiner is more complex but can be made to operate up to modulation frequencies of 5 Mc. Its operating range is somewhat restricted, however.

FM and SSB Radiotelephone Tests on a VHF Ionospheric Scatter Link During Multipath Conditions—J. W. Koch, W. B. Harding, and R. J. Jansen (p. 183)

Experiments have been carried out on an ionospheric-scatter link to observe the effects of long-delayed multipath signals, caused by F_2 propagated back scatter, on the intelligibility of voice communication. Frequency modulation and single-sideband modulation equipments were used for the tests. During periods when the back-scatter signal levels approached the level of the normal ionospheric-scatter sig-

nals, the frequency-modulation voice transmissions were unintelligible; however, under the same conditions, single-sideband voice communication intelligibility remained at almost 100 per cent although there was some loss in quality.

Criteria for the Ultimate Capability of the Optimized Tropospheric Scatter System—C. A. Parry (p. 187)

Behavior of the tropospheric scatter mechanism is now sufficiently well understood to permit a determination of optimum transmission criteria. The requirements for optimization are established from the channel signal-to-noise ratio equation. It is shown that the optimum is related not only to the basic RF transmission loss, but also to the effective noise figure, antenna gain, and medium aperture loss.

It is considered that if a minimum product of antenna height, path length, and frequency are maintained, there will be a cubic relation between path loss and frequency. When the frequency dependence of the other factors is also taken into account, it is found that the net result will depend either directly or inversely upon frequency, depending upon the choice of system parameters. On this basis, and by using a graphical solution, an optimum frequency is found, for which the system gain maximizes. It is seen that, for a given antenna, the product of frequency and path length is substantially constant. From this, it is found that the minimum product of antenna height, path length, and frequency is achieved, so validating the use of the initial cubic relation. It is shown that when the optimum frequency is used, the associated medium aperture loss is rather small, so that improved accuracy in the determination of this factor is unlikely to produce substantial improvement in the optimized system. Also, the plane wave antenna gain is not exceptionally high, so that structures which are more economic than paraboloidal types may be contemplated

Curves for path loss vs distance are derived using optimum frequencies; total loss curves for 99.9 per cent reliability of the optimized system are also shown. This data is used to establish a series of system capability curves which are directly related to transmitter power, noise bandwidth and the signal-to-noise ratio at receiver input. It is considered that with the optimized system, very low power may be used to carry high-capacity circuits over quite long spans.

Simple Methods for Designing Troposcatter Circuits—Leang P. Yeh (p. 193)

As troposcatter circuits come more and more and more widely into use, there is a need for simple and reasonably accurate design methods for routine use, since the speed of obtaining a suitable design is sometimes of the utmost importance.

This paper attempts to present such a method, derived primarily from experimental data, but with occasional reliance upon theoretical calculations. Certain essential design factors, some of which are still rather controversial, such as path loss and correction factors caused by terrain and climatological effects, aperture-to-medium coupling loss, etc., are discussed in detail. Circuit reliabilities determined from combining instantaneous signal-fading distributions are briefly described. Sets of appropriate curves in simple form are proposed for practical engineering applications.

Component Parts

Vol. CP-7, No. 3, September, 1960

A Recommended Standard Resistor-Noise Test System—G. T. Conrad, Jr., N. Newman, and A. P. Stansbury (p. 71)

This paper describes a recommended standard resistor-noise test system, with the theory of operation given in considerable detail. The system provides for the measurement of a definitive resistor-noise quality *Index*. This *Index*, the "microvolts-per-volt" *Index*, is a modified form of the "conversion gain" index formerly used at NBS. The *Index* is a decibel expression for the number of microvolts of noise per volt of applied dc voltage transmitted in a frequency decade. A practical example is given to illustrate how the *Index* may be used to calculate the magnitude of current noise generated by fixed resistors in a given application. To complete the example, the combined effects of thermal noise, tube noise, and current noise are then considered.

A description is also given of an existing test set which is based upon specifications associated with the recommended measuring system. The full specifications for this set are given, and distinctive design features are discussed. The simple operation of the test set and the computation of the *Index* are carefully explained.

Symposium on Tantalum Capacitors—W. M. Allison, S. W. Bubriski, H. D. Hazzard, and R. J. Millard (p. 88)

This article gives a description of the state of the art insofar as small tubular tantalum capacitors for military and industrial applications are concerned. Foil anode paste-electrolyte, sintered-anode liquid-electrolyte, and solid-tantalum capacitors are described and their performance characteristics discussed. Data on reliability of the various types are presented.

The Transient Effect in Capacitor Leakage Resistance Measurements—Raymond W. France (p. 106)

The leakage resistance of capacitors as a function of time is a characteristic to be considered in the choice and control of capacitors, especially in many modern military electronics applications. This paper, by the use of transient circuit analysis, shows why most leakage resistance data accumulated in the electronics industry for capacitors are invalid. Valid data can be obtained by using low resistance meters to make such measurements. Valid experimental curves of leakage resistance vs time for thirteen types of capacitors, each type employing a different dielectric combination, are shown; and the significance of these curves is discussed

Engineering Management

Vol. EM-7, No. 3, September, 1960

Work Measurement and Productivity in Engineering Design—H. W. Martin and R. J. Thomson (p. 83)

Analysis of design engineering functions has suggested the practicality of determining the normal degree of their occurrence by means of supervisor samplings of the elements of work being done during representative work periods. Such sampling data can be analyzed to determine 1) the intrinsic time-out or job fatigue trends; 2) elemental work profiles for each representative work category; 3) productivity indexes for each organization or any appropriate section thereof. The sampling data may also be correlated with time charges to projects and subdivisions thereof to determine time standards. Thus, analysis of the sampling data and correlative statistics may provide bases for improved control of project costs, personnel characteristics, and productivity. Data derived from an experimental application of these concepts to a sizable civil engineering organization are presented.

The Application of Closed-Loop Techniques to Engineering Project Planning—R. W. Haine and W. Lob (p. 96)

The techniques described in this paper to control research, development, and engineering projects are adaptations of those developed and well-proven methods used for controlling manufacturing processes.

To complete an engineering project to meet established specifications, within allotted funds and in the scheduled time, it is necessary to program the various phases and requirements of the project in great detail. The use of a project schedule chart as a formal tool of project management increases the project engineer's ability to evaluate quantitatively project status. Information about the progress made toward meeting the project goals can be used in a closed-loop system to initiate corrective action when there are deviations from scheduled plans.

The project schedule chart as a basic source of information has other applications in the management of an engineering organization. For example, the tabulation of schedule chart data by means of punched cards facilitates rapid evaluation of the quantitative needs for manpower, funds, and facilities within the organization. Evaluation of project performance through simplified analysis of project activity at all levels of management directs attention to "problem" projects. Data processing, including coding and tabulation of data, implements control of the projects, the project group, the system groups, the laboratories, and the common support activities which, when taken altogether, make up an engineering department.

A Generalized Network Approach to Project Activity Sequencing—Raoul J. Freeman (p. 103)

R & D projects are viewed as networks of interrelated events to be achieved in proper ordered sequence. This paper generalizes some earlier work. The present paper takes cognizance of technical performance and scarce resources as well as time. By means of the analysis presented here, it is possible to find the optimal combination of time, technical performance level, and resources for any project.

What is the Role of the Government Laboratory?—A Questionnaire Study in One Government Laboratory—Eugene Walton (p. 114)

A sample of the top scientists and engineers in a large government laboratory were interviewed in depth about the role of the Government laboratory in the total American defense structure. Six categories of answers were obtained, indicating a range of roles which are not mutally exclusive.

A Model for Planning Study-Type Contracts—D. R. J. White and R. Adm. T. J. Hickey USN (Ret.) (p. 117)

A decision regarding the best scope and depth of effort is often difficult to make in writing proposals for study contracts. A model is presented for systematizing this decision making. The factors considered include: contract price, various components of cost and profit. A "potential performance capability" is defined, and its use is illustrated. An example of the suggested method of analysis is given.

Human Factors in Electronics

Vol. HFE-1, No. 2, September, 1960

Determination of Human Operator Functions in a Manned Space Vehicle—Charles Owen Hopkins (p. 45)

Man's participation in limited space travel is imminent. Attention must be focused now upon the nature and extent of his participation in future manned space systems. It is imperative that the human not be assigned functions as an afterthought. Rather, functions must be assigned in a manner that will optimize system performance with respect to the mission requirements. This paper describes a practical methodology for determining the human operator functions within the context of a specific mission. A space ferry mission is used to illustrate the approach.

Evaluation of Aircraft Steering Displays—A. Z. Weisz, J. I. Elkind, B. C. Pierstorff, and L. T. Sprague (p. 55)

A number of radar steering display designs utilizing the moving-airplane principle were compared with the standard Air Force moving-horizon display in a series of simulator experiments. Significant improvement in tracking performance for military pilots with and without prior fire-control experience was found for a display which incorporated rate feedback and pursuit tracking features in addition to the moving-aircraft principle. Results of smaller-scale tests with naive and relatively inexperienced subjects are also reported.

A Comparative Evaluation of a Pursuit Moving-Airplane Steering Display—D. K. Bauerschmidt and S. N. Roscoe (p. 62)

An experiment was conducted using a flight simulator to determine the relative ease with which pilots can learn to use four types of airborne fire-control system steering displays. The four displays compared were 1) a moving-horizon display with a space-stabilized error dot, 2) a moving-horizon display with an aircraft-stabilized error dot, 3) a compensatory type moving-airplane display, and 4) a pursuit type moving-airplane display. Of the four displays the moving-airplane types were found to yield significantly smaller firing errors and require less learning as compared to either moving-horizon type display. Furthermore, the pursuit type of moving-airplane display yielded learning performance and terminal performance error levels superior to any of the other displays.

Coding Electronic Equipment to Facilitate Maintenance—J. H. Ely, N. B. Hall, and C. E. Van Albert (p. 66)

The aim of this study was to improve maintenance of electronic equipment by determining what information to place on the equipment and developing techniques for its display. Trips to various communications installations were made in order to examine equipment, observe maintenance activities, examine manuals, and interview personnel. Detailed data were collected showing the marked variation between observed test point readings and those called for in maintenance manuals. Recommendations were developed concerning information to be displayed on prime electronic equipment, covering: 1) designation of functional groupings, 2) identification of signal paths, 3) identification and sequence for using test points, and 4) presentation of historical information for each test point. These recommendations were evaluated by incorporating them on an oscilloscope; comparing this "coded" scope with an identical uncoded one showed that trouble-shooting time was reduced on the average to approximately one-half that for the uncoded equipment.

A Minimum Analog Driving Simulator—David B. Learner (p. 69)

System requirements were developed for a minimum cost and fidelity simulator appropriate for the study of driving behavior. The simulator is composed of three sub-systems: a pulsewidth modulation recording and reproducing unit to provide road geometry, a vehicle dynamics computer to solve the automobile motion equations, and a cathode-ray tube display that provides a representation of the visual information required by the driver.

Industrial Electronics

Vol. IE-7, No. 2, July, 1960

A New Digital Computer System for Commercial Data Processing—J. A. Brustman (p. 2)

A computer system, the RCA 501, has been designed to meet the needs of commercial data processing. The equipment utilizes transistors as active elements, ferrite cores for high-speed memory, magnetic tape as primary bulk and working store, and built-in and programmable accuracy control. Input-output equipment includes paper tape (in), card (in and out), and line printer (out).

The language of the computer system exploits variable-word and variable-message-length for efficiency. The instruction complement is designed to facilitate the programming of data-processing tasks, taking advantage of the variable word and message and of built-in simultaneous operation provisions.

The system is adaptable in size to small and large applications.

The Operational Information System and Automation of Sterlington Steam Electric Station—Joseph A. Reine, Jr. (p. 14)

The system for scanning and logging operational data at Sterlington Electric Station is described. This advanced system includes the sensors, scanning equipment, analog-to-digital converters, data storage, computer, and various output presentations. Operating experience and problems associated with incorporation of the system into normal plant operation are described.

Production-Line Testing Programmed by Punched Cards—Richard E. Wendt, Jr. (p. 20)

Automatic equipment for production-line testing of power capacitors provides advantages in speed and accuracy over previous manual testing. The equipment described provides means for automatic part handling, test selection, data collection and interpretation, and test results recordings.

The Universal Elements of Multipurpose Automatic Test Systems—Ibrahim H. Rubaii (p. 24)

To assure the continuing satisfactory operation of a complex bombing-navigation and missile guidance system, extensive efforts must be expended in the testing process, which depends heavily upon the test system. In this paper, the testing process and systems are treated in analytical fashion. The system is divided into basic functional elements that are universal to all test systems. These functional elements, or subsystems, are then integrated into a theoretical automatic multipurpose system; boundary conditions imposed on this general system would lead to any special-purpose test system.

The theoretical model created is useful:

1) in designing any test system where boundary conditions are imposed;
2) in evaluating and standardizing existing and proposed text systems for a specific application; and
3) in extending available techniques of analysis in the fields of communication, computing, and control systems to the important, integrated system testing and test systems.

A New High-Power Electron Accelerator—M. R. Cleland and K. H. Morganstern (p. 36)

An electron accelerator for industrial use has been developed which provides improved efficiency and reduced cost of operation. The design incorporates a unique dc accelerating voltage supply consisting of cascaded rectifiers driven in parallel from an RF oscillator. Data are given for equipment rated up to 3 mev, 30 kw.

Microwave Theory and Techniques

Vol. MTT-8, No. 6, November, 1960

Design of Wide-Band (and Narrow-Band) Band-Pass Microwave Filters on the Insertion Loss Basis—George L. Matthaei (p. 580)

A method for design of band-pass microwave filters is described that combines the image and insertion-loss points of view to give an approximate design method having simplicity, but also high precision. This method is applicable for filter designs ranging from narrow to very wide bandwidths (2 to 1 or more). The desired insertion loss characteristic is obtained by use of a lumped-element, Tchebycheff, or maximally flat (or other) low-pass prototype. With the aid of the concept of impedance inverters, the prototype is converted into a cascade of symmetrical (but differing) sections. The image properties of symmetrical sections of the band-pass microwave filter structure are then related to those of corresponding sections of the prototype. Straightforward design equations are given for filters using short-circuited or open-circuited stubs, and also for filters using parallel-coupled lines. Mapping functions are derived that permit accurate prediction of the microwave filter cutoff characteristic from that of the prototype. The responses of a number of filter designs were computed, and a Tchebycheff filter with a 2.2 to 1 bandwidth was built and tested. The responses of all the filter designs were in close agreement with the prescribed characteristics, and the accuracy of the mapping functions was verified.

Radio-Frequency System of the Cambridge Electron Accelerator—Kenneth W. Robinson (p. 593)

The requirements for the RF system of the Cambridge Electron Accelerator are investigated and the choice of the major parameters of the system is discussed. The strongly coupled waveguide cavity system is analyzed and the performance of the system with various types of imperfections is calculated.

Model Studies of a Strongly Coupled Synchrotron RF System—A. E. Barrington, J. Dekleva, and J. R. Rees (p. 597)

The strongly coupled multicavity synchrotron RF system proposed for the 6-bev Cam-

bridge Electron Accelerator operates at 475 Mc and, because of its large size, presents complex problems of assembly and tuning. To achieve a better understanding of the characteristics of the system, a scaled model operating at 9000 Mc was constructed. The work was undertaken in two stages; first a simple single-cavity ring was studied and later a more complicated double-cavity ring. An account is given of the design of cavities and waveguide links of variable electrical length, and instrumentation devised for various measurements is described. This is followed by experimental data which were in good agreement with theoretical predictions. Recommendations arising from the model study for the assembly and tuning of the 475-Mc system are put forward.

Operation of the Field Displacement Isolator in Rectangular Waveguide—R. L. Comstock and C. E. Fay (p. 605)

A field displacement isolator in WR-159 rectangular waveguide consisting of a full height ferrite slab having a resistive film on one face is treated analytically. The resultant transcendental equation was programmed for a computer and values of the propagation constant found in the frequency range 5.90 to 6.45 kMc for various film resistivities. Two TE modes are found to exist whose relative behavior depends on the resistivity of the film.

Reasonably close experimental verification of the results was obtained for the total attenuation and for the predicted E-field distributions by E-field probe tests. Additional attenuation above that predicted by the theory for a single mode is observed as a reult of an interference at the end of the ferrite.

A partial height ferrite slab isolator was subjected to E-field probe tests. The field distributions were found to be similar to the full height case. Here, also, additional attenuation is obtained at some frequencies as a result of an interference.

Peak Internal Fields in Direct-Coupled-Cavity Filters—Leo Young (p. 612)

Microwave filters are limited in their power-handling capacity by high fields generated inside the filter.

Simple formulas are derived here for the peak fields inside each cavity of a direct-coupled-cavity filter at any frequency. The computed peak fields in each cavity of a three-cavity, a four-cavity, and a six-cavity filter as a function of frequency are reproduced up to several harmonics. Inside the pass band, the internal fields are generally minimum at center frequency, rising to sharp peaks just outside the pass band.

Phase characteristics were also computed, and their relation to the internal field amplitudes is explained.

Mismatch Errors in Microwave Phase Shift Measurements—G. E. Schafer (p. 617)

The phase difference between the incident and transmitted waves at the input and output ports, respectively, of a two-arm waveguide junction in a reflection-free system is a characteristic of the waveguide junction and is defined as the "phase shift." The difference between the phase shift in a reflection-free system and the "change of phase" observed in a system which is not reflection-free will be termed mismatch error. The mismatch error depends not only on the reflections present in the system, but also on the choice of the wave used as the reference wave in a phase measurement. Similar considerations hold for the measurements of variation of phase shift and the observed change of phase in adjustable components.

A formal scattering matrix analysis is used to derive expressions for phase relationships of the wave amplitudes for a two-arm waveguide junction in a system with reflections. The results of this analysis are used to evaluate mismatch error for different choices of reference waves. Two techniques of variation of phase-shift measurements are analyzed. Graphs of the limits of mismatch error in a commonly used method of measurement are presented.

A Note on the Optimum Source Conductance of Crystal Mixers—R. J. Mohr and S. Okwit (p. 622)

This paper describes an accurate and convenient technique for measuring the match of a crystal mixer. Use is made of the fact that with a proper RF drive level, the fundamental conductance of a mixer crystal may be made equal to the optimum source conductance of the crystal for mixer operation. The required drive level depends on certain crystal parameters and on the image frequency termination of the mixer. Design curves are given which simplify the determination of the proper RF drive level for a wide range of crystal parameters and their condition of image frequency termination.

Microwave Switching with Low-Pressure Arc Discharge—R. M. Hill and S. K. Ichiki (p. 628)

The characteristics of a low-pressure, hot cathode arc discharge have been studied and applied to microwave switching applications. The combination of rapid plasma build-up, low ignition voltage, and fairly rapid plasma decay, offers promise for the development of broadband, high-power microwave switches which can be closed in tenths of microseconds and opened in a few microseconds or less. Experimental results on some particular switches are reported.

Characteristic Impedances of Broadside-Coupled Strip Transmission Lines—Seymour B. Cohn (p. 633)

Formulas are given for the even- and odd-mode characteristic impedances of shielded coupled strip-transmission-line configurations that are especially useful when close coupling is desired. Applications may be made to wide-band coupled-strip-line filters, 3-db directional couplers, and many other components. The cross sections considered are thin broadside-coupled strips either parallel or perpendicular to the ground planes. Modification of the formulas for thick strips is discussed. The derivations are outlined, with particular attention given to the underlying assumption that restricts the use of the formulas to cases of close coupling.

Thickness Corrections for Capacitive Obstacles and Strip Conductors—Seymour B. Cohn (p. 638)

Capacitive thickness corrections are derived exactly for two basic geometries involving pairs of semi-infinite plates. In one arrangement, the pair of plates are coplanar, while in the other they are parallel to each other. In each case the total capacitance per unit length between the pair of plates is infinite, but the incremental increase of capacitance when the thickness is increased from zero to a value t is finite. These capacitance increments are evaluated, and it is shown how they may be used as approximate thickness corrections in a great variety of more complicated geometries involving capacitive obstacles in waveguide, coaxial line, and artificial dielectric media. They may also be applied to coupled-strip-line conductors. As examples, the corrections are applied in detail to a waveguide iris, and to three useful coupled-strip-line cross sections.

Inhomogeneous Quarter-Wave Transformers of Two Sections—Leo Young (p. 645)

An inhomogeneous transformer is defined as one in which the guide wavelength is a function of position; for a homogeneous transformer, the guide wavelength is independent of position.

A previous paper has dealt with inhomogeneous transformers of one section; the existence of an optimum design (which is never homogeneous) was demonstrated. The mathematical tools for inhomogeneous transformers of two or more sections have been presented in another paper. Our purpose here is to apply these results to the solution of the two-section inhomogeneous transformer.

The maximally flat ideal transformer was solved exactly and the design equations verified by subsequent numerical analysis. An approximate procedure to improve the performance over a finite bandwidth (similar to the Tchebycheff response of homogeneous transformers) is also explained.

Errors in Dielectric Measurements Due to a Sample Insertion Hole in a Cavity—A. J. Estin and H. E. Bussey (p. 650)

The measurement of complex permittivities of isotropic media at microwave frequencies is performed with high precision by means of cylindrical cavity resonators. However, a hole in the cavity wall for inserting the sample causes a frequency pulling of the resonator, which in turn introduces an error in the measured dielectric constant. These effects are measured, and with perturbation theory as a guide, correction factors are developed.

Correction—D. S. Lerner and H. A. Wheeler (p. 653)

A Pre-TR Tube for High Mean Power Duplexing—D. W. Downton and P. D. Lomer (p. 654)

A gas discharge tube for transmit-receive switching capable of handling average power levels up to at least 25 kw at 3000 Mc is described. The discharge is excited in the annular space between two concentric silica tubes, and recovery time is controlled by the dimensions and gas pressure. In this way, a tube with constant characteristics during life has been achieved. The tube is mounted in a thick resonant iris, and sparking is avoided by using accurately ground silica mounted in a precision-bore hole.

The arc loss of the tube in this form of mount is less than 0.1 db at 5 Mw peak 10 kw average, and the recovery time is about 100 μsec to 3 db. The attenuation is about 30 db, and the insertion loss is less than 0.1 db.

Performance of this form of tube is discussed for average power levels of up to 50 kw in a phase-shift duplexer and 25 kw in a balanced duplexer, and the expected performance during life is also considered. Lives in excess of 10,000 hours are deduced from extrapolated data obtained with radioactive krypton in tubes operating at 10 kw average.

Circular Electric Mode Directional Coupler—Bunichi Oguchi (p. 660)

This paper describes a circular electric mode directional coupler, composed of two coaxial bifurcations in circular waveguide. The coupling coefficient of the directional coupler depends on the separation between the two bifurcations, and a hybrid junction for the circular electric mode may be obtained at the proper separation. The analysis is carried out in terms of scattering matrix elements characterizing each coaxial bifurcation.

The scattering matrix elements were experimentally determined via the Weissfloch tangent method at 5000-Mc band. For convenience, experiments were carried out in sectoral waveguide instead of circular waveguide. Measured characteristics at 9000-Mc band are in good agreement with values determined by circuit calculations employing parameters of the coaxial bifurcation measured at 5000-Mc band. For the case of a hybrid junction, wide-band matching has been accomplished and verified experimentally. Applications of this directional coupler are outlined.

Abstracts and References

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NOTE: The Institute of Radio Engineers does not have available copies of the publications mentioned in these pages, nor does it have reprints of the articles abstracted. Correspondence regarding these articles and requests for their procurement should be addressed to the individual publications, not to the IRE.

The number in heavy type at the upper left of each Abstract is its Universal Decimal Classification number. The number in heavy type at the top right is the serial number of the Abstract. DC numbers marked with a dagger (†) must be regarded as provisional.

UDC NUMBERS

Certain changes and extensions in UDC numbers, as published in PE Notes up to and including PE 666, will be introduced in this and subsequent issues. The main changes are:

Artificial satellites:	551.507.362.2	(PE 657)
Semiconductor devices:	621.382	(PE 657)
Velocity-control tubes, klystrons, etc.:	621.385.6	(PE 634)
Quality of received signal, propagation conditions, etc.:	621.391.8	(PE 651)
Color television:	621.397.132	(PE 650)

The "Extensions and Corrections to the UDC," Ser. 3, No. 6, August, 1959, contains details of PE Notes 598–658. This and other UDC publications, including individual PE Notes, are obtainable from The International Federation for Documentation, Willem Witsenplein 6, The Hague, Netherlands, or from The British Standards Institution, 2 Park Street, London, W. 1, England.

ACOUSTICS AND AUDIO FREQUENCIES

534:061.3 4078

Program of the 59th Meeting of the Acoustical Society of America. (*J. Acoust. Soc. Am.*, vol. 32, pp. 912–942; July, 1960.) Summaries of papers presented at the meeting held at Providence, R. I., June 9–11 1960, are given.

A list of organizations which have available English translations of Russian journals in the electronics and allied fields appears at the end of the Abstracts and References section.

The Index to the Abstracts and References published in the PROC. IRE from February, 1959 through January, 1960 is published by the PROC. IRE, June, 1960, Part II. It is also published by *Electronic Technology* (incorporating *Wireless Engineer* and *Electronic and Radio Engineer*) and included in the April, 1960 issue of that Journal. Included with the Index is a selected list of journals scanned for abstracting with publishers' addresses.

534.26 4079

The Diffraction of a Plane Wave through Two or More Slits in a Plane Screen—E. B. Hansen. (*Appl. Sci. Res.*, vol. B8, no. 2, pp. 73–83; 1960.) The diffraction of a plane acoustic wave is investigated by means of an integral-equation technique.

534.4 4080

Acoustical Signal Detection in Turbulent Airflow—M. W. Smith and R. F. Lambert. (*J. Acoust. Soc. Am.*, vol. 32, pp. 858–866; July, 1960.) The improvement in signal-to-noise ratio obtainable using correlation and filtering techniques is determined for the case of a 1-kc sinusoidal signal masked by bands of additive electronic noise and by turbulent noise extending from 300 cps to 5 kc.

534.62 4081

Low-Reflection Sound Measurement Chambers—W. Bausch and R. Schubert. (*Frequenz*, vol. 13, pp. 324–331; October, 1959.) The design of anechoic chambers is discussed and curves are given of the calculated and the measured deviation of the sound level in anechoic chambers from the $1/r$ law, where r is the distance from the sound source. The construction and characteristics of various types of toothed sound-absorbing panels are also described.

534.75 4082

The Recovery Process of the Ear after Exposure to Noise—E. Schaefer. (*Frequenz*, vol. 13, pp. 316–323; October, 1959.) Apparatus investigating the auditory readaptation processes following exposure to medium-level noise is described. The results of subjective tests are discussed and related to the findings of other authors. 36 references.

534.78:621.376.22:538.632 4083

A Correlator employing Hall Multipliers applied to the Analysis of Vocoder Control Signals—A. R. Billings, and D. J. Lloyd. (*Proc. IEE*, vol. 107. pt B, pp. 435–438; September, 1960.) Auto- and cross-correlators for analyzing signals in the 0–100-cps band are described. Examples of measured functions for sine waves, noise, and the control signals of a vocoder are given.

534.8 4084

Ambient Noise in a Deep Inland Lake—M. R. Lomask and R. A. Saenger. (*J. Acoust. Soc. Am.*, vol. 32, pp. 878–883; July, 1960.) Background noise spectra from 11 to 250 cps have been obtained.

534.84+534.86 4085

Modern Acoustical Engineering—D. Kleis. (*Philips Tech. Rev.*, vol. 20, pp. 309–326; September 21, 1959. Also, vol. 21, pp. 52–72; December 16, 1959.) Part 1—General Principles (pp. 309–326). Part 2—Electroacoustical Installations in Large Theatres (pp. 52–72).

534.84.621.396.712.3 4086

Diffusion of Sound in Small Rooms—K. E. Randall and F. L. Ward. (*Proc. IEE*, vol. 107, pt. B, pp. 439–450; September, 1960.) Particular attention is given to acoustic problems in broadcast and television studios.

534.845 4087

Sound Levels in Rounded Corners and Edges—G. Zimmermann. (*Hochfrequenz. und Elektroak.*, vol. 68, pp. 122–125; November, 1959.) The effect on acoustic absorption of rounding the corners and edges of rooms is investigated. See also 1852 of June (Wöhle).

534.88+621.396.663 4088

The Accuracy of Measurement of the Direction of a Sound Source by Directive Receiver Systems—M. Federici. (*Ricerca Sci.*, vol. 29, pp. 2301–2313; November, 1959.) Four methods of finding the direction of a source radiating sound or EM waves are considered to assess their accuracy, which is shown to depend only on the signal-to-noise ratio and the directivity characteristics of the system.

534.88 4089

Angular Deviation in Directional Receiver Correlation—M. J. Jacobson and R. J. Talham. (*J. Acoust. Soc. Am.*, vol. 32, pp. 810–820; July, 1960.) A study is made of the effect on system output of deviations of the axes of pressure-gradient receivers (see 1478 of May) from the broadside position.

534.88:534.417 4090

Digital Array Phasing—V. C. Anderson. (*J. Acoust. Soc. Am.*, vol. 32, pp. 867–870; July, 1960.) A description is given of the DIMUS (digital multibeam steering) technique for processing the output of an array of elements in an underwater acoustic field.

534.88:534.417 4091

Small-Signal Detection in the DIMUS Array—P. Rudwick. (*J. Acoust. Soc. Am.*, vol. 32, pp. 871–877; July, 1960.) An analysis is made of the effectiveness of an array beam for detecting a small plane-wave signal in isotropic Gaussian noise, together with a comparison of

DIMUS (see 4090 above) with conventional steering systems.

621.395.616 4092
Vibration Sensitivity of Condenser Microphones—E. Rule, F. J. Suellentrop, and T. A. Perls. (*J. Acoust. Soc. Am.*, vol. 32, pp. 821–823; July, 1960.) Expressions and graphs are given for calculating the lower limit of resolvable sound pressure in a vibration environment. The merits of various methods for overcoming vibration effects are discovered.

621.395.623.7 4093
The Influence of the Air-Gap Dimensions of Annular-Gap Magnet Systems on the Electroacoustic Efficiency of Loudspeakers—E. Unger. (*Hochfrequenz. und Elektroak.*, vol. 68, pp. 125–127; November, 1959.)

621.395.625.3 4094
Reproduction of Magnetic Tape Recordings by Means of the Hall Effect—F. Kuhrt, G. Stark and F. Wolf. (*Elektron. Rundschau*, vol. 13, pp. 407–408; November, 1959). The design of a reproducing head which consists of two parallel ferrite plates with the gap between them filled by a thin layer of InSb is described. The advantages of the Hall-generator head over the conventional magnetic head are summarized.

681.84.087.7 4095
The Limits of "Trick Stereophony" using Pilot Frequencies below Threshold Level—F. Enkel. (*Elektron. Rundschau*, vol. 13, pp. 362–364; October, 1959.) The fundamental limitations inherent in a single-channel stereophonic system, such as that described in January 10, are discussed.

ANTENNAS AND TRANSMISSION LINES

621.315.212:621.372.54 4096
Periodically Inhomogeneous Coaxial Cables as Filter Systems in the Decimeter Wave Range—H. Loele. (*Nachrtech.*, vol. 9, pp. 465–470; October, 1959.) The two coaxial systems considered are a) a continuous cable filled with different types of dielectric, and b) a cable in which the diameter of the inner conductor changes abruptly along its length. The filter characteristics of these systems, treated as quadrupoles, are calculated.

621.372.2 4097
The Voltage Distribution along a Two-Wire Line Open at One End with Time-Dependent Terminal Impedance for the Case $R = G = 0$—D. Suschowk. (*Frequenz*, vol. 13, pp. 366–369; November, 1959.)

621.372.2:621.372.4 4098
Transformation of Impedances having a Negative Real Part and the Stability of Negative-Resistance Devices—B. Rosen. (PROC. IRE, vol. 48, p. 1660; September, 1960.) The standard Smith chart can be used if the radius vector is regarded as the reciprocal of the reflection coefficient.

621.372.21:681.142 4099
Simulation of a Line with Various Boundary Conditions with the Aid of an Analogue Computer—J. Matyáš. (*Arch. elekt. Übertragung*, vol. 13, pp. 482–486; November, 1959.) The simulation of a homogeneous loss-free transmission line is described, and the treatment of various boundary conditions is illustrated by an example of a delay line.

621.372.821:621.372.832.8 4100
J-Band Strip-Line Y Circulator—S. Yoshida. (PROC. IRE, vol. 48, p. 1664; September, 1960.) Typical figures obtained for transmission loss were as follows: forward, 0.35 db; backward, 34.8 db; and voltage SWR, 0.3 db at 360 Mc.

621.372.829+621.372.85 4101
Investigations of the Disk-Loaded and Helical Waveguide—B. T. Henoch. (*Kungl. tek. Högsk. Handl., Stockholm*, no. 129, 84 pp.; 1958. In English.) Report of theoretical and experimental investigations of both types of waveguide.

621.372.852.22 4102
Wave Propagation in an Inhomogeneous Transversely Magnetized Rectangular Waveguide—C. T. Tai. (*Appl. Sci. Res.*, vol. B8, no. 2, pp. 141–148; 1960.) A study is made of propagation in a medium which is considered either continuously or discontinuously inhomogeneous in the broadside direction, using a modified Sturm-Liouville differential equation.

621.396.67.095 4103
Current Waves in a Thin Cylindrical Conductor: Part 1—Currents and Impedance of a Transmitting Aerial—L. A. Vainshtein. (*Zh. Tekh. Fiz.*, vol. 29, pp. 673–688; June, 1959.) The current in a cylindrical conductor is represented as the sum of three traveling waves, one starting at the point of excitation, and the others at the two ends of the conductor. The complex amplitudes are expressed as slowly varying functions, whose derivatives are a solution of a Volterra integral equation of the first kind. The accuracy of the method increases with antenna length.

621.396.67.095 4104
Current Waves in a Thin Cylindrical Conductor: Part 2—The Current in a Passive Oscillator and the Radiation of a Transmitting Aerial—L. A. Vainshtein. (*Zh. Tekh. Fiz.*, vol. 29, pp. 689–699; June, 1959.) The current excited by a plane wave incident on a thin cylindrical conductor is expressed in terms of the functions introduced in Part 1 (4103 above). The radiation field of the conductor is calculated using the reciprocity theorem.

621.396.674.095 4105
Half-Wave Cylindrical Antenna in a Dissipative Medium: Current and Impedance—R. King and C. W. Harrison. (*J. Res. NBS*, vol. 64D, pp. 365–380; July/August, 1960.) An integral equation for the current distribution along a cylindrical antenna in a conducting dielectric is derived. The equation is solved for the current and the driving-point impedance, and numerical values of impedance are given for media such as an isotropic ionosphere, dry salt, earth, and lake water.

621.396.674.31 4106
Theory of Coupled Folded Antennas—C. W. Harrison, Jr., and R. King. (IRE TRANS. ON ANTENNAS AND PROPAGATION, vol. AP-8, pp. 131–135; March, 1960. Abstract, PROC. IRE, vol. 48, p. 1353; July, 1960.)

621.396.676 4107
The Flight Evaluation of Aircraft Antennas—G. W. Leopard. (IRE TRANS. ON ANTENNAS AND PROPAGATION, vol. AP-8, pp. 158–166; March, 1960. Abstract, PROC. IRE, vol. 48, p. 1353; July, 1960.)

621.396.677:551.510.535 4108
Theoretical Study of Some Aerials of Rhombic or Rectangular Form for Vertical Ionospheric Sounding—P. Halley. (*Ann. Télécommun.*, vol. 14, pp. 289–296; November/December, 1959.)

621.396.677.3 4109
Linear Arrays with Arbitrarily Distributed Elements—H. Unz. (IRE TRANS. ON ANTENNAS AND PROPAGATION, vol. AP-8, pp. 222–223; March, 1960. Abstract, PROC. IRE, vol. 48, p. 1354; July, 1960.)

621.396.677.3.029.62 4110
The Power Gain of Multitiered V.H.F. Transmitting Aerials—P. Knight and G. D. Monteath. (*BBC Eng. Div. Monographs*, no. 31, 38 pp.; July, 1960.) A method of calculating the power gain is described, and results computed, for a comprehensive range of variables presented in tabular form.

621.396.677.71 4111
The Effects of Errors on the Polar Diagram of a Slot Array—D. S. Palmer. (*Marconi Rev.*, vol. 23, pp. 110–114; 3rd Quarter, 1960.) Algebraic expressions are given for the correlation between the errors in the field from a slotted waveguide as measured in two directions, in terms of the random errors in field strength and phase which are assumed to be introduced at each slot.

621.396.677.71 4112
The Slot Antenna with Coupled Dipoles—R. W. P. King and G. H. Owyang. (IRE TRANS. ON ANTENNAS AND PROPAGATION, vol. AP-8, pp. 136–143; March, 1960. Abstract, PROC. IRE, vol. 48, p. 1353; July, 1960.)

621.396.677.83 4113
The Calculation of the Effective Area of Surface Radiators with Non-cophasal Loading—G. F. Koch. (*Arch. elekt. Übertragung*, vol. 13, pp. 462–466; November, 1959. Correction, vol. 13, p. 532; December, 1959.) The effect of a deviation from in-phase loading is considered for active and passive radiators.

621.396.677.832 4114
Radiation Patterns of Finite-Size Corner-Reflector Antennas—A. C. Wilson and H. V. Cottony. (IRE TRANS. ON ANTENNAS AND PROPAGATION, vol. AP-8, pp. 144–157; March, 1960. Abstract, PROC. IRE, vol. 48, p. 1353; July, 1960.)

621.396.677.832 4115
A Slot-Excited Corner Reflector for Use in Band V (610–960 Mc/s)—D. J. Whythe and K. W. T. Hughes. (IRE TRANS. ON ANTENNAS AND PROPAGATION, vol. 107, pt. B, pp. 431–454; September, 1960.) A description is given of a corner reflector excited by a four-tier slotted cylinder. The antenna can be used at any frequency within range of 1.16:1 by simple modifications to the slot loading and feeder system.

621.396.677.85 4116
Metal-Disc Delay Dielectrics—C. Dhanalakshmi and S. K. Chatterjee. (*J. Inst. Telecommun. Engrs., India*, vol. 6, pp. 83–85; February, 1960.) Theoretical and experimental estimates of the phase change for microwave transmission through an artificial dielectric are given.

AUTOMATIC COMPUTERS

681.142 4117
Analogue Multiplication using Time as One Variable—T. R. Hoffman. (*Electronics*, vol. 33, pp. 136–138; August 12, 1960.) If one analog quantity appears as a time interval, accurate electronic multiplication is simplified. Transistor circuits giving products proportional to average or peak output voltage are described.

681.142 4118
The Minimization of the Effect of Drift in D.C. Analogue Computers—E. T. Emms and K. H. Brinkmann. (*Electronic Engrg.*, vol. 32, pp. 550–553; September, 1960.)

681.142 4119
The Elliott Sheffer Stroke Static Switching System—P. Kellett. (*Elec. Engrg.* vol. 32, pp.

534–539; September, 1960.) A system is described in which interconnections between a number of logic elements, all of the same type (the Sheffer stroke), permit any logical configuration or switching sequence.

681.142:535.215 4120
All-Purpose Computer Circuits Automatically Connected to Solve Specific Problems—R. J. Domenico and R. A. Henle. (*Electronics*, vol. 33, pp. 56–58; August 19, 1960.) Different connections may be made automatically using a photoconductor matrix, which may also be used to detect and replace faulty parts.

681.142:621.317.729 4121
The Resistance Network, a Simple and Accurate Aid to the Solution of Potential Problems—J. C. Francken. (*Philips Tech. Rev.*, vol. 21, pp. 10–23; December 11, 1959.) A method applicable to two-dimensional problems, and to three-dimensional problems where there is rotational symmetry, is described. In either case, Laplace's equation for given boundary conditions reduces to a differential equation involving two independent variables only.

CIRCUITS AND CIRCUIT ELEMENTS

621.3.049.7:621.382 4122
Theory of a Monolithic Null Device and some Novel Circuits—W. M. Kaufman. (Proc. IRE, vol. 48, pp. 1540–1545; September, 1960.) A semiconductor structure which behaves as a twin-T filter network is described and applied to a tuned amplifier, oscillator and transducer.

621.316.8 4123
The Miniaturization of Resistors—H. Henniger. (*Nachrtech.*, vol. 9, pp. 514–517; November, 1959.) A review is given of available types of carbon- and metal-film resistors, resistance materials and resistor cooling systems, with tabulated results of climatic tests on film-type resistors.

621.316.825:546.26-1 4124
Semiconducting Diamonds as Thermistors—G. B. Rodgers and F. A. Raal. (*Rev. Sci. Instr.*, vol. 31, pp. 663–664; June, 1960.) The performance and construction of diamond thermistors which have high thermal conductivity and resistance to corrosion is described.

621.316.86 4125
Conducting Hard Rubber and its Use as Composition Resistor—S. Mishra. (*J. Inst. Telecommun. Engrs., India*, vol. 6, pp. 77–82; February, 1960.) With certain types of carbon black, it is possible to obtain electrically stable compounds with specific resistances of up to 10 MΩ/cm.

621.318.57:537.312.62 4126
Thin-Film Cryotrons: Parts 1–3—C. R. Smallman, A. E. Slade and M. L. Cohen. (Proc. IRE, vol. 48, pp. 1562–1582; September, 1960.) A discussion is given of the characteristics of evaporated superconductive films, as applied to cryotrons, together with details of a thin-film cryotron, made by vacuum deposition, which is much smaller than the wire-wound component. The performance of this cryotron is given, and it is applied to flip-flop circuits. Finally, its use in ring oscillators is analyzed by two different methods.

621.319:537.228.1:621.314 4127
Piezoelectric Voltage Transformers—A. E. Crawford. (*Wireless World*, vol. 66, pp. 510–514; October, 1960.) Possible modes of operation are considered, and the design and performance of a ceramic transformer with respect to one of these modes is examined. The advantages and possible applications of such devices are discussed.

621.372:621.391.822:530.162 4128
Irreversible Thermodynamics of a Nonlinear *RC* System—W. Bernard and H. B. Callen. (*Phys. Rev.*, vol. 118, pp. 1466–1470; June 15, 1960.) The solution is compared with those of other investigators [see, *e.g.*, 2651 of 1958 (van Kampen)].

621.372.012(083.7) 4129
IRE Standards on Circuits: Definitions of Terms for Linear Signal Flow Graphs, 1960—(Proc. IRE, vol. 48, pp. 1611–1612; September, 1960.) Standard 60 IRE 4.S1.

621.372.4/.6(083.7) 4130
IRE Standards on Circuits: Definitions of Terms for Linear Passive Reciprocal Time Invariant Networks, 1960—(Proc. IRE, vol. 48, pp. 1608–1610; September, 1960.) Standard 60 IRE 4.S2.

621.372.4 4131
Partial Equivalence with Reference to a Theorem of Cocci-Cauer—K. H. R. Weber. (*Hochfrequenz. und Elektroak.*, vol. 68, pp. 118–121; November, 1959.) The equivalence of two-terminal networks containing *R*, *C* and *L* elements is discussed. See 697 of 1957.

621.372.4 4132
On Network Synthesis with Negative Resistance—F. T. Boesch and M. R. Wohlers. (Proc. IRE, vol. 48, pp. 1656–1657; September, 1960.) A procedure is outlined which results in realizable networks with lossy elements arranged in Foster terms.

621.372.5:621.372.44 4133
Solution of Ladder Networks containing Nonlinear Resistances—T. Kovattana and J. R. Barker. (*Brit. J. Appl. Phys.*, vol. 11, pp. 437–439; September, 1960.) A graphical method of solving network problems involving nonlinear and/or negative resistances is described. Such networks have been used for the solution of nonlinear differential equations. See also, 1227 of 1952 (Cherry).

621.372.54 4134
Design of Networks with Prescribed Delay and Amplitude Characteristics—J. K. Skwirzynski and J. Zdunek. (*Marconi Rev.*, vol. 23, pp. 115–139; 3rd Quarter, 1960.) A general analytic method is described for designing reactive quadripoles with specified group delay characteristics; means of equalizing attenuation without affecting the delay are discussed.

621.372.54:534.143 4135
Image-Parameter Theory for Mechanical Quadripoles in Compressional or Torsional Oscillation—C. Kurth. (*Nachrtech.*, vol. 9, pp. 490–502; November, 1959.) The equivalence of the parameters of a mechanical system transmitting compressional or torsional oscillations and the parameters of an electrical transmission line is established. The design of mechanical filters is described, and design formulas with response characteristics are given for the basic filter sections.

621.372.543.2:621.372.412 4136
Special Band-Pass Half Sections—K. Stegemann. (*Nachrtech.*, vol. 9, pp. 502–505; November, 1959.) The design of crystal filters of branch-network type is described. See also, 1904 of June (Poschenrieder).

621.372.56 4137
A "Decimal" Attenuator—E. R. Wigan. (*Electronic Engrg.*, vol. 32, pp. 560–566; September, 1960.) A network combining the properties of a conventional voltage or current divider with those of a constant-resistance attenuator is given.

621.372.6 4138
A Multiple Isolated-Input Network with Common Output—C. M. Allred and C. C. Cook. (*J. Res. NBS*, vol. 64C, pp. 225–228; July–September, 1960.) Design equations are developed for the general case of *n* isolated inputs with a common output. Measurements made on two-input and three-input units are given.

621.373.42 4139
Frequency of the Three-Phase *RC*-Coupled Oscillator: Part 2—Inductive Anode Load Resistance—H. Rakshit and M. C. Mallik. (*Indian J. Phys.*, vol. 34, pp. 36–54; January, 1960.) Part 1: 1998 of 1956.

621.373.42 4140
The Optimum Design of *RC* Valve Oscillators—T. Zagajewski. (*Hochfrequenz. und Elektroak.*, vol. 68, pp. 127–136; November, 1959.) Nonlinear distortion is analyzed, and optimum operating conditions are determined by means of an analytical method using nonlinear coefficients.

621.373.443 4141
Shock Excitation of a Radio-Frequency Power Circuit by means of a Saturable-Core Reactor—W. F. Westendorp and H. Hurwitz, Jr. (*Rev. Sci. Instr.*, vol. 31, pp. 662–663; June, 1960.) A circuit which produces high-power RF pulses under conditions allowing repeated excitation without degrading the circuit *Q* is described.

621.373.52:621.383.53 4142
Circuit Applications of Field-Effect Transistors—R. R. Bockemuehl. (*Electronics*, vol. 33, pp. 132–135; August 12, 1960.) Applications of photosensitive CdS transistors in sawtooth generators, amplifiers and phaseshift oscillators are described.

621.374.4+621.376.2:537.56 4143
Microwave Detection and Harmonic Generation by Langmuir-Type Probes in Plasmas—J. M. Anderson. (Proc. IRE, vol. 48, pp. 1662–1663; September, 1960.) Rectification effects are obtained with cold-cathode dc discharges in He or Ne.

621.374.4:621.372 4144
A Traveling-Wave Harmonic Generator—D. L. Hedderly. (Proc. IRE, vol. 48, p. 1658; September, 1960.) A scheme is outlined in which a series of delay-line outputs, displaced in phase relative to one another, are combined to deliver pulsed power at a predetermined harmonic of the input frequency.

621.375.3/.4:621.318.57 4145
Systems using Transistors and Transductors—D. A. Ramsay. (*Elec. Engrg.*, vol. 32, pp. 476–479, 540–544, and 640–643; August–October, 1960.) Amplifier, modulator and switching systems are described in which transistors and transductors are combined.

621.375.4 4146
High-Input-Impedance Transistor Circuits—I. Levine. (*Electronics*, vol. 33, pp. 50–52; September 2, 1960.) An impedance greater than 50 MΩ over a wide temperature range has been obtained with emitter-follower circuits having low noise.

621.375.4 4147
Linear-Phase Transistor Amplifier—P. Hirsch. (*Elec. Engrg.*, vol. 78, pp. 1184–1189; December, 1959.) The design of a simple shunt-compensated linear-phase amplifier is described.

621.375.4.024 4148
A Low-Drift Transistor Chopper-Type D.C. Amplifier with High Gain and Large Dynamic Range—I. C. Hutcheon and D. Summers. (*Proc. IEE*, vol. 107, pp. 451–461; Discussion, pp. 461–465; September, 1960.) The voltage and current drifts are less than ± 10 μv and and $\pm 4\times 10^{-3}$ amperes, respectively. The gain is such that inputs of 0–10 mv or 0–4 μa can be presented as an output of 0–5 volts to an accuracy within ± 0.1 per cent.

621.375.426 4149
Narrow-Band Amplification with Transistors—H. Beneking. (*Nachrichtentech. Z.*, vol. 12, pp. 543–546; November, 1959.) The design formulas for tuned-circuit coupling of amplifier stages with resistance and with reactance matching are considered, and design curves are given for optimum circuit conditions.

621.375.432 4150
A Nonlinear Effect in Transistor Amplifiers with Feedback—I. Gumowski. (*C.R. Acad. Sci., Paris*, vol. 249, pp. 2514–2516; December 9, 1959.) The normal equivalent circuit for a transistor amplifier is no longer applicable when more than 20 db of feedback is applied. The nonlinear effect introduced under these conditions is illustrated by a practical example.

621.375.9:538.569.4 4151
Inversion by Fast Passage in a Multilevel Spin System—P. E. Wagner, J. G. Castle, Jr., and P. F. Chester. (*J. Appl. Phys.*, vol. 31, p. 1498; August, 1960.) Some measurements of adiabatic fast passage in a multilevel electron-spin system are described with particular reference to a recent proposal for a "staircase" maser [2522 of 1959 (Siegman and Morris)].

621.375.9:538.569.4.029.63 4152
Some Characteristics of a Maser at 1420 Mc/s—B. Bölger, B. J. Robinson and J. Ubbink. (*Physica*, vol. 26, pp. 1–18; January, 1960.) A regenerative solid-state maser has been constructed for 1420 Mc using 0.05 per cent Cr^{+3} in $K_3Co(CN)_6$ and a pump frequency of 3850 Mc.

621.375.9:621.372.44 4153
Optimum Noise and Gain-Bandwidth Performance for a Practical One-Port Parametric Amplifier—J. C. Greene and E. W. Sard. (PROC. IRE, vol. 48, pp. 1583–1590; September, 1960.) Analysis shows that the conditions necessary for minimum noise temperature are compatible with those necessary for maximum gain-bandwidth product if the diode has a high self-resonance frequency. There is a characteristic figure of merit for the diode and an optimum pump frequency. A series of design curves is given.

621.375.9:621.372.44 4154
Symmetrical Matrix Analysis of Parametric Amplifiers and Converters—S. Deutsch. (PROC. IRE, vol. 48, pp. 1595–1602; September, 1960.) Expressions are derived for gain, bandwidth, and noise figure, and, by regarding the matrix as a nodal admittance array, an equivalent conductance circuit is constructed. It is shown that, for low-noise figure and wide bandwidth, the idler frequency should be much higher than the signal frequency.

621.375.9:621.372.44 4155
A Transmission Matrix Analysis of the Cavity Parametric Amplifier—R. E. Aitchison. (*Proc. IRE, Australia*, vol. 21, pp. 479–480; July, 1960.)

621.375.9:621.372.44:537.227 4156
Interaction of Two Microwave Signals in a Ferroelectric Material—I. Goldstein. (PROC. IRE, vol. 48, p. 1665; September, 1960.) An exchange of energy was observed from the pump to the signal frequency in polycrystalline $BaTiO_3$ via an idler frequency.

621.375.9:621.372.44:621.382.2 4157
On Stabilizing the Gain of Varactor Amplifiers—B. J. Robinson, C. L. Seeger, K. J. van Damme and J. T. de Jager. (PROC. IRE, vol. 48, p. 1648; September, 1960.) Use of the varactor dc to control pump level improved the gain stability.

621.375.9:621.372.44:621.382.23 4158
An X-Band Parametric Amplifier using a Silver-Bonded Diode—S. Kita and F. Obata. (PROC. IRE, vol. 48, pp. 1651–1652; September, 1960.) A wafer-type construction is used for the silver-bonded diode. The design and performance data of an amplifier operating at 11440 Mc are given.

621.375.9:621.372.44:[621.385.6+621.387 4159
Parametric Amplifier Theory for Plasmas and Electron Beams—G. S. Kino. (*J. Appl. Phys.*, vol. 31, pp. 1449–1458; August, 1960.) A theory for a parametric amplifier which uses a gas-discharge plasma is given. An experimental amplifier is described. Using a signal frequency of 300 Mc, the gain was only 2 db. It is hoped to improve on this by reducing the velocity dispersion.

621.376.22:621.318.134 4160
The Theory of Magnetic Ring Modulators—R. Elsner. (*Arch. elekt. Übertragung*, vol. 13, pp. 486–494; November, 1959.) The equivalent circuit of the magnetic ring modulator is derived for idealized B/H characteristics, and the design of a modulator circuit is given [see also 2039 of 1958 (Elsner and Pungs)].

621.376.5:621.382.333 4161
A New Use of the Junction Transistor as a Pulse-Width Modulator—I. Tagoshima. (PROC. IRE, vol. 48, p. 1663; September, 1960.) The base pulse current is modulated in a common-emitter configuration.

GENERAL PHYSICS

530.162 4162
Fluctuations from the Nonequilibrium Steady State—M. Lax. (*Rev. Mod. Phys.*, vol. 32, pp. 25–64; January, 1960.) A macroscopic treatment of noise using Markovian and stationary assumptions is presented.

537.214 4163
The Electrostatic Energy of a Space Charge—O. Emersleben. (*Hochfrequenz. und Elektroak.*, vol. 68, pp. 111–118; November, 1959.) See also 1540 of May.

537.226.31 4164
Microwave Measurements of Dielectric Absorption in Dilute Solutions—H. Kramer. (*Z. Phys.*, vol. 157, pp. 134–138; October 15, 1959.) Absorption measurements at 7 mm λ on dipole molecules in dilute solution with a nonpolar solvent were made, using the arrangement described by Lane and Saxton (3399 of 1952) which was modified to increase the sensitivity.

537.291:538.56 4165
Acceleration of Charged Particles in Travelling or Standing Electromagnetic Waves—G. A. Askar'yan. (*Zh. Eksp. Teor. Fiz.*, vol. 36, pp. 619–621; February, 1959.) The average Lorentz force acting on a charged particle in an electromotive field depends on the resonance properties of the motion of the particles and on the spread in their transverse momentum. Conditions under which continuous acceleration can be achieved by spatial variation of the particle oscillation parameters are discussed.

537.311.33 4166
Determination of the Effective Scattering Mechanism Parameter of Electron Transport Theory—T. C. Harman. (*Phys. Rev.*, vol. 118, pp. 1541–1542; June 15, 1960.) Fermi-level energy, effective scattering mechanism parameter, and effective mass and relaxation time can be obtained from the magneto-Seebeck effect for Corbino-disk geometry when combined with other transport measurements.

537.312.62 4167
An Analogue Solution for the Static London Equations of Superconductivity—N. H. Meyers. (PROC. IRE, vol. 48, pp. 1603–1607; September, 1960.) Measurements of field distributions in the space around the normal conductors of a growing-exponential-function generator provide useful cryogenic-circuit design data.

537.312.62 4168
Gauge Invariant Formulation of the Bardeen-Cooper-Schrieffer Theory of Superconductivity—T. A. Oliphant and W. Tobocman. (*Phys. Rev.*, vol. 119, pp. 502–503; July 15, 1960.)

537.312.7/.8 4169
An Analogy between the Effects of Fluctuating Electric Fields and Steady Magnetic Fields in Isotropic Conductors when a Universal Relaxation Time cannot be Defined—E. J. Moore. (*Aust. J. Phys.*, vol. 13, pp. 95–97; March, 1960.)

537.533 4170
Propagation of Perturbations in a One-Dimensional Two-Beam Electron Flow—Chzhan Dzhi-min (Chang Chih-ming). (*Zh. Tekh. Fiz.*, vol. 29, pp. 745–755; June, 1959.) Using a difference-kernel integral-equation method, a solution is obtained for drift in two-beam flow in the presence of a transverse electric field.

537.533 4171
Three-Dimensional Space-Charge Flow—J. Rosenblatt. (*J. Appl. Phys.*, vol. 31, pp. 1371–1377; August, 1960.) Theory and experimental results for stationary beams, allowing for electrostatic interaction between the particles, are given.

537.533 4172
Equilibrium Conditions for Electron Beams—V. S. Anastasevich. (*Zh. Tekh. Fiz.*, vol. 29, pp. 738–744; June, 1959.) The conditions are determined for a beam in which the density of secondary particles is much greater than that of primary electrons.

537.533 4173
Nonlinear Behaviour of a Modulated Electron Beam in the Presence of a Velocity Distribution—S. V. Yadavalli. (*J. Electronics and Control*, vol. 8, pp. 365–375; May, 1960.) The harmonic currents in an electron beam with a velocity distribution can be evaluated by a procedure based on the Boltzmann equation.

537.533:538.3 4174
The Electrokinetic Power Theorem—H. W. König. (*Arch. elekt. Übertragung*, vol. 13, pp. 475–476; November, 1959.) The electrokinetic power theorem is shown to be valid also for arbitrary electron velocities (relativistic conditions) if certain definitions are adopted.

537.533:538.566 4175
On the Properties of the Electron Beam in the Presence of an Axial Magnetic Field of Arbitrary Strength—H. Wilhelmsson. (*Chalmers Tek. Högsk. Handl.*, no. 205, 32 pp.; 1958. In English.) A study is made of the effect of an axial magnetic field on the propagation of waves in an idealized electron beam, using small-signal theory and neglecting collisional effects. The possibility of angular asymmetric excitation is considered, and special attention is paid to the influence of the ac-drift Lorentz

terms, and of the relativistic corrections in the derived equations.

537.533:621.385.632.3 4176
The Electromagnetic Interaction between Two Crossing Electron Streams: Parts 1 & 2—G. H. Joshi. (*Chalmers tek. Högsk. Handl.*, no. 183, 31 pp.; 1957. Also no. 197, 10 pp.; 1958. In English.) The interaction between two infinitely extended velocity-modulated streams has been studied. In Part 1, where beam velocities common to microwave tubes are considered, the Lorentz term in the equation of motion has been omitted; it is introduced in Part 2 for higher beam velocities.

537.56 4177
The Distribution of Ions formed by Attachment of Electrons Moving in a Steady State of Motion through a Gas—C. A. Hurst and L. G. H. Huxley. (*Aust. J. Phys.*, vol. 13, pp. 21–26; March, 1960.) The distribution of ions formed by attachment of electrons diffusing through a gas is solved exactly, and the results are compared with an approximate calculation given earlier by Huxley (812 of March).

537.56 4178
Ionic Conductivity of Highly Ionized Plasmas—M. Sakuntala, A. von Engel and R. G. Fowler. (*Phys. Rev.*, vol. 118, pp. 1459–1465; June 15, 1960.) Values of plasma resistivity as measured by a current entering and leaving the plasma, and the flow velocity in hydrogen at various gas pressures are given, together with a discussion of the theoretical aspects of the problem.

537.56:538.56 4179
Propagation and Production of Electromagnetic Waves in a Plasma—R. Gallet. (*Nuovo Cim.*, vol. 13, suppl. no. 1, pp. 234–256; 1959.) A general review of nonthermal mechanisms for the emission of electromotive waves in a plasma.

537.56:538.56 4180
Linearized Theory of Plasma Oscillations—L. Oster. (*Rev. Mod. Phys.*, vol. 32, pp. 141–168; January, 1960.)

537.56:538.566.029.6 4181
Microwave Conductivity of a Plasma in a Magnetic Field—D. C. Kelly. (*Phys. Rev.*, vol. 119, pp. 27–39; July 1, 1960.) The Boltzmann equation for electrons in a uniform isothermal plasma is solved. The microwave conductivity is simply related to certain coefficients of the solution.

537.56:538.69 4182
The Transport Phenomena in Cylindrical Discharges in the Presence of Magnetic Fields—J. Friedrich, H. Schirmer and I. Stober. (*Z. Naturforsch.*, vol. 14a, pp. 1047–1056; December, 1959.)

537.56:621.576.2+621.374.4 4183
Microwave Detection and Harmonic Generation by Langmuir-Type Probes in Plasmas—Anderson. (See 4143.)

538.2:52 4184
Waves in a Conducting Sheet Situated in a Strong Magnetic Field—I. C. Percival. (*Proc. Phys Soc., London*, vol. 76, pp. 329–336; September 1, 1960.) "The hydromagnetic approximation is applied to the elementary linear theory of transverse waves in a thin uniform plane conducting sheet, in which the inertia is provided by the sheet, and the restoring forces by strong vacuum magnetic fields on either side of the sheet. The dispersion relation and damping are obtained. The waves should be observable in the laboratory."

538.222:538.569.4 4185
Nuclear Spin-Lattice Relaxation Caused by Paramagnetic Impurities—W. E. Blumberg. (*Phys. Rev.*, vol. 119, pp. 79–84; July 1, 1960.)

538.3 4186
On the Uniqueness Theorem for Electromagnetic Fields—H. Unz. (PROC. IRE, vol. 48, pp. 1663–1664; September, 1960.) Resonant modes and mixed boundary conditions in the steady state are considered.

538.566 4187
Impulse Excitation of a Conducting Medium—J. Galejs. (IRE TRANS. ON ANTENNAS AND PROPAGATION, vol. AP-8, pp. 227–228; March, 1960. Abstract, PROC. IRE, vol. 48, p. 1354; July, 1960.)

538.566 4188
Electromagnetic Transients in Conducting Media—S. N. Zisk. (IRE TRANS. ON ANTENNAS AND PROPAGATION, vol. AP-8, pp. 229–230; March, 1960. Abstract, PROC. IRE, vol. 48, p. 1354; July, 1960.)

538.566 4189
A Reciprocity Theorem for the Electromagnetic Field Scattered by an Obstacle—A. T. De Hoop. (*Appl. Sci. Res.*, vol. B8, no. 2, pp. 135–140; 1960.) See also 3797 of November.

538.566:535.42 4190
Propagation at Oblique Incidence over Cylindrical Obstacles—M. P. Bachynski. (*J. Res. NBS*, vol. 64D, pp. 311–315; July–August, 1960.) Results of model experiments at 1.25 cm λ with cylindrical and conical obstacles are given. The effect of oblique incidence can be considered as a change in the effective radius of curvature of the diffracting obstacle.

538.566:535.42 4191
Diffraction by Smooth Conical Obstacles—H. E. J. Neugebauer and M. P. Bachynski. (*J. Res. NBS*, vol. 64D, pp. 317–329; July–August, 1960.) Expressions obtained earlier (*e.g.*, 3957 of 1958) are generalized to oblique incidence and conical surfaces. The derivation is based on a generalized concept of the Green's function and on the use of corrective factors. Results are compared with scale-model measurements.

538.566:535.42 4192
A New Method of Solving the Problem of the Diffraction of Electromagnetic Waves by a Thin Conducting Disk—N. N. Lebedev and I. P. Skal'skaya. (*Zh. Tekh. Fiz.*, vol. 29, pp. 700–710; June, 1959.) The problem is reduced to the determination of two functions, each of which satisfies a Fredholm integral equation which can be solved by numerical methods. A simple formula for the scattering coefficient is derived.

538.566:535.42 4193
The Planar Problem of the Diffraction of Electromagnetic Waves by Two Ideally Conducting Strips of Finite Width Located One below the Other—Yu. V. Pimenov. (*Zh. Tekh. Fiz.*, vol. 29, pp. 711–715; June, 1959.) A mathematical analysis is made based on the method of successive approximations using special approximation formulas.

538.566:535.43 4194
Reciprocity and Scattering by Certain Rough Surfaces—W. S. Ament. (IRE TRANS. ON ANTENNAS AND PROPAGATION, vol. AP-8, pp. 167–174; March, 1960. Abstract, PROC. IRE, vol. 48, p. 1353; July, 1960.)

538.566:535.43 4195
Backscattering from a Finite Cone—J. B. Keller. (IRE TRANS. ON ANTENNAS AND PROPAGATION, vol. AP-8, pp. 175–182; March, 1960. Abstract, PROC. IRE, vol. 48, p. 1353; July, 1960.)

538.566:537.533 4196
The Interaction between an Obliquely Incident Plane Electromagnetic Wave and an Electron Beam: Parts 2 & 3—H. Wilhelmsson. (*Chalmers tek. Högsk. Handl.*, nos. 198 and 206, 32 pp. and 17 pp.; 1958. In English.) The work described earlier (2926 of 1955) is extended in Part 2 to include the case where there is no static magnetic field present. In Part 3, results obtained are analyzed for possible resonance conditions to provide a more direct physical interpretation of the formulas derived. See also 4175 above.

538.566.1:539.23 4197
Depth of Penetration as a Measure of Reflectivity of Thin Conductive Films—F. T. Koide. (PROC. IRE, vol. 48, pp. 1654–1655; September, 1960.) For conductors with intrinsic impedance of unity or less, the minimum thickness which gives a reflection coefficient greater than 90 per cent is shown to be 3 per cent of the depth of penetration.

538.569.4:538.221 4198
Electromagnetic Theory of D.C. Effects in Ferromagnetic Resonance—H. J. Juretschke. (*J. Appl. Phys.*, vol. 31, pp. 1401–1406; August, 1960.) Propagation through thin sheets of ferromagnetic conductors is given.

538.569.4:538.222 4199
Paramagnetic Resonance along the Direction of the Polarizing Field—P. Jung, J. Van Cakenberghe and J. Uebersfeld. (*Physica*, vol. 26, pp. 52–60; January, 1960.) "A radio-frequency susceptibility along the polarizing field is observed when the electron spin resonance of DPPH is partly saturated at microwave frequency. The variations of the real and imaginary parts as a function of the radio frequency have been studied. Theoretical calculations are in good agreement with experiment. In some cases a negative susceptibility appears, which has been used in a molecular amplifier experiment."

GEOPHYSICAL AND EXTRATERRESTRIAL PHENOMENA

523.152:629.19 4200
Space Research—R. Fellows, J. E. Jackson, H. E. Newell, Jr., and M. Stoller. (*Engineer, London*, vol. 208, pp. 405–408 and 444–451, October 9 and 16, 1959. Discussion.) A slightly abridged test is given of a survey paper prepared by the NASA, Washington, D. C., on space research techniques and recent experimental data, with a summary of a discussion by experts from NATO countries at a meeting at Aachen, Germany, on September 24–25, 1959.

523.164 4201
A New Limit to the Galactic Magnetic Field set by Measurements of the Zeeman Splitting of the Hydrogen Line—R. D. Davies, C. H. Slater, W. L. H. Shuter and P. A. T Wild. (*Nature, London*, vol. 187, pp. 1088–1089; September 24, 1960.) Results give no positive evidence for a magnetic field in any of the clouds studied. Measurements made on the Taurus-A cloud show a field $<2\times10^{-5}$ oersteds and, in each of the three clouds in the direction of Cassiopeia-A, a field $<1\times10^{-5}$ oersteds. See also 4202 below.

523.164 4202
An Attempt to Detect the Galactic Magnetic Field using Zeeman Splitting of the Hydrogen Line—J. A. Galt, C. H. Slater and W.L.H.Shuter.(*Mon. Not. Roy. Astron. Soc.*, vol. 120, pp. 187–192; 1960.) Measurements made in the direction of Cassiopeia-A have shown no

significant Zeeman effect, indicating that the magnetic field component is $<5\times10^{-5}$ oersteds.

523.164 4203
The Possibility of Detecting a Gravitational Red Shift in 21-cm Radiation from the Galaxy—F. J. Kerr. (*Nature, London*, vol. 188, pp. 216–217; October 15, 1960.) There seems to be little possibility of recognizing a gravitational red shift as suggested by Landovitz and Marshall (*ibid.*, vol. 187, pp. 223–224; July 16, 1960) until the detailed structure and motions have been established more definitely.

523.164 4204
Brightness Distribution over some Strong Radio Sources at 1427 Mc/s—R. Q. Twiss, A. W. L. Carter and A. G. Little. (*Observatory*, vol. 80, pp. 153–159; August, 1960.) Results are given of measurements on Centaurus-A, Taurus-A, Cygnus-A and the Orion nebula made with groups of antennas of the "Christiansen cross" array [1126*j* of 1958 (Christiansen and Mathewson)].

523.164 4205
On the Spectra of Radio Sources—R. G. Conway, J. R. Shakeshaft and G. R. Whitfield. (*Observatory*, vol. 80, pp. 162–163; August, 1960.) Expressions are derived which suggest that there should be a progressive increase in the slope of the frequency spectrum of the flux density for more distant sources than Cygnus-A. See also 3790 of 1958 (Whitfield).

523.164.32:523.165 4206
Relation Between the Solar Emission of Cosmic Rays and Type IV Bursts—Y. Avignon and M. Pick-Gutmann. (*C. R. Acad. Sci., Paris*, vol. 249, pp. 2276–2278; November 30, 1959.) A close relation is found to exist between 10-cm bursts of type IV, associated with flares occurring on the west of the solar meridian, and cosmic radiation observed near the earth.

523.3:621.396.96 4207
Characteristics of 488-Mc/s Radio Signals Reflected from the Moon—B. C. Blevis and J. H. Chapman. (*J. Res. NBS*, vol. 64D, pp. 331–334; July/August, 1960.) Signals received on dish-mounted orthogonal dipoles give the effective radar cross section as 0.05 of the projected area: libration fading gives a cross-correlation of 0.89.

523.53:621.396.96 4208
Radio-Echo Observations of Southern-Hemisphere Meteor-Shower Activity from 1956 December to 1958 August—A. A. Weiss. (*Mon. Not. Roy. Astron. Soc.*, vol. 120, pp. 387–403; 1960.) A continuation of the radio survey of meteor activity at Adelaide (see 112 of 1958) is given. With the 67-Mc narrow-beam equipment used, weak showers can be detected only if they transit within 30 degrees of the zenith. The faintest detectable meteor trail has an electron line density of 1.3×10^{11} electrons per cm.

550.384:538.632 4209
Influence of Hall Effect on the Induced Current in the Earth owing to Magnetic Disturbances—J. S. Chatterjee. (*Sci. and Culture, Calcutta*, vol. 26, pp. 92–94; August, 1960.) Earlier theory (*e.g.*, 2719 of 1956) of the origin of geomagnetism is modified by allowing for Hall effect which accelerates the build-up of induced currents in the earth's crust.

550.385.37 4210
Some Characteristics of Geomagnetic Micropulsations (*Pc*)—J. A. Jacobs and K. Sinno. (*Nature, London*, vol. 188, pp. 285–287; October 22, 1960.) An analysis of data recorded by seventeen observatories during the IGY shows that micropulsations may be classified in two groups with periods 15–30 seconds or 30–90 seconds.

551.311.122 4211
Measured Electrical Properties of Snow and Glacial Ice—A. D. Watt and E. L. Maxwell. (*J. Res. NBS*, vol. 64D, pp. 357–363; July/August, 1960.) Graphs of conductivity and dielectric constant at frequencies between 30 cps and 200 kc are given. In general, the conductivity of snow and glacial ice is much higher than that of pure ice.

551.507.362:061.3 4212
Rocket and Satellite Instrumentation—B. G. Pressey. (*Nature, London*, vol. 188, pp. 265–266; October 22, 1960.) A report is given of a symposium organized jointly by the British Interplanetary Society and the Society of Instrument Technology, held in London, Eng., on September 1, 1960.

551.507.362.2 4213
The Radiation from Artificial Earth Satellites—P. Miram and E. Palm. (*Frequenz*, vol. 13, pp. 360–365; November, 1959.) The various factors affecting EM wave propagation from satellites are reviewed and discussed with reference to results obtained by radio observations and CR DF equipment.

551.507.362.2 4214
Satellite Perturbations from Extraterrestrial Gravitation and Radiation Pressure—F. T. Geyling. (*J. Franklin Inst.*, vol. 269, pp. 375–407; May, 1960.) The equations of motion of a satellite are written in terms of displacement components relative to the unperturbed elliptic orbit. A moving system of coordinates is used, which consists of an orthogonal triad whose origin is always located at the nominal satellite position on the elliptic orbit. In a numerical example, perturbations of a 100-foot balloon of 0.0005 inch thickness are considered.

515.507.362.2:551.510.535 4215
Fading of Satellite Transmissions and Ionospheric Irregularities—J. Mawdsley. (*J. Atmos. Terr. Phys.*, vol. 18, p. 344; August, 1960.) The orientation of the irregularities is suggested as an explanation of the observations of Kent (488 of February).

551.507.362.2:551.510.535 4216
Earth Satellite Observations and the Upper Atmosphere: Temperature Inversion in the F_1 Layer—W. Priester and H. A. Martin. (*Nature, London*, vol. 188, pp. 200–202; October 15, 1960.) The suggested "wiggle" in the curve for logarithmic density [Kallmann (3300 of 1959)] has been derived exactly from satellite observations; it shows that temperature inversion takes place at heights between 180–200 km.

551.507.362.2:551.510.535 4217
Earth-Satellite Observations and the Upper Atmosphere: Diurnal and Seasonal Density Variations in the Upper Atmosphere—W. Priester, H. A. Martin and K. Kramp. (*Nature, London*, vol. 188, pp. 202–204; October 15, 1960.) A continuation of earlier investigations is given [1595 of May (Martin and Priester)].

551.507.362.2:621.391.812.33 4218
The Use of Polarization Fading of Satellite Signals to Study the Electron Content and Irregularities in the Ionosphere—C. G. Little and R. S. Lawrence. (*J. Res. NBS*, vol. 64D, pp. 335–346; July/August, 1960.) A ray tracing program and a model ionosphere have been used to evaluate electron content. Refraction and, where necessary, path splitting are taken into account. Irregularities several hundred kilometers in size, and fractional variations of about 1 per cent in electron content have been detected.

551.507.362.2:621.391.812.63 4219
Second-Order Faraday Rotation Formulas—K. C. Yeh. (*J. Geophys. Res.*, vol. 65, pp. 2548–2550; August, 1960.) The formulas take ionospheric refraction into account in satellite measurements, and allow the integral $\int N^2 dh$ to be determined.

551.507.362.2:621.396.96 4220
Determination of Satellite Orbits from Radar Data—I. Harris and W. F. Cahill. (PROC. IRE, vol. 48, pp. 1657–1658; September, 1960.) Procedural stages in an optimum computer routine, using two orbital points and the transit time between them, incorporate a differential correction based on short range data. It is claimed that, within one minute, positional predictions are produced accurate to within 500 yards.

551.510.52 4221
Power Spectra of Temperature, Humidity and Refractive Index from Aircraft and Tethered Balloon Measurement—E. E. Gossard. (IRE TRANSACTIONS ON ANTENNAS AND PROPAGATION, vol. AP-8, pp. 186–201; March, 1960. Abstract, vol. 48, p. 1353; July, 1960.)

551.510.535 4222
On the Physical Properties and Composition of the Upper Atmosphere between 100 and 400 Kilometers above Ground in Middle Latitudes—T. Yonezawa. (*J. Radio Res. Labs., Japan*, vol. 7, pp. 69–84; March, 1960.) Computations for middle latitudes show substantial agreement with the results of other workers.

551.510.535 4223
A Relation between Ionospheric Drifts and Atmospheric Dynamo Current Systems—L. H. Heisler. (*Aust. J. Phys.*, vol. 13, pp. 188–191; June, 1960.) Geomagnetic data suggest that the focus of the atmospheric dynamo current system moves from north to south of Sydney, Australia, as solar activity increases. This would explain the reversal in the direction of ionospheric drifts at Sydney during recent years.

551.510.535 4224
Effects of Vertical Diffusion of Electrons near the Magnetic Equator—E. R. Schmerling. (*Nature, London*, vol. 188, pp. 133–134; October, 1960.) The effects are shown to account for the major features of the "geomagnetic anomaly" discussed by Croom, *et al.* (882 of March). The anomaly is an excess of ionization, due to diffusion, away from the equator, rather than a deficiency of ionization at the equator.

551.510.535 4225
Anisotropic Field-Aligned Ionization Irregularities in the Ionosphere near the Magnetic Equator—R. D. Egan. (*J. Geophys. Res.*, vol. 65, pp. 2343–2358; August, 1960.) Equatorial scatter-echoes were measured at Huancayo during the IGY. They were of two classes: a) those associated with the E region, having scattering heights between 100 and 200 km, which were present nearly all the time; b) those associated with the maximum of the F region. The E-region echoes were concentrated towards the direction of the subsolar point, and were estimated to be due to mean-square electron-density variation of about 10^{-5}. These irregularities were aligned along the earth's field, and were closely correlated with the equatorial electrojet and the presence of equatorial E_s.

551.510.535 4226
Experimental Relations between Ionospheric True Height, Group Height and Phase Height—J. A. Thomas and R. W. E. McNicol. (*Aust. J. Phys.*, vol. 13, pp. 132–138; June, 1960.) Changes in the phase height have been

determined using phase fringes, and compared with changes in height deduced from $N(h)$ profiles based on $h'(f)$ ionograms. The results are mutually consistent.

551.510.535 4227
The Determination of the True Height of Maximum Ionization by the Ten-Point Method—A. Haubert. (*J. Atmos. Terr. Phys.*, vol. 18, pp. 337–339; August, 1960. In French.) A graphical method for determining h_m directly from an ionogram is given.

551.510.535 4228
True Height and Thickness of the Ionospheric E Layer—K. Rawer. (*Ann. Géophys.*, vol. 15, pp. 547–550; October-December, 1959.) A method proposed by Schmerling (1733 of 1958) has been applied to calculations of the true height and thickness of the E layer. Results given for a single daytime period show irregularities in the fine structure of the layer.

551.510.535 4229
Nonseasonal Variation in the E-layer Ionization—T. Shimazaki. (*J. Radio Res. Labs., Japan*, vol. 7, pp. 95–109; March, 1960.) Appreciably greater ionization is found in December than in June. A relation to the Van Allen radiation belts is tentatively suggested.

551.510.535 4230
The World-Wide Semi-annual Cycle in the E Layer of the Ionosphere—C. M. Minnis and G. H. Bazzard. (*J. Atmos. Terr. Phys.*, vol. 18, pp. 306–308; August, 1960.) The monthly mean values of the E-layer character figure for eight stations in the northern and southern hemispheres have been calculated. At high solar activity, they exhibit a semiannual change of ±10 per cent, as graphically shown, with peaks in January and July/August in both hemispheres. There is no such change at the minimum of the solar cycle.

551.510.535 4231
A Synoptic Study of the F_2 Region of the Ionosphere in the Asian Zone—R. G. Rastogi. (*J. Atmos. Terr. Phys.*, vol. 18, pp. 315–331; August, 1960.) The seasonal and directional development of the anomalous belt of the F_2 layer is traced. Many abnormal features of the F region, observed at middle latitudes, are explained on the basis of horizontal movements in the ionosphere.

551.510.535 4232
A Relationship between Spread-F and the Height of the F_2 Ionospheric Layer—G. G. Bowman. (*Aust. J. Phys.*, vol. 13, pp. 69–73; March, 1960.) An extension is made of earlier work (3101 of September) to investigate the variation throughout the night of range-spreading spread-F widths at Brisbane, Australia. Evidence is presented to support the hypothesis that the ripple amplitude of the spread-F ionospheric irregularities varies directly with the layer height.

551.510.535 4233
Theory of Spread-F based on Aspect-Sensitive Back-Scattered Echoes—J. Renau. (*J. Geophys. Res.*, vol. 65, pp. 2269–2277; August, 1960.) A large class of spread-F echoes in equatorial regions may be explained by assuming that backscatter echoes are aspect-sensitive with regard to irregularities aligned along the earth's magnetic field.

551.510.535 4234
The Effects of Diffusion and of Attachment-Like Recombination on the F_2 Region—J. E. C. Gliddon and P. C. Kendall. (*J. Geophys. Res.*, vol. 65, pp. 2279–2283; August, 1960.) Theoretical formulas for the electron density in the F region (see 2738 of August) have been used to derive the diurnal variation of N_mF_2 and h_mF_2, taking into account vertical diffusion, and assuming isothermal conditions with exponentially decreasing attachment-like recombination.

551.510.535 4235
Equatorial Spread—F and F-Layer Heights—A. J. Lyon, N. J. Skinner and R. W. Wright. (*Nature, London*, vol. 187, pp. 1086–1088; September 24, 1960.) An extension is made of earlier work (3815 of 1958) to include a study of the high correlation between the rise in height of the F layer just after local sunset and the subsequent occurrence of spread-F.

551.510.535:523.164 4236
Ionospheric Refraction in Radio Astronomy: Part 1—Theory—M. M. Komesaroff. (*Aust. J. Phys.*, vol. 13, pp. 153–167; June, 1960.) Expressions are derived for the apparent displacements of cosmic radio sources at transit resulting from ionospheric refraction. The theory includes the effects of horizontal electron density gradients which often outweigh those due to a spherically symmetrical ionosphere. The relation of ionospheric refraction to the "total thickness" and the total electron content in a vertical column are discussed. For a preliminary report of this work, see 2973 of 1959 (Komesaroff and Shain).

551.510.535:523.164 4237
Scintillation, Spread-F, and Transequatorial Scatter—J. R. Koster and R. W. Wright. (*J. Geophys. Res.*, vol. 65, pp. 2303–2306; August, 1960.) Both radio-star scintillation and spread-F show little dependence on magnetic activity during sunspot minimum; at sunspot maximum they are strongly negatively correlated, while transequatorial scatter is positively correlated with magnetic activity.

551.510.535:523.745 4238
Short-Term Differences in the Behaviour of Two Daily Indices of Solar Activity during the I.G.Y.—G. H. Bazzard. (*J. Atmos. Terr. Phys.*, vol. 18, pp. 290–296; August, 1960.) Changes in the relative magnitudes of the daily E-layer character figure and the flux of solar noise at 10.7 cm λ are associated with increases in geomagnetic activity and the presence of active regions on the sun's disk.

551.510.535:523.754 4239
A Monthly Ionospheric Index of Solar Activity Based on F_2-Layer Ionization at Eleven Stations—C. M. Minnis and G. H. Bazzard. (*J. Atmos. Terr. Phys.*, vol. 18, pp. 297–305; August, 1960.) The construction of an index is described, which statistical tests show to be preferable to sunspot number or solar noise flux at 10.7 cm λ for use in forecasting critical frequencies of the F_2 layer.

551.510.535:523.78 4240
Sunrise and Eclipse Effects on the Ionosphere at Brisbane—G. G. Bowman. (*Aust. J. Phys.*, vol. 13, pp. 52–68; March, 1960.) See also 4232 above.

551.510.535:550.385 4241
Dynamic Characteristics of the Ionosphere and their Coherency with the Local and Planetary Magnetic Index—K. Bibl. (*J. Geophys. Res.*, vol. 65, pp. 2333–2343; August, 1960.) Transient variations (<1 hour) in MUF, $h'F$ and fE_s have been partially correlated with magnetic indexes. Results show that the appearance of E_s is associated with an increase in F-layer height, and that the presence of E_s ionization decreases the fluctuations in the local magnetic field.

551.510.535:550.386 4242
Geomagnetic Field and Ionospheric Drift—S. N. Mitra and K. K. Vij (*J. Inst. Telecommun. Engrs., India*, vol. 6, pp. 90–96; February, 1960.) Drift measurements at New Delhi do not show the semidiurnal periodicity which would be expected if the drifts were in the form of lunar or solar tides. Some correlation with the magnetic index K is looked for, but is not found except on "disturbed" days when the northward velocity of the north-south component increases with increasing K.

551.510.535:550.386 4243
On the Effect of the Magnetic Field of the Earth on Winds in the Ionosphere—V. P. Dokuchaev. (*Izv. Akad. Nauk SSSR, Ser. Geofiz.*, no. 5, pp. 783–787; May, 1959.) A theoretical treatment of electrodynamic and hydrodynamic processes in the ionosphere showing that, at a height of 110–120 km and in regions above, the geomagnetic field has a considerable effect on the character of ionospheric winds.

551.510.535:550.387 4244
Ionospheric Electrostatic Fields and the Equatorial Electrojet—A. J. Zmuda. (*J. Geophys. Res.*, vol. 65, pp. 2247–2253; August, 1960.) During the time of the peak overhead electrojet current, the eastward electrostatic force has an intensity of 4×10^{-4} v/m and drives an eastward current of density 10^{-5} a/m². If the positive ions are considered stationary, this current corresponds to a westward electron velocity of 620 m/s. The region containing the peak current is electrically neutral, but there are very small excesses of electrons and positive ions to the east and west of the peak, respectively. See also 1987 of June.

551.510.535:621.391.812.3 4245
Fading of C.W. Signals as a means of Spread-F Study—M. S. V. G. Rao, B. R. Rao and P. R. R. Pant. (*Current Sci., India*, vol. 29, pp. 304–305; August, 1960.) Fading records of CW transmissions on 11.717 Mc are analyzed using the spread-F index defined in 2006 of June.

551.510.535:621.391.812.63 4246
A Study of 2-Mc/s Ionospheric Absorption Measurements at High Latitudes—K. Davies. (*J. Geophys. Res.*, vol. 65, pp. 2285–2294; August, 1960.) From a study of the data of five stations in Canada during the IGY, it is found that: a) the winter anomaly of noon absorption occurs at Churchill, but is absent at Resolute Bay; b) the effect of solar zenith angle, as illustrated by the diurnal variation of absorption, decreases with increasing latitude; c) midnight absorption is a maximum in the auroral zone, but is also high over the polar cap.

551.510.535:621.391.812.63 4247
Identification of Mode in Low-Frequency Sweep Ionospheric Sounding, and Interference Patterns between Overlapping Echoes—A. Brunnschweiler and H. N. Carlson. (*Nature, London*, vol. 188, pp. 217–218; October 15, 1960.) The echo is received on a pair of crossed coplanar horizontal dipoles and split into its two circular components by means of a two-channel receiver. The resulting video signals are electrically subtracted and applied as brilliance modulation to a conventional CRT, where the echo is displayed as a light or dark trace, depending on its sense of rotation. The technique is convenient for observing interference fringes, and these effects are discussed.

551.510.535(98) 4248
Some Magneto-ionic Phenomena of the Arctic E Region—J. W. Wright. (*J. Atmos. Terr. Phys.*, vol. 18, pp. 276–289; August, 1960.) Unusual phenomena at Thule (dip 85.5°) are described, and are attributed to the effects of electron collisions on radio wave propagation at high latitudes. The E-layer z component can be

explained in this way. Several phenomena could allow the existence and extent of a valley between the E and F layers to be studied.

551.510.62 4249
Vertical Distribution of Radio Refractive Index in the Medium Height of Atmosphere—K. Tao and K. Hirao. (*J. Radio Res. Labs., Japan*, vol. 7, pp. 85–93; March, 1960.) An examination of radiosonde and captive-balloon data from Japanese stations indicates an exponential variation for the lower atmosphere, but not for the upper.

551.594.5:621.396.96 4250
41-Mc/s I.G.Y. Auroral Radar at Ithaca, New York—C. W. Gartlein, G. Sprague and R. C. Waag. (*J. Geophys. Res.*, vol. 65, pp. 2255–2259; August, 1960.) Echoes are reflected at distances between 500 and 1200 km north of Ithaca. Analysis of those echoes which correspond with visual sightings indicates that the reflections are caused by scattering centers throughout the whole aurora.

551.594.5:621.396.96 4251
Simultaneous V.H.F. Auroral Back-Scatter Measurements—W. A. Flood. (*J. Geophys. Res.*, vol. 65, pp. 2261–2268; August, 1960.) Measurements on 49.7, 143.5 and 226 Mc exhibit a wavelength dependence of $\lambda^{3.5}$ for 49.7- and 143.5-Mc, and $\lambda^{6.5}$ for 143.5- and 226-Mc echoes. The size of the irregularities is about 40 cm transverse to the magnetic field, and is not inconsistent with an estimate of 3 meters along the field.

551.594.6 4252
Some E.L.F. Phenomena—E. T. Pierce. (*J. Res. NBS*, vol. 64D, pp. 383–386; July/August, 1960.) Electric-field fluctuations at frequencies below 1 kc are discussed with reference to EM changes associated with atmospherics and electrostatic variations in atmospheric electricity.

551.594.6 4253
Energy Fluxes from the Cyclotron Radiation Model of V.L.F. Radio Emission—R. A. Santirocco. (PROC. IRE, vol. 48, p. 1650; September, 1960.) Further consideration of the cause of "dawn chorus." See also 2017 of June (Murcray and Pope).

LOCATION AND AIDS TO NAVIGATION

534.88+621.396.663 4254
The Accuracy of Measurement of the Direction of a Sound Source by Directive Receiver Systems—Federici. (See 4088.)

621.396.96 4255
Forward Scattering by Coated Objects Illuminated by Short-Wavelength Radar—R. E. Hiatt, K. M. Siegel and H. Weil. (PROC. IRE, vol. 48, pp. 1630–1635; September, 1960.) Theory and experiment show that partial or total coating with absorbent material increases scattering into the forward lobe when the object is large compared with the incident wavelength.

621.396.96 4256
The Ineffectiveness of Absorbing Coatings on Conducting Objects Illuminated by Long Wavelength Radar—R. E. Hiatt, K. M. Siegel and H. Weil. (PROC. IRE, vol. 48, pp. 1636–1642; September, 1960.) Experimentally confirmed theory shows that thin coatings have little effect on the Rayleigh scattering coefficients of objects small compared with the wavelength; if the wavelength is sufficiently large, thin, slightly conducting sphere scatters as a perfectly conducting sphere.

621.396.96:621.376.23 4257
Application of the Correlation Method to Radar—F. Klempfner. (*Nachrtech.*, vol. 9, pp. 507–511; November, 1959.) A simple cross-correlation system for facilitating signal detection in noise is outlined.

621.396.96:621.376.23 4258
Optimum Radar Integration Time—J. M. Flaherty and E. Kadak. (IRE TRANS. ON ANTENNAS AND PROPAGATION, vol. AP-8, pp. 183–185; March, 1960. Abstract, PROC. IRE, vol. 48, p. 1353; July, 1960.)

621.396.962.33 4259
Broad-Band Frequency-Scanning Radar System—S. R. Hennies and J. V. N. Granger. (*Electronics*, vol. 33, pp. 44–47; September 2, 1960.) A multifrequency HF system is described in which synchronous detection is used to show Doppler shifts caused by target motion. This has been used to study movements of artificially produced clouds of ionization.

621.396.969.34 4260
Aircraft Scintillation Spectra—R. B. Muchmore. (IRE TRANS. ON ANTENNAS AND PROPAGATION, vol. AP-8, pp. 201–212; March, 1960. Abstract, PROC. IRE, vol. 48, pp. 1353–1354; July, 1960.)

MATERIALS AND SUBSIDIARY TECHNIQUES

531.788. 4261
The Effect of Residual Gases on the Supercritical Current of a Static Magnetron—A. S. Borodkin. (*Zh. Tekh. Fiz.*, vol. 29, pp. 778–783; June, 1959.) The lowest pressure detectable by a magnetron manometer is estimated theoretically to be about 10^{-4} mm Hg. This agrees with experimental results.

531.788.7 4262
New Type of Cold-Cathode Vacuum Gauge for the Measurement of Pressures below 10^{-3} mm Hg—G. Barnes. (*Rev. Sci. Instr.*, vol. 31, pp. 608–611; June, 1960.) A gauge using a field-ion emitter source is described which, with a phosphor scintillation probe detector for measuring the ionization current, should be capable of measuring pressures down to 10^{-15} mm Hg.

535.5:621.383+[621.385 4263
Epoxy Resin Joints for Sealed-Off, High-Vacuum Tubes—J. F. Sayers. (*J. Sci. Instr.*, vol. 37, pp. 203–205; June, 1960.)

535.215:546.48'221 4264
Trapping and Diffusion in the Surface Region of Cadmium Sulphide—J. J. Brophy. (*Phys. Rev.*, vol. 119, pp. 591–596; July 15, 1960.) An extension is made of earlier work [2767 of August (Brophy and Robinson)] to include measurements on CdS under 4400-Å illumination.

535.215:546.48'221 4265
Current Noise due to Ohmic Contacts on Cadmium Sulphide—J. J. Brophy and R. J. Robinson. (*J. Appl. Phys.*, vol. 31, pp. 1343–1344; August, 1960.) Current noise measurements on the same lightly doped CdS crystal, having soldered contacts of different-quality In, are used to demonstrate the strong influence of contacts on the observed noise spectra.

535.37:546.47'221:537.533 4266
External Field Emission of ZnS Single Crystals—W. Bertoldi and C. Kleint. (*Ann. Phys., Lpz.*, vol. 4, pp. 388–395; October 13, 1959.) The field emission of pointed ZnS crystals was measured under conditions of darkness, illumination, Ba absorption, and electron bombardment. Currents up to about 0.2 ma were obtained. The I/V characteristics measured are discussed with reference to the theory developed by Stratton (717 of 1956).

535.37:546.48'221 4267
Excitons and the Absorption Edge of Cadmium Sulphide—D. G. Thomas, J. J. Hopfield and M. Power. (*Phys. Rev.*, vol. 119, pp. 570–574; July 15, 1960.)

535.376 4268
Investigations of Cathodothermoluminescence: Part 2—H. Gobrecht, H. Nelkowski and D. Hofmann. (*Z. Phys.*, vol. 156, pp. 657–666; October 6, 1959.) The temperature dependence of cathodoluminescence of various phosphors was measured in the range 90–450°K, and glow curves were obtained after strong and weak cathode-ray bombardment. Part 1: *Z. Elektrochem.*, vol. 61, pp. 202–209; January, 1957 (Gobrecht, Hahn and Scheffler).

535.376 4269
Electroluminescence under Pulsed Square-Wave Excitation—R. Zallen, W. T. Eriksen and H. Ahlburg. (*J. Electrochem. Soc.*, vol. 107, pp. 288–295; April, 1960.) "The slow return of an electroluminescent cell to its equilibrium state following a field excitation has been studied for a blue-green emitting Zn(S,O): Cu, Cl phosphor and for a yellow-emitting ZnS: Mn, Cu phosphor. The light pulse emitted upon the rise of a square voltage pulse was measured as a function of repetition rate and of temperature between −130° and 150°C. Relaxation times encountered varied between 10^{-2} sec and 10^{5} sec."

535.376 4270
Microscopic Observations on Electroluminescent Phosphors—A. Kremheller. (*J. Electrochem. Soc.*, vol. 107, pp. 8–12; January, 1960.) The brightness of single phosphor particles is studied in liquid-dielectric cells.

535.376:546.47-31 4271
The Edge Luminescence of ZnO—B. Andress and E. Mollwo. (*Naturwiss.*, vol. 46, pp. 623–624; November, 1959.) Curves of the spectral distribution of light emission from single-crystal ZnO with excitation by 9-kv electrons are analyzed for components parallel and perpendicular to the c axis.

535.376:546.47'221 4272
Voltage Dependence and Particle Size Distribution of Electroluminescent Phosphors—W. Lehmann. (*J. Electrochem. Soc.*, vol. 107, pp. 20–26; January, 1960.) See also 2266 of 1959.

535.376:546.47'221 4273
The Mechanism and Efficiency of Electroluminescence in ZnS Phosphors—F. F. Morehead, Jr. (*J. Electrochem. Soc.*, vol. 107, pp. 281–287; April, 1960.) An extension is made of earlier work (1214 of 1959).

535.376:546.47'48'221 4274
ZnS:Cu,Cl and (Zn,Cd)S:Cu,Cl Electroluminescent Phosphors—A. Wachtel. (*J. Electrochem. Soc.*, vol. 107, pp. 602–608; July, 1960.) Procedures for the preparation of lead-free electroluminescent phosphors are based on firing the raw materials in an oxidizing atmosphere containing sulphur vapor.

535.376:546.47'48'221 4275
Gold-Activated (Zn,Cd)S Phosphors—M. Avinor. (*J. Electrochem. Soc.*, vol. 107, pp. 608–611; July, 1960.) "Gold is shown to produce three emission bands in CdS at 640, 800 and 1150 mμ. The long wave band appears only when a coactivator is used while the short wave bands are observed with activation by gold alone. The 1150 mμ band in CdS is shown to correspond to the 530 mμ gold band in ZnS."

537.227 4276
Nonlinearity of Certain Ferroelectrics at High Frequency—A. A. Obukhov. (*Fiz. Tverdogo Tela*, vol. 1, pp. 1730–1732; November, 1959.) Results of measurements on $Ba(TiSn)O_3$ show that the variation of permittivity with field intensity at 10 Mc is due to internal heating and is only a function of temperature. The reversible HF permittivity is due to induction polarization.

537.227 4277
Shape of Nucleus Domain Anchored to a Screw Dislocation in Ferroelectric Crystal—H. Takahasi, T. Nakamura and Y. Ishibashi. (*J. Phys. Soc. Japan*, vol. 15, pp. 853–859; May, 1960.)

537.227:546.431'824–31 4278
Theoretical Study on the Properties of Coercive Field of $BaTiO_3$ Single Crystal—R. Abe. (*J. Phys. Soc. Japan*, vol. 15, pp. 795–801; May, 1960.)

537.311.33 4279
Ion Scattering of 'Warm' Electrons in Nondegenerate Nonpolar Semiconductors—K. Seeger. (*Z. Phys.*, vol. 156, pp. 582–591; October 6, 1959.) The theory of carrier heating under the influence of ion and lattice scattering is developed; scattering by acoustic and optical phonons is considered. A comparison with experimental data indicates that ion scattering is insufficient to explain variations between different specimens. See also 164 of 1959 (Sodha and Agrawal).

537.311.33 4280
Dielectric Properties of Semiconductors—H. Rabenhorst and J. Raab. (*Ann. Phys., Lpz.*, vol. 4, pp. 352–359; October 13, 1959.) The dielectric properties of polycrystalline Se and single-crystal Ge and Si were measured as a function of temperature to below −160°C at frequencies between 100 and 400 kc. The loss-angle maxima obtained for Se and Si, and observed by other authors, may be due to surface-contact effects.

537.311.33 4281
Polar Scattering in III-IV Compounds—C. Hilsum. (*Proc. Phys. Soc., London*, vol. 76, pp. 414–416; September 1, 1960.) Available data for various III-V compounds are used to compare measured room-temperature mobilities with values calculated on the basis of polar optical-mode scattering.

537.311.33 4282
A Possible Method of Determining the Ratio of Capture Cross-Sections of Recombination Centres in Semiconductors—S. G. Kalashnikov and K. Konstantinesku. (*Fiz. Tverdogo Tela*, vol. 1, pp. 1763–1766; November, 1959.) The method is based on measurement of the temperature and equilibrium densities of electrons and holes at which the lifetime of excess electrons and holes is independent of their concentration.

537.311.33:539.12.04 4283
Measurement of the Energy of Lattice Defect Formation in Various $A^{III}B^{V}$ Compounds by Electron Irradiation—R. Bäuerlein. (*Z. Naturforsch.*, vol. 14a, pp. 1069–1071; December, 1959.) Measurements were made on InP, GaAs and InAs. Results are compared with radiation-induced energy levels for Si, Ge and InSb.

537.311.33:546.23 4284
The Effect of Tin and Bismuth Impurities on the Thermal Conductivity of Selenium—N. A. Aliev and N. I. Ibragimov. (*Fiz. Tverdogo Tela*, vol. 1, pp. 1668–1669; November, 1959.)

537.311.33:[546.28+546.289 4285
Effect of Deformation on the Energy Spectrum of Holes in Germanium and Silicon—G. E. Pikus and G. L. Bir. (*Fiz. Tverdogo Tela*, vol. 1, pp. 1642–1658; November, 1959.) An expression is derived for the energy spectrum of the holes in a lattice of the Ge type for an arbitrary deformation of the crystal. At high temperatures, the piezoresistive effects are proportional to the deformation and are relatively small; at low temperatures, electrical properties show a sharp anisotropy, the degree of which depends on the direction of the deformation.

537.311.33:[546.28+546.289 4286
An Energy Barrier between Slow Surface Traps and Bulk in Germanium and Silicon—I. I. Abkevich. (*Fiz. Tverdogo Tela*, vol. 1, pp. 1676–1678; November, 1959.) Variations of contact potential with time after illumination ceases are independent of the intensity and wavelength of the light. The width of the energy barrier calculated from experimental data for different samples is in the range 5.8–8 Å. See also 3768 of 1959.

537.311.33:[546.28+546.289 4287
Spin-Lattice Relaxation of Shallow Donor States in Ge and Si through a Direct Phonon Process—H. Hasegawa. (*Phys. Rev.*, vol. 118, pp. 1523–1534; June 15, 1960.) The spin-lattice relaxation rate of certain donors in Ge and Si due to the modulation of the g shift by lattice vibrations has been calculated. The characteristic features of the rate are discussed.

537.311.33:[546.28+546.289 4288
***g*-Factor and Donor Spin-Lattice Relaxation for Electrons in Germanium and Silicon**—L. M. Roth. (*Phys. Rev.*, vol. 118, pp. 1534–1540; June 15, 1960.) The g-factors calculated on the basis of the effective mass approximation are consistent with experimental spin-resonance data. The anisotropic part of g is responsible for a large interaction of donor electron spins with shear waves, and this can account for the small observed spin-lattice relaxation times of donor electrons in Si.

537.311.33:[546.28+546.289 4289
Phonon Broadening of Impurity Lines—E. O. Kane. (*Phys. Rev.*, vol. 119, pp. 40–42; July 1, 1960.) The theory of line broadening given by Lax and Burstein (2030 of 1955) is found not to apply to shallow impurities in Ge and Si.

537.311.33:[546.28+546.289 4290
Internal Friction in Germanium and Silicon: Part 1—Electron and Impurity Relaxation—P. D. Southgate. (*Proc. Phys. Soc., London*, vol. 76, pp. 385–397; September 1, 1960.) The internal friction of single-crystal Si and Ge at 100 kc shows a relaxation peak of electronic origin near 0.56 of the melting temperature. The relaxation time is the carrier lifetime, and the temperature variation of both intrinsic and extrinsic lifetime is deduced. The height of the peak gives the deformation potential constant. The effects of oxygen in Si crystals are discussed.

537.311.33:[546.28+546.289 4291
Internal Friction in Germanium and Silicon: Part 2—Oxygen Movement and Dislocation Damping—P. D. Southgate. (*Proc. Phys. Soc., London*, vol. 76, pp. 398–408; September 1, 1960.) Experimental measurements of internal friction are used to study the production of recombination centers associated with oxygen impurity in Si, and the internal precipitation of oxygen.

537.311.33:546.28 4292
Impact Ionization of Impurities in Silicon at Low Temperature—J. C. Sohm. (*C.R. Acad. Sci., Paris*, vol. 249, pp. 2737–2739; December 24, 1959.) Measurements made on n- and p-type Si specimens at 20°K are reported. See also 212 of January (Kaiser and Wheatley).

537.311.33:546.28 4293
Lifetime Preservation in Diffused Silicon—M. Waldner and L. Sivo. (*J. Electrochem. Soc.*, vol. 107, pp. 298–301; April, 1960.) Experimental results show that lifetimes of 20–100 μsec may be obtained in diffused p-n junctions formed by the diffusion of boron from a BCl_3 carrier. Similar results were obtained with PCl_5 and with chlorine.

537.311.33:546.28 4294
Visible Light Emission and Microplasma Phenomena in Silicon *p*-*n* Junction: Part 1—M. Kikuchi and K. Tachikawa. (*J. Phys. Soc. Japan*, vol. 15, pp. 835-848; May, 1960.) It is found that the light-emitting spot does not necessarily coincide with the microplasma spot. A simple model of a p-n junction is proposed to account for microplasma phenomena.

537.311.33:546.28:535.215 4295
Photoemission from Si Induced by an Internal Electric Field—R. E. Simon and W. E. Spicer. (*Phys. Rev.*, vol. 119, pp. 621–622; July 15, 1960.) "External photoelectric emission from silicon with a threshold of response corresponding to the band gap (1.05 ev) has been observed from a back biased p-n junction which had received a cesium surface treatment. This emission current is proportional to the intensity of the incident light. The spectral distribution of this field-induced photoemission has been simply related to the spectral distribution of the fundamental absorption of silicon."

537.311.33:546.289 4296
The Cross-Section of Capture of Electrons and Holes by Nickel Atoms in Germanium—S. G. Kalashnikov and K. P. Tissen. (*Fiz. Tverdogo Tela*, vol. 1, pp. 1754–1757; November, 1959.)

537.311.33:546.289 4297
Determination of the Ratio of the Electron and Hole Capture Cross-Sections of Copper Atoms in Germanium—K. Konstantinesku. (*Fiz. Tverdogo Tela*, vol. 1, pp. 1766–1768; November, 1959.) A note of results obtained using the method described in 4282 is given.

537.311.33:546.289 4298
Emission Properties of Germanium Treated in Caesium Vapour—V. G. Bol'shov, L. N. Dobretsov, A. A. Zharinov, T. V. Krachino and M. K. Repnikova. (*Fiz. Tverdogo Tela*, vol. 1, pp. 1768–1770; November, 1959.) A brief report is given of an experimental investigation of thermionic, photoelectric and secondary electron emission of n-type Ge single crystals and of Ge films deposited on glass or on Ta foil after Cs-vapor treatment.

537.311.33:546.289 4299
The Diffusion in Germanium Crystals which Contain a Grain Boundary—F. Karstensen. (*Z. Naturforsch.*, vol. 14a, pp. 1031–1039; December, 1959.) The diffusion of As, Sb, In and Ga in Ge along grain boundaries is investigated by observing the migration of a p-n junction. The solution of the diffusion equation for boundary conditions is related to the results of earlier measurements (172 of 1958) and to subsequent work.

537.311.33:546.289 4300
Effect of Cu Precipitation on Dislocation Etch Pits in Ge—H. Savage. (*J. Appl. Phys.*, vol. 31, pp. 1472–1473; August, 1960.)

537.311.33:546.289 4301
Field-Induced Photoemission and Hot-Electron Emission from Germanium—R. E.

Simon and W. E. Spicer. (*J. Appl. Phys.*, vol. 31, pp. 1505–1506; August, 1960.) Effects have been observed in a Ge *p-n* junction similar to those reported for Si (4295). Experimental data are given.

537.311.33:546.289:539.12.04 4302
Transitory Electrical Properties of *n*-Type Germanium after a Neutron Pulse—H. J. Stein. (*J. Appl. Phys.*, vol. 31, pp. 1309–1313; August, 1960.) Measurements of electrical conductivity and Hall effect have been made after neutron bombardment of Sb-doped Ge. The changes found are discussed theoretically.

537.311.33:546.289:621.391.822 4303
Surface-Dependent *1/f* Noise in Germanium—A. U. MacRae and H. Levinstein. (*Phys. Rev.*, vol. 119, pp. 62–69; July 1, 1960.) Noise and field-effect measurements have been made on the same samples as a function of surface parameters. The large increase in *1/f* noise as the surface conductance becomes inverted with respect to the bulk may provide an indication of the source of this noise.

537.311.33:546.47'48'86 4304
The Inversion of the Type of Conductivity of the Semiconducting System $Zn_xCd_{1-x}Sb$—K. Šmirous and L. Štourač. (*Z. Naturforsch.*, vol. 14a, pp. 1073–1074; December, 1959.) Inversion was observed in Te-doped $Zn_{0.15}Cd_{0.85}Sb$, for the doping range 0.025–0.5 per cent.

537.311.33:546.681'18 4305
Observation of Microplasma Pulses and Electroluminescence in Gallium Phosphide Single Crystal—M. Kikuchi and T. Iizuka. (*J. Phys. Soc. Japan*, vol. 15, p. 935; May, 1960.) A brief report of effects similar to those observed in Si *p-n* junctions is given.

537.311.33:546.681'19 4306
Heat Treatment of Gallium Arsenide—J. T. Edmond. (*J. Appl. Phys.*, vol. 31, pp. 1428–1430; August, 1960.) An experimental investigation is made of changes in carrier concentration.

537.311.33:546.682'86 4307
The Change in Electron Mobility in Indium Antimonide at Low Electric Field—Y. Kanai. (*J. Phys. Soc. Japan*, vol. 15, pp. 830–835; May, 1960.) The dependence of electron mobility on electric field, and also the effect of a transverse magnetic field, are studied at 77°, 201° and 297°K. The results indicate the relative importance of lattice scattering by polar and acoustic modes, and of impurity scattering.

537.311.33:546.682'86 4308
Internal Field Emission at Narrow *p-n* Junctions in Indium Antimonide—A. G. Chynoweth and R. A. Logan. (*Phys. Rev.*, vol. 118, pp. 1470–1473; June 15, 1960.) Good agreement has been obtained between experimental results and the theoretical expression for barrier transparency. Temperature-dependence data show that the tunneling in InSb occurs by direct transitions, and that the temperature variation of the tunneling probability is determined almost completely by that of the energy gap.

537.311.33:546.682'86 4309
Infrared Absorption and Valence Band in Indium Antimonide—G. W. Gobeli and H. Y. Fan. (*Phys. Rev.*, vol. 119, pp. 613–620; July 15, 1960.) An investigation of absorption near liquid-helium temperature in *n*- and *p*-type degenerate samples with various carrier concentrations is given.

537.311.33:546.817'241 4310
Weak-Field Magnetoresistance in *p*-Type Lead Telluride at Room Temperature and 77°K—R. S. Allgaier. (*Phys. Rev.*, vol. 119, pp. 554–561; July 15, 1960.)

537.311.33:546.824–31 4311
Electrical and Optical Investigation of Absorption Centres in Rutile Single Crystals—K. G. Srivastava. (*Phys. Rev.*, vol. 119, pp. 516–520; July 15, 1960.)

537.311.33:546.824–31 4312
Transfer of Electric Charges through Rutile Single Crystals—K. G. Stivastava. (*Phys. Rev.*, vol. 119, pp. 520–524; July 15, 1960.)

537.311.33:546.824–31:538.569.4 4313
Electron Paramagnetic Resonance of Fe^{3+} in TiO_2 (Rutile)—D. L. Carter and A. Okaya. (*Phys. Rev.*, vol. 118, pp. 1485–1490; June 15, 1960.)

537.311.33:548.0 4314
Super-Cell Structure of Semiconductors—B. R. Pamplin. (*Nature, London*, vol. 188, pp. 136–137; October 8, 1960.)

537.311.33:621.317.3.029.6 4315
The Measurement of Conductivity in Semiconductors with the Aid of Microwaves—T. Stubb. (*Acta Polytech., Stockholm*, no. 259, ph 2, 14 pp.; 1959.) Application of a resonator method described by Horner, *et al.* (966 of 1946) to the measurement of loss-angle of thin disk-shaped samples with conductivities in the range 0.1–200 $\Omega^{-1}\cdot cm^{-1}$ is given.

537.311.33:621.382.23 4316
***P-N* Junctions between Semiconductors having Different Energy Gaps**—T. K. Lakshmanan. (PROC. IRE, vol. 48, pp. 1646–1647; September 1, 1960.) A *p-n*-junction device using nondegenerate CdO and Se is proposed.

537.312.62 4317
Energy Gap in Superconductors Measured by Electron Tunnelling—I. Giaever. (*Phys. Rev. Lett.*, vol. 5, pp. 147–148; August 15, 1960.) From observation of the *I/V* characteristics of an oxide layer separating two metals at low temperatures, the energy gap for Pb, Sn and In is estimated to be about $4kT_c$ in each case.

537.312.62:538.569.4 4318
Correlation between Superconductivity and Nuclear - Magnetic - Resonance Properties—W. E. Blumberg, J. Eisinger, V. Jaccarino and B. T. Matthias. (*Phys. Rev. Lett.*, vol. 5, pp. 149–152; August 15, 1960.) Measurements of Knight shifts, line widths, and quadrupole interactions in various vanadium intermetallic compounds show striking correlations with the superconductivity transition temperatures of these compounds.

537.312.62:538.63 4319
Critical Field for Superconductivity in Niobium-Tin—R. M. Bozorth, A. J. Williams and D. D. Davis. (*Phys., Rev. Lett.*, vol. 5, p. 148; August 15, 1960.) The critical field for suppression of superconductivity in Nb_3Sn is about 70,000 oersteds at 4.2°K.

538.221 4320
Investigations of the Reversal of the Spin Vectors in Charged 180° Bloch Walls—C. Greiner. (*Ann. Phys., Lpz.*, vol. 5, pp. 57–69; October 31, 1959.) Three types of vector reversal are cons dered, and the charge distribution, wall thickness, and energy concentration are calculated.

538.221 4321
Ferrimagnetism of Mn_3Ge_2—K. Yasukōchi, K. Kanematsu and T. Ohoyama. (*J. Phys. Soc. Japan*, vol. 15, p. 932; May, 1960.) Saturation magnetization measurements over a wide temperature range indicate that Mn_3Ge_2 may be considered as a typical *N*-type ferrimagnetic material with Néel point 710°K and compensation point 395°K.

538.221 4322
Magnetic After-Effect in Iron due to Motion of Dislocations—G. Biorci, A. Ferro and G. Montalenti. (*Phys. Rev.*, vol. 119, pp. 653–657; July 15, 1960.) The observer after-effect in single crystals can be explained as a relaxation of the magnetostrictive stresses due to the interaction among domain walls and dislocations.

538.221:539.23 4323
Magnetoresistive Measurements on Domain Rotation in Nickel-Iron Alloy Films—F. G. West. (*Nature, London*, vol. 188, pp. 129–130; October 8, 1960.) See also 1955 of 1959 (Bradley and Prutton).

538.221:539.23:538.614 4324
The Investigation of Thin Iron Films by means of the Faraday Effect—H. Boersch, M. Lambeck and W. Raith. (*Naturwiss.*, vol. 46, pp. 595–596; November, 1959.) The results of magnetization measurements on Fe film 250 Å thick made by three methods, including that described by Reimer (3592 of 1957), are given.

538.221:539.234 4325
The Effect of Tension on the Transverse Magnetization of Vapour-Deposited Nickel Films—W. Hellenthal. (*Z. Phys.*, vol. 156, pp. 573–581; October 6, 1959.) The reduction of saturation field strength in thin Ni films compared with that of bulk material can largely be attributed to a decrease in spontaneous magnetization and the presence of tensile stress in the plane of the film.

538.221:539.234 4326
The Frequency Dependence of the Coercivity of Thin Vapour-Deposited Nickel Films Measured in an Alternating Magnetic Field—W. Hellenthal. (*Z. Naturforsch.*, vol. 14a, pp. 1077–1078; December, 1959.) Measurements on films of different thickness were made in the frequency range 30 cps–10 kc. See also 3210 of September.

538.221:621.318.134 4327
Exchange Anisotropy Memory Effect—I. S. Jacobs and P. E. Lawrence. (*J. Appl. Phys.*, vol. 31, pp. 1388–1391; August, 1960.) A magnetic "memory" effect is observed in a low-Curie-point ferrimagnetic spinel containing a coherent antiferromagnetic impurity, despite long storage at temperatures above the ferrimagnetic Curie point.

538.221:621.318.134 4328
Diffusion After-Effect in Nickel-Zinc Ferrites Rich in Iron—A. Marais and T. Merceron. (*C.R. Acad. Sci., Paris*, vol. 249, pp. 2511–2513; December 9, 1959.) Three relaxation phenomena occurring in the temperature range from liquid-nitrogen temperature to the Curie point are discussed.

538.221:621.318.134 4329
On the Specific Heat of Zn-Mn and Ni-Zn Ferrite between 20°C and 350°C—J. L. Verhaeghe, G. G. Robbrecht and W. M. Bruynooghe. (*Appl. Sci. Res.*, vol. B8, no. 2, pp. 128–134; 1960.)

538.221:621.318.134:538.652 4330
The Magnetostriction of Lithium-Chromium Ferrite in the Neighbourhood of its Compensation Point—E. W. Lee and R. R. Birss. (*Proc. Phys. Soc., London*, vol. 76, pp. 411–412; September 1, 1960.)

538.222:538.569.4 4331
Paramagnetic Resonance Spectrum of Manganese in Corundum—W. Low and J. T. Suss. (*Phys. Rev.*, vol. 119, pp. 132–133; July 1, 1960.)

538.222:538.569.4:548.5 4332
Preparation of Large Calcium Tungstate Crystals containing Paramagnetic Ions for Maser Applications—K. Nassau and L. G. Van Uitert. (*J. Appl. Phys.*, vol. 31, p. 1508; August, 1960.) A note on the application of the Czochralski method is given.

539.23:[621.372.83+621.317.794 4333
Properties and Applications of Thin Metal Films in the Microwave Range—M. Schneider. (*Tech. Mitt. PTT*, vol. 37, pp. 465–495; November 1, 1959.) Various methods of depositing films are summarized. The applications principally reviewed are waveguide couplers and bolometers. 93 references.

539.232:533.5 4334
Simple Dosing Equipment for Vacuum Vapour Deposition—H. Strosche. (*Z. angew. Phys.*, vol. 11, pp. 441–443; November, 1959.) A mechanism for accurate control of the distribution of the constituents in multielement vapor-deposited films is described.

MATHEMATICS

517.5 4335
Extremum Methods for Certain Electrical Problems involving Homogeneous Anisotropic Material—G. Power. (*Appl. Sci. Res.*, vol. B8, no. 2, pp. 84–92; 1960.) Methods are suggested for estimating the value of an important unknown occurring in certain types of electrical problems by bracketing it between upper and lower bounds.

MEASUREMENTS AND TEST GEAR

529.786 4336
Precision Crystal Chronometer—R. A. Spears. (*Electronic Tech.*, vol. 37, pp. 368–372; October, 1960.) A transistorized battery-operated crystal-controlled clock is described. A thermally sensitive phase-shift network is used to modify the frequency/temperature characteristic of the crystal, and provision can be made to reset the clock for small errors only by a single pulse from a standard source.

621.3.018.12(083.74) 4337
Phase-Angle Master Standard for 400 Cycles per Second—J. H. Park and H. N. Cones. (*J. Res. NBS*, vol. 64C, No. 3, pp. 229–240. July-September, 1960.) Comprehensive design data are given for a continuously variable 0–180° phase shifter with an accuracy within 0.01°. Methods of impedance compensation in calibrating other instruments are described, and the effects of waveform distortion in supply voltage are discussed.

621.3.018.41(083.74):536.58 4338
Precision Thermostat for the Frequency Standards—Y. Hiruta. (*J. Radio Res. Labs., Japan*, vol. 7, pp. 111–124; March, 1960.) Methods of temperature compensation using double ovens for the quartz-crystal standards at Station JJY are described.

621.317.33 4339
On the Influence of Shape and Variations in Conductivity of the Sample on Four-Point Measurements—E. B. Hansen. (*Appl. Sci. Res.*, vol. B8, no. 2, pp. 93–104; 1960.)

621.317.335.3.029.422 4340
A Method for the Determination of the Complex Permitivity of Dielectrics at Very Low Frequencies—H. Martinot. (*C. R. Acad. Sci., Paris*, vol. 249, pp. 2734–2736; December 21, 1959.) The dielectric constant and loss factor of a specimen are determined by a potentiometer method at frequencies between 1 and 10^{-5} cps.

621.317.39:523.164:629.19 4341
Use of the Hydrogen Line to Measure Vehicular Velocity—S. Feldon. (Proc. IRE, vol. 48, p. 1644; September, 1960.) Factors are considered which affect the design of an automatic hydrogen line tracker for continuous measurement of radial velocity with respect to a celestial source.

621.317.44:538.632 4342
Indium Arsenide Hall Generators for Measurement of Magnetic Field Strength—N. V. Zotova and D. N. Nasledov. (*Fiz. Tverdogo Tela*, vol. 1, pp. 1690–1694; November, 1959.)

621.317.444:538.569.4:551.507.362 4343
Magnetic Measurements in Space—D. Mansir. (*Electronics*, vol. 33, pp. 47–51; August 5, 1960.) Proton precession and optically pumped alkali vapor magnetometers are described.

621.317.7:621.374.32:621.387.4 4344
Transistorized Precision Ratemeter—G. Giannelli and V. Mandl. (*Rev. Sci. Instr.*, vol. 31, pp. 623–625; June, 1960.) Full circuit details are given of a ratemeter for use with radiation counters which operates at 10–1000 pulses/sec with an accuracy within 1 per cent.

621.317.729:681.142 4345
The Resistance Network, a Simple and Accurate Aid to the Solution of Potential Problems—Francken. (See 4121.)

621.317.733.029.5:537.226 4346
R.F. Admittance Bridge for Liquid-Dielectric Measurements—R. G. Bennett. (*J. Sci. Instr.*, vol. 37, pp. 195–197; June, 1960.) The bridge described is suitable for the measurement of the complex permittivity of liquid dielectrics at frequencies between 100 kc and 3 Mc.

621.317.755 4347
Multibeam Cathode-Ray Tube aids Shock-Wave Studies—L. Mancebo. (*Electronics*, vol. 33, pp. 51–53; August 26, 1960.) Traces from 39 separate cathodes are controlled by one pair of deflection plates.

621.317.755:621.374 4348
Fractional Millimicrosecond Electrical Stroboscope—W. M. Goodall and A. F. Dietrich. (Proc. IRE, vol. 48, pp. 1591–1594; September, 1960.) Descriptions are given of the strobe pulse generator and coaxial gate of a stroboscope having a rise time of 6×10^{-11} and a 6-db bandwidth of 5.5 kMc.

621.317.794 4349
Resistive-Film Milliwattmeters for the Frequency Bands 8.2–12.4 Gc/s, 12.4–18 Gc/s and 26.5–40 Gc/s—I. Lemco and B. Rogal. (*Proc. IEE*, vol. 107, pt. B, pp. 427–430; September, 1960.) Details are given of improved milliwattmeters using Nichrome films on thin glass for power measurements in the range 1–100 mw (see also 1227 of 1958). The input voltage SWR is 0.8 or higher over the greater part of the frequency bands and the error limit of a dc calibration is ±2 per cent.

OTHER APPLICATIONS OF RADIO AND ELECTRONICS

537.56:629.1.03 4350
Plasma Propulsion by a Rapidly Varying Magnetic Field—M. M. Klein and K. A. Brueckner. (*J. Appl. Phys.*, vol. 31, pp. 1437–1448; August, 1960.) Both diamagnetic and nondiamagnetic plasmas have been considered. The efficiency of conversion of energy appears to be rather low in both cases—probably too low for practical applications in the case of a plasma driven by a magnetic field from a stationary coil.

621.362:537.322 4351
Performance of a Thermoelectric Converter under Constant-Heat-Flux Operation—P. S. Castro and W. W. Happ. (*J. Appl. Phys.*, vol. 31, pp. 1314–1317; August, 1960.) Under conditions of constant heat flux, the optimum operating conditions for a thermoelectric converter differ from those for constant junction temperatures.

621.362:621.385.1 4352
Contribution of Anode Emission to Space Charge in Thermionic Power Converters—A. F. Dugan. (*J. Appl. Phys.*, vol. 31, pp. 1397–1400; August, 1960.) The space-charge theory of Langmuir has been extended to cover this case; calculations indicate that anode emission has the most pronounced effect if the cathode-anode work-function difference is large.

621.362:621.387 4353
Generation of Alternating Current in the Cesium Cell—H. L. Garvin, W. B. Teutsch and R. W. Pidd. (*J. Appl. Phys.*, vol. 31, pp. 1508–1509; August, 1960.) The Cs cell, usually used as a thermionic energy converter, under certain conditions also produces a significance output of ac power. The output waveform depends systematically on the dc terminal voltage.

621.365.029.63:537.56 4354
The Microwave Plasma Burner—W. Schmidt. (*Elektron. Rundschau*, vol. 13, pp. 404–406; November, 1959.) A description is given of an electronic torch [see also 2785 of 1951 (Cobine and Wilbur)] for use at 2.4 kMc in high-temperature heating applications requiring a chemically pure atmosphere.

621.365.55 4355
Microwave Generator for the Dielectric Heating and Drying of Nonmetallic Webs and Foils—W. Schmidt. (*Elektron. Rundschau*, vol. 13, pp. 359–361; October, 1959.) The web of paper, fabric or plastic material passes through slots in the walls of a rectangular waveguide operating in the H_{10} mode and bent so that it repeatedly traverses the web.

621.365.55.029.63 4356
Dielectric Heating at 12-cm Wavelength—A. Frieser. (*Nachrtech.*, vol. 9, pp. 512–514; November, 1959.) A description of a tunable cavity-resonator system and a discussion of the results of dielectric-heating tests carried out with it are given.

621.373.52:551.508.5 4357
Transistor Cup Anemometer—R. R. McGregor. (*J. Sci. Instr.*, vol. 37, pp. 189–190; June, 1960.) A description of an anemometer with a shielding vane controlling a transistor-oscillator switching circuit for remote indication of wind speeds down to 0.2 meter per second is given.

621.38:61 4358
Trends of Development and Present-Day Importance of Medical Electronics—M. von Ardenne. (*Nachrtech.*, vol. 9, pp. 442–448; October, 1959.) The whole field of electronic applications in medicine is reviewed, and tables listing the types of measurement and therapeutic treatment available, the equipment or application, and relevant references are given.

621.383:681.6 4359
Line-Drawing Pattern Recognizer—L. D. Harmon. (*Electronics*, vol. 33, pp. 39–43;

September 7, 1960.) A dilating-circular-scan method gives similar transformations for geometrically similar figures, and can be applied to recognition of numbers and letters in various styles.

621.384.6 4360
A Method of Bunching Fast Electrons—S. P. Kapitsa. (*Zh. Tekh. Fiz.*, vol. 29, pp. 729–731; June, 1959.) A note on a method based on the fact that the time of rotation of an electron in a magnetic field is proportional to its total energy is given.

621.384.611 4361
Cyclotron with an Oblique Accelerating Gap—N. K. Abrosimov. (*Zh. Tekh. Fiz.*, vol. 29, pp. 726–728; June, 1959.) A critical comment on a proposal of Varshni (see 1517 of 1958) is given.

621.384.612 4362
Phase Oscillations in High-Current Synchrotrons—I. G. Henry. (*J. Appl. Phys.*, vol. 31, pp. 1338–1342; August, 1960.) The case of an accelerating voltage of variable amplitude is considered.

621.387.464:621.383.29 4363
Light-Coupled Multivibrator—L. Cathey. (*Rev. Sci. Instr.*, vol. 31, pp. 661–662; June, 1960.) The output from a photomultiplier is used to light an indicator bulb, which further illuminates the photocathode producing a current pulse. This is applied to a scintillation counter operating at frequencies up to 20 kc.

621.398:616 4364
The Technique of Ingestible Intestinal Transmitters—M. von Ardenne, H. Mielke, H. Rackwitz and F. Volland. (*Nachrtech.*, vol. 9, pp. 449–456; October, 1959.) Intestinal transmitters for pressure and pH-value measurements are described, and details are given of the specially developed receiving and recording equipment. See also 3834 of 1959 (von Ardenne and Sprung).

PROPAGATION OF WAVES

621.391.812.6.029.4 4365
Mode Theory and the Propagation of E.L.F. Radio Waves—J. R. Wait. (*J. Res. NBS*, vol. 64D, pp. 387–404; July/August, 1960.) A treatment of the mode theory as applied to propagation in the range 1.0 cps–3 kc is given. Extensions to the theory are developed, including the effects of the earth's magnetic field and an inhomogeneous ionosphere, and the propagation of pulses. See 3631 of October.

621.391.812.6.029.4 4366
Possible Application of the System-Loss Concept at E.L.F.—K. A. Norton. (*J. Res. NBS*, vol. 64D, pp. 413–414; July/August, 1960.) See 4174 of 1959.

621.391.812.6.029.45 4367
Influence of Earth Curvature and the Terrestrial Magnetic Field on V.L.F. Propagation—J. R. Wait and K. Spies. (*J. Geophys. Res.*, vol. 65, pp. 2325–2331; August, 1960.) The attenuation in a sharply bounded and homogeneously ionized medium is: a) increased by a factor of two when the earth's curvature is taken into account; b) much greater when propagation is in the east-west than in the west-east direction. These results are in agreement with experimental data of Taylor (4004 of November).

621.391.812.62 4368
Tropospheric Propagation at V.H.F.—J. M. Dixon. (*Proc. IRE, Australia*, vol. 21, pp. 398–406; June, 1960.) An analysis is made of VHF field-strength recordings of signals propagated over undulating country to distances beyond the horizon.

621.391.812.62 4369
Experimental Test of Reciprocal Radio Wave Propagation over a V.H.F. Circuit—H. Akima. (*J. Radio Res. Labs., Japan*, vol. 7, pp. 125–128; March, 1960.) Tests at 152.05 Mc over a 125-km path show no nonreciprocal effects.

621.391.812.62.029.63:621.397 4370
Problems of U.H.F. Television Propagation—Rowden. (See 4399.)

621.391.812.63 4371
Measurements of Changes in the Phase Path of Radio Waves Reflected from the Ionosphere at Normal Incidence—R. W. E. McNicol and J. A. Thomas. (*Aust. J. Phys.*, vol. 13, pp. 120–131; June, 1960.) The phase changes in pulses reflected from the different layers are described, with photographs of typical phase fringe patterns in which care has been taken to obtain high signal-to-noise ratios and good resolution. The rate of change varies from as low as 1 msec for smooth night E_s layers, to 10–40 msec for the F_2 layer.

621.391.812.63 4372
Approximate Calculations Relating to the Γ-Function and to Weber's Equation. Application to a Plane Electromagnetic Wave which Propagates across an Ionized Layer (in the Presence of Collisions and with Parabolic Distribution of Electron Density as a Function of Height)—R. Meynieux. (*Ann. Télécommun.*, vol. 14, pp. 262–276; November/December, 1959.)

621.391.812.63 4373
Statistical Analysis of Fading of a Single Down-Coming Wave—P. Dasgupta and K. K. Vij. (*J. Atmos. Terr. Phys.*, vol. 18, pp. 265–275; August, 1960.) The amplitude distribution distribution of rapidly fading waves is found to be of the Rayleigh type, while for slow, quasi-periodic fading it conforms to a bimodal distribution, termed *M*-type. Time analysis of both distributions results in a Pearson type-VII distribution for the Rayleigh amplitude distribution and a Gaussian distribution for the *M*-type distribution. Values of the random velocity of the ionospheric irregularities derived from the time analysis and from the autocorrelation function of the amplitude agree well.

621.391.812.63 4374
Note on a Test of the Equivalence Theorem for Sporadic-E Propagation—J. W. Wright and T. N. Gautier. (*J. Res. NBS*, vol. 64D, pp. 347–348; July/August, 1960.) Measurements at vertical and oblique incidence verify the second ϕ frequency relation.

621.391.812.63 4375
Equatorial Ionospheric Effects—T. W. Bennington. (*Wireless World*, vol. 66, pp. 501–506; October, 1960.) Possible causes of post-sunset fading on transequatorial circuits are discussed. The suggestion that the breakup of tropical E_s may sometimes be responsible is used to resolve differences in the characteristics o the Singapore-U.K. and Johannesburg-U.K. circuits.

621.391.812.63:551.507.362.2 4376
Second-Order Faraday Rotation Formulas—Yeh. (See 4219.)

621.391.812.63.029.51:523.5 4377
Changes in the Fading Speed of Low-Frequency Radio Waves—W. A. Cilliers. (*J. Atmos. Terr. Phys.*, vol. 18, pp. 339–341; August, 1960.) Fast fading is associated with meteor incidence on the ionosphere.

621.391.812.63.029.53 4378
Some Medium-Frequency Sky-Wave Measurements—J. M. Dixon. (*Proc. IRE, Australia*, vol. 21, pp. 407–409; June, 1960.) Field-strength measurements in the range 550–1220 kc at distances up to 2000 miles from the transmitter are reported for the period 1953–1958. Correlation of the field strength with sunspot number and E-layer critical frequency is discussed.

621.391.812.63.029.62 4379
The Long-Distance Transmission in the 40–52 Mc/s Waveband via the F_2 Layer—H. Wisbar. (*Nachrtech. Z.*, vol. 12, pp. 547–553; November, 1959.) Investigations of the propagation conditions at 43.6 and 50–52 Mc for the path U.S.A.–Europe were made during the period September, 1958–January, 1959, to assess the validity of the propagation index K_f established for an earlier series of observations (654 of February). The analysis is particularly concerned with abnormal conditions affecting propagation, such as E_s-layer formation, scatter and auroral-type effects.

621.391.812.8 4380
Sunspot-Cycle Variations in the Discrepancies between Predicted and Observed Frequencies for Use in Radiocommunication—R. J. Hitchcock, G. O. Evans, and R. Naismith. (*Proc. IEE*, vol. 107, pt. B, pp. 423–426; September, 1960.) The discrepancies observed over a sunspot-cycle at 18.4 Mc on the London-Bombay circuit are especially marked in summer; these are attributed to the influence of the E_s layer, although there is no marked sunspot-cycle effect attributed to this layer. The phase of the sunspot cycle must therefore be considered in discussing these discrepancies.

RECEPTION

621.391.812.3:621.3.95.625.3 4381
Rapid Frequency Analysis of Fading Radio Signals—J. M. Watts and K. Davies. (*J. Geophys. Res.*, vol. 65, pp. 2295–2301; August, 1960.) Magnetic tape recordings of slowly fading signals are made at tape speeds of about 0.02 inch per second, and played back for analysis at 30 inches per second. The phase of the fading is also obtained using this method.

621.391.82 4382
Measurements of the Spectrum of Radio Noise from 50 to 100 c/s—M. Balser and C. A. Wagner. (*J. Res. NBS*, vol. 64D, pp. 415–418; July/August, 1960.) Experimental noise spectra obtained by a digital processing technique show no significant evidence of earth-ionosphere cavity effects.

621.391.822.2.029.6 4383
Apparent Thermal Noise Temperatures in the Microwave Region—E. Weger. (IRE TRANS. ON ANTENNAS AND PROPAGATION, vol. AP-8, pp. 213–217; March, 1960. Abstract, vol. 48, p. 1354; July, 1960.)

621.391.832.24:621.396.97.029.62 4384
V.H.F. Sound Broadcasting—R. V. Harvey. (*Proc. IEE*, vol. 107, pt. B, no. 35, pp. 412–422; September, 1960. Discussion.) A study is made of distortion for different ratios of the primary and delayed signals, and the manner in which the subjective annoyance changes with the receiver design parameters. For delays corresponding to path differences in the range 8–16 km, a delayed-signal amplitude of 10 per cent of the primary signal can cause perceptible distortion in piano music.

STATIONS AND COMMUNICATION SYSTEMS

621.376.3/.4 4385
Angle-Modulated Wave—W. C. Vaughan. (*Electronic Tech.*, vol. 37, pp. 387–388; Octo-

ber, 1960.) An extension and correction to 3851 of 1959 is given.

621.391 4386
Information Theory—(*Nuovo Cim.*, vol. 13, suppl. no. 2, pp. 337–619; 1959.) The text is given in English of papers presented at the 7th Course of the International School of Physics, held at Varenna, July 7–14, 1958.

621.391 4387
Sampling Theorem of the Second Kind—H. Wolter. (*Arch. elekt. Übertragung*, vol. 13, pp. 477–481; November, 1959.) The validity of a modified sampling theorem is investigated. See also 4027 of November.

621.391:519.272 4388
Noise Conditions in Real Correlation Processes—K. H. Schmelovsky. (*Nachrtech.*, vol. 9, pp. 505–507; November, 1959.) A problem of practical correlation analysis involving integration over finite periods is discussed.

621.391:621.394 4389
On the Transmission of Information by Orthogonal Time Functions—H. F. Harmuth. (*Commun. and Electronics*, no. 49, pp. 248–255; July, 1960.) See also 4390.

621.391:621.396.65 4390
Radio Communication with Orthogonal Time Functions—H. F. Harmuth. (*Commun. and Electronics*, no. 49, pp. 221–228; July, 1960.) Characteristic properties of systems using orthogonal time functions for the transmission of information over radio links are described.

621.395:621.376.3:621.391.833.44 4391
Error Probabilities for Telegraph Signals Transmitted on a Fading F.M. Carrier—B. B. Barrow. (PROC. IRE, vol. 48, pp. 1613–1629; September, 1960.) Analysis of element error probabilities for frequency-shift, phase-shift and amplitude-keyed signals indicates that most errors occur when the carrier fades below the receiver threshold. A method is given for extending results obtained for a single receiver to multiorder diversity systems, and the importance of the performance of diversity combiners below the threshold is demonstrated. See also 1396 of April (du Castel and Magnen).

621.395:621.376.5 4392
The Optimum Detection of Analogue-Type Digital Data—E. Bedrosian. (PROC. IRE, vol. 48, pp. 1655–1656; September, 1960.) Minimization of the mean-square error between detector output and the original signal leads to a design criterion which is a function of pulse amplitude. Error reduction over a conventional detector is about 1 db.

621.396.65:621.391.812.624 4393
Optimum Design Considerations for Radio Relays utilizing the Tropospheric Scatter Mode of Propagation—C. A. Parry. (*Commun. and Electronics*, no. 47, pp. 71–80; March, 1960.) 53 references.

621.396.946 4394
Optimum Frequency Selection for Interplanetary Communication—S. Chandra. (*J. Brit. Interplanetary Soc.*, vol. 17, pp. 362–365; July/August, 1960.) The power required for one-way radio communication from the Earth to Jupiter, Venus, Mars and the Moon has been calculated at various frequencies by choosing suitable minimum detectable power, molecular atmospheric absorption, receiver bandwidth and antenna gains; a frequency of 3000 Mc is considered most suitable.

SUBSIDIARY APPARATUS

621-526 4395
An Optimal Discrete-Stochastic-Process Servomechanism—G. C. Sponsler. (PROC. IRE, vol. 48, pp. 1647–1648; September, 1960.) An extension of Mill's theorem is given.

621.324.63 4396
The Influence of Impurities on the Strong-Field Effect in Selenium Rectifiers—G. B. Abdullaev, M. G. Aliev and I. Kh. Geller. (*Fiz. Tverdogo Tela*, vol. 1, pp. 1670–1675; November, 1959.) The reverse *I/V* characteristic of Se rectifiers depends chiefly on the purity of the materials used. With pure Se, the reversal of the sign of the temperature coefficient is displaced towards lower temperatures and higher voltages.

621.314.63:621.382.333.3 4397
The Design of Controlled Rectifiers using Triode Transistors—E. E. Ward. (*Proc. IEE*, vol. 107, pt. B, pp. 473–480; September, 1960.) Polyphase rectifiers are described with switching elements of *p-n-p* and *n-p-n* transistors, and stability conditions are investigated graphically.

621.316.722.078.3 4398
Highly Stable Medium-Voltage Direct- and Attenuating-Voltage Sources: Part 2—R. Stenzel and H. Helke. (*Z. angew. Phys.*, vol. 11, pp. 443–448; November, 1959.) An addition is made to an earlier review (2115 or 1955) dealing with short-term stabilization by tube circuits or transductors, and with the reduction of long-term drift in dc power units. 27 references.

TELEVISION AND PHOTOTELEGRAPHY

621.397:621.391.812.62.029.63 4399
Problems of U.H.F. Television Propagation—R. A. Rowden. (*J. Telev. Soc.*, vol. 9, pp. 223–229; April–June, 1960.) The effect of a sharply-beamed vertical radiation pattern on the local coverage of a transmitter is discussed, and curves of variation of field strength with distance based on data from U.K. and U.S.A. measurements are compared. The greater variation of field strength in built-up areas of UHF compared with VHF is shown. Interference due to long-distance propagation, particularly over sea, is considered.

621.397.13:621.376.56:621.395 4400
Video Transmission over Telephone Cable Pairs by Pulse Code Modulation—R. L. Carbrey. (PROC. IRE, vol. 48, pp. 1546–1561; September, 1960.) A description of a seven-digit PCM system which is used for transmission of quality television signals over standard voice-frequency telephone circuit is given. The system uses the reversed binary code with the Sears coding tube.

621.397.132 4401
The Problem of Compatibility between Modified N.T.S.C. Colour Television Systems with Differing Chrominance Bandwidths—K. Bernath. (*Tech. Mitt. PTT*, vol. 37, pp. 496–503; November 1, 1959.) A theoretical investigation is made of the distortion of color images which would result from a program exchange between two 625-line systems of differing characteristics, such as those based on the CCIW and the OIR standards.

621.397.132 4402
Comparison of Transient Response of the Electronics and the Picture Tube in Colour Television—P. Neidhardt. (*Elektron. Rundschau*, vol. 13, pp. 399–403; November, 1959.) An analysis is made of the transient effects inherent in the NTSC system, including those arising in the circuit and electron-optical system and those due to inertia of the tube-screen phosphors. The effects of these transients on picture quality are tabulated.

621.397.132:621.395.625.3 4403
Operational Facilities in the RCA Colour Television Tape Recorder—A. H. Lind. (*J. Brit. IRE*, vol. 20, pp. 611–619; August, 1960.)

621.397.334:621.397.62 4404
Single-Gun v. Three-Gun Tubes: their Influence on Colour Receiver Design—R. N. Jackson. (*J. Telev. Soc.*, vol. 9, pp. 207–222; April–June, 1960.) Basic problems and advantages of each type are discussed, and circuit requirements are outlined.

621.397.62:621.373.444.1 4405
A New Vertical Timebase—E. M. Cherry. (*Proc. IRE, Australia*, vol. 21, pp. 387–393; June, 1960.) A description and analysis of a timebase circuit for use in television receivers are given. Improved characteristics are obtained by the use of a high-gain negative-feedback loop.

621.397.62:621.375.2 4406
Improvements in Television Receivers: Part 8—The Design of Frame Output Stages—B. G. Dammers, A. G. W. Uitjens, A. Boekhorst, A. M. H. Schellekens and A. P. Tanis. (*Electronic Applic.*, vol. 20, pp. 1–11; February, 1960.) Part 7: 4048 of November (Dammers, *et al.*).

621.397.62:621.376.33 4407
Synchronous Demodulator for Television—P. J. Waller. (*Electronic Tech.*, vol. 37, pp. 378–382; October, 1960.) The unit described enables accurate measurements to be made on vestigial-sideband systems, and provides high-quality monitoring facilities.

621.397.743 4408
The Principles of Planning of Television Transmitter Networks in Bands IV/V—H. Fleischer and W. Berndts. (*Nachrtech. Z.*, vol. 12, pp. 554–560; November, 1959.) The fundamental differences in planning for Bands I and III and for Band IV/V networks are outlined. The problems of transmitter height/range characteristics, siting, power and frequency allocation are discussed and illustrated by the example of a 60-channel network.

TUBES AND THERMIONICS

621.382.032.9 4409
Equipment for the Encapsulation of Semiconductor Devices—R. D. Knight. (*J. Sci. Instr.*, vol. 37, pp. 197–199; June, 1960.) A detailed description of a production process which lends itself to automation is given.

621.382.2/.3 4410
Spreading Resistance in Cylindrical Semiconductor Devices—D. P. Kennedy. (*J. Appl. Phys.*, vol. 31, pp. 1490–1497; August, 1960.) Computation of the spreading resistance is considered a boundary-value problem of the solid circular cylinder. The solutions may be used to characterize several semiconductor devices.

621.382.22 4411
Radiative Recombination in Gallium Phosphide Point-Contact Diodes—H. C. Gorton, J. M. Swartz and C. S. Peet. (*Nature, London*, vol. 188, pp. 303–304; October 22, 1960.) A measurement of the energy spectrum has been made by a simple arrangement of a diffraction grating and a 35-mm camera. Results show the energy of the recombination radiation to be between 1.96 and 2.19 ev with a peak density at 2.12 ev.

621.382.23 4412
Gallium Arsenide Diffused Diodes—J. Lowen and R. H. Rediker. (*J. Electrochem. Soc.*, vol. 107, pp. 26–29; January, 1960.) A

description of the fabrication techniques and electrical properties of GaAs diffused diodes designed for use as variable capacitors and computer diodes is given. Rectification ratios (at 2 volts of 10^{10} and switching times of 10^{-9} seconds have been obtained.

621.382.25 4413

GaAs Tunnel Diodes—R. Gremmelmaier and H. J. Henkel. (*Z. Naturforsch.*, vol. 14a, pp. 1072–1073; December, 1959.) Room temperature *I/V* characteristics are given for three GaAs tunnel diodes made by alloying Zn-doped GaAs with Sn. The characteristics of one of these diodes measured at 100°, 300° and 450°K show that these diodes are useful over a wide temperature range. The time constant is of the order of 10^{-8} seconds and could be improved by stronger doping.

621.382.23 4414

Investigation of *p-n* Junctions at High Current Densities—Yu. V. Barsukov. (*Fiz. Tverdogo Tela*, vol. 1, pp. 1659–1667; November, 1959.) An investigation of the transition blocking process in fused In-Ge *p-n* junctions at high injection levels for forward current densities of 10–1000 a/cm² is given. The inertia of the junction decreases with increase in the forward current preceding the blocking process. This is attributed to retardation in the increase of excess carrier density due to marked carrier injection in the high-impurity region.

621.382.3.012 4415

A Representation of the High-Frequency Characteristics of Transistors—W. Engbert. (*Telefunken Röhre*, no. 36, pp. 5–44; October, 1959.) The transistor is treated as a current node for the emitter, base and collector currents; a current vector triangle can then be derived to represent any operating condition for small-signal operation.

621.382.333 4416

On the Variation of the Transport Factor of a Junction Transistor with Injected Carrier Concentration—A. N. Daw. (*Indian J. Phys.*, vol. 34, pp. 20–35; January, 1960.) An attempt is made to set up a general equation for the distribution of injected carriers in the base region of a *p-n-p* junction transistor and hence to obtain an expression for the transport factor. Results are compared with those of other workers, *e.g.*, Kaufmann (2556 of July).

621.382.333 4417

Epitaxial Diffused Transistors—H. C. Thuerer, J. J. Kleimack, H. H. Loar and H. Christensen. (Proc. IRE, vol. 48, pp. 1642–1643; September, 1960.) A thin semiconducting layer, epitaxially deposited on low-resistivity substrates of the same semiconductor, substantially reduces the collector series resistance and excess stored charge. Switching speed and high-frequency gain are increased.

621.382.333.3 4418

Voltage Breakdown of Junction Transistors in a General Circuit—W. Guggenbühl. (*Arch. elekt. Übertragung*, vol. 13, pp. 451–461; November, 1959.) The various mechanisms of voltage breakdown are reviewed, with particular consideration of avalanche breakdown. A formula is derived for the maximum permissible collector voltage as a function of external circuit parameters. The methods of specifiying maximum voltage limits used by various manufacturers are compared.

621.382.333.3.012.8 4419

A Simple Equivalent Circuit of Junction Transistors taking account of the Temperature Dependence—J. Winter. (*Frequenz*, vol. 13, pp. 351–359; November, 1959.) Giacoletto's equivalent circuit is modified by taking account of barrier-layer capacitances, and the problem of stabilizing the collector current is considered.

621.382.333.33:621.372.632 4420

Transistor Operation beyond Cut-Off Frequency—V. W. Vodicka and R. Zuleeg. (*Electronics*, vol. 33, pp. 56–60; August 26, 1960.) Nonlinearities in transistor characteristics are used in a converter circuit to provide useful gain well beyond the normal cutoff limits of HF transistors.

621.382.333.33.012.8 4421

On the Determination of the Extrinsic Equivalent-Circuit Parameters of Drift Transistors—M. B. Das. (*J. Electronics and Control*, vol. 8, pp. 351–363; May, 1960.) Methods presented involve measurements at frequencies less than the cutoff frequency. Results obtained by these and other methods are compared for several types of graded-base transistor.

621.383.001.4 4422

High-Frequency Light Modulation—R. L. Williams. (*J. Sci. Instr.*, vol. 37, pp. 205–208; June, 1960.) Apparatus for measuring response time of infrared detectors is described. Details are given of the electrical drive and suspension circuits for a high-speed rotor one inch in diameter and having 180 reflecting faces. Response times down to 0.02 μsec can be measured. An example is given of the application of the system to measurements on an InSb specimen.

621.383.5 4423

The Inertia of Selenium Barrier-Layer Photocells—F. König. (*Z. angew. Phys.*, vol. 11, pp. 418–428; November, 1959.) The results of measurements of impedance and alternating photo-EMF as a function of frequency and bias voltage on 16 different photocells are discussed to assess the adequacy of representing the photocell by equivalent two-pole networks. An interpretation of the inertia effects observed is given; this does not cover relaxation effects at frequencies below about 15 cps.

621.383.53:621.373.52 4424

Circuit Applications of Field-Effect Transistors—Bockemuehl. (See 4142.)

621.385.032.212 4425

Internal Field Emission and Low-Temperature Thermionic Emission into Vacuum—D. V. Geppert. (Proc. IRE, vol. 48, pp. 1644–1646; September, 1960.) Constructional and experimental details are given of a barrier-layer cold cathode using Cu_2O as the barrier material. See also 2180 of June (Mead).

621.385.032.213.13 4426

Migration of the Activators Magnesium and Silicon in Indirectly Heated Oxide Cathodes—W. Düsing. (*Telefunken Röhre*, no. 36, pp. 99–110; October, 1959.) The changes of activator distribution in the Ni sleeve are considered as a function of cathode operating time. In overheated cathodes, the major part of the activator migration takes place during the first 50–1000 hours.

621.385.032.213.13 4427

The Determination of the Oxide Content of Silicon and Magnesium in the Cathode Nickel to Obtain its True Activator Content—H. Leibiger. (*Telefunken Röhre*, no. 36, pp. 111–134; October, 1959.)

621.385.032.213.13 4428

The Problem of Electrical Breakdowns between Filament and Cathode Sleeve of Indirectly Heated Oxide Cathodes—K. Veith and H. Kallweit. (*Telefunken Röhre*, no. 36, pp. 135–158; October, 1959.) Model tests show that heater breakdowns are caused by the oxidation of residual gas or by oxide films on the tungsten filament of the heater. These results do not agree with existing hypotheses on breakdown.

621.385.032.213.13:535.37 4429

Anode Luminescence in Oxide-Cathode Receiving Valves—H. N. Daglish. (*Proc. IEE*, vol. 107, pt. B, pp. 481–484; September, 1960.) The nature of the luminescent material is examined, and the results suggest that it is barium and/or strontium oxide transferred from the cathode coating during processing.

621.385.032.214:537.56 4430

Negative-Glow Plasma as a Cathode for Electron Tubes—J. M. Anderson and L. A. Harris. (*J. Appl. Phys.* vol. 31, pp. 1463–1468; August, 1960.) The noise content of the plate current of an amplifier using the glow plasma as a cathode has been measured. The equivalent noise-diode current was about 10 times the plate current at 50 kc, reducing to about 0.5 times at 50 Mc.

621.385.032.26 4431

Balanced Acceleration and Deflection Electrostatic Focusing—P. A. Sturrock. (*J. Electronics and Control*, vol. 8, pp. 267–272; April, 1960.) A suitable combination of acceleration focusing and deflection focusing leads to a model for a periodic electrostatic system for the focusing of sheet beams which is free from instabilities.

621.385.032.269.1 4432

A Study of Aperture-Type Electron Lenses with Space Charge—L. A. Harris. (*J. Electronics and Control*, vol. 8, pp. 241–265; April, 1960.) The electron-optical action of round and slit apertures in the anodes of parallel-plane diodes is investigated.

621.385.1 4433

Passage of Current through the Glass Envelope of a Receiving-type Valve—H. N. Daglish. (*Brit. J. Appl. Phys.*, vol. 11, pp. 440–445; September, 1960.) Experiments are described for measuring the current flow and the parameters that affect it. Results indicate that the risk of permanent impairment of cathode emission is very small.

621.385.1:621.362 4434

Contribution of Anode Emission to Space Charge in Thermionic Power Converters—Dugan. (See 4352.)

621.385.2:530.17 4435

Analogue Study of Large-Signal High-Frequency Diodes—C. L. Andrews. (*J. Appl. Phys.*, vol. 31, pp. 1431–1437; August, 1960.) A rolling-ball analog was developed for studying the motion of electrons in a high-frequency longitudinal field. Current densities at various points and plate currents could be derived from the model.

621.385.2:621.391.822.3 4436

The Autocorrelation Function and the Power Spectrum of Nonstationary Shot Noise—L. P. Hyvärinen. (*Acta Polytech., Stockholm*, no. 252, el 2, 23 pp.; 1958.) Expressions for the autocorrelation function and statistical power spectrum of nonstationary shot noise in a temperature-limited diode are derived.

621.385.3/.5 4437

The Drive Range of Grid-Controlled Valves—P. Wolfram. (*Nachrtech. Z.*, vol. 12, pp. 573–578; November, 1959.) The relation of the grid-control range under ac conditions of triodes and multigrid tubes to the static characteristics of the tube is investigated, taking account of the cathode-interface impedance and rectification effects. Calculated and measured results are compared for high-slope pentodes.

621.385.3.029.63 4438
Investigation of Disk-Seal Triodes Type 2C39 in Oscillators—G. Pusch and H. Schnitger. (*Nachrtech. Z.*, vol. 12, pp. 566–572; November, 1959.) An oscillator circuit is described for testing the triodes at 2.6 kMc under normal operating conditions, and typical results obtained are discussed.

621.385.4.029.63:621.397.61 4439
New Grid-Controlled Valves for U.H.F. Television Transmitters—W. Kleen. (*Arch. elekt. Übertragung*, vol. 13, pp. 467–474; November, 1959.) The design is described and characteristics are given of two types of air-cooled tetrode capable of providing peak pulse power of 2.2 and 10 kw, respectively, at 790 Mc.

621.385.6 4440
Microwave Valves: a Survey of Evolution, Principles of Operation and Basic Characteristics—C. H. Dix and W. E. Willshaw. (*J. Brit. IRE*, vol. 20, pp. 577–609; August, 1960.)

621.385.6+621.387:621.375.9:621.372.44 4441
Parametric Amplifier Theory for Plasmas and Electron Beams—Kino. (See 4159.)

621.385.6:621.391.822 4442
Partition Noise in Electron Beams at Microwave Frequencies—A. Ashkin and L. D. White. (*J. Appl. Phys.*, vol. 31, pp. 1351–1357; August, 1960.) The partition noise at 4080 Mc was studied in a beam which passed through a meshed grid. With cathode magnetic fields somewhat below those corresponding to immersed flow, the partition noise exhibited sharp dips as the grid was moved through the image planes of the cathode, but with small fields the noise varied sinusoidally with the cyclotron periodicity.

621.385.63 4443
The Role of Space-Charge Waves in Modern Microwave Devices—G. D. Sims and I. M. Stephenson. (*Electronic Engrg.*, vol. 32, pp. 408–412, 499–503, and 567–571; July–September, 1960.) An introduction to the properties of space-charge waves and the part they play in the operation of backward-wave oscillators, traveling-wave tubes, parametric amplifiers and simple plasmas is given.

621.385.63 4444
The Calculation of Electron Trajectories in Superposed Electrostatic and Magnetic Fields taking account of Space-Charge Forces—R. Hechtel and R. Johne. (*Telefunken Röhre*, pp. 45–64; October, 1959.) The method given is based on the derivation of an "equivalent potential" which defines the motion of an electron in a plane rotating with the electron around the axis of symmetry. The method is applied to the calculation of trajectories in the electron gun of a traveling-wave tube with periodic magnetic focusing.

621.385.63 4445
A Low-Noise Travelling-Wave-Valve Amplifier for the 4000-Mc/s Region—K. B. Niclas and R. Hechtel. (*Telefunken Röhre*, no. 36, pp. 75–98; October, 1959.) Design details are given of a low-noise tube for the range 3.3–4.3 kMc with a noise figure <7 db and gain ≥ 20 db.

621.385.63:621.376 4446
Analysis of Modulated Travelling-Wave Devices and Beam-Type Parametric Amplifiers—H. Sobol and J. E. Rowe. (*J. Electronics and Control*, vol. 8, pp. 321–349; May, 1960.) Modulation frequencies much lower than, and comparable to, the carrier frequency are considered. Design recommendations for traveling-wave tubes for low modulation frequencies are given, and the high-frequency analysis is applied to the longitudinal-beam parametric amplifier.

621.385.63:621.396.65 4447
A Travelling-Wave Valve for Radio Link Operation in the 4-kMc/s Range—W. Heidborn. (*Nachrtech.*, vol. 9, pp. 485–489; November, 1959.)

621.385.63.032.269.1 4448
A Magnetically Partially Screened Electron Gun for a Travelling-Wave Valve—R. Johne. (*Telefunken Röhre*, pp. 65–74; October, 1959.) A method is given for producing and measuring a magnetic field of a given shape and size in an electron gun. An electron gun capable of giving laminar electron flow with the electron paths parallel to the magnetic lines of force is described.

621.385.64 4449
General Steady-State Theory of Linear Magnetrons: Part I—P. A. Lindsay. (*J. Electronics and Control*, vol. 8, pp. 177–206; March, 1960.) Expressions are given for the volume density of the emitted electrons and for the two components of the electron current density, on the assumption that the electrons have a Maxwellian distribution of their emission velocities.

621.385.64:537.533 4450
Instability of the Electron Cloud in a Magnetron—B. B. Kadomtsev. (*Zh. Tekh. Fiz.*, vol. 29, pp. 833–844; July, 1959.) In a field larger than the critical field, the static space charge in a whole-anode magnetron with a loop-type movement of electrons is unstable and cannot maintain its structure for much longer than the electron transit time.

621.387:621.362 4451
Generation of Alternating Current in the Cesium Cell—Garvin, Teutsch and Pidd. (See 4353.)

MISCELLANEOUS

621.38/.39:061.4 4452
Firato 1960—(*Wireless World*, vol. 66, pp. 482–483; October, 1960.) A review is given of the international radio and electronics exhibition held at Amsterdam, Holland, August 30–September 6, 1960.

621.38/.396:061.4 4453
Ainshow Electronics—(*Wireless World*, vol. 66, pp. 480–481; October, 1960.) A review is given of electronic equipment at the SBAC exhibition at Farnborough, Eng., September, 1960, noting recent trends in automatic systems for control and navigation.

621.39:061.4 4454
National Radio Show Review—(*Wireless World*, vol. 66, pp. 489–496; October, 1960.) A report is given of recent trends seen at the exhibiton held in London, Eng., August 24–September 3, 1960.

621.396/.397 4455
The Technical Problems of Broadcasting—(*Engineering, London*, vol. 189; January 1, 15 and 29, and February 12 and 26, 1960.) Five papers reviewing the problems and summarizing, in particular, the solutions adopted by the BBC are given.

Part 1: Sharing the Ether—E. L. E. Pawley (p. 22–23).
Part 2: Managing the Low Frequencies—D. E. L. Shorter (pp. 100–101).
Part 3: Linking the Television Network—J. C. Gallagher (pp. 168–169).
Part 4: Feeding the Transmitting Aerial—F. D. Bolt (pp. 241–242).
Part 5: Televising Internationally—R. D. A. Maurice (pp. 305–306).

Translations of Russian Technical Literature

Listed below is information on Russian technical literature in electronics and allied fields which is available in the U. S. in English language. Further inquiries should be directed to the sources listed. In addition, general information on translation programs in the U. S. may be obtained from the Office of Science Information Service, National Science Foundation, Washington 25, D. C., and from the Office of Technical Services, U. S. Department of Commerce, Washington 25, D. C.

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Journal of Technical Physics (Zhurnal Tekhnicheskoi Fiziki)	Monthly	Complete journal	National Science Foundation—AIP	American Institute of Physics 335 E. 45 St., New York 17, N. Y.
Proceedings of the USSR Academy of Sciences: Applied Physics Section (Doklady Akademii Nauk SSSR: Otdel Prikladnoi Fiziki)	Bimonthly	Complete journal		Consultants Bureau, Inc. 227 W. 17 St., New York 22, N. Y.
Radio Engineering (Radiotekhnika)	Monthly	Complete journal	National Science Foundation—MIT	Pergamon Institute 122 E. 55 St., New York 22, N. Y.
	Monthly	Abstracts only		Office of Technical Services U. S. Dept. of Commerce Washington 25, D. C.
Radio Engineering and Electronics (Radiotekhnika i Elektronika)	Monthly	Complete journal	National Science Foundation—MIT	Pergamon Institute 122 E. 55 St., New York 22, N. Y.
	Monthly	Abstracts only		Office of Technical Services U. S. Dept. of Commerce Washington 25, D. C.
Solid State Physics (Fizika Tverdogo Tela)	Monthly	Complete journal	National Science Foundation—AIP	American Institute of Physics 335 E. 45 St., New York 17, N. Y.
Telecommunications (Elekprosviaz')	Monthly	Complete journal	National Science Foundation—MIT	Pergamon Institute 122 E. 55 St., New York 22, N. Y.
	Monthly	Abstracts only		Office of Technical Services U. S. Dept. of Commerce Washington 25, D. C.
Automation Express	10/year	A digest: abstracts, summaries, annotations of various journals		International Physical Index, Inc. 1909 Park Ave., New York 35, N. Y.
Electronics Express	10/year	A digest: abstracts, summaries, annotations of various journals		International Physical Index, Inc. 1909 Park Ave., New York 35, N. Y.
Physics Express	10/year	A digest: abstracts, summaries, annotations of various journals		International Physical Index, Inc. 1909 Park Ave., New York 35, N. Y.
Express Contents of Soviet Journals Currently being Translated into English	Monthly	Advance tables of contents of translated journals		Consultants Bureau, Inc. 227 W. 17 St., New York 22, N. Y.
Technical Translations	Twice a month	Central directory in the U. S. of translations available from all major sources in the U. S.	OTS and Special Libraries Assoc.	Superintendent of Documents U. S. Gov't Printing Office Washington 25, D. C.

WHAT HAPPENED AT IBM IN 1960?

Here are some of the significant achievements in research and engineering during the past year.

NEW OPTICAL MASER

IBM scientists have developed a new approach to the continuous generation of coherent light waves, both in the visible and infrared portions of the electromagnetic spectrum. Two new optical masers emit intense beams of coherent light, one at 2.5 microns in the infrared region, and the other at .708 microns in the red portion of the visible spectrum. "Trivalent" uranium ions are the key to the new infrared device; "divalent" samarium ions in the visible red light maser. The IBM masers operate on about 1/500th the amount of power required by the ruby optical maser—the only previous one disclosed. Continuous generation of coherent light shows promise for use in radar, data processing, and space guidance systems.

VAPOR GROWTH PROCESS

A process was developed by which semiconductors can be grown from the vapor state to almost any desired purity or configuration. This major advance in solid-state technology is expected to permit eventual fabrication of functional circuit-building blocks in one continuous process for future high-speed computers.

LANGUAGE "TRANSLATOR"

A machine that translates foreign languages into English was demonstrated. Under a program sponsored by the Air Force, IBM has translated a Russian newspaper into rough but meaningful English since June, 1959. Heart of the translating system is a rotating glass disc—"photoscopic disc memory."

IMPROVED TUNNEL DIODE

A new developmental diode, which switches at speeds faster than 4/10ths of a billionth of a second, promises far greater speed and reliability for tunnel diode circuits. It is fabricated by a new method involving an electronically monitored and controlled etching technique.

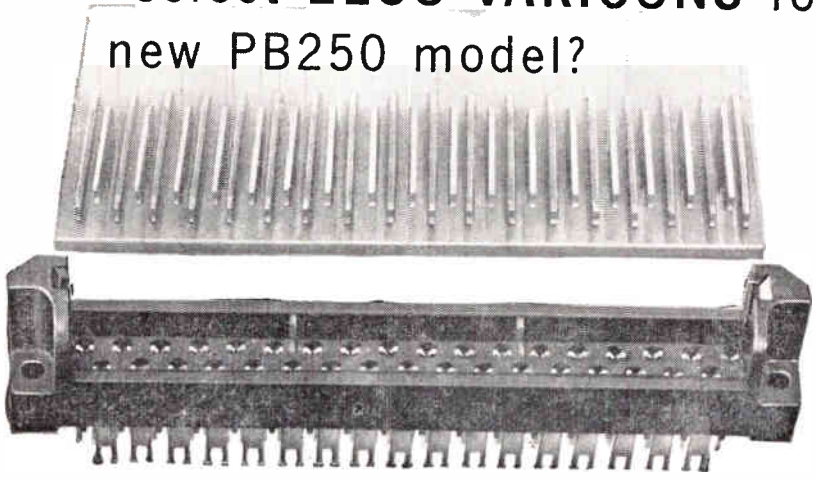
AUTOMATIC REPRODUCTION OF CRYOGENIC MEMORY PLANE

IBM announced the successful fabrication of a cryogenic thin-film memory plane and the development of automatic control techniques capable of duplicating it many times. The memory plane consists of 135 cryotron devices built up in 19 layers of material. Using 17 microscopically adjusted masks, thin layers of metals and insulating material are automatically deposited on a glass substrate.

OTHER SIGNIFICANT ACHIEVEMENTS

- Detection of cyclotron resonance in Group II-V semiconductors
- Development of a 3″ computer memory drum for airborne systems
- A computer-directed navigation display system enabling a pilot to "see" his position on a map.

why did PACKARD BELL COMPUTER select ELCO VARICONS for its new PB250 model?



because ...the reliability

which Packard Bell required for its amazingly small, medium-scale, low cost model (capable of competing with large-scale, high cost models) was "... further increased by the use of Varicon Connectors." This is another example of another world famous manufacturer relying upon the reliability of the Varicon contact, with its unique forklike design and 4 coined mating surfaces. Packard Bell specified our Series 7001, 35 contact subminiature printed circuit Varicons. They are also available to you along with countless others for a limitless variety of applications. In each, you will find the same unchallenged reliability; plus the versatility challenged only by your own imagination!

so why not request your copy of Varicon Catalog V4 immediately!

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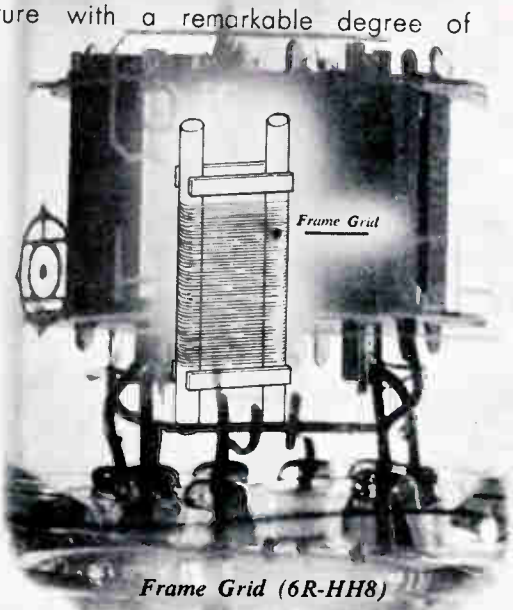
The Highest Sensitivity
and the lowest noise.....

Advanced electronic research by Hitachi technicians has now resulted in the development of a superb frame grid type twin triode (6R-HH8) with excellent high gain and low noise characteristics. As a component of the tuner, the 6R-HH8 ensures an excellent picture with a remarkable degree of definition.



Frame Grid (6R-HH8)

fig. 1 Gain characteristics

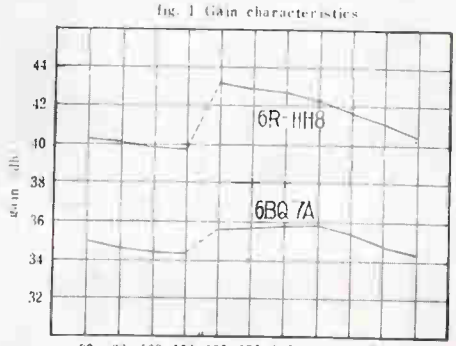
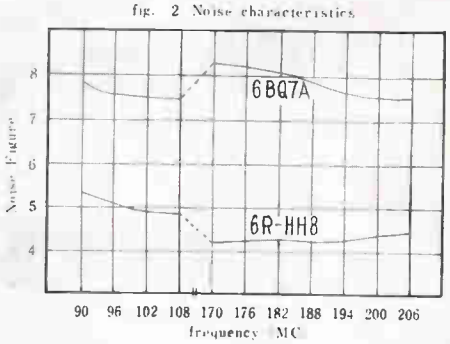


fig. 2 Noise characteristics



Hitachi also produces other receiving tubes and components for television which, when used together with the new 6R-HH8, cannot fail to earn any maker a market reputation even better than he currently enjoys.

Automatic tube testing equipment

Hitachi, Ltd.
Tokyo Japan
Cable Address: "HITACHY" TOKYO

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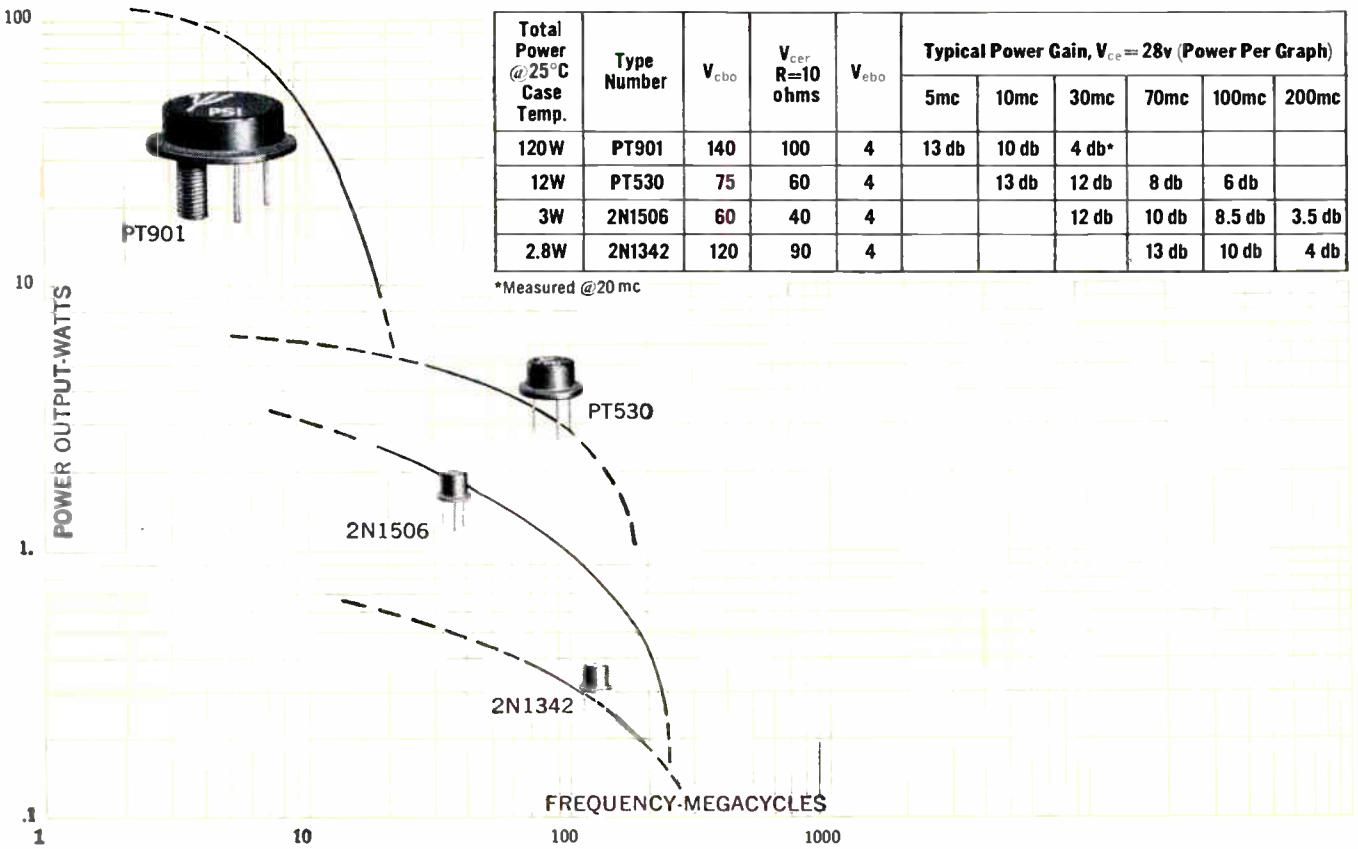
This Great New Line of Triple Diffused Silicon Mesas Provides a Transistor for Almost Every Communications Need!



Total Power @25°C Case Temp.	Type Number	V_{cbo}	V_{cer} R=10 ohms	V_{ebo}	Typical Power Gain, V_{ce} = 28v (Power Per Graph)					
					5mc	10mc	30mc	70mc	100mc	200mc
120W	PT901	140	100	4	13 db	10 db	4 db*			
12W	PT530	75	60	4		13 db	12 db	8 db	6 db	
3W	2N1506	60	40	4			12 db	10 db	8.5 db	3.5 db
2.8W	2N1342	120	90	4				13 db	10 db	4 db

*Measured @20 mc

Designers of advanced communications equipment can now take a totally new approach to engineering of high performance transmitters in power and frequency ranges never before possible.

A PT530, for example, will furnish 5 watts RF power output at 30 mc (12 db power gain) or 3 watts at 70 mc (8 db power gain). It is the only silicon transistor capable of driving the PSI type PT901 power amplifier transistor to its full 100 watts output. The new 2N1342 furnishes a substantial amount of power for the designer working in the UHF region ...200 mW RF output at 225 mc.

There are lower cost oscillator versions of the above types, too. The 2N1505 performs admirably in a circuit where you don't need the high gain characteristics of the 2N1506.

Immediate delivery is being made on evaluation quantities of types PT530 and PT901. Large quantity delivery is being made on all other PSI communications and switching transistors... including the remarkable new 2N1837 high performance switch.

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IRE People

(Continued from page 92A)

of the initial systems design for the Score, Courier and Advent satellites, and served as principal instructor for a training course in space technology at the Signal Research and Development Laboratory. Earlier, he served two years as a communications specialist with the 82nd Airborne Signal Company at Fort Bragg, N. C.

He attended City College of New York, New York, N. Y., where he majored in communications and received the bachelor of electrical engineering degree in 1950. He also received the master's degree in electrical engineering from the University of Michigan, Ann Arbor, in 1951. He has contributed a number of articles to technical journals and handbooks in the fields of astronautics and space communications.

Mr. Krassner is a member of Tau Beta Pi and Eta Kappa Nu.

❖

Philip N. Lehr (A'42–SM'48) has resigned his position as Vice President of Engineering and Research with the Dictograph Corporation of Jamaica, N. Y., as of December 31, 1960 to devote himself to management consultant work with this Corporation and for his own account.

P. N. LEHR

He has been associated with Dictograph since 1941 in various capacities: as Chief Engineer, Director of Engineering and Research, and Vice President. He has been a member of the Board of Directors of the New York Dictograph Corporation.

He holds the degree in Electrical Engineering from the University of Vienna, and the M.S. degree from the Berlin Technical University. Prior to his association with Dictograph, he had been a Chief Engineer of the French Bosch Corporation of Paris (Radio Receiver Division) and President of the Voltadyne Corporation, Paris, manufacturers of Radio Test Equipments and Signal Generators.

While with Dictograph, he conducted product developments, research and engineering for all three branches of the Corporation: the Acousticon Hearing Aid Division, the Dictograph Communications Division, and the Fire Alarm Division. He has also done consultant work for the foreign subsidiaries of the Corporation. He has personally conducted business negotiations with foreign manufacturing firms in various European countries and with U. S. government agencies.

Mr. Lehr holds twelve patents in hearing aids, telephone instruments and systems, fire alarm systems and radio communications. Several other patents are pending.

❖

(Continued on page 104A)

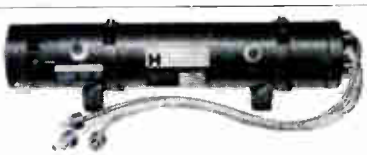
1 kw Hughes traveling wave tubes in S-Band

Now available in production quantities, these new and improved tubes offer you 1 kw of pulsed output power, with low power input, minimum heat generation and high reliability.

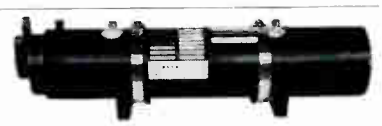
All these Hughes S-band tubes are lightweight, compact and ruggedly built to withstand the most severe environmental conditions—and provide long life. Each has been fully tested in the field.

Three of these tubes provide full octave frequency ranges of 2.0 to 4.0 kmc and you have a choice of either ½ or 1% duty, in either ungridded or gridded versions, and with gains up to 37 db. All are permanent magnet periodically focused.

311H Gridded, 1 kw minimum peak power output, 1% duty, 36 db small signal gain @ 50 mw input. Weight: 13 lbs. Length: 17-7/16". Meets usual customer requirements of MIL-E-5400, Class I environmental tests.



312H Gridded 1 kw minimum peak power output, ½% duty, 36 db small signal gain @ 50 mw input. Weight: 11 lbs. Length: 15-3/8". Meets usual customer requirements of MIL-E-5400, Class I environmental tests.



304H Ungridded, 1 kw minimum peak power output, 1% duty, 37 db small signal gain @ 1 mw input. Weight: 12½ lbs. Length: 17-31/32". Meets usual customer requirements of MIL-E-5400, Class I environmental tests.

313H Ungridded, 1 kw minimum peak power output over the center portion of the band, ½% duty, 36 db small signal gain @ 1 mw input. Weight: 17½ lbs. Length: 16-5/8". Meets usual customer requirements of MIL-E-1 environmental tests.

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IRE People

(Continued from page 102A)

George J. Laurent (A'47–SM'52) has been named executive vice-president of General Atronics Corporation, according to a recent announcement.

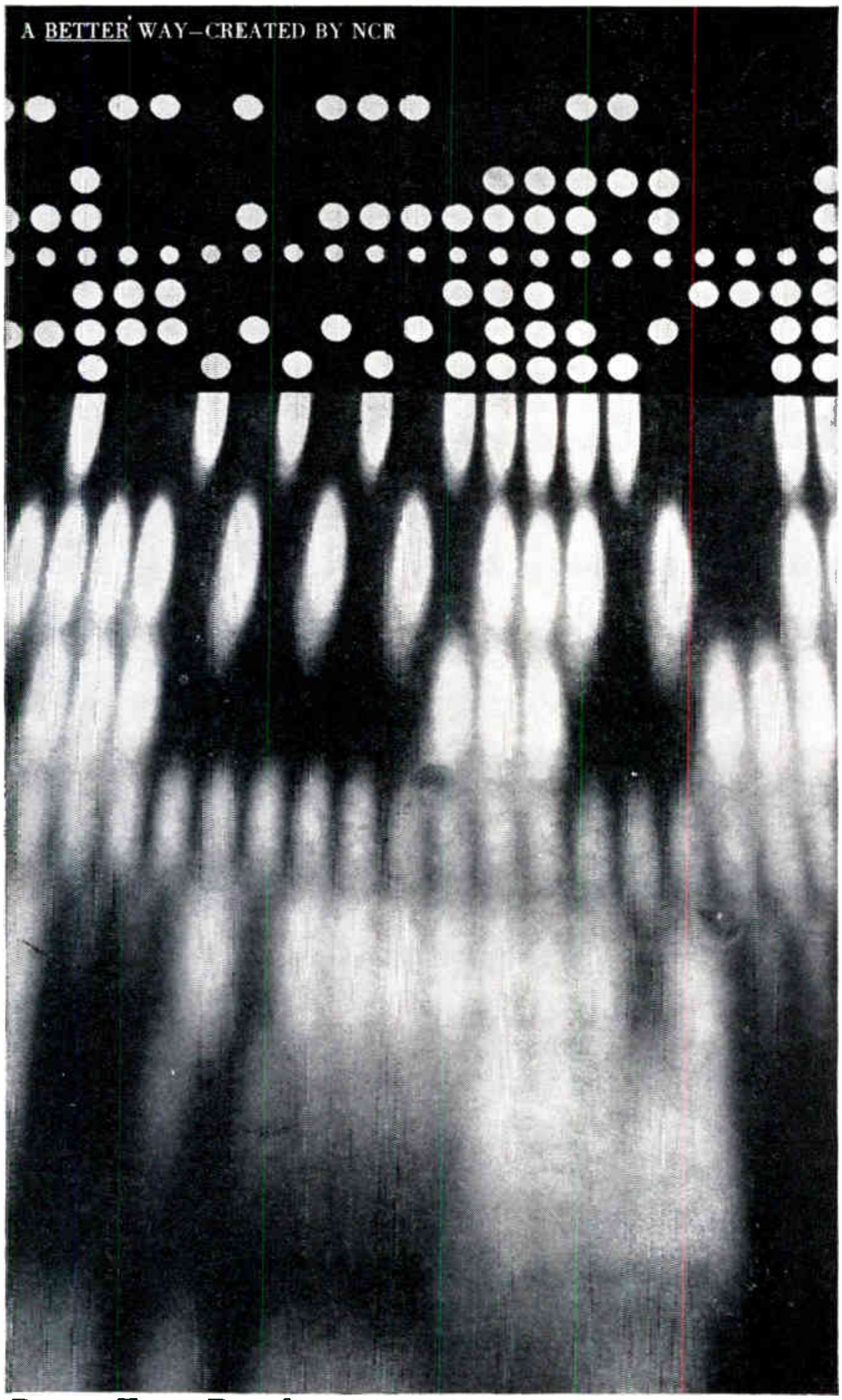
G. J. LAURENT

He has served as a Vice-President and Secretary-Treasurer of the research and consulting firm since he figured in its founding a half-decade ago, and is also president of Atronic Products, Inc., a subsidiary of General Atronics Corporation.

At Atronics, which specializes in system analysis and the development of advanced techniques in electronics, he has supervised the design and production engineering of a code recognizer, automatic checkout gear and radar control and presentation equipment.

A 1939 graduate of Massachusetts Institute of Technology, Cambridge, where he received the B.S. and M.S. degrees in Electrical Engineering, he was formerly associated with Philco Corporation, where

(Continued on page 106A)



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Seniors & Intermediates

Experienced graduate E.E.'s with 3 to 5 years in logic design and transistorized circuit design of digital equipment. Assignments will entail logic and circuit design of buffer storage units and digital peripheral equipment.

TRANSISTOR CIRCUIT ENGINEERS
Seniors & Intermediates

Highly creative positions are available in circuit analysis and design. Duties include: advanced mathematical studies in transistor circuitry, evaluation of transistor circuitry, component studies and keeping abreast of computer circuit advances. Circuit analysis ability and solid understanding of transistor theory essential. E.E. degree required.

PRODUCT ENGINEERS
Seniors & Intermediates

Assignments entail design analysis and technical liaison to develop a producible product; establishment of design requirements from a standpoint of cost, producibility and standardization; recommendation of changes for ease of manufacture. Positions require substantial knowledge of manufacturing methods, [illegible] and [illegible] solid background in electronic design of digital equipment. E.E. degree.

SYSTEMS ENGINEER

Experience required in formulating functional design specifications for digital computer systems (buffer storage, punch card, paper tape, magnetic tape, random access devices, system organizations, command structures). Training in logical design, data handling methods and programming techniques desirable. Assignment entail formulating functional specifications for business computers.

SYSTEMS TEST ENGINEERS

A responsible position entailing coordination of scheduling and utilization of both unit and systems test programs. Originate and analyze test requirements; supervise testing and analysis; recommend changes in design specification and requirements. Determine validity of test data. Requires E.E. degree plus good knowledge of [illegible] engineering, instrumentation, and design engineering.

TRANSISTOR POWER SUPPLY ENGINEER

For assignment in specifying power supplies for both large and small digital systems, supervising the design of supplies internally or by vendors, and evaluating supplies to determine conformance to specifications. Requires knowledge and design experience in solid state computer power supplies, their specification and associated transistor circuitry. Requires experienced graduate E.E. or man with formal training and [illegible] practical transistor power supply experience.

Please submit resume to [illegible] Personnel Manager

National*

The National Cash Register Company
ELECTRONICS DIVISION
[illegible]

IRE People

(Continued from page 104A)

he supervised projects in airborne radar for submarine detection and early warning and bombing systems, developed pulse to pulse filter techniques and directed statistical studies of radar return.

Mr. Laurent is a member of the Professional Group on Engineering Management.

❖

American Electronic Laboratories, Inc., has announced the appointment by the Board of Directors of a Senior Vice-President and two Vice-Presidents.

R. S. MARKOWITZ

M. NUSSBAUM

Conrad J. Fowler (S'43–A'45–SM'53) has been named Senior Vice-President, and retains his position as chairman of the Board. He is one of the original founders of AEL. **Raymond S. Markowitz** (A'51–M'58) and **Milton Nussbaum** (A'54–M'60) have been appointed Vice-Presidents.

A graduate of the Moore School of Electrical Engineering of the University of Pennsylvania, Philadelphia, Mr. Markowitz received the M.S. degree in electrical engineering in 1952. He is in charge of the Equipment Division of AEL. His group is responsible for work in UHF Communication Equipment. He participated in early development of citizens radio communication equipment, Loran, and in the development of UHF receivers for Military Airborne Television. A professional engineer registered in the state of Pennsylvania, he is a member of Sigma Tau. Prior to his joining AEL in 1953, he was engaged in research and development engineering for the Philco Corporation.

Mr. Nussbaum received the M.S. degree in electrical engineering from the Moore School of Electrical Engineering of the University of Pennsylvania in 1953. He heads the Component Division of AEL and is responsible for Microwave and Antenna System Research and Development. He has been instrumental in the development of a wide variety of antennas and antenna systems and holds patents covering antenna design. He is a member of the Professional Group on Antennas and Propagation. Mr. Nussbaum was with Remington Rand Univac prior to his joining AEL in 1952.

❖

(Continued on page 124A)

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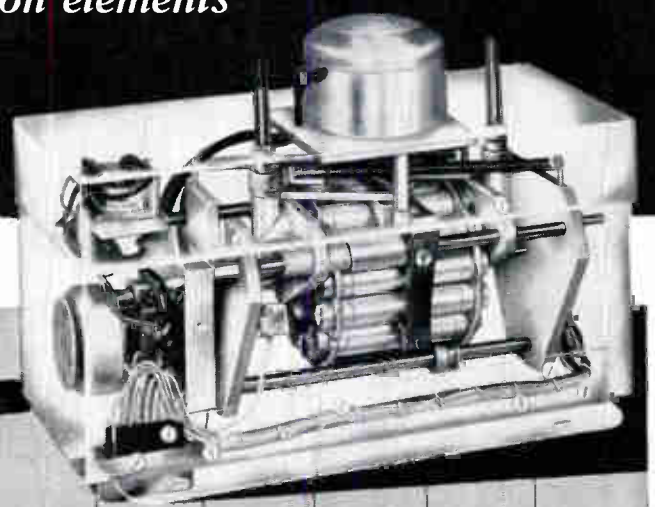

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Engineer or physicist to help with clinical applications and research associated with artificial heart-lung apparatus and development of artificial heart to replace the human heart. Advanced degree and/or experience desirable. Salary to $10,000. Large University Hospital. Send resume to Box 2036.

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Assistant or Associate Professor of E.E. M.S. or Ph.D. required. Openings in electronics and microwave theory. Beginning salary approximately $9,000-$10,000 per year depending on qualifications. Employment effected according to Civil Service regulations. Write, Head, Dept. of E.E., Institute of Technology (Air University), Wright-Patterson AF Base, Ohio.

INERTIAL SYSTEM TEST ENGINEER

Test and evaluate early prototype inertial systems. Design and develop test methods, equipment, and procedures including precision voltage analog measurements and servo, gyro, and accelerometer performance. Must have degree and applicable experience. Send resume to Mr. D. Krause, Litton Systems, Inc., 336 N. Foothill Rd., Beverly Hills, Calif.

TEST EQUIPMENT DESIGN (SYSTEM CHECKOUT)

System and circuit analysis and circuit design for automatic and manual ground-based and airborne checkout equipment. Must have degree and applicable experience. Send resume to Mr. D. Krause, Litton Systems, Inc., 336 N. Foothill Rd., Beverly Hills, Calif.

TEACHERS

Expanding graduate work in Electrical Engineering at the University of Tennessee will require the services of 2 new staff members with Ph.D. in E.E. or allied fields. A combination of teaching and research is available so that the income should be comparable with industrial salaries. Write to P. C. Cromwell, Head, E.E. Dept., University of Tennessee, Knoxville, Tenn.

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(Continued on page 114A)

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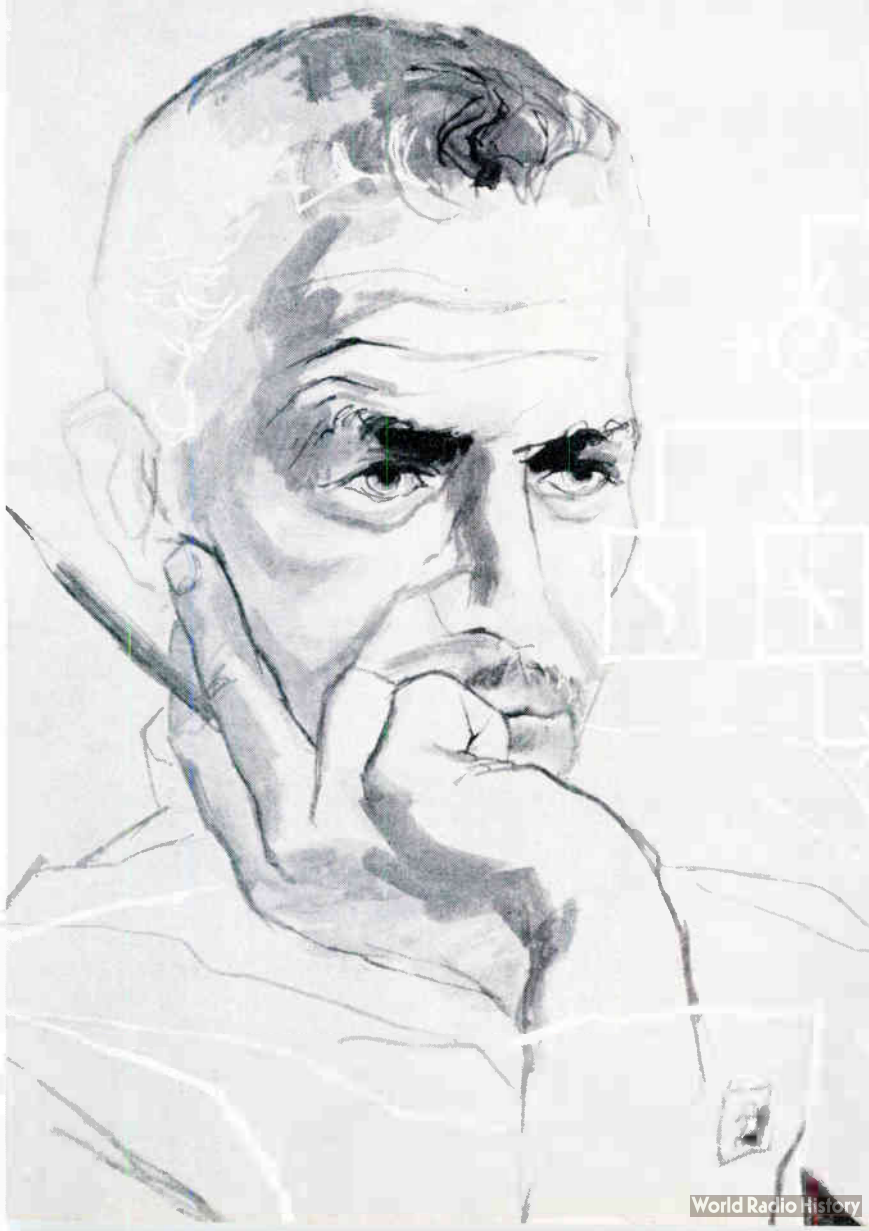

detection, space propulsion systems or related areas. Several of the positions require the ability to present contract proposals to both technical and non-technical officials. Other positions require the ability to do preliminary systems design. There are twenty-three openings in the above areas at the present time.

All of the positions involve close associations with senior engineers. All of the salaries reflect the unusual backgrounds required.

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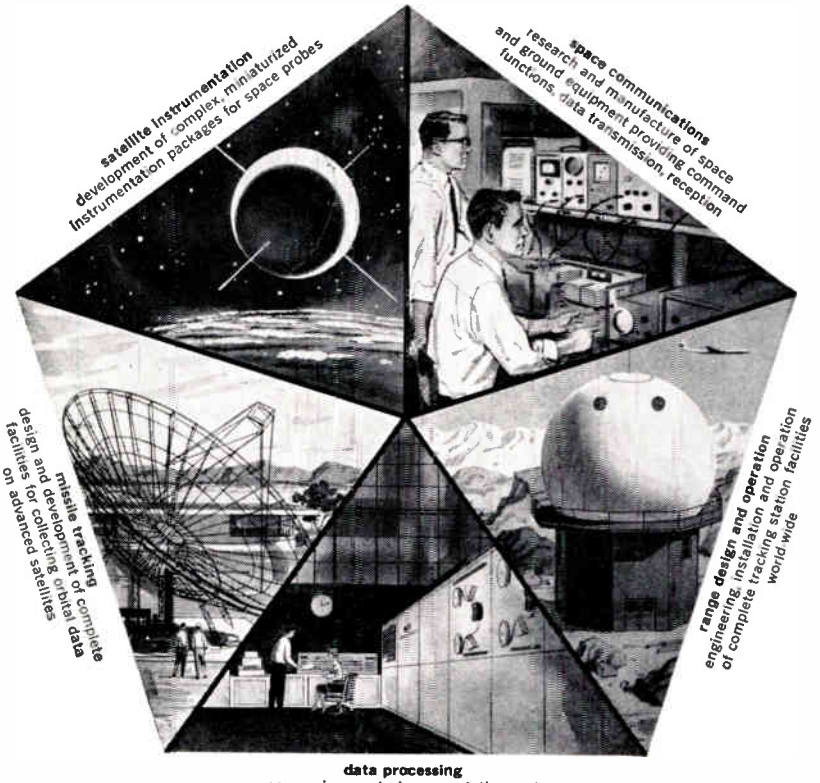

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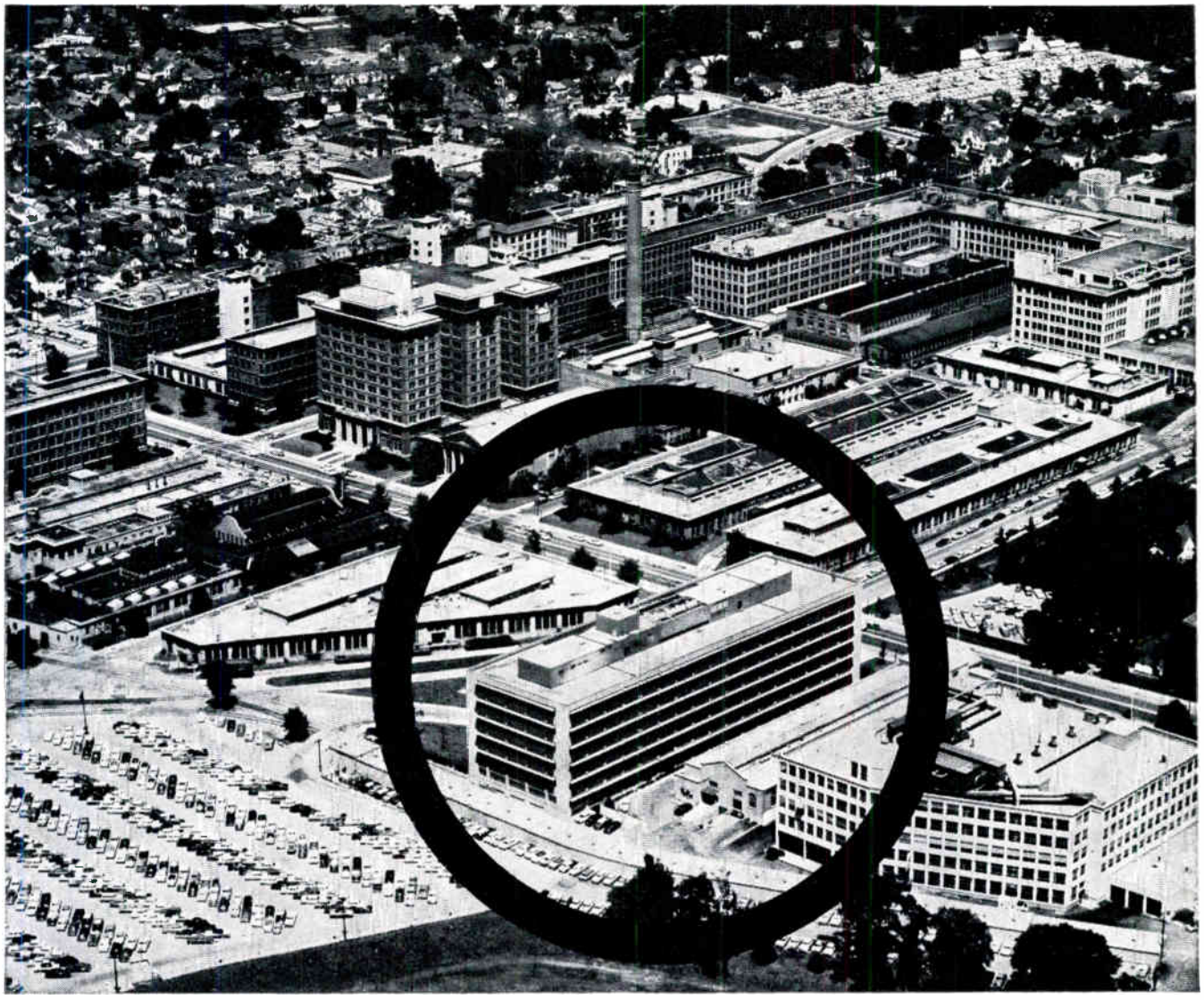


FOCUS ON RESEARCH

the first step in progress

Few, if any, organizations offer more challenging opportunity for research and new development work than The National Cash Register Company. Encompassing all sciences, the program at National's Research and Development Center at Dayton, Ohio, is built on the philosophy that Progress is limited only by man's imagination . . . that research is the first step in Progress. Perhaps your opportunity rests with us in one of the following areas:

- **ON-LINE COMPUTER SYSTEMS**
- **SEMI-CONDUCTOR RESEARCH**
- **LOGICAL and CIRCUIT DESIGN**
- **MILITARY RESEARCH & DEVELOPMENT**

Openings in the above areas of work are at an advanced level and require direct experience and an appropriate degree up to Ph.D. level.

FOR FULL CONSIDERATION, *simply send your resumé to Mr. T. F. Wade, Technical Placement Section G-2, The National Cash Register Company, Dayton 9, Ohio. All correspondence will be kept strictly confidential.*

THE NATIONAL CASH REGISTER COMPANY, DAYTON 9, OHIO

ONE OF THE WORLD'S MOST SUCCESSFUL CORPORATIONS

77 YEARS OF HELPING BUSINESS SAVE MONEY

*TRADEMARK REG. U.S. PAT. OFF.

National*

ELECTRONIC DATA PROCESSING
DIVERSIFIED CHEMICAL PRODUCTS
ADDING MACHINES • CASH REGISTERS
ACCOUNTING MACHINES • NCR PAPER

LUNAR PROBE

The moon — lacking an erosive atmosphere — may hold the key to the history of the solar system. Because of this lack of atmosphere, oceans, and wind, lunar explorations may help solve fundamental, universal questions.

Logically, the moon will be the first objective in the exploration of space. Initially the moon itself will be photographed and instrumented; then manned observation stations will be established for astronomical and meteorological purposes. In time, the moon will serve as an intermediate station enroute to other planets — step by step into infinite space.

The National Aeronautics and Space Administration's Lunar Program will utilize Lockheed's AGENA B satellite to play a significant part in forthcoming lunar explorations — as well as a host of other scientific space missions. The NASA lunar launch in 1961-62 will utilize the highly reliable Lockheed AGENA as second stage to carry the RANGER spacecraft. The AGENA will provide the extremely critical guidance and controls necessary to place the RANGER on the required lunar impact trajectory.

The lunar probe application demonstrates the versatility, reliability and success of the AGENA vehicle in Lockheed's satellite and spacecraft programs. Developed for the Air Force for use in the DISCOVERER program, the AGENA is utilized in the MIDAS missile defense alarm system and the SAMOS surveillance satellite system. Noted for a record of outstanding accomplishments, the AGENA is credited with being the first to be placed on a polar orbit; first to achieve a precise, predicted and nearly circular orbit; first to attain attitude control on orbit; first to eject a reentry capsule which was successfully recovered. The AGENA can be modified for a variety of space missions such as navigation, geophysical investigations, long-range communications and deep space probes.

Lockheed's capability in satellites and spacecraft, manifested by such an achievement as the AGENA, encompasses the entire field. It includes current and long-range programs such as interplanetary probes, global and space communication systems, and manned space travel.

Engineers and Scientists: The accomplishment of such programs offers challenging opportunities to engineers and scientists in the research, design, development, test and operation phases of these programs. If you are experienced in work related to any of the above areas, you are invited to write: Research and Development Staff, Dept. K-17, 962 W. El Camino Real, Sunnyvale, California. U.S. citizenship or existing Department of Defense industrial security clearance required.

Lockheed / **MISSILES AND SPACE DIVISION**

Systems Manager for the Navy POLARIS FBM; the Air Force AGENA Satellite in the DISCOVERER, MIDAS and SAMOS Programs

SUNNYVALE, PALO ALTO, VAN NUYS, SANTA CRUZ, SANTA MARIA, CALIFORNIA
CAPE CANAVERAL, FLORIDA • HAWAII

Positions Open

(Continued from page 108A)

uate degrees required. Address inquiries to Dr. Howard P. Hall, Dean of Faculty, Robert College, Bebek Post Box 8, Istanbul, Turkey with copy to Near East College Assoc., 548 Fifth Ave., New York 36, N. Y.

RESEARCH PROFESSOR

Electronics engineer with B.S. or M.S. degree plus radar design experience to conduct research in weather radar. Salary dependent on qualifications and experience. Contact H. W. Hiser, Head, Radar Meteorological Research, Marine Lab., University of Miami, Coral Gables, Florida.

MICROWAVE SPECIALIST

A Microwave physicist is needed for applying microwave techniques to the study of plasma flows and ionized regions around high speed models and in shock tubes. Measurements and study of the radio-frequency energy emitted by the passage of high-speed models and of the transmission and reflection characteristics of the wake are required in order to evaluate the effects of these characteristics and also as an aid to further the knowledge of flow phenomena at extreme speeds. Applicant should have advanced degree with a good background in microwave propagation and field theory as well as ability to work with microwave hardware. He should be capable of taking the initiative in the application of microwave techniques and in the interpretation of results. Write Personnel Officer, NASA, Ames Research Center, Moffett Field, California.

TEACHING—ELECTRICAL ENGINEERING

Teaching in Electrical Engineering. Background in power distribution, rotating machinery, and/or automatic control theory. General undergraduate E.E. program. Prefer M.S. or B.S. with experience. Appointment effective February 1961. Address: Head, Electrical Engineering Dept., College of the Pacific, Stockton, Calif.

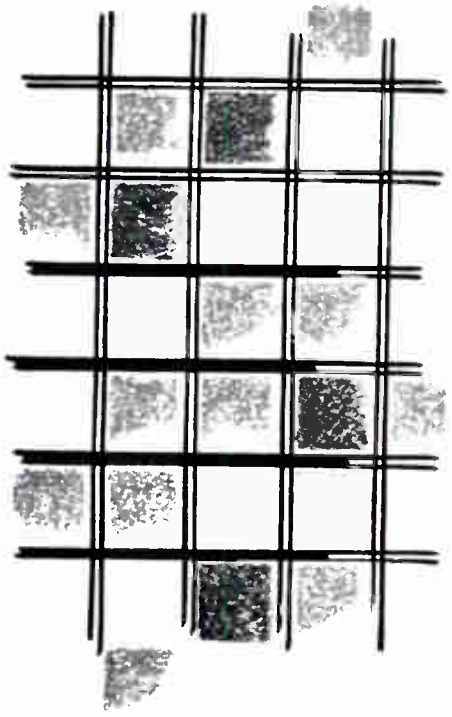
ASSISTANT DIRECTORS & SENIOR SCIENTIFIC OFFICERS

A growing Institute, the national laboratory in India for electronics, has 4 senior research positions open, with opportunities to lead research and development groups in the fields of vacuum tubes, electronic instrumentation, communications and solid state devices. A Ph.D. degree or M.S. with experience in industrial research is required. Attractive housing and good educational facilities for children are also available. Apply Amarjit Singh, Assist Director-in-Charge, Central Electronics Engineering Research Institute, Pilani (Rajasthan) India.

ENGINEERS & TEACHERS

The University of Denver's College of Engineering and Research Institute are seeking electronic engineers and physicists with Ph.D. or D.Sc. degrees for research and teaching positions in the areas of electromagnetic wave propagation, antenna research, thin film and solid state electronics, circuit development, servomechanisms and infrared techniques. Also available are overseas field engineering assignments in Japan, Australia, South America and South Africa for periods of 1 to 2 years. Address inquiries to C. A. Hedberg, Head, Electronics Div., Denver Research Institute, University of Denver, Denver 10, Colo.

(Continued on page 116A)



If your field is data processing and your ambition is to *advance*, your most promising opportunities are with RCA Moorestown, New Jersey. Here, in an ultra-modern, self-contained facility near a pleasant suburban community, a group of creative engineers and scientists are assigned to solving problems connected with advanced defense projects such as BMEWS (Ballistic Missile Early Warning System), DAMP (Downrange Anti-ballistic-missile Measurements Program), and TRADEX (Target Resolution And Discrimination Experiments). Your starting salary is based on your achievements; professional benefits are exceptional. At this time, openings exist for the following:

SYSTEMS PROGRAM-ANALYSTS—Openings for individuals who can make a real contribution to satellite tracking and space surveillance. Problems include development, optimization, and analysis of real-time computer programming systems for long-range radar/computer system applications. Six to nine years' experience is required.

NUMERICAL ANALYSTS—To contribute creative approaches to such problem areas as numerical methods in differential equations; orthogonal functions and curve fitting; and analysis of special functions (elliptic integrals, auto- and cross-correlations).

ANALYST-PROGRAMMERS—Must have the ability to do creative thinking in the programming of real-time and general mathematical problems for large scale weapon systems. Experience in developing interpretive systems, symbolic assemblies, logical programming, algebraic translators, and problem-oriented and machine-oriented languages is highly desirable. Experience in general scientific data processing systems on large-scale computers and a background in mathematics are necessary.

RCA Moorestown offers variety and opportunity to scientific data processing specialists

Address inquiries to:

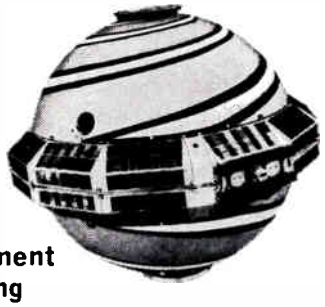
Mr. W. J. Henry, Box V-17A
RCA, Moorestown, New Jersey
(20 minutes from Philadelphia)

EQUAL JOB OPPORTUNITY For All Qualified Applicants

RADIO CORPORATION of AMERICA
Moorestown Missile and Surface Radar Division

Electronic Engineers

for assignments on APL's satellite program



Research • Development
Systems Engineering

You will find association with APL particularly rewarding if you appreciate an atmosphere conducive to original thinking, and if you are capable of making contributions to advance the state-of-the-art.

Satellite Development Group

The group is concerned with research and development of satellite-borne equipment, which will be capable of performing highly complex functions. The instruments have to operate in a space environment on exceedingly low power sources, and they have to work for five to ten years without malfunction.

Emphasis is on conceptual design rather than hardware fabrication. Engineers will work without close supervision, will enjoy freedom to create and investigate, and do not have to spend much time writing proposals. BS or more in physics or electronic engineering required. Two or more years of experience in transistor switching circuits and familiarity with utilization of memory and/or logical devices desired.

Satellite Ground Systems Group

This group is responsible for the design of data handling systems for use in shipboard and airborne navigational equipment, and for ground tracking equipment. Assignments involve development of novel and highly sophisticated data processing systems, systems coordination, and technical supervision of contractors.

BS or more in physics or electronic engineering plus four to five years of experience in data processing systems required.

For details about these career opportunities, address your inquiry to:
Professional Staff Appointments

The Applied Physics Laboratory
The Johns Hopkins University

8603 Georgia Avenue, Silver Spring, Md.
(Suburb of Washington, D. C.)

Positions Open

(Continued from page 114A)

ELECTRONIC ENGINEERS AND PHYSICISTS

An expanding R&D laboratory has openings for qualified engineers and physicists to participate in and direct research and development programs in the microwave tube area. This is an opportunity for competent individuals who are interested in the direction of R&D programs at the leading laboratories in the country as well as participating in microwave in-house research. Salary from $7560 to $12,210, depending on experience and training. Send complete resume to Box 2038.

ENGINEERS

Expanding opportunities for research and graduate instruction at master's and doctor's level. Steady growth has created a need for highly qualified persons with a doctor's degree and a background of research and teaching in one of the following fields: mechanical dynamics; metallurgy; thermodynamics; applied physics; mathematics (statistics and operations research); electrical engineering (electronics and control). Contact Dean of the Hartford Graduate Center, Rensselaer Polytechnic Institute, East Windsor Hill, Conn.

ENGINEER OR PHYSICIST

Engineer or physicist to head Electronics Dept. of large bio-medical research institute in New York City. Knowledge of radiation physics detectors and circuits essential. Job involves design of new instruments and supervising maintenance. Send complete resume to Box 2040.

SENIOR ENGINEER

TO HEAD DEPARTMENT
IN FIELD OF
Electrical Filters & Networks

Requires sound background in filter design and associated components and techniques from DC to 100 MC. Knowledge of modern network synthesis desired.

Other Senior Engineers For

- **TRANSISTOR CIRCUIT DESIGN**
- **TRANSMITTER & RECEIVER DESIGN**
- **SINGLE SIDEBAND COMMUNICATION**
- **MECHANICAL DESIGN**

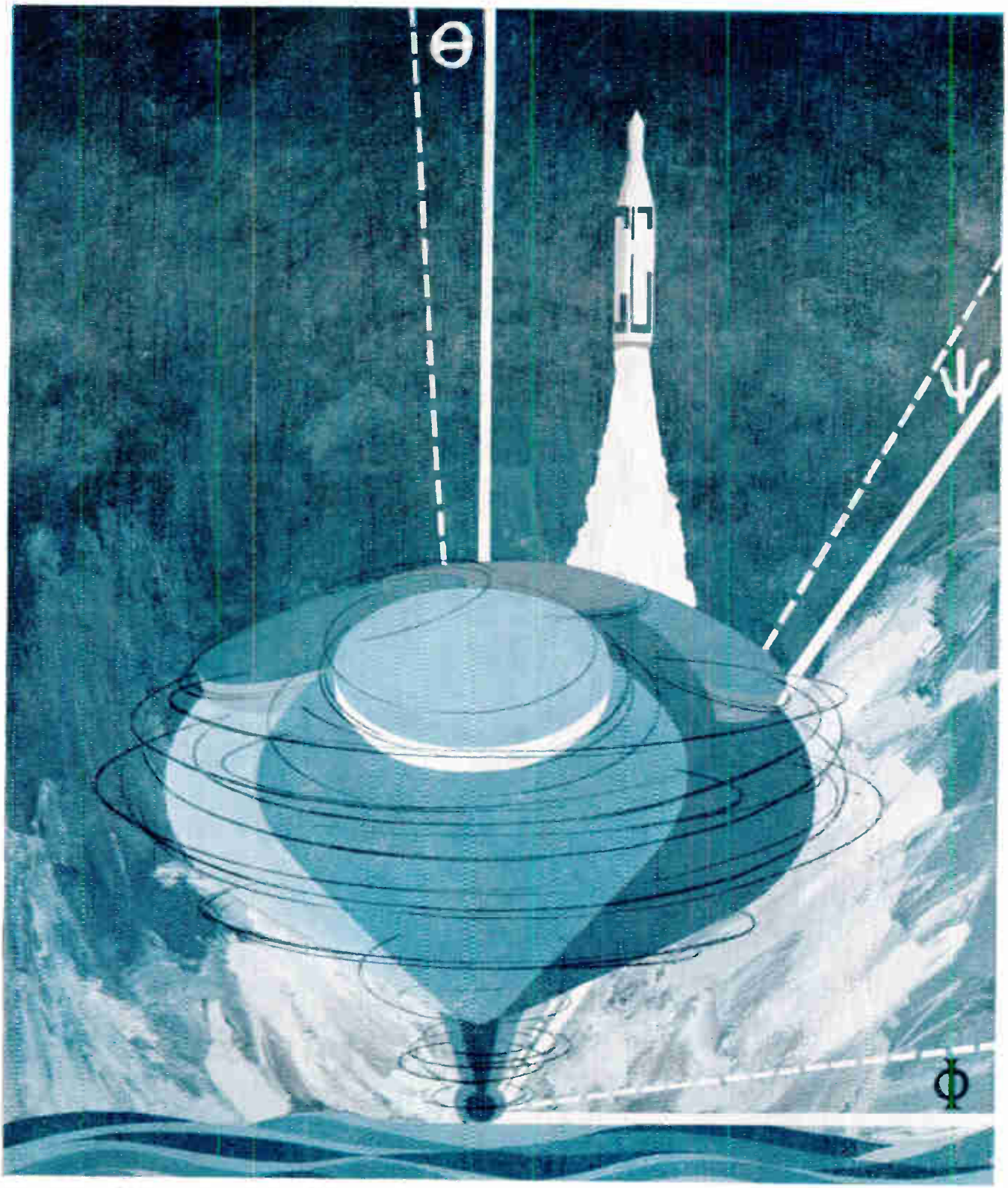
These are excellent opportunities for creative engineers to become part of a financially sound, reputable company established 28 years in the electronics industry. Advantages include excellent salary and individual recognition of achievements and contributions.

Mail Resume To

MR. B. MATOSSIAN,
Chief Engineer

Barker & Williamson, Inc.

BRISTOL, PA.

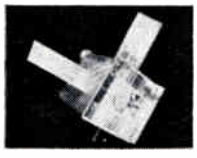


SORRY, HERR PROFESSOR EULER, BUT WE HAVE OUR OWN ANGLE!

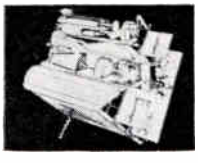
Your angles are necessary when dealing with large rotations, but the mathematics is complicated. However, our single degree of freedom gyros and tight gimbal servo loops result in very small angles of rotation. Thus, we avoid heavy mathematics and also improve guidance system performance. This approach has paid off in our Thor, Mace and Titan guidance systems. If you can understand complex physical laws but know how to work around them, and have a BS, MS or PhD in Physics, ME, EE, or Math, please contact Mr. D. B. Allen, Director of Scientific and Professional Employment, 7929 S. Howell, Milwaukee 1, Wisconsin.

AC SPARK PLUG ⚛ THE ELECTRONICS DIVISION OF GENERAL MOTORS

An invitation for Physicists and Engineers to work on Research and Development at the M.I.T. Instrumentation Laboratory . . .



The Laboratory, with its staff of 1,000 employees, is primarily engaged in the conception and perfection of completely automatic control systems necessary for the flight and guidance of missiles and space vehicles. Many "firsts" in these fields have been developed at the Laboratory.



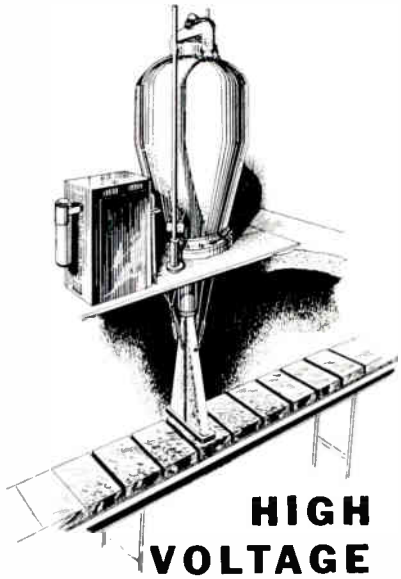
R and D opportunities exist in: • ANALYSIS OF SYSTEMS AND COMPONENTS • ASTRONAUTICS • HIGH PERFORMANCE SERVOMECHANISMS • POWER SUPPLIES & MAGNETIC AMPLIFIERS • DIGITAL & ANALOG COMPUTERS • ELECTRO-MECHANICAL COMPONENTS • TRANSISTOR CIRCUITRY & PULSE CIRCUITRY • RESEARCH, DESIGN & EVALUATION OF GYROSCOPIC INSTRUMENTS • COMPUTER PROGRAMMING & SIMULATOR STUDIES • LOGICAL DESIGN • AND IN MANY OTHER AREAS

CALL or WRITE:
DR. C. S. DRAPER, Director

INSTRUMENTATION LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

68 Albany Street, Bldg. I-A
Cambridge 39, Massachusetts
UNiversity 4-6900, Ext. 3544

- Graduate courses may be taken for credit while earning full pay
- U. S. Citizenship required



HIGH VOLTAGE ENGINEERING CORPORATION

the largest designer and manufacturer of high energy particle accelerators, serving the physical sciences, radio-therapy and industry throughout the world.

Our unprecedented expansion enables us to offer several challenging positions with excellent growth potential.

SENIOR PHYSICIST

Highly responsible position requiring advanced degree and good theoretical and experimental background in the semi-conductor devices field. Project involves development of novel methods of solar cells fabrication.

ELECTRICAL ENGINEER

To work on high voltage transformer design and manufacturing problems and high voltage power supply design. EE degree and 5 years' experience preferred.

ELECTRONIC ENGINEERS

To design and develop basic electronic amplifier and stabilization systems, and to design, develop and test electronic stabilizers, magnetic field measuring devices and control systems. Good basic knowledge of electronic circuit theory required.

PHYSICISTS

Several openings for junior and intermediate physicists with BS degree and 1 to 3 years' experience to work in the fields of ion propulsion, colloids, or general engineering and applications work.

Send resume in confidence to:
Mr. Gordon R. Hamilton, Jr.
Personnel Director

HIGH VOLTAGE ENGINEERING CORP.
BURLINGTON, MASSACHUSETTS

Positions Wanted

By Armed Forces Veterans

In order to give a reasonably equal opportunity to all applicants and to avoid overcrowding of the corresponding column, the following rules have been adopted:

The IRE publishes free of charge notices of positions wanted by IRE members who are now in the Service or have received an honorable discharge. Such notices should not have more than five lines. They may be inserted only after a lapse of one month or more following a previous insertion and the maximum number of insertions is three per year. The IRE necessarily reserves the right to decline any announcement without assignment of reason.

Address replies to box number indicated, c/o IRE, 1 East 79th St., New York 21, N.Y.

TEACHING

Ph.D. Engineer-Physicist; age 38; Member IRE; American Phys. Society. Experience: 16 years teaching, research, industry, including supervisory. Publications. Specialty microwaves and devices (PGMTT, PGED). Seeks full professorship or chairmanship in reputable, growing E.E. Dept. Box 3001 W.

ELECTRONIC ENGINEER

MEE. Seeks affiliation with, or will organize planning staff for technical-economic evaluation of new ideas, products and acquisitions in the electronic and electromechanical fields. 15 years diversified experience R&D, studies, project engineering, proposals and presentations, planning and requirements. Top references. Box 3002 W.

ELECTRONIC ENGINEERS

Electronic Engineer 1943 B.S. Extensive laboratory and supervisory experience in R&D and applications of electron tubes and solid-state devices in military and industrial equipment. Desires responsible technical position in Australia, preferably with American affiliated company. Box 3003 W.

TEACHING

Industrial, technical, or vocational teaching of radio, TV, and Industrial Electronics. B.S. in Television Engineering. Anywhere in the U.S. Age 40. Box 3004 W. 10 years experience.

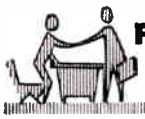
MARKETING/PRODUCT PLANNING

Data Communication Systems. Regional sales and field engineering manager, military and commercial accounts. Standard and special systems using wire line, radio and microwave transmission. Also experience in computer and special purpose EDP systems sales, advertising and sales promotion. BSEE. Age 37. 13 years experience. Box 3007 W.

ELECTRONICS SALES EXECUTIVE

South or Central America desired, as representative for electronics component or system manufacturing. BSEE, 10 years applied experience from Semi-conductors to Systems. Demonstrated managerial ability. Fluent in Spanish and other languages. Married and family. Previous overseas engineering experience. Member of IRE, age 37. Box 3008 W.

(Continued on page 122A)



Positions Wanted

By Armed Forces Veterans

(Continued from page 120A)

ELECTRONICS ENGINEER

BEE, MSEE, 1st Lt. Army Ordnance. INDUSTRIAL EXPERIENCE: 17 months as research engineer, military communication systems, programming digital computers. MILITARY EXPERIENCE: 2¾ years to include two new missile systems as technical and project officer. Available April 1961. Box 3009 W.

ENGINEERING EXECUTIVE

15 years experience in directing engineering departments in field of entertainment electronics, with additional background in manufacturing, purchasing, finance, and general management. Expert in handling growing pains of small company in $2,000,000-$5,000,000 yearly gross sales category. Age 40. Will consider participation. Box 3010 W.

ENGINEERING TECHNICIAN

Graduate of American Television Institute of Technology, with B.S. in Television Engineering. Married, age 37. 10 years experience in Radio and TV Broadcast Engineering. Wants position with up and coming firm that is going places with opportunity for further study and advancement desirable. Box 3011 W.

MANUFACTURERS' REPRESENTATIVE

California Experience. Now in New York area planning April 1961 return to West coast. Interested in interviewing companies anxious for better representation and more sales. If not near New York suggest we meet during IRE Show, but please write now. Box 3015 W.

ENGINEERING TECHNICIAN

6 years experience in Military communications systems, and miniature audio systems. Will graduate from RCA Institutes (advanced electronics course) in February of 1961. Some college background. Age 28; married. Box 3016 W.

ELECTRICAL ENGINEER

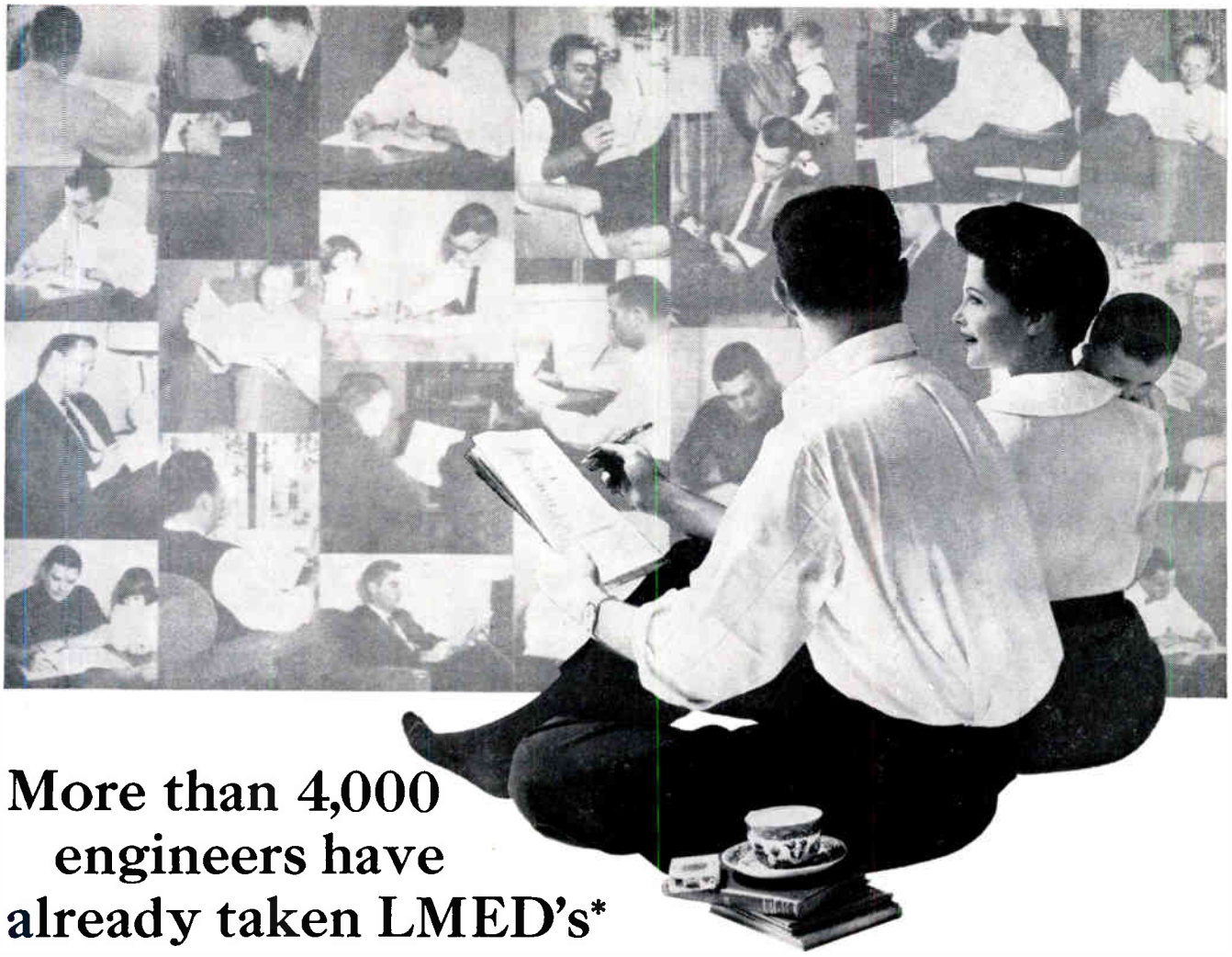
Seeking management position. Nearly 10 years of successful experience in planning, organizing, and administering of various phases of projects in the development of electro-mechanical products from specifications through prototype and final test. Box 3017 W.

CONSULTING ENGINEER

BSEE, 1958, EIT certificate 1958. 2 years technical publications experience with technical and managerial training at the graduate level. 1 year Naval electronic school and 1 year as a Naval electronics technician. Other electrical utility and heavy steel mill control experience. Member IRE, Associate Member AIEE. Age 27. Desires association with an architectural and engineering firm. Box 3018 W.

TRANSFORMER DESIGNER

9 years experience in design, production, test and tooling for a wide variety of small transformers. Particular emphasis on design for epoxy encapsulation and on design of Hi Q reactors and low level multi shielded units. Box 3019 W.



More than 4,000 engineers have already taken LMED's* self-appraising technical tests! *Have you?*

Whether you're thinking about a change, or simply interested in finding out how you stack up against other engineers in your field, LMED's Technical Tests will give you a sound means for appraising your abilities—right in your own home.

Carefully designed and pre-tested by LMED engineers, these technical quizzes are meant to be taken and scored for your self-appraisal only. The results need never be divulged to anyone—including Light Military.

Individual tests are available for the fields of Radar, Microwave, Communications, Electronic Packaging (ME), and Engineering Administration (a self-scoring psychological questionnaire).

Just check your fields of interest below, and we'll send you the corresponding tests, answer sheets and evaluation guides. They'll give you an objective basis for determining the probabilities of your success at Light Military—*before you even consider making application.*

MAIL THIS COUPON FOR YOUR TESTS

Current Areas of Activity At The Light Military Department

Space Communications & Telemetry • Missile & Satellite Computers • Space Vehicle Guidance • Undersea Warfare Systems • Thermoplastic Data Storage • Space Detection & Surveillance • Command Guidance & Instrumentation • Infrared Missile Applications.

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53-MA

Mr. R. Bach
Light Military Electronics Dept.
General Electric Company, French Road, Utica, New York

Please send me tests (limited to 2 subjects per individual) answer and self-evaluation sheets covering the areas checked:

☐ RADAR ☐ MICROWAVE
☐ ELECTRONIC PACKAGING (ME)
☐ COMMUNICATIONS ☐ ADMINISTRATIVE ENGINEERING

Name_____

Home Address_____

City_____ Zone_____ State_____

Home Phone_____

Degree(s)_____ Year(s) Received_____

IRE People

(Continued from page 106A)

The election of **Dr. John L. McLucas** (S'50–A'51–SM'52) to the Board of Directors of Astro-Science Corporation, Los Angeles, Calif., was recently announced.

J. L. McLucas

He is President of HRB-Singer, Inc., State College, Pa., a subsidiary of The Singer Manufacturing Company. HRB-Singer is an electronics research and development firm.

Dr. McLucas, who received the Ph.D. degree in physics and electrical engineering from Pennsylvania State University, University Park, and the Master's degree in physics and mathematics from Tulane University of Louisiana, New Orleans, is a member of the Young Presidents' Organization, Institute of Aeronautical Sciences, Operations Research Society, American Institute of Physics, American Rocket Society and other professional organizations. He has published numerous scientific and technical papers in the professional literature.

❖

Warren P. Mason (A'36–VA'39–F'41) of the Applied Mechanics Research Department, Bell Telephone Laboratories, Murray Hill, N. J., recently applied for a patent on his 200th invention. This gives Dr. Mason more inventions to his credit than any other employee in the history of Bell Laboratories.

W. P. Mason

His latest invention is a semiconductor strain gauge which has applications to military and peacetime uses.

During his 39 years with the Laboratories, he has seen 170 of his inventions receive U. S. Patents. They have been in the fields of crystals, ultrasonics, radar and sonar, and mechanical properties of solids.

He has also written three books and 150 papers for professional journals. He is a graduate of the University of Kansas, Lawrence, and holds the Ph.D. degree in physics from Columbia University, New York, N. Y.

Some of his specific inventions include a silencer for pistols, a directional microphone for use in broadcasting, and several crystals and crystal filters used in carrier, submarine cable and radio systems.

❖

(Continued on page 129A)

Why don't you Talk with Westinghouse about Your Environment!

Westinghouse-Baltimore has created an environment favorable to engineering growth and development. Here, the research and development programs, both under contract and company sponsored, can call on the finest of facilities—all company owned—to give the engineering teams freedom to pursue the most advanced electronic projects. There are abundant opportunities for professional growth, including the Westinghouse program for assistance in the pursuit of graduate degrees through The Johns Hopkins University and The University of Maryland.

Westinghouse-Baltimore is ideally located in the suburbs between Baltimore and Washington . . . the heart of the Chesapeake Bay country . . . famous for fine housing, good schools and pleasant living.

Before you make any career decision, why don't you talk with Westinghouse about the challenging opportunities available with this "engineer's company".

Current openings include:

Communication Systems
Digital Techniques
Solid State Systems
Microwave Theory
Systems Engineering Analysis
Transistor Circuit Design
Radiating Systems Design

Send resume to: Mr. J. F. Caldwell, Dept. 364

Westinghouse

BALTIMORE

P.O. BOX 746 Baltimore 3, Maryland

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Bausch & Lomb

A firmly established giant in the optical industry, this upstate New York corporation is rapidly expanding in electronic-mechanical systems work. Emphasis lies in commercial analytical and scientific instrumentation with a healthy balance of research and development contracts for military programs. Look into these professional opportunities with Bausch & Lomb Incorporated.

- SECTION HEAD IN ELECTRICAL ENGINEERING— B.S. and E.E. with M.S. desired. Five or more years experience in circuit design, controls, servos, and feedback systems. Must be familiar with analysis, synthesis and a wide range of components for control systems, displays, etc. Will lead the Electronic Design Section in the Military Products Division. Will integrate the electronics activity with optical and mechanical engineering groups. Technical consultant in electronics. Also openings for several project engineers in the above area.
- ELECTRICAL ENGINEER— B.S. and E.E. with three or more years broad experience in circuit design. Instrument experience valuable but not required. Will be responsible for electrical engineering design of scientific instruments. Must be capable of independent design work.
- LIVE IN ROCHESTER
  Rochester is located in the heart of the upstate New York vacation country and is noted for its beautiful homes and gardens, fine schools and University, outstanding cultural advantages and high ratio of professional residents.
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14 Bausch Street • Rochester 2, New York

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WAVE PROPAGATION • RADAR SYSTEMS

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- *Science Education Program leading to advanced degrees*
- *Excellent facilities and equipment, and atmosphere conducive to high levels of research*
- *Liberal leave and retirement system, and greater job security through competitive Civil Service program of benefits*

There is an unmistakable degree of professional pride evident when a scientist or engineer says, "I am a part of the Naval Research Laboratory." To become a part of NRL requires a considerable degree of competence, of course. To learn how you may qualify for the many excellent job opportunities at NRL, please write to the Personnel Officer.

NRL

U. S. Naval Research Laboratory
WASHINGTON 25, D.C.

Research Engineers

Immediate Openings for Specialists to staff a new Research Function of

Lenkurt
Electric Company, Inc.

(A Subsidiary of General Telephone and Electronics)

Areas of Immediate Interest are listed below for your consideration:

- TELEPHONE and DATA CARRIER MULTIPLEXING SYSTEMS —600 channels and higher
- PASSIVE and ACTIVE FILTER NETWORKS for Communication purposes.
- MODULATION METHODS AM, FM, PCM, and PPM, etc.
- PROPAGATION STUDIES AND METHODS in cable open wire G line, microwave and optical spectrum.
- MICROWAVE, SOLID STATE, GENERATOR DETECTORS, RELAYS for GROUND and SATELLITE COMMUNICATION.
- THEORETICAL STUDIES for large "Hypothetical" Communication Systems.

LABORATORIES are located in Central California on the beautiful San Francisco Peninsula . . . 30 minutes south of San Francisco —and only minutes from Stanford University Campus.

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Address all inquiries to:
Dr. Vladimar Vodicka,
Director of Advanced Development Laboratories

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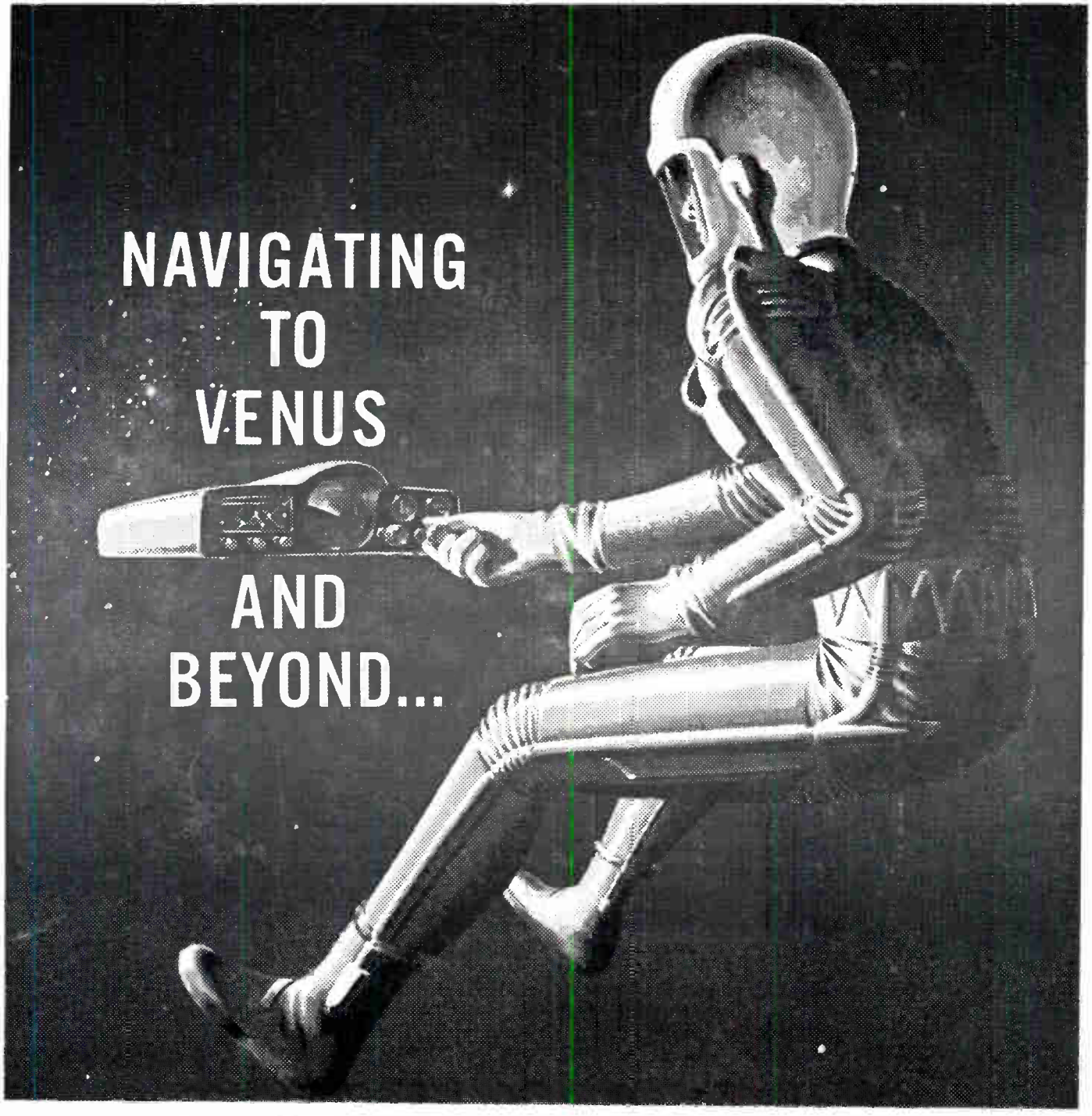
ELECTRIC CO., INC.
San Carlos, California
a subsidiary of General Telephone & Electronics



A CHALLENGE TO EXCITE ANY ELECTRONICS ENGINEER WORTH HIS SALT...THE KIND RYAN NEEDS RIGHT NOW

We do not know where Venus is, within 50,000 miles or more. What is needed is a guidance system capable of injecting space vehicles into interplanetary orbits with the accuracy required for advanced space missions.

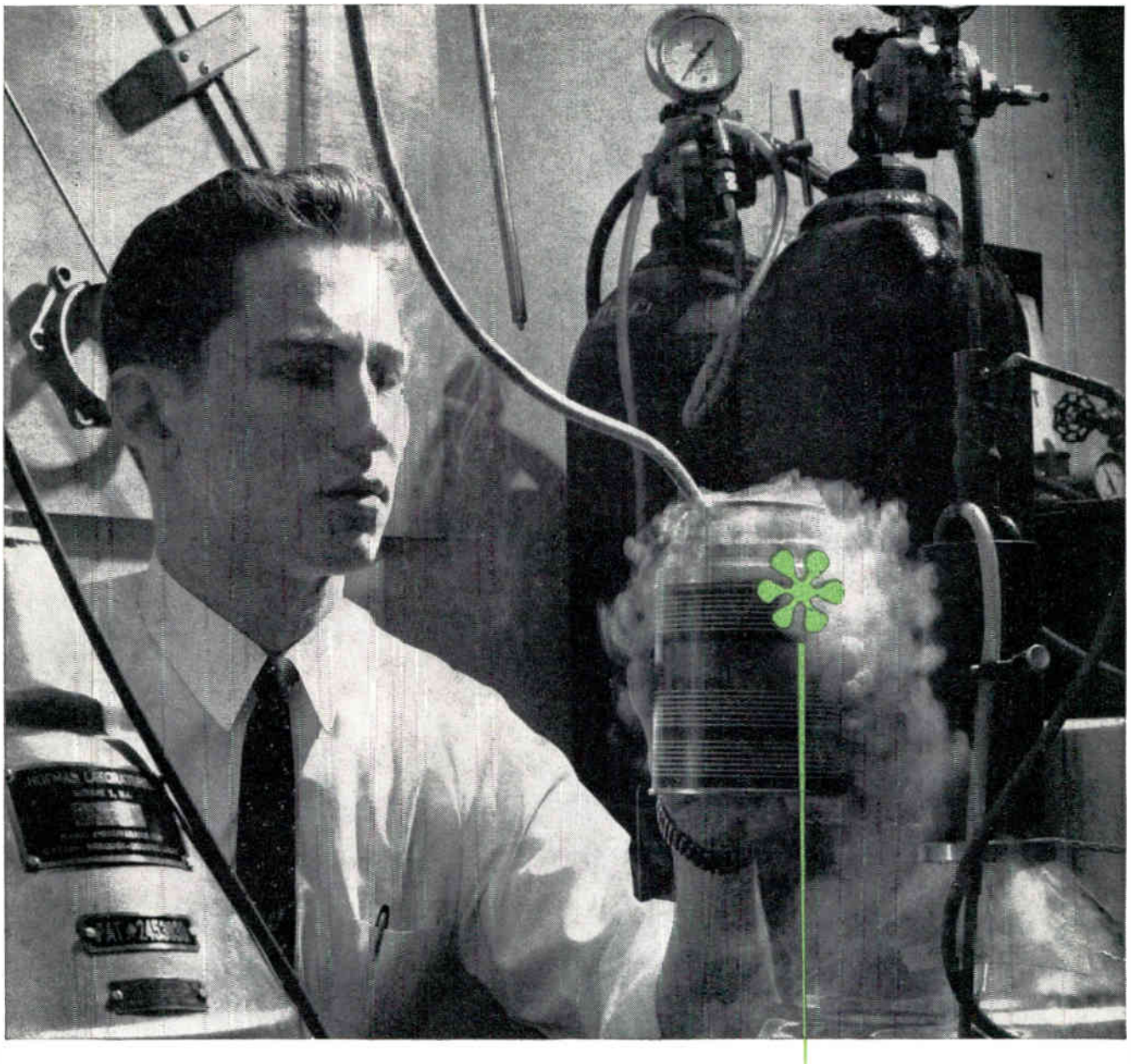
We are confident that the C-W doppler systems, of which Ryan is the world leader, will meet this challenge of space navigation. This is one reason Ryan is the largest electronics firm in San Diego—*and the fastest growing!* If you are an electronics engineer ambitious to help advance the art, as well as your own career, through vital "frontier work"—we want you *right now* at Ryan Electronics.

Ryan Electronics employs over 2000 people and has over one-third of the company's $149-million backlog of business. Under the leadership of some of America's most prominent scientists and engineers, Ryan is probing beyond the known . . . seeking solutions to vital problems of space navigation.

Expanding facilities of Ryan Electronics at San Diego and Torrance in Southern California are among the most modern in the West. You enjoy living that's envied everywhere, plus facilities for advanced study. Send your resume or write for brochure today: Ryan Electronics, Dept. 1, 5650 Kearny Mesa Road, San Diego 11, Calif.

DIVISION OF RYAN AERONAUTICAL COMPANY
SAN DIEGO & TORRANCE · CALIFORNIA

RYAN ELECTRONICS



In Martin Cryogenics Laboratory, liquid nitrogen in Dewar flask produces -196°C for low-temperature tests of vacuum deposited specimen.

ELECTRONIC ENGINEERS AND SCIENTISTS

Cold facts about professional accomplishment!

It is professional accomplishment that matters *most* to the confident and capable engineer or scientist.

He welcomes the challenge of exploring new concepts with a rapidly expanding company that is leading the way in missile / space technology. This is why so many outstanding engineers and scientists are joining the Martin-Baltimore engineering-production team. They see the opportunity for significant accomplishment in their chosen fields. They want to share importantly in the rewarding future that is being created *today* at Martin's. They know that at Martin's the exceptional engineer or scientist is assured exceptional advancement.

Our expanding programs have created openings for:

PROJECT SUPERVISORS
SR. DESIGN ENGINEERS

For assignments in these fields:

RADAR . . SONAR . . . RELIABILITY ANALYSIS . . TEST EQUIPMENT DESIGN . . INFRARED . . CIRCUIT DESIGN . . . ACOUSTICS . . INSTRUMENTATION . . SOLID STATE PHYSICS . . . GUIDANCE & NAVIGATION SYSTEMS . . TRANSISTOR CIRCUITRY . . COMMUNICATIONS . . . OPTICS . . . HUMAN FACTORS

WRITE
giving brief outline of your education and experience to:
MR. J. W. PERRY
Professional Employment, Dept. 10

MARTIN
BALTIMORE 3, MD.

IRE People

(Continued from page 124A)

Raymond Minichiello (M'59) has been appointed manager of mobile communications product planning for General Electric's Communication Products Department, Lynchburg, Va.

R. MINICHIELLO

In his new position, he will have responsibility for product development guidance on vehicular two-way radios, portable transceivers, pocket units and associated systems devices.

He has specialized in electronics and communications for the General Electric Company for the past 19 years. Most recently, he has been district communications sales manager for the company at Wellesley, Mass., where he handled systems engineering on a number of major communication projects.

He joined General Electric in 1941 at West Lynn, Mass., in the Aircraft Instrument Dept., where he worked on electronic totalizing systems. During 1945 and 1946, he was an instructor in communications at the Navy radio school at Gulfport, Miss.

(Continued on page 130A)

IRE People

(Continued from page 129A)

In December of 1948, he transferred to the G-E Aircraft and Ordnance Department, engineering guidance and control devices on Project Hermes at White Sands. In October, 1954, he became a member of the sales organization of the G-E Aircraft and Accessory Department at Lynn, Mass.

In February, 1956, he was appointed communications engineer for the G-E Communication Products Department's regional office at Wellesley, Mass. He was named district sales manager there in January, 1958.

A Registered Professional Engineer, he is a member of the Professional Group on Vehicular Communications, the Armed Forces Communications and Electronics Association, and the American Rocket Society.

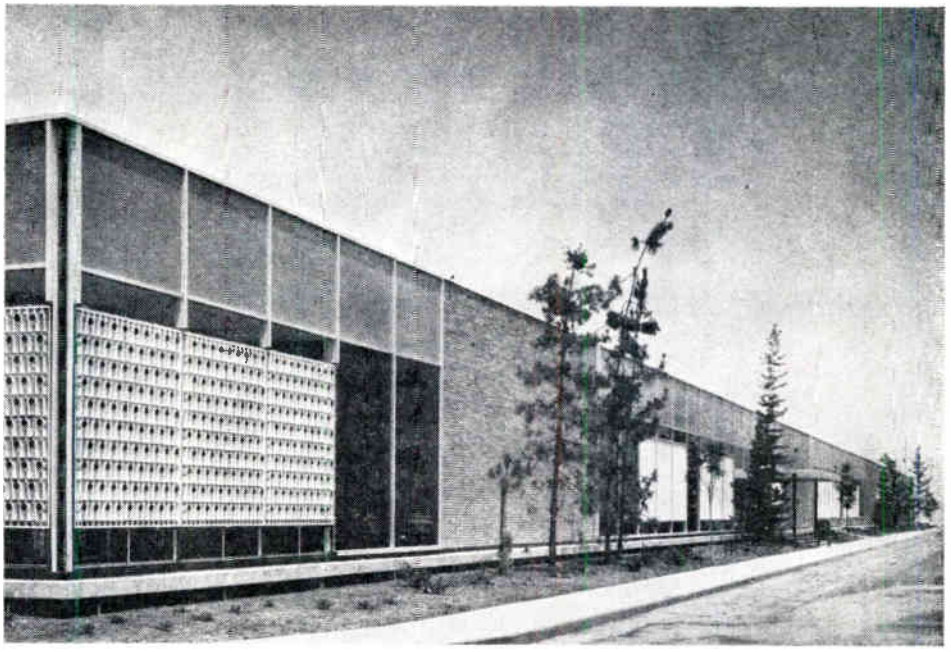
❖

Kendric A. Moore (S'41–A'43–M'44) has joined Granger Associates, Palo Alto, Calif., as manager of aviation products. He will be responsible for product planning and development, marketing and applications engineering for the firm's aviation products.

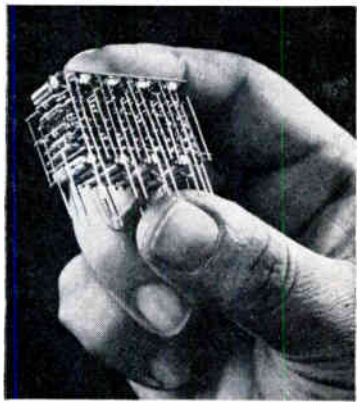
Until coming to Granger, he was based in New York as manager of communications for Pan American World Airways'

(Continued on page 132A)

ADVANCED FACILITY TO IMPLEMENT ADVANCED CONCEPTS IN COMPUTER SYSTEMS



Merritt MacKnight, Manager, Systems Development Department, demonstrates the sophisticated design of a Litton digital computer assembly for the new Grumman A2F.



Welded wire techniques substantially increase component packing densities.

This 180,000-square-foot building is the first unit of a facilities complex which eventually will comprise 825,000 square feet in the Los Angeles suburb of Woodland Hills, California. This facility of the Electronic Equipments Division of Litton Industries is designed for maximum convenience, comfort, and efficiency.

The primary areas of work here are the research, development and production of advanced real-time digital computer systems miniaturized for airborne applications; and high speed general purpose digital computers which incorporate the latest advances in the state of the art.

In our Guidance Systems Laboratory, pure inertial, astro-inertial, and inertial-doppler guidance systems are brought from newborn concepts to operating equipments.

If personal reasons dictate that you seek a new association at any time during the year, contact Mr. Sheldon Hirsch, Head, Research & Engineering Staff, Ventura Freeway at Canoga Avenue, Woodland Hills, California.

LITTON SYSTEMS, INC.
Electronic Equipments Division
Woodland Hills, Canoga Park, Beverly Hills, California • Waltham, Massachusetts

Computer & Control Systems • Tactical Data Processing Systems • Inertial Guidance & Navigation • Advanced Communication Techniques

IRE People

(Continued from page 130A)

Overseas Division. This involved engineering responsibility for radio communications and navigational equipment on PAA's fleet of B-707 and DC-8 jets and administrative responsibility for PAA's world wide communications network.

From 1945 to 1959, he was superintendent of radio engineering for the Pacific-Alaska Division of PAA. He supervised the development of "SELCAL," the I.C.A.O. recognized air/ground selective calling system, and has been active in development of automatic signaling and communications techniques.

In 1958, he headed up the cooperative PAA-industry program to develop "TROPSCAT" long range air/ground VHF techniques. From 1941 to 1945, he was a radio engineer for the Alaska Division of PAA, under contract to the U. S. Navy during World War II.

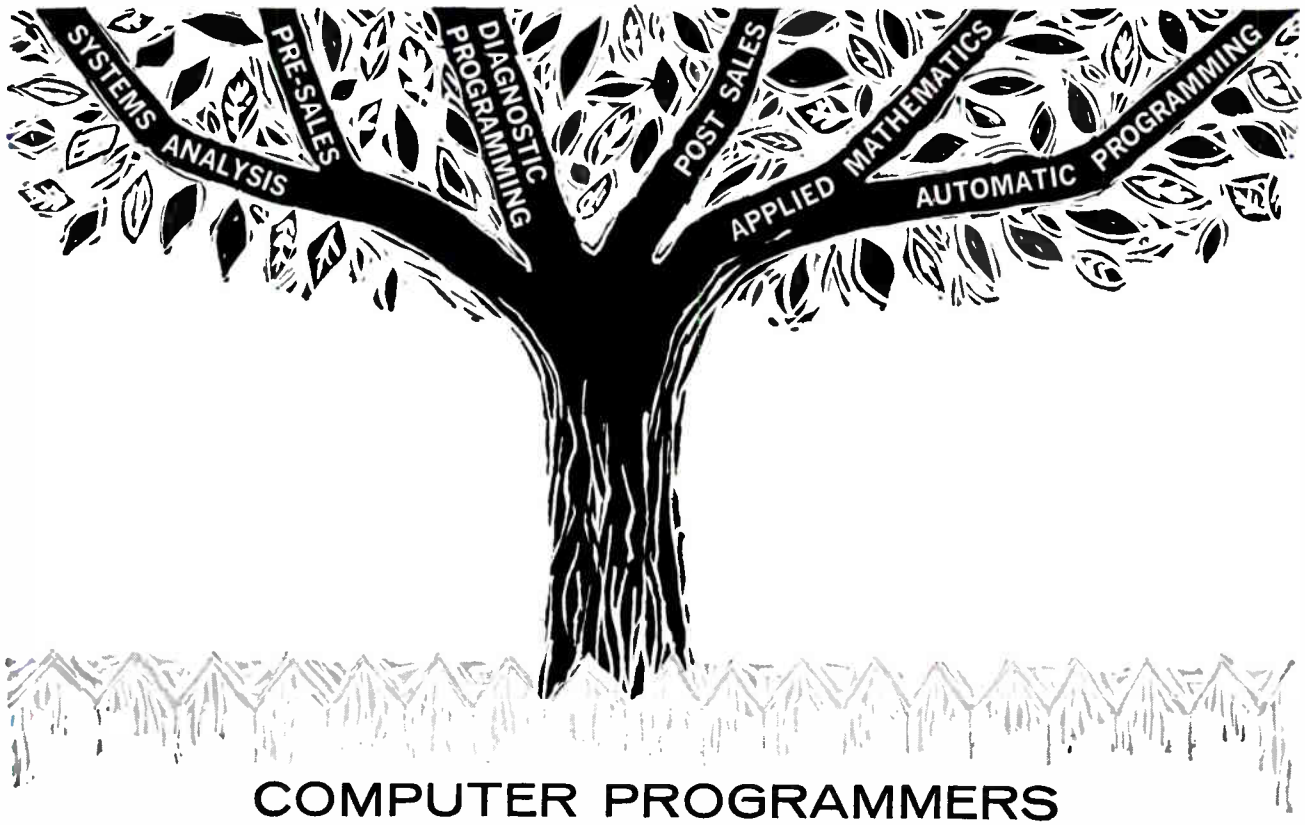
He has been active in ARINC, AEEC and airline industry committees in promoting airline communications improvement and reliability programs. In 1950, he was appointed as the first CAA-designated Radio Engineering Representative in International Region activity, holding the appointment until last January.

Mr. Moore is a member of Tau Beta Pi.

❖

(Continued on page 134A)

COMPUTER GROWTH OPPORTUNITIES



COMPUTER PROGRAMMERS

Our continuing growth is creating new positions for qualified programmers . . . a growth accelerated by recognition of individual achievement . . . a growth YOU can share. Persons who have written and debugged a variety of scientific and/or commercial programs on a large-scale binary computer are needed.

PHILCO offers a carefully expanding organization, educational program leading to advanced degrees, excellent facilities, equipment and atmosphere conducive to high levels of achievement.

New employees will receive a minimum of two months advanced training in the PHILCO 2000 system. Upon completion of the training program they should be available for assignment to a major metropolitan area. A relocation allowance is provided by the company.

If you are a mathematician, physicist or electronic engineer we invite you to investigate the opportunities as a Customer Service Representative. Inquiries are also invited from experienced Computer Sales Representatives, Systems Analysts and Field Engineers.

APPLY
Mr. John Felos
Professional Employment Mgr.
PHILCO COMPUTER DIV.
Willow Grove, Pa.

PHILCO®

Famous for Quality the World Over

IRE People

(Continued from page 132A)

Dr. William M. Mueller (S'52–A'53–M'58) has been appointed assistant manager of manufacturing for the Hughes Aircraft Company's microwave tube division, it was recently announced.

In addition to management responsibilities, involving microwave tube production, he will be in charge of special development projects in the manufacturing department.

Dr. Mueller formerly was a member of the technical staff of the Hughes Research Laboratories in Malibu, Calif. Before joining the Company in 1956, he was engaged in microwave tube research work at the University of California Microwave Laboratory and the Electronics Research Laboratory. He received the B.S. degree in 1950 from the University of California, Berkeley, and the Ph.D. degree from the same university in 1958.

❖

Robert H. Packard (A'45–M'50) was appointed Chief Engineer of Power Sources, Inc., Burlington, Mass., according to a recent announcement.

In his new position, he will assume the responsibility of all phases of the company's engineering work. This will include direction of the development programs and special custom designs, and technical direction of the quality control section.

He has more than 25 years of experience in the electronics field, having served as a Project Engineer for Raytheon Manufacturing Company, Arthur D. Little, Inc., General Communication Company, Baird, Atomic, Inc., and Technical Operations, Inc., all of Boston Mass. He joined Power Sources, Inc., on May 2, 1960.

Mr. Packard is a member of the Harvard Engineering Society.

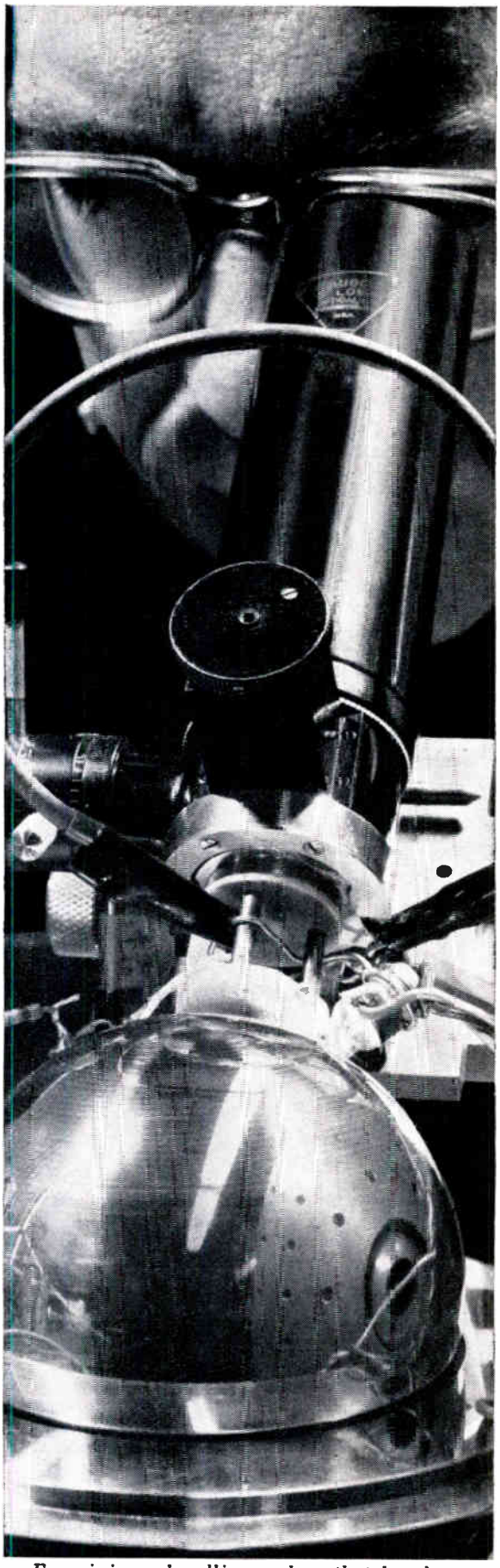
❖

The appointment of **Eliasz Poss** (S'51–A'54) as Chief Circuit Development Engineer of Electronic Energy Conversion Corporation, N. Y., was recently announced by Dr. Victor Wouk, president. Mr. Poss will be in charge of circuit design and development for dc and ac power supplies, line voltage regulators, inverters and converters.

E. Poss

He received his early technical education in Rome, Italy, and subsequently received the BSEE degree from Yale University, New Haven, Conn., and the MSEE from Columbia University, New York, N. Y. He was formerly an Associate Research Scientist with the Research Division of New York University, New York,

(Continued on page 138A)



Examining a beryllium sphere that has been machined to tolerances finer than 15 millionths of an inch to form the rotor of an electrically suspended gyro.

Inertial Navigation Career Opportunities at

Honeywell-Aero

The continued expansion of Honeywell's Marine Systems Group has created a number of important new openings. This group is assigned the interesting and stimulating task of developing new electrically suspended gyros and submarine inertial systems using these advanced gyros. Openings include:

INERTIAL SYSTEMS ANALYST: Mathematician or engineer with strong background in vector analysis, operational calculus, matrix algebra and related techniques, to carry out analysis of inertial systems configurations including error evaluation.

DIGITAL SYSTEMS AND LOGIC DESIGNERS: BSEE or MSEE for design and development of electronic data processing equipment. Familiar with digital logic techniques at current state of the art; capable of organizing computing systems to perform various tasks including logical design and critical parameter specifications. Also engineers familiar with digital to analog data conversion.

ELECTRONIC ENGINEER: Electrical engineering degree plus experience in miniaturized semi-conductor electronics development. To design servo, pickoff, and other electronics for use with gyros and accelerometers.

ENGINEERING PHYSICIST: Physicist with practical and theoretical understanding of mechanics, magnetism and electricity to analyze and develop inertial sensors of novel and original design. Also experimental physicist with experience in the development of small, precise electro-optical devices.

MECHANICAL ENGINEER: BSME with 3 to 5 years' experience in extreme precision fabrication techniques to work on the alignment and stable mounting of precision optical-mechanical instruments.

INERTIAL COMPONENTS ENGINEER: Familiar with inertial component specifications and available sources to conduct component evaluations for marine systems.

To discuss these or other openings, write Mr. James H. Burg, Technical Director, Aeronautical Division, 2600 Ridgeway Road, Minneapolis 40, Minn., Dept. 839.

Honeywell

Military Products Group

To explore professional opportunities in other Honeywell operations coast to coast, send your application in confidence to H. T. Eckstrom, Honeywell, Minneapolis 8, Minn.

IRE People

(Continued from page 134A)

N. Y., where he performed extensive developmental work on Airborne Navigational Equipment and Inertial Guidance. He was also Associate Electronic Engineer with Emerson Radio and Phonograph Corporation, where he was concerned with design and development of transistorized power supplies, dc to ac converters, magnetic amplifiers, test equipment and system study.

Mr. Poss is a member of the Professional Groups on Electron Devices, Automatic Control, Circuit Theory and Instrumentation.

❖

The selection of **Herbert H. Rosen** (S'51–A'54–M'57) as Corporate Director of Public Relations of the Hoffman Electronics Corporation, Los Angeles, Calif., was recently announced. He recently served as Assistant Director for Educational Programs for the National Aeronautics and Space Administration.

He will be responsible for planning and coordinating the expanding public relations activities in the corporation's five divisions—Consumer Products, Industrial Products, Military Products, Science Center, and Semiconductor.

He joined NASA in 1958 as the Deputy Director of the Office of Public Information. He became the Assistant Director for Educational Programs earlier this year. Prior to joining NASA, he was Washington Editor for Hayden Publications, reporting extensively on Washington affairs related to the electronics industry in "Electronic Week" and "Electronic Design." Preceding his association with Hayden, he was Chief of Technical Information for the ACF Electronics and Nuclear Energy Products Divisions of ACF Industries, Inc. Earlier he was a member of the Office of Technical Information of the National Bureau of Standards, where he had started as a microwave standards engineer. He was also a writer-announcer for several radio stations in New York and Louisiana. During World War II, he served with the U. S. Marine Corps as a radar and gun data director technician.

Born and raised in Philadelphia, Pa., he attended the University of Pennsylvania, Pa., the Moore School of Engineering, Philadelphia, Pa., and received the Bachelor of Science in Engineering degree from the George Washington University, Washington, D. C. He also participated in the graduate program in engineering administration at George Washington. While an undergraduate, he was elected to Sigma Tau, honors engineering fraternity. He has served as President of the George Washington Engineer Alumni Association and as a vice president of the Governing Board of the General Alumni Association of that university.

Mr. Rosen is a member of the National Press Club, the Aviation/Space Writers Associations, the American Ordnance

(Continued on page 140A)

NASA program-highlights

NEXT DECADE IN SPACE

Year 4 to 14 of the Space Age

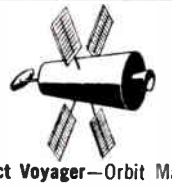
Project Mercury—U. S.'s first manned satellite.

Project Surveyor—First soft landing on moon. Conduct observations from stationary position.

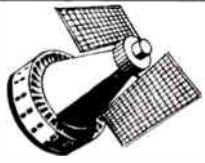
Project Prospector—Soft landing on moon and exploration of area within 50 miles of landing point.

Solar Observatory—350 lb. Large flywheel and extended arms rotate to stabilize. Under construction.

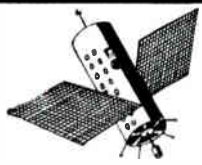
Project Mariner—600 to 1200 lbs. First U. S. Planetary missions to Venus and Mars. Modified craft for hard landings on moon.



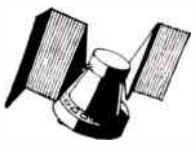
Project Voyager—Orbit Mars and Venus and eject instrumented capsule for atmospheric entry and perhaps landing.



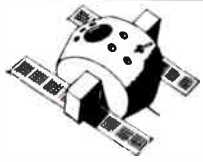
Nimbus—600 to 700 lb. meteorological satellite series. Stabilization system will keep cameras pointed earthward.



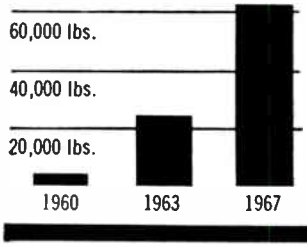
Orbiting Geophysical Observatory—1000 lb. geophysical research satellite designed for a near earth circular polar orbit or an inclined highly elliptical orbit.



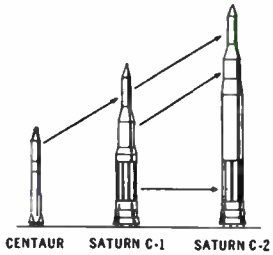
Project Aeros—24-hour stationary weather satellite. Launched in equatorial orbit. Three satellites could permit continuous observation of most of earth's surface.



Orbiting Astronomical Observatory—Standardized, 3500 lb. satellite, for several experiments with different scientific sensors and specialized devices.



Anticipated Growth of NASA Spacecraft in terms of weight of individual near earth satellites.



Launch Vehicles—New and more powerful launch vehicles; chemical, electrical, nuclear propulsion.

These programs facing the scientists and engineers of NASA comprise the most challenging assignment ever given a group of Americans.

You are invited to work alongside the many distinguished and dedicated members of our technical staff. For details about outstanding professional opportunities, address your inquiry to the Personnel Director of any of these NASA Research and Space Flight Centers—

NASA Ames Research Center • Mountain View, California

NASA Flight Research Center • P.O. Box 273, Edwards, California

NASA Goddard Space Flight Center • Greenbelt, Maryland

NASA Langley Research Center • Hampton, Virginia

NASA Lewis Research Center • Cleveland 35, Ohio

NASA Marshall Space Flight Center • Huntsville, Alabama

NASA Wallops Station • Wallops Island, Virginia

National Aeronautics and Space Administration

NASA

IRE People

(Continued from page 138A)

Association, and the Armed Forces Communications Electronics Association. During his tenure in Washington, D. C., he served as a public relations advisor to AFCEA, IRE, and several local engineering organizations.

❖

Sylvania Electric Products Inc., a subsidiary of General Telephone & Electronics Corporation, announced that **Dr. Seymour Stein** (S'48–A'54–SM'57) and **Dr. James E. Storer** (A'54–SM'58) of the company's Applied Research Laboratory have been promoted to senior scientists—the first to achieve that position within GT&E.

In making the announcement, Dr. L. S. Sheingold, Director of the Applied Research Laboratory, said the new positions are in recognition of "outstanding scientific contributions." He said the senior scientist role is "similar to that of a research professor in our leading universities—where an outstanding individual is provided with an atmosphere highly conducive to creative research."

Dr. Stein's current communications research activities include theoretical studies in secure communications, statistical stud-

(Continued on page 142A)

A message of significance to the leading microwave scientists of TOMORROW ...a message you should act on TODAY!

Sylvania's Microwave Device Operations on the San Francisco Peninsula now has programs of advanced development underway in the microwave device field. This work offers a rare opportunity to outstanding microwave specialists—an opportunity to assume overall responsibility for exploration in the fields of high power traveling wave tubes employing periodic structures, high power klystrons, and ferrite devices. The men who carry these programs forward should preferably have a Ph.D and several years of relevant experience.

You are invited to investigate now by writing to Dr. J. S. Needle at the address below. (Similar opportunities in the field of magnetrons and special purpose tubes also exist at the Microwave Device Operations in Williamsport, Pennsylvania.)

MICROWAVE DEVICE OPERATIONS

P. O. BOX 997, MOUNTAIN VIEW, CALIFORNIA

SYLVANIA

Subsidiary of **GENERAL TELEPHONE & ELECTRONICS**

GENERAL SYSTEM

6866

IRE People

(Continued from page 140A)

ies in fading radio systems (tropospheric scatter), and use of feedback communications for contravention of the effects of noise in data communications systems.

Born in Brooklyn, N. Y., he received the bachelor's degree in electrical engineering from City College of New York, and the master's and doctor's degrees in applied physics from Harvard University, Cambridge, Mass. At Harvard, he was an RCA predoctoral fellow in electronics (National Research Council).

Author of a number of papers presented before technical societies and published in technical journals, he is a member of Eta Kappa Nu, Tau Beta Pi and Sigma Xi honorary societies, and the American Association for the Advancement of Science.

Prior to joining Sylvania in August, 1957, Dr. Storer served as a consultant to the Applied Research Laboratory, performing studies relating to military systems analysis. His subsequent work at the laboratory has included fundamental research in signal analysis and data processing. He has investigated novel digital codes for radar and communications using advanced mathematical techniques. His major contribution has been the synthesis and analysis of new types of digital data communication systems.

Born in Buffalo, N. Y., he received the bachelor's degree in physics from Cornell University, Ithaca, N. Y., and the master's and doctor's degrees in applied physics from Harvard University, Cambridge, Mass. He has been an Atomic Energy Commission fellow, a research fellow and lecturer at Harvard, and a John Simon Guggenheim fellow. During his tenure as assistant professor in the division of applied science at Harvard, he served as consultant to Sylvania and other companies.

Author of numerous technical papers, Dr. Storer has also written a book, "Passive Network Synthesis." He is a member of Sigma Xi, the American Association of Physics Teachers, and the American Institute of Physics.

❖

Irwin Stelzer (A'54) has been named Sales Manager for Alloys Unlimited Chemicals, Inc., of Long Island City, N. Y.

I. STELZER

In his new position, he will supervise sales and market research for this new firm.

Before joining Alloys Unlimited Chemicals, Inc., he was a Sales Executive for United Mineral & Chemical Corporation. Since the inception of the semiconductor industry, he has specialized in marketing solid state materials.

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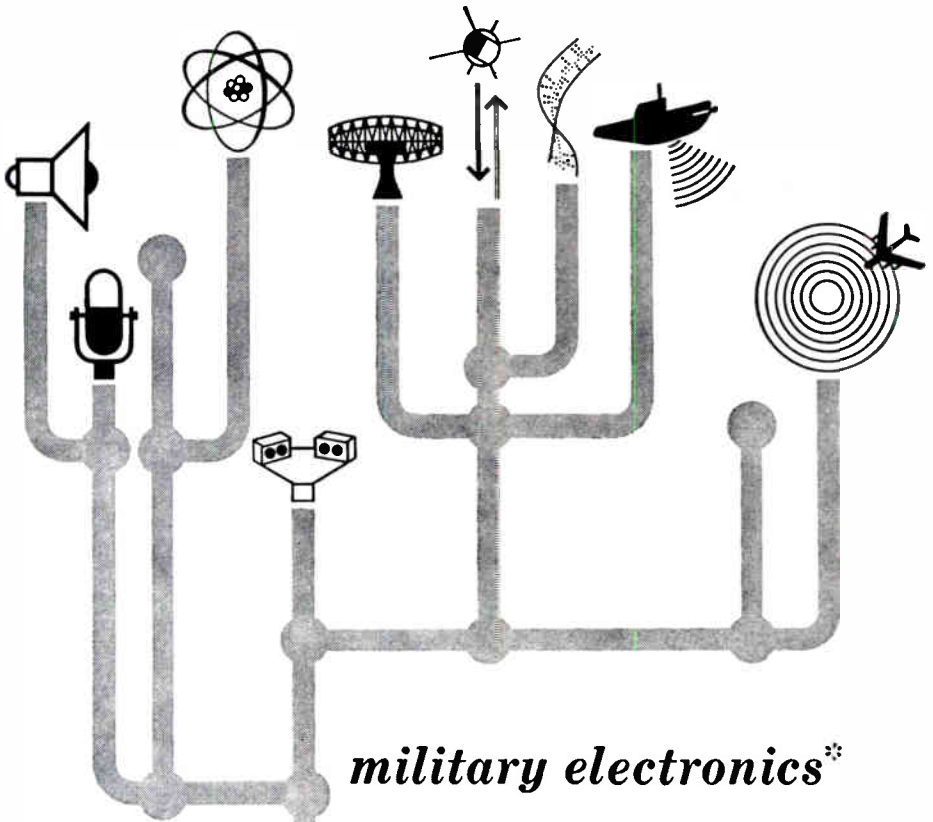

*military electronics**

*commercial electronics**

You'll find growth in both* areas at STROMBERG-CARLSON

DIVISION OF GENERAL DYNAMICS

New Professional Opportunities Now Open Across Our Entire Organization

The diversity and balance of our activities at Stromberg-Carlson – *in commercial and military fields* – creates both company strength and long term career stability for our professional personnel. *Growth* in both areas proceeds from a far-sighted policy of rising investment in research, to ensure the Company of an advantageous position as creator and supplier of continually more sophisticated systems and equipment. Specifically in the last five years, since Stromberg-Carlson became a division of General Dynamics, research budgets jumped 50%, product sales have risen dramatically, and our entire organization has expanded 60%. This year we are raising our research activity another 10%.

Areas in which Stromberg-Carlson is currently engaged include:

- **Nuclear Instrumentation**
- **Passive Reconnaissance**
- **Sonar Systems**
- **Automatic Test Equipment**
- **Stereo High Fidelity**
- **Single Side Band Communications**
- **Telecommunications**
- **Airport Traffic Control**
- **Avionic Systems**
- **Industrial Sound Systems**
- **Classified Investigations in ASW Field**
  (utilizing World's Largest Indoor Underwater Acoustic Test Facility inaugurated at Rochester, N. Y. headquarters in 1959)

Engineers and scientists interested in the career-advantages of association with a broad-based, stable and healthily expanding company, while contributing professionally to challenging technical programs, are invited to inquire about new positions in their fields.

Please address Mr. Maurice Downey.

STROMBERG-CARLSON

A DIVISION OF **GENERAL DYNAMICS**

1476 N. Goodman St., Rochester 3, New York

IRE People

(Continued from page 142A)

Mr. Stelzer received the B.S. degree from New York University, New York, N. Y., and is a member of ASTM.

❖

Robert G. Swain (A'51–M'57) has been named to the new post of product planning manager, semiconductors, for CBS Electronics, the manufacturing division of Columbia Broadcasting System, Inc., according to a recent announcement.

R. G. SWAIN

He was Eastern regional sales manager for semiconductors, and before that, was supervisor of field engineering, Eastern region.

He joined CBS Electronics in 1952 as a commercial engineer, and was subsequently a sales engineer and a semiconductor sales specialist.

A native of East Orange, N. J., Mr. Swain is a graduate of Newark College of Engineering, Newark, N. J. He is a member of the American Management Association.

❖

Appointment of **Joseph P. Vang** (S'50–A'51) as assistant manager of field sales for Stromberg-Carlson's Electronics Division was recently announced. Stromberg-Carlson is a division of General Dynamics Corporation.

J. P. VANG

He came to Stromberg-Carlson in 1957 and has held several marketing positions prior to his present assignment. Before joining Stromberg-Carlson, he was with Sperry Gyroscope Company, L. I., N. Y., for nearly eight years. While there he received a commendation from the Chief of BuShips for his work as technical advisor on a series of Navy films.

Mr. Vang is a native of Mendon, N. Y., and served five years in the U. S. Navy, from 1943 through 1947. He studied chemical engineering at Michigan State University, East Lansing, and Yale University, New Haven, Conn., and electrical engineering at Yale, where he received the bachelor's degree in electrical engineering in 1950. He is a member of the Armed Forces Communications and Electronics Association, Association of the U. S. Army, and the American Society of Chemical Engineers.

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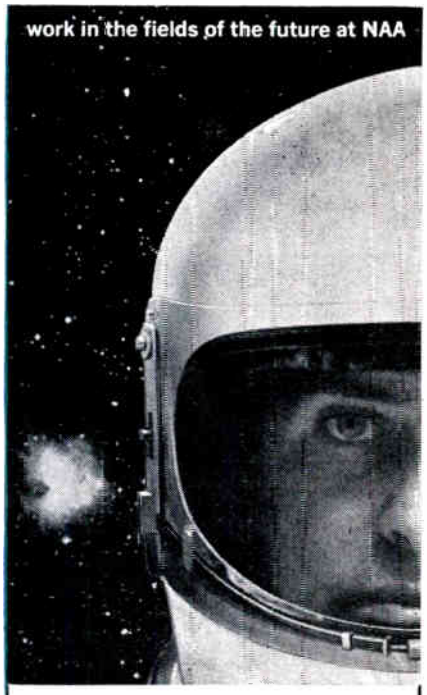
(Continued on page 146A)



OPERATIONS ANALYSIS

Opportunities for operations research analysis covering the spectrum of weapon systems. Application of analytical techniques to determination of weapon systems performance and effectiveness involving tactical analysis, statistics, game theory, and nuclear physics.

Facilities for research include new IBM 7090, analog computer laboratory, and tactical game room.

M.S. or Ph.D. in Engineering, Math or Physics preferred. B.S. or B.A. with exceptional experience or recent graduates desiring this field are also encouraged to apply.

For more information please write to: Mr. B. A. Bowman, Engineering Personnel, North American Aviation, Inc., Los Angeles 45, California

LOS ANGELES DIVISION OF
NORTH AMERICAN AVIATION

SELECTIVE OPPORTUNITIES AT MOTOROLA—PHOENIX—FOR

- TEST EQUIPMENT CIRCUIT DESIGN ENGINEERS

  SYSTEMS TEST EQUIPMENT DESIGN, CONVENTIONAL OR TRANSISTORIZED. FAMILIARITY WITH TECHNICAL SUPERVISION, OR T.E. MAINTENANCE AND CALIBRATION, OR T.E. CONSTRUCTION REQUIRED. E.E. DEGREE PREFERRED.

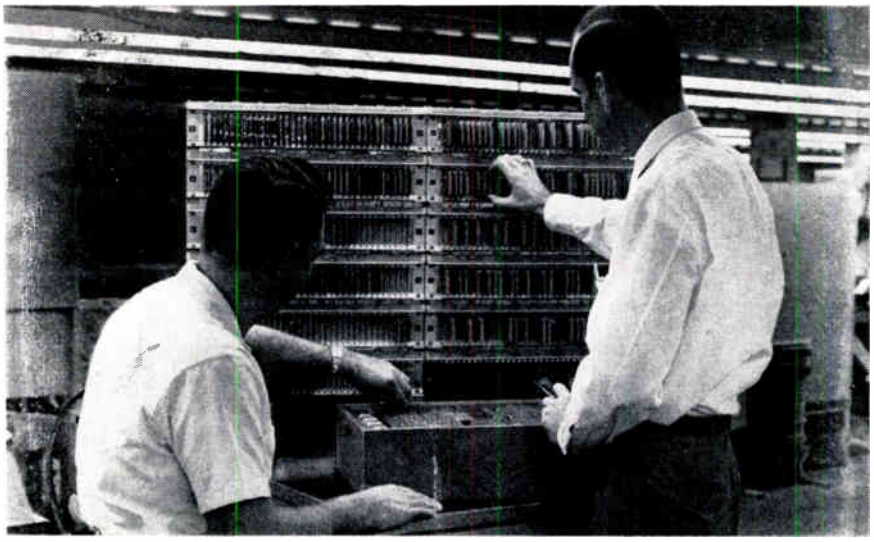
- TRANSDUCER DESIGN ENGINEER

  SUPERVISE DEVELOPMENT NEW LINE INDUSTRIAL TRANSDUCERS.

- RADIO FREQUENCY INTERFERENCE ENGINEER

  CONSULTANT TO PROJECT AND SUBCONTRACTORS. EXPERIENCE LOW THROUGH MICROWAVE FREQUENCIES AT SYSTEMS LEVEL.

WRITE BOB WORCESTER, DEPT. 101, AT ADDRESS BELOW.



THE E.E. WHO IS FINDING FULFILLMENT

With a B.S. degree (E.E.) from the University of Texas, 1950, he took his first job in industry but found it lacked security. His second job — with the guided missile division of a large corporation — offered security but lacked the growth potential he sought. In 1957 he applied to MOTOROLA. Pains were taken to place him in a job that would utilize his talents to the fullest — give him the challenge needed. Today, he is Project Leader of an Electronic Design Group in MOTOROLA's Military Electronics Division. His case is typical of advancement at MOTOROLA. For it is our policy to exercise extreme care in professional personnel placement. By doing so, we help scientists and engineers find continuing fulfillment — and thus strengthen MOTOROLA's capability to serve the nation.

EQUAL JOB OPPORTUNITY For All Qualified Applicants

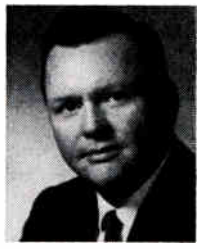
MOTOROLA

MILITARY ELECTRONICS DIVISION, WESTERN CENTER
8201 E. McDowell Road, Scottsdale, Arizona
Motorola also offers opportunities at Riverside, California and Chicago, Illinois.

IRE People

(Continued from page 144A)

Wilfred V. Warner (A'49) has been appointed to the position of Vice President—Sales, for Ford Instrument Company, Division of Sperry Rand Corporation, it was recently announced.



W. V. WARNER

He has been General Sales Manager of the Company which specializes in computers and controls for military missiles, aircraft, and warships. Previous to moving to that position, he had been Manager of Air Force contracts, and prior to this assignment was head of the company's Mid-West Sales Engineering Office in Dayton, Ohio.

Mr. Warner joined the Ford Instrument Division of Sperry Rand Corporation in 1951. He attended New York University, New York, N. Y., and was attached to the Air Transport Command in World War II. He is a member of the American Ordnance Association, the American Rocket Society, the Association of the U. S. Army, and the Society of Naval Engineers.

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(Continued on page 148A)

SANDERS ASSOCIATES INC. Announces the opening of 2 NEW FACILITIES

ADVANCED SYSTEMS LABORATORIES
(on famed "Electronics Row" in suburban Boston)

NEW ENGINEERING OPERATION
(on suburban Long Island near New York City)

To meet the recent increase to $50 million in contract commitments, Sanders Associates of Nashua, New Hampshire is rapidly expanding its engineering staff in 3 locations: Nashua Headquarters; Burlington, Massachusetts and Plainview, L.I., New York.

This new expansion follows a 9-year growth from 11 engineers to over 1600 employees – a growth soundly based on technical excellence – inventing new concepts instead of using traditional approaches.

Pioneering programs are being continued in phased arrays, radar, pulse doppler radar systems, space radar and communication systems. Advanced concepts and techniques in a variety of areas provide stimulating assignments involving space technology, missiles and radar systems.

Positions available at all locations for:

SENIOR SYSTEMS ENGINEERS
To contribute to advanced techniques in the general field of military electronic systems. Applicable experience includes systems analysis, synthesis and integration, with extensive background in circuit design augmented by hardware implementation.

CIRCUIT DESIGN ENGINEERS
EE or Physics graduates with 2 to 8 years experience and familiarity with tubes and transistors and their utilization in all types of circuits, as well as the integration of circuits into sub-systems.

TRANSMITTER DESIGN ENGINEERS
2 to 8 years experience. For work up to and including microwaves.

PRODUCT DESIGN ENGINEERS
ME with heavy experience in feasibility studies coupled with experience in taking developed systems into production, monitoring mechanical design and overall packaging concepts of ECM or other airborne systems.

Positions in Plainview, L. I.

GROUND SUPPORT EQUIPMENT ENGINEERS
To design and develop system, assembly and sub-assembly electronic test equipment for the military. Should have appreciation for test equipment philosophy, with extensive experience in circuit design and hardware follow-through.

To arrange for a convenient interview at any of the three locations, send resumes to Mr. Richard McCarthy, Employment Manager, in Nashua.

SANDERS ASSOCIATES, INC.
NASHUA, NEW HAMPSHIRE

IRE People

(Continued from page 146A)

The appointment of **James R. Weiner** (S'41–A'47–SM'54) as Vice President—Engineering for Philco Corporation's Government and Industrial Group has been announced.

In this position, which is a new one in G&I, he will report directly to the Vice President and General Manager of the Group. His responsibility will be the coordination of the engineering and development work of the five divisions with the Philco Group. These divisions include Communications and Weapons Systems, Computer Communications Systems, Western Development Laboratories, and Sierra Electronics.

Before joining Philco, he was Associate Director of Research and Manager of the Communications and Control System for the DISCOVERER, SAMOS, and MIDAS programs at the Lockheed Missiles and Space Division at Palo Alto, California. Prior to joining Lockheed, he was Assistant Vice President for Engineering with Remington-Rand UNIVAC, a division of the Sperry Rand Corporation.

He is widely known throughout the electronics industry particularly for his work in the field of digital computers. He was closely associated with development and design of the BINAC and UNIVAC systems, the solid-state UNIVAC, and the LARC, an ultra high speed, solid-state computing system.

He has numerous patents and patent applications in the computer and electronics fields. He received the Bachelor of Science degree in Engineering Physics from the University of Illinois, Urbana, and the Master of Electrical Engineering degree from Polytechnic Institute of Brooklyn, Brooklyn, N. Y., and did further graduate work at Massachusetts Institute of Technology and Harvard University, Cambridge, Mass.

Mr. Weiner is a member of numerous technical societies and has served as a consultant for DOD.

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The appointment of **Frank G. Willey** (A'48–M'48) as Manager of Infrared Systems, Missile Electronics and Controls Division, Radio Corporation of America, has been announced.

He joined the Engineering Department of the Division in 1959 as Manager, Subsystems Development, and had for the previous five years been responsible for marketing infrared, radio and servo products for the Servo Corporation and telemetry products at Data Control Systems, Inc. He holds a number of patents in these fields. He received the engineering degree from Purdue University, Lafayette, Ind., in 1937.

Membership

The following transfers and admissions have been approved and are now effective:

Transfer to Senior Member

Balakrishnan, A. V., Los Angeles, Calif.
Callaghan, J. W., State College, Pa.
Freymodsson, J. B., Torrance, Calif.
Harrison, R. I., Bayside, L. I., N. Y.
Hastings, M. S., Severna Park, Md.
Horvath, A., Quito, Ecuador, S. A.
Irby, R. F., Fairfax, Va.
Kamal, A. K., Lafayette, Ind.
Krilanovich, N. J., Riverside, Calif.
Lakshmanan, T. K., Newark, N. J.

Admission to Senior Member

Andrews, F. A., Minneapolis, Minn.
Ball, J. N., Buffalo, N. Y.
Bodner, M., Burbank, Calif.
Cohen, J., Freeport, L. I., N. Y.
Cryer, W. C., Lutherville, Md.
DeBock, A. H., Louvain, Belgium
Heywood, J. E., Newport Beach, Calif.
Hogan, W. J., Washington, D. C.
Holmes, J. R., Owego, N. Y.
Irani, K. B., Lawrence, Kan.
Ketcham, A. W., Santa Barbara, Calif.
Liebson, S. H., Dayton, Ohio
Mellen, E. D., Washington, D. C.
Mercurio, S. P., Jr., Utica, N. Y.
Murray, W D., Malvern, Pa.
Nelson, S. W., Chicago, Ill.
Pendleton, D. W., Alexandria, Va.
Ross, D. C., Rockville, Md.
Ruzic, N. P., Chicago, Ill.
Schneider, E. G., Wayland, Mass.

(Continued on page 150A)

A MAJOR CAUSE OF FAILURE ELIMINATED BY BUILDING A TRANSISTOR INSIDE ITS OWN SHELL

Most transistor failure is not abrupt. It consists of surface changes causing a gradual shift in parameters. While the whole industry has sought answers, Fairchild has followed a research and development course of its own. We can now reveal a unique solution.

Called "PLANAR STRUCTURE," this Fairchild answer uses a passivated surface — a hard, passive coating of silicon oxide — not new in theory, but new in the way it is done. Fairchild oxidizes the surface first. Then the transistor's junctions are diffused **under the oxide.** Contaminants cannot reach them during process or after. Result: performance is unchanged by time, use, environment or even exposure to foreign matter.

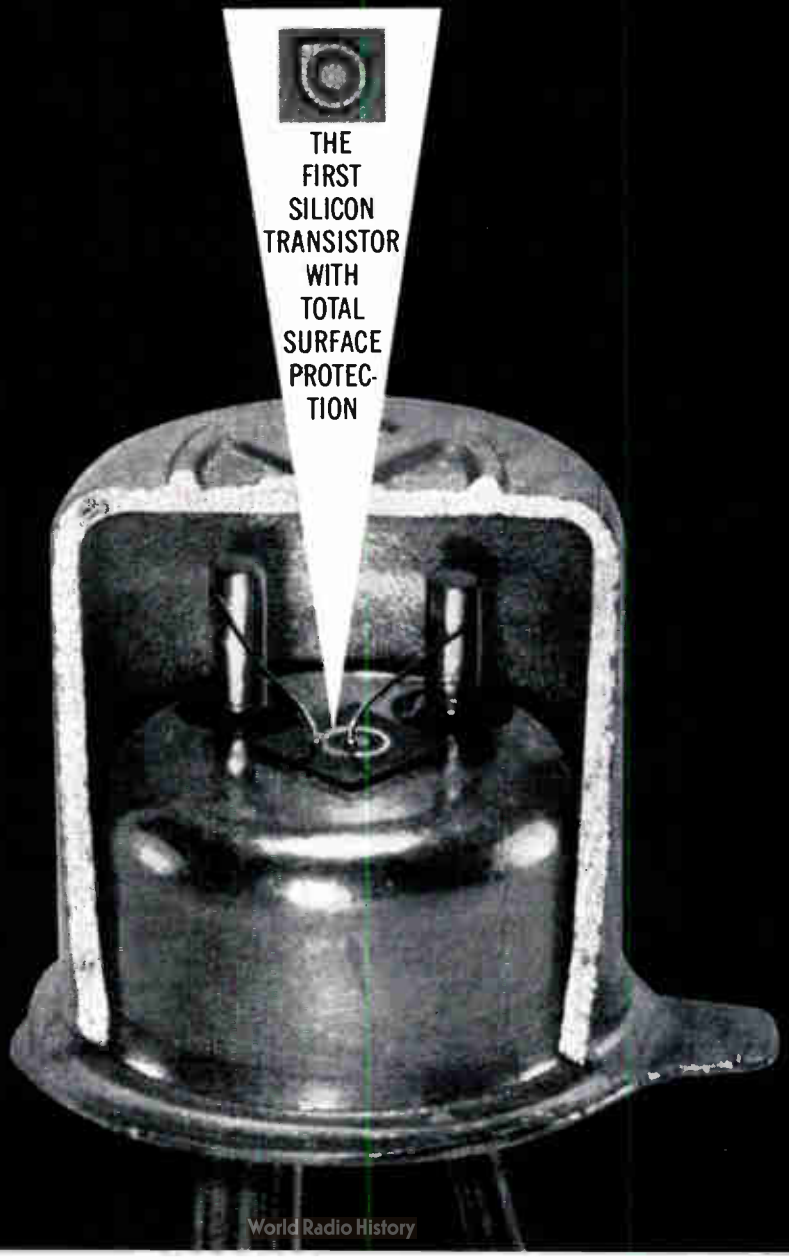
Planar is the answer: for system reliability where thousands of transistors must all be operative at an instant — for fast, simple circuits tightly packed in minimum space — for carefully matched pairs, triplets or quads that must stay exactly in balance — and for leakage reduction by a factor of one hundred. And planar is the answer even for simpler circuit requirements where high assurance has a value.

These advantages apply to planar diodes, too. Of course, Fairchild planar silicon transistors and diodes are available in production quantities. A new 12-page brochure explains the process and results more fully. May we send you a copy?

A wholly owned subsidiary of Fairchild Camera and Instrument Corp.

FAIRCHILD
SEMICONDUCTOR CORPORATION

545 WHISMAN RD. • MOUNTAIN VIEW, CALIF. • YOrkshire 8-8161



Membership

(Continued from page 148A)

Seaton, P. B., Dayton, Ohio
Siglin, P. W., Asbury Park, N. J.
Sorkness, R. E., Los Angeles, Calif.
Tank, L. E., Baltimore, Md.
Wada, M., Sendai, Miyagi-ken, Japan
Wilken, H. W., Alton, Ill.
Zitzman, K. F., Boulogne-sur-Seine, France

Transfer to Member

Adams, V. F., Jr., North Palm Beach, Fla.
Armstrong, P. S., San Mateo, Calif.
Barkley, J. W., Jr., Redwood City, Calif.
Battelle, R. B., Portola Valley, Calif.
Bonacci, E. L., Springdale, Conn.
Carter, L. J., Jr., Berkeley, Calif.
Catolla-Cavalcanti, R., Bologna, Italy
Chew, B. H., Oakland, Calif.
Corbin, M. W., Wright-Patterson AFB, Ohio
Dickerson, L. W., Sunnyvale, Calif.
Farrell, S. R., Orinda, Calif.
Fath, J. P., Trevose, Pa.
Fedak, J. F., Jr., Haddonfield, N. J.
Fey, C. F., Rochester, N. Y.
Gee, H. W., San Francisco, Calif.
Godfrey, G. F., Hamilton, Ont., Canada
Jones, M. H., Oakland, Calif.
Jorgensen, H. E., Mountain View, Calif.
Lieske, R. W., Baltimore, Md.
Lillie, W. A., Seattle, Wash.
Mason, H. J., Jr., Oklahoma City, Okla.
Maurer, C. D., Sunnyvale, Calif.
Pantell, R. H., Stanford, Calif.
Phillips, R. M., Redwood City, Calif.
Polachowski, B. A., Cayey, Puerto Rico
Pope, J. C., Walnut Creek, Calif.
Poulsen, J. E., Santa Clara, Calif.
Price, R. A., Santa Barbara, Calif.
Rehbein, N. W., Los Angeles, Calif.
Roberts, L. A., Palo Alto, Calif.
Romine, H. V., Clinton, Okla.
Rudin, M. B., Tustin, Calif.
Schneider, S., Costa Mesa, Calif.
Schnoor, K. G., Chevy Chase, Md.
Scott, D. M., Baltimore, Md.
Silverman, D., Anaheim, Calif.
Stone, K. A., Santa Ana, Calif.
Swyryd, M., Palo Alto, Calif.
Thaler, S., Reseda, Calif.
Upham, F. T., Orinda, Calif.
Vogelsberg, F. E., El Cerrito, Calif.
Walker, G. H., Nashua, N. H.
Walters, C. S., Bethesda, Md.
West, S. F., Sunnyvale, Calif.
Westwick, J., La'Mirada, Calif.
Whitten, M. G., Los Angeles, Calif.
Yagi, H. S., Santa Clara, Calif.

Admission to Member

Anderson, B. G., Poway, Calif.
Anderson, V. S., Chicago, Ill.
Anselmo, A. J., Melville, N. Y.
Arenberg, K. M., Skokie, Ill.
Ashley, L. F., Los Angeles, Calif.
Atkinson, P. H., London, Ont., Canada
Ayers, H. W., Torrance, Calif.
Bacque, C. D., Baltimore, Md.
Baker, W. A., Dover, N. J.
Barna, A., Pasadena, Calif.
Barrows, W. A., Owensboro, Ky.
Barton, H. O., Skokie, Ill.
Basford, R. L., Murray Hill, N. J.
Bauer, A. A., Elizabeth, N. J.
Beasley, J. M., Brentwood, Mo.
Bednar, E. S., Murray Hill, N. J.
Behrnes, F. G., Jr., Richardson, Tex.
Benike, H. R., Santa Ana, Calif.
Bigien, C., Santa Monica, Calif.
Bone, G. D., Jr., Severna Park, Md.

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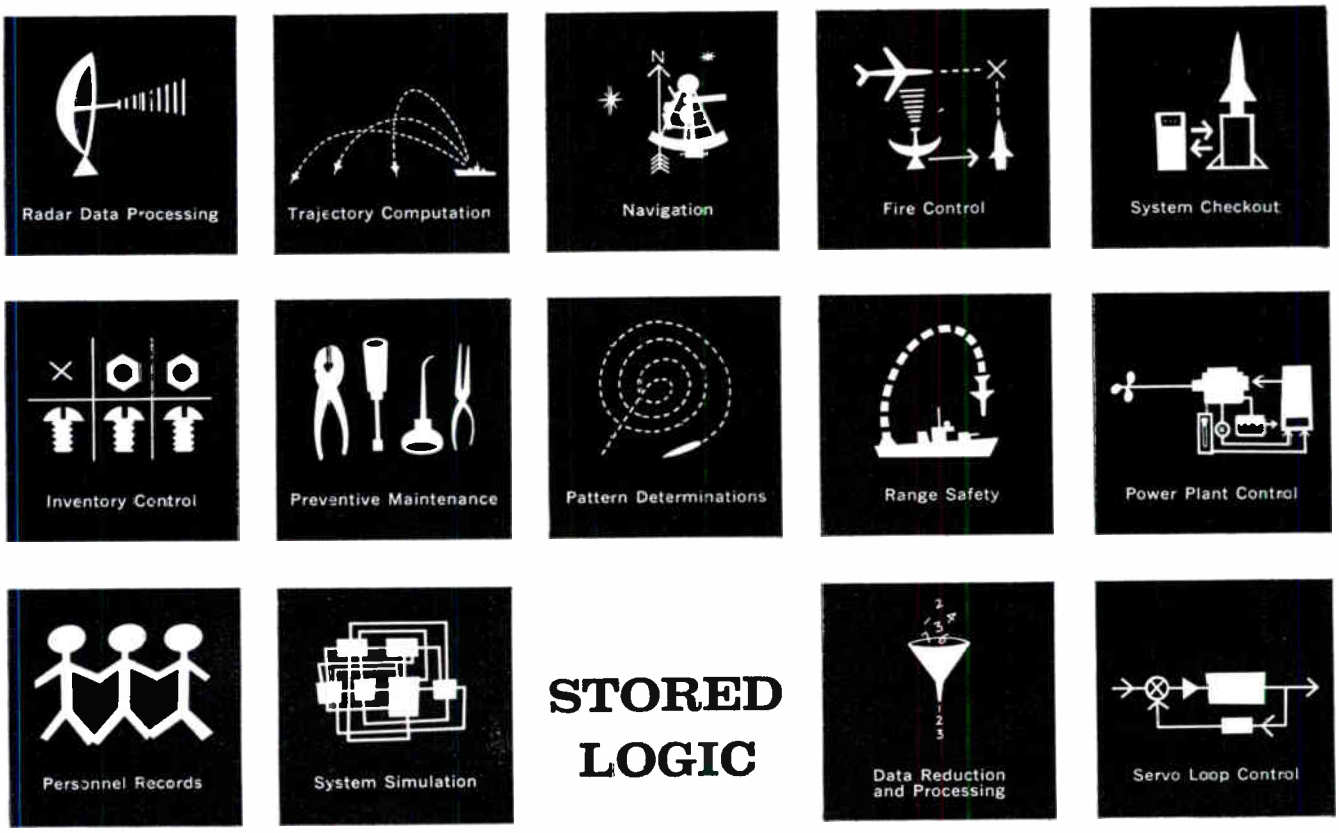


How to get a computer to think it's a one-man gang

Most computers are pretty fussy about the kind of problems they are willing to handle. While it's true that a "business" computer can be made to do "scientific" problems, and vice versa, every experienced computer user knows it's no simple matter to get a machine to accept such a change of character gracefully. Besides the fancy reprogramming involved, the computer is likely to be inefficient and uneconomical at solving problems it wasn't designed for.

From the user's point of view, the "ideal" computer is a *multiple-purpose* machine that can be used *efficiently* in many different types of applications, and at no higher cost than a computer intended primarily for any one of these applications.

From the programmer's point of view, the "ideal" machine is one with a flexible set of instructions that can be easily manipulated to fit just about any kind of problem that comes along. Both programmer and designer are likely to agree that the most practical way to realize this "ideal" computer is by using the *stored logic* principle.

Stored logic concepts developed by Ramo-Wooldridge are being used in the AN/UYK-1, a low-price, multiple-purpose Navy computer intended for shipboard use. In the Ramo-Wooldridge approach, stored logic permits the user to select a word length, order structure and instruction repertoire especially suited to the problem at hand. These normally "wired in" characteristics are specified by data stored in the computer's memory and may be changed during the normal loading procedure without hardware modification.

The AN/UYK-1 "Stored Logic" Multiple-Purpose Computer takes its place alongside the RW-400 "Polymorphic" data processing system as an outstanding example of the kind of advanced work in computer design which has characterized Ramo-Wooldridge over the past six years. Senior programmers are urgently needed to help develop a large "software" package for commercial and military applications of R-W *stored logic* computers, to prepare programs for the polymorphic data processing system, and to work on challenging applications engineering problems.

RAMO-WOOLDRIDGE

A DIVISION OF

THOMPSON RAMO WOOLDRIDGE INC.

8433 FALLBROOK AVENUE · CANOGA PARK, CALIFORNIA

Membership

(Continued from page 150A)

Boothe, R. R., Huntsville, Ala.
Bordman, S. L., Little Neck, L. I., N. Y.
Bott, W. J., Winston-Salem, N. C.
Boyshow, R., Gardena, Calif.
Bowler, B. L., Ithaca, N. Y.
Braswell, R. C., Severna Park, Md.
Brown, G. G., Ho Hokus, N. J.
Buntschuh, R. F., Ft. Walton Beach, Fla.
Burns, R. R., Leesburg, Va.
Calhoun, B. F., Norfolk, Va.
Carlson, E. R., Palos Verdes Estates, Calif.
Carroll, J. J., Indianapolis, Ind.
Cathey, L. Aiken, S. C.
Cheney, P. W., Palo Alto, Calif.
Chung, T., Costa Mesa, Calif.
Collie, S. T., Arlington, Tex.
Cooke, L., Winnipeg, Man., Canada
Corbett, T. H., Vancouver, B.C., Canada
Courtney, E. W., La Jolla, Calif.
Crane, A. S., Jr., Portland, Ore.
Cronenwett, W. T., Austin, Tex.
Crouch, W. M., Nashville, Tenn.
Culler, V., Plainsboro, N. J.
Dankel, O. L., Wichita, Kan.
Dehm, G. E., Severna Park, Md.
Dempsey, R. C., Canoga Park, Calif.
DeVoe, S. E., Indianapolis, Ind.
Dickey, J. R., Brooks AFB, Tex.
Ducote, B. A., Richardson, Tex.
Dunlop, L. J., Wappingers Falls, N. Y.
Dutton, D. C., Mobile, Ala.
Dwyer, T. A., Dayton, Ohio
Eberly, J. F., Watertown, Mass.
Eden, M., Cambridge, Mass.
Effinger, D. D., La Habra, Calif.
Ellis, R. E., New York, N. Y.
Engler, H. V., Huntsville, Ala.
English, G. G., Vancouver, B.C., Canada
Epstein, I. Cleveland, Ohio
Espey, H. R., Houston, Tex.
Estrin, S., Huntsville, Ala.
Ewin, W. H., Union, N. J.
Fisher, M. B., Los Gatos, Calif.
Flanders, M. C., Mobile, Ala.
Flesner, H. E., Norwalk, Calif.
Forssander, P. H., Indianapolis, Ind.
Foster, F. K., Ottawa, Ont., Canada
Fradette, D. M., Framingham, Mass.
Fredrick, G. F., Palo Alto, Calif.
Fresch, W. C., Phoenixville, Pa.
Gambrell, J. B., San Francisco, Calif.
Ganias, T. E., Rochester, N. Y.
Garino, A., Rome, Italy
George, C. H., Pittsfield, Mass.
Gilliam, A. A., Aiea, Hawaii
Glasgow, H., Mount Baldy, Calif.
Goldberg, M. E., Chicago, Ill.
Goldman, J., Norwalk, Conn.
Gomas, E. G., Buenos Aires, Argentina
Gowland, W. H., Baltimore, Md.
Gray, H. L., Irving, Tex.
Greenberg, N. S., Elizabeth, N. J.
Griffeth, G. C., Philadelphia, Pa.
Guenther, C. H., Mission, Kan.
Haase, C. W., Washington, D. C.
Hansford, J. L., Mobile, Ala.
Harris, M. G., Mobile, Ala.
Harris, R., Dayton, Ohio
Hart, J. L., Jr., Mobile, Ala.
Herman, L. K., Hawthorne, Calif.
Hogan, J. W., Brookley AFB, Ala.
Hong, L. K. Y., Seattle, Wash.
Hunter, M., Utica, N. Y.
Hussain, M. I., Los Angeles, Calif.
Hutchinson, D. P., Irvington-on-Hudson, N. Y.
Jackson, C., Jr., Owensboro, Ky.
Jacobson, W. H., Jr., Arlington, Va.
Jinguji, J. M., Pomona, Calif.
Johnson, N. C., Harrison, N. J.

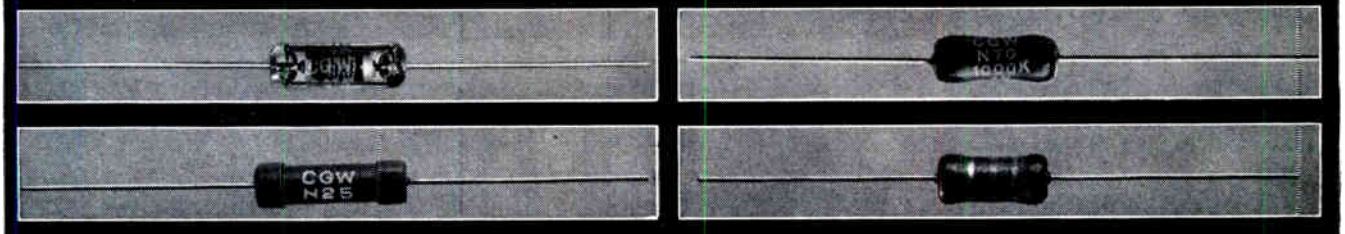
(Continued on page 154A)

COMPUTERS AND OTHER ELECTRONIC INSTRUMENTS demand resistors which give predictable performance in a small space and high ambient temperatures. This is a good description of Corning tin oxide film resistors, which are now competitive in price with other makes.

Tin oxide and glass are among the most stable materials. They are also low in cost.

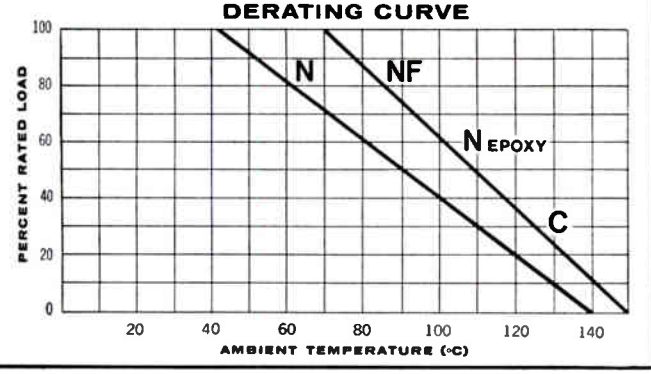
Couple these materials with exacting methods of manufacture, as we have done, and you have low-cost resistors meeting the pinching specifications required for computers and similar devices.

You have resistors with excellent reactive properties. With a shelf life of 0.1 to 0.2% per year. With noise levels lower than 0.1 microvolt per volt. And with typical values like these:



TYPE	DESCRIPTION	CORNING MODEL	WATTAGE	RESISTANCE (ohms)	TC	LOAD LIFE	OVERLOAD	MOISTURE RESISTANCE
NF	Glass ENCAPSULATED MIL-R-10509C, Char. B	NF60 NF65	⅛ ¼	100 100K 100 348K	150ppm/°C. −55 +150°C.	0.3%	0.03%	0.2% (Char. B)
N EPOXY	MIL-R-10509C, Char. B	N60 N65 N70	⅛ ¼ ½	10 133K 10 499K 10 1Meg	150ppm/°C. −55 +105°C.	0.5%	0.03%	0.5% (Char. B.)
N	MIL-R-10509B, Char. X	N12 N20 N25 N30	¼ ½ 1 2	100 133K 10 500K 10 1.5Meg 30 4.12Meg	150ppm/°C. −55 +105°C.	0.35%	0.1%	0.15% (Char. X)
C	Lowest cost film resistor; silicone insulation MIL-R-11C	C20 C32 C42	½ 1 2	51 150K 51 470K 10 1.4Meg	150ppm/°C. −55 +125°C.	1.5%	0.2%	0.3%

Note: Noise level for all models is less than 0.1 uv/v of applied signal.



For quantities of less than 1000, contact the nearest distributor serviced by Erie Distributor Division. For data sheets on Corning Type NF, N, N-EPOXY or C resistors, write CORNING GLASS WORKS, 542 High St., Bradford, Pa.

CORNING ELECTRONIC COMPONENTS
CORNING GLASS WORKS, BRADFORD, PA.

Membership

(Continued from page 152A)

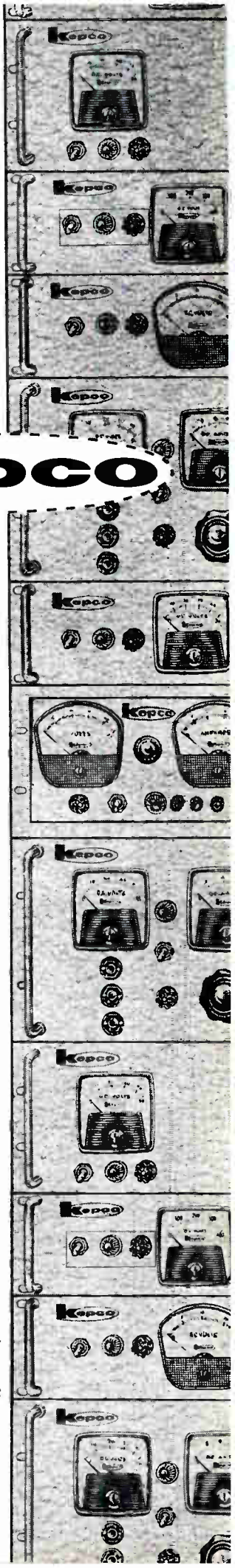
Jones, R., Philadelphia, Pa.
Kashihara, T. K., Willow Grove, Pa.
Keller, E. W., State College, Pa.
Kenyon, R. E., Ithaca, N. Y.
Kidwell, O. A., La Puente, Calif.
Kirchmaier, T. W., Topsfield, Mass.
Kirvaitis, K., Chicago, Ill.
Kluever, H. C., Buffalo, N. Y.
Kornberg, F., Brooklyn, N. Y.
Kumar, R., Walton-on-Thames, Surrey, England
La Capra, J., Melbourne, Fla.
Lesnik, M. I., N. Wilmington, Mass.
Levien, F. H., Allentown, Pa.
Levinson, H., Seattle, Wash.
Lipple, H., Fayetteville, N. Y.
Litman, G. G., Los Angeles, Calif.
Litt, S. S., New York, N. Y.
Loewenthal, W., Los Angeles, Calif.
Madvig, R. M., Sunnyvale, Calif.
Maksimik, C. J., Flushing, N. Y.
Malloy, W. J., Eau Gallie, Fla.
Martin, R. L., Jr., Palo Alto, Calif.
Maxwell, E. L., Boulder, Colo.
May, J. L., Ottawa, Ont., Canada
McCall, B. F., Orlando, Fla.
McDonald, T. B., Mobile, Ala.
McIntyre, W. B., Bethesda, Md.
McManamon, P. M., Oak Park, Ill.
Melvin, W. J., North Hollywood, Calif.
Meyer, C. H. W., Philadelphia, Pa.
Michaels, J. D., Los Angeles, Calif.
Mickelsen, J. K., Liverpool, N. Y.
Miller, D. J., Philadelphia, Pa.
Mondloch, A. J., Buffalo, N. Y.
Montgomery, D. H., Dayton, Ohio
Morrison, J. W., Jr., New York, N. Y.
Mullins, A. F., North Wales, Pa.
Murray, R. F., Seattle, Wash.
Neill, D. L., Plainview, L. I., N. Y.
Nipp, J. H., Minneapolis, Minn.
Novotny, G. V., New York, N. Y.
O'Connell, J. A., Poughkeepsie, N. Y.
O'Conor, J. S., Philadelphia, Pa.
Olt, R. D., E. Chicago, Ind.
Oram, D. O., Dallas, Tex.
Orthel, J. C., San Diego, Calif.
Palmer, F. H., West Acton, Mass.
Patterson, C. W., Eau Gallie, Fla.
Perron, J. Y., Montreal, Que., Canada
Pfeifer, A. F., Lakewood, Calif.
Pogue, M. C., Belmont, Calif.
Powner, O. D., Van Nuys, Calif.
Prisant, M. B., Newton, Mass.
Raisanen, W. R., St. Paul, Minn.
Rasnick, B., Somis, Calif.
Ravitch, L. I., Philadelphia, Pa.
Reed, A. R., Torrance, Calif.
Reeder, B. B., Anaheim, Calif.
Ristad, C. H., Endicott, N. Y.
Roberts, L. D., Los Angeles, Calif.
Rogers, S. C., San Jose, Calif.
Rohde, P. J., Berwyn, Pa.
Rosenfield, S. B., Pelham Manor, N. Y.
Salasin, H., Plymouth Meeting, Pa.
Salisbury, J. T., Collingswood, N. J.
Schietzel, R. J., Ulm/Donau, Germany
Schiller, H. D., Toronto, Ont., Canada
Schmid, F. R., El Segundo, Calif.
Schmidt, F. J., San Diego, Calif.
Scott, E. H., North Hollywood, Calif.
Scott, L. D., APO, San Francisco, Calif.
Shewchun, J., Waterloo, Ont., Canada
Sigismonti, I., Upper Darby, Pa.
Silverstein, L. S., Syracuse, N. Y.
Simon, A., Fairlawn, N. J.
Sindhvananda, K., Philadelphia, Pa.
Simpson, D. C., Huntsville, Ala.
Simpson, L., New York, N. Y.
Skiko, E. J., Poughkeepsie, N. Y.
Slater, R. J., Cleveland Heights, Ohio

Smith, P., Farmingdale, N. J.
Somers, J. W., Dallas, Tex.
Spector, L., Randolph, Mass.
Stern, I. A., Manhattan Beach, Calif.
Sternes, K. J., Portland, Ore.
Stone, S. H., Jr., Mountain View, Calif.
Thome, R. E., Poughkeepsie, N. Y.
Thompson, G. O., Wichita, Kan.
Tkacz, A., Bedford, Mass.
Tomlinson, J. R., Falls Church, Va.
Tompas, R. P., Fairfax, Va.
Towry, G. G., Dallas, Tex.
Trexler, W. E., Alamogordo, N. M.
Tsai, S., Chicago, Ill.
Tucci, A. E., Philadelphia, Pa.
Van Schooneveld, C., Den Haag, Netherlands
Varon, A. R., Washington, D. C.
Vetter, W. J., Waterloo, Ont., Canada
Verbeek, L. A. M., Cambridge, Mass.
Vincent, C., Owensboro, Ky.
Waldron, K. A., Topsfield, Mass.
Wetter, A., Margate City, N. J.
Williams, C. M., Burlington, Ont., Canada
Williams, J. M., Oklahoma City, Okla.
Wilson, W. W., Menlo Park, Calif.
Wiscavage, W. J., Great Falls, Mont.
Yager, L. A., New York, N. Y.
Yamamoto, T. H., Port Washington, L. I., N. Y.
Yard, R., Hillsdale, N. J.
Young, D. W., Jr., Canoga Park, Calif.

Admission to Associate

Allen, W. D., Garland, Tex.
Armstrong, J. B., Broadview, Ill.
Arnold, R. A., Rome, N. Y.
Balacek, T. V., Astoria, L. I., N. Y.
Baloun, R. J., Chicago, Ill.
Barker, L. R., San Francisco, Calif.
Beveridge, D. M., Chicago, Ill.
Beecher, M. J., Mineola, L. I., N. Y.
Bergwerk, J. C., Bellflower, Calif.
Boehler, H. L., Brookfield, Wis.
Borden, R. A., Salem, Mass.

(Continued on page 156A)



Membership

(Continued from page 155A)

Bos, R. A., La Grange, Ill.
Brandt, E. W., Jr., Falls Church, Va.
Broaddus, A. G., Jr., Richmond, Va.
Callis, T. J., Chicago, Ill.
Chaffee, A. W., South Pasadena, Calif.
Chalekian, J., Montreal, Que., Canada
Clark, W. A., Palo Alto, Calif.
Coleman, J. R., Hempstead, L. I., N. Y.
Commerton, J. M., New Hyde Park, L. I., N. Y.
Connell, R. D., Kingston, N. Y.
Corbett, K. M., Hingham, Mass.
Cortelyou, R. G., Staten Island, N. Y.
Daniels, R. W., Hastings-on-Hudson, N. Y.
Davison, C. A., Asbury Park, N. J.
Dubret, F., Geneva, Switzerland
Duffy, D. J., Laurel, Md.
Dvorak, A. R., Lincoln, Nebr.
Egan, A. C., Northampton, Mass.
Enderle, P. H., Allegany, N. Y.
Erickson, D. H., Nashua, N. H.
Erkanli, H. T., Long Beach, Calif.
Evers, L., Summit, N. J.
Fillman, D. L., Winston-Salem, N. C.
Fish, V., Jr., Balboa Island, Calif.
Fisher, G. E., Charlottesville, Va.
Fisher, L. M., New York, N. Y.
Flickinger, C. D., Baltimore, Md.
Foster, J. Y., Des Moines, Iowa
Francisco, R. S. F., Bogota, Colombia
Frank, E. J., Rehovoth, Israel
Frederick, W. H., Alamogordo, N. M.
Fruchtnis, G. S., Bogota, Colombia
Garner, H. D., London, Ont., Canada
Gialanella, J. A., North Caldwell, N. J.
Goleas, E. J., Skokie, Ill.
Grayson, C. A., Dallas, Tex.
Green, J. W., San Antonio, Tex.
Hall, D. R., Edmonds, Wash.
Harvell, H. K., Oklahoma City, Okla.
Hawkes, R. M., Ossining, N. Y.
Hempfling, J. T., Jr., Indianapolis, Ind.
Hiett, R. W., Jr., Manhattan Beach, Calif.
Irons, R. E., Burke, Va.
Kaminski, J. F., Brooklyn, N. Y.
Kanarek, S. S., Kew Gardens, L. I., N. Y.
Kawalek, A. M., Baltimore, Md.
Keck, P. T., Worthington, Ohio
Kersten, E. W., Albuquerque, N. M.
Klee, P. T., Tampa, Fla.
Koci, J. C., Barrington, Ill.
LaMantia, N. E., Woonsocket, R. I.
Landry, R. P., Lawrence, Mass.
Lane, J. T., Plandome, N. Y.
Lane, S., New York, N. Y.
Lautermilch, J. J., Mineola, L. I., N. Y.
Lewis, R. A., Chicago, Ill.
Luckey, R. F., Baltimore, Md.
Ludtke, J. U., Laval des Rapides, Que., Canada
Lum, P. H. P., Lawndale, Calif.
Maki, C. J., Sepulveda, Calif.
Martin, E. J., Fairhaven, Mass.
Martin, S. E., Richmond, Va.
McCarter, K. P., Philadelphia, Pa.
Mertel, H. K., San Diego, Calif.
Miniter, J. J., Richardson, Tex.
Nardo, F. K., East Boston, Mass.
Needham, G. A., Collingswood, N. J.
Neiditz, M. M., Greensboro, N. C.
Niekamp, R. B., St. Louis, Mo.
Norton, W. J., Sarasoto, Fla.
Nost, B., Waltham, Mass.
Olsen, R. T., Dahlgren, Va.
Perez, J. M., Buenos Aires, Argentina
Perryon, P., St. Laurent, Montreal, Que., Canada
Pfarrer, J., Califon, N. J.
Piu, C., Hunghom Kowloon, Hong Kong
Prevedel, H. V., Buenos Aires, Argentina
Ratner, E. Z., Arlington, Va.
Rath, G., Philadelphia, Pa.
Rogers, R. F., Little Compton, R. I.

Roulston, A. M., Winnipeg, Man., Canada
St. George, R. C., Manchester, N. H.
Sandretto, L. J., Winston-Salem, N. C.
Schlachter, L. M., Los Angeles, Calif.
Singh, S., Poona, India
Stevens, H. A., Washington, D. C.
Sutton, R., Brooklyn, N. Y.
Taylor, S. L., Trenton, Ont., Canada
Tejasen, S., London, England
Thompson, J. E., Belmont, Calif.
Tippett, W. D., High Point, N. C.
Van Rhee, L. A., Den Haag, Netherlands
Wallenmeyer, R. L., Biloxi, Miss.
Webster, R. E., Ottawa, Ont., Canada
Zeise, F. F., Needham, Mass.

NEWS New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your IRE affiliation.

(Continued from page 34A)

X-Ray Spectrometer

A new N-1281 X-ray Spectrometer which offers unmatched performance in the energy analysis and a high degree of versatility in the data handling and data presentation aspects of X-ray crystallography is announced by **Hamner Electronics Co., Inc.,** P.O. Box 531, Princeton, N. J.

Noise levels have been reduced to below one kilovolt, allowing the soft X-rays, such as Aluminum Koc, to be resolved with the suitable detection equipment. A system gain stability of better than 0.25% per day and linearity of better than 0.1% provide the user with a measuring system that can be used over long periods of time and over wide ranges of energy without re-calibration.

The system incorporates both a linear rate meter coupled to a recorder for analogue presentation and a high speed printing decade scaler and printing crystal controlled electronic timer for maximum versatility in digital presentation. The scaler-timer combination can also be used to punch paper tape or cards. For detailed information and price, please write to the firm.

Power Transistors

The 2N1651, 2N1652 and 2N1653, a series of Diffused Alloy Power transistors designed for efficient high current (I_c=25 adc maximum) switching at high frequencies is available from **The Bendix Corp., Semiconductor Products,** Holmdel, N. J. A diffused base region provides very low input resistance and high cutoff frequency (typically 2.0 mc.) while maintaining high breakdown voltage (vce=120 vdc absolute maximum rating for the 2N1653). A low input resistance means better circuit stabilization at high temperatures and greatly increases the maximum available gain.

The high frequency, high voltage characteristics of the 2N1651, 2N1652 and 2N1653 DAP transistors are particularly suitable for use as a switch. In addition the flat beta parameter makes it suited as an amplifier.

For further information contact the firm.

Gregory Joins Sonex

Terence Richard Gregory, British-born engineer, has joined **Sonex, Inc.,** Philadelphia 44, Pa., as Chief Engineer. Gregory will be head of research and development.

He is an honor graduate of Wimbledon Technical College and Borough Polytechnic Institute, London, England. Gregory also graduated from the London Institute of Electrical Engineers with post-graduate work accomplished at the Northampton Polytechnic Institute of London. Since coming to the United States, he has continued his advanced education at the University of Pennsylvania.

(Continued on page 158A)

NEWS New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your IRE affiliation.

(Continued from page 157A)

Before coming with Sonex, Gregory held key positions with Hawker Aircraft, Ltd., Avro Aircraft, Ltd., Burroughs Research Center, and Clifton Precision Products, Inc., and until July of this year was a group supervisor at Teledynamics Division of American Bosch Arma.

A specialist in solid state circuitry, he will be responsible for new product development and related research.

Pulse Separator

A telemetering pulse separator for operation with the major, commercially-available, PAM decommutation system was introduced by **Telemetrics, Inc.**, 12927 S. Budlong Ave., Gardena, Calif.

Designated the TPS-100-B, this system is capable of decoding a 100% nonreturn to zero commutated wave train into a standard IRIG return to zero wave train with a high degree of stability and synchronization.

The frame (samples per second) conforms to or extends IRIG standard, operaerating at frame rates from 20 to 7200 pps. The TPS-100-B is designed to operate with systems where information bit channels total 30, 45, 60 or 90 per frame. Some decommutation systems may require

minor modification for use with the TPS-100-B.

Decommutation rate variations of ±20% do not affect system synchronization which also remains normal despite missing pulses from complete loss of as many as 20 consecutive data channels. After 20-minute warmup, the TPS-100-B is stable within 0.20% over an eight-hour period.

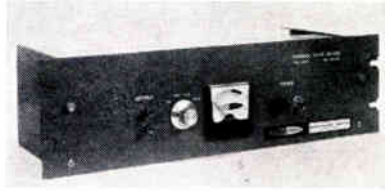
Other specifications: Single-ended input, 3.0 to 20 volts peak-to-peak; linearity within ±0.25% of full scale. Power requirements of +250 vdc at 50 ma, or 12.6 vdc at 900 ma can be obtained from TDS used with the TPS-100-B. Front panel switch makes operational commutation rate changes.

Designed to mount in standard 19-inch relay racks, the TPS-100-B is $1\frac{3}{4}$ inches high; 13 inches deep, plus connectors.

For added information, contact Robert L. Burr at the firm.

Thermal Noise Source

A new laboratory instrument that furnishes a random electrical spectrum with a Gaussian amplitude distribution has been developed by **Western Electro-Acoustic Laboratory, Inc.**, 11789 San Vicente Blvd., Los Angeles 49, Calif.



Designated as the 300C, the product is a laboratory instrument designed for applications such as synthesizing rocket or jet noise spectra, random vibration shake table operation, high intensity noise chamber experiments.

The source of noise is derived from thermal agitation within a cold resistor. This source is extremely stable, dependent only upon magnitude of the resistance and the ambient temperature.

New features of the instrument include a low microphonic feedback, an extended frequency range of more than 15 octaves, including sub-audible, sonic and ultrasonic and a filter network to allow selection of equal energy per cycle per octave. The instrument is ac operated, is readily transportable, mounts in standard racks, or can be used in either a horizontal or vertical position or on any convenient surface. All operating controls are mounted on front panel. A panel meter provides a quick check of critical tube currents. Overall size is 19″ wide, $5\frac{1}{6}$″ high, and $7\frac{3}{4}$″ deep.

Technical literature is available and for more details please write the manufacturer direct.

(Continued on page 160A)

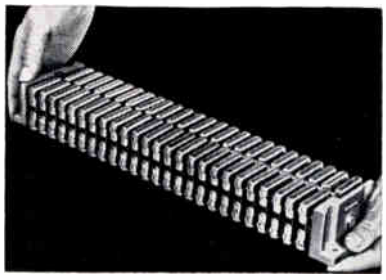
NEWS New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your IRE affiliation.

(Continued from page 158A)

Silicon Rectifier

Modular silicon superpower high voltage rectifier columns capable of delivering up to 1000 watts of power per cubic inch of volume have been announced by **International Rectifier Corp.**, 1521 E. Grand Ave., El Segundo, Calif.



These new rectifier columns incorporate the modular design concept to provide more power per cubic inch of rectifier area than other existing rectifier stack configurations, along with compact size, physical ruggedness and predictable reliability of the highest order. In addition, modular rectifier design insures maximum design flexibility, shortens development time and simplifies procurement cycles.

The columns are available for voltages ranging from 10,000 to 120,000 volts, with current capacity ranges from 1 to 50 amperes.

Applications requiring superpower supplies of this magnitude include long-range radar, television and broadcast transmitters, high voltage dc resistance welders, particle accelerators, induction heaters, pulse modulators and pulse-forming circuitry for plasma research.

The basic rectifier column module is polyester glass board containing two rectifier cells, voltage dividing circuitry, connectors and heat dissipating shield. A standard type 1HV column is made up of 50 basic modules mounted on an 18 inch central beam.

Oscillograph Bulletin

A four-page bulletin containing photos and specifications describes in full the operation of a new, low-cost, portable recording oscillograph developed by the **Electro Mechanical Instrument Div., Consolidated Electrodynamics Corp.**, 360 Sierra Madre Villa, Pasadena, Calif., subsidiary of Bell & Howell Co.

The 5-124 recording oscillograph weighs 40 pounds and is one of the easiest to load and operate of any oscillograph available. Its accuracy and range of usefulness are equal to many of the more elaborate recorders.

Bulletin 5124 is available from the firm.

(Continued on page 162A)

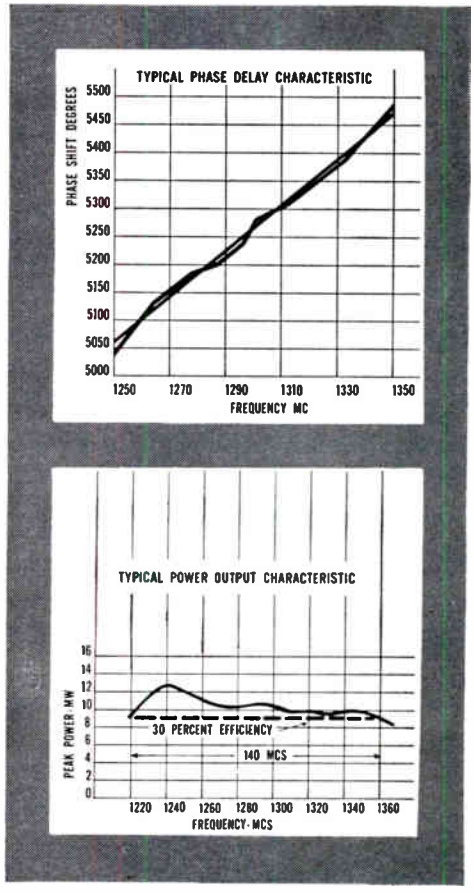
New Broadband Klystrons

140 MEGACYCLES - (1db) BANDWIDTH AT L-BAND
10 MEGAWATTS - PEAK POWER OUTPUT

New additions to the Litton Industries Broadband Klystron family extend broadband performance to even higher power levels as shown in the typical performance curves to the right. These tubes, like all those produced by Litton Industries, are conservatively designed and rated; and rigorously processed to provide many thousands of hours of reliable operation. Using Litton developed broadbanding techniques, it is now possible to achieve wide bandwith, high peak and average rf power output and linear phase shift versus frequency characteristics simultaneously. This latter feature enables the radar equipment designer to utilize pulse compression techniques to attain improved system performance.

Litton Klystrons providing these outstanding performance characteristics can be supplied in both the L and S-bands at peak rf power levels ranging from 2 to 20 megawatts. Typical of the performance obtained with Litton Klystrons is that of the L-3035, a 2.2 megawatt L-band Klystron, whose average operating life in field service is approaching 3,000 hours. Some of these tubes are continuing to provide excellent service after having operated for more than *17,000* hours.

Should you require high power broadband amplifier tubes to satisfy your system requirements, please write to us at Litton Industries, Electron Tube Division, 960 Industrial Road, San Carlos, California. Our telephone number is LYtell 1-8411.



LITTON INDUSTRIES
Electron Tube Division
MICROWAVE TUBES AND DISPLAY DEVICES

"Capability that can change your planning"

NEWS New Products

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(Continued from page 160A)

Voice Transmission

Model 100 Articulator, an entirely new sound reproducing system for transmission of the human voice, particularly from space, has been developed by **Astrometrics, Inc.**, 1108 Santa Barbara St., Santa Barbara, Calif.

The firm points out that recovery of the human voice under conditions of space travel has been a relatively untouched field, sound data from unmanned missile program is now of little value, they stress.

Auxiliary markets for the Articulator are stated to be especially broad. Product is suited for use in any communications system when intelligibility is important i.e.: Military/Commercial airport operational facilities, government listening posts, police, ambulance, any emergency dispatching operation, civilian defense, industrial/commercial paging operations, public address systems, and fleet/field communications.

The new development lets the listener "tune up" the precise sound he wants and "tune down" all other interference. It is designed to increase the intelligibility of the human voice under conditions of a high noise level at (1), listening and (2), transmitting and (3) in transmission link itself. The compact Articulator is added to the ground communication system between the final electrical voice output and the human receiver. Communications systems up to the human receiver can be AM, FM, single sideband, double sideband, narrow band FM, phase modulation, or any other. Communications can be landline, clipped, or digitized and then reconstituted in an analog form.

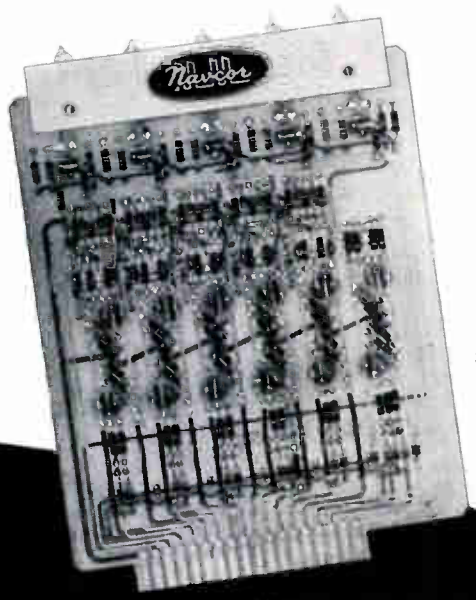
The system is comprised of three separate components: 1) main chassis, housing controls; a 90° phase shifter; two separate audio servosound amplifiers and dc power supply. Physical dimension of cabinet is: 5¼" high×19" wide×13½" deep. 2) Two companion units are identical rack-mounted speaker enclosures positioned at same height, on same plane, with center-to-center distance in the range of 6 to 20 ft. Speakers' size is same as main chassis. All are constructed of Templan with aluminum front panel.

The concept put to work by Astrometrics in the Articulator is that human ears are directional devices, relying on both amplitude and arrival time differences for information. The listener is thus able to locate the exact source of sound he is after—tuning down all other interference. This is attained in the system by feeding all wanted and unwanted signals from a signal channel line into a phase shifter which has the characteristic of presenting two outputs which have a constant phase difference relationship at all frequencies (i.e., all frequencies from 20 to 20,000 cps are 90° apart at the two output terminals). A precise but different time delay from one output to the other results for every individual frequency component in the sound.

Operationally, ninety degrees represents 2.5 milliseconds difference at 100 cps, 250 microseconds at 100 cps, and 25 microseconds at 10,000 cps. If these three frequencies are transmitted by two widely spaced speakers and the 90° phase relationship maintained, the three frequencies appear to the listener to be coming from three different locations between the two speakers.

Each voice has an attack transient containing a band of identifying frequencies. These become locating frequencies in this system. If several voices, hum, and static are all being transmitted over one line, use of the Articulator, its developers say, will make the hum seem to be coming from one point, one voice from another point and so on. User will subconsciously locate the desired sound

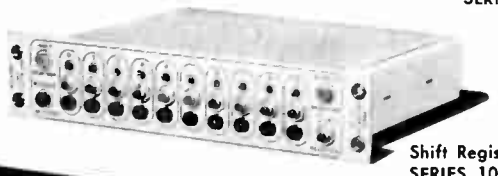
(Continued on page 164A)



5 Stage
Reversible
Binary Counter
SERIES 300

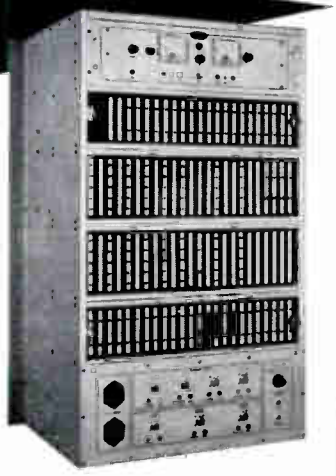
19" Relay Rack Housing
with new
Series 300 5" x 6" modules

Pulse Delay Tri-Unit
SERIES 100



Shift Register Decade Unit
SERIES 100

TRANSISTORIZED DIGITAL SYSTEMS BLOCKS

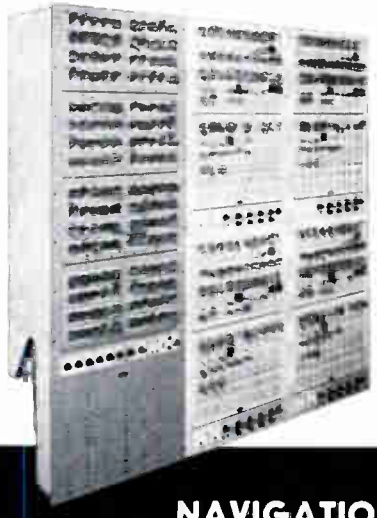


FREE

Send for complete data and specifications on either the 100 Series or 300 Series systems blocks.

Creative engineering by NAVCOR has successfully developed the 100 Series transistorized modules - for digital test equipment and prototype development, and the newer 300 Series card modules - for constructing complete data handling systems. Delivered complete and attractively packaged, these economical systems modules are ready to operate with a minimum of inter-unit wiring.

NAVCOR can engineer and manufacture complete systems to your requirements. Years of experience, devoted exclusively to semiconductor digital systems design, have produced hundreds of thousands of operating logic stages.



GENERAL CHARACTERISTICS

100 SERIES

Time proven 100 Series modules have been used extensively for bench top test equipment and for rapidly building system prototypes. Complete 10 stage BINARY COUNTERS, SHIFT REGISTERS, etc., are attractively packaged in 2¼" x 10½" slide-in units, which assemble into portable cabinets or relay rack housing.

The completely compatible 100 Series transistor circuitry is operable from D. C. to 200KC.

300 SERIES

The completely compatible 300 Series transistor circuitry is operable from D. C. to 300KC and is packaged on 5"x6" glass epoxy cards, with neon indicators and pull handles. There are five stage BINARY COUNTERS, SHIFT REGISTERS, etc. per card.

As many as 1001 bits of logic circuitry may be contained in a single 19" relay rack housing. Gold taper pin connectors facilitate inter-unit wiring.

UNITS AVAILABLE

- PULSE GENERATORS
- PULSE DELAYS
- FLIP-FLOP STORAGE REGISTERS
- SHIFT REGISTERS
- REVERSIBLE SHIFT REGISTERS
- BINARY COUNTERS
- COMPLEMENTING FLIP-FLOPS
- REVERSIBLE BINARY COUNTERS
- BINARY DECIMAL COUNTERS
- PULSE STANDARDIZERS
- AMPLIFIED NOR LOGIC
- COMPARATORS
- ELECTRONIC SWITCHES
- PULSE SORTERS
- LOW LEVEL AMPLIFIERS
- DIGITAL TO ANALOG CONVERTERS
- DIGITAL DECODERS & ENCODERS
- DIODE GATES
- DELAY MULTIVIBRATORS
- INVERTERS, EMITTER FOLLOWERS

NAVIGATION COMPUTER CORPORATION
VALLEY FORGE INDUSTRIAL PARK, NORRISTOWN, PA.
GLendale 2-6531

Navcor

NEWS New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your IRE affiliation.

(Continued from page 162A)

and tune down all interference.

The firm says this, therefore, enhances the ability of the listener to extract the intelligence from a single channel sound transmission system. In effect, he can mentally "tune in" on the voice.

A series of random-number and other tests on listening groups under a variety of ambient listening conditions, recently undertaken by Astrometrics, reveals that average intelligence improvement under conditions of noise in the transmission line is 3 db. A moving airplane would result in a significant range increase of 1.4 to 1. Intelligibility improvement under conditions of ambient room interference is said to be much more noteworthy.

Section Meetings

ALAMOGORDO-HOLLOMAN

"Passive Instrumentation on WSMR," C. W. Williston, Res. & Dev. Section, IRM WSMR. 10/25/60.

ATLANTA

"The Lockheed Jet Star Electronics System," B. E. Montgomery, Lockheed Aircraft Corp. 10/28/60.

"The Use of Microwave Energy to Support High Altitude Platforms," Dr. R. L. McFarlan, IRE President. 11/10/60

BAY OF QUINTE

"Some Observations on Air Traffic Control," Mr. L. Britney, Dept. of Transport. 10/19/60.

BENELUX

"Parametric Amplifiers," B. J. Robinson Radio Observatory. 10/20/60.

BUFFALO-NIAGARA

"Masterminds at Work," John N. Dyer, IRE Vice-President. 10/19/60.

CENTRAL PENNSYLVANIA

"Contemporary Power Supply Developments," O. M. Baycura, IBM Corp. 10/18/60.

"Some Control & Auxiliary Power Aspects of Nuclear Power Plants," C. F. Currey, Westinghouse Atomic Power Dept. 11/15/60.

CHICAGO

"Electroluminescent Displays," I. D. Greenberg, Sylvania Elec. Products, Inc. 10/14/60.

CINCINNATI

"Organs, Past & Present," Al Bissonette, Baldwin Piano Co.; "Electronic Production of Choral Tones," William Wayne, Jr., Baldwin Piano Co.; Movie: Memory Devices-Bell Labs. 9/20/60.

"Fundamentals & Applications of Infra-Red Systems," D. L. Haas, Avco Electronic & Ordnance Div. 10/18/60.

CLEVELAND

"Compatible Single Sideband & AM Stereo," L. R. Kahn, Kahn Res. Labs. 10/13/60.

(Continued on page 166A)

Section Meetings

(Continued from page 164A)

DALLAS

"Project ECHO," J. E. Froehlich, Alpha Corp.; "Project ECHO," R. L. McCreary, Collins Radio Co. 10/27/60.

"Advanced Systems Planning," F. A. Holm, Wright Air Dev. Div., ARDC-USAF. 11/17/60.

EL PASO

"Trends in New Components," John Dunkle, Klictera, Inc.; "IRE, Aims & Operation," C. E. Harp, Dir. IRE Region 6.

FLORIDA WEST COAST

"Saturn—Work Horse of Space," Wernher von Braun, Marshall Space Flight Center, NASA. 11/15/60.

FORT HUACHUCA

"The Polymorphic Principle of Computer Application," D. A. Goodall, Ramo-Wooldridge. 10/24/60.

FORT WAYNE

"Micromodules," William Bentley, RCA 11/3/60.

FORT WORTH

"The Pioneer V Payload Communication System," Y. Shibuya, Space Technology Labs. 10/11/60.

"Semiconductor Electronics," W. R. Savage, Texas Instruments Inc. 10/18/60.

"Transistor & Diode Action & Device Design," R. F. Stewart, Texas Instruments. 10/25/60.

HAMILTON

"Semi-Conductors," Mr. J. Beardall, Rogers Electronic Tubes Ltd. 9/19/60.

"Master Minds at Work," E. C. Forster, Bell Tele. Co.; "The IRE Member & His Obligations," J. N. Dyer, IRE Vice-President. 10/19/60.

HOUSTON

"Theory & Application of Tunnel Diodes," R. S. Foote, Texas Instruments. 10/18/60.

KITCHENER-WATERLOO

"Some Control Aspects of Canada's First Large Scale Nuclear Generating Station," F. M. Foulkes, Atomic Energy of Canada Ltd. 10/17/60.

LAS VEGAS

"Designing Digital Data Systems Around Electronic Counters," Harry Schultheis, Hewlett-Packard. 10/14/60.

LITTLE ROCK

"The IRE Member, His Society, His Responsibilities, & His Future," John N. Dyer, IRE Vice-President. 10/24/60.

LOS ANGELES

"Purposeful Studies of Porpoise Echo Location Leading Exotic Underwater Electronic Navigation & Detection Systems," K. S. Norris, Marineland of the Pacific. 11/1/60.

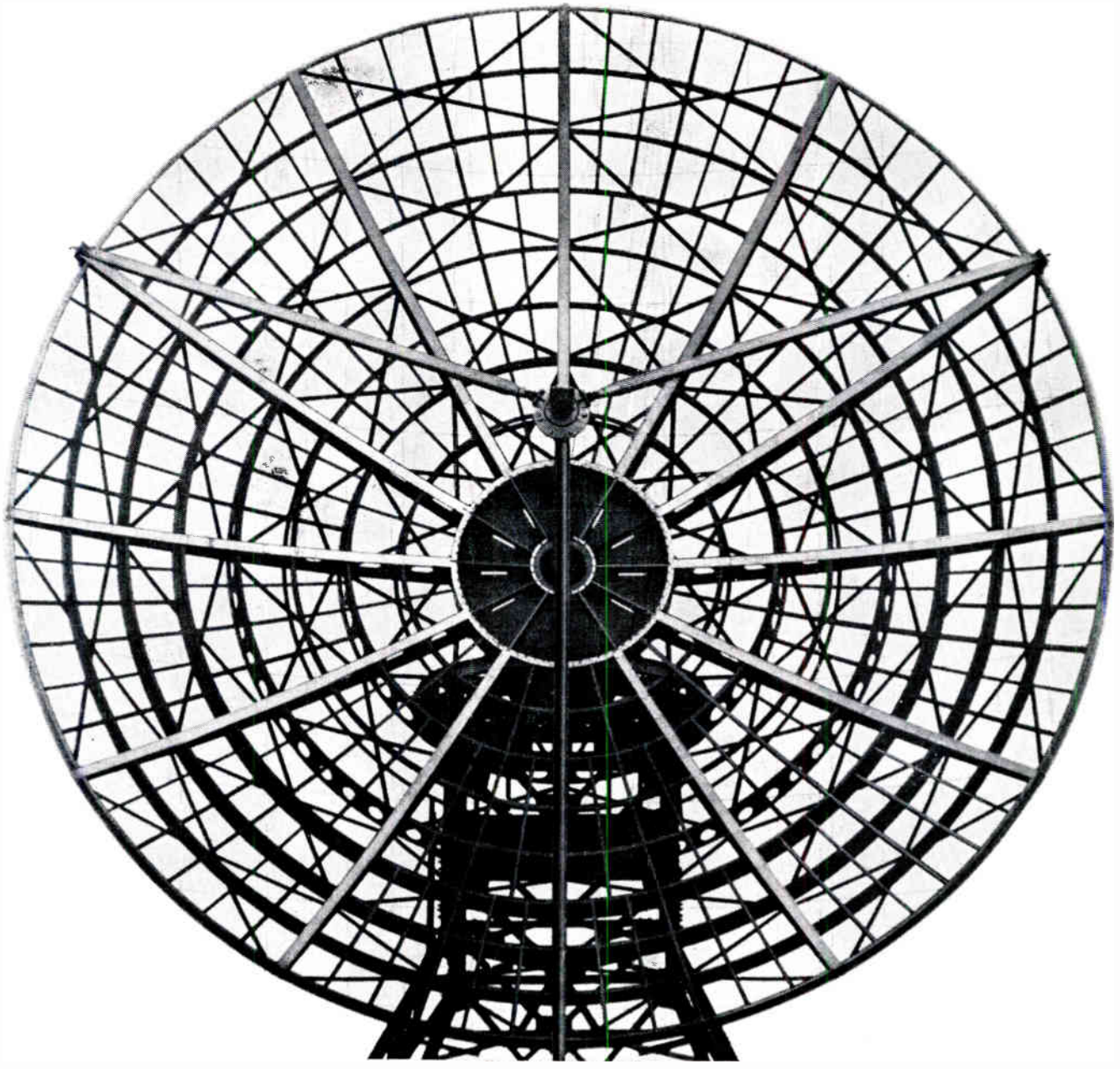
LUBBOCK

"Submillimeter Waves," Harold Spuhler, Texas Technological College. 10/18/60.

MILWAUKEE

"The IRE Member, His Society, His Responsibilities, & His Future," John N. Dyer, IRE Vice-President. 11/9/60.

(Continued on page 168A)



In electronics, you have to look twice at Japan

Japan's capability in electronics is more than pocket radios. It's also communications systems matching in sophistication and reliability those produced anywhere in the world. Microwave systems and multiplex-carrier equipment are two examples. In either, NEC can offer the most advanced systems commercially available. This 60-year-old company is the only one offering microwave systems in all bands, from 800 to 14,000 mc. Capacities go to 2,400 voice channels. Its unique over-the-horizon system, requiring 1/100 of the power of conventional systems, is drastically reducing the cost of this type of link. NEC makes multiplex-carrier equipment for all modes of transmission—wire line, coaxial cable, power line, radio, and microwave. Much of it is completely transistorized, resulting in the world's smallest carrier equipment. This capability in medium- and large-capacity communications systems is what you see when you take a second look at electronics in Japan.

Helping to advance the state of the art NEC *Nippon Electric Co., Ltd.*
Tokyo, Japan

Section Meetings

(Continued from page 166A)

NORTH CAROLINA

Annual Fall Symposium—"The Challenging Sixties," 11/1–11/2/60.

NORTHERN ALBERTA

"Forestry Communication in Alberta," Mr. A. Earnshaw, Dept. of Lands & Forest. 10/18/60.

NORTHWEST FLORIDA

"Radio Meteorological Instrumentation for Eglin Gulf Test Range," V. E. Moyer, A & M Res. Foundation. 8/30/60.

"Transistor Data Sheets," Joe Walston, Texas Instrument Co. 9/22/60.

ORLANDO

"Ballistic Missile Early Warning System," Mr. Sloan, RCA. 10/19/60.

OTTAWA

"The Canadian Topside Sounder Satellite," R. K. Brown, D. F. Page, C. A. Franklin, J. Mar, DRTE Defence Res. Board. 11/3/60.

PHILADELPHIA

Field Trip to Sage Installation, McGuire AFB Wrightstown, N. J. 10/8/60.

"The Challenge of the Deep," B. F. McMahen, RCA-11/2/60.

PRINCETON

"Interception Techniques of Bats," David Cahlander, MIT Lincoln Labs. 10/13/60.

RIO DE JANEIRO

"Raw Materials & General Materials for Communication & Electronics," H. A. Pradal, War Ministry. 10/12/60.

ROCHESTER

"Why Not Put Your Imagination to Work?" W. D. McFadden, Eastman Kodak Co. 10/12/60.

ROME-UTICA

"IRE Role in Medical Electronics," Dr. R. L. McFarlan, IRE President. 10/31/60.

SACRAMENTO

"Space & Such," W. C. Carnahan, Varian Associates. 10/29/60.

"Project ECHO," C. P. Morrill, Jr., Pacific Tel. & Tel. Co. 11/10/60.

"Pulse Code Modulation," D. P. Cannon, Pacific Tel. & Tel. Co. 11/10/60.

ST. LOUIS

"Travelling Wave Tubes & Solid State Microwave Systems," C. L. Cuccia, RCA. 9/20/60.

"Nuclear Electronics," R. D. Alberts. Wright Field Air Dev. Center. 10/18/60.

SAN ANTONIO-AUSTIN

"The Silicon Unijunction Transistor," C. W. Martin, Kelly AFB. 10/14/60.

SAN DIEGO

"Semi-conductors, & Semi-conductor Applications," H. W. Volberg, Straza Industries. 10/5/60.

SCHENECTADY

"Industrial Applications of Silicon Controlled Rectifiers," John Harnden, Jr., GE Co. 11/1/60.

"Intelligence from Outer Space," Su-Shu Huang, Inst. for Advanced Study. 11/15/60.

(Continued on page 171A)

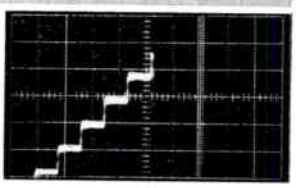
500-TIMES MAGNIFICATION—VERTICALLY

...for detailed waveform analysis

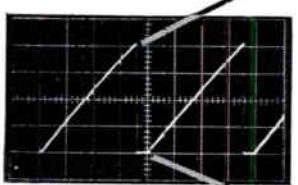
Waveform Details of a 100-v Staircase

Vertical Expansion 500 Times

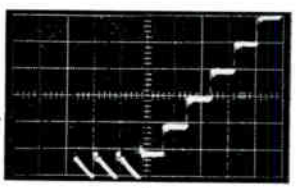
Horizontal Expansion 500 Times



Vertical	Horizontal
50 mv/cm	10 μsec/cm
$V_C = +92.5$	



Vertical	Horizontal
25 v/cm	5 ms/cm
$V_C = 0$	



Vertical	Horizontal
50 mv/cm	10 μsec/cm
$V_C = -5.5$	

TYPICAL APPLICATIONS

FAST-RECOVERY AMPLIFIER—observe small signals riding with large gates.

MODULATION MONITOR—measure amplitude modulation on a digital train pulse.

HIGH-AMPLITUDE HUM REJECTION—reject up to 200 volts peak-to-peak common-mode hum.

SEMICONDUCTOR CHARACTERISTICS—measure Zener diode ac impedance and Zener voltage together, measure transistor output impedance.

PULSE-HEIGHT ANALYSIS—select any pulse above a preset dc level.

COMPONENT MATCHING—check components to easily-interpreted tolerances.

MAIN CHARACTERISTICS

3 Modes of Operation—as a conventional preamplifier, as a differential-input preamplifier, or as a calibrated differential comparator.

50-mv/cm Sensitivity—nine calibrated attenuation steps to 25 v/cm.

Wide Passband—dc to 13 mc with Tektronix fast-rise scopes.

±100-volt Dynamic Range—permits common-mode signals up to 100 volts to be applied to the unit without attenuation.

40,000 to 1 Common-mode Rejection Ratio—allows measurement of differential signals less than 50 millivolts.

Comparison Voltage Accuracy—within 0.25% on the ±1-volt scale; within 0.20% on the ±10-volt scale; within 0.15% on the ±100-volt scale.

Safety Feature—the Type Z eliminates "floating oscilloscope" operation.

AC and DC VTVM—extends oscilloscope accuracy in both ac and dc voltage measurements to 0.2%.

Price, Type Z Plug-in Unit, f.o.b. factory **$525**

New differential plug-in preamplifier rejects up to 100 v of an input signal . . . accepts 100-v waveforms for oscilloscope display at 50-mv/cm sensitivity . . . provides an equivalent vertical scale length of ±2000 centimeters.

You can now display small segments of large waveforms at maximum oscilloscope sensitivity, with vertical expansion equivalent to as much as 500 times. You can select magnified "window" displays of all portions of a waveform, and make amplitude measurements with a degree of accuracy that closely approaches the possibilities of digital techniques. The flexibility and simplicity of the analog (oscilloscope) presentation is retained for accurate analyses of complex waveforms.

The new Type Z Plug-In Unit is a triple-purpose device, acting also as a conventional preamplifier and a differential-input preamplifier. It can be used in all Tektronix Type 530, 540, 550, and *580 Series Oscilloscopes. Ask your Tektronix Field Engineer to demonstrate the dynamic range, waveform resolution, and amplitude accuracy of the Type Z in your application.

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Section Meetings

(Continued from page 168A)

SOUTH BEND-MISHAWAKA

"Parametric Amplifiers," R. S. Engelbrecht, Bell Tel. Labs.; "IRE Policy & Activities," John N. Dyer, IRE Vice-President. 9/29/60.

"Numerically Controlled Machine Tools, "Ray Nynberg, Bendix Products Div. 10/27/60.

SOUTH CAROLINA

"Problems Facing Engineering Education," J. N. Thurston, Clemson College. 10/21/60.

SYRACUSE

"Ballistic Missile Early Warning System," B. P. Brown, GE Co. 10/17/60.

TOLEDO

"The Toledo Valuematic, A Digital Electronic Computing Scale," R. E. Bell, Toledo Scale. 11/10/60.

TORONTO

"Bright Radar Display for Air Traffic Control," T. W. R. East, Raytheon Canada Ltd. 10/24/60.

TULSA

"Thermoelectric Heating & Cooling," A. R. Orsinger, Texas Instruments Co. 9/15/60.

"Electronic Devices Needed in Medical Research," Averill Stowell, Children's Medical Center. 10/11/60.

VIRGINIA

"Helicopter Flight Principles & Electronics Related Thereto," J. C. Mundy, Airlant Avionics. 9/28/60.

"Electronics In Nuclear Controls," A. C. Lapsley, Univ. of Virginia Engrg. School. 10/28/60.

WASHINGTON

"Electrical Methods of Tone Generation & Control," R. White, Kitt Music Co. 9/12/60.

"The Monopulse System—A Precision Tracking Radar," P. J. Allen, Naval Res. Lab. 10/10/60.

SUBSECTIONS

BUENAVENTURA

"In-Flight Physiological Instrumentation at USNMC," F. G. Kelly, USNMC. 10/12/60.

"Refraction of Radar Waves," L. J. Anderson, Smythe Res. Associates. 11/9/60.

EASTERN NORTH CAROLINA

Tour of "Aerotron" Plant, J. S. Hill, III, W. H. Horne, III, W. W. Scott, Worth White, Aeronautical Electronics, Inc. 10/21/60.

MEMPHIS

Tour of the Transmitter Facility, Irby Boyd, WREC-TV. 10/28/60.

MERRIMACK VALLEY

"New Look in Engineering Education," Peter Euas, MIT. 9/26/60.

"Esaki Diodes," G. C. Dacey, Bell Labs. 10/17/60.

MID-HUDSON

"Some Thoughts on Digital Components," Arthur Lo, IBM Corp. 10/20/60.

"Energy Entropy and Micro Electronics," J. J. Suran, GE Co. 11/15/60.

MONMOUTH

"Bell Laboratories Participation in Project Echo," W. C. Jakes, Jr., Bell Tele. Labs. 9/21/60.

"Survey of Advanced Digital Computer Components," R. C. Sims, The Bendix Corp. 10/19/60.

(Continued on page 172A)

PROFESSIONAL CONSULTING SERVICES

Section Meetings

(Continued from page 171A)

ORANGE BELT

"How to Get Out of This World—and Why," H. M. Hanish, Litton Industries. 10/18/60.

PASADENA

"What's Needed in Air Navigation Electronics," A. G. Van Alstyne, Gilfillan Bros., Inc. 10/13/60.

"Underwater Electronic Navigation & Detection Systems," K. S. Norris, Univ. of Calif. 11/1/60.

SAN FERNANDO VALLEY

"Man in Space," Stanley Swals, Bendix Corp., William Benner, McDonnell Aircraft Corp. 10/12/60.

"The Fleet Ballistic Missile Program," Nicholas Brango, Lockheed Aircraft Corp. 11/9/60.

SANTA ANA

"Radio Astronomy—A Window on the Universe," Otto Struve, US National Radio Astronomy Observatory. 10/6/60.

WESTCHESTER

"Some Problems of Space Navigation," Bernard Paiewonsky, Aeronautical Res. Assoc. of Princeton.; "Theory & Applications of Micro-Module Sub-Assemblies," V. J. De Fillipo, Mr. D. Levy, RCA. 6/18/60.

"The Taming of the Sea" (Electronics in Oceanography), L. A. Gregory, Columbia Univ. 9/28/60.

"Project TIROS"—Some Aspects of its Instrumentation, H. I. Butler, US Army Signal Res. & Dev. Lab. 10/27/60.

WESTERN NORTH CAROLINA

Conducted Tour of Duke Power Company's New IBM 707 Computer. 10/28/60.

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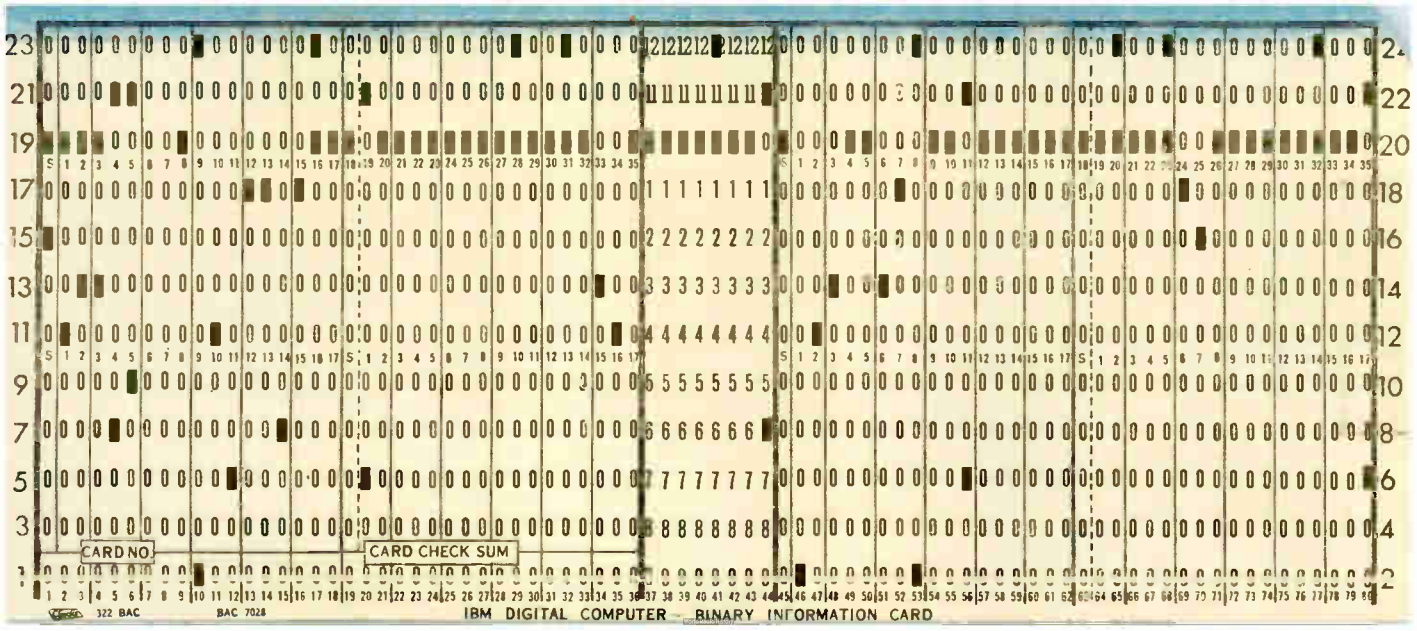
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BAC 7028
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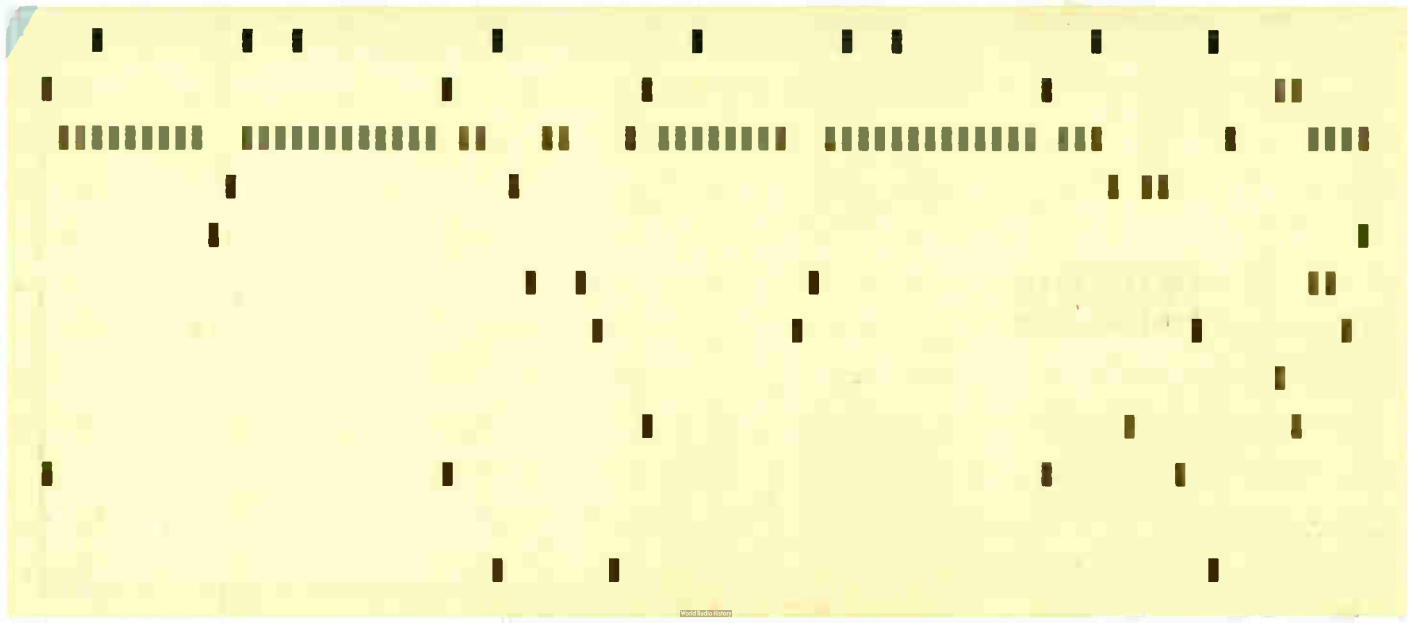

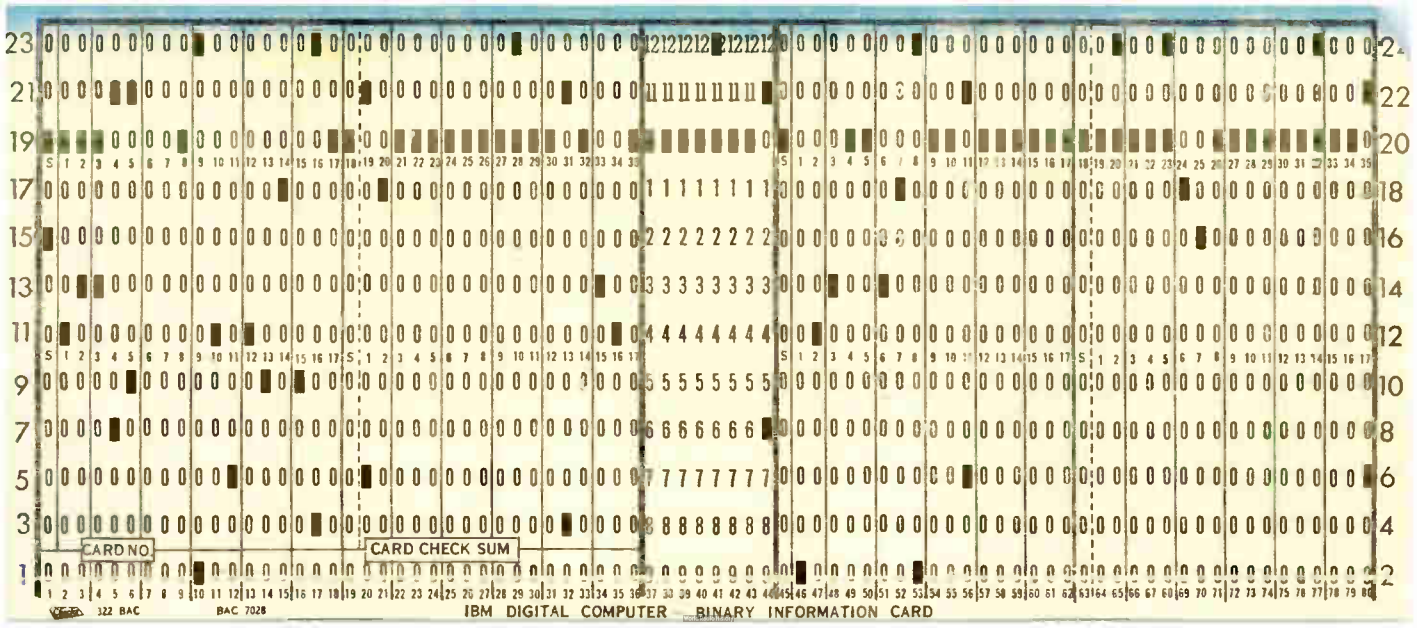
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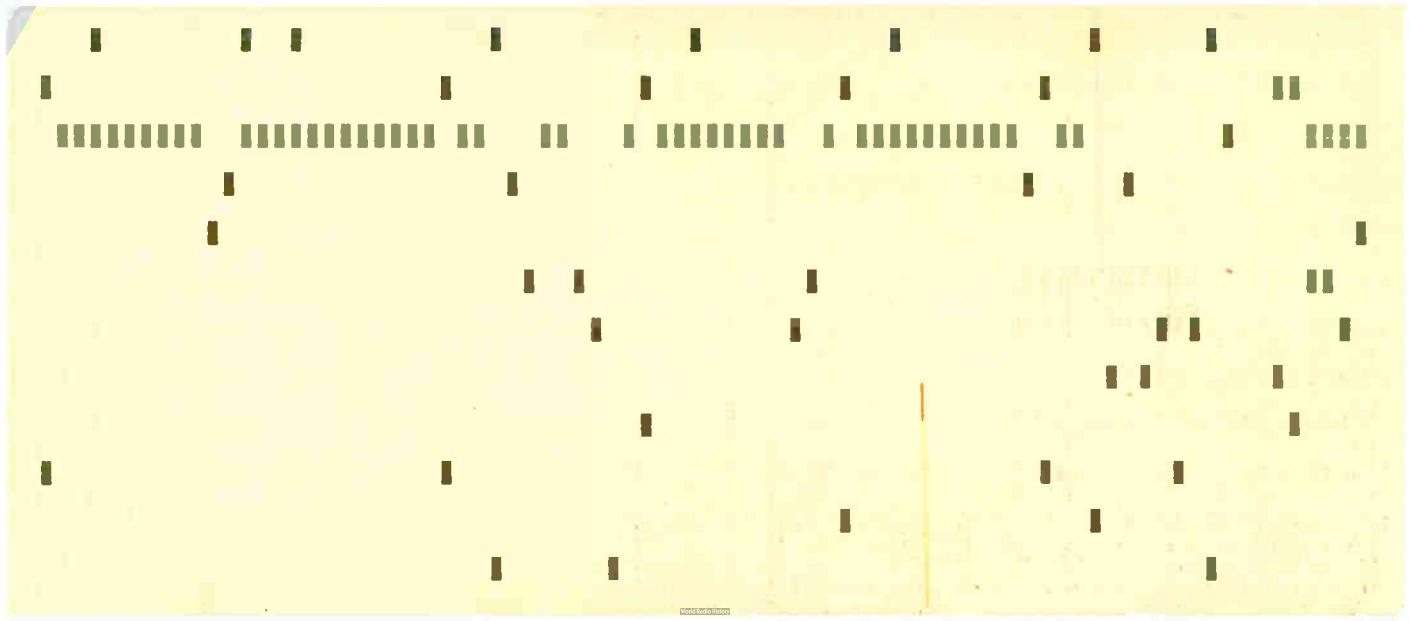

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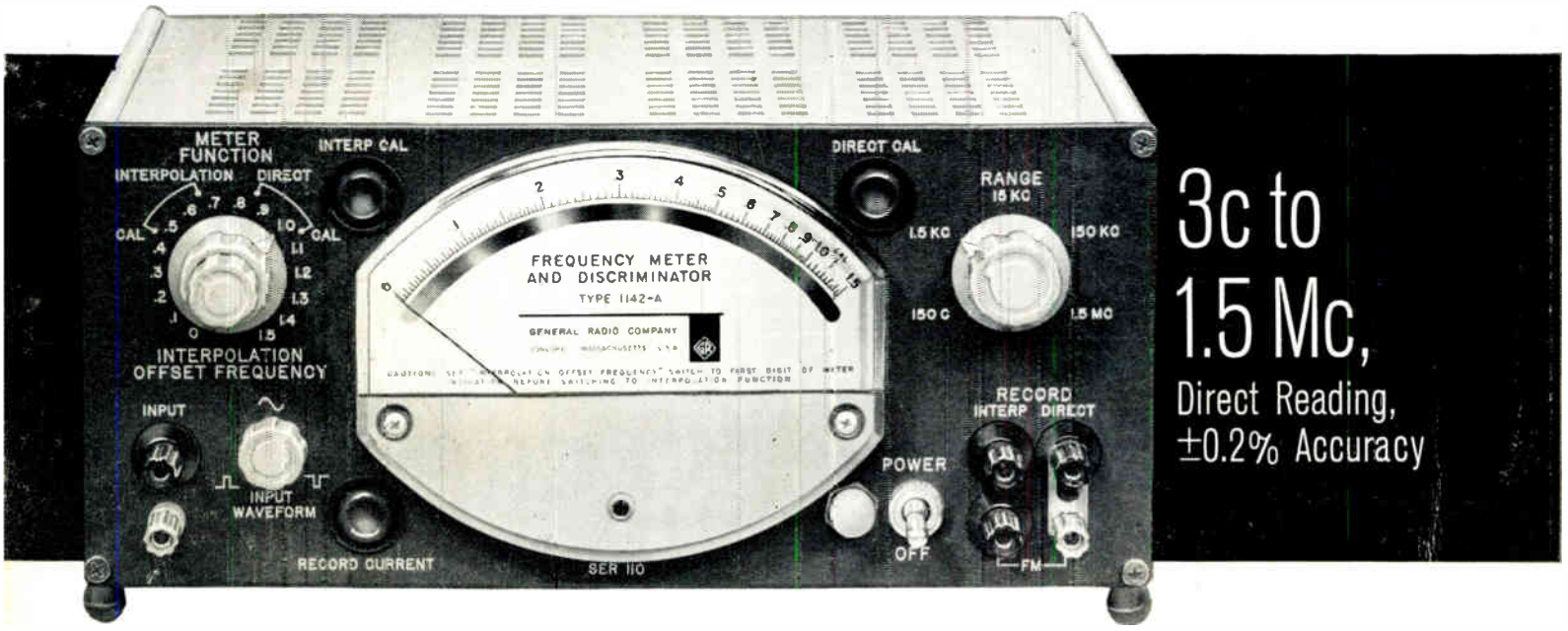

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- Output: 15v, full scale, on all ranges
- Low Noise: Residual fm more than 100 db below full output
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- Adjustable output provides current proportional to input frequency up to 5 ma to drive recorders.
- Interpolator output for high-impedance recorders provides voltage proportional to frequency deviation from preset references.

Type 1142-A Frequency Meter and Discriminator . . . $495

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±0.05% of range setting +0.05% of measured frequency, below 15 kc; ±0.1% of range setting +0.1% of measured frequency above 15 kc

Additional Meter Error:
Direct reading, ±1% above 10% of full scale. Interpolating, ±0.1% of range switch setting.

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2N858	40v	150 mw	0.1 μa	15	75	5 mc
2N859	40v	150	0.1	30	120	6
2N860	25v	150	0.1	15	45	6.5
2N861	25v	150	0.1	30	100	7.5
2N862	15v	150	0.1	20	60	8
2N863	15v	150	0.1	40	120	10
2N864	6v	150	0.1 (6v)	25	125	16
2N865	10v	150	0.1	100	350	24

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