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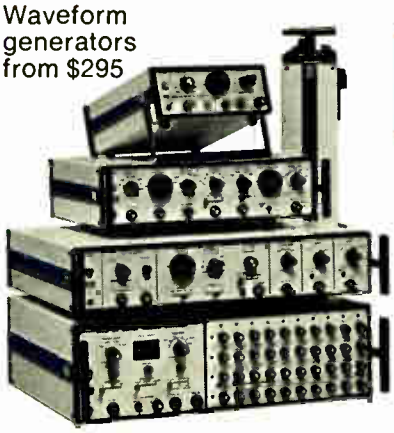

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Forum

Readers are invited to comment in this department on material previously published in IEEE SPECTRUM; on the policies and operations of the IEEE; and on technical, economic, or social matters of interest to the electrical and electronics engineering profession.

Another view on IEEE's role

By the time this letter reaches print, assuming it ever does, the fate of the SST will presumably have been settled by Congress. But the issues raised by Arthur Rubin in "Forum" and responded to by Editor DeWitt in "Spectral lines" (February issue) deserve further attention.

Mr. Rubin urges the Institute to abandon its hands-off policy in regard to political activism, and, in that, I tend to side with him. But the cause he wishes us to be politically active for is another matter, which brings up the question of how IEEE concensuses would be arrived at. Mr. Rubin wants us to fight for the SST primarily because "the careers of literally thousands upon thousands of our members may . . . . . depend upon" continuation of the project.

In our scheme of things, a person is entitled to a share of the product of the economy according to the job he holds or to the capital he owns or both. Since only a small portion of the citizenry owns any productive capital whatsoever, it is not surprising that there is great public support for anything that increases the amount of "work" to be done so that there will be jobs for all. Yet I submit, particularly now that the finiteness of the earth's resources is becoming ever more apparent, that there is something basically absurd about the generation of artificial need and the advocacy of projects whose sole or chief justification is that they make work.

It doesn't take much empathy to feel for those whose access to an income is cut off by a policy decision of Congress, but the message is that we should alter the rules for legitimizing a share of the economy. Our method for dividing up the spoils made a great deal of sense when the efforts of all able-bodied citizens were required to meet subsistence needs. In the "post-industrial" society we find that the goal of full employment leads to featherbedding, planned obsolescence, artificial stimulation of consumer demand, military adventurism, and other forms of nonsensical economic behavior.

If the IEEE is to lobby for anything in this connection, it should be for bringing some rationality to the distribution system so as to make it appropriate to the economic environment that our technology has constructed.

David W. Kean
Techno/culture Associates
Sunnyvale, Calif.

I think that it would be appropriate for the IEEE, AIAA, and SCi to take action in various matters as suggested by Arthur I. Rubin.

The first such action should be opposition to the proposed supersonic transport (SST). If that project is continued, it will be the most expensive white elephant in history. The airlines are in financial trouble, ground transportation is chaotic, long-term exposure to the pollutants on our city streets causes brain damage, and ever-increasing numbers of Americans are destroying their environment at an increasingly rapid rate. The quality of life, and probably the lives themselves, of literally thousands upon thousands of our members now, and in the years to come, may depend on an unfavorable vote by Congress on the SST.

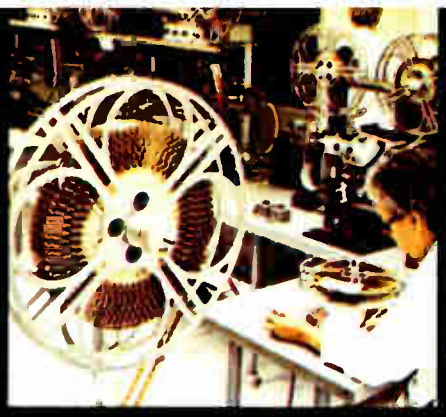
The A-11A and the XB-70 were technical challenges, the SST is only the application of that technology to passenger service. The SST is forward looking only through the tunnel vision of faster for the sake of fastness.

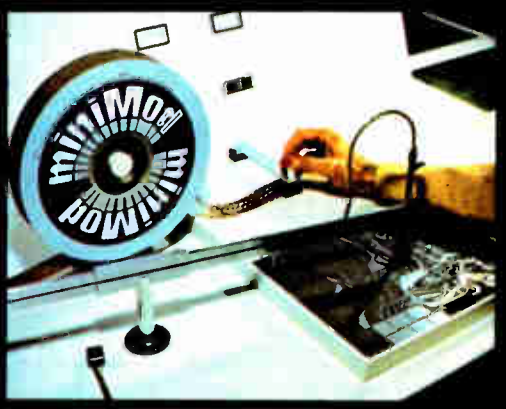
I would encourage your organizations to advance positive arguments for all programs that affect the environment, quality of life, and long-term interests of mankind. The last thing you should do is to preserve the *status quo* for its own sake.

Nolan T. Jones
Winchester, Mass.

Arthur I. Rubin's letter in "Forum" forces me to take part in the debate on the IEEE's function.

1. It is misleading to overemphasize





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The photos above show operation of a miniMod IC mounting system developed for low-volume PC board or hybrid use, a typical miniMod hybrid application and typical high-volume handling equipment. In addition, we've worked with several manufacturers of production equipment, and they're now ready to discuss specific production needs with you.

For more information about GE's new miniMod IC's or how to use them, write General Electric Company, Integrated Circuit Products Department, Section 770-01, P.O. Box 131, Liverpool, New York 13088.

GENERAL ELECTRIC

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the importance of the aerospace/defense sector of the overall U.S. industrial complex. I believe that more engineers are concerned about taxes than about the SST. Most of us could not care less about certain sophisticated ventures bankrolled by the United States Government, except that they be eliminated. And I include the SST—we cannot afford it.

2. The outcry over unemployment in the aerospace industry is amusing. I have yet to hear an outcry about the engineers laid off by the metal, glass, automotive, etc., industry. It is a tragedy to lose one's job. But this tragedy is the same for all. As a taxpayer and engineer, I resent the suggestions that one small segment of my colleagues be given preferential treatment, and this leads up to:

3. Any engineer who joined the aerospace group did receive higher pay than the "common industry" engineer. There are (were?) two reasons for this: (a) high-risk employment and (b) narrow specialization. Now the worst has come to pass, and jobs are vanishing. Why did these engineers think their pay was higher? This is not meant to sound cynical, but the time has come to face the facts.

4. The IEEE is and should be a technical society. Views on current topics of national importance, such as the IBM, should be aired in *IEEE Spectrum*. But we must not let the IEEE become a lobbying organization. The members of the IEEE belong to too many sectors of industry, and it would be unfair to misrepresent their interests.

5. The P.E. organizations could become involved in lobbying, etc. Their function is different.

John A. Fitzgerald
PPG Industries, Inc.
Pittsburgh, Pa.

Engineers' wives speak out

Even if I overlook the condescending language of the write-up in the IEEE Convention booklet, my reaction to the "goodies" that were in store for engineers' wives on the ladies' program was less than enthusiastic.

What brings women together at the IEEE Convention? Largely, the fact that our husbands are engineers. We depend on the engineering industries for the jobs that feed, house, and clothe our families—and right now these industries are putting many engineers out of work. The war in Vietnam, the resultant inflation, and the recession that is an attempt to control this symptom rather than the cause, concern us all. Why were there no sessions on unemployment and what we can do about it, for both men and their wives?

We travel on antiquated mass transit

systems in decaying cities, or we move to the suburbs where our cars add to the pollution produced by the industries we depend on. What are engineers doing about these problems? Wives would love to learn.

Which one of us can be happy when maintaining our living standard depends on our husbands' development of more sophisticated ways to rain death on Asia's war-weary people?

The technology enmeshing us loses sight of the people involved—technical considerations, rather than people's needs, dictate what will be done. The children upon whom we impose this society and whom we educate according to technology's needs, may turn to drugs—so IEEE offered us a lecture on "The Drug Scene."

A more useful and relevant women's program would have been one that attempted to talk about the social implications of technological change. The entire conference would have been far more useful to society if engineers had left their semiconductors and microwave subsystems for three days and talked about where our technology is going, and why.

As women, we can't evade the despoiled environment: we must breathe the same air and depend on the same transportation and communications networks as men. We don't wish to be shunted off with "fashion shows" or a "peek" at Greenwich Village. We needed a public forum at the IEEE Convention to discuss how technology may serve the people, and why the people must stop being its servants. We must give technology a human focus, for the greater good of a greater number of people.

Barbara Marsh
New York, N.Y.

Informing the minorities

In further response to the letters of Dr. Willenbrock, J. B. Ring, and T. M. Kvam in the January 1971 "Forum," I felt it more than imperative that an engineer of a lesser represented segment of our society (Afro-American) should make additional comments on this subject for those engineers who might wish the views of a minority group member.

I am in total agreement with the bulk of Dr. Willenbrock's views, particularly on the blocks (social, educational, economic, or psychological) he mentions that are capable of steering large segments of our society away from fields such as engineering. These blocks are unquestionably most applicable to the minority segments of our society. Because of this I feel it urgently necessary to further make known the desperate need to inform our society's underrep-

resented that they too have an opportunity to become productive members of what they might consider a biased profession. (In my particular case, lack of such vital information and orientation most probably would have resulted in my pursuing a career in public school teaching, rather than engineering.)

I believe encouraging programs that will better inform minority groups of the various career opportunities in the field of engineering will not result in giving them special advantages, but can make them positively aware of the tremendous career opportunities, available to any serious and industrious individual regardless of his color, race, or national origin. (Programs such as that instituted by the Berkeley Student Branch of IEEE could be very instrumental in remedying the educational and psychological blocks as mentioned by Dr. Willenbrock.)

I, therefore, feel that it is particularly necessary for IEEE to make known that it sanctions all constructive efforts at encouraging minority group members to pursue careers in engineering. I suggest this not just to help right some of the many imbalances in our society (as mentioned by Dr. Willenbrock and perhaps the only portion of his article about which I hold a different view), but to allow the United States to greatly benefit from what is probably a wealth of unknown and unduly suppressed talent.

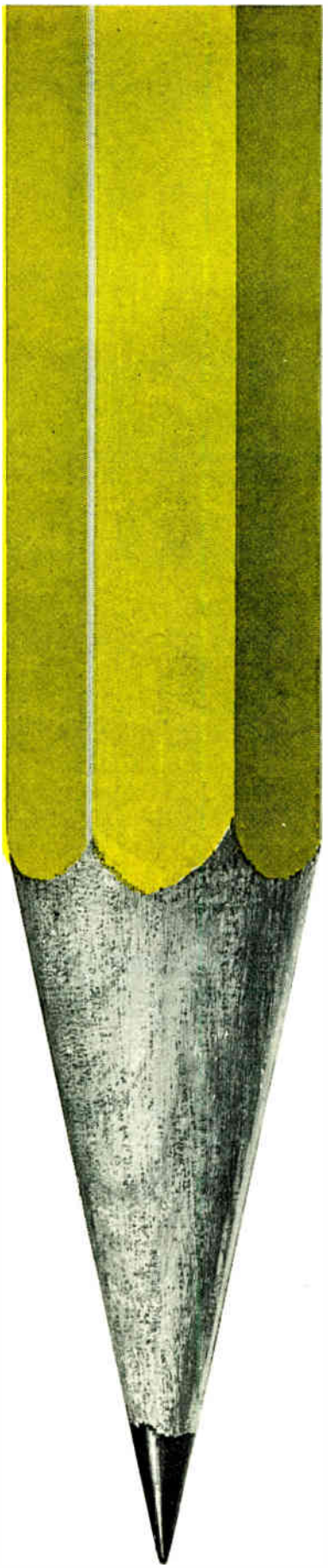
Lawrence E. McCrary
Emerson Electric Co.
St. Louis, Mo.

Radar set parts needed

The United States Air Force Museum at Wright Patterson Air Force Base desires components of radar set SCR-270B for their Ground Radar Exhibit. It is intended to reconstruct the radar operator's positions in a simulated section of the SCR-270B operating van as it existed at the time of the detection of the Japanese attack on December 7, 1941, at Pearl Harbor, Hawaii. Two important components for the exhibit are the BC-403 oscilloscope and BC-404 receiver. Additional components desired but not so essential are radio transmitter BC-405, water cooling unit RO-3, and keying unit BC-402.

Difficulty has been encountered in locating these components through Air Force agencies, movie studios, and surplus sources. Information covering the location of these components will be greatly appreciated. Persons knowing such information please contact John E. Cruickshank, RADC (Rome Air Development Center), Griffiss Air Force Base, Rome, N.Y. 13440.

Idea Machine



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Spectral lines

A question of priorities. The IEEE Technical Activities Board is conscious of the fact that IEEE should be more meaningful to society and has initiated steps to increase the relevance of its activities. Although there is a basic willingness for the IEEE to change its point of view and to try to be more responsive to society's needs, so much time and effort are required to accomplish this that the results may not be apparent to society or even to our members.

Further, it is by no means clear that there is any single "best" thing to do to achieve desirable and meaningful results. Rather, there are many things that must be done, and the accomplishment of several worthwhile objectives does not eliminate the necessity for continuing efforts to attain the goals that remain. It is important to place higher on the list of priorities for technology the needs of society rather than simply to emphasize our skills and expertise. Those of us responsible for the direction of IEEE's technical activities have been working hard to bring about this reordering of priorities, both in the IEEE and in the outside world in which we all live. Without question our labors would be benefited by help from more of our IEEE members, and we are grateful for your ideas and assistance.

Technology's place in the social system is a changing one. For years technological advances were brought forth for the people of the world to marvel at and to use. These developments—of electric power and communication, of transportation and automation, of information handling and entertainment—have so grown in magnitude and pervasiveness that they tend to dominate today's world.

Now, with a broader range of alternatives from which to choose, society is reodering its priorities and coming up with new needs. It has become apparent that such conditions as quiet, clean air and clean water, and freedom of choice may have subjective values that override technical novelty and achievement.

The following are examples of ways in which the IEEE is beginning to interact with the outside world.

1. At the local level of a city, county, or IEEE Section, IEEE members are being encouraged to work on problems of unemployment, education, traffic control, and information for government and hospitals. Joining with persons proficient in many disciplines and having different responsibilities, our IEEE members are serving as skilled citizens to define problem areas and plan solutions.

2. At the national level of a country, IEEE members are instituting conferences with other disciplines to discuss national goals and priorities. Such meetings serve to bring together people with various technical and nontechnical skills and to highlight the national needs as viewed from many different disciplines. Environmental quality, energy requirements, transportation, employment, education, and medicine are typical of some of the problem areas that are being considered. From such conferences a clearer understanding of the tasks that involve engineers should emerge.

3. At the international level, there is an increasing concern for the world's environment, resources, and human wants. The magnitude of the problems at the national level emphasizes the need for multinational, transnational, and international approaches to these challenges to society. Through United Nations meetings as well as international conferences sponsored in many countries of the world by IEEE and other organizations, more IEEE members are being encouraged to devote their ideas and energies to learning about and helping to satisfy the world's needs. At home, too, progress is being made. In this respect, we can cite such examples as the efforts of John R. Whinnery, who initiated the establishment of the IEEE Committee on the Application of Electrotechnology to Society, which is currently chaired by W. E. Cory. Other groups in the IEEE dedicated to attacking these problems at the national and international levels are the Committee on Transportation under Arthur Goldsmith and Bernard Manheimer's Committee on Environmental Quality, which was started by Edward Wolff.

4. The problem of assisting developing countries with their technological growth and skills is another area in which social needs are influencing IEEE activities. In some countries, such as Mexico in Region 9, IEEE Student members and others are serving on committees to help with rural electrification projects. Some members of the IEEE Computer Society and Control Systems Society have assisted the U.N. in preparing a report on the "Application of Computer Technology for Development." Other IEEE Groups and Societies also may have opportunities to contribute in the application of their technical expertise to the problems of developing countries.

With more than 165 000 members, it would appear that IEEE can do more than advance the cutting edge of technology through our publications and conferences. We are looking for new and more effective ways to be more helpful to our members and to society. We welcome your suggestions and support.

Harold Chestnut
Vice President, Technical Activities

Threshold logic

Not only do threshold-logic designs have the edge over conventional Boolean realizations in terms of reduced numbers of components and improved power and speed, but these versatile gates are also compatible with LSI technology

Daniel Hampel *RCA Advanced Communications Laboratory*

Robert O. Winder *RCA Laboratories*

A threshold gate has binary inputs and outputs just like any other logic gate. The difference, however, is that in the threshold gate the inputs may be weighted and, eventually, a binary decision made as to whether the total weight is more or less than some reference. This principle of weighting and summing the inputs rather than simply noting the presence of all inputs as high (as in an AND gate) or one input high (as in an OR gate) is the reason that a threshold gate can tell more about the state of the inputs, thus providing greater "logic power." This article gives some examples of the applicability of threshold logic, as well as an integrated-circuit approach for building arrays of versatile threshold gates. In addition, some logic designs are described and compared with conventional ECL implementations.

The concepts underlying threshold logic can be readily understood by referring to Fig. 1, which illustrates both the principle involved and the logic representation for a typical gate. This article will be concerned with the fundamental approach to threshold-logic circuit design, performance, and application. Fortunately, a large amount of theory has evolved that is concerned with the types of functions that any single (or multiple) threshold gate can realize, as well as how best to realize any given function with threshold gates.[1–4]

This article is based upon work that was partially sponsored by the United States Air Force Avionics Laboratory, Wright-Patterson AFB, Ohio.

Threshold gates

In the threshold gate symbolized by Fig. 1(A), the number associated with each input is called the "weight" of that input, with the number T within the gate itself indicating the "threshold." As a result, the output of the gate will be high if the total sum of the weighted inputs is equal to or greater than the predetermined threshold; otherwise, the output will be low.

It is relatively simple to arrive at the function that a particular gate realizes. First, write down the expressions for all single combinations of the inputs (which, by definition, will be high if they produce a weighted sum equal to or greater than the threshold T) and create an OR expression F from these products. Next, either by Boolean algebra, Karnaugh mapping, or N cubes, simplify the overall expression. In general, the threshold of an n-input gate can be anywhere between 1 and n, the former case being equivalent to an OR gate, the latter an AND gate. The case where $T = (n + 1)/2$ is referred to as a "majority" gate.

Even the relatively simple gate of Fig. 1(B) demonstrates the power of threshold logic. This majority gate provides a function that would otherwise require three to four conventional Boolean gates—i.e., a NAND gate or OR/NOR gates. If the complexity of this gate were three to four times that of the conventional gate, much of the remaining material in this article would be only of academic interest. However, as will be seen later, this is not the case.

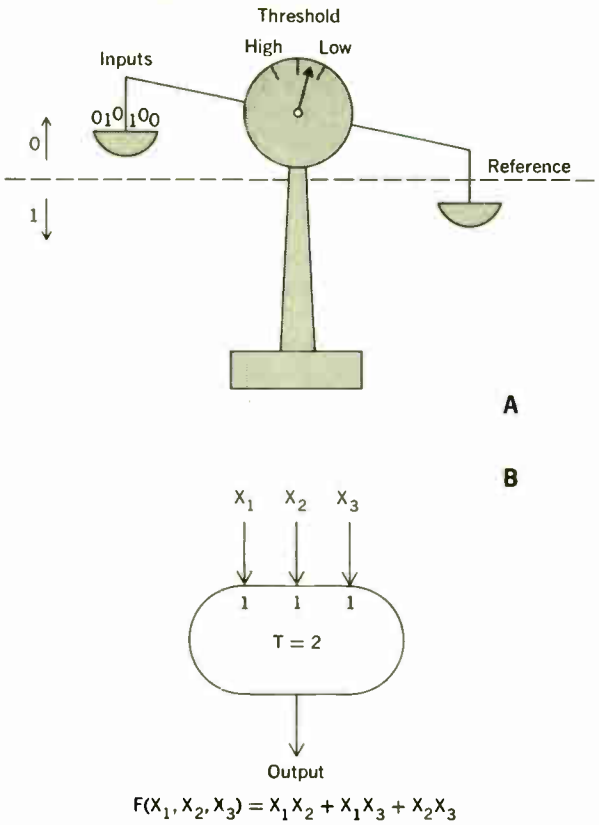


FIGURE 1. A—Principle of threshold logic. B—Example of a relatively simple threshold gate.

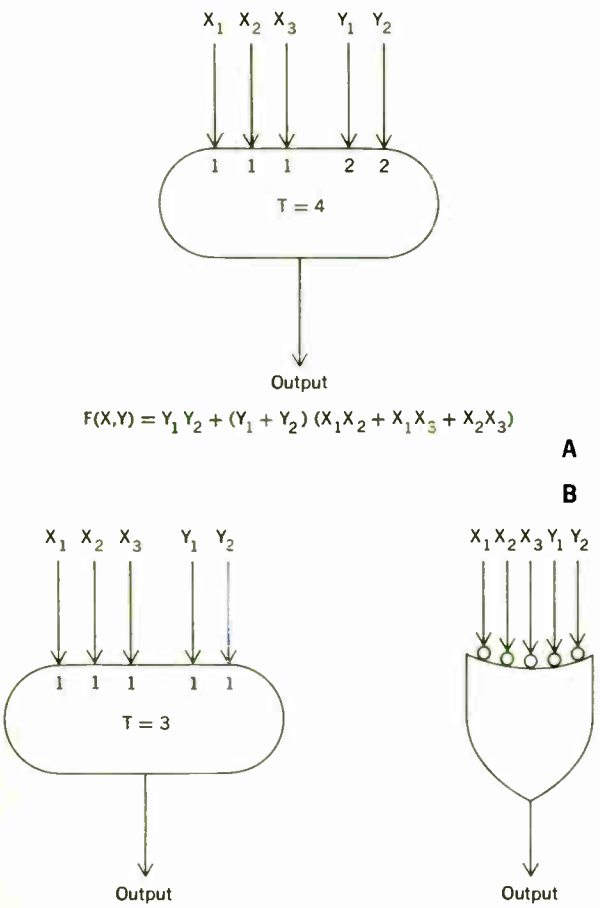


FIGURE 2. A—Example of threshold-gate flexibility. B—Example of threshold-gate versatility.

The problem of proceeding from a function to its threshold-logic implementation is more involved, especially if the function cannot be realized with a single threshold gate. However, design procedures are now available that can be used by the logic designer who is accustomed to using only Boolean gates.[3,5] Moreover, all the realizations of functions up to four variables have already been catalogued.[6] In addition, a formidable library of designs has evolved for frequently used functions, and controls can be added to these to suit particular applications.

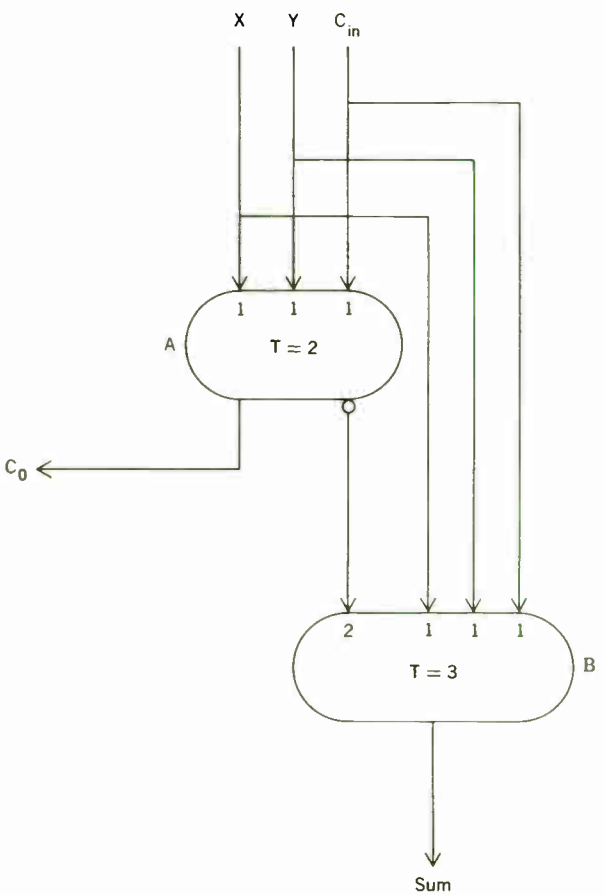
To illustrate an important characteristic of threshold gates, consider the gate of Fig. 2(A). If Y_1 is tied to a constant high level and Y_2 to a constant low level, then the output of the gate is the same as that of Fig. 1(B). By tying one of the double-weighted inputs to a single-weighted input, the resulting four-input gate (3, 2, 1, 1, $T = 4$) is equivalent to a (2, 1, 1, 1, $T = 3$) gate, which demonstrates the flexibility of these gates.

An illustration of the versatility of threshold gates is given in Fig. 2(B). Here, the Y inputs can be considered

I. Function versatility of threshold gates

Y_1	Y_2	Output Function	Gate
0	0	$X_1X_2X_3$	AND
0	1	$X_1X_2 + X_1X_3 + X_2X_3$	majority
1	0	$X_1X_2 + X_1X_3 + X_2X_3$	majority
1	1	$X_1 + X_2 + X_3$	OR

FIGURE 3. Threshold-gate realization of a full adder.



II. Use of weighted inputs in a common two-gate design

Inputs High Among X, Y, C_{in}	Σ Weights in Gate A	C_0 (2-out-of-3) Gate	$\overline{C_0}$	Σ Weights in Gate B	Sum (3-out-of-5) Gate
0	0	0	1	2	0
1	1	0	1	3	1
2	2	1	0	2	0
3	3	1	0	3	1

to be control lines, with Table I showing the output as a function of the control-line states. In effect, different thresholds are realized as far as the X inputs are concerned. By contrast, a conventional Boolean gate with control inputs always computes the same function of the input variables: hence, the output of the NOR gate in Fig. 2(B) is always the NOR of the inputs.

An example of a common two-gate design—the full adder—is shown in Fig. 3. Gate A gives the carry-out function for the three inputs to the adder. The complemented carry-out signal-feeding gate B (2, 1, 1, 1, T = 3), which also receives the three inputs, gives the sum. Table II demonstrates why.

Threshold logic, then, involves gates that have weighted inputs and an internal threshold that, in effect, marks the boundary between high and low outputs. The circuits for accomplishing this will be described in the next section.

Threshold gate circuitry

The functions common to any circuit implementation of a threshold gate are those of *summation* and *decision*. In this capacity, digital inputs are summed (in accordance with their weights) and a binary decision with respect to a reference is made at the summation point. This decision can be made within the gate itself so that a pure binary output is produced, or it can be made within the input circuit of a succeeding gate. In the latter case, the output is somewhat analog in nature. In fact the threshold circuit is a form of digital-to-analog converter in which only the levels in the immediate vicinity of the reference (the threshold) are of interest. A functional block diagram illustrating the principle of such a gate is given in Fig. 4.

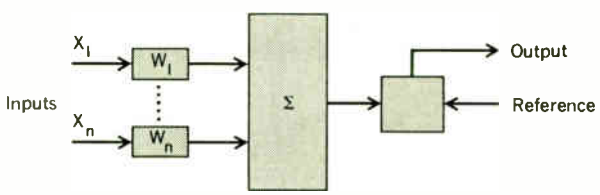
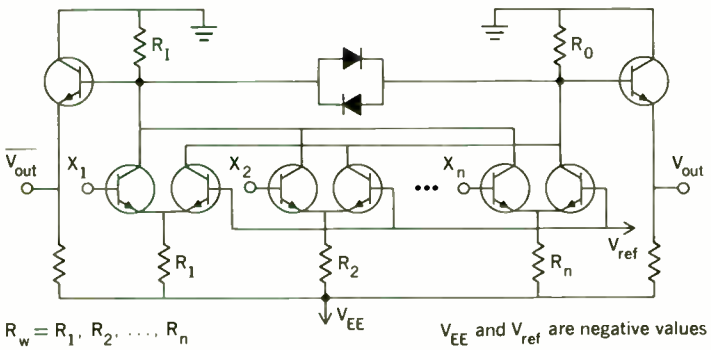


FIGURE 4. Block diagram of a threshold gate.

FIGURE 5. Schematic of a threshold gate suitable for LSI.



The problem, therefore, amounts to designing useful threshold gates that are consistent with the limitations and natural features of LSI technology.[5,7–9] This has been done in the circuit approach of Fig. 5. Each input feeds a differential switch that serves the dual purpose of (1) deriving a weighted current (by virtue of a determining resistor R_n) and (2) making a binary decision as to the state of the input (whether it is higher or lower than the reference). In this circuit the input side currents are summed and produce a voltage across R_0, and the reference side currents are similarly summed and produce a voltage across R_1. The sum points feed emitter followers, which provide drive capability and reestablish compatible input levels to succeeding input circuits.

Each input that is above the reference draws a number of units of current through R_0, the number of units or weight of the input being determined by the emitter resistor R_n for that input. Each input that is below the reference draws its units of current through R_1. The values of R_1 and R_0 are chosen so that T unit currents are necessary before the output of the emitter follower drops below the reference. The gate must do this over a large temperature range and without stringent power-supply and resistor tolerance requirements.

Circuit design

Let n equal the number of inputs to a gate, and let all inputs have unity weight and count each input with a weight $P > 1$ as P inputs. All emitter resistors are R_w, a value that gives a weight of 1. Also, let m equal the number of inputs that are "high," $(n - m)$ equal the number of inputs that are "low," and T equal the desired threshold of the in-phase output; $V_{out} = V_{ref}$ if $m = T - \frac{1}{2}$. Then

$$V_{out} = I_w R_1 (n - m) - V_{be} \tag{1}$$

where

$$I_w = \frac{(V_{EE} - V_{ref} + V_{be})}{R_w}$$

$$V_{out} = \frac{(V_{EE} - V_{ref} + V_{be})}{R_w} R_1 (n - m) - V_{be}$$

$$V_{out} = (V_{EE} - V_{ref}) \frac{R_1}{R_w} (n - m) - V_{be} \left[1 - \frac{R_1}{R_w} (n - m) \right] \tag{2}$$

Setting V_{out} equal to V_{ref} by making $m = T - \frac{1}{2}$,

$$V_{ref} = - V_{be} \left[1 - \frac{R_1}{R_w} \left(n + \frac{1}{2} - T \right) \right] \tag{3}$$

$$(V_{EE} - V_{ref}) \frac{R_1}{R_w} \left(n + \frac{1}{2} - T \right)$$

For independence of V_{be} variation with temperature, we let

$$\frac{R_I}{R_w}\left(n + \frac{1}{2} - T\right) = 1 \qquad (4)$$

Substituting (4) into (3),

$$V_{\text{ref}} = V_{EE} - V_{\text{ref}}$$
$$V_{\text{ref}} = \frac{1}{2} V_{EE} \qquad (5)$$

Hence, with the reference at half the power supply value, as well as basically easy to derive and distribute, and with the ratio of

$$\frac{R_I}{R_w} = \frac{1}{n + 1/2 - T}$$

the output of an n-input gate will be centered about the reference for any desired threshold T, independent of temperature and absolute resistor values. Thus the attributes of LSI have been capitalized upon and the effects of its limitations have been eliminated.

The flexibility of this circuit approach lies in choosing an R_I that results in a threshold from 1 to n for an n-input gate. From Eq. (4), we derive Table III. Note that by making the R_0 sum resistor the same value as R_I, the $\overline{V_{\text{out}}}$ signal is the complemented dual function of the V_{out} signal. For the three values of T shown in Table III, $\overline{V_{\text{out}}}$ would represent NAND, majority, and NOR functions, respectively. With constant current sources for each switch, R_0 is identical to R_I; otherwise R_0 is made slightly smaller to account for the higher current produced by an input over that of a reference side transistor.

The cross-coupled diodes in Fig. 5 perform a clamping of the sum-point signals that is limited to excursions immediately about the reference where the 1,0 decision is made. In so doing, all the analog information except that of importance is destroyed. Otherwise the sum-point levels could get so high as to saturate succeeding-stage input transistors or so low as to saturate the transistors of the gate itself.

III. Use of R_I in choosing a threshold

T	R_I	Gate
1	$\frac{2R_w}{2n-1}$	OR
⋮	⋮	
$\frac{n+1}{2}$	$\frac{2R_w}{n}$	majority
⋮	⋮	
n	$2R_w$	AND

IV. Signal swings for majority gates

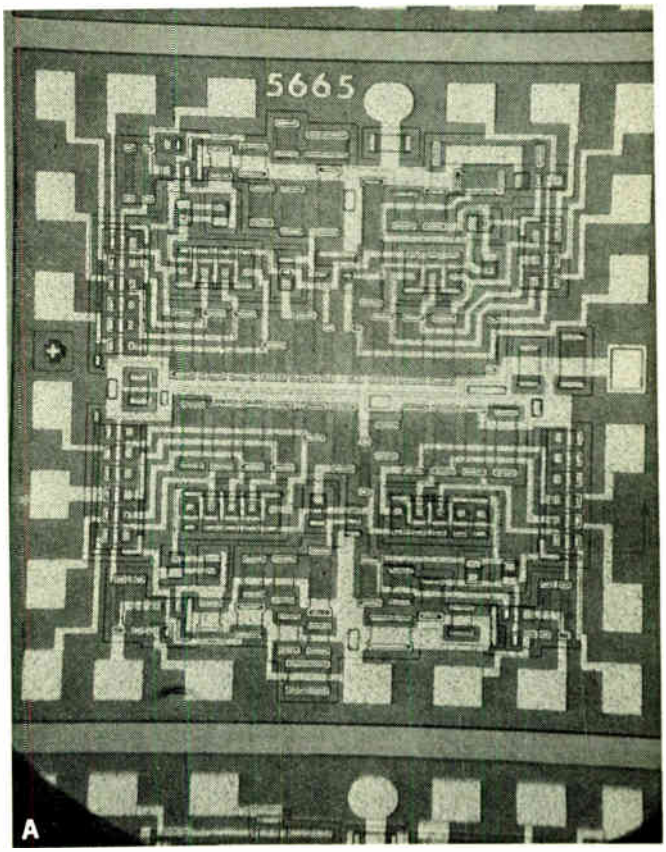
N	Signal Swing About V_{ref} for: $V_{EE} = -4$ volts	$V_{EE} = -5$ volts
3	±400 mV	±575 mV
5	±240 mV	±350 mV
7	±170 mV	±250 mV

Circuit performance

For a fixed power-supply and unit current (or R_w), the threshold gate's minimum output swing about the reference will depend on the number of inputs and the threshold setting. This provides a measure of the noise immunity and latitude in worst-case resistor ratio effects. As seen in the expressions for R_I in Table III, for a given fan-in the signal swing is lowest for OR and highest for AND; in the latter case, this signal swing is independent of n. Signal swings for gates with thresholds set at their majority value ($R_0 = 2R_w/n$) are given in Table IV ($V_{\text{ref}} = V_{EE}/2$; $I_w = 2$ mA). These swings (and even lower values) are deemed quite adequate for operating succeeding threshold gates in the relatively noise-free environment within a current-mode circuit array, where the reference in fact tracks with the power supply and temperature effects are eliminated.

Among the several types of threshold gates that have been successfully integrated are 3- and 5-input majority gates. A microphoto and a schematic diagram of a chip

FIGURE 6. Microphotograph and diagram of a four-gate dual-adder chip.



that contains four gates (integrated with 500-MHz transistors) are given in Fig. 6. It is possible to perform "OR-ing" with these gates, not by designing for a $T = 1$, but by simply paralleling input transistors on any input switch; an example is given in Fig. 7. Here, a switch resembles the basic module of a conventional ECL gate, groups of which are then superimposed for the threshold gate. In this manner, the capability of OR/threshold logic (OR/majority, OR/AND, etc.) is realized.

Design examples

As previously mentioned, there has been considerable practical logic design using threshold gates. Such designs include arithmetic units, multipliers, parity circuits, registers, and counters.[10]

Figure 8 shows an adder that has been modified with control inputs to perform three other functions generally useful in an arithmetic unit. The circuit, one stage of an arithmetic unit with inputs X_i, Y_i, C_{i-1}, can perform the functions listed in Table V under control of three signals K_1, K_2, and K_3. In the first case, K_1 and K_2 being of opposite value, the carry-out signal is propagated and the circuit function is the standard two-threshold-gate adder.

In condition 2, the carry-out is forced to 0 since K_1 and K_2 cause the output to respond to $X_i + Y_i$. In condition 3, the carry-out is forced to 1, causing the output to respond to X_iY_i. Finally, in condition 4, the carry-in is overidden by K_3 and the circuit effectively responds to $X_i \oplus Y_i \oplus 1 = X_i \oplus Y_i$. This example illustrates the versatility of control inputs with these threshold gates.

The comparison with ECL in this case is even more advantageous for threshold logic. Each control function normally requires a gate, but in threshold logic an additional input switch or transistor does the job.

As a further example, examine an adder that sums three binary numbers at once (Fig. 9). Assuming "carry ripple," each stage has three bit inputs and two carry inputs, and provides two carry outputs and a sum output. The threshold-logic design consists of three gates, as shown in Fig. 9. A conventional ECL realization, however, would require 21 gates.

In the circuit design example, a power supply of -4 volts was assumed and the output levels were centered about -2 volts. To maintain compatibility with ECL, which is centered at -1.2 volts, three choices are possible. If the power supply were -2.4 volts, the output would be automatically compatible, but the gate would not have enough signal swing for all but the highest threshold setting—the AND gate. Alternatively, the summing resistors could be returned to a positive supply V_{CC} (instead of ground), and V_{EE} could be lowered to keep the power constant so V_{ref} is -1.2 volts. Finally, simple level-shift circuitry could be used, which would consist of a single switch with a special load resistor that could convert input and output signal levels in accordance with exact ECL requirements. The latter approach has been used in an integrated-circuit demonstration vehicle. Overall advantages in an array of threshold gates with these level shifters are not significantly altered, since the shifters can perform a stage of OR logic in the process of converting levels.

Refinements for improved "logic power"

Recalling the circuit of Fig. 5, keep in mind that R_I and R_0 are nearly equal, restricting the two outputs to the role of complementary duals of each other. Also, the collector-to-collector diode clamp in this circuit sets the output voltage limits symmetrically about the threshold since $R_I \approx R_0$. If, in a particular application, however, the collectors can be independently clamped, it is possible to have independent values of T for the two outputs by selecting unequal values for R_I and R_0. Figure 10 describes a full adder that performs the same function as Fig. 3 (with a reduced component count) by the use of unequal summing resistors, and by using

FIGURE 7. OR-ing in conjunction with threshold logic.

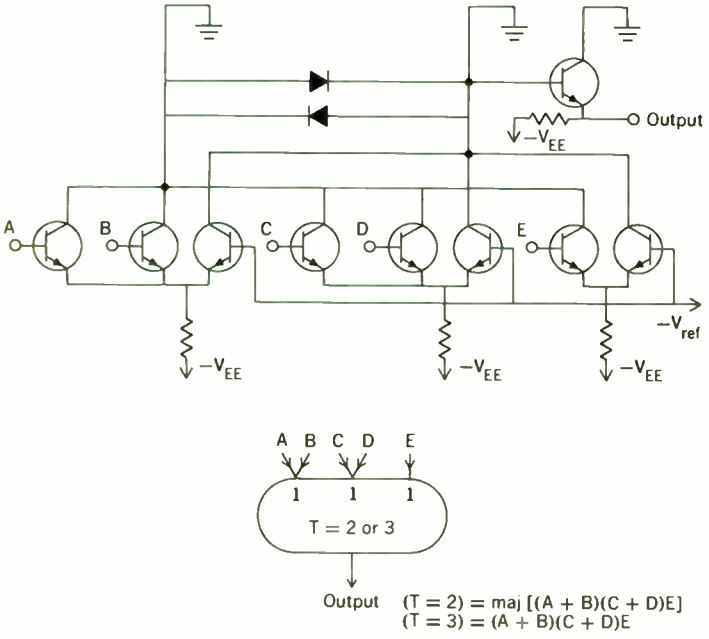
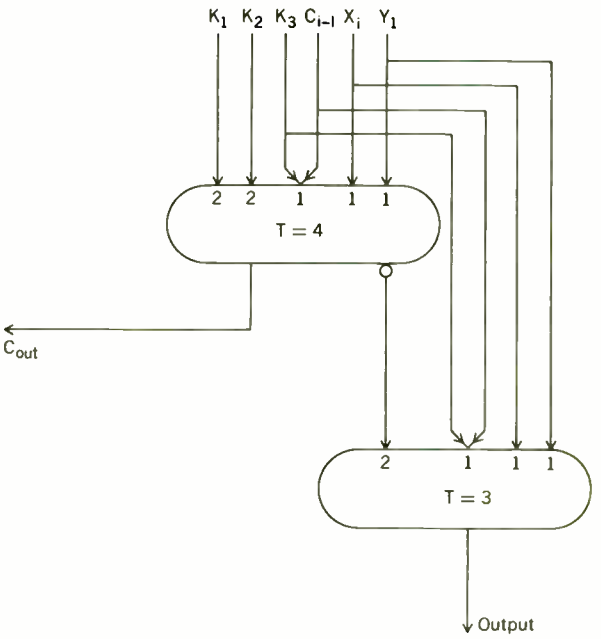


FIGURE 8. Example of an arithmetic unit.



V. Functions derived from three control signals

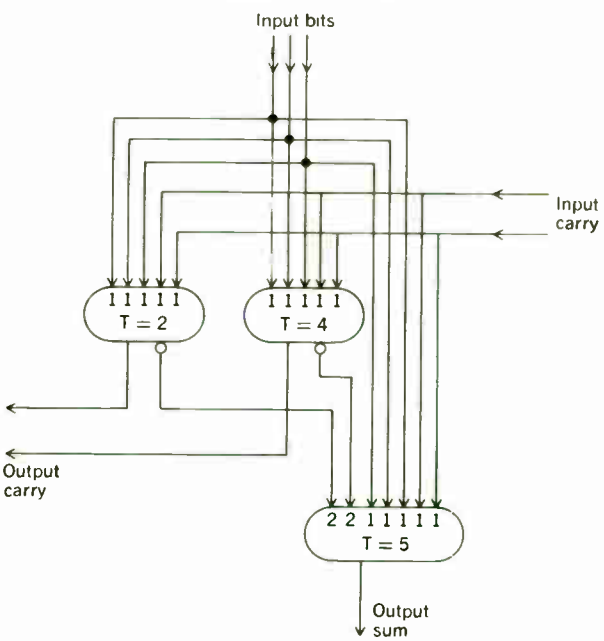
Condition	Control States K_1 K_2 K_3	Function	Output Gate
1	1 0 0	Adder	sum
2	0 0 0	$X_i + Y_i$	OR
3	1 1 0	$X_i Y_i$	AND
4	1 0 1	$X_i \oplus Y_i$	exclusive OR

the result of the threshold decision on one output to put a weighted current component into the current sum of the other output.

In this circuit, the resistor R_1 calculates the inverted majority function of the three inputs (two out of three, as it always did) and feeds a double-weighted module that now serves the purpose of gate B in the adder design of Fig. 3. This module's true side output sums on R_2, which is also fed by the original three inputs. The value of R_2 is specified to calculate the three-out-of-five functions of the three unity inputs and double-weighted module. If two or three inputs are "high," the bottom decision switch contributes a double current through R_2; otherwise, it contributes zero current. Examining the currents through R_1, R_2, and R_3 for the various input conditions shows that the outputs represent $\overline{C_{out}}$ and S_{out} (see Table VI). This circuit is logically and electrically identical to the previous threshold-logic realization of an adder, yet eliminates three switches and their associated connections and power.

To maintain both points about their threshold for speed, clamping, or signal-excursion-control purposes, devices Q_1, Q_2, D_1, and D_2 are provided as indicated in Fig. 10. Transistors Q_1 and Q_2 prevent the sum points from becoming too negative by virtue of the bias on their bases furnished by the reference-source circuit C (shown within the dashed lines). Reference circuit A supplies the

FIGURE 9. A three-addend adder stage.



VI. Current values for various input conditions

Input States X	Y	$\overline{C_{in}}$	Units of Current Through R_1	R_2	R_3	$\overline{C_{out}}$ (R_1)	S_{out} (R_2)
0	0	0	1	2	2	high	high
0	0	1	0	3	2	high	low
0	1	0	2	3	0	low	low
0	1	1	1	2	2	high	high
1	0	0	2	3	0	low	low
1	0	1	1	2	2	high	high
1	1	0	3	2	0	low	high
1	1	1	2	3	0	low	low

main signal reference $V_{ref} = \frac{1}{2} V_{EE}$ with relatively good regulation, independence of V_{be}, and low power dissipation.

Diodes D_1 and D_2 prevent the sum points from becoming too positive. For example, when the sum point of R_1 approaches a very high value—when zero or one unit of current follows through R_1—the bottom decision switch conducts more than its normal two units of current, causing D_1 to turn on and, in turn, supply current through R_1 to lower the potential at its sum point. On the other hand, when the R_1 sum point is "low" ($\overline{C_{out}}$ is 0), the reference side of the bottom decision switch conducts, thus providing a rather accurate double-weighted current through R_2.

At those instances when the sum point of R_2 tends to go high transiently (less than two units of current through R_2) due to a change of input conditions, D_2 turns on to keep at least 1½ units flowing through R_2. This will only happen at instances when D_1 does *not* have to supply current through R_1. The consequence—too-high levels for the $\overline{C_{out}}$ or S_{out} signals—would serve to saturate succeeding stages of logic.

Reference circuit B provides current biasing in such a way that the unit current, determined by V_{ref_2}, increases with temperature just enough to offset the lower V_{be} drop of the output emitter-follower transistors. Just as in the original circuit of Fig. 5, when the number of inputs equals the threshold, the sum-point potential increases in magnitude with increasing temperature so that the outputs remain at $V_{EE}/2$. Reference circuits A, B, and C can be common to several gates.

The power dissipation of the circuit, assuming 2 mA per unit current switch, 1 mA per emitter follower, and a 4-volt supply, is about 50 mW. The $\overline{C_{out}}$ appears in one gate delay and S_{out} in about two gate delays. These delays, measured on a breadboard at this power level using 1-GHz transistor differential pairs, were about 3.5 ns and 6 ns, respectively. Experience with the circuit of Fig. 6 indicates that these values will be reduced by 30 percent when this circuit version is integrated.

The number of components in a basic adder is now

4 per switch × 4 switches	= 16
2 per emitter follower × 2	= 4
2 for clamping each side × 2	= 4
	24

The bias and reference sources common to an array of gates could represent an average of two additional components. The capability of these threshold gates, with "OR-ing" on the input switches and making use of double-function thresholding, can be extended to parity

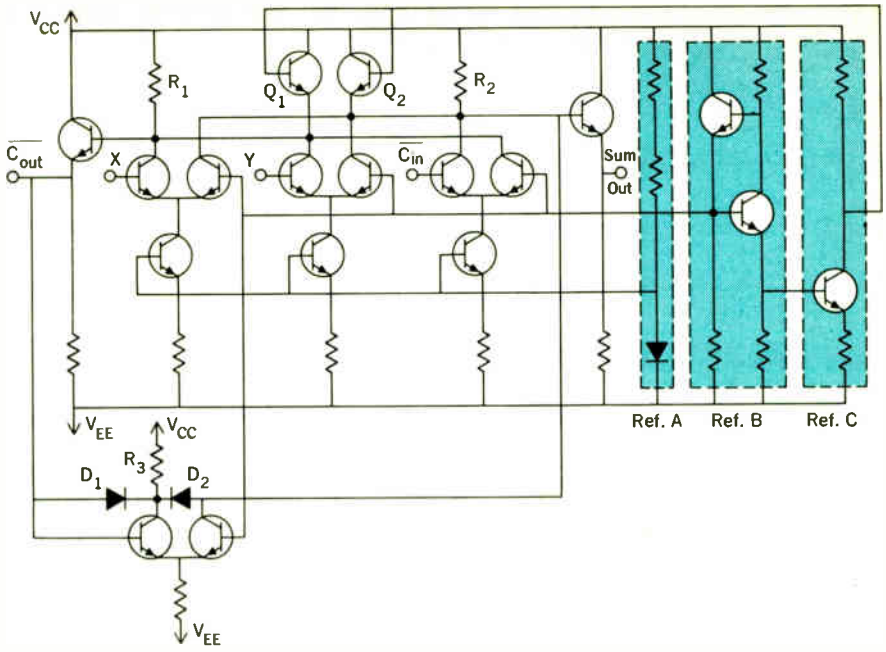
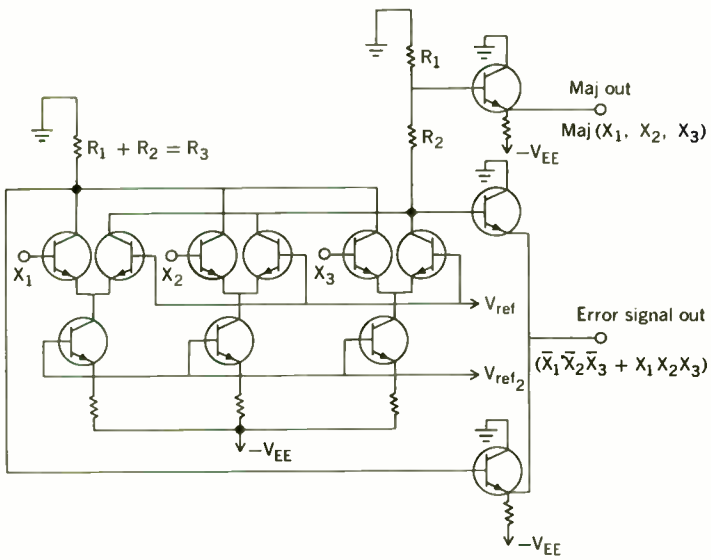


FIGURE 10. Multifunction threshold-gate full adder.

checkers and multipliers, quite similar to the adder.

A majority voter with an error indication that makes use of these principles will now be described. A three-input majority gate will of course give an output representative of two or three out of its three inputs. What is frequently desired is an indication if one of the three inputs disagrees with the other two. Figure 11 displays such a circuit. The in-phase summing resistor is divided into two parts; the upper resistor R_1 is the two-out-of-three value and provides the majority signal, the lower resistor R_2 when added to R_1 provides the output of an AND gate. The out-of-phase summing resistor R_3 calculates the NOR of the inputs, and is in fact equal to $R_1 + R_2$, thus providing the complemented dual of the AND gate. Virtual OR-ing of the AND and NOR outputs, readily achieved with the emitter-follower outputs, then gives a signal output that is high only if all the inputs agree.

FIGURE 11. A majority voter with error indication.



Circuit tolerances and noise immunity

With this new circuit, it is still possible to account for V_{be} temperature effects by tailoring the V_{ref_2} current bias source as shown in Fig. 10. With these values, the outputs of both summing sides are centered at V_{ref} for $n/2$ inputs "high" independent of temperature. This circuit is still dependent on resistor ratios for its success and, to a much lesser degree, absolute resistor values. Absolute values greater than ±15 percent would simply affect power and delay (inversely). As in the basic gate of Fig. 5, however, the larger the fan-in and the lower the threshold, the tighter the resistor-ratio tolerance. It has been determined that five-input majority gates need have no better ratios (among the current-determining resistor, summing resistors, and biasing resistors) than ±3 percent for a worst-case reduction in signal swing, with a 4-volt supply of about 20 mV.

Ratio accuracy of ±2 percent with 12-μm-wide resistors are considered practical. That is, on a statistical basis where ratios would be factored into chip acceptance, the overall effect on yield is felt to be very slight, with other gross effects generally predominating. This would provide for reliable seven-input majority gates with ECL-compatible signal swings.

The original threshold gate (without constant-current sources) tracked within a very wide power-supply range, limited only by a minimum when the signal output is reduced beyond tolerable noise immunity. This was true because the reference was derived from the power supply and is always half its value. For example, although the integrated gates of Fig. 6 were designed for a nominal supply of 4 volts, they worked equally well from 3.2 to 6 volts. This range is not as wide in the multifunction gate, where constant-current sourcing is necessary. Although V_{ref} still tracks properly at half the supply, V_{ref_2} does not. However, tolerances of ±5 percent

will not detract more than about 15 mV from the worst-case signal swing.

Finally, V_{be} matching of 3 or 4 mV and α matching of ± 0.01, both easy to obtain within a chip, will not contribute significant error over that due to resistor ratios. A center α design value of 0.98 is included in the specification of the nominal resistor values. Other assumptions used in these designs are

$$\Delta V_{be}/\Delta T: -2 \text{ mV/°C}$$

Resistor tolerances: $\pm 20\% + 0.2\%/°C$

V_{be}: 0.75 volt at $I_e = 2$ mA

Summary and conclusions

Traditional threshold-logic gates have been described, along with a departure that uses the normally complementary dual outputs for completely different functions. Original threshold-logic designs have shown improvements over conventional Boolean-gate realizations of two or three to one in component count, power, and speed. However, new bases of comparison are now necessary. Specifically, threshold-logic circuit techniques may be viewed among other LSI logic implementations in the following ways:

1. Basic Boolean-gate arrays—OR/NOR in the ECL family.
2. The use of double-level (cascode) switching to achieve AND-ing within the OR/NOR gate.
3. The use of tying collectors of ECL switches together for AND-ing.
4. Threshold gates.
5. Multifunction threshold gates.

In all cases, virtual OR-ing of outputs is possible. Case 3 is in fact the special case of a threshold gate where $T = n$ for an n-input switch gate. It is difficult to make precise comparisons between the techniques of case 5 and those of cases 2 or 3. A basic full adder was seen to take 20 to 24 components depending on clamping (which in itself is dependent on desired speed and external circuit compatibility). A circuit based on the techniques of case 3, using exclusive-OR gates, can result in a full adder with 39 components.[11] Advantages such as these, or even greater ones, will be maintained for such circuits as multipliers and parity checkers. Power and speed must also be judged in individual cases; however, the threshold gate, where applicable and using equivalent transistor geometries, might produce a two-to-one improvement.

The point is, why not consider the use of threshold-logic techniques for functional units where such methods afford an advantage? LSI technology offers the opportunity for functional designs where Boolean and threshold methods are both used on the same silicon chip, fabricated by a standard process.

REFERENCES

1. Winder, R. O., "The status of threshold logic," *RCA Rev.*, vol. 30, pp. 62–84, Mar. 1969.
2. Hu, S. T., *Threshold Logic*. Berkeley: Univ. of Calif. Press, 1965.
3. Lewis, P. M., II, and Coates, C. L., *Threshold Logic*. New York: Wiley, 1967.
4. Winder, R. O., "Fundamentals of threshold logic," in *Applied Automata Theory*, J. T. Tou, ed. New York: Academic Press, 1968.
5. Beinart, J., Hampel, D., Prost, K., and Winder, R. O., "Integrated threshold logic," Final Rept., AF Avionics Lab. Contract AFAL-TR-69-195, June 1969.
6. Cyprus, J. H., "Optimal synthesis of the Boolean functions of four variables with majority logic," Ph.D. dissertation, Rice University, Houston, Tex., 1963. (University Microfilms, Inc., Ann Arbor, Mich.)
7. Amodei, J. J., Hampel, D., Mayhew, T. R., and Winder, R. O., "An integrated threshold gate," *1967 Internat'l Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 114–115, Feb. 1967.
8. Winder, R. O., "Threshold logic will cut costs, especially with boost from LSI," *Electronics*, vol. 41, pp. 94–103, May 27, 1968.
9. Beinart, J. H., *et al.*, "Threshold logic for LSI," *NAECON Proc.*, May 1969.
10. Hampel, D., Beinart, J. H., and Prost, K. J., "Threshold logic implementation of a modular computer system design," Final Rept., NASA Contract NAS12-2130, Oct. 1969.
11. DeWitt, D., Private communication.

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Semiconductor random-access memories

Random-access read–write semiconductor memories typify the revolution in computer memories—storage elements that promise to replace ferrite cores and plated wires in the seventies. Prices have dropped as yields have improved

L. L. Vadasz, H. T. Chua, A. S. Grove *Intel Corporation*

In the last few years, semiconductor random-access memory (RAM) components have been introduced into high-speed scratchpad applications and small buffer memory systems, where the performance or cost advantage of semiconductor components is greatest. More recently, developments in the technology of large-scale integrated (LSI) circuits have resulted in cost–performance characteristics of semiconductor RAMs that are competitive in computer main-frame memories as well. This article reviews the basic circuit concepts used in these components, representative products that are presently available, and some systems considerations involved in their use.

Semiconductor memories have been a part of high-performance computers for the last four to five years. Because of their high cost, these elements were used only in applications where no other memory component could provide the desired performance. Consequently, those applications were all related to high-performance bipolar semiconductor memory elements.

The first large semiconductor memory subsystem, the Cache memory, was reported by IBM in 1969.[1] Its major characteristics were a system access time of 60 ns and a minimum memory size of 112 kilobytes. The system used 64-bit bipolar memory chips.

Whereas early bipolar memory elements gave rise to the development of a new class of memory systems, the emerging metal oxide semiconductor (MOS) technology provided the first competitive semiconductor product in a market that was served by magnetic-core elements. The most vulnerable target was the small buffer memory of a few thousand bits per system, with access times of 1 to 5 μs. In such applications, the cost of using cores can be quite formidable, because of the high cost of overhead electronics needed for the core memory systems. Even early MOS memories were able to compete economically with such memory approaches. For instance, in one typical application of these MOS buffer memories, two small 16-pin dual-inline-package 256-bit static MOS memory components replaced a whole board of cores and associated electronics.

Another memory system also evolved in the past few years. This system is based not on RAMs, but rather on serial shift-register memory elements. Such memory systems find typical use in computer terminals where they can be used as refresh memories for CRT displays.

Examples of the emerging application of LSI main-frame memories are the use of high-speed bipolar memory circuits in the IBM System 370/145, and in the ILLIAC IV process element memory (Fig. 1), one quarter of which uses sixty-four 130-kilobit systems with a cycle time of less than 200 ns. The bulk of these systems use bipolar chips containing 256 bits of storage.[2] Other, less performance- and more cost-oriented applications are the Data General Supernova minicomputer, and the Four Phase IV/70, which use up to 1-μs MOS memory chips, typically containing 1024 bits of storage. Most of these systems were introduced commercially in the latter part of 1970 or first part of 1971. They are based on semiconductor memory components that are typical of the state of the art as of 1971.

The bistable flip-flop as a storage cell

Although there are many devices that may be used as storage elements, the bistable flip-flop, made of two cross-coupled inverters, has been the most widely adopted basic storage cell for both bipolar and static MOS circuits. The cell is simple to design, is inherently very high speed, and is generally insensitive to process parameter variations; these properties provide high-yield, low-cost components. In Fig. 2 the inverter is made of a transistor and a collector load resistor R_c. For an MOS circuit, R_c is made of another MOS transistor, which provides a small-area nonlinear resistor when its gate is tied to its drain.

In a flip-flop, one transistor is normally on, which keeps the other transistor off. When the "off" transistor is forced into the "on" state by an external signal, the "on" transistor turns off. The flip-flop can, therefore, have two stable states, and will remain in either of these states until an external signal is used to change its state. The two stable states may be used to store information by being interpreted as logical "1" and "0."

Bipolar memories. A gating arrangement gets information in and out of the circuit—writing or reading of the memory, respectively. Figure 3 shows some of the tech-

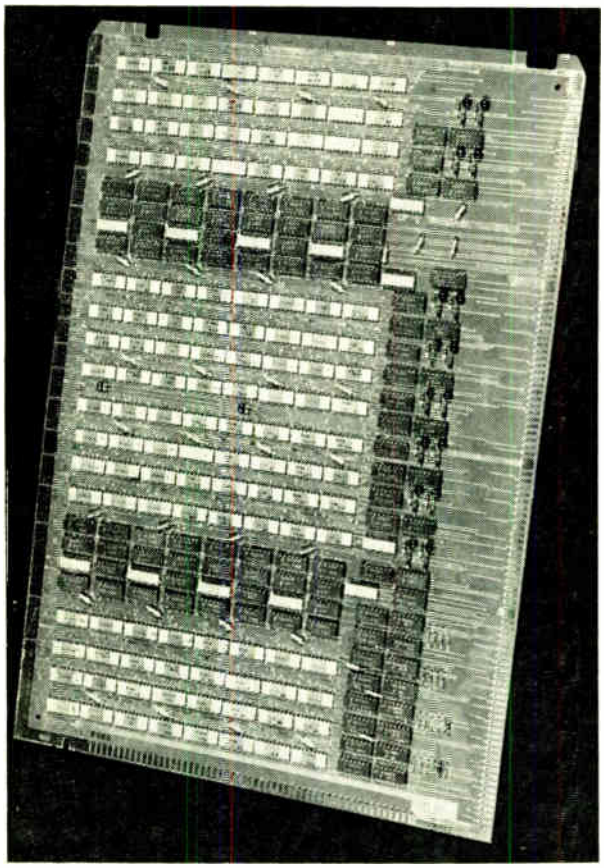
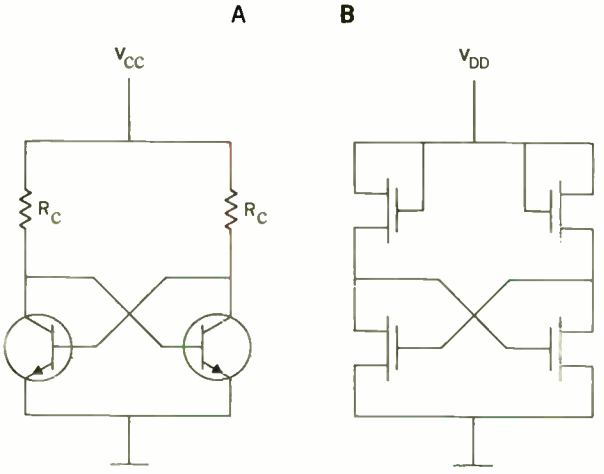


FIGURE 1. Memory module of the ILLIAC IV system. The 30.5- by 43-cm two-layer board contains 2048 words of 16 bits of memory, including data registers. The board contains 128 μL4100 256-bit bipolar memory devices. The memory system in which this board is used operates at a 200-ns read or write cycle time and a 188-ns maximum read access time. (Courtesy Fairchild Semiconductor)

FIGURE 2. Basic flip-flop memory cell that uses (A) bipolar elements and (B) MOS elements.



niques used for this purpose. Figure 3(A) illustrates a basic flip-flop made with two dual-emitter transistors.[3] One of the emitters from each transistor is tied to one of the bit lines. The remaining emitter of each transistor is tied to a common word line. Many flip-flops may be interconnected to form a large memory array where each flip-flop has a unique location, or address. A particular memory cell may be selected (addressed) for either writing or reading by applying proper signals to the word and bit lines. The word-line voltage is raised to read the content of a cell. The flip-flop current, which normally flows through the word line, transfers to one of the bit lines. A current-sensing amplifier detects the signal current. A cell is similarly selected for writing. Unbalancing the voltage at the two bit lines forces the flip-flop into the desired state. When the cell is not selected, the word-line voltage is low, and cell current flows through the word line. Under this condition, there is no signal current at the bit line, and the content of the cell is not sensed. Similarly, raising or lowering the voltage on the bit line will not affect the state of the flip-flop.

This circuit is very simple and consumes very little silicon area. It has been used successfully in many of the larger bipolar memory circuits, such as 64-bit random-access memory components by Intel, Intersil, Computer Microtechnology, and Raytheon. It is also used in Fairchild's 256-bit RAM, on which the ILLIAC IV memory module is based. The circuit is applicable to either the standard gold-doped TTL process or to the more novel Schottky process. The speed of accessing of the memory depends largely on the amount of current available from the cell for sensing. To maintain consistent and fast switching speed, the collector load resistors (R_C) of the flip-flop must not have wide variations in resistance.

The circuit shown in Fig. 3(B) operates in a different mode. This circuit is particularly suitable for the Schottky process because the two added gating Schottky diodes are made within the collector region of the flip-flop transistor, which keeps the increase in the size of the memory cell very small. A cell is selected for reading by lowering the voltage of its word line. Signals may be detected on the bit line through the Schottky diode. For writing, a cell is first selected. A large current feeds into one of the bit lines through the Schottky diode, which simultaneously turns on the "off" transistor and increases the collector load current of the previously "on" transistor, forcing it to turn off quickly. The access speed of the memory is not significantly affected by the size of the collector resistor R_C; therefore, R_C may be made large to reduce power dissipation. Low-power operation is further achieved in this circuit as a result of low voltage across the unselected cell. This circuit is used in Intel's 256-bit memory, the 3102. A collector bulk resistor, which provides a higher resistance for a given silicon area, is being used as R_C of the memory cell.

A third class of bipolar memory cells is shown in Fig. 3(C). This circuit is popularly used in emitter-coupled logic (ECL) circuits. A commercially available ECL memory product that uses this basic cell is Advanced Memory System's 64-bit memory. This circuit employs two layers of metal interconnections. Successful fabrication of an ECL memory circuit containing 128 bits using single-layer metal interconnection has also been reported.[4]

The memory cell operates as follows: A particular bit is selected by raising its word-line voltage. Writing or read-

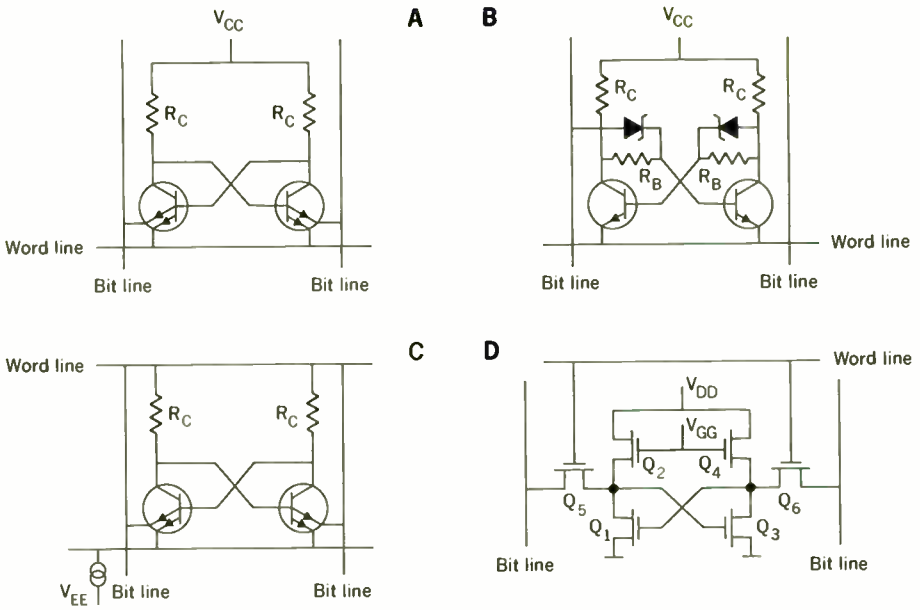


FIGURE 3. Various flip-flop memory cells. A—Basic flip-flop with two dual-emitter transistors. B—Flip-flop with two added gating Schottky diodes within the collector region. C—A basic cell for ECL circuits. D—An MOS flip-flop cell.

ing of the memory cell is very similar to that of the multi-emitter cell of Fig. 3(A), except that the voltage across the selected cell is higher than that across the unselected cell; therefore, a large sense current is available from the flip-flop when it is selected. When the flip-flop is not selected, the voltage across its supply terminal is quite low, and low standby power dissipation is thereby maintained.

MOS memories. The MOS flip-flop memory shown in Fig. 3(D) works as follows: The flip-flop formed by Q_1, Q_2, Q_3, and Q_4 is gated by transistors Q_5 and Q_6. To read the cell, the word line turns on Q_5 and Q_6, transferring the data of the flip-flop to the bit lines. To write into a cell, the word line again turns on Q_5 and Q_6 and now forces the cell into its proper logic state by establishing the proper voltage on the bit lines.[5]

The voltages V_{DD} and V_{GG} are the negative supply voltages for the cell for the case of p-channel MOS transistors. These voltages can be identical or different (V_{GG} more negative than V_{DD}), depending on a particular design. Having a common V_{DD} and V_{GG} line reduces the cell size. Having separate V_{DD} and V_{GG} lines, however, allows the user to switch to low-power standby mode in the time period when access is not made to the memory. This mode of operation will be further discussed in later sections. An MOS flip-flop storage cell uses six transistors per bit. This circuit is used in all of the commercially available 256-bit decoded MOS memory

FIGURE 4. Cell size of bipolar memory components as a function of time. Static and dynamic MOS cells are included for comparison.

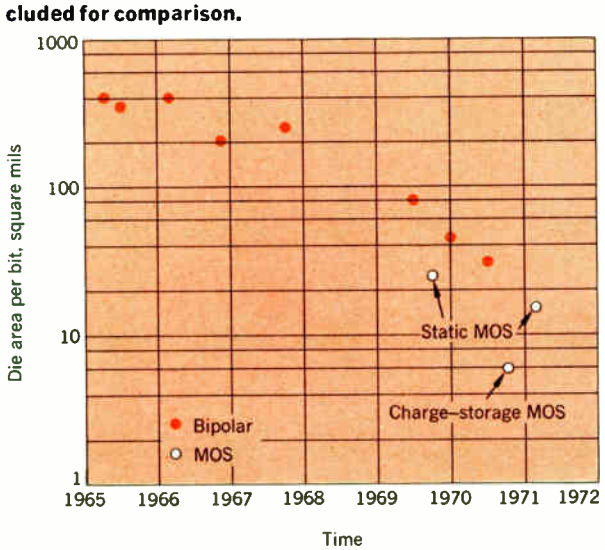
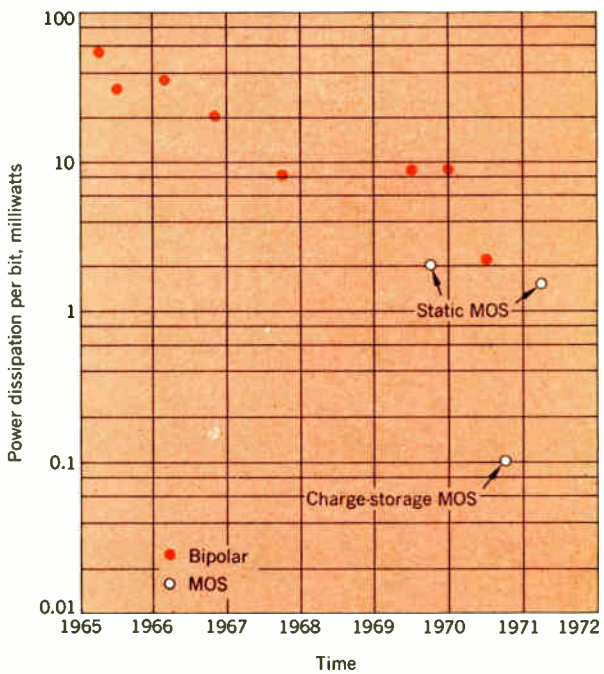


FIGURE 5. Power dissipation of bipolar memory component as a function of time. Static and dynamic MOS cells are included for comparison.



arrays—for example, Intel, Unisem, Intersil, and Computer Microtechnology.

Progress in bipolar semiconductor memory. Semiconductor memory became commercially available in its primitive form in early 1965. The memory chips made in those days typically contained four to eight bits per chip and were organized as linear select type, with several bits per word. Because of the high ratio of the number of sense amplifiers to the number of bits per chip, the memory cells had to be made complex enough to deliver level-compatible signals to the outside world without elaborate buffering and sensing. As the number of bits per chip increased, the memory cells became less complex and dissipated less power, while more sophistication was added to the drive and sense circuits.

Figures 4 and 5 show the cell size and power dissipation, respectively, of some of the typical memory chips made during the years 1965 to 1970. In 1965, the power dissipation was typically 30–40 mW, and the cell occupied approximately 400 square mils (0.258 mm²) of silicon area. By 1970, commercially available cells consumed only 30 square mils of silicon area and dissipated 2 mW. Figure 6 shows a photomicrograph of a partially decoded 256-bit bipolar memory chip with such characteristics. Cell size of 20 square mils is practical using today's technology.

Hybrid memory systems

Even as bipolar memory cells decreased in size and in power consumption, a different approach to semiconductor memories was suggested, which used MOS flip-flops for storage.[6] Since the MOS process contains fewer steps, and since for a given set of tolerances it is capable of higher component density than the bipolar process, this approach promised to yield a lower-cost semiconductor storage. Figures 4 and 5 include the static MOS memory cell that became commercially available in 1969 for comparison. Both the smaller cell size and lower power consumption of MOS flip-flops are evident.

MOS devices are basically high-impedance devices, and their drive capability is limited. When their load is another small-geometry MOS device on the same chip, even the limited drive is sufficient to result in a generally satisfactory switching speed (100 ns or less). When, however, MOS devices must drive devices in another package, the greater loading results in a significant performance degradation. Thus, a desirable hybrid approach to semiconductor memories could be based on the use of MOS devices for storage and bipolar devices for the support circuitry: driving, sensing, and decoding.

The MOS storage cells, which make up the bulk of the system, are inherently less expensive to produce. The power consumed by the MOS cells is lower than the power that would be consumed by bipolar cells. The high-speed bipolar drive and sense circuits enable high-speed operations that MOS circuits alone cannot achieve. In addition, bipolar input and output circuits can be easily made level-compatible with any form of logic circuits now in existence.

Early hybrid memory systems were made by interconnecting MOS memory arrays and bipolar drive and sense circuits on a ceramic substrate by beam leads or solder bumps. The MOS chip—storage arrays of MOS flip-flops with minimum drive and sense circuitry—contained the highest number of bits per chip producible with reasonable yield in the given time period. The bipolar

FIGURE 6. Photomicrograph of a partially decoded 256-bit bipolar memory chip.

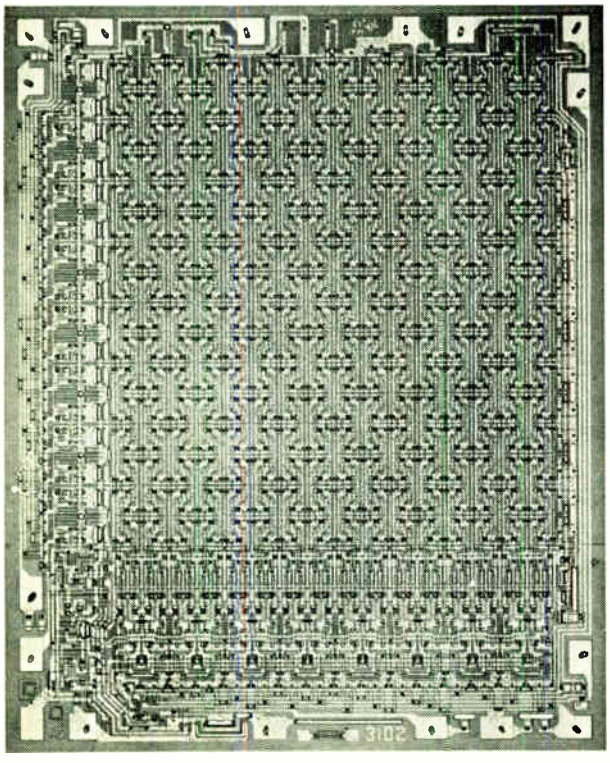
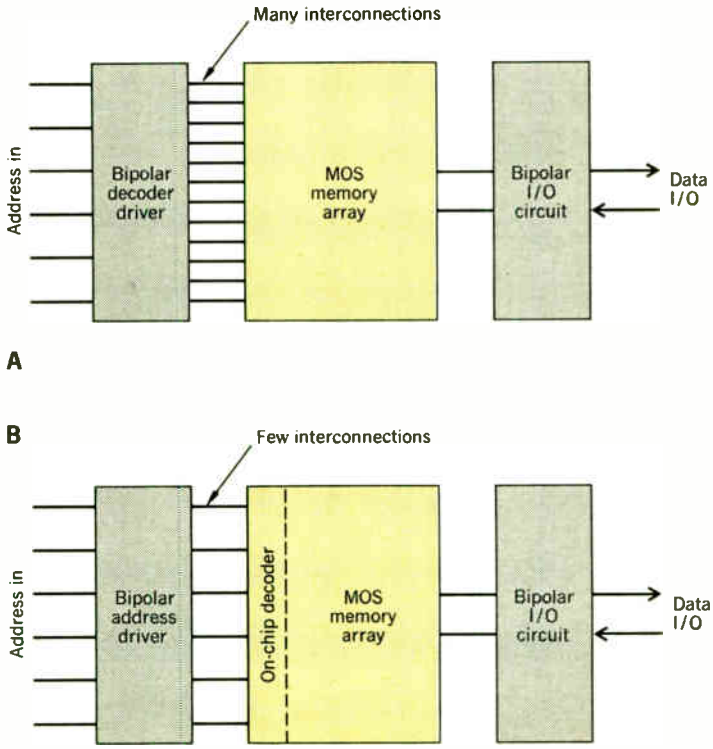


FIGURE 7. Shift in partitioning of semiconductor memories that use both MOS and bipolar devices.



circuits performed the necessary decoding, level shifting, buffering, and sensing functions.

Some semiconductor companies see the hybrid system described above as the ultimate approach to utilizing fully the potential capability of both the bipolar and MOS technologies. Fairchild Semiconductor was the first to develop such a system.[7] Fairchild's system, called the Semiconductor Active Memory, is a 16-kilobit memory stack made up of 64-bit MOS memory arrays and bipolar drive and sense circuits. Motorola Semiconductor subsequently developed an 8-kilobit memory module, which claimed access times of less than 150 ns. Its basic storage array was a 256-bit MOS chip. The only commercially available multichip hybrid memory product is Computer Microtechnology's device, a 4-kilobit hybrid memory module built from 256-bit MOS chips. Its cycle time is rated at 400 ns.

These hybrid approaches were all partitioned in such a way that bipolar circuits were used for decoding. As a result, the storage chips had to have a large number of interconnections made to them—up to 40 for a 256-bit array. Because such a large number of interconnections is very cumbersome and expensive in the case of a multichip module, all of these approaches were based on some face-down bonding technique, such as flip-chip or beam-lead bonding.

These techniques have been in development many years. Although all of them were eventually shown to be technically feasible, they were not as effective in reducing assembly and package costs as had been hoped. As a result of high costs and of the development of MOS storage circuits other than the conventional flip-flop, the partitioning of MOS/bipolar memory has changed to permit decoding to be done on the MOS storage chips, with only the driving and sensing functions performed by bipolar circuits. This greatly reduces the number of required interconnections and permits the use of conventional packages and assembly techniques without excessive costs. Figure 7 illustrates this shift in partitioning, which took place as more area-efficient storage techniques developed.

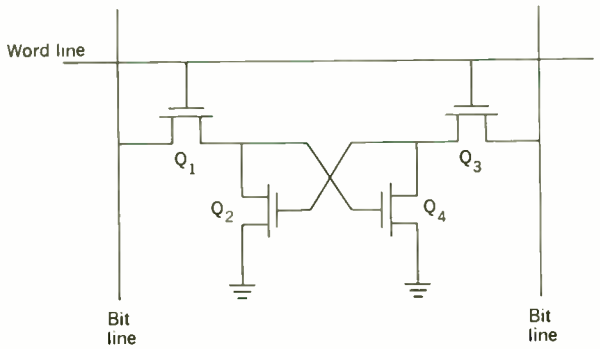


FIGURE 8. Four-transistor-per-bit charge-storage MOS memory cell.

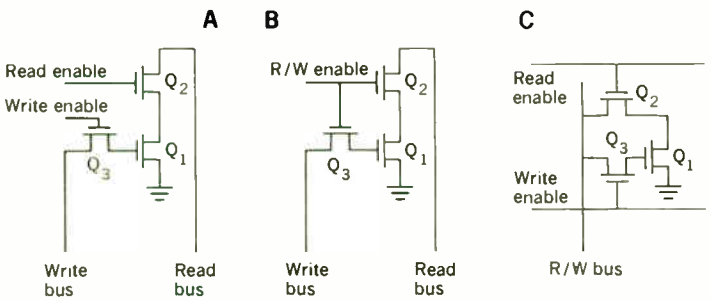
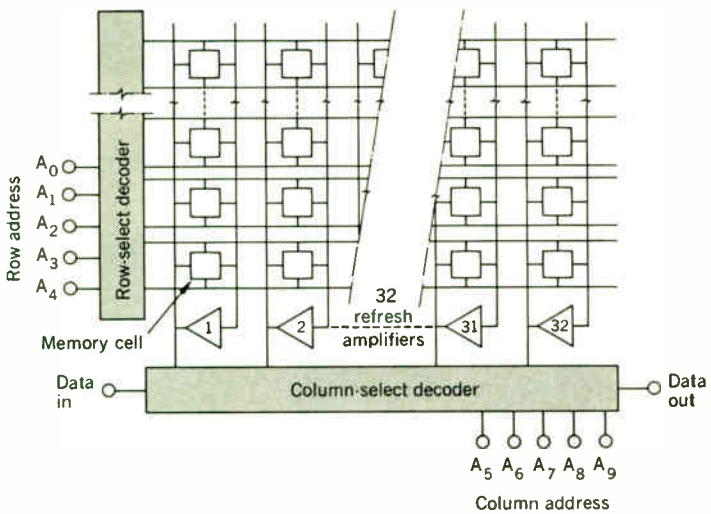


FIGURE 9. Various charge-storage MOS memory cell configurations that use three transistors per bit.

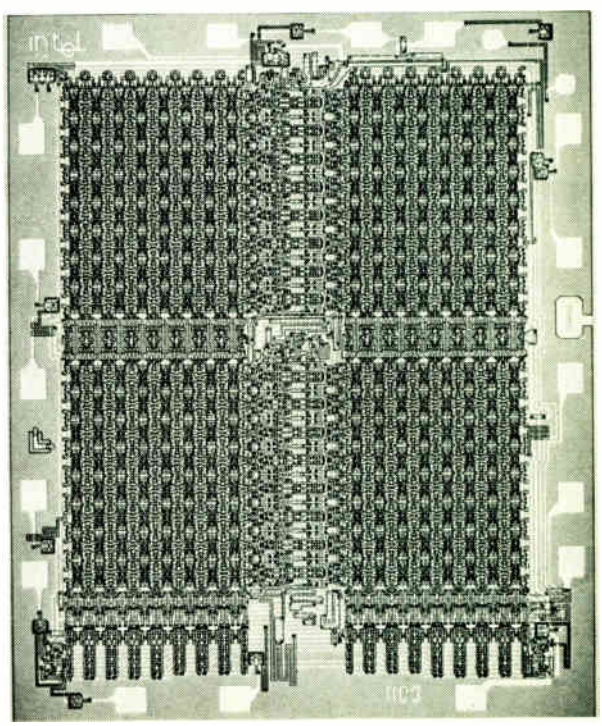
FIGURE 10. Organization of a fully decoded 1024-bit charge-storage MOS memory chip.



Charge-storage memory elements

The major disadvantages of bistable flip-flop storage elements are twofold: (1) They dissipate too much power, which limits the number of bits that can be put into a package module. (2) They occupy too much silicon area, which limits the number of bits that can be economically

FIGURE 11. Photomicrograph of a fully decoded 1024-bit charge-storage MOS memory chip.



put on a monolithic circuit. Various techniques have evolved to combat these shortcomings of flip-flop-based semiconductor memories. For example, the simplest way to reduce the power dissipation of an MOS storage cell of Fig. 3 is to clock the V_{GG} supply line. While the V_{GG} supply line is negative the MOS transistors connected as load elements will be active. When V_{GG} is positive, the load elements will be turned off. Correct memory information is maintained by charge storage only. One side of the flip-flop was negative prior to the turnoff of V_{GG}. This side will maintain its potential by storing this negative charge on the gate capacitance of the other flip-flop side. Parallel with this gate capacitance, however, is the junction capacitance associated with the crosscoupled MOS devices. These junctions will provide a parasitic leakage path—through the leakage current of a reverse-biased junction—for the stored charge and, therefore, will limit effective charge storage to a finite time period. One characteristic feature of dynamic charge-storage semiconductor memories, therefore, is that they all need a *periodic refreshing* of the charge stored in their cells. In the case of the memory cell of Fig. 3(D), this is accomplished by periodically turning V_{GG} negative, which activates the load elements and replenishes the lost charge through this load element. The minimum rate is determined by the quality of the process and the temperature range of operation. Power dissipation figures as low as a few microwatts per bit can be achieved in the standby mode.

This or similar methods—while achieving significant power reduction and thus removing one important limitation—do not effectively attack the most significant problem: packing density of memory cells. Economics dictate that, for minimizing bit cost, the number of bits per chip has to be maximized. The technological constraints are a given maximum chip size and a set of photolithographic tolerance rules.

Somewhat better packing density can be achieved using the cell of Fig. 8. This is a four-transistor cell—basically a flip-flop without the load devices. Unlike a conventional flip-flop cell, the word-enable transistors and the load devices (Q_1 and Q_3) are one and the same. If the proper device ratios are maintained between Q_1 and Q_2, and between Q_3 and Q_4, the flip-flop maintains its proper logic state. To read, one senses the currents in the bit line. If Q_2 is on, the bit line associated with this side will carry current, the other bit line will not. To write into the memory cell, one forces the bit lines into the proper states and then transmits these data into the cell by enabling the word line. To refresh such a cell, the bit lines change to a common negative potential (for the case of p-channel circuits) and turn on the word line. This

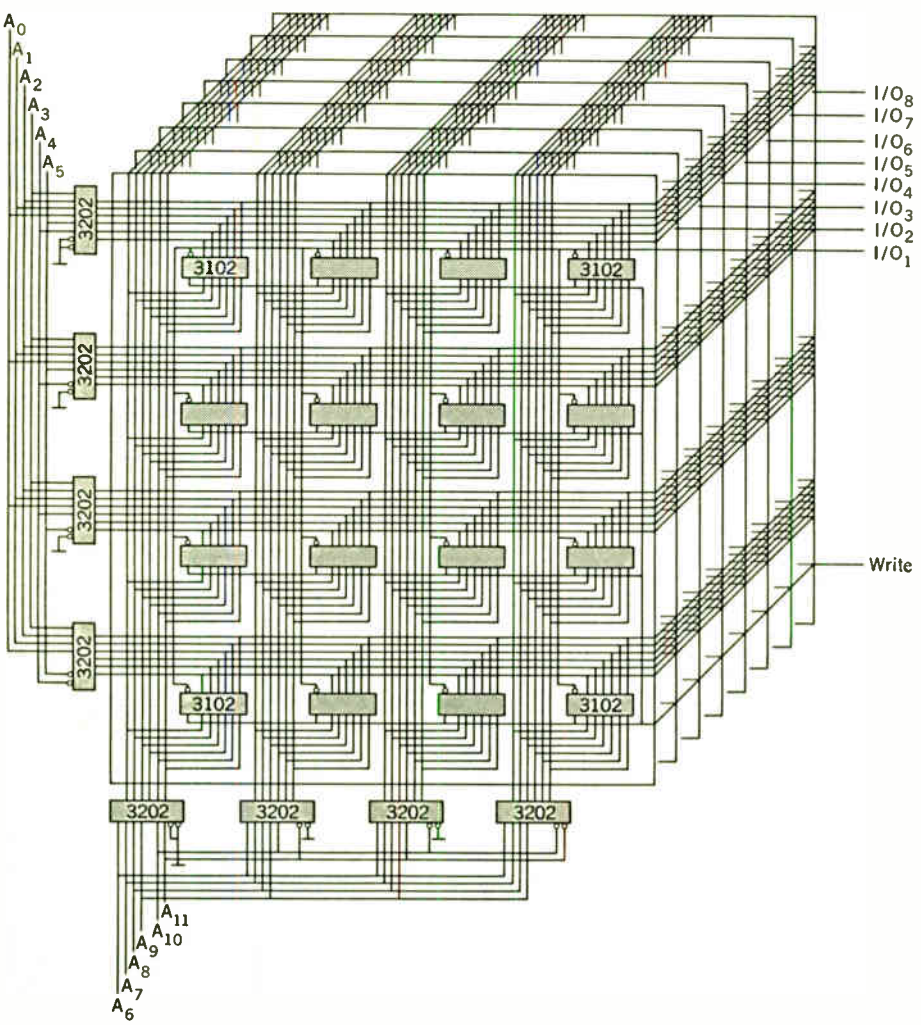


FIGURE 12. Organization of a 4096-word by 8-bit memory system that uses partially decoded 256-bit bipolar memory components. The memory chips are marked 3102, and the decoder-drivers are marked 3202. The diagram shows eight identical planes that each contain 4096 words of one bit.

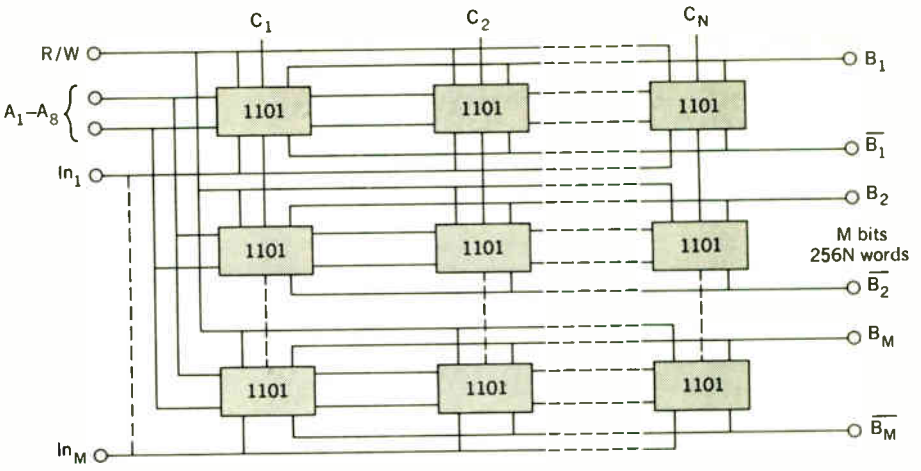
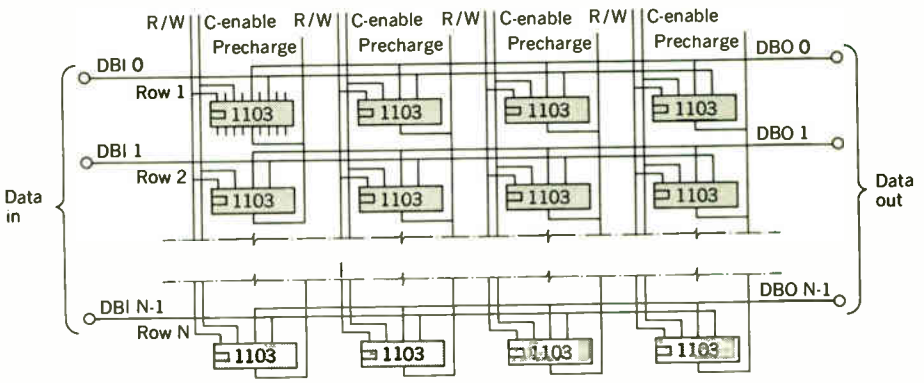


FIGURE 13. Organization of a memory system that uses fully decoded 256-bit MOS memory components, which are marked 1101. All address inputs are connected in parallel, and the appropriate memory units are enabled by the chip-select inputs for input or output operation.



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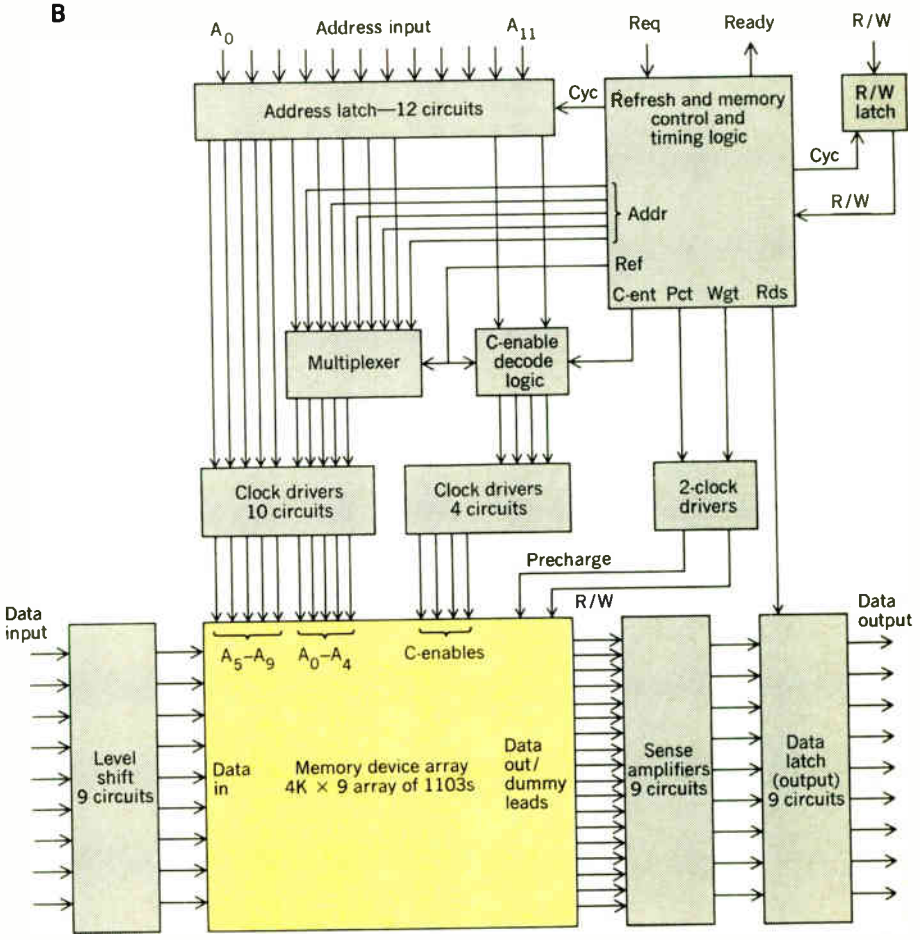


FIGURE 14. Organization of a memory system that uses fully decoded 1024-bit memory components. The memory components, marked 1103, can be connected in an array of 1024M words by N bits. System access times of under 250 ns and cycle times of under 400 ns are achievable with such memories. A—Organization of the memory plane. B—Block diagram of a 4096-word by 9-bit memory system.

causes the regeneration of information in the cell. This type of cell is used in AMI's 512-bit dynamic RAM and in Cogar's 1024-bit memory chip.[8]

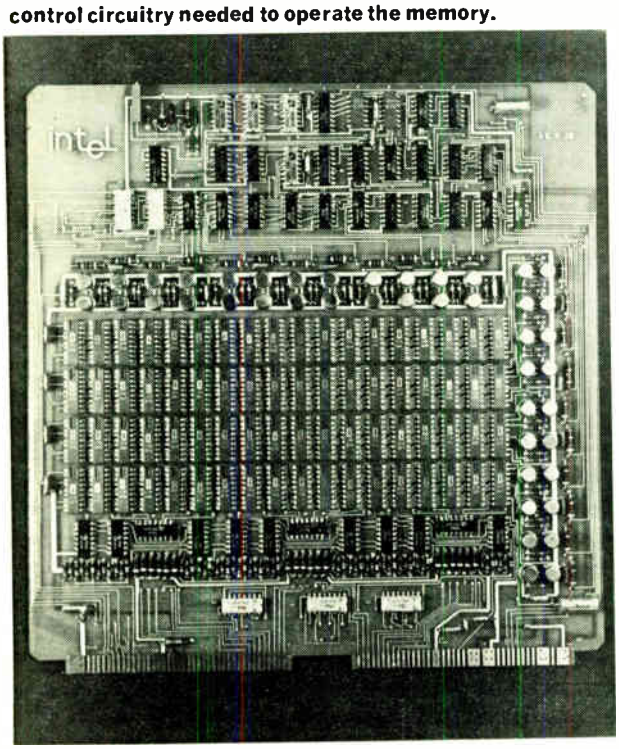
To store charge, however, a flip-flop is not needed; only one MOS transistor whose gate is the storage node is used.[9,10] For a *p*-channel MOS transistor the presence of a sufficient amount of negative charge on its gate will mean that the device is on. An insufficient amount of charge on this gate will mean that the device is off—an electrical analogy to the logic "1" and logic "0" conditions. A means for supplying charge or no charge to the gate of the MOS transistor (for writing into the cell) and a means for interrogating the cell for its content (for reading it) is needed. Figure 9(A) shows a configuration of such a charge-storage memory cell. Transistor Q_1 is the charge-storage element. Transistor Q_2 connects Q_1 to the *read bus* when it is activated by the *read-enable* signal. Transistor Q_3 provides a *write* path to the charge storage node when activated by the *write-enable* signal. Transistor Q_3 also provides periodic refreshing of the memory data. This process rewrites or reinforces the charge condition of the storage node from an on-chip refresh amplifier. In a typical memory array organization (Fig. 10) each column of M bits has its own refresh amplifier. There are N columns in the memory array. Activating any one of the M read-enable signals writes the content of the memory cells in that row into their respective refresh amplifiers. This, followed by the write-enable command on that same row, will refresh all memory cells in that row. Refreshing the entire memory plane requires going through M rows only because each refresh cycle will refresh N bits simultaneously.

The memory cell shown in Fig. 9(A) is used in Intel's 1103, a 1024-by-1 dynamic RAM, whose basic organization is shown in Fig. 10. A photomicrograph of this chip is shown in Fig. 11. Various other products (AMI's 6001 and Mostek's MK 4006P) use similar charge-storage concepts. There are some differences in cell connections, Fig. 9(B) and (C), or periphery designs, but all of these products are based upon the three-transistor memory cell.

Although these dynamic RAMs are only now available commercially, they already represent significant competition to any existing main-frame memory elements, such as cores or plated wire. They achieve high performance: less than 200-ns access time, less than 100-μW/bit power dissipation in the active mode, and less than 10-μW/bit power dissipation in the standby mode. Their small geometry allows extremely high packing density on a memory chip, as shown by the comparison in Fig. 4. A 1024-bit memory chip using three-transistor cells has about the same dimensions as a 256-bit memory chip using bistable flip-flop cells. As a result, these memories can be cost-competitive with either cores or plated wires.

Although all existing products based on charge storage use MOS transistors as storage elements, a bipolar equivalent of this principle has been proposed that uses diodes for storage.[11] This concept is in the development state at present.

FIGURE 15. The memory system. The two-layer board contains 4096 words of 18 bits and all driver, sense, and control circuitry needed to operate the memory.



System organization using semiconductor memories

Although semiconductor memories represent some of the most complex integrated chips in digital systems today, they are usually organized in such a manner that system design flexibility is maintained. The following simple examples illustrate how semiconductor memory components may be interconnected to form a variety of large memory systems.

Figure 12 shows a 4096-word by 8-bit system built of partially decoded 256-bit bipolar memory chips (marked 3102) and decoder–drivers (marked 3202). For purposes of illustration, the diagram is drawn to show eight identical planes. Each plane contains 4096 words of one bit. To increase the word length, one needs only to increase the number of planes. Word size may be increased by increasing the size of each plane in the x or the y direction, or both. Cycle time of such a system is 100 ns.

Fully decoded static MOS memories can be used to construct a memory system in a similar manner. Figure 13 illustrates the expansion of a 256-by-1 fully decoded memory component (marked 1101) into a 256N words by M bits memory system. In Fig. 13, the outputs can be OR-tied to expand the number of words. All address inputs are connected in parallel and the appropriate memory units are enabled by the chip-select inputs for input or output operation. The input and output parts are directly interfaced to commonly used bipolar logic circuits such as TTL integrated circuits. System performance is in the 1-μs cycle time range.

In larger memories (4 to 8 kilobytes, or more) dynamic MOS memories based on the charge-storage concept provide the most economical approach.[12] In Fig. 14, the memory components (marked 1103) can be connected in an array of 1024M words by N bits very much like the smaller system of Fig. 13. The interface circuitry, however, is not as simple as that used in a memory system based on fully decoded static memory elements. Address

and clock inputs require a level shifter that converts a transistor–transistor logic (TTL) level to the higher voltage level required to drive the charge-storage memory array, Fig. 14(B). Instead of feeding into a TTL gate, the outputs will require a sense–amplifier interface.

MOS memories that use charge storage require periodic refreshing of information in the cells. For the 1103 this is accomplished by cycling through the 32 states of the address inputs A_0 to A_4. This has to be done within a certain time period. For the 1103 this time is 2 ms.

Special refresh cycles may be executed by the controller to guarantee this condition for a random-access memory. For a 600-ns cycle, the refresh operation requires less than one percent of available memory cycles. Although refresh control is a special requirement inherent in the use of dynamic MOS memory components, it adds only a negligible cost to the total system.

The performance of a system such as Fig. 14 equals or exceeds that of most core memory systems. System access times of under 250 ns and cycle times of under 400 ns are achievable with such memories. Figure 15 shows such a memory system.

The use of semiconductor memory components provides great system flexibility. Memory systems built of semiconductor memory components are easily expandable. Using the wide variety of commercially available semiconductor memory components permits systems of various sizes and speeds.

Conclusions

Semiconductor IC memory elements whose availability was announced in the past year or so herald the existence of a new memory element: the semiconductor memory component. They are the product of a fast developing field that is based upon the ten-year history of IC technology.

The evolution of the IC business has been very rapid. Circuit yields have improved continuously as production costs have decreased; unit prices reaching less than five cents per gate in 1970 for TTL elements, less than one cent per bit for MOS shift-register elements. These economics were made possible by the continuous technology improvements characteristic of the IC industry. These technology improvements are responsible for the existence of LSI arrays, such as semiconductor memory elements that contain thousands of devices on a monolithic chip, and will lead to further cost reduction of these components in the future.

REFERENCES

1. Ayling, J. K., Moore, R. D., and Tu, G. K., "A high-performance monolithic store," *ISSCC Dig. Tech. Papers*, pp. 36–37, Feb. 1969.

2. Rice, R., Sander, W. B., and Greene, F. S., Jr., "Design consideration leading to the ILLIAC IV LSI process element memories," *IEEE J. Solid-State Circuits*, vol. SC-5, pp. 174–181, Oct. 1970.

3. Dunn, R. S., and Jeansonne, G. E., "Active memory design using discretionary wiring for LSI," *ISSCC Dig. Tech. Papers*, pp. 48–49, Feb. 1967.

4. Bryant, R., Tu, G., Kwei, T., and Robinson, R., "A high-performance LSI memory system," *Computer Design*, pp. 71–77, July 1970.

5. Schmidt, J. S., "Integrated MOS random-access memory," *Solid-State Design*, pp. 21–25, Jan. 1965.

6. Pleshko, P., and Terman, L. M., "An investigation of the potential of MOS transistor memories," *IEEE Trans. Electronic Computers*, vol. EC-15, pp. 423–427, Aug. 1966.

7. Dumesnil, M., and Schroeder, J., "A large-scale integration hybrid substrate," *ISSCC Dig. Tech. Papers*, pp. 66–67, Feb. 1969.

8. Lund, D., Allen, C. A., Andersen, S. R., and Tu, G. K., "Design of a megabit semiconductor memory system," *Proc. Fall Joint Computer Conf.*, pp. 53–62, Nov. 1970.

9. Boysel, L., Chan, W., and Faith, J., "Random-access MOS memory packs more bits to the chip," *Electronics*, vol. 43, pp. 109–115, Feb. 16, 1970.

10. Regitz, W. M., and Karp, J. A., "Three-transistor cell 1024-bit 500-ns MOS RAM," *IEEE J. Solid-State Circuits*, vol. SC-5, pp. 182–186, Oct. 1970.

11. Waaben, S., "Electronically variable semiconductor memory using two diodes per memory cell," *ISSCC Dig. Tech. Papers*, pp. 46–47, Feb. 1970.

12. Hoff, M. E., "Design an LSI memory system that outperforms cores—economically," *EDN*, pp. 6–15, Jan. 15, 1971.

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H. T. Chua received the bachelor of science degree in electrical engineering from Ohio University and the master of science degree in electrical engineering from the University of California, Berkeley. During the past eight years, he worked at the Electronics Division of the National Cash Register Company and at Fairchild Semiconductor, where he was group leader for the development of TTL, MSI, and memory circuits. He is at present manager of bipolar engineering at Intel Corporation. Mr. Chua is a member of Tau Beta Pi and Sigma Xi.

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