

## Synchrodyne receiver • Forth for conitrol Compact dise mastering • Loop aerial

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| AS | 315 |
| :---: | :---: |
| DK, | 3800 |
| Drn | $7 \mathrm{b0}$ |
| Dria | 360 ()0 |
| DFI | 978 |
| L | 4100 |
| N/8 | 480 |
| Prs | 420 ()0 |
| St 1 | 8 () |
| MS | $18(1)$ |
| \$ | 400 |



## GRUNDIG OSCILLOSCOPES

## M020: 20MHz DUAL-CHANNEL

 OSCILLOSCOPE- 20 MHz Dual channel oscilloscope
- $2 \mathrm{mV} / \mathrm{cm}$ with full bandwidth
- Automatic peak-value trigger
- $T V$ line and field triggering
- Add and invert (Both channels invertable)
- Internal graticule and $X$ - $Y$ operation

This 20 MHz dual-channel oscilloscope has advanced facilities, making it easy-to-use, with all the ruggedness and reliability to meet your go-anywhere testing needs. Included is a peak-value trigger to ensure stationary displays. Triggering facilities allow clear display of even complex signal shapes.
£275


VIDEO GENERATOR VG 1000

- Professional video generator
- Comprehensive range of test patterns
- Includes VTR head adjustment signal
- Excellent signal quality
- External sync. facility
- RGB output

A professional broadcast-quality pattern generator to meet the highest professional standards. Its special test card allows full visual assessment of the video system, including a special output for
precision testing of VTRs
£1650


## M022: 20MHz DUAL-CHANNEL

 OSCILLOSCOPE WITH AUTOMATIC TIME
## RANGE

- 20 MHz Dual channel oscilloscope
- Automatic time base selection
- Soft tuning for fast manual adjustment
- Triggerable 2nd time-base, guarantees error free 'zooming-in'
- Hold-off control and $Z$ modulation
- Plus all the advanced engineering of the M020


Now, the world's first low cost 'scope with automatic time-base selection. Dual-range 20 MHz capabilities also include'soft tuning' in manual mode, so the 'scope leaves you free to carry out the measurement.
$£ 395$ GRUNDIG TV/VIDEO TEST EQUIPMENT

COLOUR GENERATOR FG 7

- PAL pattern generator
- 15 test patterns
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- Compact and versatile for field or laboratory


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and the IF output
£545


FIELD STRENGTH METER ME9O

- Fully automated field strength measurement - LF radio to UHF TV in a single unit
- Versatile test result selection

Storage of received signal frequencies, for rapid testing

- Alpha numeric display for station checks
- Unattended monitoring with built-in results printer
- Stereo decoding

Fully portable: integral battery and charger Microprocessor controlled for push-button operation in all transmitter checks. The ME90 allows fast and accurate measurements in radio and TV bands, long wave to UHF. Versatile print capabilities provide hard-copy confidence whether routine or continuous monitoring.

For further information and a colour brochure contact our Sales Office.
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February 1986 Volume 93
Number 1600

## FEATURES

| Naiad robot trainer - 4 <br> by R.H. Becker <br> Interfacing the robot arm with <br> Apple, BBC, Commodore and IBM computers. | Forth in control <br> by David N. Sands <br> The computer language Forth is, argues D.N. Sands, particularly suited to the control of machinery. He explains how. |
| :---: | :---: |
| Data conversion by M.E. Eccles Listing, by manufacturers, of a-to-d and d-to-a converter i.c.s and modules |  |
|  | Timing by remote control 63 <br> by Peter Ferris <br> This versatile self-contained $Z 80$ timer controls eight appliances with 100 on-off settings using coded r.f. bursts injected in the mains supply. |
| Short-wave loop aerial <br> by G. Wareham Using Mukherjee's April 1985 design with clomestic receivers. |  |
|  | 68000 hoard - 5 <br> by R.F. Coates Guided tour of the Kaybug monitor software's 26 system calls. |
| Compact disc mastering <br> by J.R. Watkinson <br> The confusion about p.c.m. adapters and video recorders is explained, together with the formats. |  |
|  | D.b.s. - a plan in search of 75 some users <br> by Tom Ivall <br> An element of confusion still attends plans for satellite television, in spite of two international conferences. Tom Ivall explains. |
| Synchrodyne a.m. receiver 53 <br> by J.L. Linsley Hood Circuit details and setting-up procedure for the phase-locked oscillator. |  |

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Shaft encoder counting.

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## New products

Super-fast floppy Speech recognition. New 6800 with MMU. Super-fast 16/32-bit processor.


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Advertising 01-661 3130.
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LEVELL COUNTERS MET100/600/1000 £99/126/175 8 digit $05^{\prime \prime}$ LED display. 5 Hz to $100600^{\prime} 1000 \mathrm{MHz}$ Resolves 0.1 Hz . Sensitivity 5 mV up to 10 MHz . Low pass filter. Mains/rechargeable battery powered

LEVELL FUNCTION GENERATORS TG302/3 £156/236 0.02 Hz 2 MHz in 7 ranges. Sine, square, trangle, pulse and ramp 20 mV to 20 Vpp from 50 O . DC offset $\mathrm{O}=10 \mathrm{~V}$. TL output. TG303 also has a CMOS output and 6 digi 1 MHz counter with INT EXT switch.

LEVELL RC OSCILLATORS TG152D/DM £95/120 $3 \mathrm{~Hz} \cdot 300 \mathrm{kHz}$. 5 ranges, acc $2 \%+0.1 \mathrm{~Hz}$ up to 100 kHz $3 \%$ at 300 kHz Sine or square $<20 \mathrm{qu}$ to 2.5 Vms . Distn $<02 \% 50 \mathrm{~Hz} .50 \mathrm{kHz}$ DM has an output meter.

LEVELL RC OSCHLLATORS TG200D/DMP £130/165 $1 \mathrm{~Hz} \dagger \mathrm{MHz}$. 12 ranges, acc $1.5 \%+0.01 \mathrm{~Hz}$ to 100 kHz $2 \%$ at 1 MHz . Sine or square outputs $<20 \mathrm{q}_{1} \mathrm{~V} \cdot 7 \mathrm{Vms}$ Distortion $<0.05 \% 50 \mathrm{~Hz}-15 \mathrm{kHz}$. Sync output $>1 \mathrm{~V}$. DMP has output meter and fine frequency control.

LEVELL DECADE OSCILLATOR TG66A
$£ 330$ $0.2 \mathrm{~Hz}-1.22 \mathrm{MHz}$. 5 ranges. 4 digıts, acc $0.3 \%$ $6 \mathrm{~Hz}-100 \mathrm{kHz}$. Sine output $<3 \mathrm{q}_{\mathrm{N}} \mathrm{V}-5 \mathrm{Vmms} .-2 \mathrm{~dB} /+4 \mathrm{~dB}$ and $V$ scales. Distn.<0.15\% 15 Hz -150kHz. Mans/battery

## ANALOGUE METERS

LEVELL AC MICROVOLTMETERS TM3A/B £150/170 16 ranges $15 \mu \mathrm{Vfs} / 500 \mathrm{~V} f \mathrm{~s}$, accuracy $1 \%+1 \% \mathrm{fs}+1 \mu \mathrm{~V}$ $20 \mathrm{~dB}+6 \mathrm{~dB}$ scale. $\pm 3 \mathrm{~dB} 1 \mathrm{~Hz} \cdot 3 \mathrm{MHz} .150 \mathrm{mV}$ fs output TM3A: 83 mm scale. TM3B: 123 mm scale and LF filter.

LEVELL BROADBAND VOLTMETERS TMGA/B
£235/265 16 LF ranges as $\mathrm{TM} 3 \mathrm{~A} / \mathrm{B}+8 \mathrm{HF}$ ranges $1 \mathrm{mVfs} / 3 \mathrm{Vfs}$, accuracy $4 \%+1 \%$ fs at $30 \mathrm{MHz} . \pm 3 \mathrm{~dB} 300 \mathrm{kHz} 400 \mathrm{MHz}$.

LEVELL DC MICROVOLTMETER TM8
£130
23 linear ranges $\pm 3 \mu \mathrm{~V} 4300 \mathrm{~V}$ and $\pm 3 \mathrm{pA} \pm 300 \mathrm{nA}$ plus 2 $\log$ ranges for nulling. Output $\pm 300 \mathrm{mV}$ at fs.

LEVELL DC MULTIMETERS TM9A/BP £199/235 18 voltage ranges $3 \mu \mathrm{~V} / 1 \mathrm{kV} f$ s. Current ranges 3 pA to 1 A (TM9A 1 mA ). Linear $R$ ranges $3 \Omega$ to $1 \mathrm{G} \Omega$

LEVELL MULTTTESTER TM11
£175
$5 q^{2} \mathrm{~V} / 500 \mathrm{~V}$ fs ac, $50 \mathrm{pA} / 500 \mathrm{mAfs}$ ac. $15 \mathrm{qu}_{\mathrm{V}} / 500 \mathrm{Vfs}$ dc, $150 \mathrm{pA} A^{\prime} 500 \mathrm{mAts}$ dc, $0.2 \Omega$ to $100 \mathrm{G} \Omega$. lin'log null. Diode/LED test. Optional RF, HV and Temperature.

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Transistor, diode and zener leakage to $0.5 n A$ at 2 V .150 V Breakdown to 100 V at $1 \mathrm{quA}, 10 \mathrm{quA}, 1 \mathrm{~mA}$. Gain at $1 \mu \mathrm{~A} \cdot 100 \mathrm{~mA}$. Vsat and Vie at 1 mA 100 mA .

## LEVELL INSULATON TESTER TM14

E210 Log scale covers 6 decades $10 \mathrm{M} \Omega 10 \mathrm{~T} \Omega$ at 250 V , $500 \mathrm{~V}, 750 \mathrm{~V}, 1 \mathrm{kV} ; 1 \mathrm{M}-1 \mathrm{~T} \Omega$ at $25 \mathrm{~V} \cdot 100 \mathrm{~V} ; 100 \mathrm{k} \cdot 100 \mathrm{G} \Omega$ at $2.5 \mathrm{~V} 10 \mathrm{~V} ; 10 \mathrm{k} 10 \mathrm{G} \Omega$ at 1 V . Current 100 pA 10 Gu A.

## DICITAL METERS

LEVELL DIGITAL THERMOMETER DT1K E44 $120^{\circ} \mathrm{C}+820^{\circ} \mathrm{C}$, acc $0.2 \% \pm 1^{\circ} \mathrm{C} .3$ digit 8.5 mm LCD. A standard Type K thermocouple socket is fitted. Bead couple is supplied. Battery life $>3000 \mathrm{hrs}$

THURLBY DIGIT AL CAPACITANCE METER CM200 £89 1 pF to 250 MF , acc $0.2 \%$. $4^{1 / 2}$ digit 9 mm LCD. Fast settling. 3 readings per second. Mains/battery.

THURLBY DMMs 1503/1503HA/1504 £169/185/199 $4^{3 / 4}$ digit LCD. Up to $1.2 \mathrm{kVdc}, 750 \mathrm{Vac}, 10 \mathrm{~A} .32 \mathrm{MO}$. 4 MHz Resoln. $10 \mathrm{~V}, 10 \mathrm{nA}, 10 \mathrm{~m} \Omega$. Mans battery 1503: dcV 0.05\%. 1503HA: 0.03\%. 1504: True mis ac THURLBY INTELLIGENT MULTIMETER 1905a £349 $5^{\prime} z$ digit LED. Up to $1.1 \mathrm{kVdc}, 750 \mathrm{Vac}, 5 \mathrm{~A}, 21 \mathrm{M} \Omega$. Resoln. $1 \mu \mathrm{~V}, 1 \mathrm{nA}, 1 \mathrm{~m} \Omega$. dcV $0.015 \%$. Computing and storage functions. RS232/IEEE interface optons.

# LEVELL 

## for INSTRUMENTS



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THURLBY DUALS PL3100MD/3200MD £269/339 Two O.30V O-1A (2A on 320) with isolated, seres tracking, series or parallel modes of operation.

THURLBY TRIPLES PL310K/320K E275/345 $310 \mathrm{~K}: 0.30 \mathrm{~V}$ at $01 \mathrm{~A}, 0.30 \mathrm{~V}$ at $1 / 2 \mathrm{~A} \& 4 \mathrm{~V}-6 \mathrm{~V}$ at $31 / \mathrm{A}$. $320 \mathrm{~K}: 0.30 \mathrm{~V}$ at $02 \mathrm{~A}, 0.30 \mathrm{~V}$ at $1 \mathrm{~A} \& 4 \mathrm{~V} 6 \mathrm{~V}$ at 7 A .

## OSCILLOSCOPES

CROTECH SINGLE TRACE 2OMHz 3031/36 £195/216 2 mV 10 V div $40 \mathrm{~ns}-0.2 \mathrm{~s}$ div. Component tester 3031: CRT $1.5 \mathrm{kV} \mathrm{5} \mathrm{\times 7cm} \mathrm{} .\mathrm{3036} \mathrm{:} \mathrm{CRT} \mathrm{2kV8} \mathrm{\times 10cm.40}$
CROTECH DUAL TRACE 2OMHz (@2mV) 3132 £295 $2 \mathrm{mV} \cdot 10 \mathrm{~V} \mathrm{~cm} . \mathrm{Ch} 1 \pm \mathrm{Ch} 2 . \mathrm{X}-\mathrm{Y}$ mode. Cal 0.2 V 1 kHz sq . 40 ns 02 s cm . Auto, normal or TV trig. Component comparator. DC outputs. $Z$ input. CRT $2 \mathrm{kV} 8 \times 10 \mathrm{~cm}$

CROTECH DUAL TRACE 30MHz (@5mV) 3337/39
£425/570 $5 \mathrm{mV} \cdot 50 \mathrm{~V} / \mathrm{cm}$. Ch $1 \pm \mathrm{Ch} 2$. Signal delay. $X Y$ mode 40 ns 1 s cm . Auto, normal or single shot trigger. Cal $O 2 \mathrm{~V}$ 1 kHz square. $Z$ mput. CRT $10 \mathrm{kV} 8 \times 10 \mathrm{~cm}$
3339: VDU mode. Component tester. DC outputs.
HAMEG DUAL TRACE 20MHz (@2mV) HM203-5£270 $2 \mathrm{mV} 20 \mathrm{~V} / \mathrm{cm}$. Ch $2+\mathrm{Ch} 1$. X-Y Cal 0.2 V 2 V 1 kHz sq. $20 \mathrm{~ns}-0.2 \mathrm{~s} / \mathrm{cm}$. Auto, normal or TV trig. Component test CRT $2 \mathrm{kV} 8 \times 10 \mathrm{~cm}$. Long decay CRT E 25 extra.

HAMEG DUAL TRACE 20MHz (@5mV) HM204-2 £365 $1 \mathrm{mV}-50 \mathrm{~V} / \mathrm{cm}$. Ch2 2 Ch 1 . Sig delay. $X Y$ mode. $Y$ out $10 \mathrm{~ns} \cdot 1.25 \mathrm{~s} / \mathrm{cm}$. Sweep delay 100 ns 1 s . Cal 0.2 V 2 V $1 \mathrm{kHz}, 1 \mathrm{MHz}$. Z input. Comp. test. CRT $2 \mathrm{kV} 8 \times 40 \mathrm{~cm}$.

HAMEG DUAL TRACE 60MHz (@5mV) HM605 £515 $1 \mathrm{mV}-50 \mathrm{~V} / \mathrm{cm}$. Ch $2 \pm \mathrm{Ch} 1$. Sig delay, $X \cdot Y$ mode $Y$ out. 5 ns 2.5 s cm . Sweep delay 100 ns 1 s . Cal 0.2 V 2 V 1 kHz 1 MHz . $Z$ input Comp. test. CRT $14 \mathrm{kV} 8 \times 10 \mathrm{~cm}$.

HAMEG DIGITAL STORAGE 20MHz HM208 £1300 1 mV 50 V cm . Ch $2+\mathrm{Ch} 1$. Single shot and $X Y$ modes $20 \mathrm{~ns}-0.25 \mathrm{~s} / \mathrm{cm}$. 20 MHz sampling. Two 2 K memores Plotter output $0.1 \mathrm{~V} / \mathrm{cm}, 10 \mathrm{~s} / \mathrm{cm}$. CRT $14 \mathrm{kV} 8 \times 10 \mathrm{~cm}$.

HITACHI BATTERY DUAL 20MHz (@5mV) V209 £680 1 mV 12 V div. Ch1 $1 \pm \mathrm{Ch} 2 . X Y$ mode. Cal 0.5 V 1 kHz . $50 \mathrm{~ns}-0.5 \mathrm{~s} \mathrm{~cm}$. Auto, normal or TV triq. Internal rechargeable batt. or mains. CRT $1.5 \mathrm{kV} 5 \times 6.3 \mathrm{~cm}$.

HITACHI DUAL 2OMHz V212/22/23 £299/395/450 1 mV -12V cm. 20MHz@5mV. Ch1 $\pm \mathrm{Ch} 2$. X-Y. Ch1 output. $100 \mathrm{~ns} 0.5 \mathrm{~s} / \mathrm{cm}$. Auto, normal or TV trigger Cal 0.5 V 1 kHz square. Z input. CRT $2 \mathrm{kV} 8 \times 10 \mathrm{~cm}$. $\vee 222 N 223$ : DC offset and alternate magnify. $\vee 223$ Sweep delav $1 \mu \mathrm{~s}-100 \mathrm{~ms}$.

HITACHI DUAL 40MHz (@5mV) V422/23 £580/650 As V222 V 223 but $40 \mathrm{MHz}, 20 \mathrm{~ns} \mathrm{~cm}$ and 12 kV on CRT

HITACHI QUAD $100 \mathrm{MHz}(@ 5 \mathrm{mV}$ ) V1050F £ 1095 Ch1/Ch2: $0.5 \mathrm{mV}-12 \mathrm{~V} / \mathrm{cm}$. Trigger Ch3 Ch4: $0.2 \mathrm{~V} / \mathrm{cm}$ Dual time bases $2 \mathrm{~ns}-0.5 \mathrm{~s}^{\prime} \mathrm{cm}$ and 2 ns 50 ms cm . Signal and sweep delay. CRT $20 \mathrm{kV} 8 \times 10 \mathrm{~cm}$.

HITACHI QUAD 100MHz V1070/1100A £ $1580 / 2390$ Ch1/Ch2: $1 \mathrm{mV}-12 \mathrm{~V} / \mathrm{cm} . \mathrm{CH} 3 \mathrm{Ch} 4: \quad 0.1 \mathrm{~V}-0.5 \mathrm{~V} / \mathrm{cm}$ Dual time bases $2 \mathrm{~ns}-0.5 \mathrm{sicm}$ and $2 \mathrm{~ns}-50 \mathrm{~ms} \mathrm{~cm}$ Digital display of set values. CRT $18 \mathrm{kV} 8 \times 10 \mathrm{~cm}$ V1100A: Digital display of ACV. DCV. frequency

HITACHI DIGITAL STORAGE 10MHz VC6015 £1350 $5 \mathrm{mV}-12 \mathrm{~V} \mathrm{~cm}$. Ch $1 \pm \mathrm{Ch} 2$. Single shot and $X-Y$ modes. lOOns 05 scm .1 MHz sampling. Two 1 K memories Plotter output $1 \mathrm{~V} \mathrm{~cm}, 510 \mathrm{~s} / \mathrm{cm}$. CRT $2 \mathrm{kV} 8 \times 10 \mathrm{~cm}$

HITACHI DIGITAL STORAGE 40 MHz VC6041 £3850 $1 \mathrm{mV} \cdot 12 \mathrm{~V} / \mathrm{cm}$. Ch $1 \pm \mathrm{Ch} 2$. Single shot and $X \cdot Y$ modes. $20 \mathrm{~ns} 0.5 \mathrm{~s} / \mathrm{cm}$. 40 MHz sampling. Two 4 K memories. Plotter output $1 \mathrm{~V} \mathrm{~cm}, 210 \mathrm{scm}$ CRT $12 \mathrm{kV} 8 \times 10 \mathrm{~cm}$.

THURLBY 8 CHANNEL MULTIPLEXER OM358 £179 Increases any oscilloscope to 8 channels. Choice of trigger from any channel. Response DC- 35 MHz .

## LEVELL DECADE BOXES

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## The price of entertainment

Possibly one or two well-heeled readers may have received satellite dishes in their Christmas stockings. If so, they will probably be too busy watching Mirrorvision,
Teleclub, RAIuno and the rest to worry much about the future of tv: no doubt they think they already have it.
The mushrooming satellite tv industry is installing small 12 GHz terminals as fast as it can get them and already there are many in private hands. But even though the high-street rental chains can now offer you a system on monthly instalments, satellite tv is likely to stay very much a rich man's toy.

Of course, true d.b.s.
television for all has yet to arrive in Europe. But when it does, it is hard to believe that the price of terminals will fall to the levels which the public is willing to pay for conventional aerial installations (which is to say, pratically nothing).

And now the prospect of still greater expense is on the horizon for satellite tvwatchers, with the introduction of high-definition tv. Satellite transmission gives the perfect opportunity to introduce new
technical standards which can by-pass the shortcomings of our present system. In Japan, an 1125 -line, 60 -field standard, devised by Sony and adopted by the Japanese broadcasting corporation NHK has already been chosen for the d.b.s. service to come into operation there in 1988.
The CCIR has so far shown no taste for this system. But there will be pressure from other 60 Hz countries, notably the US, to adopt it as a de-facto world standard.
This pressure ought to be resisted. For all its qualities and the pictures and sound it gives are all that could be desired - the Sony system is quite unsuitable for a public service.

For one thing, it breaches the cardinal principle of technical innovation in broadcasting, which is that you launch a new development only when you have found a way of making it compatible with existing equipment. This principle made possible stereo sound, colour tv, teletext and many other improvements of which the casual viewer is unaware.

Certainly there has to be
major change sometimes. In Britain, the last occasion came with the introduction of u.h.f. tv and the closure of the v.h.f. stations. Though costly for the broadcasters, it went virtually unnoticed by the public.
But high-definition tv is a different matter all round. At a stroke, the Sony system makes all existing equipment obsolete, both in the studio and the viewer's home. This would not necessarily matter but for the enormous cost of its replacement.

The audience for the new service will have to find simultaneously the price of a satellite terminal (the wrong side of $£ 1000$ at current prices), the cost of a special tv set, plus a contribution, somehow or other, to the huge expense of making the programmes. The specialtv set is perhaps the most daunting part. Imagine the cost of a super-high resolution c.r.t. or projection tv with a 5:3 aspect ratio, plus the special processor needed to recover the compressed video signal!
Costs at the transmission end are just as dizzying. Camera, telecines, v.t.rs, production desks, distribution equipment,
all will have to be thrown out. And simultaneous transmission of the new programmes on existing channels will be possible only via complex standards converters (at a quarter-of-a-million pounds a time, according to one source). We can expect few viewers or broadcasters to show much enthusiasm.
Surely a much better solution is that proposed in Britain by the IBA and outlined elsewhere in this issue. The IBA has charted a coherent hierarchy of improvements to the existing standard, a ladder which viewers and broadcasters could ascend each at their own pace.

The biggest step is still the first one, the adoption of C-mac in place of Pal. But with the move towards modular tv receivers and the development of special C-mac i.cs, there is no reason why it should add significantly to the viewer's costs. And the EBU has already declared its support for C-mac.
The goal at the top of the IBA's ladder is just the same, true high-definition tv. But reached this way, it could be affordable.


Steve Webb developed a system for receiving data from the two UOSAT satellites to keep his daughter Jenny, and his two other children, amused. The system, known as Astrid (see WW New Products Oct. 1985), is now being marketed worldwide and has found many enthusiastic users in schools, receiving news and data from space as well as pictures of the earth and cloud formations; useful for amateur weather forecasters.

## World's largest satellite network

Linking 93 locations in 52 countries for Explo 85, an international congress of 15 million Christians, BT International claim that this was the biggest link-up of its type ever. They have organized global satellite links before, for events such as the Olympics, the World Cup, and the recent Live Aid concert. For the congress BT booked broadcast quality tv channels on three Intelsat vehicles, two over the Atlantic
and one over the Indian ocean. Similar channels have been booked on the European regional satellite and on domestic satellite systems over N. America and the Caribbean, Brazil and the Indian subcontinent. The major satellites transmit signals between continents; the signals were then retransmitted to local satellites for reception on locally-sited small-dish anntennae.

## Enhanced C-mac

In the wake of Sony's demonstrations of the 1125 -line tv system chosen for the forthcoming d.b.s. service in Japan, Britain's Independent Broadcasting Authority has been showing the results of its own work on improved television standards.
'Evolution not revolution' is the slogan adopted by the IBA. For whilst the Sony-NHK system (December issue, page 5) represents a major break with existing transmission systems, the IBA aims to reach a high-definition standard gradually, through a series of orderly enhancements to the present
European standard. And in demonstrations staged at their London headquarters in December, IBA engineers showed a transitional highdefinition system based on modified 625 -line equipment and their C-mac transmission system.
Tom Robson, the IBA's director of engineering, while saluting the achievement of the Japanese engineers, stressed the drawbacks of their approach."The 1125/60 system is not satisfactory to Europe and should not be accepted as a worldwide system", he said.
A major problem was the 60 Hz field rate, since threequarters of the world used 50 Hz . And although standards conversion was possible, good conversion was very expensive. According to another IBA engineer, Sony's own h.d.t.v. converter was rumoured to have cost over half a million pounds. And standards conversion could not cope with the 10 Hz beat which arose when 60 Hz equipment was used under 50 Hz studio lights.
But one of the most serious objections, according to Mr Robson, was that direct change to any new system such as Sony's would mean making all existing equipment obsolete
overnight. He said that hroadcasters would find it difficult to finance such a changeover; a high-definition service would be an expensive luxury in its early days and revenues would take a long time to build up.
In the IBA demonstration, live pictures came from a Link Electronics 625 -line camera modified to give the extra width
were impressively realistic, though they still looked like television - in contrast to Sony's, which have the appearance of a superior kind of cinema picture. Even so, the film grain on 35 mm telecine was noticeable at close quarters. Yet the option to enhance resolution later on by increasing the number of lines still remains open under the IBA's scheme.
For comparison, two conventional colour monitors
showed the same pictures
market, which seemed likely to adopt the NHK standard, appeared to see it mainly as a medium for electronic production for the cinema rather than as a broadcast system in its own right.

Describing the IBA system in more detail, Dr Gary Tonge outlined the changes which would take place, both at the studio and in the viewer's home. First, PAL pictures would give way to C -mac as d.b.s.
transmissions were introduced. MAC had been shown to fit well into a satellite channel, and C-mac decoders (which would use chips now at an advanced stage of development) would not add greatly to the cost of a receiving terminal. Then the system could be enhanced by stages to give a wider image, more lines displayed per field and reduced flicker.
So enhanced Cmac would reach the same targets as Sony'sh.d.t.v., but by an evolutionary route rather than
This off-screen photograph shows the $5: 3$ aspect ratio of the IBA's system. When the camera moved closer, the Debussy arabesque on the music-stand could be read clearly enough to be played.
demanded by the $5: 3$ picture aspect ratio, and there were inserts from video recordings and telecine. All signals, with accompanying stereo sound, were coded in the enhanced $C$ mac system (by which the analogue luminance and colour signals are combined by timedivision multiplexing, with a separate time-slot given over to data and digital sound).

Display equipment included a fairly ordinary, though modified, American-made projection ty (which cost, as the engineers gleefully pointed out, about a tenth of the price of Sony's); and a Barco shadowmask monitor fitted with a Japanese tube and some special electronics, which gave a sequential scan of all 625 lines at a 50 Hz repetition rate (twice the normal rate) simulating the linestructure of a 1250 -line picture.

The large-format pictures
through an ordinary C-mac decoder and in PAL form after transcoding. And it could be seen that the double scan of the wide-screen monitor reduced field-rate flicker very effectively, disposing of one of the major advantages claimed for the 60 Hz system.

Mr Robson said that the Japanese approach was based on 12-year-old technology and did not take account of recent developments in tv equipment design - such as the field-store in the wide-screen monitor. (And indeed the charge-coupled delay-line i.cs recently developed by Philips mean that field stores should be appearing in 625-line domestic sets very soon.) Yet it might take years for domestic receiver technology to match the quality which had been shown in h.d.t.v. demonstrations.

And he indicated that the US

## Prize-winning aids for the disabled

Cedric the computer allows the user to select words, letters or symbols from a video screen by sensing the direction of eye movement. It was designed for use by those with high-level paralysis and loss of speech and was a winner of the IEE Prize for helping disabled people. The other joint winner was a device for bladder control for
paraplegics.
The Cedric computer uses very low intensity red light to reflect off either ese and detects the point on a video screen to which the user is looking. Selection is accomplished by eye fixation on the desired word or control can contain more than 1,500
words and there is also a visual keyboard to "type" out letters and words. There is no attachment to the user but a headrest is recommended for comfort and stability. Small head movements are allowed for, as is eye blinking. If the eye moves out of range the screen display tells the user and waits for realignment. Each time the computer is switched on, it is automatically calibrated to the user's eye. The computer can be linked through an RS232 port to a printer or other peripheral and can be used as a remote control system for environmental control, to switch lights or appliances on and off, for example. The joint

Robert Hum is about to test a v.l.s.i. telecommunications circuit in a GenRAD GR 18 i.c. tester. The tester, claimed to be the most advanced in the world, is capable of performing 11520000000 tests per second. So it would have completed about 170 billion tests in the time it takes to read this paragraph. Mr Hum works for BellNorthern Research in Canada on the development of v.l.s.i. circuits for Northern Telecom. The manufacture of reliable chips depends on the ability of the research centre in understanding how and why chips fail and then on the ability to prevent such occurances.


## Open technology

A technical college equivalent of the Open University las been launched bs Telford College Edinburgh.called Teltec. Each course consists of practicalkits. audio and videotapes and texts and coverssuchareas as control and instrumentation, electronics, microelectronics, pneumatics and hydraulics, electrical skills and computer appreciation. Tutorial
centres are located throughout the country so that students can have expert guidance when needed.
Tutors can also work under contract to individual companies to provide in-house training.
If Teltec does not offer a course required they can trace and request a suitable package from another participant in the Open Tech scheme.
prizewinner was Cedric's inventor, Andrew Downing, senior lecturer in electrical and electronic engineering at Adelaide University

The other prizewinner was Peter Donaldson, chief engineer at the MRC neurological prosthesis unit. The bladder controller treats incontinence by electrical stimulation of the sacral anterior roots in the spine. A receiver unit is planted beneath the ribs and is controlled by a transmitter held adjacent to it outside the body

Signals from the receiver are connected by implanted cables to the nerves in the spinal column.

## Alvey's Flagship

Flagship is the major demonstration model for the Alvey advanced computer research programme. Much accent is placed on the need for parallel processing and also on 'declarative' programming languages which improve the computer interface and enable the user to tell the computer what to do in plain language.
The project is the joint responsibility of Plessey, ICL, Manchester University and Imperial College, London. Manchester University has developed a data-flow computer and Imperial College are working on Alice, a graph reduction machine which uses about 200 Inmos Tranputers.
Plessey's contribution will be in speech recognition and synthesis and in v.l.s.i. design, under the leadership of Dr. Keith Warren.
We suggested to Dr. Warren that task-specific transputers would be the next logical step in speeding up the processing, and he agreed but said that they were already progressing beyond the Transputer and were looking at bit-slice processors, some of which may be task-specific.
The computers produced by this research are not aimed at replacing existing systems but at doing tasks not previously possible on a computer, especially in the areas of artificial intelligence and in user/computer interfacing,

As has been predicted for some time, the compact disc can be used to store computer data and used like a rom. Hitachi have produced CD-Rom. Each disc has a read-only memory capacity of 552 Mbits and the data transfer rate is $176 \mathrm{Kbit} / \mathrm{s}$.


Dr David Wright was awarded an Honorary Fellowship of the Royal Television Society. He is a specialist in colour and worked in optics when he became involved in the early development of television. The colour system adopted by the NTSC was based largely on Dr Wright's researches. He was Professor of Technical Optics at Imperial College, and has published many papers and a standard reference work: The measurement of colour.

The next generation of mobile telephone systems in Europe is under consideration at Ericsson. Basing their researches on the existing Nordic cellular system and on experiences in other areas of the world, Ericsson will present the results of their deliberations to the European
Telecommunications Administration during this year.

A better deal for disabled and elderly telephone users is called for by DIEL, an independent advisory committee on telecommunications for the disabled and elderly. They are particularly concerned that the research into low data-rate visual phone system should continue at Essex University and that such users should be relieved from paying vat on equipment and services.

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| 7014 | 525 MHz Ditigal Counter | ¢850 |
| 7 M 11 | Delay Line | ¢750 |
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## AFGODFGES Hewlett Packard

Hewlett Packard
$4204 A$
Decade Osc（New）

Wavetek Decade Osc（New）
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6054800

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Hewlett Packard

2950
82100

| Marconi | ＇Q＇Meter | C1200 |
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| TF1246 | Oscillator | C650 |
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| GEणन： |  |  |
| luke |  |  |
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|  | M．D．S．Terminal | ¢9000 |
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SOFTY II

| SOFTY |  | MALE |  |  |  |  |
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| This low cost inteligent eprom progra | er can program 2716. 2516. | Ang Pins | 120 | 180 | 230 | 350 |
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|  |  |  | 175 | 275 | 325 |  |
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| Adaplor for | 2764! | Ang Pins | 160 | 210 | 275 | 440 |
| 2564 | £25.00 | Solder | 90 | 130 |  | - |
| SPECIAL |  |  | 195 | 325 | 375 |  |
| 2764-25 £ 2 : | O(d). | St Hood | . 90 | 95 | 100 | 120 |
| 27128-25 £ | O(d): | $\begin{aligned} & \text { Screw } \\ & \text { Lock } \end{aligned}$ |  |  |  |  |
| 6264 LP-15 £ | 00(d); |  |  |  |  |  |
| ACORN IEEE INTERFACE£278(a) | industrial programmer EP8000〔695 (a) | SOCKETS <br> 28-pin 99.00 |  |  | $\begin{aligned} & 24-\mathrm{p} \\ & 40 \text { pr } \end{aligned}$ | $\begin{gathered} n \in 7.50 \\ \varepsilon \in 12.00 \end{gathered}$ |

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Stacked Versions
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3.5' Drives

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Buitt-in safety interiock to avoid accidental exposure Buit-in safety interlock to avoid accidental exposure
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| (grey/metre) |  |  |  |
| $10-$ way | $40 p$ | 34 -way | $160 p$ |
| 16 -way | $60 p$ | 40 way | $180 p$ |
| 20 -way | 85p | 50 -way | 200 p |
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| DIL HEADERS |  |  |
| :---: | :---: | :---: |
|  |  |  |
| 14 pin | Solder | 10 C |
| 16 pin | 50 p | 100 p |
| 18 pin | 60 p | 110 p |
| 20 pin | 75 p | - |
| 24 pin | 100 p | 150 p |
| 28 pin | 160 p | 200 p |
| 40 pin | 200 p | 225 p |

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\hline \multicolumn{2}{|l|}{74 Series} \& \& 7415273125 \& tac Series \& \multirow[t]{2}{*}{\begin{tabular}{ll}
4076 \& 0.65 \\
4077 \& 0.25 \\
4078 \& 0.25 \\
\hline
\end{tabular}} \& \multicolumn{3}{|c|}{LINEARICs} \& \multicolumn{5}{|c|}{COMPUTER COMPONENTS} \\
\hline 7400 \& 0.30 \& \begin{tabular}{ll}
74276 \\
78278 \\
\hline 7.190
\end{tabular} \& \({ }_{7} 74\) LS5289 01.90 \& \& \& AD7581 12.00 \& LM710 0.48 \& PBA64t8X1 4.00 \& \& TMS 450014.00 \& epron \& \& xeyboamd \\
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74283 \\
74792 \& 1.05 \\
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\end{tabular} \& 74452900.80 \& \(\begin{array}{ll}74 \mathrm{CO}^{4} \& 0.50 \\ 74008 \\ 0.70\end{array}\) \& （1082 \begin{tabular}{ll}
4082 \\
4085 \\
0.60 \\
0.25 \\
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\end{tabular} \& \({ }^{\text {A A P79，900 } 25.000}\) \&  \& \begin{tabular}{ll} 
TAAB30 \\
TBA80 \& 0.80 \\
0.90 \\
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\end{tabular} \& \begin{tabular}{ll}
\(1802 C E\) \\
26504 \\
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\end{tabular} \& TMS9902 \({ }^{\text {S }}\) \& 2566＋5V 3．50 \& \({ }^{75160}\) \& \\
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74293 \& 0.90 \\
74298 \& 1.80 \\
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\end{tabular} \& 744S295 1.40 \& \(\begin{array}{ll}74 C 14 \& 0.50 \\ 74 C 20 \& 0.70\end{array}\) \& \(\begin{array}{ll}4089 \& 1.25 \\ 4093 \& 0.35\end{array}\) \& AY－3．9910 4.900 \& \begin{tabular}{lll} 
LM 741 \\
LM747 \& 0.722 \\
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\end{tabular} \& \begin{tabular}{l} 
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TBA920 \\
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2564 \& 7517 \& \begin{tabular}{l}
\(74 C 922\) \\
\(74 C 923\) \\
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\end{tabular} \\
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4094 \\
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743654 \\
74368 \\
\hline 0.80
\end{tabular} \& \({ }_{74455321} 7.70\) \& \begin{tabular}{ll}
74448 \\
7448 \\
\hline 1.50 \\
\hline
\end{tabular} \& \({ }^{40965}\) \& CA3028A 1.10 \&  \& TCA210 3.50 \& \begin{tabular}{ll}
65828 \\
6800 \& 8.50 \\
\hline 8.50
\end{tabular} \& \begin{tabular}{l} 
z80CrC \\
Z80aCTC \\
2.505 \\
\hline 2.75
\end{tabular} \& \({ }_{2}^{27716+5 V^{4}} \mathbf{4} 5.50\) \& \(\begin{array}{ll}75189 \& 0.60 \\ 75365 \& 1.50\end{array}\) \& \\
\hline 7410 \& 0.30 \& \(743674 \quad 0.80\) \& \({ }^{7} 44.5332243 .90\) \& \(74 C 731.00\) \& \begin{tabular}{lll}
4097 \& 2.70 \\
\hline 098 \\
0.75
\end{tabular} \& CA3046 0.70 \& LM18013 3.00 \& TCA220 3.50 \& \({ }^{6802} 33.00\) \& R800AAPT 6.50 \& \({ }^{2716-35} 5.50\) \& \({ }_{75450} \quad 0.80\) \& ditaraios \\
\hline \& 0.3 \& 74376 \& \({ }_{7}^{7445323} 3.00\) \& \begin{tabular}{ll}
\(74 C 74\) \& 1.20 \\
74767 \& 100 \\
\hline
\end{tabular} \& \begin{tabular}{ll}
4098 \\
4099 \& 0.75 \\
\hline 0.99
\end{tabular} \& \begin{tabular}{l} 
CA3359 \\
CA3060 \\
\hline 3．50
\end{tabular} \& \begin{tabular}{l} 
LM1830 \\
\hline 18.50 \\
\hline M1871 \\
3
\end{tabular} \& TCA940 1.75 \&  \& \& 4．50 \& \& \\
\hline 7413 \& 0.50 \& 743931.20 \& 74 L53982 200 \& \(\begin{array}{ll}74 C 83 \& 2.00\end{array}\) \&  \& CA3080E 0.70 \& LM1872 3.00 \& TDA 1004 A 5.00 \& \({ }^{6809 E} 10.00\) \& 00 \& \& \begin{tabular}{lll}
75452 \\
75453 \\
\hline 7.70
\end{tabular} \& M81166．50 \\
\hline 74 \& 0.70 \& \& 744 \& \begin{tabular}{ll}
744685 \& 2.25 \\
\(74 C 868\) \& 0.50 \\
\hline 74
\end{tabular} \& \({ }_{4503}{ }^{4502} \begin{array}{ll}0.36\end{array}\) \& CA3085 1.50 \& LM18866 6.00 \& TDA1022 4.50 \& 6880910.00
68809 E 12.00 \& \& 2732A－30 6.00 \& \(\begin{array}{ll}75454 \& 0.70\end{array}\) \& \\
\hline 7417
7420 \& 0.40 \& \multirow[t]{2}{*}{Tus senit} \& \multirow[t]{2}{*}{7445356
74 LS 363
1.180 74L．S364 1.80} \& \begin{tabular}{ll}
\(74 C 90\) \\
\hline \(74 C 93\) \& 1.90 \\
\hline
\end{tabular} \& \({ }_{4504}^{4504}\) \& \multirow[t]{2}{*}{CA3089E2．50} \& \multirow[t]{2}{*}{\begin{tabular}{l} 
LM 2917 \\
LM3302 \\
\hline 0.90 \\
\hline 1000
\end{tabular}} \&  \& 68800－LB 36，00 \& 5100／2／9 7.00 \& \multirow[t]{2}{*}{2764－25 2.00 \(27 \mathrm{C} 64-2510.00\)} \& \multirow[t]{2}{*}{\[
\begin{aligned}
\& 75490 \\
\& 7599 \\
\& 75992
\end{aligned}
\]} \& \multirow[t]{2}{*}{UARTs} \\
\hline 742 \& 0.60 \& \& \& \({ }_{74 C 95} 1.56\) \& \begin{tabular}{ll}
4506 \\
4509 \\
\hline 0.95
\end{tabular} \& \& \& TDA2002 3.25 \& \& 2808P10 5.00 \& \& \& \\
\hline \& －0．36 \& 7415000024 \& \[
\begin{aligned}
\& 74 L .5364 \\
\& 74 L S 5650.80 \\
\& \hline
\end{aligned}
\] \& \begin{tabular}{l}
\(74 C 107\) \\
740150 \\
\hline 1000
\end{tabular} \& \(4508 \quad 1.20\) \& CA3140 \&  \& TDA2003 1．90 \& \(\begin{array}{ll}80 C 35 \& 6.00 \\ 8039\end{array}\) \& 2808CTC 5 5000 \& \multirow[t]{5}{*}{27128－25 3．00 27128－257．50 27256－25 20.00 \(27256-30 \quad 12.00\)
17258 27512 P．O．A
TMS2716 5.00} \& \({ }^{8126} \quad 120\) \& \multirow[t]{4}{*}{\begin{tabular}{l}
AY310．5P 3.00 \\
AY51013P 3.0 \\
\begin{tabular}{ll} 
\\
M6402 \& 4.50 \\
\hline
\end{tabular}
\end{tabular}} \\
\hline \& 0.40 \&  \& \& \({ }^{744151512.00}\) \& \begin{tabular}{ll}
4510 \& 0.55 \\
4511 \& 0.55 \\
\hline
\end{tabular} \& CA3140才 1.00 \& LM3914 3.50 \& \begin{tabular}{l} 
TDA2006 3.20 \\
TDA2020 3.20 \\
\hline
\end{tabular} \& \({ }^{80 C 39} 77.00\) \& \& \& \({ }^{81795} 11.20\) \& \\
\hline 7427 \& 0.32 \& 74450310.24 \& \({ }_{7} 74.543730 .90\) \& \begin{tabular}{l}
744160 \\
\hline 1.80 \\
\hline 14
\end{tabular} \& \begin{tabular}{ll}
4512 \& 0.55 \\
4513 \\
\hline 150 \\
\hline
\end{tabular} \& \multirow[t]{2}{*}{CA3360E 1.50
CA3615 2.00
Ca3162E 6.00} \& LM3916 3.40 \& TDAZOO30 2.50 \& \({ }^{80885 A} \quad 3.00\) \& \multirow[t]{2}{*}{vemonies} \& \& \(\begin{array}{ll}8796 \\ 8197 \\ 8 \& 1.20 \\ 1.20\end{array}\) \& \\
\hline \& 0.43 \& 741504 0.24 \& 7445374 0 \& \({ }_{74 C 16151.80}\) \& \({ }_{4513}^{4513}\) \& \& LM39600 1.50 \& \({ }^{\text {TOA } 259395.00 ~}\) \& \begin{tabular}{l}
800854 \\
8086 \\
\hline 8.50 \\
22.00
\end{tabular} \& \& \& \[
\begin{array}{ll}
8797 \& 1.20 \\
8198 \& 120
\end{array}
\] \& \\
\hline 7432 \& 0.36 \& 744508080 \& \({ }_{7} 7453771.30\) \& \({ }_{744163} 1.800\) \& \begin{tabular}{ll}
4515 \\
\hline 516 \& 1.10 \\
\hline 055
\end{tabular} \& \multirow[t]{2}{*}{CA3189E 2.70
CA3240 1.50
CA3280G
3．00} \& M51513L 2.30 \& TDA35607．50 \& \& \multirow[t]{2}{*}{\begin{tabular}{ll}
\(216-150\) \& 4.00 \\
2101 \& 4.00 \\
2102 \& 2.50 \\
\(2107 B\) \& 5.00 \\
\&
\end{tabular}} \& \& \multirow[t]{2}{*}{\[
\begin{array}{lr}
81 L S 95 \& 1.40 \\
81 L S 96 \\
81.40 \\
81 L S 97 \& 1.40
\end{array}
\]} \& modulions \\
\hline 7433
743 \& 0.30 \&  \& \begin{tabular}{l}
7445378 \\
7415379 \\
\hline 1.95 \\
\hline 180
\end{tabular} \& \begin{tabular}{l} 
74C173 \\
\hline \(74 C 174\) \\
\hline 1.50 \\
\hline
\end{tabular} \&  \& \&  \&  \& \(8741 \quad 15.00\) \& \& \multirow[t]{2}{*}{COWITRTLER} \& \& \\
\hline 7438 \& 0.40 \& \(\begin{array}{llll}74 L 511 \& 0.24\end{array}\) \& \multirow[t]{2}{*}{74453814.50
74 S 3855
3.25} \& 7441751.50 \& \& 07002 6.000 \& 1413 0．75 \& TEA 10027.00 \& \(8748 \quad 16.00\) \& 2111 A－35 4.00 \& \& \begin{tabular}{l}
\(\begin{array}{ll}81 \text { LS97 } \& 1.40 \\ 81 \text { LS98 } \& 1.40\end{array}\) \\
88 LS 1203.00
\end{tabular} \& \multirow[t]{2}{*}{\(\begin{array}{ll}\text { 6MH2 } \& 3.75 \\ 8 \mathrm{MHz} \& 4.50\end{array}\)} \\
\hline 77440 \& \({ }_{0}^{0.40}\) \& 74LS 14.0 .50 \& \& \begin{tabular}{l} 
744C193 \\
\(74 C 194\) \\
\hline 1.50 \\
\hline 740
\end{tabular} \& \(4520 \quad 0.60\) \& DACO8003．00 \& MC1495 3.00 \& \({ }^{\text {TLO62 }}\) \& \multirow[t]{3}{*}{\[
\begin{array}{ll}
\text { TMS: } 1601 \& 12.00 \\
\text { TMS99980 } 14.50 \\
\text { TMS9995 } \& 12.00
\end{array}
\]} \& \begin{tabular}{lll}
2114 \\
\(214-2\) \& \& 3.50 \\
\hline 2.50
\end{tabular} \& RT5027 18.00 \& \& \\
\hline 744 \& 0.90 \& 74LS15 0.24 \& \({ }^{7} 745353391\) \& \begin{tabular}{l}
\(74 C 195\) \\
\hline 74505
\end{tabular} \& \begin{tabular}{ll}
4521 \\
4522 \& 1.15 \\
\hline 0.80
\end{tabular} \& DACO8083．00 \& MC149660．70 \& TLO64 0.90 \& \& \& \multirow[t]{2}{*}{EF9364 8.00} \& \multirow[t]{2}{*}{\[
\begin{array}{ll}
9602 \& 3.00 \\
9636 A \\
9637 A P \& 1.60 \\
\hline 9.60
\end{array}
\]} \& \multirow[t]{2}{*}{\[
\begin{aligned}
\& \text { sound a } \\
\& \text { viskow }
\end{aligned}
\]} \\
\hline \begin{tabular}{l}
744 \\
744 \\
\hline
\end{tabular} \& 1.00 \& 74LS21 \& \({ }_{74 L 5399} 1.40\) \&  \& \({ }_{4526} \quad 0.70\) \& HA1366 1.90 \& мСЗ 34010 \& TLO72 0.70 \& \& \& \& \& \\
\hline 744 \& \({ }^{1.10}\) \& 744－S22
7
\(74 L S 24\)
0.24
0.50 \& \multirow[t]{2}{*}{\({ }^{744.5465} 1.120\)} \& \begin{tabular}{l} 
74C245 \\
\(74 C 373\) \\
\hline 2.25 \\
\hline 2.25 \\
\hline
\end{tabular} \& \begin{tabular}{ll}
4527 \\
4588 \& 0.80 \\
\hline 585
\end{tabular} \& \({ }^{\text {ICLITO66 }}\) \& \begin{tabular}{l} 
MC3401 0.65 \\
MF 100 N \\
\hline 0.10
\end{tabular} \& \multirow[t]{2}{*}{\[
\begin{array}{ll}
\mathrm{TLO81} \& 0.35 \\
\mathrm{TLLO82} \& 0.55 \\
\mathrm{TLO} \& 0.75
\end{array}
\]} \& \multirow[t]{2}{*}{\begin{tabular}{ll}
\(z 80\) \& 2.50 \\
\(z 80\) \& 2.90 \\
\(z 808\) \& 5.50 \\
7804 \& 750 \\
\hline 8
\end{tabular}} \& \(\begin{array}{ll}4116 \\ 4116-20 \& 2.00 \\ 1.50\end{array}\) \& \multirow[t]{2}{*}{\[
\begin{aligned}
\& \text { EF9366 } 2.00 \\
\& \text { EFF9367 } 36.00 \\
\& M C 6845 \\
\& \hline 6.50
\end{aligned}
\]} \& 9637AP 1.60 \& 12 MHz 22.00 \\
\hline 7446 \& 1.00 \& 744－S26 0.26 \& \& \begin{tabular}{l}
744374 \\
\hline 2.25 \\
\hline
\end{tabular} \& \multirow[t]{2}{*}{\(\begin{array}{ll}4529 \\ 453 \\ 453 \& 1.00 \\ 0 \& 0.75\end{array}\)} \& \multirow[t]{2}{*}{} \& MK502409．00 \& \& \& \multirow[t]{3}{*}{\[
\begin{array}{ll}
{ }_{41256-207}^{41256} \& 0.50 \\
\hline 0.50
\end{array}
\]} \& \& \& crustas \\
\hline \({ }_{7448} 7\) \& 1.00 \& \(\begin{array}{ll}\text { 744528 } \& 0.24\end{array}\) \& \multirow[t]{2}{*}{\(74 L 5540\)
74.554
7} \& \begin{tabular}{l}
744992 \\
\(74 C 911\) \\
\hline 9.00 \\
\hline
\end{tabular} \& \& \& \begin{tabular}{l} 
ML50398 \\
ML．902 \\
50.00 \\
\hline 1000
\end{tabular} \& \multirow[t]{2}{*}{\[
\begin{array}{ll} 
\& 0.75 \\
\text { TLOBS } \& 0.75 \\
\text { TLOB4 } \& 1.00 \\
\text { TLO94 } \& 2.00
\end{array}
\]} \& \& \& \multirow[t]{2}{*}{MC6845SP 6.50 MC6847 6.50} \& \multirow[t]{2}{*}{COMISGLER} \& \multirow[t]{2}{*}{crystals} \\
\hline \({ }^{7450}\) \& \({ }^{0.36}\) \& 74LS300 0.2 .24 \& \& \multirow[t]{2}{*}{\(74 C 922\)
76.00
74993
76.50} \& \multirow[t]{2}{*}{\begin{tabular}{ll}
4536 \\
\hline 538 \& 2.50 \\
\hline 855 \\
\hline 8.75
\end{tabular}} \& \multirow[t]{2}{*}{（1CM2168 22.00} \&  \& \& Sulpres \& \& \& \& \\
\hline 745 \& 0.38 \& 744532 0.24 \&  \& \& \& \& \(\begin{array}{ll}\text { M } 4622^{1 / 4} \& 3.00 \\ \text { NE } 529 \\ 2.20\end{array}\) \& \[
\begin{aligned}
\& \mathrm{TLI7O} \\
\& \mathrm{CL} 430 \mathrm{CO} \\
\& 120
\end{aligned}
\] \& \& \[
\begin{array}{ll}
4164.15 T 1 \& 3.00 \\
4164 \\
4
\end{array}
\] \& SFF96364 8.00 MS9918 15.00 MMS9928 10.00 \& \& \begin{tabular}{l}
00 MHz 2.70 \\
1.6432 MHz 2.25
\end{tabular} \\
\hline 7454
7460 \& \({ }_{0}^{0.55}\) \& \begin{tabular}{l} 
744LS33 \\
744537 \\
\hline 0.24 \\
0.24
\end{tabular} \& \({ }^{7} 74.561819 .9000\) \& \multirow[t]{2}{*}{\(74 \mathrm{C926} 7.50\)} \& \(\begin{array}{lll}4541 \& 0.75 \\ 454\end{array}\) \&  \& \multirow[t]{2}{*}{\begin{tabular}{ll} 
NE534 \& 1.20 \\
NE5 \\
NE555 \& 1.92 \\
\hline
\end{tabular}} \& \[
\begin{aligned}
\& \text { UAA } 1003-3.9 .35 \\
\& \text { UAF59 }
\end{aligned}
\] \& \& \multirow[t]{2}{*}{\(\begin{array}{ll}4164-20 \& 2.00 \\ 4416-15 \\ 3.50 \\ 4532-20 \& 2.50\end{array}\)} \& \& \multirow[t]{2}{*}{\[
\begin{array}{rr}
765 A \& 13.00 \\
6843 \& 8.00 \\
8271 \& \text { P.O.A }
\end{array}
\]} \& \[
\begin{aligned}
\& 1.6432 \mathrm{MHR} 2.25 \\
\& 200 \mathrm{MHz} 2.25 \\
\& 2.45760 \mathrm{MH}(\mathrm{~L}) \\
\& 200
\end{aligned}
\] \\
\hline 7470
7472 \& 0.50 \& \begin{tabular}{l}
\(74 L 5388\) \\
\hline 7454
\end{tabular} \& \begin{tabular}{l} 
74LS6626 2.25 \\
74.5628 \\
\hline 2.25 \\
\hline
\end{tabular} \& \& \(\begin{array}{lll}4541 \\ 4543 \& 0.97 \\ 0.70\end{array}\) \& －LC7730 \({ }^{\text {L }}\) \& \& \[
\begin{array}{ll}
\text { UAZ240 } \\
\text { UAA } 170 \\
\hline 170
\end{array}
\] \& \begin{tabular}{ll}
32450 \\
6552 \\
6522 \& 3.00 \\
3 \& 3.50 \\
\hline
\end{tabular} \& \& wTERFACE IC \& \& \[
\begin{array}{r}
2.00 \\
2.45760 \mathrm{MHz}(\mathrm{~S})
\end{array}
\] \\
\hline 7473 \& 0.45 \& 7445420.50 \& \multirow[t]{2}{*}{\begin{tabular}{l}
7445629 \\
\(74 L 5640\) \\
\hline 1.00
\end{tabular}} \& \multirow[t]{2}{*}{74als series} \& \begin{tabular}{ll}
4553 \& 2.40 \\
\hline 155 \& 0.46 \\
\hline
\end{tabular} \& \multirow[t]{2}{*}{} \& \multirow[t]{2}{*}{\begin{tabular}{ll} 
NE556 \\
NE54 \& 4.00 \\
NE565 \& 1.20 \\
\\
\hline
\end{tabular}} \& UAA170 1.70 UCNABOIA 4.00 ULN200：A 0.75 \& \multirow[t]{2}{*}{\begin{tabular}{ll}
65222 \& 3.50 \\
6522 A \& 5.50 \\
6532 \\
6551 A \& 6.80 \\
\hline 680
\end{tabular}} \&  \& \& \multirow[t]{3}{*}{FD1771 20.00 FO1791 20.00 FD1797 22.00} \& 2．45760MHz（S） \\
\hline 7474 \& \({ }^{0.50}\) \&  \& \& \& \multirow[t]{2}{*}{\begin{tabular}{ll}
4556 \\
4557 \& 0.50 \\
\hline 2.40 \\
\hline
\end{tabular}} \& \& \& \multirow[t]{2}{*}{－N20024 0.75 ULN2002A 0.75} \& \& \multirow[t]{2}{*}{5101／1／501 4.00
\(5551 / 51144.00\)
5516} \& \multirow[t]{6}{*}{} \& \& \multirow[t]{2}{*}{\(\begin{array}{ll}2.5 \mathrm{MHz} \& 2.50 \\ 2662 \mathrm{MHz} \& 1.75\end{array}\)} \\
\hline 7476 \& 0.45 \& 74 LS49 1.00 \&  \& \& \& \[
\begin{array}{ll}
\text { LF351 } \& 0.60 \\
\text { LF353 } \& 0.90 \\
\hline
\end{array}
\] \&  \& \& \[
\begin{array}{ll}
6532 \\
6551 \mathrm{~A} \& 4.80 \\
6.00
\end{array}
\] \& \& \& \& \\
\hline \({ }_{7}^{7480}\) \& \({ }_{1}^{0.65}\) \&  \& \multirow[t]{2}{*}{（74LS642－13．00} \& \({ }^{744 \mathrm{LS} \text { SO2 }} 0.45\) \& \({ }_{4566} \quad 1.40\) \& \[
\begin{array}{l|l}
\text { ĽF355 } \& 0.90 \\
\text { LF356N } \& 1.10
\end{array}
\] \& \[
\begin{array}{ll}
\text { NE567 } \& 1.25 \\
\text { NE570 } \& 4.00
\end{array}
\] \& ULN2003A 0.75 ULN2004A 0.75 \& \& \[
\begin{aligned}
\& 5516 \\
\& 5517 \mathrm{AP}
\end{aligned} \begin{aligned}
\& 6.00 \\
\& 6.00
\end{aligned}
\] \& \& \multirow[t]{3}{*}{WD 169115.00 WO2143 12.00 WD2793
WD2797
27.00 W02797 27.00} \&  \\
\hline \({ }_{7}^{748}\) \& \({ }_{1}^{1.25}\) \& 74LS555 00.24 \& \& \multirow[t]{2}{*}{} \& \begin{tabular}{ll}
45668 \\
4569 \& 2.40 \\
4.70 \\
\hline 4.
\end{tabular} \& \multirow[t]{2}{*}{（LF357 10.00} \& \[
\begin{array}{ll}
\text { NEST1 } \& 3.00 \\
\text { NE592 } \& 0.90 \\
\text { NE5532P } \& 1.50
\end{array}
\] \& ULN2068 2.90 ULN2802 1.90 \& \multirow[t]{2}{*}{\[
\begin{array}{lc}
688621 \& 1.50 \\
6820 \\
6890 \& 12.50 \\
6840 \& \\
\hline
\end{array}
\]} \& \({ }_{61,165-3} \mathbf{3}\) 3．50 \& \& \& \(\begin{array}{ll}3.579 \mathrm{MHz} \\ 4.1 .50 \\ 4.194 \mathrm{MHz} \& 1.50 \\ 2.00\end{array}\) \\
\hline \& 0.4 \&  \& 74456433 1.500
7415644
73.50 \& \& \begin{tabular}{ll}
4572 \& 0.45 \\
4583 \& 0.90 \\
\hline
\end{tabular} \& \& NE5533P 1.50 \& U－N2804 1.90 \& \& \& \& \& \({ }^{4} 9.952 \mathrm{MHz} 2.50\) \\
\hline \({ }_{7489}\) \& 2.10 \& \(744576 \wedge 0.36\) \&  \& \({ }^{74 \text { PALS32 }} 0.45\) \&  \& LM M 307 0.0 .45 \& NEE5534P 1.20 \& UPC5923 2.00 \& 6850
68850 \& \(6264 \mathrm{P}-15750\) 6264 LP － 154.0 O 0 \& \& \& \({ }_{\text {a }}^{5.00 \mathrm{MHz}} \mathbf{1} \mathbf{1 . 5 0}\) \\
\hline 7491
7 \& 0．70 \& 744578
\(74 . S 83 A\)
0.42
0.70 \& \({ }^{744566688909090}\) \& （eatsis 1.50 \& \(4724 \quad 1.50\) \&  \& OP－07EP 3.50 \& UPCC1156H
UPC1185
3．000 \& \& \& \& \& O0MHz 1．40 \\
\hline 74923 \& 0.70 \& \({ }^{74 L \text { LS85 }} 00.75\) \& 74 S5670 1.70 \&  \& \(\begin{array}{ll}14411 \\ 14412 \& 7.50 \\ \& 7.50\end{array}\) \& LM311 0.60 \& \({ }^{\text {PLC44，}}\) \& \(\times \mathrm{R} 2104.00\) \& 688854
688.00 \& \(6810-45\)
6810 \& \begin{tabular}{ll} 
OMB131 \\
OP8304 \& 6.50 \\
\hline 1.50
\end{tabular} \& ceenervion \& \({ }^{6.144 \mathrm{MHz} 1.40} \mathrm{f}\) \\
\hline 749 \& ． 10 \& \begin{tabular}{l}
744.5866 \\
74.590 \\
\hline 0.38 \\
\hline 0.458
\end{tabular} \& \({ }_{7}^{74 L 566883} 3.500\) \&  \& 14416 \& \begin{tabular}{ll} 
LM318 \\
LM319 \& 1.80 \\
\hline 1.80
\end{tabular} \&  \& \begin{tabular}{l} 
XR2206 \\
\(\times R 22074.75\) \\
\hline 3.50 \\
\hline
\end{tabular} \& \(6875 \quad 5.00\) \& \& \(\mathrm{OS}^{\text {S3691 }}\) \& 13047.50 \& \({ }^{7} 1.160 \mathrm{Hzz} 1.75\) \\
\hline 749 \& 0.60 \& \({ }^{744591} 0\) \& \({ }^{7445684} 3.50\) \& 7 74ALS574 4.50 \& （14499 \(\begin{array}{ll}14.60 \\ 14490\end{array}\) \&  \&  \& \begin{tabular}{l} 
XR2211 \\
\hline
\end{tabular} \& \(8154 \quad 8.50\) \& \& 058831 1.50 \& \& \({ }_{8}^{8.867 \mathrm{MHz} \mathrm{I}^{1.75}}\) \\
\hline \& 2.10 \& 74L593 \& \({ }_{74}\) \& 74ALS5880 2.60 \& 14495 \& Lм3352 1.30 \& S50280

550200 \& XR2240 1.20 \& 8155
8156 $\begin{aligned} & 3.80 \\ & 3.80\end{aligned}$ \& $\begin{array}{ll}\text { 933 } \\ \text { 9322 } & 7.50\end{array}$ \& OS8833 \& \& 10．00M Az
10.50 Hzz
2.50 <br>

\hline \& \&  \& 74L5783 21.00 \& 4000 SEanes \& 14599 \& LM339 ${ }^{\text {L－436 }}$ \& | SAA 9000 |
| :--- |
| SFF96364 |
| 8.0 .00 |
| .00 | \& ZN414 \& \& \& OS8836 \& \& | 10.70 MHz |
| :--- |
| 1100 MHz | <br>

\hline 74 \& 0 \& 74LS1070．0．40 \& \& $4000 \quad 0.20$ \& $\begin{array}{ll}22900 \\ 22101 & 3.50 \\ 7.00\end{array}$ \& LM34888 0.50 \& S．4．900
SN760130
3.000 \& ZN419P \& $\begin{array}{lll}8212 & 2.00 \\ 8215\end{array}$ \& \& －77002 ${ }^{\text {P800 }}$ \& \& 12．000 Hz 1.50 <br>

\hline \& \& 74.51120 .45 \& 7as serits \& $4001{ }^{0.24}$ \& | 22102 |  |
| :--- | :--- |
| 40014 | 7.00 |
| 0.48 |  |
| 0 |  | \& LM377 3.00 \& SN76023 \& 2Na24E 1．30 \& ${ }_{8}^{822}$ \& qoms \& MC1488 \& \& | 14.00 MHz |
| :--- |
| 14.31 MHz |
| 1.60 |
| 1.75 |
| 1 | <br>

\hline \& \& 744S113 0.45 \& \& 002 0.25 \& $40085 \quad 1.20$ \& ［m380 \& SN76033 3．00 \&  \& $8226 \quad 4.25$ \& \& MC3446 2.50 \& \& 14.756 MHz 2.50 <br>
\hline 74 \& 1.70 \& 744512200.70 \& 74500 \& 40070 \& $\begin{array}{ll}40097 \\ 40098 \\ & 0.36 \\ 0.40\end{array}$ \& LM381AN1．70 \& SN76489 4．00 \& ZNa27e86．00 \& ${ }_{82288}^{8228}$

8243 \& \begin{tabular}{ll}
24510 <br>
2.50 <br>
185030 <br>
2.00 <br>
\hline 200

 \& MC3459 4.50 \& \& 

15.000 MHz <br>
16.00 MHz <br>
2.00 <br>
2.00 <br>
\hline 100
\end{tabular} <br>

\hline ${ }_{74}$ \& 0.55 \& ${ }^{7} 744 \mathrm{SL123} 20.8080$ \& ${ }_{74504}^{74502}$ \& 4008
4009 \&  \& LM384 ${ }^{\text {L }}$ \& SN764954．00 \&  \& \&  \& MC34808．50 \& \&  <br>
\hline 74 \& ${ }_{0}^{0.8}$ \& ${ }^{744 \text { LS } 126} 00.50$ \& $\begin{array}{ll}74405 \\ 74508 & 0.50 \\ 0.50\end{array}$ \& 4010

4011 \& \begin{tabular}{ll}
401002 \& 1.35 <br>
\hline

 \&  \& 

SPO256AL 7.00 <br>
SP8515 <br>
\hline 7.50
\end{tabular} \& ZN447E 9 9．00 \& \&  \& MC3487 2.25 \& \& ${ }_{18} 18.303 \mathrm{MHHz}$ <br>

\hline \& 0.65 \& \& 745100.50 \& $4012 \quad 0.25$ \& ${ }^{40103}{ }^{2} 10300$ \& LM389 1.818 \& TA7120 1.20 \& ZNA50E 7.50 \& ${ }_{8}^{8253 C-5}{ }^{8}$ \& \& MC4024 5.50 \& \& 19．9694Hz 1.50 <br>

\hline 74126 \& \&  \& 74811 \& ${ }^{0.36}$ \& 40105 \& LM391 \& | IA7130 |
| :--- |
| 1.40 |
| 150 | \& ZNa59CP 3.00 \& 8256 18．00 \& $\begin{array}{ll}{ }_{82 S 23} & 1.50\end{array}$ \& MC14411 9.00 \& 00 \& 24.00014 Hz 175 <br>


\hline 74132 \& 0.75 \& 74LS139 0.55 \& 745220.50 \& $4015 \quad 0.70$ \& ${ }^{40106}$ \& LM 3930.85 \& IA7205 0.90 \& Zna 10406.60 \& \& | 82S123 |
| :--- | :--- |
| 8825129 |
| 8.75 | \& 751070.90 \& SAA5041 16.00 \& $11.6 \mathrm{WHz} \mathrm{F}^{2.5}$ <br>

\hline ${ }_{7}^{74136}$ \& 0.70
0.90
0.90 \& 744S1445 0.95 \& ${ }_{7}^{744530}$ \& $\begin{array}{ll}4016 & 0.36 \\ 4017 & 0.55 \\ 0.55\end{array}$ \& 40108
4080 \& LM LM 709 CHe 0.35 \& $\begin{array}{ll}\text { TA7222 } \\ \text { TA7310 } & 1.50 \\ 1.50\end{array}$ \&  \& ${ }^{825}$ \& \& $75108 \quad 0.90$ \& SAA50509．00 \& PXO1000 12.00 <br>

\hline 74142 \& 2.50 \& 74LS 1481.40 \& 7453780.60 \& 4018 0．60 \& | 40109 | 0.80 |
| :--- | :--- |
| 40110 | 85 |
| 2.05 |  | \& \& \& \& \& \& $75110 \quad 0.90$ \& \& <br>

\hline 741

741 \& 2.70 \& 7445151520.60 \& \begin{tabular}{ll}
<br>
744538 <br>
74540 \& 0.60 <br>
\hline 750

 \& $\begin{array}{ll}4019 & 0.60 \\ 4020 & 0.80\end{array}$ \& 40114 \& \& \& \&  \& EPR \& 

75112 <br>
75113 \& 1.60 <br>
1.20 <br>
\hline
\end{tabular} \& \& 左 <br>

\hline 74145
74147 \& 1.10

1.70 \& 7441533 0.65 \& $\begin{array}{ll}74551 \\ 74564 & 0.60 \\ 0.45\end{array}$ \& ${ }^{0.60}$ \& $\begin{array}{ll}414147 \\ 40163 & 1.80 \\ 1.00\end{array}$ \& A \& ED vo \& TIC TO220 \& \& \& | 7514 |
| :--- | :--- |
| 75115 |
| 1.40 | \& 11 prices \& subject to <br>

\hline 74 \& ${ }^{1.70} 1.75$ \& ${ }^{744 \text { LS } 155} 00.655$ \& ${ }_{7}^{74574}$ \& $\begin{array}{ll}4023 & 0.30 \\ 4024 & 0.48 \\ 40\end{array}$ \& ［40173 | 40.20 |  |
| :--- | :--- |
| 40174 | 1.00 | \& ${ }^{+} \mathrm{VE}$ \& \& VE \& \&  \& 75121 1.40 \& ge \& ut notic <br>


\hline 74151 A \& 0.70 \& 74LS $1577^{0.50}$ \& 745861.00 \& $\begin{array}{ll}4025 & 0.24 \\ & 0.2026\end{array}$ \& | 40175 |
| :--- |
| 4090 |
| 1.00 | \& $6 \mathrm{6V} 7806$ \& 0 \& 0．50 \&  \& （16x16） 4.50 \& $\begin{array}{ll}75122 \\ 75150 & 1.40 \\ 1.20\end{array}$ \& Only curr \& ime grade <br>

\hline \& 0.80 \& 74.51580 .65 \& 748112 \& 0.90 \& ${ }_{40193}{ }^{401929}$ \& 6V7808 \& 5 \& 0．50 \& OTHERs \& \& \& \& <br>
\hline \& 0.80 \& 74．5．61／A 0.75 \& 7451141.20 \& 4028 0．60 \& $4{ }^{40194}$ \& 15 V 78150.5 \& 50 \& \& \& \& \& \& <br>
\hline ${ }_{74} 7$ \& 0．80 \& ${ }^{74455162 A} 0.753{ }^{0.75}$ \& $\begin{array}{lll}745124 & 1.00 \\ 745132 & 1.00\end{array}$ \& 4029
4030 \& $40245 \quad 1.50$ \& 18V 248784.5 \& $50 \quad 7924$ \& \& $\begin{array}{ll}\text { 2NST77 } & 0.50 \\ \text { BPX25 }\end{array}$ \& 0．125＂ \& 0.2 \& We also \& ck a wide <br>

\hline \& ${ }_{1}^{175}$ \& 744．5164 ${ }^{\text {7 }}$ \& | 744133 | 0.60 |
| :--- | :--- |
| 745138 |  |
| 1.80 |  | \& $\begin{array}{ll}4031 \\ 4032 & 1.25 \\ 100\end{array}$ \& | 40257 |
| :--- | :--- |
| 40373 |
| 1.80 |
| 1.80 |
| 180 | \& ${ }^{1 A} \mathrm{FIX}$ \& EED VOLTAGE PL \& STIC 1092 \& \& RED TLR290．12

GRN TLL211 0.16 \& | Ti1220 |  |
| :--- | :--- |
| T1222 | 0.15 |
| 0.18 |  | \&  \& of： <br>

\hline 74161 \& 0.80 \& ${ }^{74151566 A} 1.50$ \& ${ }_{745139} 1.80$ \& | 4033 | 1.25 |
| :--- | :--- |
| 403 |  | \& | 40374 | 1.80 |
| :--- | :--- |
| 80050 |  | \& 5 SV 788060 \& \& 91120.50 \& ORP12 1.20 \& Fil \& TiL226 0.22 \& Trans \& stors， <br>

\hline 74162
74.63 \& ${ }_{1,10}^{1.10}$ \&  \& 745140
745151

71.00 \& | 4034 |
| :--- | :--- |
| 4035 |
| 40.50 |
| 0.70 | \& 0.75 \& 8V 78L08 \& \& 150．50 \& $\begin{array}{ll}\text { ORP60 } & 1.20 \\ \text { ORP61 } & 1.20\end{array}$ \& （R／G／Y） 0.30 \& courtens \& es \& cs Plastic， <br>

\hline 74164
74165 \& ${ }_{1.10}^{1.20}$ \& ${ }^{\text {744SLITO }} 1.400$ \& $\begin{array}{ll}745153 & 1.50 \\ 745157 & 2.00 \\ \\ 7\end{array}$ \& $\begin{array}{ll}4036 \\ 4037 & 2.50 \\ 40 \\ 10\end{array}$ \& \& 15V 78L15 \& \& \& SFF205 1.00 \& \& \& Bridg \& ectifiers， <br>
\hline 67 \& 1.40

4.00 \&  \& |  |  |
| :--- | :--- | :--- |
| 7445585 | 2.00 |
| 745163 | 3.00 | \& $\begin{array}{ll}40388 \\ 4040 & 1.00 \\ 40.60\end{array}$ \& \& OTHER F \& cilators \& \& T1L7888．55 \& aph \& $\begin{array}{ll}744 \mathrm{Ca26} & 6.50 \\ 74928 \\ 6.50\end{array}$ \& Thy \& ors and <br>

\hline 170 \& 2.00 \& 74iSisi 2.00 \& ${ }^{745169} 5.50$ \& 4041 \& FIXED \& ators \& \& \& TLLE\％ 1.20 \& Red \& ${ }^{72168} 822.00$ \& \& <br>
\hline 74172

743 \& \& | 7425183 |
| :--- |
| 74 S 190 |
| 0.750 | \& \& 40420.50 \& LM \& 1A 5 SV \& \& ${ }_{3.50}$ \& TL． 10000.75 \& \& \& \& one for <br>

\hline \& \&  \& $\begin{array}{ll}745188 \\ 74 S 88 & 1.80 \\ 780\end{array}$ \& | 4044 |
| :--- | :--- |
| 4045 |
| 0.60 |
| 100 | \& ${ }_{78 \mathrm{H} 12} 78 \mathrm{HCO}$ \& $5{ }_{5} 5$ A 12 V \& \& 5.40

6.40 \& \& MAN66102．00 \& Lм ${ }^{1914} 3$ \& \& <br>
\hline 74776 \& 1.00 \& ${ }^{7} 741519944040.75$ \&  \& $4046 \quad 0.60$ \& 78 P \& 1045 V \& \& 9.00 \& \& TLL311 6.50 \& Lм ${ }^{\text {LM9：6 }}$ 3．50 \& \& <br>

\hline 178 \& ${ }_{1.50}^{1.50}$ \& ${ }^{7} 7441519594060.80$ \& | 745195 |
| :--- |
| 745196 |
| 3.50 |
| 3.50 | \& | 4047 |
| :--- | :--- |
| 4048 |
| 40.00 |
| 0.55 |
| 0.50 | \& AR \& regulators \& \& \& \& T1／729 1.00 \& UON61183．20 \& \& <br>

\hline 180 \& 1.00 \& 74LS1970 0．80 \& 7442000.50 \& $4049 \quad 0.36$ \& LM317T \& то－220 \& \& 1.50 \& FNDSOO／TLT \& MANB910 1.50 \& ULN2003 0.90 \& Optors \& Lator <br>
\hline 74182 \& 1.40 \& 7415240 0．80 \& ${ }_{745225} 5.20$ \& ${ }_{4051}^{4050}{ }^{4.65}$ \& LM31 \& O3 \& \& 2．40 $\begin{array}{r}2.25 \\ 2.25\end{array}$ \& － 0507 TH｜i200 \& Man8990 \& UL 200040.90 \& $1074{ }^{1.30}$ \& ［LL111 <br>

\hline 35A \& | 1.80 |
| :--- |
| 1.80 |
| 1 | \& 744．S241

74.5824
0.90

0.90 \& $\begin{array}{ll}742420 & 4.00 \\ 745241 & 4.00\end{array}$ \& | 4052 |  |
| :--- | :--- |
| 4053 | 0.60 |
| 0.60 |  |
| 0.60 |  | \& LM35906 \& $10 A+v a 8$ \& \& 4.00 \& ${ }^{00}$ \& mispuy \& UL N2802 1.90 \& ${ }_{1}^{2.20}$ \&  <br>

\hline 74 \& 1.30 \& 74LS243 0.90 \& ${ }^{745244} 4.50$ \& $4054 \quad 0.80$ \& L－M733N \& \& \& 0．50 \& 1.00 \& \& UUN2083 1.80 \& MCS2400 1.90 \& T1． 1116 <br>

\hline 74 \& ${ }_{1}^{1.30}$ \& ${ }^{\text {744．S244 }} 0$ \& | 745251 |
| :--- | :--- |
| 745257 |
| 72.50 |
| 750 | \& $\begin{array}{ll}4055 \\ 4056 & 0.80 \\ 0.85\end{array}$ \& ${ }_{7} 78 \mathrm{BH} \mathrm{HOSKC}$ \& 5AsV \& \& $\begin{array}{r}5.75 \\ 6.50 \\ \hline\end{array}$ \& MAN3640

MAN6640
2.750 \& 9368

9370 \& 754910.70 \& MOC3020 1.50 \& | SN137 | 3.60 |
| :--- | :--- |
| SN139 | 1.75 | <br>

\hline 74193 \& 1.15 \& 744．5247 1.10 \& | 7445258 |
| :--- | :--- |
| 745250 |
| 750 | \& ${ }^{4060} 00.70$ \& ${ }_{78 G \mathrm{GIC}} 78 \mathrm{Cl}$ \& 1AtVAR \& \& 2．25 \& \& \& \& \& <br>


\hline \& 100 \& 744.584981 .10 \& | 745260 |
| :--- |
| 745261 |
| 1.00 | \& | 4063 |  |
| :--- | :--- |
| 4066 | 0.85 |
| 0.40 |  | \& ${ }_{79 \text { 79HGKC }}$ \&  \& \& （e ${ }^{6.75}$ \& LOW PROF \& FILE SOCKETS By \& \& WIFE WRAP SOC \& KETS EY Ti <br>


\hline 74197 \& | 1.30 |
| :--- |
| 1.10 | \& ${ }^{744.5251} 0.75$ \& $\begin{array}{lll}744283 \\ 745887 & 2.70 \\ 72.25\end{array}$ \& | 4067 |
| :--- | :--- |
| 4068 |
| 8.35 |
| 0.25 | \& Switching \& regulation \& \& \& \& \& \& ${ }_{\text {coin }}^{18017}$ \& <br>


\hline 74198 \& | 2.20 |
| :--- |
| 2.20 | \& | 744.525650 .90 |
| :--- |
| 74.524540 | \& $\begin{array}{lll}7442888 \\ 745289 & 2.00 \\ 72.25\end{array}$ \& | 4069 | .23 |
| :--- | :--- |
| 4070 |  |
| 40.24 |  |
| 0.24 |  | \& （Cliz660 \& \& \& 2.50

3.00 \& 14pin

16pin \& $\begin{array}{lll}20 \mathrm{pan} & 18 \mathrm{p} \\ \text { 22pin } & \\ 200\end{array}$ \& nter $\begin{aligned} & \text { nep } \\ & \text { 30p }\end{aligned}$ \&  \& $$
\begin{aligned}
& 28 \mathrm{pin} \quad 80 \mathrm{p} \\
& 40 \mathrm{pin} 100 \mathrm{p}
\end{aligned}
$$ <br>

\hline 921 \& ${ }_{1}^{2.20} 1.10$ \& ${ }^{744152525258 A}$ 0．70 0.70 \&  \& | 40070 |  |
| :--- | :--- | :--- |
| 4071 | 0.24 |
| 0.24 |  | \& TL．494 \& \& \& 3.00 \& \& \& \& \& <br>


\hline 74251 \& 100 \& | 744．5259 1.20 |
| :--- |
| $7 / 51560$ | \& 7453373

7457300 \& | 4072 | 0.24 |
| :--- | :--- | :--- |
| 4073 |  |
| 0.24 |  | \& ${ }_{78540}^{71.497}$ \& \& \& ＋3．00 \& 析 \& \& ${ }^{16 \mathrm{pom}}$ \& in \& in <br>

\hline ${ }_{74265}^{74459}$ \& ${ }^{1.50}$ \& ${ }^{744 \text { SS266 }} 00.75$ \& | 7443384 |
| :--- |
| 74538 |
| 2.00 | \& $\begin{array}{ll}4073 \\ 4075 & 0.24 \\ & 0.24\end{array}$ \& ${ }_{\text {RC4 }}$ \& \& \& 1.50 \& \& \& \& \& in 90p <br>

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## Newnes Technical Books



# Naiad training rohot 

# Robot arm interfaces with Apple, BBC, Commodore and IBM computers. Design by Peter Wells and Dick Becker 

The control electronics of Naiad are split between the three printed-circuit boards: computer interface, solenoid driver and power supply. The computer interface shown below, communicates with the host computer bus, provides the power for the d.c. motor, generates 5 V signals for the solenoid driver board, and processes signals for return to the computer. There are also a number of inputs and outputs for interfacing to additional equipment such as sensors,
conveyor belt, indexing table and so on.
The robot works with parallel data from the computer and the fastest way of interchanging data is by connecting straight onto the bus of the computer. Computer manufacturers provide a variety of means of gaining access to the bus and there are two edge connectors on the interface board. The first connector is specifically for the BBC computer and the second one for other machines. Leads terminated with suitable plug-in
cards for the Commodore 64, Apple IIe and IBM computers are available. Connection is made to the 1 MHz bus connector, expansion port (rom games socket) and expansion slots respectively.

The signals required for the computer interface are: eight data lines, the five leastsignificant address lines, the read/write signal, a block decode of a minimum of 32 addresses, and the clock. For
continues on page 20
by R.H.Becker




the IBM the generation of a block decode and the combination of signals i/o write and i/o read to read/write takes place on the IBM plug-in card. Although only four computer types have been mentioned, almost any computer or microprocessor system will control the Naiad providing there is access to the bus and a 20 -way cable is made.

Operation of the interface, pp: $18 \& 19$, follows. Circuits $\mathrm{IC}_{1}$ and $\mathrm{IC}_{2}$ gate together $\mathrm{A}_{4}$, the clock, read/write and a linkselectable choice of block decodes (Jim and Fred) to generate valid write and valid read signals defining the conditions that data is being sent to the robot, and is required from it, respectively. Circuits $\mathrm{IC}_{3}$ and $\mathrm{IC}_{4}$ act similarly for computers other than the BBC. Only one computer can be connected at any one time and a slide switch shown, positioned between the edge connectors, selecting which interface is operative, and this is shown by led indicators $\mathrm{D}_{1}$ and $\mathrm{D}_{2}$. The switch selects directly the clock and indirectly, by data selector $\mathrm{IC}_{5}$, the valid write and valid reads signals.
To avoid loading heavily the bus of the host computer the data bus is buffered by $\mathrm{IC}_{12}$ which is a transceiver meaning
that it will work in either direction. This is necessary as data needs to be received back from the robot as well as sent and there is a direction signal on pin 1. Normally this signal is low and the computer data is passed to the data bus of the robot, but when the analogue to digital converter signals are read, the direction signal goes high and data on the bus of the robot is transferred to the bus on the computer.
The lowest four address lines are also buffered with half of $\mathrm{IC}_{10}$ and the addresses decoded by $\mathrm{IC}_{9}$ and $\mathrm{IC}_{11} \cdot \mathrm{IC}_{9}$ decodes the addresses to give the signals 'output-enable learn' and 'output-enable feedback' for the two a-to-d converters and 'end-of-conversion test' which is used for checking that the converters are ready to be read. $\mathrm{IC}_{11}$ decodes the addresses to give a write-clocks signal for the three data latches $\mathrm{IC}_{13}, \mathrm{IC}_{15}$ and $\mathrm{IC}_{16}$ and to give the signals 'address, latch enable' and 'output enable' for the converters. The unused outputs of the decoders function as external outputs for operating peripheral equipment.
Data latch $\mathrm{IC}_{13}$ is the one written to, for defining the next position of axis 3, the d.c. motordriven wrist elevation. The data, which is held on the latch until written to again, is
transferred to the digital-toanalogue converter $\mathrm{IC}_{11}$. The output of the d-to-a converter is buffered by $\mathrm{IC}_{60 \mathrm{GIT}}$ providing a 0 to +5 V signal. Being an eightbit system there are $2^{8}$ i.e. 256 possible levels, therefore for each bit data change there is an output change of 20 mV .
The reference voltage for the d-to-a converter is +10 V and is derived from the +5 V rail by $\mathrm{IC}_{6 \mathrm{a}}$. With +5 V on pin 3 , the output settles at the voltage which also gives +5 V on pin 2 . As $R_{46}$ and $R_{47}$ are equal the output is twice the , input. $\mathrm{IC}_{6 \mathrm{~b}}$ inverts the +10 V to provide a -10 V rail. As the -10 V rail is used for powering the various potentiometers used for position sensing of the robot and the simulator, the current output capability of the operational amplifier is boosted by $\mathrm{Tr}_{2}$.
Axis 3 feedback (position sensing) potentiometer output is buffered by $\mathrm{IC}_{18 \mathrm{~b}}$. The potentiometer nulls out the offset voltage which is the voltage on the potentiometer at the zero (lowest) position. The gain of the stage is less than unity to give an output range of 0 to +5 V for the $250^{\circ}$ of movement of the axis. The circuit has around it two diodes and a transistor to limit the output to no more than 5 V , which is the maximum
permitted on the input of the a-to-d converter.
The feedback signal from $\mathrm{IC}_{18 \mathrm{~b}}$ is compared with the dac output by $\mathrm{IC}_{18 \mathrm{a}}$ to give an error signal in the range of -5 to +5 V and this then passes through $\mathrm{IC}_{19 \mathrm{~b}}$ which is a variable gain transconductance amplifier. The current out from pin 12 is proportional to the voltage across its input pins 13, 14 and the gain is proportional to the current entering pin 16.
The gain controlling current comes from voltage-to-current converter $\mathrm{IC}_{19_{a}}$, the voltage to which comes from a discretecomponent d-to-a converter comprising $\mathrm{R}_{7}$ to $\mathrm{R}_{21}$ and $\mathrm{IC}_{607 \mathrm{~b}}$. Seven out the outputs of data latch $\mathrm{IC}_{16}$ feed an $\mathrm{R} / 2 \mathrm{R}$ ladder network giving an output in the range of 0 to 2.5 V which is buffered by $\mathrm{IC}_{607 \mathrm{~b}}$. This type of converter is not as accurate as $\mathrm{IC}_{14}$ but although a couple of percent difference in position is very important, this amount of change in the gain of the system is hardly noticeable. Sources of error in the discrete component version are the resistors themselves, which are $1 \%$ tolerance, and the differing impedances of t.t.l. outputs in the high and low states. TT logic is intended to sink current rather than supply it and the output impedance is about 200
ohms higher in the high state.
The error signal from $\mathrm{IC}_{19 \mathrm{p}}$ is finally amplified to a level suitable for driving the motor by power operational amplifier $\mathrm{IC}_{20}$. The potentiometer nulls out the input offset so that zero error signal gives zero output. As motors do not start to move until 2 to 3 V is applied to them, the gain of the stage is boosted (by blocking the feedback path with zener diodes $D_{5}$ and $D_{6}$ ) so that almost any error will cause an output sufficient to just turn the motor. Once 3 V output is reached, the diodes conduct and the gain of the stage drops to that set by the ratio of $\mathrm{R}_{37}$ to $\mathrm{R}_{36}$. Diodes $D_{7}$ and $D_{y}$ indicate the direction of drive to the motor.
Controlling the solenoids is rather simpler than the motor as the aim is simply for the computer to turn them on or off and the eight outputs of data latch $\mathrm{IC}_{1.5}$ together with one of the outputs of $\mathrm{IC}_{16}$ set the states of the nine solenoids. To prevent a programming error from simultaneously turning on both valves of an axis, thereby causing a hydraulic short circuit, gates 601 to 604 are used to disallow this condition.
The solenoids are 24 V types meaning that 24 V should be
applied to turn them on. However once turned on, they will stay on until the voltage drops below about 8 V . A continuous 24 V is therefore a waste of energy which causes unnecessary heating inside the robot base and the solenoid driver board is used to supply more appropriate voltages to the solenoids. The board takes the 5 V control signals from the interface board and briefly applies over 30 V to the appropriate solenoid turning it on very rapidly. This surge is then followed by a steady 17 V to give a holding current which causes only $50 \%$ of the heat resulting from the use of a steady 24 V

The solenoid drive circuitry, (page 20) is repeated for the nine valves. Taking solenoid $S_{0}$ : when the input signal is at 0 V , which represents the off condition, $\operatorname{Tr}_{1013}$ is off and its collector high turning on $\mathrm{Tr}_{10}$. The voltage across $\mathrm{D}_{104}$ and $\mathrm{R}_{109}$ is insufficient to turn on $D_{101}$ hence $\mathrm{Tr}_{102}$ is off. $\mathrm{C}_{101}$ charges almost to supply voltage, from current flowing along the path $D_{104}-C_{101}-R_{103}-\operatorname{Tr}_{101}$. When the input signal switches to $+5 \mathrm{~V}, \mathrm{D}_{145}$ glows indicating this condition and $\operatorname{Tr}_{103}$
saturates, turning off $\mathrm{Tr}_{101}$ and also turning on $\operatorname{Tr}_{102}$. This places the charged capacitor across $D_{104}$. The voltage on the solenoid is now equal to the supply rail plus the charge on the capacitor (less the small drops across $D_{10.4}$ and $\operatorname{Tr}_{103}$ ). The solenoid has a resistance of about 100 ohms so the time constant of the capacitor discharge is 22 ms which is more than adequate for turning on the valve which normally has a turnon time of about 5 ms .

To enable the computer to read the positions of the axes of the robot and of the simulator there are two a-to-d converters. $\mathrm{IC}_{7}$ reads the feedback from the robot whilst $\mathrm{IC}_{8}$ is for the learn axes of the simulator. Spare inputs are used as external inputs from any peripheral equipment. The ADC0809 is an 8 bit, 8 channel multiplexed converter.
First the converters are written to, to define the axis to be read. Buffered data lines 0,1 , 2 are used to define the learn axis and data lines $4,5,6$ to define the feedback axis. Next they are written to again to start the conversions, which occur simultaneously on the two converters. The data sent in this
write operation is irrelevant but in the examples given later, zero is always used. Finally a read operation takes data from one of the converters. Conversion takes about $100 \mu \mathrm{~s}$ so if in doubt as to whether sufficient time has elapsed for the conversion (little doubt when using Basic!) the state can be checked by reading the end-of-conversion signals.
Although there is no mention of it in the data book, a-to-d converters can catch out the unwary with a phenomenom known as s.c.r. breakdown. If this occurs heavy current is drawn leading to overheating and eventual destruction. This can be triggered by voltage spikes on the bus or overvoltage on the inputs. To avoid any chance of breakdown, the converters are connected to the buffered bus of the robot rather than straight onto the computer bus. There are also resistor network on the converter inputs and voltage limiters on the amplifiers feeding them.
Each signal from the potentiometers passes through a buffer ( $\mathrm{IC}_{101}$, up to $\mathrm{IC}_{5044}$ ). similar to that of axis 3 , providing offset adjustment and limiting for the converter.
The power supply, below

provides regulated supply rails of $+5 \mathrm{~V},+15 \mathrm{~V},-15 \mathrm{~V}$ for the computer interface board, +18 V unregulated for the solenoid driver board and 240 V for the pump.
The Naiad is memory mapped (i/o mapped when used on the IBM) meaning that the computer treats the robot as if it were part of its memory (i/o space on the IBM) and can be written to or read from. Table 1 gives the addresses used by the robot. Operation is most simply shown by examples and for these, BBC Basic will be used. In BBC Basic both poke and peek are represented by?.


To:
define address of start of block decode JIM
rotate axis 0 clockwise turn on solenoid $\mathrm{S}_{0}$ ) set all bits low except $D_{0}$
rotate axis 0 anticlockwise turn on solenoid $S_{1}$ ) set
all bits low except $D_{1}$
raise axis 2 (turn on solenoid $S_{4}$ ) set all bits low except $\mathrm{D}_{4}$
raise axis 2 and rotate axis 0 clockwise set all bits low except $D_{0}, D_{4}$
close the gripper set $D_{0}$ of next latch high ( $G$ is an even integer defining the gain of axis 3 amplifier)
open gripper again
send axis 3 to lowest position
send axis 3 to centre position
set amplifier gain to $1 / 2$ of maximum
read axis 0 feedback(set data lines low on multiplexer)
read axis 3 feedback (set $D_{4}, D_{5}$ high on multiplexer)
read axis 3 learn (set $D_{0}, D_{1}$ high on multiplexer)
read analogue input EXIP5
enable external device on EXOP1 read end-of-conversion feedback
read external digital input EXIP1

You can see that very simple statements will operate the axes of the Naiad together with external devices. Data back from the robot and external devices is also easily obtained by the host computer, and programs performing servoing and interacting with peripheral devices are readily accomplished. A large amount of software has already been written for the Naiad and will be supplied with it. Even more is being written and peripheral equipment is under development. The first devices to be available will be an indexing
$A=\& F D 00$
$?(A+1)=1$
$?(A+1)=2$
$?(A+1)=16$
$?(A+1)=17$
$?(A+2)=G+1$
$?(\mathrm{~A}+2)=\mathrm{G}$
? $A=0$
? $\mathrm{A}=128$
$?(A+2)=128$
? $(A+6)=0$
? $\mathrm{A}+7)=0$
$\mathrm{F} 0=$ ? $(\mathrm{A}+17)$
$?(A+6)=48$
$?(A+7)=0$
$\mathrm{F} 3=$ ? $(\mathrm{A}+17)$
$?(A+6)=3$
$?(\mathrm{~A}+7)=0$
$\mathrm{L} 3=$ ? $(\mathrm{A}+16)$
$?(A+6)=7$
$?(A+7)=0$
EXIP5 $=$ ? $(A+16)$
? $(A+3)=0$
EOCF =? ( $\mathrm{A}+18$ ) AND 1
$B=?(A+18): E X-$ $1 \mathrm{P} 1=$ (B AND 8)DIV8
table, a conveyor system using a stepper motor for position incrementing and a range of sensors.

The Naiad is manufactured by Cybernetic Applications, West Portway Industrial Estte, Andover, Hants SP10 3WW, Tel 0264 50093, and is available either ready-built or as a selfassembly kit.


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## Antennas - more width

The bandwidth of many current receiving antennas for u.h.f. television and v.h.f. radio is barely adequate and can produce problems. The performance towards the limits of the various "groups" tends to fall off, particularly at the high-frequency end, for example, when rainwater collects on the elements. For Band 2 radio, many of the multi-element beams in use to improve stereo reception were designed with an upper limit of 100 MHz and are becoming far less efficient as the band extends up to 108 MHz . The problem also occurs on some of the older transmitting antennas which, for local radio, were designed for use below 100 MHz and are now having to be changed to accommodate the new Geneva Plan 1984 frequencies.

However, the design of antennas having broader bandwidth is making progress. At the 1985 International Conference on Antennas and Propagation (ICAP85) several papers were published on wideband u.h.f. antennas suitable for television applications. A Polish paper by R.J. Katulski of Gdansk University, Poland, analysed the log. pyramidal periodic (l.p.p.) antenna which comprises two log.-periodic structures mounted in diverging planes. His design was claimed as suitable for television reception throughout the range 150 to $900 \mathrm{MH} z$ with more gain than a comparable log.-periodic array.

A BBC paper on antennas for outside broadcast links included log.-periodic arrays, parabolic dish reflectors with log.-periodic feeds and a conical logarithmic-spiral antenna that forms a "rove" antenna with circular polarization for mobile links, with all three types suitable for use from 580 to 950 MHz Conical logarithmic-spiral antennas are also attracting increasing interest for communications applications.
Jimmy Wong and Howard King of the Aerospace Corporation have show (IEEE
Trans on Ant. \& Prop., Vol
AP-33, No 8, August 1985)
that by using an "open-sleeve" dipole as the feed element, the bandwidth of a Kraus corner reflector antenna can effectively cover 240 to 400 MHz , a bandwidth ratio of 1:1.7. Incidentally earlier work by King and Wong was used by James Miller in the design of his helical antennas for 435 MHz ( $E \& W W$, June 1985, pp. 43-6).
A new end-fire radiator antenna, the corrugated surface plane (c.s.p.) system, has been reported by C.A. King and D.A. Downs, based on work carried out at the US Naval Research Laboratory, Washington DC (Electronics Letters. Vol 21, No 24, 21 November 1985).
They note that many applications require the use of narrow-beam endfire radiators. A popular microwave approach is the polyrod antenna comprising a dielectric rod fed by a short section of waveguide. However, at u.h.f. such antennas become heavy and cumbersome due to the weight of the dielectric. They have evolved an antenna consisting of a pair of corrugated surfaces mounted back-to-back with a dipole feed element perpendicular to the surface with its mid-point in the plane of the surfaces. Each of the 21 -inch corrugated surfaces has 42 slots, $1.5-\mathrm{in}$ wide and $1.5-\mathrm{in}$ deep. The antenna weighs 151 b compared to an estimated 601b for a comparable polyrod.
Measurements at 500, 750 and 1000 MHz show half-power beamwidths of $50^{\circ}, 31^{\circ}$ and $25^{\circ}$ respectively. Sidelobe levels are 20 dB down. considered low in comparison with previously-reported surface-wave antennas.

## Philips embrace MAC

There was a piquant flavour to the 1985 Shoenberg memorial Lecture of the Royal Television Society. Given by C.J. van der Klugt, vicepresident of Philips, it argued very strongly in favour of "evolutionary MAC" and - at least for the 75 per cent of the world with 50 Hz mains supplies and 50-field television systems - strongly against
acceptance of "revolutionary" 1125 -line, 60 Hz , h.d.tv systems.

His almost wickedly provocative attack on the widely-promoted NHK/Sony production standard was presented under the urbane chairmanship of recently retired Stuart Sansom who. only a few weeks before, had been arguing equally strongly in favour of the NHK production standard as one of the founder-members of Sony Broadcast.

Mr van der Klugt confirmed that Philips expect to begin marketing first-generation MAC receivers in 1987, though he did not elaborate on whether these would be suitable for D2-MAC or CMAC or both.

The 60 Hz proposals, formulated by Japan with support from the USA and Canada, attracted much opposition at the recent CCIR meeting. It failed to achieve the clesired status of a draft recommendation, and remains simply a proposal. With so much opposition from 50 Hz countries, it would appear to have little chance of being formally approved as definite recommendation at the pleanary assembly of the CCIR next May. It could be, of course, possible for countries to go ahead without CCIR endorsement.

In his lecture, Mr van der Klugt said: "Philips anticipates a technical solution, concerning the $50 / 60 \mathrm{~Hz}$ impasse. If we achieve what we now believe is possible, an umbrella standard for studio production for conversion to both 50 Hz and 60 Hz , one of the stumbling blocks will be removed. It would seem obvious that major modifications to the Japanese h.d.tv system will be required before it can adequately meet the test of providing the best service for the most people. " We have an important not-to-be-missed opportunity to create an orderly videocompatible world . . . but if fear of no decision drives us to making a decision that puts more than half the world at a disadvantage, then we have failed to use the opportunity now available to good advantage.'

To obtain agreement on world standards he believes it
essential for people to get together before taking up a firm stand and quotes as a valuable precedent the successful adoption of the Compact Disc standard following early discussions between Philips and Sony.

## Early radio

Dr Geoffrey Phillips resolutely tackled the near-impossible in attempting to cover "the history of sound broadcasting' from Faraday in 1831 to current re-engineering by the BBC of the v.h.f. network for circular polarization, all in the course of a single IEE lecture. nevertheless he succeeded in spotlighting, if only briefly, surprisingly large number of the landmarks in radio broadcasting.

He noted the early work in Belgium in 1914, interrupted by the Great War and then succeeded by the famous Hague Concerts of 1919 to about 1922 to which UK listeners were invited to subscribe and which were also sponsored for a year by the Daily Mail. The Melba broadcast from Chelmsford in 1920 was followed by the procrastinations of the British government, finally resolved by the building of 2 LO London, 2ZY Manchester, 5IT
Birmingham, the long-wave transmitter at Daventry (5XX) in the era of the British Broadcasting company (19221926), and the old Savoy Hill studios in the IEE building in which he was speaking, with their "meat safe"
microphones. Steel tape recording was a feature of the 'thirties, first with the Blattnerphone and later the Marconi-Stille machines.

He acknowledged the early "Empire" broadcasts in 1927 and 1928 by Gerald Marcuse on 31 metres with 1.5 kW , followed by the BBC from G5SW at Chelmsford and finally the official start of BBC external services in 1932.

The progression from crystal sets to valve sets with their "reaction" whistles to upset the neighbours gave Dr Phillips the opportunity to stress the advantages for medium-wave reception of the old-fashioned "frame" and modern "ferrite-rod" aerials
that can help to reject interference, including local electrical interference. He also highlighted the anti-fading properties of the two-section 725 -ft mast radiator on which the old "Third Programme" used to go out from Droitwich.
He admitted that the UK had been slow to adopt v.h.f. radio. The classic paper by Howard Armstrong had been published in 1936 but it was not until 1954 that the service began from Wrotham, although this followed exhaustive tests not only of f.m./a.m. but also a.m.l. in which a very broad receiver response permitted the use of very effective noise limiters on pulses that had not been sharpened by a narrow i.f. This system, he considered, came very close to f.m. in performance.

## PCGG

The mention by Dr Phillips of the Hague Concerts deserves to be elaborated upon. These were organized by 35 -year-old Hanso Steringa Idzerda after he obtained a licence to transmit music and voice on PCGG in The Hague. His first transmission was on November 6, 1919 after the programme of his "Radio Soiree-Musicale" had been advertised the day before in a Dutch newspaper, and the station remained in service until October, 1924. It preceded KDKA in 1920. Wireless World drew attention to these broadcasts in June 1920 and special concerts for

## Simplified circuit of the

 PCGG transmitter. The carbon microphone in series with coil L2 effects frequency modulation


The original PCGG transmitter as it was displayed in the Nederlands Postmuseum at The Hague, Netherlands. Not visible are the huge aerial loading coil and the rotary machines used for powering the transmitter. PCGG operated on a wavelength of 670 meters.

English listeners were introduced.
In 1917 Idzerda, as manager of Nederlandse RadioIndustrie, had persuaded Philips to begin manufacturing radio valves which they agreed to do if he would agree to buy at least 180 valves per year. So began, early 1918, production of Philips-Ideezet "soft" valves. In the first year he sold 1200 of them. His broadcasts were intended to promote the sale of his receivers. Later it is believed he quarrelled with Philips, though he had initiated their entry into valve manufacture.
The Dutch claim PCGG as the world's first broadcast transmitter, though this tends to be disputed by the Belgians, and there was also Prof. Fessenden's Christmas Eve "broadcast" in 1906.
PCGG actually employed a form of narrowband frequency modulation on 670 metres, being received best with the receiver slightly detuned.
In 1940 the original transmitter was donated to the Dutch Postmuseum where for many years it was regularly demonstrated on dummy load and is still located.
Hanso Idzerda, unhappily, was arrested by the Germans on 3 November 1944, found in possession of radio equipment, (and may have been involved in the clandestine Dutch radio service) and shot without trial at Wassenar.
My thanks to Dick Rollema, PAOSE, for much of this information.

## CH radar

Adding to the excellent series of papers presented last year at the three-day IEE seminar to mark the 50th anniversary of British radar, readers may wish to note several special articles in The GEC Journal of Research (Vol 3, No 2, 1985). These include a detailed account by B.T. Neale "CH the first operational radar" providing technical and operational details of the 25 MHz Chain Home with its transmitters built by Metropolitan-Vickers and receivers by A.C. Cossor Ltd to TRE specification.
W.E. Willshaw describes the evolution of the microwave magnetrons to which Eric Megaw of the GEC Research laboratories and Gutton of SFR, Paris contributed significantly. The account by Willshaw is one of the most detailed accounts of this major UK development by Boot and Randall.

## Amateur Radio

## Awards

RSGB awards this year did reflect some genuine experimental work. Roy Jones, G3NKL received the Mullard Award for some careful observations of 10 GHz signals
over obstructed paths in which he found interesting signal enhancements just after sunset and just before dawn.
Ray Cracknell, G2AHU (former ZE2JV) received the Wortley Talbot trophy and an ARRL award for technical excellence. As one of the pioneers whose detailed observations led to a better understanding of transequatorial propagation, since his return to the UK he has continued his studies of 50 MHz propagation. It may be recalled that he had the greatest difficulty in persuading the Radio Regulatory Department to renew his British licence without having to retake the examinations!
There appears to be a good chance that the new 50.0 to 50.5 MHz band will be released on a 24 -hour basis to UK amateurs about February 1986. It is clear, however, that DTI are undertaking a major revision of the terms of the amateur licence.
A Raynet Trophy was presented to Staffordshire amateurs who had helped organize emergency communications with Mexico after the recent earthquake.

## In brief

Arthur Watts, G6UN, who died recently aged 91 was a World War I member of the Royal Navy Intelligence Department and, as president of the RSGB in 1939, was responsible for the recruitment of several hundred pre-war radio amateurs as Voluntary Interceptors of the Radio Security Service (MI5) working under Lord Sandhurst

During June 1985 a new world record for a tropospheric contact on 430 MHz was established between KH6HME, Hawaii and a station near San Francisco. On 1296 MHz KH6HME worked N6CA in Los Angeles. Both distances exceed 4000 km over the Pacific path that appears to support v.h.f. and u.h.f. signals at intervals of several years. . The ARRL has proposed a band plan for 24 MHz as follows: 24.89 to 24.92 MHz c.w. only. 24.92 to 24.93 c.w./digital. 24.93 to 24.99 MHz s.s.b./s.s.tv.

# Data conversion 

# This supplement to January's data conversion feature contains the first part of a comprehensive list of d-to-a and a-to-d converter i.cs and modules. 

Digital-to-analogue converters are given in the first part of the table and analogue-to-digital devices in the second. There's news of a new molybdenum i.c. process on page 29 and an example of converter grounding on page 32 .
An extra column is included in the a-to-d converter section to
show the conversion method used. With the aid of last month's glossary, the abbreviations used should be clear.
Speed is given as seconds for conversion. With most of the devices, we have given typical parameters. Where the typical value is unclear we have given a worst-case figure.

| Manufacturer | Device | Bits | Speed | Interface | Tech. | Features |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| AMD | DAC08 | 8 | 85 n | Par. | Bip. | Mult., 0.1\% linearity, differential I o/p |
|  | Aml408 | 8 | $250 n$ | Par. | Bip. | Mult., $0.2 \%$ linearity, $157 \mathrm{~mW}, \mathrm{I} \mathrm{o} / \mathrm{p}$ |
|  | Am 1508 | 8 | 250n | Par. | Bip. | Mult., $0.2 \%$ linearity, 157 mW I o/p |
|  | Am6012 | 12 | $250 n$ | Par. | Bip. | Mult., 4 mA diff. $\mathrm{o} / \mathrm{p}, 230 \mathrm{~mW}$ |
|  | Am6022 | 12 | 75 n | Par. | Bip. | Mult., 4 mA diff. $0 / \mathrm{p}, 500 \mathrm{~mW}$ |
|  | Am6070 | 12 | 300 n | Par. | Bip. | Companding for control systems, 72dB |
|  | Am6080 | 8 | 160 n | Proc. | Bip. | Mult., $0.1 \%$ linearity, $5 \mathrm{pmm} /{ }^{\circ} \mathrm{C}, \mathrm{I} \mathrm{o} / \mathrm{p}$ |
|  | Am6081 | 8 | $200 n$ | Proc. | Bip. | Mult., $0.1 \%$ lin., range mpx, diff. I $0 / p$ |
| Analog Devices | AD390 | $4 \times 12$ | $8 \mu$ | Proc. | Hyb. | Quad, $\pm 1 / 2 \mathrm{l}$.s.b. linearity |
|  | AD558 | 8 | $1 \mu$ | Proc. | Hyb. | 2 range, 5 V supply, 75 mW |
|  | AD561 | 10 | $250 n$ | Par. | Bip. | $\pm 1 / 4$ l.s.b. error |
|  | AD562 | 12 | $1.5 \mu$ | Par. | Bip. | Mult., $\pm$ /ilsls.b. error, $10 / p$ |
|  | AD563 | 12 | $1.5 \mu$ | Par. | Bip. | Mult., $\pm 1 / 4 \mathrm{l}$. s.b. error, $10 / p$, int. ref. |
|  | AD565 | 12 | 250n | Par. | Bip. | $225 \mathrm{~mW}, \mathrm{I} \alpha / \mathrm{p}$, internal reference |
|  | AD566 | 12 | 350 n | Par. | Bip. | $180 \mathrm{~mW}, \mathrm{Io} / \mathrm{p}$ |
|  | AD567 | 12 | 500 n | Proc. | Bip. | 500 ns to $\pm 1 / \mathrm{bit}, 1 \%$ loV reference |
|  | AD569 | 16 | $6 \mu$ | Proc. | $\mathrm{Bi} / \mathrm{mos}$ | Ratiom., 0.02\% linearity, V o/p, 150 mW |
|  | AD667 | 12 | $4 \mu$ | Proc. | Bip. | $4 \mu \mathrm{~s}$ to $0.01 \%, 1 \% 10 \mathrm{~V}$ ref., 300 mW |
|  | AD1408 | 8 | 250n | Par. | Bip. | Mult., $0.1 \%$ linearity, $157 \mathrm{~mW}, \mathrm{I} / \mathrm{p}$ |
|  | AD1508 | 8 | $250 n$ | Par. | Bip. | Mult., $0.1 \%$ linearity, 157 mW , I o/p |
|  | AD3860 | 12 | $5 \mu$ | Proc. | Hyb. | o/p. amp., $\pm \frac{1}{2} \mathrm{l} . \mathrm{s} . \mathrm{b}$. linearity, int. ref. |
|  | AD6012 | 12 | 250 n | Par. | Bip. | Mult., $\pm 1 / 21 . s . b$ linearity, I o/p, 230 mW |
|  | AD7110 | 6 | 150 kHz | Par. | $\mathrm{C}-\mathrm{mos}$ | Log. 0 to $-88 \mathrm{~dB}, 1.5 \mathrm{~dB}$ res., $100 \mathrm{~dB} \mathrm{~s} / \mathrm{n}$ |
|  | AD7111 | 8 | $3 \mu$ | Proc. | $\mathrm{C}-\mathrm{mos}$ | Log. 0 to $-88 \mathrm{~dB}, 0.375 \mathrm{~dB}$ res., 5 V supply |
|  | AD7115 | 9/12 | $5 \mu$ | Proc. | C -mos | Log. 0 to $-19.9 \mathrm{~dB}, 0.1 \mathrm{~dB}$ res., b.c.d. i/p |
|  | AD7118 | 6/17 | $0.4 \mu$ | Par. | $\mathrm{C}-\mathrm{mos}$ | Log. 0 to $-85 \mathrm{~dB}, 1.5 \mathrm{~dB}$ res., 5 V supply |
|  | AD7224 | 8 | $7 \mu$ | Proc. | $\mathrm{C}-\mathrm{mos}$ | $10 \mathrm{~V} / \mathrm{o} / \mathrm{p}, 2 \mathrm{i} / \mathrm{p}$ regs, + ve supply |
|  | AD7225 | $4 \times 8$ | $5 \mu$ | Proc. | C-mos | 4 sep. refs, + or $\pm$ rails, V o/p |
|  | AD7226 | $4 \times 8$ | $7 \mu$ | Proc. | $\mathrm{C}-\mathrm{mos}$ | $4 \times 8$ bit, positive supply, V o/p |
|  | AD7240 | 12 | 550n | Par. | $\mathrm{C}-\mathrm{mos}$ | $\pm 1$ l.s.b. error, 30 mW , +ve supply, $V$ o/p |
|  | AD7520 | 10 | 500 n | Par. | C-mos | Mult., 20mW, 2ppm f.s. $/{ }^{\circ} \mathrm{C}$, 5 V supp., $10 / p$ |
|  | AD7521 | 12 | 500 n | Par. | $\mathrm{C}-\mathrm{mos}$ |  |
|  | AD7522 | 10 | 500n | Ser/par. | $\mathrm{C}-\mathrm{mos}$ | Mult., positive supplies, I o/p |
|  | AD7523 | 8 | 100n | Par. | $\mathrm{C}-\mathrm{mos}$ | Mult., I o/p |
|  | AD7524 | 8 | 150 n | Proc. | $\mathrm{C}-\mathrm{mos}$ | Mult., $\pm$ 1/bl.s.b. acc., 5 V rail, 10 mW , $1 \mathrm{o} / \mathrm{p}$ |
|  | AD7525 | 12 | $1 \mu$ | Par. | $\mathrm{C}-\mathrm{mos}$ | $3 y_{1}$-digit b.c.d. i/p pot., $\pm \frac{1}{2} 1 . s . b$. lin. |
|  | AD7528 | 2x8 | $350 n$ | Proc. | $\mathrm{C}-\mathrm{mos}$ | Mult., dual latches, I o/ps matched to 1\% |
|  | AD7530 | 10 | 500n | Par. | $\mathrm{C}-\mathrm{mos}$ | Mult., I o/p, 20mW, 5 to 15 V supply |
|  | AD7531 | 12 | 500n | Par. | $\mathrm{C}-\mathrm{mos}$ | Mult., I o/p, 20mW, 5 to 15V supply |
|  | AD7533 | 10 | 600 n | Par. | $\mathrm{C}-\mathrm{mos}$ | Mult., I o/p, 5 to 15 V supply |
|  | AD7334 | 14 | $1.5 \mu$ | Proc. | $\mathrm{C}-\mathrm{mos}$ | Mult., 8bit bus, $0.5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ gain co., I o/p |
|  | AD7535 | 14 | $1.5 \mu$ | Proc. | $\mathrm{C}-\mathrm{mos}$ | Mult., o.5ppm $/{ }^{\circ} \mathrm{C}$ gain co., <20nA o/p leak. |
|  | AD7541 | 12 | 600 n | Par. | $\mathrm{C}-\mathrm{mos}$ | Mult., I o/p, $\pm 1$ l.s.b. gain error |
|  | AD7542 | 12 | $2 \mu$ | Proc. | $\mathrm{C}-\mathrm{mos}$ | Mult., 40mW, $\pm$ bit linearity, 4 bit bus |
|  | AD7543 | 12 | $2 \mu$ | Ser. | $\mathrm{C}-\mathrm{mos}$ | Mult., $40 \mathrm{~mW}, \pm$ bit linearity |
|  | AD7545 | 12 | $2 \mu$ | Proc. | $\mathrm{C}-\mathrm{mos}$ | 2ppm $/{ }^{\circ} \mathrm{C}$ gain coeff., 5V supply, 0.5 mW |
|  | AD7546 | 16 | 4-10ر | Proc. | C -mos | $\mathrm{V} 0 / \mathrm{p}, 50 \mathrm{~mW}, 16 \mathrm{bit}$ bus/latch |
|  | AD7548 | 12 | $1.5 \mu$ | Proc. | $\mathrm{C}-\mathrm{mos}$ | 8 bit bus, mult., 5ppm $/{ }^{\circ} \mathrm{C}$ gain co., + ve supp. |
|  | AD7549 | $2 \times 12$ | $1.5 \mu$ | Proc. | $\mathrm{C}-\mathrm{mos}$ | Mult., 4 bit bus, 3 l.s.b. f.s. error, $10 / p$ |
|  | AD9700 | 8 | $10 n$ | Latch | Bip. | 125 MHz samp. vid. + sync, -5V supp., int. ref. |
|  | AD9702 | $3 \times 4$ | 5 n | Par. | Bip. | RGB channels, 125 MHz samp., e.c.l./t.t.l. i/p |
|  | AD9768 | 8 | 5 n | Par. | Bip. | Vid. 100 MHz samp., $20 \mathrm{~mA} \mathrm{o} / \mathrm{p}$, int. ref. |
|  | DAC08 | 8 | 85 n | Par. | Bip. | Mult., 0.1\% linearity, I o/p |
|  | DAC71 | 16 | 5 $\mu$ | Par. | Hyb. | 0.003\% lin., $7 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ gain co., V or I o/p |
|  | DAC72 | 16 | $5 \mu$ | Par. | Hyb. | 0.003\% lin., $5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ gain co., V or I o/p |
|  | DAC80 | 12 | $2 \mu$ | Par. | Bip. | $\pm 1 / 41.8 . b$ linearity, int. ref., I or V o/p |
|  | DAC83 | 12 | $2 \mu$ | Par. | Bip. | $\pm k_{4} 1.8 . b$ linearity, int. ref., I or V o/p |
|  | DAC87 | 12 | $2 \mu$ | Par. | Bip. | $\pm$ thl.s.b. linearity, int. ref., I or V o/p |
|  | DACl00 | 10 | 375 n | Par. | Bip. | t.t.l./d.t.l. i/p, I $0 / \mathrm{p}$, int. ref. |
|  | DACll36 | 16 | $6 \mu$ | Par. |  | $\pm$ thl.s.b. linearity |


| Manufacturer | Device | Bits | Speed | Interface | Tech. | Features |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Analogic | DACl158 | 18 | $10 \mu$ | Par. | Hyb. | $\pm$ ml.s.b. linearity |
|  | DAC1146 | 18 | 64 | Par. | Hyb. | lppm $/{ }^{\circ} \mathrm{C}$, high linearity |
|  | HDD0810 | 8 | 10 n | Par. | Hyb. | Vid., $75 \Omega \mathrm{o}$ p, sync $i / p$, int. ref. |
|  | HDD1015 | 10 | $15 n$ | Par. | Hyb. | Vid., $75 \Omega \mathrm{o} / \mathrm{p}$, sync $i / p$, int. ref. |
|  | HDD1206 | 12 | $2 \mu$ | Par. | Hyb. | $\mathrm{I} / \mathrm{p}$ register, 6 MHz update, o/p. buff. |
|  | HDD1409 | 14 | $5 \mu$ | Par. | Hyb. | 200kHz sample rate, o/p buffer |
|  | HDG805 | 8 | 8 n | Par. | Hyb. | Video, -5.2 V supply, sync $i / p$ |
|  | HDG605 | 6 | 6 n | Par. | Hyb. | Video, -5.2 V supply, sync $i / p$ |
|  | HDG403 | 4 | 4 n | Par. | Hyb. | Video, -5.2V supply, sync i/p |
|  | HDH0802 | 8 | 200n | Par. | Hyb. | $10 \mathrm{~V} o / \mathrm{p}$, video, i/p buffer |
|  | HDS0820 | 8 | $20 n$ | Par. | Hyb. | $10 \mathrm{~mA} o / p$, video, i/p buffer |
|  | HDH1003 | 10 | 300 n | Par. | Hyb. | $10 \mathrm{~V} 0 / \mathrm{p}$, video, i/p buffer |
|  | HDH1205 | 12 | 500n | Par. | Hyb. | $10 \mathrm{~V} 0 / \mathrm{p}$, video, i/p buffer |
|  | HDM1210 | 12 | 175 n | Par. | - | Mult., 10 mA o/p, 10 MHz 3 dB analogue b.w. |
|  | HDS0810 | 8 | 10 n | Par. | Hyb. | -5.2V rail, $75 \Omega \mathrm{o} / \mathrm{p}$, e.c.l. $\mathrm{i} / \mathrm{p}$ |
|  | HDS0820 | 8 | $20 n$ | Par. | Hyb. | $10 \mathrm{~mA} 0 / \mathrm{p}$, video, int. ref., i/p buff. |
|  | HDS1015 | 10 | $15 n$ | Par. | Hyb. | $-5.2 V$ rail, $75 \Omega \mathrm{o} / \mathrm{p}$, e.c.l. i/p |
|  | HDS1025 | 10 | 25n | Par. | Hyb. | $10 \mathrm{~mA} \alpha / p$, video, e.c.l. $i / p$, int. ref. |
|  | HDS1240 | 12 | 40 n | Par. | Hyb. | $16 \mathrm{~mA} 0 / \mathrm{p}$, e.c.l. buff., int. ref. |
|  | HDS1250 | 12 | 35 n | Par. | Hyb. | $10 \mathrm{~mA} / \mathrm{o} / \mathrm{p}$, video, e.c.l. $\mathrm{i} / \mathrm{p}$, int. ref. |
|  | AH8304TC | 4x3 | $10 n$ | Latch | Hyb. | IV RGB 0/ps, t.t.l., synchronous blanking |
|  | AH8304TM | $4 \times 3$ | 50 n | Latch | Hyb. | As TC but with 32 word colour mem. |
|  | AH8S08E | 8 | 7 n | Latch | Hyb. | IV comp. vid. o/p, 5V supply, t.t.l. i/p |
|  | AH8308T | 8 | $15.5 n$ | Latch | Hyb. | IV comp. vid. o/p, 5V supply, t.t.l. i/p |
|  | AH8308TC | $8 \times 3$ | 10 n | Latch | Hyb | RGB IV o/p, t.t.l. i/p, synch. blanking |
|  | AH8404TC | 4x3 | $40 n$ | Latch | Hyb. | RGB IV o/p, t.t.l. i/p, o.6W. |
|  | AH8404TM | $4 \times 3$ | 30n | Latch | Hyb. | As 8404TC but with 32 word mem., 0.8 W |
|  | MP1480 | 12 | $10 \mu$ | Proc. | Mod. | 4-20mA current loopo/p, bin. or b.c.d. opts |
|  | MP1814 | 14 | <15 | Par. | Mod. | $\mathrm{V} 0 / \mathrm{p} 4$ rngs, int. ref., $\pm 0.003 \%$ f.s. lin. |
|  | MP1913A | 13 | $1 \mu$ | Latch | Mod. | I or $V \mathrm{o} / \mathrm{p}$, int. ref., $\pm 0.006 \%$ f.s. lin |
|  | MP1914A | 14 | $1 \mu$ | Latch | Mod. | I or V o/p, int. ref., $\pm 0.003 \%$ f.s. lin. |
|  | MP1914TC | 14 | $1 \mu$ | Latch | Mod. | As A vers. but lppm/ ${ }^{\circ} \mathrm{C}$ stab. not 2ppm |
|  | MP1915A | 15 | $1.2 \mu$ | Latch | Mod. | I or V o/p, int. ref., $\pm 0.0015 \%$ f.s. lin. |
|  | MP1915TC | 15 | $1.2 \mu$ | Latch | Mod. | As A vers. but lppm/ ${ }^{\circ} \mathrm{C}$ stab. not 2ppm |
|  | MP1916A | 16 | $1.5 \mu$ | Latch | Mod. | I or V o/p, int. ref., $\pm 0.001 \%$ f.s. lin. |
|  | MP1916TC | 16 | $1.5 \mu$ | Latch | Mod. | As A vers. but lppm/* ${ }^{\circ} \mathrm{C}$ stab. not 2 ppm |
|  | MP1926A | 16 | $<3 \mu$ | Par. | Mod. | Audio 0.005\% h. dist., int. ref., V o/p, 0.25 W |
|  | MP1926S | 16 | <40] | Par. | Mod. | Audio 0.005\% h. dist., int. ref., V o/p, 0.25 W |
|  | MP1936 | 16 | $6 \mu$ | Par. | Mod. | Audio -110dB noise, <-86dB f.s. h.dist., V o/p |
|  | MP8116 | 16 | $25 \mu$ | Latch | Mod. | $\pm 0.25$ bit lin., 3 V \& 2 I o/p rngs, $0.25 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ stab. |
|  | MP8308ECL | 8 | 10 n | Latch | Mod. | Video o/p, sync./blank i/ps, $\pm 5 \mathrm{~V}$ supplies |
|  | MP8308TTL | 8 | 25n | Latch | Mod. | Video o/p, sync./blank i/ps, $\pm 5 \mathrm{~V}$ supplies |
|  | MP8318ECL | 8 | $10 n$ | Latch | Mod. | Video o/p, $\pm 5 \mathrm{~V}$ supplies |
|  | MP8318TTL | 8 | 25n | Latch | Mod. | Video 0/p, $\pm 5 \mathrm{~V}$ supplies |
| Brooktree |  | $8 \times 3$ | 20n | Par. | C -mos | 50 MHz samp. RGB $19 \mathrm{~mA} / \mathrm{p}, 500 \mathrm{~mW}$, latches, 5 V |
|  | BT102* | 8 | $14 n$ | Par. | C -mos | 75 MHz 8 mp . vid., $28 \mathrm{~mA} 0 / \mathrm{p}, 500 \mathrm{~mW}$, latch, 5 V |
|  | BTl03* | $4 \times 3$ | 14 n | Par. | C -mos | 75 MHz samp. RGB $26 \mathrm{~mA} 0 / \mathrm{p}, 500 \mathrm{~mW}$, latches, 5 V |
|  | BT444* | $4 \times 3$ | 25n | Par. | C -mos | 40 MHz samp. RGB vid. $0 / \mathrm{p}, 600 \mathrm{~mW}$, latches |
| Burr-Brown | DAClOHT | 12 | 200n | Par. | Hyb. | Int. ref., -55 to $200^{\circ} \mathrm{C}, \pm 1 / 4$ bit linearity, I o/p |
|  | DAC60-12 | 12 | $150 n$ | Par. | Mod. | Int. ref., $\pm 1 /$ bit linearity, I o/p, lobit vers av. |
|  | DAC63 | 12 | 35n | Par. | Hyb. | Int. ref., $\pm 30 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ gain drift, I o/p |
|  | DAC70 | 16 | $50 \mu$ | Par. | Hyb. | Int. ref., I o/p, $\pm 0.003 \%$ f.s. linearity |
|  | DAC71/I | 16 | $1 \mu$ | Par. | Hyb. | Int. ref., I o/p, $\pm 0.003 \%$ f.s. linearit.y |
|  | DAC $71 / \mathrm{V}$ | 16 | $10 \mu$ | Par. | Hyb. | Int. ref., $\mathrm{V} 0 / \mathrm{p}, \pm 0.003 \%$ f.s. linearity |
|  | DAC72/I | 16 | $1 \mu$ | Par. | Hyb. | Int. ref., $\pm 0.003 \%$ f.s. linearity, 2 I o/p ranges |
|  | DAC72 N | 16 | $10 \mu$ | Par. | Hyb. | Int. ref., $\pm 0.003 \%$ f.s. linearity, $2 \mathrm{~V} 0 / \mathrm{p}$ ranges |
|  | DAC73 | 16 | $50 \mu$ | Latch | Mod. | Int. ref., I or V o/p $(\mathrm{V}=50 \mu \mathrm{~s})$, $\pm 0.00015 \% \mathrm{f.s}$. lin. |
|  | DAC74 | 16 | $20 \mu$ | Latch | Mod. | Self cal., $\pm 0.0015 \%$ total error, 10 or $\pm 10 \mathrm{~V} 0 / \mathrm{p}$ |
|  | DAC80/I | 12 | 300 n | Par. | Hyb. | Int. ref., 2 I 0/p rngs, $\pm 0.012 \%$ f.s. lin., 3 dig. vers |
|  | DAC80/V | 12 | $3 \mu$ | Par. | Hyb. | Int. ref., $5 \mathrm{~V} 0 / \mathrm{p}$ rngs, $\pm 0.012 \%$ f.s. lin., 3 dig. vers |
|  | DAC82 | 8 | $2.5 \mu$ | Par. | Hyb. | Mult., int. ref., 5 V \& 2 I o/p rnges, $\pm 0.16 \%$ f.s. lin. |
|  | DACB5/I | 12 | $300 n$ | Par. | Hyb. | Int. ref., 2 I o/p rngs, $\pm \frac{1}{2}$ bit f.s. lin. error |
|  | DAC85 N | 12 | $5 \mu$ | Par. | Hyb. | Int. ref., 5 V o/p rngs, $\pm 1 / 2 \mathrm{bit} \mathrm{f} . \mathrm{s}$. lin. error |
|  | DAC90 | 8 | 200n | Par. | Monol. | Int. ref., 2 I o/p rngs, $\pm$ thbit $\mathrm{f} . \mathrm{s}$. lin error |
|  | DAC700 | 16 | $350 n$ | Par. | Monol. | Int. ref., -2mA o/p, $< \pm 0.003 \%$ f.s. lin. error |
|  | DACr701 | 16 | $<8 \mu$ | Par. | Monol. | Int. ref., $10 \mathrm{~V} 0 / \mathrm{p},< \pm 0.003 \%$ f.s. lin. error |
|  | DAC702 | 16 | $350 n$ | Par. | Monol. | Int. ref. $\pm 1 \mathrm{~mA} 0 / \mathrm{p},< \pm 0.003 \%$ f.s. lin. error |
|  | DAC703 DAC706 | 16 16 | $<8 \mu$ $350 n$ | Par. | Monol. | Int. ref., $\pm 10 \mathrm{~V} / \mathrm{p},< \pm 0.003 \%$ f.s. lin. error |
|  | DAC706 DAC707 | 16 16 | $350 n$ $<8 \mu$ | Proc. | Hyb. Hyb. | Int. ref., $\pm 1 \mathrm{~mA} 0 / \mathrm{p},< \pm 0.003 \%$ f.s. linearity Int. ref., $\pm 10 \mathrm{~V} 0 / \mathrm{p},< \pm 0.003 \%$ f.s. linearity |
|  | DAC708 | 16 | 350 n | Proc. | Hyb. | Int. ref., $-2 \mathrm{~mA} 0 / \mathrm{p},< \pm 0.003 \%$ f.s. lin., ser. $i / p$ |
|  | DAC709 | 16 | < $8 \mu$ | Proc. | Hyb. | Int. ref., $10 \mathrm{~V} 0 / \mathrm{p},< \pm 0.003 \%$ f.s. lin., ser. $i / p$ |
|  | DAC800/I | 12 | 300 n | Par. | Monol. | Int. ref., 2 I 0/p rngs, $\pm$ \% bit linearity |
| Data Trans. | DT214 | $12 \times 4$ | $35 \mu$ | Par. | Mod. |  |
|  | DT214H | $12 \times 4$ | $8 \mu$ | Par. | Mod. | Mult., quad 10 V or $4-20 \mathrm{~mA} 0 / \mathrm{p}, \mathrm{c}-\mathrm{mos}$ opt. |
|  | DT215 | $8 \times 4$ | $35 \mu$ | Par. | Mod. | Mult., quad lov or 4-20mA o/p, c-mos opt. |
|  | DT215H | $8 \times 4$ | $8 \mu$ | Par. | Mod. | Mult., quad 10 V or 4-20mA o/p, c-mos opt. |
|  | DT212 | $12 \times 2$ | $1 \mu$ | Par. | Mod. | 2 ch . XY point plot, $50 \mathrm{~mA} 0 / \mathrm{ps}$, latches |
| Ferranti | 2N425 | 8/6 | $1 \mu$ | Par./ck | Bip. | Int. reference \& ramp count., V o/p, 5 V supply |
|  | 2N426 | 8/6 | $1 \mu$ | Par. | Bip. | Int. reference, $V o / p, 5 V$ supply |
|  | 2N428 | 8 | 800n | Proc. | Bip. | Int. reference, 5V supply, V o/p |
|  | 2N429 | 8 | $1 \mu$ | Par. | Bip. | 5V supply, V o/p, 25mW |
|  | 2N434 | 4 | 300n | Par. | Bip. | 5 V supply, ext. reference or int. $5 \mathrm{~V} / 2, \mathrm{~V} 0 / \mathrm{p}$ |
|  | 2N435 | 8 | 800 n | Par.,'ck | Bip. | Int. reference, ck \& u/d ramp count., V o/p, 5V |

New molybdenum- gate c-mos technique increases converter speed and accuracy

A newly developed c-mos i.c. process involving the use of molybdenum is now being used to manufacture a highspeed and accurate flash converter which, it is claimed, outperforms much more expensive hybrid devices.

Sampling at up to 2 MHz with $\pm \frac{1}{2}$ bit accuracy, the 11-bit monolithic flash converter costs significantly less than equivalent hybrid products says manufacturer and developer Micropower Systems.

Two-step conversion is used (see subranging converter under 'Converter terms'), one step for the five mostsignificant bits and one for the six least significant. Through use of an 'overflow' bit, two devices can easily be connected in series to give 12bit resolution. Alternatively, two devices can be connected in paratlel to give a 4 MHz sampling rate.

Refractory molybdenum gate metal with a low resistance of $0.5 \Omega$ per square resulting in very short delays of 0.5 ps over $10 \mu \mathrm{~m}$ at $3 \mu \mathrm{~m}$ width is the main feature of the patented c-mos process.


This speed compares with 10 to 20ps delays for silicon. Consumption of the device is 150 mW .

Not only speed is improved. Using molybdenum also allows more accurate and stable capacitors and resistors to be made on the chip. Dry plasma etching is used for the molybdenum pattern which gives precision matched resistors. Molybdenum with the second layer of aluminium is also used to produce 'auto-zero'

## capacitors

Direct ion implantation greatly improves parasitic input capacitance. The process is implemented using what is claimed to be a unique reduced-width molybdenum gate which does not overlap at the edges of the source and drain regions. The metal acts as a mask for ion implantation which brings the source and drain regions back to the edge of the gate as the diagram shows.

A non-critical self-aligned
process with low gate overlap capacitance results. Effective gate length of $2 \mu \mathrm{~m}$ with 0.1 pF overlap gate capacitor and less than 1ns gate delay are achieved.

Molybdenum is also used as a first layer metal interconnect to further improve circuit density and speed without other disadvantages, claims Micropower. Typical molybdenum interconnect time delay is less than 0.5 ps for each $10 \mu \mathrm{~m}$ length.
Moreover the molybdenum, with its low resistivity of $0.5 \Omega$ per square and ability to make good contact, is easily plasma etched to fine tolerances to make the precision resistors needed for quantizing voltage levels in a flash converter.

Second layer interconnect aluminium at $0.025 \Omega$ per square with silicon nitride dielectric between defines a reliable high-value capacitor of $0.8 \mathrm{pF} / 25 \mu \mathrm{~m}^{2}$. This further reduces parasitics associated with the capacitor bottom plate due to its much reduced size and increases dynamic range of the input signal.

| Manufacturer | Device | Bits | Speed | Interface | Tech. | Features |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | ZN436 | 6 | $1 \mu$ | Par. | Bip. | V o/p, 5V supply |
|  | ZN454 | $4 \times 3$ | 8 n | Par. | Bip. | $\mathrm{RGB} 0 / \mathrm{ps}$, syncs, int. reference, ext. gain set |
|  | ZN558 | 8 | 800 n | Par. | Bip. | Int. reference, latches, 5 V supply, V o/p |
| Honeywell <br> (S. P. Tech.) | CAL24010 | 12 |  |  |  | Calibrator, 1 to 0.001 decade attenuator |
|  | DAC805 | 8 | 5 n | Par. | Hyb. | 200 MHz samp. vid. + sync, int. ref./latch, HDG805 compat. |
|  | DAC9700 | 8 | 5 n | Par. | Bip. | 200 MHz semp. vid. + sync, int. ref./latch, AD9700 compat. |
|  | DAC34010 | $4 \times 3$ | 5 n | Par. | Bip. | 200 MHz samp. RGB + sync, int. ref./latches, -5 V supply |
|  | DAC34020 | $4 \times 3$ | 10 n | Par. | Bip. | 100 MHz samp. RGB + sync, int. reference/latches |
| Intech | DAC3400 | $4 \times 3$ | $15 n$ | Par. | C -mos | 40 MHz samp. RGB + sync, 5 V 250 mW , latches |
|  | DAC3405S | $4 \times 3$ | 15 n | Par. | $\mathrm{C}-\mathrm{mos}$ | 40 MHz samp . RGB + sync, int. ram, 5 V |
|  | DAC3800 | $8 \times 3$ | - | Par. | Hyb. | 40 MHz samp. RGB + sync, latches, 500 mW |
|  | DAC3808 | $8 \times 3$ | - | Par. | Hyb. | 40 MHz samp. RGB + sync, memory, 1.5 W |
|  | DACS150 | $4 \times 3$ | $13 n$ | Par. | E.c.l. | 80 MHz samp. RGB + sync, int. reference/ram |
|  | DAC5151 | $4 \times 3$ | 7 n | Par. | E.c.l. | 150 MHz samp. RGB + sync, int. ref., latches |
|  | DAC1840 | 8 | 15 n | Com. bin. | C -mos | 40 MHz samp., vid./sync o/p, latches, -5 V supply |
|  | DACl842 | 8 | 15 n | Bin. | C-mos | 40 MHz samp., vid./sync o/p, latches, -5 V supply |
| Intersil | AD7520 | 10 | 500 n | Par. | C -mos | Mult., 5V 20mW supply, Io/p, 200na o/p leakage. |
|  | AD7521 | 12 | 500 n | Par. | C-mos | Mult., 5V 20mW supply, I o/p, 200nA o/p leakage. |
|  | AD7323 | 8 | 100n | Par. | C -mos | Mult., 5V supply, 8/9/10bit lin. opts., I o/p |
|  | AD7530 | 10 | 500n | Par. | C -mos | Mult., 5V 20mW supply, Io/p, 300nA o/p leakage. |
|  | AD7531 | 12 | $500 n$ | Par. | C -mos | Mult., 5V 20mW supply, I o/p, 300nA o/p leakage. |
|  | AD7533 | 10 | 600 n | Par. | C -mos | Mult., 5V supply, 8/9/10bit lin. opts., I o/p |
|  | AD7541 | 12 | $1 \mu$ | Par. | C-mos | Mult., 5V supply, 11/l2bit lin. vers., I o/p |
|  | ICL7112 | 12 | 500 n | Par. | C-mos | Mult., 5V supply, $\pm 0.02 / 0.01 \%$ lin., I o/p |
|  | ICL7113 | 3dig. | 500n | Par. | C-mos | Mult., 5V supply, b.c.d. i/p, I o/p |
|  | ICL7134 | 14 | $3 \mu$ | Proc. | C -mos | Mult., + or +/-o/p, preliminary |
|  | ICL7520 | 10 | $500 n$ | Par. | C -mos | Mult., $20 \mathrm{~mW}, 8,9$ or 10 bit |
| Micro Networks | DAC71/I | 16 | $1 \mu$ | Par. | Hyb. | -2 or $\pm 1 \mathrm{~mA}$ o/p, int. ref., $\pm 0.003 \%$ f.s. linearity |
|  | DAC71/V | 16 | $10 \mu$ | Par. | Hyb. | 10 or $\pm 10 \mathrm{~V} 0 / \mathrm{p}$, int. ref., $\pm 0.003 \%$ f.s. linearity |
|  | DAC80/I | 12 | 300n | Par. | Hyb. | -2 or $\pm 1 \mathrm{~mA} 0 / \mathrm{p}$, int. ref., comp. bin./b.c.d. opts |
|  | DAC80/V | 12 | $3 \mu$ | Par. | Hyb. | 5 V //p ranges, int. ref., comp. bin./b.c.d. opts |
|  | DAC85/I | 12 | 300 n | Par. | Hyb. | -2 or $\pm \operatorname{lmA}$ o/p, int. ref., $\pm t_{2}$ or $1 / 4$ bit lin. opts |
|  | DAC85/V | 12 | $3 \mu$ | Par. | Hyb. | $5 \mathrm{~V} 0 / \mathrm{p}$ ranges, int. ref., $\pm \frac{1}{2}$ or $1 / 4$ bit lin. opts |
|  | DAC87 | 12 | $3 \mu$ | Par. | Hyb. | $5 \mathrm{~V} 0 / \mathrm{p}$ ranges, int. ref., < $\pm 1 / \mathrm{b}$ bit linearity, 0.9 W |
|  | DAC88 | 12 | <10ر | Latch | Hyb. | $3 \mathrm{~V} 0 / \mathrm{p}$ ranges, int. ref., < $\pm$ /2bit linearity, 0.76 W |

* Preliminary data only; these devices do not use $\mathrm{R}-2 \mathrm{R}$ ladder.

| Manufacturer | Device | Bits | Speed | Interface | Tech. | Meth. | Features |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| AMDAnalog Devices | Am6108 | 8 | $1 \mu$ | Proc. | Bip. | - | Int. ref., 0.1* lin., ratiom. |
|  | Am6112 | 12 | $7 \mu$ | Proc. | Bip. | S.a. | Prog. modes, 15 mA ref. o/p, 8 bit bus, lbit lin. |
|  | Am6148 | 8 | $1 \mu$ | Proc. | Bip. | - | Int. ref., 0.1\% lin., ratiom. |
|  | Am6688 | 4 | 5 n | Par. | Bip. | Samp. | 100 MHz rate, 50 MHz b.w., e.c.l. |
|  | AD376 | 8 | $15 \mu$ | - | Hyb. |  | Ref. |
|  | AD570 | 8 | $25 \mu$ | Par. 38 | Bip. | S.a. | Ref. \& int. ck, 10 or $\pm$ SV i/p |
|  | AD571 | 10 | 25 | Par. 38 | Bip. | S.a. | Ref. \& int. ck, 10 or $\pm 5 \mathrm{Vi} / \mathrm{p}$ |
|  | AD572 | 12 | <25 $\mu$ | Ser/par | Hyb. | S.a. | 0.012\% lin., long termstab., 900 mW |
|  | AD573 | 10 | 204 | Proc. | Bip. | S.a. | Ref. \& clock, 10 or $\pm 5 \mathrm{~V} \mathrm{i} / \mathrm{p}$ |
|  | AD574 | 12 | 25\% | Proc. | Hyb. | S.e. | l2bit bus, $250 n s$ access, 4 range i/p |
|  | AD575 | 10 | 304 | Ser. | Bip. | S.a. | Ref. \& int/ext ck, 4 range i/p |
|  | AD578 | 12 | $3 \mu$ | Par/ber | Hyb. | S.e. | $0.012 \%$ lin., long term stab., 4 range |
|  | AD579 | 10 | $1.8 \mu$ | Par. 38 | Hyb. | S.a. | 0.05\% lin., long term stab., 4 range |
|  | AD670 | 8 | $10 \mu$ | Proc. | Bip. | S.a. | Sig. cond. i/p, 5V supp., int. ref. |
|  | AD675 | 8 | 20ر | Proc. | Bip. | S.a. | Ref. \& clock, 10 or $\pm 5 \mathrm{~V} \mathrm{i} / \mathrm{p}$ |
|  | AD5010 | 6 | 10 n | Par. | Bip. | Flash | $100 \mathrm{MHz}, 450 \mathrm{~mW}$, e.c.l. $0 / \mathrm{p}$, $1 / 4$ bit lin. |
|  | AD5200 | 12 | 50M | Ser/par | Hyb. | S.a. | No adj., $0.4 \times$ f.s. abs. acc. |
|  | AD5210 | 12 | $13 \mu$ | Ser/par | Hyb. | S.a. | No adj., 0.1\% f.s. abs. acc. |
|  | AD5240 | 12 | $5 \mu$ | Ser/par | Hyb. | S.a. | $0.012 \%$ lin., long term stab. |
|  | AD6020 | 6 | 20 n | Par. | Bip. | Flarh | $50 \mathrm{MHz}, 450 \mathrm{~mW}$, e.c.l. $\mathrm{o} / \mathrm{p}$ |
|  | AD7550 | 13 | 40 m | Proc. | $\mathrm{C}-\mathrm{mos}$ | Q.slo. | Ratiom., lppm/ ${ }^{\circ} \mathrm{C}$, \%bit rel. acc. |
|  | AD7552 | 12 | 160 m | Proc. | $\mathrm{C}-\mathrm{mos}$ | Q.slo. | Ratiom., l lis.b. error |
|  | AD7571 | 10 | $80 \mu$ | Ser/par | $\mathrm{C}-\mathrm{mos}$ | s.a. | Diff. i/p, int. ck., lobit + sign |
|  | AD7574 | 8 | $15 \mu$ | Par. 38 | C -mos | S.a. | Ratiom., SV supp., diff. i/p, 30 mW |
|  | AD7576 | 8 | 104 | Proc. | $\mathrm{C}-\mathrm{mos}$ | S.a. | 15mW, 5 V supp., high i/p imp. |
|  | AD7578 | 12 | 100 $\mu$ | Proc. | $\mathrm{C}-\mathrm{mos}$ | S.a. | 8 bit bus, auto-zero, 75 mW |
|  | AD7581 | $8 \times 8$ | 66, | Proc. | $\mathrm{C}-\mathrm{mos}$ | S.a. | 8-i/p mpx, 64-bit mem., ratiometric |
|  | AD7582 | 12 | 1004 | Proc. | $\mathrm{C}-\mathrm{mos}$ | S.a. | 4-i/p mpx, 8bit bus, auto-zero |
|  | AD7820 | 8 | $1.4 \mu$ | Proc. | $\mathrm{C}-\mathrm{mos}$ | Subrng | Ratiometric, 5V supp., 75 mW |
|  | AD9000 | 6 | 13 n | Par. | Bip. | Flash | 75 MHz , e.c.l. $0 / \mathrm{p}$ |
|  | ADC71 | 16 | 45, | Ser/par | Hyb. | S.a. | $45 \mu \mathrm{~s}$ for $14 \mathrm{bit}, 0.003 \%$ lin., 850 mW |
|  | ADC72 | 16 | $45 \mu$ | Ser/par | Hyb. | S.a. | $45 \mu \mathrm{~s}$ for 14 bit , $0.003 \% \mathrm{lin} ., 850 \mathrm{~mW}$ |
|  | ADC80 | 12 | $25 \mu$ | Ser/par | Hyb. | S.a. | $0.012 \%$ lin., ref. $0 / \mathrm{p}, 5 \mathrm{i} / \mathrm{p}$ ranges |
|  | ADC84 | 10 | $6 \mu$ | Ser/par | Hyb. | S.a. | 0.048\% lin., ref. o/p, 5 i/p ranges |
|  | ADC85 | 12 | 104 | Ser/par | Hyb. | S.a. | 0.012\% lin., ref. o/p, $5 \mathrm{i} / \mathrm{p}$ ranges |
|  | ADC816 | 10 | 800 n | Ser/par | Hyb. | S.a. | thit lin., $6 \mathrm{i} / \mathrm{p}$ ranges, 15 V supp. |
|  | ADCl131 | 14 | $12 \mu$ | Ser/par |  | S.a. | $10 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ gain drift, 14 bit acc./res. |
|  | ADC1140 | 16 | 55 | Par. | Hyb. | S.a. | $0.003 \%$ lin. |
|  | ADCl143 | 16 | $70 \mu$ | Ser/par |  | S.a. | to $0.003 \%$ diff. lin., lppm/ ${ }^{\circ} \mathrm{C}, 150 \mathrm{~mW}$ |
|  | CAV0920 | 9 | 50 n | Par. | P.c. | Subrng | 20MHz, e.c.l. $0 / \mathrm{p}$ |
|  | CAV1040 | 10 | $25 n$ | Par. | P.c. | Subring | 40 MHz , e.c.l. o/p, range select |
|  | CAV1210 | 12 | 100 n | Par. | P.c. | Subrng | 10 MHz , e.c.l. o/p |
|  | HAS0802 | 8 | $1.2 \mu$ | Par. 3 s | Hyb. | S.a. | 0.05\% f.s. error, low power |
|  | HAS1002 | 10 | $1.7 \mu$ | Par. 3s | Hyb. | S.a. | 0.025\% f.s. error, low power |
|  | HASI201 | 12 | $1 \mu$ | Par. 3 s | Hyb. | - | Track \& hold, 1 MHz word rate |
|  | HAS1202 | 12 | $2.8 \mu$ | Par. 3s | Hyb. | S.a. | 0.012\% f.s. error, low power |
|  | HAS1204 | 12 | $2 \mu$ | Ser/par | Hyb. | Sample | 500 kHz word rate, 4 MHz bandwidth |
|  | HAS1409 | 14 | $8 \mu$ | Par. 3s | Hyb. | Subring | Track \& hold, 125 kHz rate, for $\mathrm{f} / \mathrm{t} . \mathrm{d} . \mathrm{m}$. |
|  | MATV811 | 8 | 90 n | Par. | P.c. | Subrng | Small llMHz vid., $743 \mathrm{o} / \mathrm{p}$, buff. i/p |
|  | MatV816 | 8 | $63 n$ | Par. | P.c. | Subrng | Small 16 MHz vid., 74S o/p, buff. i/p |
|  | MATV 820 | 8 | 50 n | Par. | P.c. | Flash | Small 20 MHz vid., buff. i/p |
|  | MOD1005 | 10 | 200n | Par. | P.c. | Subring | 20MHz analogue b.w., t.t.1. o/p |
|  | MOD1020 | 10 | 50 n | Par. | P.c. | Subrng | 20MHz word rate, e.c.l. $o / p$ |
|  | MOD1205 | 12 | 200n | Par. | P.c. | Subrng | 5 MHz word rate, t.t.l. $0 / \mathrm{p}$ |
| Analogic | ADAM724 | 14 | $6.8 \mu$ | Par. 3 s | Mod. | S.a. | Int. ref., s-s-h, p.g.a., $\pm 0.003 \%$ lin. |
|  | ADAM812 | $12 \times 2$ | $19.5 \mu$ | Par. | Mod. | S.a. | Int. ref., s- $8-\mathrm{h}, \pm 0.025 \%$ f.s. error |
|  | ADAM822 | $12 \times 2$ | 39 | Par. | Mod. | S.a. | Int. ref., s-8 $-\mathrm{h}, \pm 0.025 \%$ f.s. error |
|  | ADAM824 | 14 | $50 \mu$ | Par. 3s | Mod. | S.a. | Abs. acc. $\pm 0.006 \%$ f.s., 20 kHz rate, 0.9 W |
|  | ADAM825 | 15 | 59 | Par. 3s | Mod. | S.a. | As 824 but 18 kHz rate, both have s-8-h |
|  | ADAM826-1 | 16 | $2.3 \mu$ | Par. 3s | Mod. | S.a. | Int. s-s-h, 10 or $\pm 10 \mathrm{~V} \mathrm{i} / \mathrm{p}$ options |
|  | ADAM826-2 | 16 | $2 \mu$ | Par. 3s | Mod. | S.a. | Int. s- $8-\mathrm{h}, 10$ or $\pm 10 \mathrm{~V} \mathbf{i} / \mathrm{p}$ |
|  | ADAM826-3 | 16 | $1.5 \mu$ | Par. ${ }^{\text {Ps}}$ | Mod. | S.a. | Unbuffered i/p |
|  | ADAM834 | 14 | $63 \mu$ | Par. 3s | Mod. | S.a. | Int. s-8-h, wide temp. rng, $0.9 \mathrm{~W}, 50 \mu \mathrm{~V}$ noise |
|  | ADAM835 | 15 | $63 \mu$ | Par. 38 | Mod. | S.a. | As ADAM834 but l5bit, better lin. \& temp. co. |
|  | MP2S16 | 16 | 27 m | Pulse | Mod. | 2 sl . | Isolated with supply, p.g.a. \& reference |
|  | MP2321 | 3.5d | 10 m | Par. | Mod. | Int. | Ratiom., isol. b.c.d. o/p, int. supp. \& ref. |
|  | MP2522 | 12 | 10 m | Par. | Mod. | Int. | Retiom., isol. bin. $/$ /p, int. supp. \& ref. |
|  | MP2712 | 12 | $5 \mu$ | Par/ser | Mod. | S.a. | Int. ck/ref., $4 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.015 \%$ abs. acc. |
|  | MP2715 | 15 | 10, | Par/ser | Mod. | S.a. | Int. ck/ref., $4 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.009 \%$ abs. acc. |
|  | MP2714 | 14 | $10 \mu$ | Par/ser | Mod. | S.a. | Int. ck/ref., $4 \mathrm{i} / \mathrm{p}$ ranges. $\pm 0.007 \% \mathrm{abs}$ acc. |
|  | MP2734 | 14 | $6.8 \mu$ | Par. 38 | Mod. | - | Int. ck/ref., $4 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.007 \%$ abs. acc. |
|  | MP2735-1 | 15 | $5 \mu$ | Par. | Mod. | Subring | Audio $\pm 0.005 \%$ t.h.d., int. ref., 3dB idle noise |
|  | MP2735-2 | 15 | 54, | Par. | Mod. | Subrng | 2735-1 with no $8-8 \mathrm{c}-\mathrm{h}, 200 \mathrm{kHz}$ not 125 kHz rate |
|  | MP8008R | 8 | 3u | Par. 3 s | Mod. | Samp. | $0.02 \%$ differential linearity, $\pm 5 \mathrm{~V} \mathrm{i} / \mathrm{p}$ |
|  | MP8014 | 14 | $10 \mu$ | Par/ser | Mod. | S.a. | Int. ck/ref., $\pm 0.006 \%$ abs. acc., 10 or $\pm 10 \mathrm{~V} \mathrm{i} / \mathrm{p}$ |
|  | MP8015 | 15 | $15 \mu$ | Par/ser | Mod. | S.a. | Int. ck/ref., $\pm 0.006 \%$ abs. acc., 10 or $\pm 10 \mathrm{~V} \mathrm{i} / \mathrm{p}$ |
|  | MP8016 | 16 | $32 \mu$ | Par/ser | Mod. | S.e. | Int. ck/ref., $\pm 0.003 \% \mathrm{abs}$. acc., 10 or $\pm 10 \mathrm{~V} \mathrm{i} / \mathrm{p}$ |
|  | MP8037 | 17 | 4 ms | Par. | Mod. | Subrng | Ratiom., int. ck/ref., $\pm 0.005 \%$ abs. acc., 10 V i/p |
|  | SHADZA | $16 \times 2$ | $17.5 \mu$ | Par/ber | Mod. | 3-s1. | Audio 150 kHz samp. sing. ch., -86 dB distortion |
| Burr-Brown | ADClOHT | 12 | 50¢ | Par/ber | Hyb. | S.a. | Ck/ref., -55 to $200^{\circ} \mathrm{C}, \pm 0.012 \% \mathrm{f.s}$. lin., 0.25 W |
|  | ADC60-12 | 12 | $3.5 \mu$ | Par/ber | Mod. | S.a. | Int. ck/ref., $6 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.195 \%$ f.s. lin . |
|  | ADC60-10 | 10 | $1.88 \mu$ | Par/ber | Mod. | S.a. | Int. ck/ref., $6 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.0488 \%$ f.s. lin. |
|  | ADC60-8 | 8 | 0.884 | Par/ser | Mod. | S.a. | Int. ck/ref., $6 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.0244 \% \mathrm{f.s}$. lin. |
|  | ADC71 | 16 | $50 \mu$ | Par. | Hyb. | S.a. | Int. ck/ref., $6 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.003 \%$ f.s. lin. |
|  | ADC72 | 16 | 50, | Pars | Hyb. | S.a. | Int. ck/ref., $6 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.003 \%$ f.s. lin. |
|  | ADC73 | 16 | -170 | Par/ser | Mod. | S.a. | Int. ck/ref., $4 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.00075 \%$ f.s. lin. |
|  | ADC76 | 16 | $15 \mu$ | Par. | Hyb. | S.a. | Int. ck/ref., $6 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.003 \% \mathrm{f.s}. \mathrm{lin}$. |
|  | ADC $80-10$ | 10 | 21ر | Par/ser | Hyb. | S.e. | Int. ck/ref., $5 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.048 \%$ f.s. lin. |
|  | ADC80-12 | 12 | $25 \mu$ | Par/ser | Hyb. | s.a. | Int. ck/ref., $5 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.012 \%$ f.s. lin. |



| Manufacturer | Device | Bits | Speed | Interface | Tech. | Meth. | Features |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Data Trans.** | ADC82 | 8 | $2.8 \mu$ | Par/ser | Hyb. | S.a. | Int. ck/ref., $6 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.2 \%$ f.s. lin. |
|  | ADC84-10 | 10 | $6 \mu$ | Par/ser | Hyb. | S.a. | Int. ck/ref., $5 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.048 \% \mathrm{f.s}$. lin. |
|  | ADC84-12 | 12 | 104 | Par/ser | Hyb. | S.a. | Int. ck/ref., $3 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.012 \%$ f.s. lin. |
|  | ADC85 | 10/12 | 6/10ر | Par/ser | Hyb. | S.a. | As ADC84 10 \& l2bit, but better temp. co. |
|  | ADCl00 | 16 | 200m | Par/ser | Mod. | Int. | Ck/ref., 0.005\% lin., models for bin. \& b.c.d. o/p |
|  | ADC731 | 16 | $170 \mu$ | Par/ser | Mod. | s.a. | ADC73 with instrumentation amplifier i/p |
|  | ADC803 | 12 | $1.5 \mu$ | Par. | Hyb. | s.a. | Int. ck/ref., $3 \mathrm{i} / \mathrm{p}$ ranges, $\pm 0.012 \%$ f.s. lin. |
|  | ADC804 | 12 | $17 \mu$ | Ser. | Hyb. | S.a. | $\pm 0.012 \%$ f.s. lin., $<500 \mathrm{~mW}$ |
|  | PCM75 | 16 | 174 | Par. | Hyb. | S.a. | Audio, 0.004\% f.s. t.h.d., int. ck/ref. |
|  | DT5701 | 12 | $19 \mu$ | Par. | Mod. | - | $16 \mathrm{ch}$. mpx, 4 ranges, ser. $0 / \mathrm{p}$ opt. |
|  | DT5710 | 12 | $6 \mu$ | Par. | Mod. | - | $16 \mathrm{ch} . \mathrm{mpx}, 4$ ranges, ser. o/p opt. |
|  | DT5703 | 12 | - | Par. | Mod. | - | $4 \mathrm{ch} . \mathrm{mpx}, 10 \mathrm{mV}$ to $10 \mathrm{~V} \mathrm{i} / \mathrm{p}$, isolated |
|  | DT5704 | 12 | $10 \mu$ | Par. | Mod. | - | $4 \mathrm{ch} . \mathrm{s} / \mathrm{h} \mathrm{mpx} 10 \mathrm{~V} \mathrm{i} /$, |
|  | DT5712 | 12 | $25 \mu$ | Par. | Mod. | - | $16 \mathrm{ch} . \mathrm{mpx}, 10 \mathrm{mV}$ to $10 \mathrm{~V} \mathrm{i} / \mathrm{p}$ |
|  | DT5714 | 14 | $70 \mu$ | Par. | Mod. | - | $16 \mathrm{ch} . \mathrm{mpx}, 5 \mathrm{mV}$ to $10 \mathrm{~V} \mathrm{i} / \mathrm{p}$ |
|  | DT5716 | 16 | $350 \mu$ | Par. | Mod. | - | $16 \mathrm{ch} . \mathrm{mpx}, 5 \mathrm{mV}$ to $10 \mathrm{~V} \mathrm{i} / \mathrm{p}$ |
|  | DT3722 | 12 | $2.5 \mu$ | Par. | Mnd. | - | $16 \mathrm{ch} . \mathrm{mpx}$, opt. p.g.a., 3 range $\mathrm{i} / \mathrm{p}$ |
|  | DT5726 | 16 | $6 \mu$ | Par. | Mod. | - | $4 \mathrm{ch} . \mathrm{mpx}, \pm 10 \mathrm{~V} \mathrm{i} / \mathrm{p}$ |
| Ferranti | 2N425 | 8/6 | 1 m | Par. | Bip. | Ramp | Internal reference \& counter, 5 V supply |
|  | ZN427 | 8 | $10 \mu$ | Proc. | Bip. | S.a. | Internal reference, ratiometric |
|  | 2N432 | 10/8 | $15 \mu$ | Par/8er | Bip. | S.a. | Int. ref. \& amplifier |
|  | 2N433 | 10/8 | $1 \mu$ | Par/ser | Bip. | Track. | Int. ref. \& amplifier, |
|  | 2N435 | 8 | $800 \mu$ | Par. | Bip. | Ramp | Int. ck, ref. \& count., 5 V supp. |
|  | 2N439 | 8 | $5 \mu$ | Proc. | Bip. | S.a. | Int. ref., ck, $1 / 4$, $/$ or or lbit lin. options |
|  | 2N440 | 6 | 60 n | Par. | Bip. | Flash | 16 MHz rate, $\pm$ kbit lin., t.t.l., 0.7 W |
|  | ZN447 | 8/6 | $9 \mu$ | Proc. | Bip. | S.a. | Int. clock \& ref., $\pm 1 / 4$ bit linearity |
|  | 2N448 | 8/6 | $9 \mu$ | Proc. | Bip. | S.a. | Int. clock \& ref., $\pm$ \% bit linearity |
|  | 2N449 | 8/6 | $9 \mu$ | Proc. | Bip. | S.a. | Int. clock \& ref., $\pm$ lbit linearity |
|  | 2NSOI | 10 | $15 \mu$ | Proc. | Bip. | S.a. | Int. ref., l or 2 byte read, $\pm \%_{2}$ bit lin. |
|  | ZN502 | 10 | $15 \mu$ | Proc. | Bip. | S.a. | Int. ref., 1 or 2 byte read, $\pm$ lbit lin. |
| Intersil | ADC0801 | 8 | $<100 \mu$ | Proc. | C-mos | S.a. | Diff. 5V i/pp., 5V supp., $\pm 1 / 4$ bit lin. |
|  | ADC0802 | 8 | <100] | Proc. | C -mos | S.a. | Diff. 5V i/p, 5V supp., $\pm$ \%bit linearity |
|  | ADC0803 | 8 | <100] | Proc. | C-mos | S.a. | Diff. 5V i/p, 5V supp., $\pm$ /2bit linearity |
|  | ADC0804 | 8 | $<100 \mu$ | Proc. | C-mos | S.a. | Diff. 5V i/p, 5V supp., $\pm$ lbit linearity |
|  | ICL7109 | 12 | 0.03 | Proc. | C-mos | 2-sl. | Xtal i/p ck, diff. i/p, $15 \mu \mathrm{~V}$ noise |
|  | 8052/7104 | 14-16 | - | Proc./ser. | - | 2-81. | 2 i.c., ratiom., int. ck, ref., auto zero |
|  | 8068/7104 | 14-16 | - | Proc. ser. | - | 2-sl. | As above but 2 not 1 MHz analogue bandwidth |
| Micro Networks | ADC80 | 12 | $25 \mu$ | Par/ser | Hyb. | S.a. | İnt. ck/ref., $5 \mathrm{i} / \mathrm{p}$ ranges, $10 / 12 \mathrm{bit}$ opts |
|  | ADC84 | 12 | $8 \mu$ | Par/ber | Hyb. | S.a. | Int. ck/ref., $5 \mathrm{i} / \mathrm{p}$ ranges, $10 / 12 \mathrm{bit}$ opts |
|  | ADC85 | 12 | $8 \mu$ | Par/ber | Hyb. | S.a. | As ADC84 but 15 not 30ppm/C gain drift |
|  | ADC87 | 12 | $8 \mu$ | Par/ber | Hyb. | S.a. | As ADC85 but for -55 to $125^{\circ} \mathrm{C}$ |
|  | MN574A | 12 | $25 \mu$ | Proc. | Hyb. | S.a. | 8/16bit read, $\pm 0.012 \%$ f.s. err. int. ck/ref. |
|  | MN5065 | 8 | 100M | Par/ser | Hyb. | S.a. | Int. ref., 12 V 70 mW supp., $\pm 5 \mathrm{~V} \mathrm{i} / \mathrm{p}$ |
|  | MNS066 | 8 | $100 \mu$ | Par/ber | Hyb. | S.a. | Int. ref., 12 V 70 mW supp., $10 \mathrm{~V} \mathrm{i} / \mathrm{p}$ |
|  | MN5100 | 8 | $1.5 \mu$ | Par/ber | Hyb. | S.a. | Int. ref., $9 \mathrm{i} / \mathrm{p}$ ranges, $\pm$ \% lis.b. lin. |
|  | MNS101 | 8 | 900 n | Par/ser | Hyb. | S.a. | Int. ref., $9 \mathrm{i} / \mathrm{p}$ ranges, $\pm$ ¢ $1.8 . \mathrm{b}$. lin. |
|  | MN3120 | 8 | 6 4 | Par/ber | Hyb. | S.a. | Int. ref., $4 \mathrm{i} / \mathrm{p}$ range options |
|  | MN5130 | 8 | 2.54 | Par/ber | Hyb. | S.a. | Int. ref., $4 \mathrm{i} / \mathrm{p}$ range options |
|  | MN5140 | 8 | $2.5 \mu$ | Par/ber | Hyb. | S.a. | As 5130 but $\pm 12 \mathrm{~V}$ not $\pm 15 \mathrm{~V}$ supply |
|  | MN5150 | 8 | $2.5 \mu$ | Proc/ser | Hyb. | S.a. | Int. ref., $\pm$ t/ l.s.b. linearity |
|  | MN5200 | 12 | $50 \mu$ | Par/ser | Hyb. | S.a. | $0.05 \%$ f.s. err., 0.9 W , int. ref. opt. |
|  | MN5210 | 12 | $13 \mu$ | Par/ber | Hyb. | S.a. | 0.05\% f.s. err., 0.9W, int. ref. opt. |
|  | MN5240 | 12 | $5 \mu$ | Par/ser | Hyb. | S.a. | Int. ck \& ref., 5 buffered i/p ranges |
|  | MN5243 | 12 | $2 \mu$ | Par/ser | Hyb | S.a. | Int. ck \& ref., $6 \mathrm{i} / \mathrm{p}$ ranges, $10 / 12 \mathrm{bit}$ opts |
|  | MN5244 | 12 | $2 \mu$ | Par/ber | Hyb | S.a. | Int. ref., $6 \mathrm{i} / \mathrm{p}$ ranges, $10 / 12 \mathrm{bit}$ opts |
|  | MN5245 | 12 | 900 n | Par. | Hyb. | Subrng | Int. ref., 0.024* f.s. err., 5 V i/p |
|  | MN5243A | 12 | 900 n | Par. 3s | Hyb. | Subring | Int. ref., 0.024* f.s. err., $5 \mathrm{~V} \mathrm{i} / \mathrm{p}$ |
|  | MN5246 | 12 | 900 n | Par. | Hyb. | Subrng | Int. ref., 0.024* f.s. err., $\pm 2.5 \mathrm{~V}$ i/p |
|  | MN5246A | 12 | 900 n | Par. 3s | Hyb. | Subrng | Int. ref., 0.024* f.s. err., $\pm 2.5 \mathrm{~V}$ i/p |
|  | MN5247 | 12 | 450 n | Par. 3s | Hyb. | Subrng | Int. ref., 12 bit monot., 5 V i/p |
|  | MN5248 | 12 | 450 n | Par. 3s | Hyb. | Subrng | Int. ref., l2bit monot., $\pm 2.5 \mathrm{~V}$ i/p |
|  | MN5250 | 12 | $173 \mu$ | Par/ser | Hyb. | S.e. | $0.1 \%$ f.s. abs. err., $80 \mathrm{~mW}, 4 \mathrm{i} / \mathrm{p}$ range opts |
|  | MN5260 | 14 | 250M | Par/ser | Hyb | S.e. | $0.05 \%$ f.s. err., 500 mW , $\pm 10 \mathrm{~V} \mathrm{i} / \mathrm{p}$ |
|  | MN5280 | 16 | $100 \mu$ | Par/ser | Hyb. | S.e. | $0.006 \%$ f.s. linearity, $6 \mathrm{i} / \mathrm{p}$ rags, int. ref. |
|  | MN5282 | 16 | $50 \mu$ | Par/aer | Hyb. | S.e. | $0.006 \%$ f.s. linearity, $6 \mathrm{i} / \mathrm{p}$ rngs, int. ref. |
|  | MN5284 | 16 | ${ }^{50 \mu}$ | Par/ser | Hyb. | S.e. | 15 bit monot., $7 \mathrm{i} / \mathrm{p}$ rngs, 300mW |
|  | MN5290 | 16 | \$5 $\mu$ | Par/ser | Hyb. | s.a. | $0.003 \%$ f.s. lin., $6 \mathrm{i} / \mathrm{p}$ ranges, int. ck/ref. |
|  | MN5291 | 16 | 354 | Par/ser | Hyb. | S.a. | As 3290 but 13 not 14 bit mon. over temp. range |
|  | MN5420 | $12+4$ | $3.1 \mu$ | Par. | Mod. | - | Float. pt., $120 \mathrm{~dB}-10 \mu \mathrm{~V}$ in $10 \mathrm{~V}, 320 \mathrm{kHz}$ rate |
|  | MN5810 | 12 | $13 \mu$ | Par/ser | Hyb. | S.a. | \%/.s.b. lin., 915 mW , four range options |
|  | MN5700 | 12 | $250 \mu$ | Parlser | Hyb. | S.a. | 1\% f.s. err. at $200^{\circ} \mathrm{C}$, int. ref., $4 \mathrm{i} / \mathrm{p}$ rngs |
|  | MN5815 | 8 | 700 n | Par/ser | Hyb. | S.a. | Int. ck/ref., 6 rngs, log. sel. + or $\pm \mathrm{i} / \mathrm{p}$ |
|  | MN5825 | 8 | $1 \mu$ | Par/ser | Hyb. | S.e. | Int. ck/ref., 6 rngs, log. sel. + or $\pm \mathrm{i} / \mathrm{p}$ |
|  | MN7120 | 8 | $7 \mu$ | Parsis/ser | Hyb. | - | $8 \mathrm{ch} . \mathrm{mpx}, 75 \mathrm{kch} / \mathrm{s}$, int. $\mathrm{ck}, \pm \mathrm{L}_{2} \mathrm{bit} \mathrm{lin}$. |
|  | MN7140 | 12 | 401. | Par. | Hyb. | S.a. | $8 \mathrm{ch} . \mathrm{mpx}$., int. ck/ref., $0.1 \%$ f.s. abs. err. |
|  | MN7150-8 | 12 | $9 \mu$ | Proc. | Hyb. | - | $8 \mathrm{ch} . \mathrm{mpx}$ diff. hich-Z i/p, int. ck/ref. |
|  | MN7180-16 | 12 | $9 \mu$ | Proc. | Hyb. | - | $16 \mathrm{ch} . \mathrm{mpx}$ high-z i/p, int. $\mathrm{ck} / \mathrm{ref}$. . $50 \mathrm{k} \mathrm{ch} / \mathrm{s}$ |
|  | Company produces expanders for some listed devices and a large number of analosua input/output modules for specific computer buses and applications. |  |  |  |  |  |  |



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| AMD House | Analogic |
| Goldsworth Rd | The Centre |
| Woking | 68 HIgh St. |
| Surrey GU21 1JT | Weybridge KT13 8BN |
|  |  |
| AMI Microsystems | Burr Brown |
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| Wilts SN1 2HU | Coole Marketing |
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The rest of this list of i.cs and modules, logether wilh relevant addresses, will appear next month.

## New approach to instrumentation amplifier design

This idea deals with two new concepts, leading to a programmable amplifier design.
The first circuit uses theoretical results by Sun, according to which effective resistance $\mathrm{R}_{\text {eff }}$ of a resistor and switch in series is
approximately proportional to

$$
\left(\mathrm{R}+\mathrm{R}_{\mathrm{on}}\right) \mathrm{T}_{5} \mathrm{~d}=\mathrm{R}_{0} \mathrm{~T}_{5} / \mathrm{d}
$$

where $R_{\text {on }}$ is the on resistance of the switch, $\mathrm{T}_{\mathrm{s}}$ is the switching period and $d$ is the on time in a period. Circuit gain A is given by

$$
\left(1+2 \frac{R_{1}}{R_{n}}\right) \frac{d}{T_{5}}
$$

Gain of this instrumentation amplifier nay be programmed by choosing the ratio of $\mathrm{d} / \mathrm{T}_{\mathrm{s}}$, where $f_{s}=1 / T_{s}$, is the subaudio switching frequency. To obtain a positive output voltage, a fourth op-amp with feedback diode is applied to give the albsolute value of the output signal.
Two voltage op-amps at the input of the instrumentation amplifier are used in the second design. The difference amplifier is replaced by a transconductance op-amp with two linearizing diodes. For a transconductance op-amp, between the output current and input voltage $I_{\text {out }}=\mathrm{gV}_{\text {in }}$ is

thetransconductance of the op-amp where $g$ is $1_{c} / 2 \mathrm{~V}_{\mathrm{T}}$ which is $19.231_{c}$; control current $I_{c} \leqq 2 m A$.
Gain of the instrumentation amplifier shown in the second figure is given by

$$
A=19.23\left(1+2 \mathrm{R}_{\mathrm{t}} / \mathrm{R}_{2}\right) \mathrm{RI}_{\mathrm{C}} .
$$

Supposing ( $1+2 R_{1} / R_{2}$ ) is constant. gain A may be programned either by resistance R or more simply bycontrol current $l_{\text {c }}$.

## K. Kraus

Rokycany
Czechoslovakia
Sun Y. and Frisch 5., Resistance Multiplication by Means of
Switching. IEEE transactions on
Circuit Theory, Vol. CT-15, Sept. 1968 No.3. pp. 184-192.

## Pulses for medical use

We needed a device capabled of producing $30-100 \mathrm{~V}$ at 50 mA from 5 V pulses for use as a stimulator for diagnosing nerve palsy. The 5 V pulses come from a medical computer. Initially we used a pulse amplifer with a regulated power supply to compensate for fluctuating mains voltages, but this later approach is much simpler.

Transistor $\mathrm{Tr}_{1}$ is saturated by each positive pulse from the pulse transformer. This transistor's collector current pulses are applied to a shunt regulator, so output-pulse amplitude depends solely on the potentiometer setting.
provide additional safety is in case the mains transformer primary and secondary short.
José I. Crakovski
Buenos Aires

Argentina

Output voltage is independent of mains voltage variations. Resistors $\mathrm{R}_{1.2}$


## Economical long- time-constant integrator

Long time-constant integrators can be built if output of a voltage-to-frequency converter is connected to a counter feeding a d-to-a converter (block diagram). Resulting output is the integral of input because each v-to-f converter
may be taken as an integrator. Using a programmable timer, the design is similar and cheaper(r.h.diagram). Duration of timing cycle $T$ is given as NRC where N is an integer in the range $1 \leqq N \leqq 225$. When resistor $R$ is

(b)
replaced by a current source, frequency

$$
\mathrm{f}=\mathrm{V}_{\mathrm{in}} / \mathrm{NCR}_{\mathrm{E}} \mathrm{~V}_{\mathrm{K}}
$$

where $\mathrm{V}_{\mathrm{K}}$ is 3.8 V for BC 252 C .
Output is the integral of input voltage with a time constant
between $1 \mu$ sand 5 days.
Cascading timers gives
extremely long time constants.
Kamil Kraus
Rokycancy
Czechoslovakia
 interference.

## Power watchdog

Pulses from a computer port keep this power watchdog circuit activated by holding the p-channel power fet on. The dual fet network provides negative resistance. When the network is unbiased, current equal to the lower of the two $I_{\text {DDs }}$ can flow, keeping the p-channel device off even in the presence of considerable

Once current supplied by the 2N7000 exceeds zero, the j-fets soon pinch off. If the watchdog pulses fail, the RC network
discharges until voltage across it is less than the combined pinch-off voltage, when the transistor turns off rapidly.

Devices with from 3-7V pinch-off voltage are suitable for this arrangement. Oider dmos devices with gate zener diodes or less than 40 V drainsource voltage should not be used.
Components R and C are chosen to suit the application. Leakage of the fet is typically less than $\operatorname{lnA}$ in the pinchedoff condition.
M.D. Bacon

Taunton
Somerset
ELECTRONICS \& WIRELESS WORLD FEBRUARY 1986

## Burglar alarm

In spite of the simple appearance of this circuit. it has many features - keypad lock/unlock, arm delay, alarm delay, 15 min alarm timeout, eight sensor loops and an anti-tamper interlock. There are four mat and four loop sensors.

The keypad is straightforward and may be replaced by a key switch. Heart of the circuit is a 4060 oscillator and divider which provides timing.
In safe mode, the oscillator and bistable devices are reset. On arming, the first 60s cycle elapses and inhibits the clock but enables the sensor latch. When triggering occurs, the clock is enabled and after 60s the alarm is set for a further $7.5,15$ or 30 min depending on the circuit setting. After this period, the circuit returns to the initial armed mode ready for the next break-in.

Switching the keypad to safe at any time resets the control circuit. Affected zones are indicated by leds. Use a lead-acid accumulator and not an NiCd battery - it is more reliable. Cutting the keypad wire does not stop the alarm.

## Quentin Rice

Lower Kingswood Surrey


## Simple charger for AA cells

Constant current of 50 mA for $14-16$ hours is usually needed for AA NiCd cells.
Overcharging at the correct current does not harm the batteries so an overnight charge is possible using a constant-current charger.

Up to six cells can be charged at once using this simple circuit. Besides indicating that the cells are properly conncected and being charged, the led forms a constant-voltage source. When the cells are not connected, the led is off.

Resistor R determines
charge current.
V. Mehra

Chandigarh
India


## Shaft encoder counting

Croft's circuit for shaft encoder counting in the November issue is effective in many applications but it can miscount if repeated reversals occur.
As the first timing diagram shows, if the shaft is repeatedly reversed over a fraction of a cycle it is possible to produce a unidirectional count even though no net motion has occurred. This can happen in practice if there is mechanical bounce on starting or stopping the shaft.
To solve this problem, a onebit longer counter is needed; twice the number of counts are
generated compared with Croft's system. The first Or gate produces a transition at every transition of either of the quadrature lines.
A brief negative transition is produced by the second Or gate at every transition from the first gate because the signal on one of its inputs is inverted and delayed compared with the other one. Trailing edges of these pulses clock the counter, after the up/down line has had plenty of time to settle.
M. Winder

Reading University
Berkshire


## Analogue voltage multiplier

Suitable for low-frequency applications, this circuit was designed for use in measurement of patients' breathing patterns. Differential inputs A are provided, and $\mathrm{A}_{+}$ must always be positive with respect to $\mathrm{A}_{-}$. Input B can be positive or negative, as the 4016 analogue switch is at a virtual earth. The circuit can be rearranged as shown to form a divider.

Remaining i.c. elements were used in sample-and-hold circuits.
G.G.R. Rutter

London

multiplexer during refresh, and $\mathrm{A}_{14}$ during read/write cycles.
Row-address strobe RAS is produced by the MREG memory request signal. Switch signal MUX is provided by the next clock cycle after MREQ goes low provided that RFSH is high, therefore not switching during refresh. Columnaddress stobe $\overline{\mathrm{CAS}}$ is produced from $\overline{\text { MUX }}$ after delay and inversion.
Using this circuit and simple wire links on the p.c.b., 16 K drams can be exchanged for 64 K types using the same sockets and p.c.b.
R.J. McClelland

Liverpool
Merseyside

Delay to allow time for the multiplexer to settle MAO to MA7 before producing [AS

## Multiplexer for 16 or 64 K d-rams

In designing a 280 -based computer, I produced this circuit allowing simple switching between 16 and 64 K d-rams.
For 16 K rams, the usual multiplexed addresses are produced as $\mathrm{MA}_{0-6}$. A further multiplexed address is needed for 64 K devices, for which I used the remaining top two bits of the address bus $\mathrm{A}_{14.15}$ to provide multiplexed addresses for 16 and 64 K d-rams during write/read cycles.
A problem with 64 K rams is that during refresh they need $\mathrm{A}_{7}$ on $\mathrm{MA}_{7}$, not $\mathrm{A}_{14}$ as it would be on the system described so far. To overcome this I use the $\overline{\text { RFSH }}$ signal to gate $\mathrm{A}_{7}$ to the

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# Short-wave loop aerial 

# Modifications to the earlier designs enable the aerial to be used with domestic receivers 

In April 1985, S. Mukherjee described a useful indoor short-wave aerial for use with well-screened receivers. His design is not very suited to ordinary domestic receivers because their lack of screening allows signals to bypass the loop. The result is loss of directionality and, at the same time, trouble from local interference of the kind which a magnetic aerial rejects.
Some relatively simple changes can avoid these problems. The first requirement is to provide the receiver with some sort of screening enclosure to exclude direct pickup. A complete screening box is impracticable since it would prevent access to the controls. Experiment shows that an open-fronted box will work, provided that it is deep enough for the receiver to be pushed well inside.
My tests indicate that a cardboard box covered with aluminium kitchen foil makes an adequate short-wave screen. On long and medium waves the amount of screening provided by the thin foil is reduced, enabling the receiver's ferrite aerial to function on these bands.

Having eliminated direct pickup of short-wave signals, the next job is to deal with pickup by the downlead. This is done in two steps. First, an unscreened, unearthed loop is substituted for the original design. Any thick, insulated wire (such as mains flex) can be used for the loop, the signals being extracted via a transformer. The primary is formed by passing one or two turns of the loop conductor round a ferrite rod (a). (An aerial rod from an old m.w. receiver is adequate.) Coupling to the unscreened twin downlead is effected by a secondary winding: two or three turns will generally be optimum, but the user can easily experiment with different numbers. For reasons explained below it is useful to make the secondary detachable.
Although considerations of symmetry suggest an arrangement like (a), where the loop can float above earth in a balanced fashion, practical use is eased by putting the tuning capacitor at the bottom (b) where it is easily reached. I have not noticed any impairment in performance from the assymmetry which results.

The aerial and clownlead are balanced, but the receiver input circuit is not. A balun is needed, and this can take the form of a centre-tapped autotransformer (c), made with a bifilar winding of hookup wire on a magnetic core. Possible core materials are pieces of ferrite aerial rod, ferrite toroids, and tuning slugs of the throughhole type, which can be used as toroids. In general, the number of turns needed is $5-10$, connected as shown. The balun is placed either just outside or just inside the screening box, with its centre tap connected to the foil by a short lead (fold its end into the foil or staple it to the foil). Coupling to the receiver is by wrapping a few turns of insulated wire round the end of the built-in telescopic aerial. (I find that this is still the best method, even in a receiver which also has proper aerial and earth terminals. It is not necessary to earth the screening box except when power supply considerations require it as explained later.
Check for downlead pickup by slipping the secondary coil off the transformer rod. Signals

P42

Fig. 1 (a) shows the one or two-turn primary on ferrite rod and, at (b), the recommended capacitor position. At (c) is the balun to match aerial and downlead to receiver and (d) shows the method of avoiding signal injection from the power-supply lead.

continued from $p 46$
should vanish or at least become very noisy.

If a receiver is mains operated, the mains lead brings unwanted signals into the screening box. A power-supply filter is then required. My own receiver is a battery-powered one which can be mains-driven via an external adapter (trans-former-rectifier unit) which supplies the required low-voltage d.c. via a long lead. In this case, the appropriate side of the d.c. supply is connected to the screening foil and the 'live' side taken to the receiver via a three-terminal capacitor-type filter (d). A lead from the earthy battery terminal of the receiver is connected to the foil to complete the circuit. A conventional pi-section LC filter can also be used: I had good results from a home-made filter where the series $L$ was a tv frame coil on a ferrite ring core and the Cs were 100 nF polyester film capacitors. Whatever arrangement is used it is essential to keep the connections between capacitors and screening foil very short - a centimetre or less. If longer, their inductance impairs filtering. The case of my feed-through filter is the earth terminal and contact with the foil is made by bolting the filter unit to the screening box. The earth connections are made by trapping the bared ends of the earthy d.c. leads between filter and foil.
I have not so far attempted a filter for a receiver with a builtin mains power unit. A balanced filter would presumably be needed, with the earth line connected to the foil and to mains earth. Safety considerations suggest that the screening box should itself be enclosed in an insulating box to avoid contact with the foil.
If the receiver can be battery operated it is useful, when testing power-supply filters, to set up the receiver with the filter in situ but the mains power off. If the receiver is now battery operated it can be seen if signals are getting into the box via the filter.
When operating a wellscreened receiver, bringing one's hand to the controls introduces stray signals. This can be an advantage since it allows the receiver to be pretuned to the required frequency before tuning in the loop.

## INDOOR LOOP <br> AERIAL

If you happen to live near a powerful radio transmitter you will find that short-wave reception is marred by breakthrough by the local transmission. This can occur even when the wanted station is far removed in frequency from the local transmission, through such mechanisms as intermodulation.
In principle, the directional properties of a loop aerial can be utilized to null the local
transmission but, in practice, a simple loop oriented in the vertical plane does not give a complete null. The reason is that the ground wave from the local transmitter is not quite vertically polarized but tilted by wave drag.
The loop null can be intproved by tilting the loop away from the vertical to match the interference. Readers who suffer from localstation interference might find it useful to construct short-wave loops in a way which permits some adjustments of tilt. For most cases a tilt range of $0-30^{\circ}$ will be sufficient.
R. Jones

Dorchester
Dorset

## FFT

Your contributors Larsen and Dyrik express the hope that their article will inspire readers to experiement with machine code f.f.ts and spectral analysis.

We took this path some years ago and can report that indeed many happy hours can be spent optimising an implementation of the f.f.t. algorithm, and one dicovers many subtle issues that do not seem to be covered in the standard literature.
Starting from the Basic program given, the main decision to be made in preparing a machine-code version is how to represent the data arrays D and E. If floating point is used, execution will be little faster than in Basic. With fixed point, however, optimizing the dynamic range is a non-trivial problem, since the data values grow in a way which cannot reasonably be predicted at the outset. Automatic rescaling is thus usual and desirable, but this raises yet another level of subtlety if the rounding or truncation inherent in a rescaling is not to contribute further errors. Welch ${ }^{1}$ considers three strategies, none of which is optimal.
For those who are more interested in the finished article than the joys and frustrations of development, we have made our BBC spectrum analyser commercially available through

Structured Softare, and will be pleased to supply full details on request.
P.G. Craven
J.C. Davies

Bromborough
Wirral
Merseyside

## Reference

1. Welch, P.D., A Fixed-Point Fast Fourier Transform Error Analysis. IEEE Trans Audio \&
Electroacoustics AU-17, 2, 151-157 (JUne 1969).

## ADD-ON CURRENT DUMPER

I was very interested to read Erik Margan's add-on circuit to convert a conventional Class B amplifier output into a non-switching type. I have, in the past, tried to develop such a circuit, but have never been fully satisfied with my efforts. Mr Margan's circuit appear to be a very competent solution.
Mr Margan gives no clue regarding the value of $\mathrm{R}_{\mathrm{e}}$. However, analysis of the circuit indicates that if $R_{c}$ is less than about one fifth of the value of $\mathrm{R}_{\mathrm{e}}$, the circuit current limiting will come into operation before $\mathrm{Tr}_{3}$ or $\mathrm{Tr}_{4}$ are turned off.
I would be very interested to know of the effect of Mr Margan's modifications on the distortion figures of a typical Class B amplifier and the extent to which an improvement in sound quality may be heard.
Graham Nalty
Borrowash
Derby

## ENERGY <br> TRANSFER

P. L. Taylor (Wireless World, p. 15 October 1985) likes the choice between e.m. wave energy transfer through space, as required by the Poynting vector, or through wires, as required by the Slepian vector. There is, in fact, a third choice advocated by Cambridge Professor G. H. Livens. Writing 'On the flux of energy in radiation fields' at $p$. 313 of his 1926 book 'The Theory of Electricity', published by Cambridge University Press, he argued in favour of an alternative to Poynting's theory. Waves do not need to carry energy at their speed of propagation. Their generation merely adds energy to a common pool of energy in the field medium at the locality of the transmitter and their absorption draws on that pool in the locality of the receiver. I like this third alternative, because it is easier for me to picture
creation a a big splash in an existing smooth pool of energy than as a big bang appearing from nowhere in a complete void.
J.N. Kidman

Southampton

## NAVAL MARCONI

In the November issue you had an article by Nigel Cawthorne, which I am happy to say was complimentary to Marconi in most respects, but did rather belittle the Marconi Fast Tune (MFT) range of equipment. I would like to point out that in addition to the drive and 10 kW amplifiers we also have a 50 kW i.s.b. amplifier, a 1 kW amplifier and a transceiver based on the drive/receiver in
development. But by far the most important part of MFT2 is the remote computer control system that goes along with the basic hardware; this system allows for automation in service selection which includes frequency, mode, audio source and antenna selection, along with any other aspect that needs controlling.
I would also take this
opportunity to point out that our new Swordfish transceiver is not, as depicted in the picture caption Redifon's R800 v.l.f. receiver.
P.A.T. Turrall,

Publicity Manager,
Marconi Communication Systems, Chelmsford

## RELATIVELY BORING

H. Morgan complains in your July issue that relativity is boring. This view will be shared by many physicists, but they do not seem to have noticed that one cause of the confusions and contradictions is that it is not a scientific theory. This Einstein made quite clear when he said that the "real basis of the special relativity theory" was the Lorentz equations (Bull. Amer. Math. Soc., 41, 1935). Physics is based on matter, motion and force: equations in physics are only relations between terms that represent numbers obtained by measurement; and these are put into Nature by ourselves. They can never tell us, just as Einstein could not, whether an ether was a necessary physical assumption or not: at one time he had said not; and then later "space without ether is unthinkable'". Moreover, Lorentz's times were dates and these do not enter into physical laws.
Many other confusions are caused by lack of linguistic care. If we think carefully about light, for example, we realise that we never
see light, or anything moving, and that beams and rays cannot be found in highly evacuated regions, so that reflection may be reradiation. One fact about light has, however, been verified sufficiently to give us considerable confidence in its truth; this that if we have a source and a receiver at a fixed distance from one another on a rigid body, the time delay of interaction between them is always $\mathrm{d} / \mathrm{c}$ where c is a universal constant. I have suggested that c should be called the constant of interaction: no hypothetical element is then involved (such as ether, waves, photons and the rest) and action at a distance is not ruled out (as Maxwell admitted long ago). This one fact allows us to settle the thought experiment involving a train passing an embankment, which relativists use to 'prove' the supposed relatively of simultaneity.

The train and the embankment are said to be struck by lighting at two places a distance apart. An observer on the embankment, halfway between the two flashes, is said to find them both simultaneous, but the observer on the train is said not to agree. In this case there are two rigid bodies - the embankment and the train and both observers are at a distance $\mathrm{d} / 2$ from both flashes. The time for interaction is thus the same for both flashes so that both observers should find simultaneity. If the sources are said to be moving with respect to the observer on the train, this should cause no difference, since the 'velocity of light' is held to be independent of the motion of the source.

As length-contraction is 'proved' in thought experiments by founding it in the supposed relativity of simultaneity, is clear that length contraction is also delusory.

A note of interest is a recent statement from a colleague of Einstein's who says that in his later years Einstein abandoned material consequences implied by relativity, which included his thought experiment purporting to show that people can get younger by rushing about - the Twins Paradox (Foundations of Physics, 15, 9, 1985).
G. Burniston Brown

Padstow
Cornwall

## ELECTROLYTICS AND DISTORTION

Since both Mr Curl and Mr Armstrong (Letters, November 1985) are writing on the same topic, it seems logical to try to answer their complaints in the same letter.

I hoped that by now I had made it clear that I am perfectly well aware that it is possible to use electrolytic capacitors in such a way as to generate disturbances in an applied audio signal; the point I wish to make is that there is nothing new or mysterious about this. The effect (low-frequency harmonic distortion when an electrolytic is allowed to cyclically depolarize) is logical and predictable, and therefore avoidable. It should not arise in a properly-executed audio design.

To recapitulate, the important point is simply to ensure that there is no significant a.c. voltage across the capacitor in question. When an electrolytic is used as a coupling or dc-blocking component there is no reason why there should be; if there is then you have, accidentally or otherwise, made a high-pass filter of dubious accuracy due to the wide tolerance of electrolytics. The a.c. voltage across the capacitor can then give rise to unpleasant effects, of which depolarization is probably the worst, as it has depressing implications for the longevity of the component.


Figure 1 shows my own, simpler, method of demonstrating that capacitors generate distortion when misused. This is a simple high-pass filter; below it is shown a table of the distortion produced, against input frequency.

Harmonic distortion is unmeasurable from 20 kHz down to 30 Hz , where things suddenly start to go wrong. Under these conditions, it is at this point that the peak voltage across the capacitor reaches 1.4 V . This seems to be the threshold at which the capacitor dielectric film starts to come undone, though dielectric absorption effects could be playing a part. Perhaps a capacitor manufacturer would like to contribute some information on this point.

Experimenting with different values of $R$ and $C$ confirms that the crucial factor is the peak a.c. voltage across the capacitor. The conclusion to be drawn is simply

that you must avoid using electrolytics (including tantalums) as filter elements, for which purpose they are quite unsuitable anyway, due to their wide tolerances, and confine them to coupling duties, where it is easy to arrange for there to be no significant signal voltage across them. Simply ensuring that there is no premature l.f. roll-off is normally sufficient to take care of this point.
The use of unbiased electrolytics for coupling purposes has a history of at least twelve years, going back to the introduction of the first really practical op-amps. It was clear that the use of $+/$ - power rails, while giving designs a greatly appreciated freedom from d.c. standing currents flowing down signal earths, would demand the use of electrolytics operating under zero-bias conditions.

There were many hasty consultations with capacitor manufacturers before it became clear that reliability would not normally be a problem. This is attributable to the absence of signal voltage across the capacitors in a well-designed coupling arrangement.

Having studied the test-circuit provided by Mr Curl, I can confirm that a non-nullable pulse residual is indeed produced; my own test assembly produced waveforms similar to those accompanying Mr Curl's letter in HiFi News ${ }^{1}$. It is not necessary to use exotic and
expensive devices such as the AD524 - a conventional instrumentation-amplifier arrangement using TL072s gives exactly the same results in this case, providing close attention is paid to trimming the c.m.r.r. My arrangement is shown in Fig. 2. However, I am inclined to think this is just a complicated way of demonstrating the same effect that Fig. 1 produces. Taking, for example, a 10 ms input pulse at point $A$, the change in voltage across the capacitor under test (c.u.t.) is 5.8 volts peak to peak, the c.u.t. being reverse-biased by about 2 volts for part of the cycle; the capacitor is not being treated kindly. This voltage is measured using A7,8,9, which forms a second instrumentation-amp. across the c.u.t. However, I submit that this ingenious test has no relevance to properly-designed audio coupling networks, as I have explained above. The lifetime of a capacitor used in such a way will be very uncertain.
Consider in what the circumstances this effect could constitute a real problem; the most obvious is the case of a warped record feeding its signal through to a preamplifier. However, it is normally considered that even a badly warped disc is unlikely to produce subsonic levels greater than -20 dB below the general levels in the audio band, ${ }^{2}$ and it will be noted that in Fig. 1 it is necessary to use signal levels only
just inside op-amp headroom to induce the lf distortion.
Nevertheless, it is always good practice to place the subsonic filtering as early as possible in the audio chain. The preamplifier design that opened this audio can of worms has its subsonic filter immediately after the disc preamp. stage, ${ }^{3}$ and in fact the only electrolytic capacitor the signal has passed through before it is the one at the very input, where signal levels average 5 mV rms. I would suggest there will be no problems there.

One criticism that may well be levelled at my reasoning is that sinewave-and-analyser testing is hopelessly unhip, and that there are all sorts of degradation phenomena that ignore sinusoids but mangle music. I have yet to see proposed any plausible mechanism that could ignore single sinewaves anywhere in the audio band, and yet still affect complex signals.

In the course of writing this reply, I re-read the reference Mr Curl cited. In some ways the articles by Jung and Marsh ${ }^{4}$ are impressive, including as they do a comprehensive survey of capacitor theory and construction,
culminating in some pictures of distortion residuals very similar to those I obtained with the circuit of Fig.1, though they nowhere make the point that no-one in their senses would make a high-pass filter with electrolytics. From this they go on to state that "When music is the a.c. signal, the sonic degradation is one of compression or a restriction of the dynamic range." I find this statement remarkable, if not actually frightening, as it implies that the capacitor is either turning up the gain in the presence of a low signal, or turning it down in the presence of a high one. I do not believe that any such effect could be measured with any type of capacitor, and I fear that this is another example of an unjustified conceptual leap beteen a known physical phenomenon, and an extremely speculative conclusion. I regret to say that such conceptual pole-vaulting is common in the hi-fi press, and is in danger of making the whole field an object of ridicule to those involved in serious engineering.
I cannot believe that I am the only one who finds it disturbing that people make such extraordinary claims without any attempt to explain how such a mechanism could conceivably operate, or making even the roughest numerical estimate of its magnitude.

I should like to say that I agree whole-heartedly with the views expressed by Mr Peter Baxandall in the correspondence columns of

HiFi News. It has become the accepted norm to pay a quite undue amount of attention to people simply asserting that such-and-such an effect occurs (it really does sound better . . .) without any sort of objective evidence. Any "new effects" allegedly discovered need the following before becoming even slightly respectable.
a) A set of double-blind, properly-conducted (no easy matter) listening tests to show that the effect really does exist, verified by a rigorous statistical analysis
b) A theoretical mechanism for the operation of the effect that is at least logically consistent, if not actually plausible.
This second condition in particular is almost always lacking in the wilder statements made about audio design.
If I can now address Mr Armstrong in particular, I must say the gold flashing on his telephone leaves me unmoved. I assume it is there to enhance reliability in unfriendly environments, as given the millions of telephones installed their reliability is of great importance. I would suggest that it is unlikely that his 'phone company are attempting to scale the higher pinnacles of hi-fi reproduction.
Secondly, I am also unimpressed by the wire-crushing thumb-wheels (or was it thumb-crushing wirewheels?) on his electricity meter. These are to ensure an accurate absolute measurement under highcurrent conditions, whereas in audio a gain variation of a few tenths of a dB are quite unimportant, always assuming that they are not level-dependent, of course.
As for Mr Armstrong's defective head amp., miraculously taking up its p.c.b. and walking after a shot of expensive capacitors, all I can say is that as far as I am concerned this kind of anecdotal evidence is worse than useless. If Mr Armtrong really has found a new psychoacoustic effect, then I would dearly like to know how it works, so I can use it. However, my own suspicion is that it's one more case of "experimenter effect".
One more thing. I try not to take all of this too seriously, but I think must decline to be labelled a pendant just because I insist that science and engineering are about reality and repeatable measurements rather than unsupported assertions. I am an engineer, and I hope that my approach to engineering is scientific, because I cannot think of any other that would work.
You might as well accuse an accountant of pedantry when he fails to embezzle his client's money.
D.R.G. Self

Bow
London WC

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Aug, 1985, p15.
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Requirements of Phonographic
Preamplifiers."', AUDIO July, 1977.
pp72-79.
3. D.R.G. Self, "A Precision

Preamplifier.", Wireless World Oct, 1983.
4. Jung \& Marsh, "Picking Capacitors" ACDIO Feb, 1980, pp52-62.
5. P. Baxandall, "Views" HFN/RR July, 1985. pp15-17.

## PRECISION <br> PRGAMPLIFIER

I agree with Mr Armstrong
(November, 1985 Letters) that Mr Self does appear pedantic, even didactic, in print, but think that Mr Self has a point in which, however, there is confusion of engineering and other factors.

Ultimately, uncontrollable variations in manufacture result in what are, on a scale of perfection, gross differences between individual items of components, let alone the differences to which Mr Curl draws attention ( $E W W$.Nov, 1985) for capacitors. On this scale of perfection every item within auditoria and studios, performance, recording or transmission, including links, and reproduction, including rooms, has a similarly highly variable effect on what we can hear, as well as undoubted variations in our own biological systems on different social and emotional levels and time scales.
In the mid-fifties I knew several professional musicians and as I got to know them it became plain that, despite acute musical appreciation of the 'sound' of auditoria and of different performers' effects on performances, when it came to radio and record reproduction they were largely indifferent to sound quality. What, it seems, they had been taught to look for were the minds and emotions of the composer and performer(s) at work and it was these that they were listening for and identifying with. As with language, it was 'the meaning' rather than detailed syntax and sound that they responded to.
So for those who like realistic quality of sound (in other than live performances), whether we put into any new system any capacitors at all or even specially selected ones may perhaps produce the ultimate of what can be heard, but each single system will have an individual sound, unlikely to be perfect reproduction of the original. But if we can accept this sound then we can relax and enjoy as many as possible of the subtleties of performance rather than be obsessed with those of the sound alone. Particularly, we have to beware of a psychological
readiness increased by highly personal criticism and advertising to accept new and expensive techniques and attitudes as inevitably better, rather than just different!

Far more insidious is the overall rise in basal and transient redundant sound, as well as greatly increased radio and mains-borne noise and interference, even with competent filtering.
David White
Llangefni
Gwynedd

## MAXWELL

The consistence of Ivor Catt's misrepresentation of Maxwell's laws is remarkable. Whatever deficiency they do contain, if any, it is certainly not at the elementary level claimed in the issue of November 1985. ('The Hidden Message in Maxwell's Equations').

The basic problem remains apparent ignorance of vectors and the role they play in Maxwellian theory. Ivor Catt seems to think that Maxwell's laws are some kind of elaborate hoax supported by an establishment conspiracy to suppress 'alternative' theories. He also believes that equations (9) and (10) in his latest diatribe represent the views of the conspirators. If they did, he would indeed have a point. But, sad to say, the windmills that this exuberant knight errant is tilting at are significantly different from the reality of Maxwell!

The mistake he makes is fundamental and disastrous. It is entirely necessary to modern em theory that the E field vector is perpendicular to the $H$ vector. Why, then, do equations (9) and (10) not show this? Without the direction property of a vector, em theory would fail to account for such simple phenomena as reflection. Ivor Catt attaches some mystical importance to $Z_{0}$; anyone who was properly conversant with EM theory would not. $Z_{0}$ is derived from the magnitude of the $E$ and $H$ vectors; their directional property is eliminated and most that is useful in the theory with it. $\mathrm{Z}_{0}$ is not a 'primitive': it lacks
directional information.
Ivor Catt's difficulties with the expression of physical concepts in mathematical form do not seem to be confined to electrical matters. True enough, if he walks along the plank far enough in the direction (hooray for direction!) ' $v$ ', ' $h$ ' does indeed decrease but so does ' $x$ '. Sorry, Ivor old son, but you are wrong again, as you walk along the plank it is because it is going backwards underneath you that it leads to that sinking feeling.
Dermod O'Reilly
Antwerp
Belgium


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# Compact disc mastering 

> John Watkinson explains away the confusion of p.c.m. adapters for use with video recorders, contrasting three different formats and detailing the more advanced codes of convolutional interleaving used in the smaller v.c.rs.

To cut a Compact Disc a digital recording must be made which contains exactly the same sample values as will appear on the disc. Unlike vinyl disc cutting, where the cutter operator has control over level, the Compact Disc cutter faithfully transfers every digit from the master tape. The disc mastering recorder is designed to produce that tape.
There are currently less than ten places in the world where Compact Discs are cut for duplication, so it is usually necessary to send the master tape to the disc plant. The robustness and convenience of a tape cassette are ideal for this journey.
The bandwidth of a digital stereo signal is about $2 \mathrm{Mb} / \mathrm{s}$, and some years ago the only devices able to record this bandwidth economically were video recorders. Digital data were encoded to resemble a tv waveform sufficiently well to fool an unmodified v.t.r. Originally, video recorders were open-reel devices, but once the U-matic cassette and its smaller relatives Betamax and VHS came into being they were soon adopted for digital audio recording. Digital mastering recorders for CD work today on the same principle.
A digital audio recorder which uses a video cassette recorder is depicted in Fig.1, in which the digital audio unit is often referred to as a p.c.m. adaptor. The unit has five main sections. Central to operation is sync and timing generation, which produces sync pulses for control of the video waveform generator and locking the video recorder, in

addition to producing sampling rate clocks and time code.
An analogue to digital converter allows a conventional analogue signal to be recorded, but this can be bypassed if a direct digital input is available. Similarly, a d-to-a converter is provided to monitor recordings and this too can be bypassed by the direct digital output. Also visible in Fig. 1 are encoder and decoder units that convert between digital data and the videolike signal known as pseudovideo or composite digital.
A typical line of pseudo video is shown in Fig.2. The line is divided into bit cells, and within them black level represents a binary zero and about $60 \%$ of peak white represents a binary one. The restriction to $60 \%$ is because most video cassette recorders use non-linear preemphasis misinterpreting the pseudo video. Clearly the bit rate must be an integer multiple
of line rate, and the sampling rate used will be derived from the frequencies in the tv standard. Thus the sampling rate of the disc was determined by video standards even though the disc itself has no video signal structure. The frequency of 44.1 kHz is derived as follows.

In the 525/60 monochrome tv standard there are about 245 useful (i.e. not blanked) lines in each field, giving a line rate of $245 \times 60=14,700$ lines per second. If three samples per channel (left and right) are stored in one video line the rate of $3 \times$ $14,700=44,100 \mathrm{~Hz}$ is obtained. This sampling rate may also be obtained on the $625 / 50$ tv standard by using 294 lines in each field, since $294 \times 50=14,700$.

Our Compact Disc series, introduced in the January 1985 issue, has so far featured:

- Principles of optical storage,

March \& April 1985

- Channel code and disc for-
mat, May \& June 1985
- Compact Disc players,

August \& November 1985.

Fig. 1. Block diagram of p.c.m. adaptor. Note the dub connection needed for producing a digital copy between two v.c.r.s.

Fig. 2. Typical video signal from p.c.m. adaptor. Data swings over only 0.3 volts to avoid activating pre-emphasis. Peak white pulse prevents a.l.c. increasing gain.



Fig. 3. Video line from PCM1610 has control bit that determines the use of pre-emphasis and selection of 44.1 or 44.0559 kHz (a). Note peak white ref. In video line from PCM-F1 in 16bit mode (b) and address at beginning of video line from JVC unit (c).

Fig. 4. In the PCM1610/1630 format, error correction is via an exclusive-or term computed from the two samples shown. c.r.c. character detects errors, parity term corrects. Redundancy is $100 \%$.

## Diversity of standards

Unfortunately the diversity of television standards has led to a complex situation for p.c.m. adaptors. The Compact Disc is a world wide standard, and it would be a desirable goal for mastering recorders to record also to a standard format.
The official CD mastering format is that produced by the Sony PCM1610, and this only exists in one version, which uses the $525 / 60$ monochrome standard because of its Japanese origin. Thus even in Europe, discs are mastered on 525/60 video recorders so that master
cassettes recorded in the USA or Japan can be cut in Europe and vice versa.
The first problem arises with the introduction of NTSC colour broadcasts. The field rate was reduced to 59.94 Hz to move harmonics of the new colour subcarrier away from the sound subcarrier inherited from the monochrome standard.
If a p.c.m. adaptor is slaved to an NTSC generator, the sampling rate falls to $44100 \times$ $59.94 / 60=44055.9 \mathrm{~Hz}$ and the timecode generator enters a mode called 'drop frame' whereby the timecode can continue to read real seconds and minutes even though there are no longer a whole number of fields in a second.
The CD sampling rate and timecode are irrevocably locked, ${ }^{2}$ and therefore a master tape with 44055.9 Hz sampling rate and drop-frame time code will be rejected by the disc cutting machine. Compact Disc and NTSC audio are incompatible. But digital sound tracks from PAL-synchronized broadcasts are compatible because the precise 50 Hz field rate of PAL can be locked to the 44100 Hz rate by a ratio of 882:1.
The position is further complicated by the existence of further standards. One of these is the EIAJ standard for consumer p.c.m. adaptors. These devices were originally intended for the top end of the hi-fi market place and enable a domestic v.c.r. to become a digital stereo


Fig. 5. In this one $35-l i n e$ interleave block of 1610/1630 format, block is divided into three sections of $11 \frac{2}{3}$ lines each, two data, one parity. Three passes through the interleave memory are needed to create the signal structure (1, 2, 3). Large $L / R$ interleave allows interpolation if dropout exceeds $11 \frac{2}{3}$ lines.
recorder. The consumer would, however, expect to be able to use the v.c.r. for regular tv recording as well. Thus the EIAJ format is in fact two incompatible formats: the first a sampling rate of 44055.9 Hz using the 525/59.94 NTSC timing, and the second 44.1 kHz sampling with $625 / 50$ timing. Both are intended for use with Betamax or VHS recorders.
The consumer division of Sony sold the EIAJ-format PCM-F1. Built with custom 1.s.i. chips made economic by volume sales, and with battery capability, it cost only a few hundred pounds. With a matching portable Betamax v.c.r., the


SL-F1, digital audio recordings could be made on location.
By contrast, the PCM1610 was intended for professional use, and relatively small volume production meant it was implemented with s.s.i. chips, which made it large and heavy and very expensive. Sales were somewhat damaged by the PCM-F1: a peculiar situation for Sony since they made both!
As a consumer product, the PCM-F1 was not ideally suited for Compact Disc mastering. There are no direct digital outputs, only an analogue output, and for this reason not too much trouble was taken with d.c. offsets in the converters. There is also an $11 \mu \mathrm{~s}$ timing error between channels, as a result of using single converters multiplexed between left and right.

These problems have been overcome in adaptor units supplied by independent companies such as RTW and Harmonia Mundi Acustica. 'They modify the PCM-F1 to give a direct digital output and use digital filters to remove offsets and timing errors, and then produce a direct digital output that is compatible with the 1610 and/or with the AES/EBU digital interconnect standard.

To add to the confusion, Sony then introduced the PCM701, a semi-professional version of the F 1 , which is rack mounting and non-portable. They then dropped the F1 which provoked such an outcry that they had to reintroduce it.
In addition to the 1610/Umatic and the F1/701/Betamax rivalry, there is a third contender from JVC for mastering , which uses industrial VHS transports. Some disc pressing plants accept the JVC cassettes.

## Formats contrasted

All three p.c.m. adaptors use the video waveform on a binary channel, with black representing zero and 50 or $60 \%$ of peak white representing 1 . However, consümer recorders with a.l.c. would increase the gain of such a signal, and so to prevent this the JVC system uses a peak white pulse once per field. The PCM-F1 uses a peak white pulse once per line. The PCM1610 is intended for use with semi-professional U-matic recorders which have no a.l.c. and has no peak white pulses.

Typical waveforms are shown in Fig.3.
All three systems use extensive interleaving to combat burst errors caused by tape dropouts. The PCM1610 has the most basic interleave/correction system which subdivides each field into seven blocks of 35 lines each, and interleaves within the blocks. The error correction method is a cross-word code. The PCM-F1 and the JVC system both use the convolutional interleave approach and more advanced codes.
The cross-word code of the PCM1610 is shown in Fig.4. Input samples 1 to 3 form a code word at (1) with a c.r.c. character. Samples 4 to 6 form a second code word at (c) with a c.r.c. character. The exclusiveor terms of the sample pairs shown form a third code word with a c.r.c.c. at (b). In the case of an error, the c.r.c. fails, but does not locate the error. All samples in the codeword are presumed faulty. For example 4,5 and 6 are declared faulty. Sample 4 is obtained from the exclusive-or of the first symbols in codewords (a) and (b) ( 10 $(1 O 4)=4)$, and so on. The system is not very efficient and the amount of redundancy is equal to the amount of data.

The interleave over a 35 -line period includes a left/right channel interleave (Fig.5). Dropouts up to $11 \frac{2}{3}$ lines long are fully correctable, since this magnitude will not destroy more than one of the three related code words. For example if line 0 is

corrupt, P1, P2 and P3 from the end of line 11 and L1, R2, L3 from the middle of line 23 are used to correct R1, L2 and R3, and so on. If the dropout continues up to $13 \frac{1}{3}$ lines, two code words of the related three will be destroyed and correction is impossible. Interpolation will then be used.

For example, if lines 0 to 12 are destroyed, L4, R5 and L6 will be uncorrectable (amongst others) but because of the interleave in line 23, L3 and L5 can be used to recreate L4, R4 and R6 can be used to recreate R5, and L5 and L7 can be used to recreate L6.

If the corruption is more severe, previous samples can be

Fig. 6. In 16 bit mode, 14 of the bits of each sample are stored as words (L, R) and the extra two bits of each sample stored as 12 bits of another word. Parity is generated on the 16 bit data, and 14 of the parity bits are stored in the P-word. Kemaining two bits are added to the 12 bits of sample data to complete the S -word.

Fig. 7. Interleave diagram of JVC format showing parity generated before and after an interleave to produce crossinterleaving.


Fig. 8. De-interleave and correction diagram for JVC format. Depending upon distribution of errors, it may be better to correct with either P1 first or P2 first: multiple re-interleave and deinterleave allows both choices. See text.
held to substitute current samples, but eventually the machine has to mute to prevent noise. In practice, dropouts are usually much smaller than $11 \frac{2}{3}$ lines, but the system has to interpolate if a random error occurs near a burst. The simple code of the PCM1610 relies on the relatively large trackwidth of the U-matic format to give good SNR. It is not suitable for VHS or Betamax video cassette recorders even if the a.l.c. is defeated.

## Convolutlonal interleave

Both the PCM-F1 and the JVC system use a much more sophisticated approach to allow the use of smaller-format v.c.rs. They use convolutional interleaving which spreads the effect of burst errors more evenly.
The PCM-F1 works in two modes. In 14 bit wordlength mode, the machine uses both Badjacent error correction and erasure (pointer) correction, and this is very powerful against random errors near to burst errors. In this mode the PCM-F1 conforms to the EIAJ standard for 14 bit consumer p.c.m. adaptors. However, in 16bit mode, which is necessary for mastering, the 14bit format is retained and the extra two bits in each of six samples and one parity word are stored in place of the 14bit B-adjacent redundancy. Thus
the power of the error correction system is reduced. The Badjacent decoding system will not be discussed further here as it does not apply to Compact Disc mastering. In 16 bit mode the PCM-F1 reverts to a system shown in Fig. 6.
Simple exclusive-or parity produces a P word from six samples. After interleave, a c.r.c. character is added to the end of each line. If the c.r.c. fails for a given line, all samples on the line are flagged bad. After de-interleave, this results in single errors with flags in many different P-code words, and correction is possible. However, the presence of a random error due to noise in the vicinity of a burst error due to dropout may cause two error flags in one Pcode word, which is uncorrectable. Interpolation will then be necessary.
The most advanced system is that of the JVC machine ${ }^{2}$, which uses cross interleaving. The cross-interleave is formed with simple parity only, and with c.r.c.c. after interleave to act as a pointer. In this respect the interleave resembles that of the DASH format ${ }^{3}$ more than the cross interleave of the Compact Disc, which uses Reed-Solomon redundancy without an additional c.r.c.c.. The arguments for cross-interleaving given in the June article ${ }^{4}$ on Compact Disc format still apply.
Fig. 7 shows the interleave continued on page 62

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# Synchrodyne a.m. receiver 

## 2 - Oscillator circuit, construction and commissioning

In the first part of this article, I discussed the design requirements for a high quality a.m. radio receiver, having good sensitivity, low demodulator distortion, freedom from whistles and with adjacent-channel selectivity which is user-adjustable.
One of the most satisfactory ways of achieving these design requirements is the use of a 'synchrodyne' (direct-conversion) receiver, of the form shown in Fig. 1, in which the incoming signal is heterodyned with a local oscillator held in frequency and phase synchronism with the incoming carrier. This allows direct recovery of the modulation imposed on that carrier, and renders adjacent-channel signals as higher-pitched audio tones - depending on the frequency separation between the wanted and unwanted carriers - which can be removed by appropriate post-demodulator audio filtering.
The essential feature of this kind of receiver system is the maintenance of a local oscillator in synchronism with the incoming carrier: this is achieved by a phase-locked loop consisting of phase sensitive detector 2 , the voltage-controlled oscillator (v.c.o.), and the $90^{\circ}$ phaseshifting arrangement, shown in the lower part of Fig. 1.
This p.1.1. function can be achieved economically, in a manner which is usable over a wide frequency range, by the use of high speed c.mos integrated circuits, as shown in Fig. 2. In this an oscillator, of which the output frequency is voltage controllable to some extent, for example by the use of a variable-capacitance diode in parallel with an LC tuned circuit, is fed to a divide-by-two stage, and thence to an exclu-


Fig. 1. Basics of directconversion process

Fig. 2. Phase-locked loop using practical devices
sive-or gate, whose logic (voltage/time) sequence is shown in ${ }^{\text {. }}$ Figs. 3 (a), (b) and (c).

This circuit arrangement generates two outputs, in quadrature, both of which are at half the frequency of the controlled oscillator. If one of these, say the output from the exclusive-or gate, is taken to one of the inputs of a suitable phase-sensitive detector, and this is used to provide an amplified and filtered control voltage to the voltage-controlled oscillator, then the other output from the circuit of Fig. 2, will, when the loop is in lock, be in accurate phase and frequency

(c) Exclusive OR output Q 090

(d) Fault condition which can arise due to uncompensated time delays $m \div 2$ stage


Fig. 4. Phase-locked local oscillator
synchronism with the incoming signal.
The circuit employed for the oscillator, and which uses a 74HC04 high speed c.mos hex. inverter, is shown in Fig. 4, and the quadrature-generating layout of divide-by-two stage and exclusive-or gate is shown in Fig. 5.
There is, unfortunately, an inherent snag in this type of
system, due to the unavoidable time delay introduced into the second input fed to the exclu-sive-or, as a result of propagation delay in the divide-bytwo stage (a 74 HC 74 dual flipflop). This can impair the simultaneity of the rising and falling edges of the waveforms of Fig. 3(a) and 3(b), and lead to the type of fault waveform shown in Fig. 3(d). Compensation for this small, unwanted, time delay is provided by the use of the small sequential propagation delays of the three unused inverter stages of the 74 HC 04 . This gives a clean quadrature output waveform, without unexpected glitches.

The use of the 74 HC 04 hex. inverter as an oscillator is very satisfactory from the point of frequency stability, and, although I have not sought to discover how high an output frequency is possible with this kind of circuit, it will certainly work at frequencies well above 10 MHz , which is more than adequate for present needs, where the required operating frequency range of 3.2 MHz 1100 kHz will give, following frequency division, a tuning range of $1.6 \mathrm{MHz}-550 \mathrm{kHz}$.

A point which should be
noted, as a possible pitfall for the unwary, into which I walked myself, is that the pin connections for the 74 HC 86 quad. exclusive-or are not the same as those for the $74 \mathrm{C} 86 / \mathrm{CD} 4070$. I have shown the required pin connections in Figs. 4 and 5.
There is a wide range of possible phase detectors usable in the phase-locked loop shown in Fig. 2. I have chosen the LM/MC1496P (14-pin, d.i.1.) double balanced modulator/demodulator for this purpose, because it is relatively inexpensive, widely available, and designed specifically for this type of application. There are some constraints in its use, particularly when employed as a synchronous demodulator for radio signals, which I will discuss later. However, in the p.1.1. application, its performance is quite trouble free.
I have shown the complete circuit of the phase locked oscillator, having a synchronous output in phase with the incoming signal, in Fig. 7. Since phase-opposed outputs are available from the 74 HC 74 , these have been used to generate push-pull drive signals to the 1496 demodulator, since symmetrical operation of this


Fig. 7. Complete phase-locked oscillator
i.c. helps preserve lock symmetry in the loop.
Considering this circuit in detail, the first inverting gate of $\mathrm{IC}_{1}$ is biassed into its linear region by $\mathrm{R}_{1}$, and positive feedback is applied via $\mathrm{C}_{3}$. 'Squegging' in the oscillator, which can happen with the ' HC ' series inverters in this circuit, though not with the lower speed c.mos, is prevented by the small resistor $\mathrm{R}_{2}$.

The operation of the LM/MC1496 can be explained with reference to the internal circuit diagram of the i.c. shown in Fig. 6. In this, a longtailed pair of transistors, $\mathrm{Tr}_{1}$ and $\mathrm{Tr}_{2}$, are fed from separate, high dynamic impedance, constant current sources $\mathrm{CC}_{1}$ and $\mathrm{CC}_{2}$. This allows the conversion gain, and internal balance to be controlled by the external resistor ' $\mathrm{R}_{\mathrm{x}}$ ' which will normally be very low in comparison with the source impedances, $\left(\mathrm{CC}_{1}\right.$ and $\mathrm{CC}_{2}$ ), but high in comparison with the dynamic emitter output impedances of $\mathrm{Tr}_{1}$ and $\mathrm{Tr}_{2}$.
Effectively, therefore, a signal applied to the E input will appear, because of long-tailed pair action, as two equal but opposite amplified current outputs at the collectors of $\mathrm{Tr}_{1}$ and $\mathrm{Tr}_{2}$, where it will be equally
divided by the matched transistor pairs, $\mathrm{Tr}_{3 / 4}$ and $\mathrm{Tr}_{5 / 6}$, before being recombined at the output pins 6 and 12 .

Because of the high degree of matching which is possible in transistors manufactured in i.cs, in the absence of any inputs to pins 8 and 10 , any signal applied at the $E$ input will be combined with an equal and opposite signal due to longtailed pair action of $\mathrm{Tr}_{1} / \mathrm{Tr}_{2}$, and will result in a null output at pins 6 or 12. Similarly, in the absence of any input to E or $\overline{\mathrm{E}}$, any signal applied to the oscillator inputs Q or $\overline{\mathrm{Q}}$ will be nulled at the output pins.

However, if signals are applied simultaneously to the signal and oscillator inputs, the output at pins 6 or 12 will be the sum and difference frequencies of these two, and in the particular case of applied signals which are in phase, the output will be a d.c. shift, superimposed on the frequency sum component.
The particular circuit layout required for the use of the 1496 is shown in Fig. 8(a), in the case of a single supply line operation, with the required d.c. input biassing obtained from a simple potential divider chain across the d.c. supply line.


| Range | Losc | L $_{\text {RF }}$ | Approx. pri. $/ \mathrm{sec}$ coupling ratio |
| :---: | :---: | :---: | :---: |
| MW <br> $(0.5$ to 1.65 MHz$)$ | $66 \mu \mathrm{H}$ | $266 \mu \mathrm{H}$ | $20 \mathrm{~T}: 100 \mathrm{~T}(20 \%)$ |
| $\frac{\mathrm{LW}}{}$ <br> 100 to 350 kHz | 1.5 mH | 5.9 mH | $80 \mathrm{~T}: 700 \mathrm{~T}(12 \%)$ |



Complete symmetry of operation, where this is desirable, can be obtained by small adjustment to the forward bias applied to $\mathrm{Tr}_{1}$ and $\mathrm{Tr}_{2}$, using the type of circuit shown in Fig. 8(b). This is unnecessary in the case of the p.l.l. circuit of Fig. 7, where the normal internal balance of the 1496 i.c. is quite adequate.

The output of $\mathrm{IC}_{5}$, in Fig. 7., is taken via a pair of unity-gain buffer stages, $\mathrm{IC}_{6 \mathrm{Ga} / \mathrm{b}}$, to a variable-gain amplifier stage, $\mathrm{IC}_{7}$, of which the h.f. response is rolled off by $\mathrm{C}_{13}$. A d.c. offset pot., $\mathrm{VR}_{2}$, is used to set the output of $\mathrm{IC}_{7}$, (TP6), initially, to half the supply line voltage $(+10 \mathrm{~V})$, with the gain control pot. $\mathrm{VR}_{3}$ approximately at the mid-point position.

Fig. 5. Quadrature waveforms generator

Fig. 6. Internal layout of LM/MC 1496 balanced modulator



Fig. 8. Use of MC
1496/1596 as double balanced demodulator, with single-supply operation is shown at (a). Method of nulling spurious responses is at (b).

The next article will deal with the receiver's
r.f. and demodulator stages

The potentiometer $\mathrm{VR}_{4}$ is used to set the proportion of the output control voltage applied to the $2-10 \mathrm{pF}$ Varicap diode, ( $\mathrm{VC}_{3}$ ), and initially this pot. can be set to maximum output. The particular type of diode employed, provided that it has a suitable capacitance range, is unlikely to be particularly important. I used BB105B units, simply because they were to hand.
The circuit, with the exception of the 'HC' c.mos i.cs, is not particularly critical in respect of the d.c. supply voltage, but it is suggested that a +20 volt line shold be used. However, since the high speed c.mos i.cs are very critical in respect of applied voltage, especially if a high degree of local oscillator stability is desired, the d.c. supply to these three i.cs is separately stabilized by a low-power voltage regulator i.c., $\mathrm{IC}_{4}(78 \mathrm{~L} 05)$.

## Commissioning the p.l.I.

Since the correct operation of the p.l.l. is crucial to the satisfactory performance of the receiver, it is suggested that, if a suitable oscilloscope and signal generator is available, the circuit should be tested, before the remainder of the circuit is put into operation, by tuning the oscillator into synchronism with an unmodul-
ated r.f. output from a signal generator, of some $2-20 \mathrm{mV}$ amplitude, injected into pin 4 of $\mathrm{IC}_{5}$ and small adjustments made to $\mathrm{VR}_{2}$ and $\mathrm{VR}_{3}$ until the best phase coincidence is obtained, on lock, between the signal input and the frequency divided oscillator output, as monitored at TP2.
In the absence of an oscilloscope, correct performance, while in lock, can be seen if a voltmeter is connected between TP6 and the 0V line, when a voltage excursion of $1-2$ volts, on either side of the mean output potential - depending on the signal generator output - should be observed as the signal generator, or oscillator tuning, is swung a few hundred Hertz on either side of the central lock frequency.
A modulated signal may then be applied and $V R_{1}$ adjusted to give the least audio output signal present at TP6. If an oscilloscope is not available, this adjustment could be made with a pair of high impedance headphones connected between TP4 and TP5. Similarly, small adjustments could be made to $\mathrm{VR}_{2}$ and $\mathrm{VR}_{3}$ using the same technique, since phase coincidence at TP2 implies phase quadrature (with minimum a.f. output) in the switching waveform applied to $\mathrm{IC}_{5}$.
As a final step, when the receiver is complete, and working satisfactorily, the values of $\mathrm{VR}_{2}$ and $\mathrm{VR}_{3}$ may be 'tweaked' to give the maximum signal strength indication on a signal, somewhere near the middle of the m.w. band, with the aerial sensitivity control adjusted to give about a half-scale reading, since the greatest value of the a.g.c. indication, other things being equal, will indicate the best phase coincidence at the MC1496 signal demodulator ( $\mathrm{IC}_{8}$ ).

Again, when the receiver is finally complete, the maximum output setting of $\mathrm{VR}_{4}$ may probably be determined by the need to avoid too great a difficulty in locking on to a strong signal at the top (low tuning capacitance) end of the m.w. band.

Hart Electronics, Ltd., of Penylan Mill, Oswestry, Shropshire, have offered to make available a kit of parts for the assembly of this receiver.

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As the number of tasks increases, it becomes more and more important for the user to understand how the system is handling the load. With this in mind, the workstation has built-in performance monitoring giving a graph-type display, as on the right of the picture, or an analogue meter display as shown in the top left.

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# Forth in control 

# The computer language Forth is particularly suited to the control of machinery, argues David Sands, who explains how it may be implemented in control applications. 

People tend to adopt languages and then defend them fervently. For example, Pascal enthusiasts expounds its virtues and ignore the drawbacks such as tedious de-bugging and editing. Basic, the single most popular language in the world, is not standardised, suffers from a multitude of dialects and is slow, unstructured and messy. A favourite target for scholars of better languages it nevertheless is arguably more efficient in terms of returns on programming effort, especially for shorter calculating programs.
The truth is, of course, that there are "horses for courses"; different languages are suited to different tasks. Forth is particularly suited to the control of machinery. It has some shortcomings, which I accept but which become less important once the full power of Forth is realised.

## What is Forth?

Without wishing to embark on a tutorial of Forth, I would just like to outline the fundamentals for the benefit of readers not acquainted with the languages. Note: In all my examples of exchanges between man and machines I will underline text typed in by the user. I won't keep mentioning the need for the return key. The computer's response will be in upper case but not underlined. My comments will be in lower case.
There are probably four fundamental principles.

## 1 - Command line

Commands numbers are typed in by the user, separated by spaces, finișhing with return.

Forth then scans the user's line acting on each word, and if everything works out OK then Forth types OK.

## 2 - the stack

All arguments are passed between procedures on a data stack. You can have variables, but they are not used much. Part of the reason for this is to maximise the performance of the system. Almost any language will first convert a formula to items on a stack. Because Forth users are interested in speed of execution they are prepared to keep account of the stack themselves. Suppose you wish to add 3 and 4 together and print the result:

$$
\geq 45+\text { (return) } 9 \text { OK }
$$

Forth scans the user's input line and first puts 4 on the stack, then puts 5 . The Forth word ' + ', then takes two values off the stack ( 5 and 4). adds them together and puts the answer on the stack, the value 9 . The Forth abbreviation ' ' then prints it. There is now nothing on the stack. If we try to print again we get:

## >. O STACK UNDERFLOW!

## which is not ok.

But the Forth data stack doesn't exist to make everyone think like a machine. At worst post-fix notation is an unfortunate sideeffect. Imagine that we wish to calculate the total content of two tanks of chemical. Each tank has a transducer in it with quite a complicated service routine, as follows:

1 Select transducer and energise.
2 Allows filters to settle.
3 Command the analogue-
to-digital converter

4 Wait for the ADC to complete.
5 Read the ADC.
6 Scale the result according to the calibration factor of the transducer.
7 Leave the scales result on the stack.
Each tank has it's own service routine, called LEFT-TANK and RIGHT-TANK. The total of both tanks is given by:-
LEFT-TANK RIGHT-TANK +
Now LEFT-TANK and RIGHT-TANK are not values! Nor variables. We are not doing PRINT X + Y. They are whole procedures which leave their results on the stack. There can even be other words between LEFT-TANK and RIGHT. TANK as long as they don't take off or put on extra items on the stack for example:

LEFT-TANK BLA-BLA RHUBARB RIGHT-TANK +

3 - the dictionary.
Instead of a handful of keywords as in Basic, there are about 150 or more words, which are organised in a "dictionary". Forth interprets a user's word by searching down the dictionary until it finds it, then carries out the activity which is in the "definition" of the word. If the word isn't in the dictionary then Forth tries to convert it as a number. If it isn't a valid number either, then Forth rejects it as an error. Most low level words in Forth tend to be abbreviations, or single characters, for example the Forth word for "print" is just a full-stop (.) whereas higher level procedures have highly descriptive names.

## 4-definitions.

This principle is fundamental to Forth users. It is the building-


David Sands is a consultant in industrial automation and software, with a small company, Sands Technology, in Cambridge. In 1979 he was one of the first to import personal computers from the USA. In the same year he designed a low-cost speech synthesizer for personal computers. Two years later he designed a talking dashboard for a car. He has also worked on naturallanguage translation using speech input and output, and on low-cost robot arms.


The Forth word " + " takes the two top numbers from the stack and replaces them with their sum.

## Summary

Forth is a highly productive language in terms of programming effort. Communication between programmer and machine is improved by the development of a vocabulary specific to the application. Programs produced with Forth have higher integrity and are more efficient than programs produced with other methods. Data types are few but highly suited to digital hardware. The use of the stack is an efficient way of passing arguments. In fact there are now single chip microcomputers available with Forth built in, such as the 65RF11. New microprocessors are being developed with stack oriented archi-tecture.

The heart of a statistical process control circuit which can be controlled by Forth, as described in the text.
block approach to programming.
Forth, straight off the disk, consists of a "kernel" of some 150 or more "words" or commands, most of which execute machine code whenever they are used. The programmer must define new words in terms of words in terms of words he/she has already define plus words from the kernel as necessary. These new words are added to the existing dictionary. Hence the programmer begins by defining short concise procedures which can be tested individually. In this way the programmer builds up a range of fully tested modules which are then used to construct more powerful procedures, and so on until the final application programme is complete, which can be just one word. The modular approach imparts a very high degree of confidence to the final application.

New procedures are created
using a colon sign, followed by the name of the procedure, then the definition ending with a semi-colon:

## : TANKS? <br> LEFT-TANK RIGHT-TANK $+$

Now all you have to do is type TANKS? to yield the total in both tanks, or alternatively TANKS? can be included in the definition of some grander procedure.

## Control applications

To illustrate the above principles more fully I can outline part of a genuine application. The system being programmed is a dedicated computer which reads from linear displacement transducers checking tolerances on motor components. Deviations from tolerance are displayed on a colour screen in bar graph form and are later analysed statis-

tically for trends, machine performance etc. This is known as Statistical Process Control or 'SPC'.
A number of transducers are connected to a multiplexer and analog-to-digital converter. The ADC is an Analog Devices AD574 used in 12 -bit mode on an 8 -bit microprocessor bus (actually a Z80), on I/O ports O and 1 . The read/convert input of the $A D C$ is driven from bit 0 of port 4. Now, suppose we are not just starting on the software but that the hardware is not proven either, being a bread-board prototype.

## Hardware development

Assuming that sufficient of the system is running to support Forth, or that a processor emulator is being used which is running Forth, then things can be typed in at the keyboard during debugging of the hardware. Checking of a prototype module or circuit addition might proceed as follows:

$$
>04 \text { OUT OK }
$$

This sends the value $O$ out through port 4 to set the ADC to convert mode. (check with logic probe).

## $>4$ OUT OK

This sets the ADC back to read mode. (check with logic probe) Suppose there are problems with the wiring. We can therefore define a word to keep writing to port 4 while we look for the missing signal with an oscilloscope. You can't do this with an ordinary monitor program. You can't do it nearly as quickly by writing a test routine in any other language. Bear in mind that you might need to devise many test routines during the development of some hardware. To check the above read/convert line you might enter:

$$
\begin{aligned}
& >: \text { TEST1 } 10000 \text { DO } 04 \text { OUT } 1 \\
& \frac{4 \text { OUT LOOP; OK }}{>\text { TEST } 1}
\end{aligned}
$$

Luckily Forth is fast enough to issue the OUT signals with sufficient regularity to be visible on an oscilloscope. If Basic were used you might be trying to view a 10 microsecond trace generated every 10 milliseconds by BASIC. This would dim the
trace by a factor of 1000 making it invisible. Forth is therefore a powerful engineer's tool.

## Hardware service modules

Hardware devices are best programmed in stages or modules. In the case of my example of the Analog Devices AD574 Analog-to-Digital converter first let's get control of the read/convert line:-
(Note in practice, programs are entered on to disk, and edited, before being compiled by Forth).

## : CONVERT

14 OUT (SET CONVERT
MODE)
00 OUT (START
CONVERSION)

When the ADC has converted a value, the 12 -bit result is available in two parts: the upper 8 bits on port address 0 and the lower 4 bits with trailing zeros on port address 1 . In my application I wired ADC data bits 0 to 3 to my bus on bits 4-7, and ADC bits $4-7$ to bus bits $0-3$. The code to read the ADC was therefore as follows. Note that hexadecimal numbering is preferred in the context of hardware:-

```
READ
04 OUT (SET READ MODE)
0 IN (GET HIGH BYTE)
OF AND (MASK LH NIBBLE
WHICH IS THE MOST
SIGNIFICANT 4 BITS)
100 * (SHIFT LEFT TO BITS
8-11)
O IN (GET HIGH BYTE
AGAIN)
FO AND (MASK RH NIBBLE
WHICH IS BITS 4-7)
OR (LOGICAL OR WITH BITS
8-11)
1 IN (GET LOW BYTE WHICH
IS BITS 0-3 PLUS 4 ZEROS)
OR (LOGICAL OR WITH BITS
4-11)
7FF - (APPLY OFFSET SO
READINGS FALL
BETWEEN +2048& - 2047)
```

The ADC is fed from a TESA signal conditioner which converts the transducer outputs into a DC voltage in the range $+\&-10$ volts. The amplifier in the signal conditioner has a choice of two gains, which I select by outputting on bit 1 of port 4, bit 0 of which is already in use. It is necessary, therefore to add, the value of this bit to the output whenever selecting read or convert modes of the ADC.

To do this we need a variable to hold a value of 0 or 2 . When the variable's name is used its address is put into the stack. The Forth word '!' stores a value into the address, i.e. into the variable. The Forth word @ fetches a value from the variable and leaves it on the stack.

## VARIABLE SCALE

The rest of the code is then modified so:
:CONVERT
SCALE @ 4 OUT (SET
CONVERT)
00 OUT (START
CONVERSION)
: READ
SCALE @ 1 OR 4 OUT (SET
READ)
0 IN OF AND 100 *
0 IN FO AND OR
1 IN OR
7FF -

Finally, before using the ADC I must set up the multiplexer in the signal conditioner by outpouring the required channel on port 2. e.g. 22 OUT selects channel 2.
If the amplifier needs a settling time the signal conditioner issues a busy signal which I input on port 6 bit 0 . Servicing the signal conditioner is coded like this:

> : CHAN
> 2 OUT
> BEGIN
> 6 IN 1 AND
> $0=$ UNTLL

The BEGIN-UNTIL loop traps UNTIL bit 0 of port 6 changes to 0 (false). Now I can build a 'bigger' word thus:-

```
: ADC
CHAN
CONVERT
READ
```

Note that the line: 2 OUT is not complete. It requires a further item from the stack and this is presumed to be on the stack before ADC is invoked. To select and read channel 2 we would therefore write

## 2 ADC

ADC contains the word READ which leaves the value of channel 2 on the stack. ADC is therefore a word which requires one value on the stack and leaves one value behind on the stack. To demonstrate the
usefulness of this we could have a condition whereby a value of, say, more than 800 on channel 4 is an alarm condition.
Suppose the diameter of a certain component were being checked by two transducers mounted each side of the component. The two transducers are required so that if the shaft were not straight then any reading produced by one transducer due to nonstraightness would cancel in the other. Suppose the transducers are on channel 5 and 6 . Then we could define a single word for diameter to read both transducers and add them together thus:

## : DIAMETER 5 ADC 6 ADC + ;

From now on whenever we want diameter we need only use the name; e.g.:

$$
>\text { DIAMETER . } 500 \text { OK }
$$

An associated word might be:-

## : TOOLARGE

```
800 >
```

This leaves a 1 (true) on the stack if the argument is more than 800 units, or a 0 (false) if not. In a later definition yhou might enter

DIAMETER TOOLARGE IF ABORT THEN.
What is now happening is that Forth statements are taking on the readability of an English sentence and becoming less cryptic. At the same time we are beginning to forget the complexities of the lower levels. We can afford to! They are fully tested and reliable.

## Machine control

Out-put to a machine is most commonly achieved with the following devices:
Triacs - used to switch contactors and solenoids e.g. solenoid valves.
Digital-to-analog converters used to issue a varying voltage to control such things as DC motors.
Transistors (e.g. hexfets) used to switch low voltage DC devices such as stepping motors and bright lamps on the machine front.
In an application a few years ago I designed and programmed a dedicated system to check the performance of hydraulic control valves as fitted to cars with power assisted steering.

The machine had a hydraulic pump from which oil was fed to the steering valve via solenoid valves controlled by my system. One problem with output ports is that although they latch (i.e. memorise) what you send to them, their contents cannot be read back. They are therefore a kind of write-only memory (wom?). If you wish to change the state of one bit on a particular port without altering any of the other bits then ideally you read the port, after a bit, then write it back. Because you can't do this it is necessary to keep account of each port in a variable. My application used an 8 -bit microprocessor, a Z-80. I had port 7 controlling 8 triacs, ports 8 and 9 controlling 16 DC lamps. The triacs were programmed thus:

## VARIABLE TRIACS

:ACOUT
DUP TRIACS!
7 OUT

Any argument to ACOUT is first DUPlicated. One copy is stored in the variable TRIACS and the other is output on port 7 . Various descriptive commands can now be defined:
: OILON
TRIACS @ 1OR (SET
BIT 0 TO 1)
ACOUT (OUTPUT
AND SAVE IN
TRIACS AGAIN)
;
: OILOFF
TRIACS @ FE AND
(SET BIT 0 TO 0
MASKING IT
OUT)
ACOUT
: CLAMPON
TRIACS@4 OR
ACOUT
: CLAMPOFF
TRIACS@FB AND
ACOUT
: AIRON
TRIACS @ OR ACOUT
: AIROFF
TRIACS @ F7 AND
ACOUT
etc. etc.
The DC outputs on parts 8 and 9 can be handled 16 bits at a time to suit Forth's 16 bit standard data size. Simply split the 16 -bit value into high and low bytes and output separately on each port.

## Compact disc mastering <br> continued from page 50

Fig. 9. The DMR4000 has extra rotary heads for confidence replay. If an additional decoder is installed in PCM1630, the machine can continue to play with a clogged head. Error status will switch output to the error-free decoder, whether playback or confidence head. Delay compensates for displacement heads.

The PCM-F1 has no timecode functions and for Compact Disc cutting F1/701 tapes have to be digitally dubbed to PCM1610 format using the RTW or Harmonia Mundi Acustica interfaces.
The JVC system buries the timecode and user bits in the pseudo-video waveform, so the poor analogue bandwidth of VHS audio tracks ceases to be a problem. An adaptor is available to produce timecode from the JVC p.c.m. adaptor.

Two of the greatest drawbacks of the use of v.c.rs for digital audio have been the lack of confidence replay, i.e. offtape monitoring during record, and the tendency of heads to clog due to a combination of inaccessibility and repeated passes during edit operations.
In the replacement for the venerable PCM1610 and VO5850 U-matic system, Sony have solved both problems. The U-matic recorder is no longer an industrial v.c.r. with the chroma

circuits and dropout compensator disabled, but a purposebuilt machine with extra replay heads in the drum for confidence replay, and an automatic head-cleaning mechanism (DMR4000). The PCM1630 generates the same tape format as the PCM1610, but can switch the replay section to the confidence output of the DMR4000. As an option a second replay channel can be fitted to the PCM1630 as shown in Fig.9.
During replay, the record/ playback heads drive one replay channel, and the confidence heads drive the second channel. Should one head become clogged, error detection circuits will choose data from the other heads. Significantly, the d.-to-a. converter of the 1630 uses oversampling by a factor of two to improve phase linearity.

In the next two parts of the series we discuss problems and techniques in editing digital recordings on rotary head machines.

## References

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4. Channel code and disc format, J.R. Watkinson, Electronics \& Wireless World, June 1985, pp.80-2.

## HDTV Camera

A television camera, which sets new standards in picture recording quality, has been developed by Robert Bosch GmbH , on behalf of the Heinrich Hertz Institute for Telecommunications Technology in Berlin. The development work was sponsored by the Federal Ministry for Research and Technology. To date five of the experimental cameras have been delivered, namely to the Heinrich Hertz Institute, the University of Dortmund, Braunschweig Technical University, the
Telecommunications Research 62
and Development Centre of the German PTT in Darmstadt. HDTV (high definition television) is a new television standard which aims to achieve even better picture resolution, that is, even clearer television pictures, on larger screens with a width/height ration of $5: 3$ (previously $4: 3$ ). When this improvement in quality will reach domestic television screens, however, remains to be seen, as it would require not only further development of all the equipment required in the television studio but also the allocation of new frequencies for transmission of the programmes, by satellite for example.
Nevertheless, the new technology could soon find its way into production studios

because HDTV productions unlike those from other systems - can be used in a "multimedial" way, which means that as well as being broadcast they can also be
transferred to video discs or 35 mm film. HDTV technology would therefore enable production studios and television stations to become considerably more competitive.

# Timing by remote control 

# This versatile self-contained Z80 timer controls eight appliances with 100 on-off settings using coded r.f. bursts injected in the mains supply. 

TThis project was originally conceived as a simple electronic replacement for an electromechanical immersion-heater timer, which had finally siezed after years of unreliable service. Then I decided that, to be really useful, the timer should be capable of controlling more than just an immersion heater; it should have a timing resolution of one minute; it should be able to store several different switching times for each appliance; and above all it should be self-contained (some advertised controllers need to be hooked up to a home computer).

It was clear to me that a microprocessor was the only economical way of achieving these requirements. I first considered using a single-chip microcomputer, to cut down construction time. One such device, Texas TMS1601A, is mask-programmed to operate as a four-channel timer, but unfortunately it doesn't lend itself easily to remote control with the operating program supplied. Also, it only provides a four-digit display (I wanted to display on and off times together) and can only control four appliances.
Single-chip microcomputers containing eprom, such as Intel's 8748 series, are still more expensive than multi-chip systems, and difficult for home constructors to find. I therefore settled for a general-purpose microprocessor with external memory, since eight-bit processors are widely available at very low prices. Standard eproms are also cheap and they can easily be programmed using a home computer with a suitable attachment.

Having to write the software myself gave me the chance to
define the operating procedure to suit my own whims. The software will be described in sufficient detail for changes to be made by constructors with different ideas of how a timer should operate.

The final design is based on a Z80 processor and has several features not usually found in commercially made timers.

- One appliance is plugged into a 13A mains socket mounted on the control unit. A further seven may be remotely controlled by means of coded r.f. bursts injected into the mains wiring ${ }^{1}$.
- Up to 100 on-and-off settings may be stored. Each
setting can control any combination of appliances, and will operate on any combination of days of the week. It may either repeat the weekly cycle indefinitely, or stop automatically on any specified last day.
- Settings are suspended rather than cancelled on the last day, and may be reactivated without being reentered from scratch. They may also be suspended or cancelled manually at any time.
- All the stored settings, or just those for a particular channel or a particular day, or all repeated settings, may be examined and altered in


## by Peter Ferris



The author developed an early interest in electronics, building his first radio at the age of 12 and going on to maintain all the school's many television sets. Having dropped out of a B.Sc. course at London University, he worked his way up through industry, testing, fault-finding and then designing analogue control systems and test equipment. He taught himself about
microprocessors the hard way, be designing and building a $Z 80$ development system from scratch, and is now employed as a senior design engineer with Dowty Electronics, where he is working on $\mathbf{Z 8 0 0 0}$-based contro systems.

turn. The display in this mode shows on and off times, day, channel and either active or suspended. For non-repeated settings the last day flashes.

- Settings are entered and altered step by step, with the relevant part of the display flashing at each stage as a prompt. A 'backstep' key allows mistakes to be corrected without having to start again.
- Individual digits of the on and off times are altered with 'up' and 'down' keys. The numbers wrap-round when zero or the upper limit is reached; impossible times such as 27 hours cannot be entered.
- Each channel has an output on/off key and a timer enable/disable key, with leds to indicate status.
- Like most digital watches but unlike most timers, the clock may be corrected in two steps if it is within half a minute of the right time.
Most of these features are provided by the software and incur no additional cost. Those that need extra hardware, such as the remote control, could simply be left out if not required.
The control unit is constructed on three printed-circuit boards: the first contains the processor and memory and most of the logic; the second holds the keyswitches, displays and display drivers; and the third is shared by the optically coupled triac switch, the power supply and the remote-control transmitter.


## Processor board

The circuit of the processor board is shown opposite. Circuit $\mathrm{IC}_{2 \mathrm{a}}$ decodes the upper two address lines to divide the processor memory map into four parts, of which two are used for the eprom and ram. The eprom may be either a 2716 (2Kbyte) or a $2732 / 2732 \mathrm{~A}$ (4Kbyte). The timer program fits into 2 Kbyte , but as the processor spends much of its time in the halt state, it could be given additional tasks such as a program for decoding the Rugby time-code radio transmissions. ${ }^{2,3}$.

Circuit $\mathrm{IC}_{7}$, a standard Z 80 peripheral device, is a fourchannel programmable coun-
ter/timer circuit (c.t.c.). Channel 0 divides the system clock down to 500 Hz , which is further divided by channel 2 to provide a 20 Hz interrupt for the timekeeping function and the display flasher. Channel 1 generates a 601 Hz interrupt for display multiplexing; it is also used as a clock for shift register $\mathrm{IC}_{13}$. Channel 3 is spare. CPU address line $\mathrm{A}_{2}$ is used directly as a chip enable for the c.t.c, which therefore occupies every address in the i/o map which has $\mathrm{A}_{2}$ zero.
Circuitry $\mathrm{IC}_{5}, \quad \mathrm{IC}_{8 \mathrm{a}, \mathrm{b}}, \mathrm{IC}_{2 \mathrm{~b}}$ decode addresses for the other four i/o ports. The decoder is inhibited when $A_{2}$ is low to avoid bus contention with the c.t.c. Lines $A_{3}$ and $A_{4}$ were arbitrarily chosen for the select inputs. Signal $\overline{I O R Q}$ is used as a data strobe in both directions; it is not necessary to use $\overline{\mathrm{RD}}$ or $\overline{\mathrm{WR}}$, because the software will never try to write to the input port ( $\mathrm{IC}_{6}$ ) or read from the output ports (IC10, 11 and 13). However, signal $M$, is gated through $\mathrm{IC}_{8 \mathrm{a}}$ to inhibit the decoder during the interrupt acknowledge cycles, when $\overline{\mathrm{M}}$, and $\overline{\mathrm{IORQ}}$ are both low and the address bus retains the program counter contents.
The key matrix is driven by $\mathrm{IC}_{5 c \text {.f }}$, their open-collector outputs avoiding the possibility of damage if keys in different rows are pressed together.

The parallel-to-serial data converter is $\mathrm{IC}_{13}$, clocked continuously at 601 Hz , but as the serial input on pin 10 is tied low the output is normally a stream of zeros. When the processor is required to switch an appliance on or off, it writes a byte into the parallel inputs. Each bit from $D_{1}$ to $D_{7}$ represents the required state of one of the remotely-controlled appliances ( 1 for on, 0 for off). The $H$ input of $\mathrm{IC}_{13}$ is tied high to provide a start bit, so $D_{0}$ is latched by $\mathrm{IC}_{12 \mathrm{~b}}$ to control the eighth (or zeroth) appliance directly. The write strobe pulse also triggers the monostable $\mathrm{IC}_{9 \mathrm{~b}}$, which enables the transmitter for the time required to transmit one byte.
The other half of $\mathrm{IC}_{9}$ is used as a pulse-width modulator to control the display brightness. It is retriggered at 1.66 ms intervals when the multiplexing software moves on from one digit to the next. With the control at maximum the pulse is
slightly shorter than the trigger interval. The $\bar{Q}$ output is therefore low, and the display enabled, for most of the time. As the control resistance is reduced the pulse becomes shorter, reducing the display duty cycle and hence the apparent brightness. To match the response of the eye, a logarithmic potentiometer is used with the wiper tied to the clockwise end
This arrangement also protects the display leds if a fault occurs which stops the display being multiplexed. Under fault conditions, $\mathrm{IC}_{9 \mathrm{a}}$ is no longer triggered. Its $Q$ output stays high, disabling both the segment driver $\left(\mathrm{IC}_{11}\right)$ and the digit decoder on the display board. Without this protection, the 60 mA segment current would flow continuously in one digit or group of leds, instead of being time-shared between the eight digits and four groups of leds.
Oscillator frequency is halved by $\mathrm{IC}_{12 \mathrm{a}}$ to provide a 1 MHz clock for the c.p.u. and c.t.c. The normal t.t.l. high level is insufficient for the c.p.u. So $\mathrm{R}_{5}$ pulls the logic 1 level up to +5 V . The halt indicator and $\mathrm{R}_{1}$ are optional. If fitted, the led appears to glow dimly most of the time (it actually flashes at a rate too fast to see), but it visibly blinks off when the clock minute increments, and sometimes when a key is pressed.

## Dlsplay and keyboard

The circuit of the display/keyboard is on page 66. External connections are numbered to correspond with the processor board circuit.
Integrated circuits 101 and 102 decode the four-bit digit number and drive one digit or group of leds at a time, via transistors 101 to 112 . The choice of transistor used is important; a d.c. gain of at least 100 is required at a collector current of 500 mA . Power disipation is low because each transistor is only conducting for one twelfth of the time.
Transistors 113 to 120 each drive one segment or discrete led of the digit or group of leds selected by the digit decoder. Resistors 125 to 132 set the current to about 60 mA peak ( 5 mA average), which gives an accep-
tably bright display without resorting to Darlington drivers, especially if high-efficiency leds are used. Although the colon between the hour and minute digits is always on, its leds are pulsed via $\operatorname{Tr}_{101}$ so that the colon brightness tracks the rest of the display.
The 32 keystrokes are connected as a four by eight matrix, which is scanned by pulling each row line low in turn, and then reading the eight column lines together. Column lines with no keys pressed are pulled high by resistors on the processor board. Debouncing the keys is left to the software (to be described later).

## Power supply

The power supply is of conventional design (shown on p. 67 with the optocoupled switch and remote-control transmitter). The five volt regulator, $\mathrm{IC}_{203}$, should be firmly bolted to the metal box for heatsinking. It should not be insulated from the box because the 0 V line, which is connected to the metal surface of the i.c., needs to be earthed as a return path for the transmitted r.f. signal. The 7805 is available either in a TO3 metal can, or in a TO220 plastic package with a metal tab. Either type is suitable.
A voltage doubler generates a raw 20 V supply for the transmitter output stage. From this, $\mathrm{IC}_{202}$ derives a stable 12 V rail for the oscillator and driver stage.

The mains filter unit is optional, and various types may be suitable depending on the environment. The prototype timer operated correctly for several weeks without a filter, but then consistently went haywire when an electric drill was plugged into the other half of the double power point where the timer was plugged in. (The timer behaved itself when the drill was moved to the next power point on the ring main.) Fitting a filter as shown in the circuit completely cured the problem.
The fuse in the mains plug has to be rated according to the largest appliance likely to be plugged into the control unit (i.e. probably a 13 A fuse), and this would not protect the mains transformer if, for example, $\mathrm{D}_{204}$ or $\mathrm{D}_{205}$ went shortcircuit. The separate low-


current fuse (F1) is therefore essential, particularly because the unit will be left on and unattended for long periods. A slow-burning fuse is required, to cater for the relatively high surge current at power-up.

## Optocoupled switch

An optically-coupled triac driver, $\mathrm{IC}_{204}$, also contains a zero-voltage-crossing circuit. The output stage is itself a small triac and for loads of less than 20 watts, such as a portable radio, the external triac and $\mathrm{R}_{221}$ may be omitted. (Connect pins 6 and 4 of $\mathrm{IC}_{304}$ directly to the live input and output lines respectively).
Remember that high-current triacs can have significant off-state leakage currents, especially when hot; a 5 watt load connected to a 15 A triac may still have several tens of
volts across it when the triac is off. Ideally, the triac's r.m.s. current rating should be about $50 \%$ higher than the maximum load current, but in practice it is possible to use, say, 15A triacs for most receivers, with one or two lower-current ones for appliances such as radios or electric blankets.
Snubber components $\mathrm{C}_{211}$ and $\mathrm{R}_{220}$ are included to limit the rate of rise of voltage across the triac when an inductive load is switched off, which could otherwise retrigger the triac as soon as it is switched off. Their optimum values depend on the maximum load current and the critical dV/dT rating of the particular triac used, though 1 $\mathrm{k} \Omega$ and $47 \mathrm{nF} / 500 \mathrm{~V}$ is a widelyused combination. They may be omitted if only resistive loads are to be controlled, or if the phase difference between voltage and current is only a few degrees.

## Remote conirol transmilter

The principles involved in using domestic mains wiring to carry data signals are discussed in reference 1 , so I will not go into too much detail here. The neutral-earth pair of wires is used for safety.
Frequency-shift keying is used for data transmission, i.e. two carrier frequencies represent logic 0 and logic 1. On page $67, \mathrm{IC}_{201}$ is a voltage-controlled oscillator whose frequency is switched by the serial data. The triangular waveform from pin 4 is filtered by $\mathrm{R}_{205}$ and $\mathrm{C}_{203}$, so that the power amplifier delivers a reasonably pure sinewave to the mains wiring. Transistors 203 and 204 keep the output stage biased off except during transmissions.
The choice of carrier frequencies depends on the impedance/frequency characteristic of the mains wiring, which
varies considerably from house to house. Measurements made at several locations suggest that an impedance peak can be expected somewhere between 100 and 500 kHz ; a simple method of finding the peak will be described later, with other tips on testing and setting up the system.

## Remate control recelver

A typical f.s.k. receiver might consist of: a bandpass filter with -3 dB points at the two carrier frequencies; a phaselocked loop to recover the original serial data; a serial-toparallel converter (usually a uart chip which can detect transmission errors); and a decoder, to determine whether the received command is intended for this receiver, and if so whether to switch the appliance on or off. If two or


more appliances are to be switched together, a separate data word must be transmitted for each one.
Since a receiver is required for each remotely-controlled appliance, I rejected this approach on the grounds of cost. Instead, I designed a novel receiver circuit which offers good immunity from mains-borne interference at a modest outlay.

The circuit is shown opposite. A Wien-bridge bandpass filter, $\mathrm{IC}_{3111}$, is tuned to the lower (off) carrier frequency.
The comparator $\mathrm{IC}_{3013 \text { a }}$ serves three purposes. First, the base/collector junction of the inverting input transistor acts as a clamp diode, holding the negative peaks of the waveform to about -0.6 V . Secondly, the positive peaks of the shifted waveform are compared with the half-supply-voltage bias on the other input; if the peak-topeak amplitude exceeds the bias, the comparator output switches low. Thirdly, the open-collector output stage acts as a rectifier; $\mathrm{C}_{307}$ is charged rapidly by the output transistor, but discharges more slowly through $\mathrm{R}_{308}$.

The output therefore remains low, although with some ripple, when a large enough signal is received. The filter $\mathrm{R}_{309}$ and $\mathrm{C}_{308}$ is to remove short pulses caused by spikes on the mains wiring.
The higher (on) carrier frequency is detected in the same way by $\mathrm{IC}_{302}$ and $\mathrm{IC}_{303 \mathrm{~b}}$. The other two comparators in $\mathrm{IC}_{303}$ are not used. (If you're wondering why I didn't use the LM393 dual comparator, which has nearly identical characteristics, check the advertised prices the LM339 quad version is usually cheaper.)
The normal operation of the rest of the circuit is best understood by referring to the waveforms, above. The serial data word always starts with an onbit. The next seven each represent the required state of one of the remotely-controlled appliances. The stop bit is always an 'off'.
The start bit triggers monostable $\mathrm{IC}_{305 \mathrm{a}}$, via $\mathrm{IC}_{304 \mathrm{~b}, \mathrm{c}}$. The Q output of $\mathrm{IC}_{305 \mathrm{a}}$ immediately triggers the second monostable, $\mathrm{IC}_{305 \mathrm{~b}}$ the Q output of which is fed back to prevent retriggering of either monostable during the receive sequence.

The first monostable is adjusted so that its pulse finishes in the middle of the data bit corresponding with the particular receiver (channel 6 in the case of Fig.5). This trailing edge latches the incoming data bit into $\mathrm{IC}_{307 \mathrm{7}}$, from where it is transferred to $\mathrm{IC}_{307 \mathrm{~b}}$ by the trailing edge of the second monostable pulse during the stop bit.
Extra gating circuits are included to provide noise immunity. To trigger the monostables, a burst of mains-borne noise has to be at or very near the on-frequency for a long enough time to discharge $\mathrm{C}_{316}$ below the logic 0 threshold. It must have no significant component at the off-frequency, since that would block the onsignal at $\mathrm{IC}_{304 c}$. At the end of the first monostable pulse, the noise must still be present, and at only one of the carrier frequencies; if neither or both are present, the $J$ and $K$ inputs of $\mathrm{IC}_{307 \mathrm{a}}$ would both be low, and the latch would not change state. At the end of the second monostable pulse the noise must still be there, but now only at the 'off' frequency; otherwise, the $J$ and $K$ inputs of $\mathrm{IC}_{307 \mathrm{~b}}$ would be held low via $\mathrm{IC}_{304 \mathrm{~d}}$ and $\mathrm{IC}_{306 \mathrm{c}, \mathrm{d}}$, and the output wouldn't switch. Even if a noise burst managed to get over those three hurdles, there is of course a $50 \%$ chance that it would only succeed in switching the output to the state it was in already.
As with the conventional receiver, the output may fail to switch if noise occurs during a signal transmission. To overcome that problem, the control unit repeats each timed transmission, ten seconds after the stored switching time.

## Local control

The three-position switch allows the appliance to be switched on and off locally, overriding the remote control. This is not strictly necessary when the appliance is to be powered via a mains socket mounted on the receiver box, as the appliance could be plugged directly into a wall socket or left unplugged. But some appliances, such as an immersion heater or a bathroom heater, must be wired directly into the receiver because power sockets aren't allowed in bath-

rooms. The switch is then the only means of local control (or any control if the transmitter fails). A switch is used rather than a pair of push-buttons because it has the advantage of providing absolute immunity from mains-borne interference - including from mischievous members of the household trying to switch the bathroom heater off when you've just settled down for a long soak! Capacitors $\mathrm{C}_{319}$ and $\mathrm{C}_{320}$ prevent noise picked up on the switch wires reaching the SET and CLR inputs to the latch. They are connected to opposite supplies to ensure that if a power cut occurs while the switch is set to 'remote', the appliance is switched off when power is restored.

The d.c. supply for the receiver is derived from a miniature mains transformer. The receiver circuit is tolerant of quite wide variations in supply voltage, and no regulator is necessary. Load current is about 17 mA for the receiver itself, plus a further 15 mA through the optocoupler and panel leds when the output is switched on.

## To be continued

Postscript. I have been asked several times why the multiplexing interrupt rate is 601 Hz rather than a round figure like 600 Hz . The reason is that the c.t.c. channel has a four-bit prescaler, which divides the 1 MHz c.p.u. clock down to 62.5 kHz . This is further divided by the programmable eight-bit counter. Dividing by 105 (decimal) gives 595.24 Hz ; dividing by 104 gives 600.96 Hz , and that's as close to 600 Hz as it's possible to get.

The serial data word always starts with an onbit; the next seven each represent the required state of one of the remote appliances; the stop bit is always an 'off'.

## References

1. The Intelligent Plug, N.McArthur, A. Wingfield and I.Witten, Wireless World. December 1979
2. Micro-controlled radio-code clock, N.E. Sand, Wireless World, June/July 1982
3. Rewbichron 2, J. Robinson, Radio \& Electronics World, April/May 1983

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| 4164 150ns Not Texas. | . 1.35 | 1.15 | 1.05 |
| 41256150 ns | 2.95 | 2.70 | 2.55 |
| 2114 200ns Low Power. | . 1.75 | 1.60 | 1.55 |
| 6116 150ns.......... | . 1.99 | 1.80 | 1.65 |
| 6264 150ns Low power. | . 3.75 | 3.45 | 3.30 |
| 2716 450ns 5 volt......... | . 3.85 | 3.45 | 3.30 |
| 2732 450ns Intel type | . 4.75 | 4.25 | 4.10 |
| 2764 300ns Suit BBC | .2.15 | 1.99 | 1.80 |
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## 68000 hoard - 5

## Bob Coates continues his description of the Kaybug monitor software with a look at its system calls

The monitor offers 26 system calls or subroutines for user programs to draw upon. These handle keyboard input and screen output functions but also include number base conversions and a 32 -bit divide routine.
The calls are invoked by setting up the appropriate entry conditions and then executing a trap \#11 instruction followed by a word-sized number indicating which call is being made.
All calls except renter when completed return to the user program and continue with the next instruction, as if a jsr instruction had been used.
Table 1 lists the calls available in version 1.0 of the monitor along with the number that follows the trap \#11 instruction.
A more detailed description of each call is now given.
renter: this call terminates a users' program and transfers control back to the monitor, giving the monitor prompt.

Entry conditions: none.
Exit conditions: not applicable.
outch: outputs a character in $\mathrm{d}_{0} . \mathrm{b}$, then checks whether 'break' < del> or 'hold' <con-
trol- $\mathrm{S}>$ characters have been received. If 'break' received, does not return to caller but aborts user program and returns to monitor. If 'hold' received, waits until a different character is received before returning to caller.
Entry conditions: $\mathrm{d}_{0} \cdot \mathrm{~b}=$ Ascii character to be output.
Exit conditions: all registers preserved.
sendch: outputs character in then returns to caller without checking for 'break' or 'hold'.
Entry conditions: $\mathrm{d}_{0} \cdot \mathrm{~b}=$ Ascii character to be output.
Exit conditions do.b. undefined, other registers preserved.
outs: outputs a space character. Uses outch (see comments about 'break' and 'hold').
Entry conditions: none.
Exit conditions: all registers preserved.
spaces: outputs a number of space characters as indicated by $\mathrm{d}_{\mathrm{l}}$.w. Uses outch.
Entry conditions $\mathrm{d}_{0} . \mathrm{w}=$ number of spaces required. 1 to 65535 .
Exit conditions: all registers preserved.
pdata 1: outputs Ascii string pointed to by $\mathrm{a}_{56}$ and terminated by a null byte (00). Sends all bits of each character unmodified. Uses outch.
Entry conditions: $\mathrm{a}_{6}=$ address of start of string
Exit conditions: $d_{0} \cdot b=0$ $a_{5}=$ address of string terminator +1 ; all other registers preserved.
pdatam: As pdata1, but takes account of the display mode currently in use.
Characters with bit 7 clear i.e. normal Ascii characters, are always output. But the outputting of characters with bit 7 set depends upon the display mode selected.
In $80-\mathrm{column}$ mode, characters with bit 7 set are ignored and there is no output. In

40-column mode, characters have bit 7 stripped and are output as normal characters.

Entry conditions: $a_{6}=$ address of start of string.

Exit conditions: $\mathrm{d}_{0} \cdot \mathrm{~b}=0$; $a_{f}=$ address of string terminator +1 ; all other registers preserved.
query: outputs a '?' and sounds bell/buzzer/bleep. Uses outch.

Entry conditions: none
Exit conditions: all registers preserved.
outhex: outputs contents of lowest four bits in $\mathrm{d}_{0}$ as an Ascii hex character. Uses outch.

Entry conditions: $\mathrm{d}_{\mathrm{n}}=$ hex value.

Exit conditions: $\mathrm{d}_{0}=$ undefined; other registers preserved.
out2hx: outputs contents of lowest eight bits in $d_{0}$ as two Ascii hex characters. Uses outch.

Entry conditions: $d_{11}=$ hex value.

Exit conditions: $\mathrm{d}_{\mathrm{in}}=$ undefined; other registers preserved.
out 4 hx : outputs contents of lowest 16 bits in $\mathrm{d}_{0}$ as four Ascii hex characters. Uses outch.
Entry conditions: $d_{0}=$ hex value.
Exit conditions: $d_{1}=$ undefin ed; other registers preserved.
out 8 hx : outputs contents of $\mathrm{d}_{0}$ as eight Ascii hex characters. Uses outch.

Entry conditions: $d_{0}=$ hex value.

Exit conditions: $d_{0}=$ undefin ed; other registers preserved.
crlf: outputs a carriage return and line feed. Uses outch.

Entry conditions: none.
Exit conditions: all registers preserved.
getch: waits for character to be received from input.
When character received, checks whether 'break' or 'hold': if 'break', does not return to caller but aborts user
program and returns to the monitor. If 'hold', waits for another character to be received (other than 'break' or 'hold') before returning to caller. Returns with Ascii character in $\mathrm{d}_{0}$.b, bit 7 forced clear.

Entry conditions: none.
Exit conditions: $\mathrm{d}_{0} . \mathrm{b}=7$-bit Ascii character; all other registers preserved.
readch: waits for character to be received from input and returns with it without checking for 'break' or 'hold'.
Entry conditions: none.
Exit conditions: $\mathrm{d}_{0} \cdot \mathrm{~b}=7$-bit Ascii character; all other registers preserved.
gethex: gets Ascii character and converts it to hex, returning with hex value in $\mathrm{d}_{0}$ and ' $c$ ' bit in status register clear. If character was not a hex character, i.e. not $0-9$ or A-F, then returns instead with Ascii code and ' $c$ ' bit set.
Uses getch: see comments about 'break' and 'hold'.

Entry conditions: none.
Exit conditions: (hex character) $d_{0} \cdot b=$ hex equivalent of character, s.r. 'c' bit $=0$; (non-hex character) $\mathrm{d}_{0} . \mathrm{b}=7$-bit Ascii character, s.r. 'c' bit=1. All other registers preserved.
conhex: as gethex, but does not get character from input. Enter instead with Ascii character in $\mathrm{d}_{0}$.b.

Entry conditions: $\mathrm{d}_{0} . \mathrm{b}=7$-bit Ascii character.
Exit conditions: (hex character) $\mathrm{d}_{0} . \mathrm{b}=$ hex equivalent of character, sr ' $c$ ' bit $=0$; (nonhex character) $\mathrm{d}_{0} . \mathrm{b}=7$-bit Ascii character, sr 'c' bit =1. All other registers preserved.
gpch: gets character from input and echoes to output. Returns with it in $\mathrm{d}_{0}$. b ; if lower case, converting it to upper case. Uses getch.
Entry conditions: none.
Exit conditions: $d_{0} . b=7$-bit Ascii character (upper case); all other registers preserved.
get2: gets two Ascii characters. Calls gpch twice and assembles the two characters in $\mathrm{d}_{0}$. w .

Entry conditions: none.
Exit conditions: $\mathrm{d}_{0} \cdot \mathrm{w}, \mathrm{b}_{15}-\mathrm{b}_{8}=$ first Ascii character; $\mathrm{b}_{7}-\mathrm{b}_{0}=$ second Ascii character.
hexin: gets string of characters from keyboard, converting them to hex and
building in $d_{1}$. Returns after a non-hex character with the last eight hex characters entered in $\mathrm{d}_{1}$, leading zeroes being inserted if necessary. Register $d_{0}$ contains the non-hex terminating character and $\mathrm{d}_{2}$ the number of hex digits entered. Uses gpch.

Entry conditions: none.
Exit conditions: $\mathrm{d}_{0} . \mathrm{b}=$ nonhex terminating character; $\mathrm{d}_{1} .1=$ eight hex characters; $\mathrm{d}_{2} . \mathrm{I}=$ number of hex characters entered; all other registers preserved.
getadr: prompts operator to enter an address. Returns with address in $a_{0}$ and number of characters entered in $\mathrm{d}_{2}$. Rejects odd addresses. Uses gpch.

## Entry conditions: none.

Exit conditions: $\mathrm{a}_{0}=$ address entered; $\mathrm{d}_{2}=$ number of characters entered.
range: prompts user to enter a beginning and end address, giving the option of re-using the last used values (as used by the $P R$ command). If values entered, updates ram registers begadr and endadr with new values. If just <cr> entered, registers left unmodified.

For Kaybug version 1.0, begadr is at $400000_{16}$ and endadr at $400004_{16}$.

Entry conditions: none.
Exit conditions: begadr and endadr updated if new values entered; all registers preserved.
strend: prompts user to enter block start and end addresses (as used by $L W$ command). Returns with start address in $\mathrm{a}_{2}$ and end address in $a_{1}$.
Entry conditions: none.
Exit conditions: $a_{1} .1=$ end address; $a_{2} . l=$ start address; all other registers preserved.
binbcd: converts a 27-bit binary number in $d_{0}$ to eight packed b.c.d. digits in $d_{1}$, with ' $c$ ' bit in status register clear.
If input value exceeds maximum allowed (5F5E0FF 16 ) then $d_{1}$ is undefined and the ' $c$ ' bit is set.
Entry conditions: $\mathrm{d}_{0} . \mathrm{l}=27$-bit binary number.
Exit conditions (valid input): $\mathrm{d}_{1}=8$-digit packed b.c.d. result, s.r. 'c' bit=0; (invalid input) $d_{1}=$ undefined, s.r. ' $c$ ' bit $=1$. All other registers preserved.
bcdbin: converts an 8 -digit packed b.c.d. number in $\mathrm{d}_{0}$ to binary equivalent in $\mathrm{d}_{1}$.
Entry conditions: $\mathrm{d}_{0} .1=$

## Motorola S-Tormat files

This format provides a means of Ascii-encoding binary object files for transfer between systems.


## S <br> n

size
address
data

## checksum

is simply the Ascii code for the letter S. is the record type: $0=$ header, $1=$ data ( 16 bit address), $2=$ data ( 24 -bit address), $9=$ end of file.
indicates the number of bytes (hex) in this record (address, data and checksum). is four or six hex characters for record types 1 and 2 respectively. For types 0 and 9 it is 0000 . is the block of ascii encoded binary data. Each record typically contains a 16 -byte block, but may be more or less. is the one's complement of the sum of the size, address and data.

Each record is followed by carriage return and line feed. This example shows the S-file produced for the object code for example 1 (to be given in the next article).
S0090000657861603120FA
52144004007000720020700000010052800601000445
S208400410558860F670
59030000F:
The header record holds the name of the object file as it was on the development system which produced this, 'EXAM1'.
eight-digit packed b.c.d. number.
Exit conditions: $d_{1} .1=$ binary result; all other registers preserved.
divide: integer-divides the number in $\mathrm{d}_{0}$ by the number in $\mathrm{d}_{1}$. Result is in $\mathrm{d}_{4}$ with remainder in $\mathrm{d}_{5}$.

All numbers are in 32 -bit two's complement binary. Sign conventions used are:

|  |  |  |  |
| :--- | :--- | :--- | :--- |
| dividend | divisor | result | remainder |
| + | + | + | + |
| + | - | - | - |
| - | + | - | - |
| - | - | + | - |

Entry conditions: $\mathrm{d}_{0}=$ dividend; $d_{1}=$ divisor.
Exit conditions: $d_{4}=$ result; $d_{5}=$ remainder; all other registers preserved.

## Exception handling

The way in which interrupt exceptions are handled by the 68000 is to go to a specified location according to the exception designation, fetch a long

Table 2

| Assignment |  | Ram oddress |  |
| :---: | :---: | :---: | :---: |
| Level | 1 | 400016 |  |
| Level | 2 | 40001 C |  |
| Level | 3 | 400022 | Autovector |
| Level | 6 | 400028 | $\}$ interrupts |
| lever | 5 | 40002 E | interrupts |
| Level | 6 | 400036 |  |
| Level | 7 | 40003 A |  |
| trap | \# 0 | 400040 |  |
| trap | * 1 | 400046 |  |
| trap | \# 2 | 400046 |  |
| trap | \# 3 | 400052 |  |
| Trap | \# 4 | 400058 | Trop |
| Trap | \# 5 | 40005 E | Pinstructions |
| trap | * 6 | 400064 | instructions |
| trap | \# 7 | 40006 A |  |
| trap | \# 8 | 400070 |  |
| trao | 49 | 400076 |  |
| trag | - 10 | 400076 |  |
| Vector | 54 | 400082 |  |
| vector | 65 | 400088 |  |
| vector | 66 | 40000 E |  |
| vector | 67 | 400094 | > User |
| vector | 68 | 40009 A | < interrupts |
| vertor | 69 | 400040 |  |
| vector | 70 | 400046 |  |
| vector | 71 | 4000 AC |  |

word (four-byte) address from it and re-start processing from that address.
There is a slight problem with the Kaycomp in that these exception vector addresses are in the eprom space and so a user program cannot alter them.
To circumvent this difficulty, for each interrupt vector that may be used on the Kaycomp, a six-byte block of ram is allocated. The exception vector in eprom contains this address and so processing will jump to this location.
The six-byte space allows the user program to insert a 'jump absolute, long' instruction, the jump destination address being that of the user's exception service routine.

The exception processing sequence will thus be

1. Get vector and go to that address.
2. Execute jump instruction at that address.
3. Continue processing at jump destination address.
Ram 'jumpers' are provided for all autovector interrupts and eight user interrupt vectors are also catered for. These are for vector numbers from $64\left(40_{16}\right)$ to $71\left(47_{16}\right)$ and would be used by 68000 peripherals interrupting on $\mathrm{IPL}_{1}$.
Trap instructions with vector numbers from 0 to 10 may also be used in user programs. These are handled in the same manner as interrupts. Trap numbers 11 to 15 are reserved for use by the monitor.

A complete list of these 'jumpers' is given in Table 2.
The remaining assigned system exceptions, such as Bus Error, Address Error etc, cannot be intercepted by the user program but can cause a return into the monitor with an appropriate message displayed.

To be concluded.

The DMS8832 memory module for this project is available under the type number EDH8832C (with the suffix - 15PC for the 150 ns version) from MicroCall, Thame Park Road, Thame, Oxfordshire; tel. 084421-5405.

## by Tom Ivall

## D.B.S. s

 s David Withers mentioned in the December issue ( p .75 ) the most recent ITU pronouncement on direct broadcasting by satellites came at last year's World Administrative Radio Conference. This meeting, WARC 85, formally approved the d.b.s. plan previously worked out in detail at RARC 83, a regional conference specially convened in 1983 for ITU Region 2, which broadly means the Americas.A similar situation occurred in 1979 when the big WARC 79 world conference formally agreed to the d.b.s. plan put together for ITU Region 1 (Europe, Africa, USSR) and Region 3 (Far East and Australasia) at WARC 77, which had been entirely devoted to satellite broadcasting. As a result we now have a complete world-wide plan - in frequencies, channels, powers, orbital positions etc. all signed and
sealed and just waiting for someone to start using it for full broadcasting operation.
The Japanese came near to starting the first cl.b.s. service in early 1984 when they launched a satellite from their Tanegashima Space Centre and placed it in geostationary orbit in their allocated orbital position of $110^{\circ} \mathrm{E}$. But, as was reported in $E \& W W$, faults rapidly developed in the transponders' travelling-wave tubes and the whole project had to be downgraded to an experimental status.
Meanwhile, we have seen the unexpected development of what has become known as 'semi-d.b.s.' or 'quasi-d.b.s.'. Transmissions from communications satellites, originally intended purely for distribution of television and sound programme feeds within the broadcasters' own networks, have become, willy-nilly, a sort of broadcasting in themselves. When cable tv systems use
these programme feeds the signals are in any case 'broadcast' to a number of widely-spaced head-end receiving stations. And when reception of these transmissions by individuals was legalized, the comsats thereby became broadcasting stations in an even fuller sense, while still doing the job they were originally intended for. D.J. Standen's article in the December 1985 issue describe this 'quasi-d.b.s.' phenomenon in detail.

International planning for satellite systems has actually been under way for two decades or more. The ITU held its first conference on extraterrestrial radio communication as long ago as 1963. This was when comsats were first beginning to establish themselves as practical relay stations. The second World Space Telecommunications Conference followed in 1971. Then came WARC 77 and


RARC 83 as mentioned above. What has emerged, however, has been somewhat confusing. The planning criteria and methods used at WARC 77 and RARC 83 are markedly different from each other. No doubt this is due to the lapse of time between the two events, the development of spacecraft and radio technology during this period, and the different interests and assumptions of the two groups of people concerned.

# ... the whole situation here is still confused and uncertain and likely to remain so for some years 

Both conferences started from the $12-\mathrm{GHz}$ frequency band specifically allocated to satellite broadcasting. Within this, Region 1 is allowed to use 11.7 to 12.5 GHz , Region 2 has 12.2 GHz, while Region 3 can operate in the two sub-bands $11.7-12.2 \mathrm{GHz}$ and $12.5-$ 12.75 GHz . From these allocated blocks of frequencies WARC 77 and RARC 83 worked out frequency channels, wave polarizations, orbital positions, coverage areas or 'footprints' and minimum and maximum radiated powers.

WARC 77 divided up the 800 MHz between 11.7 and 12.5 GHz into 40 channels spaced at equal intervals of 19.8 MHz . Each of these channels is 27 MHz wide, so there is some frequency overlap, but this is taken care of by opposite directions of circular polarization. RARC 83, on the other hand, split up the 500 MHz from 12.2 to 12.7 GHz into 32 channels, each of 24 MHz width. The obvious channel overlapping here is again dealt with by opposite directions of circular polarization. The spacing between transmissions with similar polarizations is 29.16 MHz.
In both plans the channels are grouped into 8 channelfamilies. But in WARC 77 each family consists of five frequencies spaced at four-channel intervals, while in RARC 83 each family has four frequen-
cies spaced at these intervals.
But perhaps the most marked difference between the two regional plans is in the orbital positions, or 'slots', chosen for the satellites in the geostationary orbit. In WARC 77 these slots for Regions 1 and 3 satellites are a regular $6^{\circ}$ apart. In RARC 83, however, they are not equally spaced but have a variable spacing which ranges from as close as $1^{\circ}$ to as far apart as $11^{\circ}$.

Then in WARC 77 each country in Regions 1 and 3 has been assigned just one orbital position, and it shares this with other countries. An exception is the USSR which has five slots because of its huge geographical area. But in RARC 83 several countries have more than one slot. The L'SA, for example, has eight in all.
Another difference between the two schemes is in the number of channels assigned to each country. WARC 77 gives each country a standard ration of five channels, whereas in RARC 83 there is considerable variation. Some small Region 2 countries have as few as four channels while, for example, the eastern region of the USA alone has as many as 128 .
In the power flux densities specified, however, the two plans are very similar. At the outer edge of each 'footprint' WARC 77 lays down a requirement for a minimum of - 103 $\mathrm{dBW} / \mathrm{m}^{2}$, while RARC 83 specifies a minimum of -107 $\mathrm{dBW} / \mathrm{m}^{2}$ or a little higher in some situations.
The different structures of the two plans are significant in relation to their capacity to deliver programmes and their flexibility of use in different situations. What does this mean in practice? As an illustration, E.R. Reinhart of the Satellite Television Corporation in the USA has anlaysed the differences shown up by projected implementation of WARC 77 in Africa and RARC 83 in Latin America. He concludes that Latin American countries would not only get greater numbers of channels for broadcasting but would also have greater flexibility for system implementation than would be possible for the countries of Africa.
The accompanying diagram gives some idea of what the whole d.b.s. plan looks like in
terms of orbital positions for different countries around the geostationary orbit. Because there are 150 or more countries in the world the diagram does not attempt to show them all it would be very difficult to read. Instead we have arbitrarily selected the fifty or so countries that can be expected to be the first in the field in starting up cl.b.s. services. On the assumption that these are likely to be the richest, most industrialized nations, the broad criterion has been to take those at the top of the league table of Gross National Product per capita. This means roughly the major capitalist and communist countries. An exception to this rule of thumb is Inclia, which has been included because of its outstanding pioneering work in satellite broadcasting. It was the first country in the world to set up an experimental d.b.s. system - the famous Satellite Instructional Television Experiment of 1975 (reported in this journal).*

Television transmission standards used for d.b.s. will depend on decisions outside of those laid down in the ITU world-wide plan. They could be, for example, predominantly NTSC in North America and Japan and predominantly Cmac packets in Western Europe, but the whole situation here is still confused and uncertain and likely to remain so for some years.
Britain, of course, is still a long way from establishing any kind of d.b.s. service. The government-inspired Unisat consortium collapsed last year; a new group called Britsat has put up another proposal and the government is reported to be considering this and other current suggestions. Meanwhile, it looks as though France or Germany may be the first to launch a d.b.s. service in Europe. This would be the outcome of Eurosatellite, a Franco-German manufacturing consortium which is building two similar spacecraft, the TDF-1 for France and the TV-Sat 1 for West Germany. Electronic component manufacturers in Germany have already developed and put on the market various new components for receiver designs intended to work from TV-Sat transmissions.

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## Power supplies from Sweden

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A transformer with a specific inductance stores energy while the transistor is on. The energy cannot be passed to the secondary output as it is blocked by the diode. When the transistor is cut off, the stored energy is
discharged with opposite polarity allowing the diode on the secondary side to conduct. This technique allows considerable reduction in component-count as is shown by the picture. Both circuits perform the same task.
The standard range includes d.c.-to-d.c. converters in ratings from 20 to 250 W , with up to four outputs; a.c.-to-d.c. power supplies from 60 to 240 W ; customized units from 5 to 250 W .
The range has become available as a result of reorganization within the Ericsson group. Rifa, a subsidiary has taken over the power supply division of its parent which originally produced supplies for Ericsson's own products. Rifa
AB, Market Chambers, Shelton Square, Coventry CV1 1 DJ. EWW 209 on reply card.


## CP/M on a PC

For those who have grown fond of their CP/M software and yet want to graduate to a computer running PCDOS or MS-DOS, rescue is at hand from G -Tek, an American company who have produced a CPemulator. This package makes your IBM PC. or similar, think that it is being run by a 280 with CP/M. Two parts are
used: a conversion utility to load CP/M programs onto IBMcompatible discs, and a 'bind" utility that attaches the CPemulator to the programme. All the software developed on a CP/M coniputer can then be run on a PC -IJOS computer without altering a byte. £199(+vat) from Bytron Lid. High Street.
Kirmington, S. Humberside, I)N39 6'Z. EWW 222 on reply card.


## Adhesives for electronics

A range of products specifically aimed at the electronics industry have been produced by Loctite. Chipbonder is for the rapid placement of surface mounted components so that they are held in position prior to soldering. The bonds are completely cured after 4 to 5 minutes of heat treatment or in 30 to 45 s when exposure to low intensity u-v light is followed by $120^{\circ} \mathrm{C}$ heat. The resultant bonds are flexible and shock-resistant and can withstand wave soldering. The adhesive is coloured fluorescent pink to aid inspection. Output 384 is a thermallyconductive adhesive for heat dissipation. It may be used to replace tapes, mechanical fasteners and non-conductive adhesives and is claimed to have a better heat-conductivity than zincoxide grease. It sets in 30 s and is fully cured in one to four hours.

Other adhesives are all cyanoacrylate products. Assure

425 seals fasteners and locks adjusting screws against vibration. Ultra-performance Tak Pak 382 is an improved version of an adhesive for wire tacking and bonding smaller components. Black Tak 410 is a toughened cyanoacrylate adhesive used for strain relief and the mounting of large units and covers. It is claimed to have a peel and impact strength superior to many epoxy resins. Further arlditions to the "PCB Assembly Line" range include a silicone sealant that does not tarnish copper or brass and can be used for encapsulating components, a freezer aerosol, a non-conductive solvent for cleaning, a contact lubricant and cleaner and spray-on protection shield for p.c.bs against humidity and environmental pollution. It may be soldered through for spot repairs. Loctite UK, Watchmead, Welwyn Garden City, Herts AL7 1JB. EWW 211 on reply card.

## Video effects computer

An instrument from Fairlight, the Australian makers of the Computer Music Instrument, has done to visual images what their synthesizer did to music. It is a very versatile device for manipulating images. It has a wide range of applications but, we suspect, is most likely to be used in providing the weird effects that seem to go with pop music. The Computer Video Instrument (CVI) can take an image from a "live" camera, tape, film, a slide or still picture and manipulate the image in real time. It is also provided with a stylus-sensitive pad that enables drawing or writing to be superimposed on the image. Its
repertoire inclucles a palette of over four thousand colours. Its output can be stored on video-tape and then recalled for further manipulation or combination with other images.

Background and foregrounds can be created and made to move or have live images moving through them. Three planes are used in a single CVI but more than one can be cascaded to provide a number of different planes.

A chroma-key facility enables still images to be panned or zoomed or stretched or a moving sequence can produce the sort of multi-image associated with stroboscope pictures.

Any shape may be used as a 'cut out' or matte to control areas for different foregrounds or backgrounds, patterns or other effects. A live image can be frozen and then manipulated using all the other facilities. An audio input may be used to control an image and this can be combined with freeze effects, 'trails' split or mirror images to produce some spectacular effects.

Using the input pad it is possible to pull an image out of shape and add colours or cletails; Dr Jekyll no longer needs to use a lot of changes in make-up to change into Mr Hyde: it can be done for him on the machine! Lettering or other
static devices can be added to an image using a "cut and paste" technique. Many geometrical functions can be called up for the creation of charts, graphs and diagrams, which can have any of 54 textures applied to them.

All this fits into a 19 in rack mounting box with a remote control console. The unit provides connectors for synchronization input and outputs and has two video inputs which may be composite or RGB. An RS232 communications port enable control from an external computer. $\$ 4950$ ( + tax) from Syco Video, 20 Conduit Place, London W2. EWW 213 on reply card.

## LCD oscilloscope

A hand-held, battery powered 3.2 MHz oscilloscope features a dual-trace liquid crystal display. The display consists of a 128 by 160 dot matrix with a display area of about 76 by 95 mm . The internal memory is battery-backed for waveform storage which allows later waveform analysis. Features of the Y-axis operation include a scale of four vertical divisions for each channel, a nine-range sensitivity from 10 mV to $5 \mathrm{~V} /$ division and a frequency accuracy of $\pm 3 \mathrm{~dB}$ or less from d.c. to 200 kHz . The X-axis has 10 divisions with 20 sweep speeds from $5 \mu$ s to $\overline{5} / \mathrm{Div}$ : there are continuous and single sweep measurement modes and positive, negative and switchable trigger modes. Soar Model 1000 also incorporates a full-function autoranging digital multimeter. Cost just under $£ 1000$, exclusively from Advance House of Instruments, Raynham Road, Bishop's Stortford, Iterts CM23 5PF
EWW 214 on. reply card.


## Serial line converter

L'sed one at each end of a data channel, the Serial line converters from CDOS enable data transmission to be established over longer distances than the R8232 ports of the devices to which they are attached. This is achieved by converting the transmission level to RS 422 standards. Full duplex operation is possible, with handshaking in either direction. The converter does not modify protocol or data word format, which are determined by the equipment connected to the channel.

20 mA current-loop send and receive channels can be added by plug-in modules, which provide either active or passive
ransmitter or receiver functions: four modules in all.
RS 422 extends the range of serial communication from the 30 m of RS2 32 to one km . Current loop transmission extends this even further: up to 5 km .

The transmitter and receiver modules can be adapted to cope with data from any serial source RS232, t.t.l. and CCIT'T/EIA levels. The output from a uart or a.c.i.a. can be connected directly The devices come in a case with a mains power supply but the double-sided board may be extracted and built directly into equipnent. C.D.O. Systems Ltd, Unit 65, Corby Workshops, Corby. Northants NN17 IYB. EWW 210


## Universal PCM transcoder

For use on North American and European digital transmission telephone lines, the J Iarris HC-5560. The four standard p.c.m. coding schemes can be accommodated: Alternative mark inversion (AMI), High-density bipolar three (IIDB3), Bipolar with six zero substitution (B6ZS) or with eight zero substitution (B8ZS). HDB3 is the recommended CCITT standard The device can be used in most equipment that can communicate with T1, T1C, T2 or
PCM-30/CEPT lines, including
multiplexers, channel service units, echo cancellers, digital cross connects and p.c.m. repeaters.

The device operates from a single 5 V supply with a 100 mA maximum current drain. It can encode and decode simultaneously: includes an alarm signal driver can operate asynchronously with loop-back control and transmission error detection. HC-5560 is priced at $£ 9.29$ in quantities of 100 . Harris MHS Semiconductor Ltd, Eskdale Road, Winnersh, Berks RG115TR. EWW 215 on reply card.

## Surge suppressors

A new type of power integrated circuit is capable of diverting dangerous transient energy away from sensitive electronic circuitry. Called a Surgector, this RCA monolithic device is a thyristor with a special diffused gate section which acts as a zener diode. This permits the anode voltage to turn on the device, giving it a very fast voltage rise time; lightning. for example, can rise at $1 \mathrm{kV} / \mathrm{ms}$. The Surgector device clamps the voltage by its zener action until the integral thyristor turns on and shunts the excess voltage away. In most cases, the protected circuitry never sees a voltage greater than $130 \%$ of its normal working voltage. 'Twoterminal devices have off-state voltage ratings of 30,58 and 225 V .

They switch in nanoseconds and can handle peak surge currents of 300 A . The three-terminal Surgector adds clirect access to the gate of the s.c.r. which allows the device to be triggered with a user-supplied voltage-level detector. Current devices are uni-directional but a bidirectiona 1225 V device is about to be released. They are specifically designed to protect telephone equipment. However, the small (TO202) size and low cost make then equally suitable for computers, alarm systems, cars, tv, outdoor lighting, c.a.t.v. and many other applications. RCA Solid State. Lincoln Way, Windmill Road, Sunbury on Thames, Middlesex TW 167 HW . EWW 223 on reply card.

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| :---: | :---: | :---: |
| HY30 | ． 15 | 4.3 ．．．． 1045 |
| HY60 | 3. | 4B．E10．45 |
| HY6060 | （35－30 | 4．8．E21．95 |
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| HY244 | ． 120 | $4 \quad E 22.45$ |
| HY248 | ． 120 | $8 \quad £ 2245$ |
| HY364 | ． 180 | $4 \quad$ E33．45 |
| HY368 | ． 180 | ． $\begin{aligned} & \text {（ }\end{aligned}$ |
| Distortion | less inan 0.0 | ．01\％ |


| Type | Output <br> Power <br> Watts（rms） | Load <br> Impedence <br> $\Omega$ |  |
| :--- | :--- | :--- | :--- |
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| PSU522 | 2 HY 124 | F22．45 |
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| PSU542 | ．． 1 HY248 | ¢22．95 |
| PSU552 | ． 1 MOS248 | ¢24．95 |
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## Write-once proms

Intel argues that the time consumed by extracting a u-v eprom, erasing it and then reprogramming it is too expensive to be worth it. So they have brought out a family of proms without a window so that once programmed they cannot be erased. What's more they have developed a Quick-Pulse programming algorithm that enables the devices to be programmed in 100 th of the time required by u-v eproms - about four seconds. The software is implemented in Intel's own universal programmers as well as those sold by Data I/O. The proms are manufactured in plastic as opposed to the ceramic packaging of their erasable predecessors, which makes them robust and lower cost. The proms are electrically and pincompatible with the eproms and are distinguished by the prefix " $P$ " instead of " D ". The range comprises the P2764A, P27128 and P27256. Intel Corporation (LK) Ltd, Pipers Way, Swindon, Wilts SN3 1RJ. EWW 220 on reply card.

## Charge-coupled character reader

A 256-photodiode linear c.c.d. image sensor (TH 7806) is suitable for small optical - character recognition systems and desk-top computer interfacing. Each photoelement is $13 \mu \mathrm{~m}$ square and is optimized for an even response in the 400 to 1100 nm spectral range. The maximum data rate is 2 MHz . A noise dynamic range of $6000: 1$ allows sufficient grey-scale depth to enable the easy and reliable discrimination of smudges, etc, from the printed matter.


The sensor comes in a ten-pin d.i.l. package and can have a guaranteed accuracy to within $50 \mu \mathrm{~m}$. The option of a Z-type epitaxial substrate prevents the deterioration which may be caused by infra-red components in the illumination source and ensures high performance whatever the source Thomson-CSF Components and Materials Lttl, Ringway House, Bell Road, Basingstoke. Hants RG24 0QG. EWW 221 on reply card.


## Audio measuring system

The ubiquitous microprocessor can be found lurking within the MJS401D, resulting in fast and accurate audio measurements. Standard functions allow measurement of level, noise, frequency, distortion and crosstalk. Plug-in options include extra filters, IEEE interface, IMD, wow and flutter. The unit incorporates an MD404B twin-tone oscillator, but
this can be omitted in receive-only applications.
The level measurement range is from -110 to +40 dBm with a claimed accuracy of better than 0.1 dB . Distortion measurements is possible down to $0.0008 \%$
( -102 dB ). The dual-range meter display enabled rapid calibration of the equipment under test. The meter automatically switches


## Torodial transformers and chokes

A range of toroidal transformers includes 87 different standard configurations of from 15 to 990VA. Any other configuration is available to order. The Transduktor range has been designed to maximize the advantages of toroids; lower weight, smaller size, low no-load losses, and less acoustic hum and magnetic interference. Earthed copper foil is used to prevent electrostatic interference and a Mu-metal screen around the outside of the transformer minimizes electromagnetic interference. To reduce this even further the design maintains a constant number of amp-turns per unit circumference of the toroid This requires the placing of Mylar insulation and earthed copper
screen between primary and secondary windings. The range meets the requirements of most international standards. Various options for mounting the transformers are provided.

Computerized design allows the company to respond to almost any request with an optimized transformer design. Samples can be provided very rapidly.

The range is complemented by a set of toroidal chokes for switchmode power supplies. These are designed to run at 40 kHz with a ripple current of $10 \%$. They are wound on powder cores having a distributed air gap and offer similar advantages to the transformer range. Transduktor Ltd, 443B Holloway Road, London N7. EWW 207 on reply card.
between the $\pm 12 \mathrm{~dB}$ range to a $\pm 1.5 \mathrm{~dB}$ range for adjusting the reference level which is set in 1 dB steps from the front panel. The instrument can be programmed externally through the bus to be ranged antomatically, allowing readouts of both frequency and level. Distortion and crosstalk measurements are fully automatic Technical Projects Ltd, Unit 2, Samuel Whites Industrial Estate, Medina Road, Cowes, Isle-of-Wight PO31 7LP. EWW 219 on reply card.

## High-resolution monitors

Colour monitors for data and graphics displays are built around a compact c.r.t. driver board only 140 by 178 mm . Miniaturization has been achieved by the use of thick-film hybrid circuits allowing the video amplifiers to be mounted on the c.r.t. baseboard. By separating the power supply, the driver circuit and baseboard are made suitable for use by equipment manufacturers who can obtain the c.r.ts directly and supply their own power supplies.
Kent Modular Electronics have based their marketing on a similar system for o.e.m. monochrome monitors and have found it to be successful; they are now transferring their expertise in thick-film applications to the colour monitor. They also manufacture complete monitors and produce a range of monochrome sets in both landscape and portrait format. They recently launched a 10 in colour monitor for use in such applications as bank dealer rooms where space is at a premium Kent Modular Electronics Ltd, Maidstone Road, Rochester, Kent ME1 3QL. EWW 208 on reply card.


## Off-air frequency standard

Computer-aided design has been used for the circuitry of the p.c.b. in the Quartzlock frequency standard. The design will operate on the current frequency transmissions of the BBC as well as those to come into operation in 1988. Outputs of 1 MHz and 10 MHz are accurate to 2 parts in $10^{11}$ long-term and 1 in $10^{10}$ in the medium term application. Uses include calibration, audit and
certification of frequency meters, counters, timers, signal sources and generators and radiotelephone test equipment.
The set uses an internal ferrite aerial and a socket for an external aerial is also provided. The p.c.b. can be retro-fitted to earlier Gould Advance and Quartzlock receivers. Dartington Frequency Standards, Moor Road, Staverton, Devon TQ9 6PB. EWW 212.


## Speech recognition on chips

A p.c.b. with speech-recognition l.s.i. circuits comes from NEC. The MC4760 analogue interface carries out equalization, amplification and analogue-to-digital conversion.
There is a signal processor which performs spectral analysis of the digitized voice input and systems controller to communicate with a host system. This can receive high level commands and transmit the results. The board is designed for isolated word recognition and is based on the filter-bank technique with dynamic progranming matching. There is a digital attenuator to enable the easy detection of the beginnings and ends of words.

The system features a 'learning and training' mode, whereby extracted features of a voice are stored in a reference memory. When a degree of simularity is established between the input and the stored reference, the results of the comparison are transmitted. A $98 \%$ recognition rate is claimed. With a 64 Kbyte memory the system has a vocabulary of 128 words: 512 words can be registered with a 64 K byte memory. The maximum length of utterance is two seconds and the average response time is 0.5 s . Available (appropriately) through Dialogue Distribution Ltd, Watchmoor Road, Camberley, Surrey GU15 3AQ. EWW 217.

## New 68000 with MMU

An addition to the 6800 family was introduced at the Paris component show by Philips Known as the SCC68070, the device includes the same central processor as the 68000 but also has a memory management unit (m.m.u.) and direct memory access (d.m.a.) control as well as a serial communications bus ( ${ }^{2} \mathrm{C}$ bus), RS-232C interface and three counter-timers all on the same chip.
The processor is fully software compatible with the 68000 family and is claimed to be the first processor to include d.m.a. and m.m.u in a single package. The c.mos device is likely to replace the 68000 in many applications where the reduction in component count with the associated lower cost would be advantageous. It also uses less power
Memory management is used to organise the memory during multitasking where the blocks of
memory associated with a specific task are kept separate from any others. Direct memory access allows blocks of memory to be transferred between the on-board memory and peripherals. The inter-i.c. ( $\mathrm{I}^{2} \mathrm{C}$ ) bus relieves the parallel bus from routine communications tasks where speed is not critical; similarly the RS-232C interface reduces the load on the parallel bus as well as reducing the external chip-count.
Internally the single chip has the equivalent of 100000 transistors and is built using 2 -micron geometry. With an internal maximum clock frequency of 10 MHz the device has a surprisingly low power consumption of 1 W .
Designed and manufactured jointly by Philips and Signetics, the SCC68070 is to be marketed in the UK by Mullard Ltd, Mullard House, Torrington Place, London WC1E 7HD. EWW 205.

## Superfast 16/32-bit processor

Claimed to be an inexpensive alternative to the multi-chip bit-slice processor, the GI DSP32010 is a second source for the TMS32010. It is said to combine the flexibility of a high-speed controller with the numerical capability of an array processor and can execute five million instruction/s.

The efficiency of this 'single-chip computer' is the result of a "comprehensive and easily programmed instruction set and of highly pipelined architecture.

Special instructions have been included to speed the execution of digital signal processing algorithms. High-speed applications include speech recognition and synthesis, radar and optical sensing, and servoloop computations; particularly in robotics. The device operates from a single +5 V . supply and is housed in a 40-pin d.i.l. package. Available through Campbell Collins Ltd, 162 High Street, Stevenage, Herts. EWW 218 on reply card.

## Super-fast floppy

A new flexible-disc drive from Epson has a formatted capacity of 4.8megabytes. BM-5 is a mainsoperated 5.25 in unit operating at a speed comparable to that of a hard disc drive. It can act as a back-up unit for hard discs and has the advantage over tape streamers of random access to the files. It also has an advantage over hard discs by being a removeable medium. It is possible to have an unlimited number of 5 Mbyte floppies compared with a fixed 10 Mbyte disc. Interface cards enable the drive to interface with Epson's own range of computers or the IBM PC and its compatibles.

The storage medium is a special 6 Mbyte double-sided high density 5.25 in floppy disc. The drives internal firmware 'compresses' the data to be stored and expands it
again when retrieved. The drive is in one box and the interface unit in another. The price is quoted as "somewhere in the region of £1,000." Epson(UK)Ltd, Dorland House, High Road, Wembley Middlesex HA96UH. EWW 216 on reply card.

## Test sockets

A series of low-insertion-force sockets has been produced by Aries. Called the Eject-a-dip range they are available in $14,16,24$, 28 , and 40 -pin versions. The levers at each end of the socket lock the i.c. into position when inserted and also are used to eject it after the test. Aries Electronics (Europe), Alfred House, Oatlands Drive, Weybridge, Surrey KT13 9LB. EWW 206 on reply card.

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The firmware is completely transparent to the user.
Comprehensive Documentation
Three informative manuals are included with the MPF-1/88. Their contents range from an introduction for beginners, all the way to complete technical specifications on all aspects of the hardware and firmware. The documentation is simple enough for those just beginning and complete enough to allow the MPF-1/88 to be used to its maximum potential.
The optional Tutorial manual takes you step by step through a hands-on tutorial on all aspects of the MPF 1/88 and the 8088 microprocessor.
Designed For Expansion
The card edge connector at the rear of the MPF-1/88 allows access to all system buses. Through the interface module the user may expand the system to include any combination of IBM style cards or MPF peripherals.
MPF-1/88: What the reviewers say
"The system documentation is very good indeed
"If you temch or want to learn about the 8088 then the MPF-1/88 is á good choice of hardware
Electronics \& Computing Monthly - August, 1985
"All-in-all.the MPF-1/88 can be highly recommended invaluable to those wishing to take their first steps in programming the 8086/8088
Everyday Electronics - August, 1985
"The manuals were a model of clarity and comprehensiveness"
"The MPF-1/88 will give you every opportunity to learn what the thing can do
Electronics Today International- July, 1985
The Technical Director of the Polytechnic Central London Microcomputer Unit says:

The MPF- $1 / 88$ is one of the best, if not the best training microcomputer I have come across. The hardware is good, the firmware is good and the documentation ts excellent Neal Hutchinson - Unirs Technical Director

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