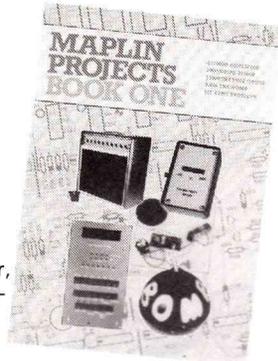


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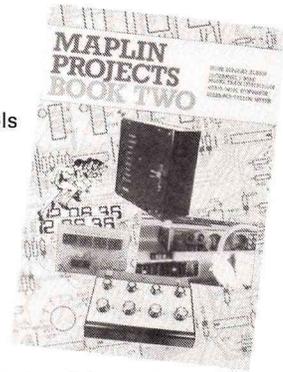
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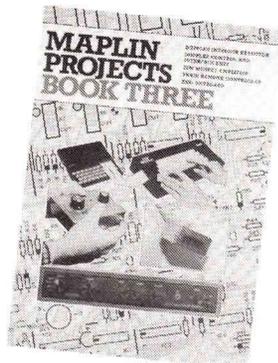
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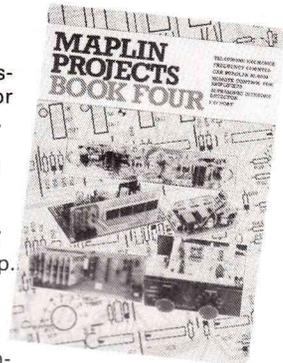
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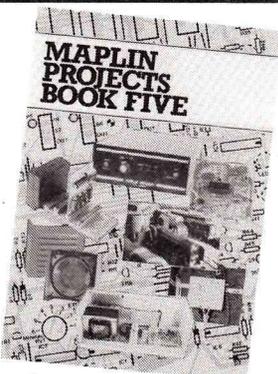
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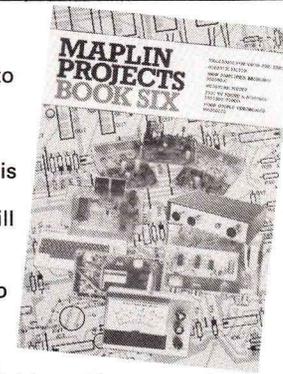
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Electronics

THE MAPLIN MAGAZINE

PROJECT BOOK SEVEN

This Project Book replaces issue 7 of 'Electronics' which is now out of print. Other issues of 'Electronics' will also be replaced by Project Books, once they are out of print. For current

prices of kits, please consult the latest Maplin price list. The price list also contains details of how to obtain a subscription to 'Electronics'.

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Vic20- RS232 Interface

- ★ Allows the VIC to connect to Modems, Printers, VDUs, or any other RS232 compatible device
- ★ Converts TTL levels to true RS232
- ★ Provides full buffering for protection of computer
- ★ Full 'X line' interface possible as well as simple '3 line' interface

by Mark Brighton

RS232 is the name given to an industry standard form of serial data communication which is used on many peripheral devices to interface them with a computer.

A byte of serial data is represented by a series of transitions between +12V and -12V on a serial data line. The marks and spaces created by these transitions contain the information for the byte of data as well as some other signals, the purpose of which is to synchronise the receiving device to the serial data stream.

The format of a 'word' of data, including these synchronising signals, is as follows:

1. The start bit. This signal alerts the receiving device that a byte of data follows, and synchronises the receiver circuitry to the incoming data.
2. Data bits. This is the ASCII encoded data, and may consist of seven or eight bits as selected by the user. It is sent least significant bit first.
3. The parity bit. This is an optional error checking bit selected by the user to conform with the requirements of the receiving set. It may be set for odd or even parity, or disabled.
4. Stop bit(s). These are one or two bits of data which are transmitted at the end of a word to separate it from the next word.

The polarity of these signals may be selected by sending normal or inverted data, either of which may be required by different devices. Apart from the serial data lines (SIN and SOUT), several other status and handshake signals are provided.

Those available on the VIC 20 are:

1. Data terminal ready (DTR). This signal is sent to indicate that the data

terminal is ready to send or receive data.

2. Data set ready (DSR). This indicates that the data set is ready to send or receive data.

3. Request to send (RTS). This signal tells the receiving device (usually called the 'data set') that the VIC (data terminal) wishes to send data.

4. Clear to send (CTS). This allows the data set to signal that it is ready to pass data from the data terminal.

5. Carrier detect (DCD). This lets the data set tell the data terminal that the communication link is established.

In addition to those lines already mentioned, there are two ground lines, protective ground and signal ground. Signal ground must always be connected, since RS232 requires that both devices have equal ground potential.

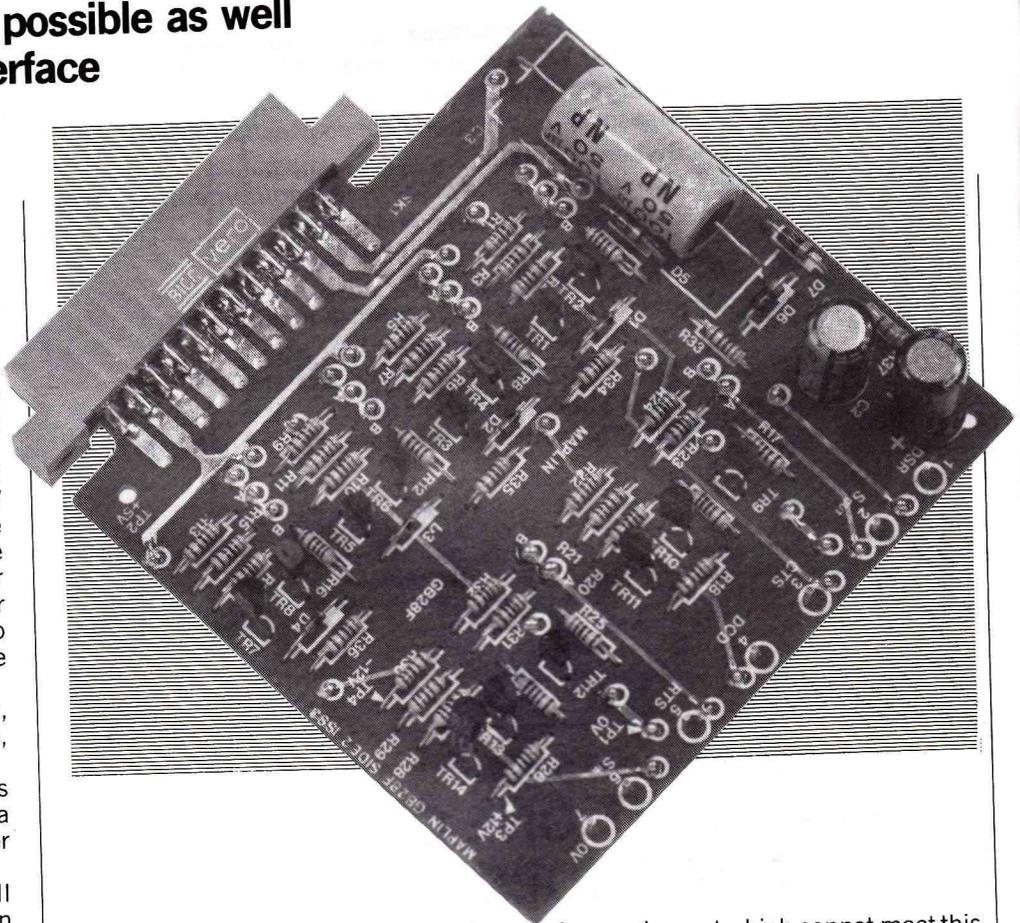
Any equipment which cannot meet this requirement is not RS232 compatible.

Circuit Description

The circuit consists of two transmit channels and four receive channels, with a power supply which provides approximately +12 and -12V from the 9V AC output on pins 10 and 11 on the user port.

Transmit Mode

SOUT from the VIC (pin M, user port) is connected to the base of TR9 via a 10k Ω resistor, R17. As TR9 turns on, bringing its collector down to 0V, TR10 turns on, raising its collector voltage to +12V. The normal, or non-inverting, output is taken via R23, a 330 Ω resistor which limits the current that may be drawn from this output to about 30mA.



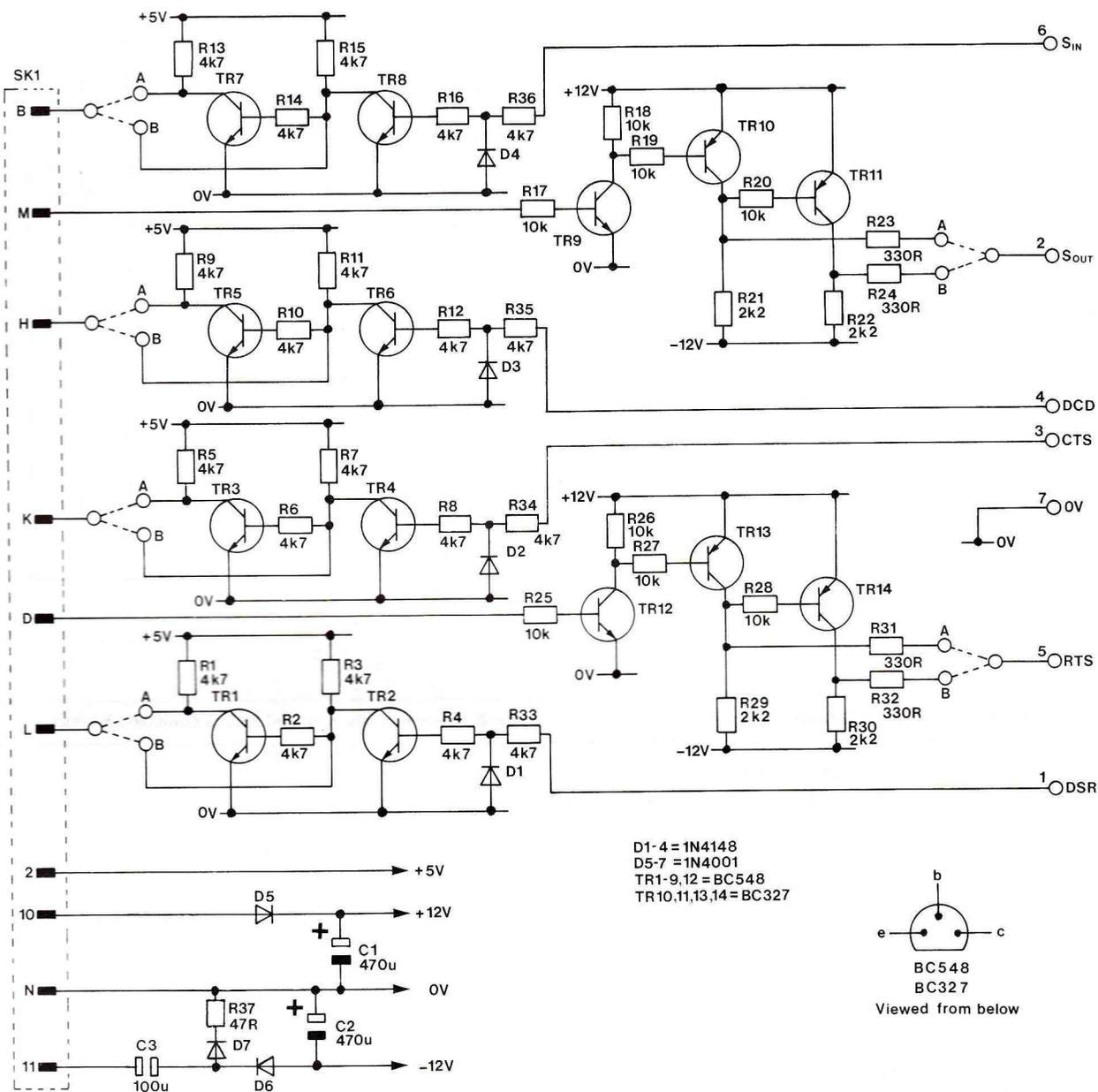


Figure 1. Circuit diagram

A second output stage is also driven from the collector of TR10, and this is identical in operation except that the output is inverted with respect to the input. The output that is used depends on the requirements of the data set.

Receive Mode

The incoming signal first has any negative content removed by D1. It then turns TR2 on and off via R4. The inverting output of the receive circuit is taken from the collector of TR2 which also drives TR1 via R2 to obtain a non-inverting output at the collector of TR1. The choice of which output to wire to the VIC is determined by the polarity of the incoming data. The VIC requires a signal which sits high between 'words' and drops low for data. S_{IN} is on pins B and C on the port, and these are connected together.

Construction

Referring to the circuit diagram and parts list, first insert all through pins (see figure 1 for signal polarity pins) and Veropins. Solder them in, not forgetting to solder both sides of the through pins. Insert all other components and solder them in. Attach the edge connector to the board, bending its pins flush with the pads on the board, and solder. Clean the board thoroughly and inspect for dry joints, shorts etc.

Testing

Plug the board into the user port, component side upwards, and switch the computer on. If the computer fails to initialise, switch off and re-check carefully for incorrectly placed components, etc. After the computer initialises,

measure test points 1 to 4 with a multimeter. These readings should be approximately as follows:

- TP1 — 0V
- TP2 — +5V
- TP3 — +12V
- TP4 — -12V

If all is well, switch off the VIC and remove the interface card. Wire the board to the data set. Reconnect to the VIC, switch both the VIC and data set on, and type in program A. Run the program, and the receiving party should receive the message 'the quick brown fox jumps over the lazy dog' continuously. Also included is a program to make the VIC act like a 'dumb terminal', for use with a modem, to call information and ordering services such as the Maplin on-line computer, South-end (0702) 552941.

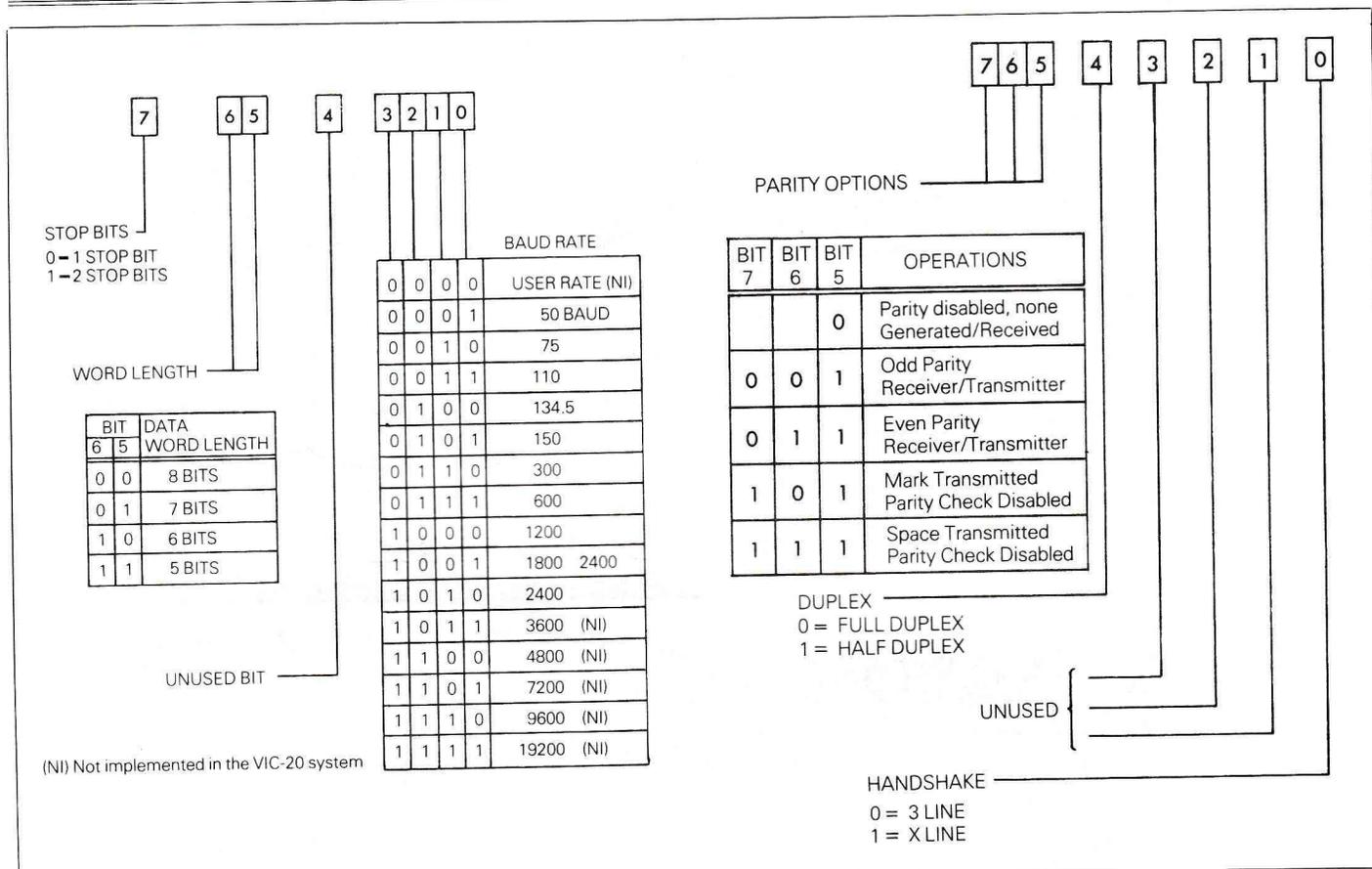


Table 1. Function of bits in the VIC RS-232 Control Register

Table 2. Function of bits in the VIC RS-232 Command Register

```

10 REM***PROGRAM A ***
20 OPEN200,2,0,CHR$(166)+CHR$(0)
30 PRINT#200,"THE QUICK BROWN FOX JUMPED OVER THE LAZY DOG."
40 GOTO30

```

```

0 REM*****          * V.D.U. PROGRAM*          *****
1 POKE36879,8:PRINTCHR$(5):WAIT 203,64
5 POKE36876,200:PRINTCHR$(147);" VIC 20 V.D.U. PROGRAM"
10 R#=CHR$(166)+CHR$(0)
20 OPEN200,2,0,R#
25 IFPEEK(203)<>64THEN500
30 GET#200,A#
35 IFA#=""THENGOTO25
40 IF ASC(A#)>95THENGOTO25
50 IF A#=CHR$(13)THENPRINTA#;:GOTO25
60 IF ASC(A#)<32THENGOTO25
70 PRINTA#;:GOTO25
500 POKE203,64:GETS#
510 IFS#=CHR$(17)THENS#=CHR$(10)
520 IFS#=CHR$(19)THENS#=CHR$(140)
530 PRINT#200,S#;:POKE203,64:S#="" :GOTO30

```

PARTS LIST FOR VIC 20 RS232 INTERFACE

Resistors - All 0.4W 1% Metal Film unless specified

R1,2,3,4,5,6,7,8,9, 10,11,12,13,14,15, 16,33,34,35,36	4k7	20 off	(CM4K7)
R17,18,19,20,25, 26,27,28	10k	8 off	(M10K)
R21,22,29,30	2k2	4 off	(M2K2)
R23,24,31,32	330R	4 off	(M330R)
R37	47R (1/2W carbon)		(S47R)

Capacitors			
C1,2	470µF 16V P.C. Electrolytic	2 off	(FF15R)
C3	100 µF reversolytic		(RK83E)

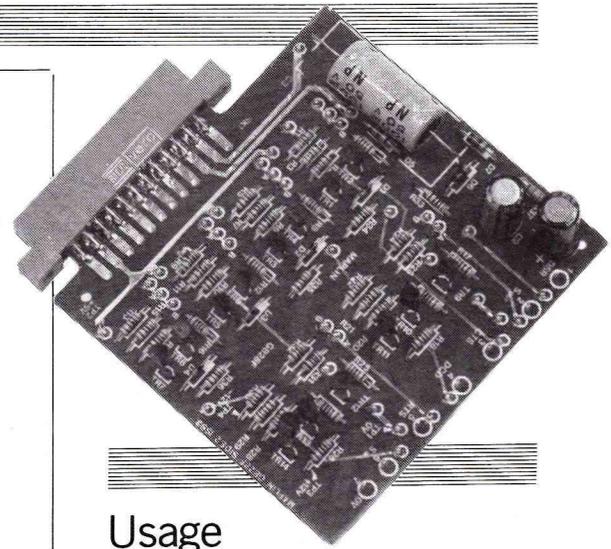
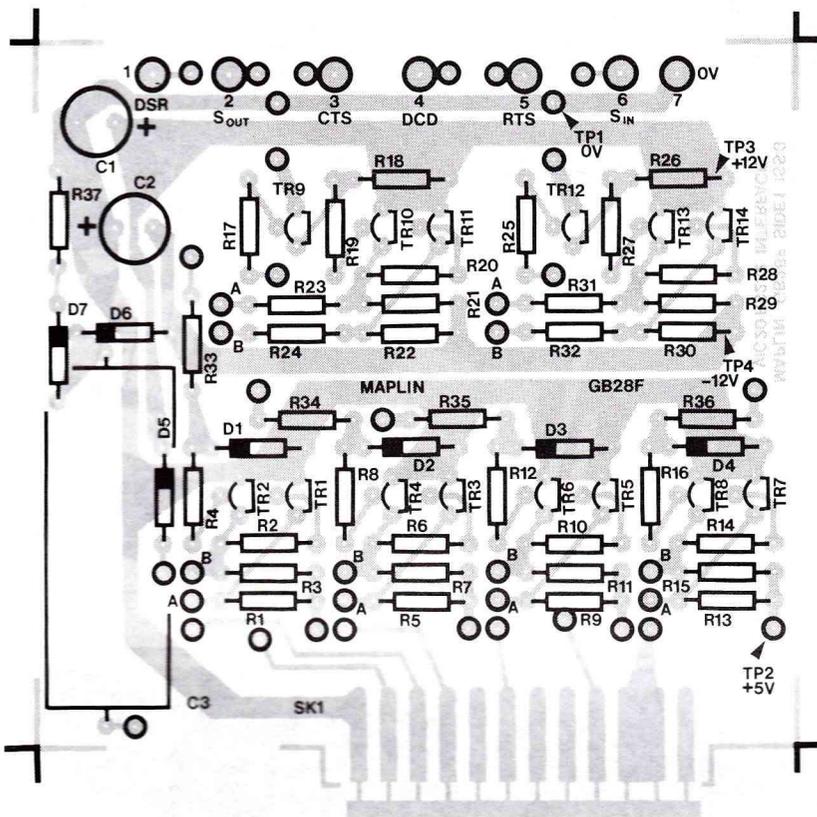
Semiconductors

D1-4 inc.	1N4148	4 off	(QL80B)
D5-7 inc.	1N4001	3 off	(QL730)
TR1-9 inc., 12	BC548	10 off	(QB73Q)
TR10,11,13,14	BC327	4 off	(QB66W)

Miscellaneous

SK1	P.C. Edgecon 2 x 12 way		(BK74R)
	Veropin 2141	1 Pkt	(FL21X)
	Track Pin	1 Pkt	(FL82D)
	P.C.B.		(GB28F)

A complete kit of all parts is available.
Order As LK11M (VIC20/RS232 Interface Kit).



Usage

To use the RS232 serial data port on the VIC the channel must first be opened as a file, specifying Baud rate (speed), number of bits per character, number of stop bits, and odd/even or disabled parity bit. This information is given by two characters after the 'OPEN' command in the form:

OPEN LF,2,0,A\$. Where LF is the logical file number, i.e., any number between 1 and 255 (if LF is greater than 127, then linefeed follows carriage return), and A\$ is two characters sent to control register and command register, the functions of which are explained in tables 1 and 2. So, for example, we can see that to set Baud rate to 300, 7 bits per character, 2 stop bits, and no parity, the OPEN command would be:

```
OPEN 200,2,0,CHR$(166)+CHR$(0).
Having opened the RS232 channel,
data is sent and received using
'PRINT LF,DATA $' and 'GET LF,DATA $'.
```

Note: To type 'PRINT' do not use the abbreviation '?'. Instead, use 'P shift R' followed by logical file number etc. It is possible to list through the RS232 port, to send a program to a friend for instance, by typing 'CMD LF : LIST', where LF=logical file number.

Remember when programming that the VIC allocates two 256 byte buffers (for transmit and receive) in the 506 bytes below RAMTOP, so there is less memory available to BASIC. Also 'DIM' statements or variables should be left until after the 'OPEN' command, as the computer performs an automatic 'CLR' before allocating the buffers.

Bibliography:

VIC Revealed by Nick Hampshire
VIC Programmers Reference Guide, Commodore

Connecting to the Maplin Modem

With reference to Figure 5, page 4, Project Book 5, the following connections should be made:

VIC 20 Interface	Maplin Modem
pin 2 (S _{OUT})	to pin 17 (RS232 IN)
pin 6 (S _{IN})	to pin 10 (RS232 out)
pin 7 (S _{GROUND})	to pin 21 or 22 (S _{GROUND})

Ensure that the link on the Modem is in the RS232 position.

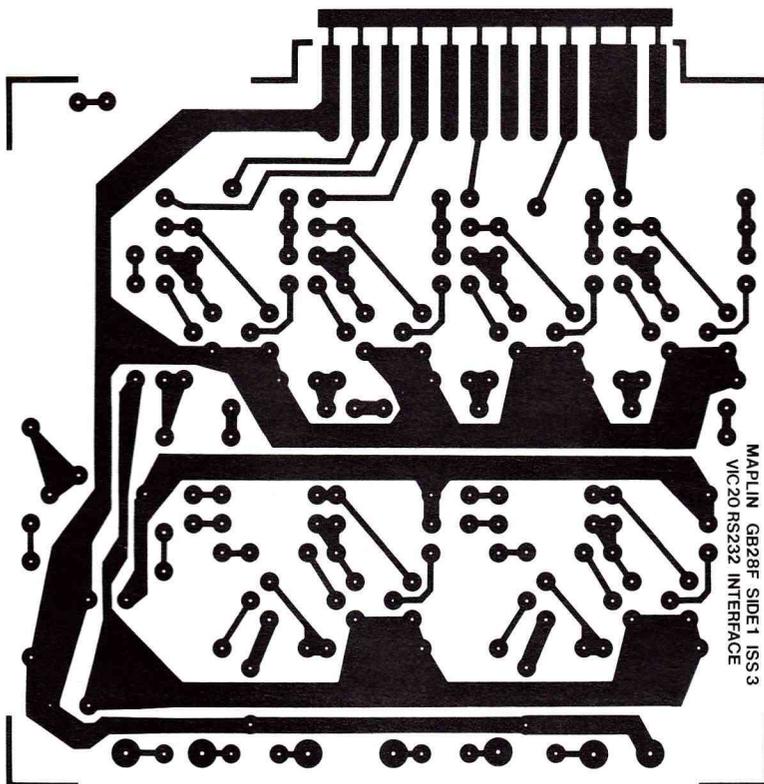
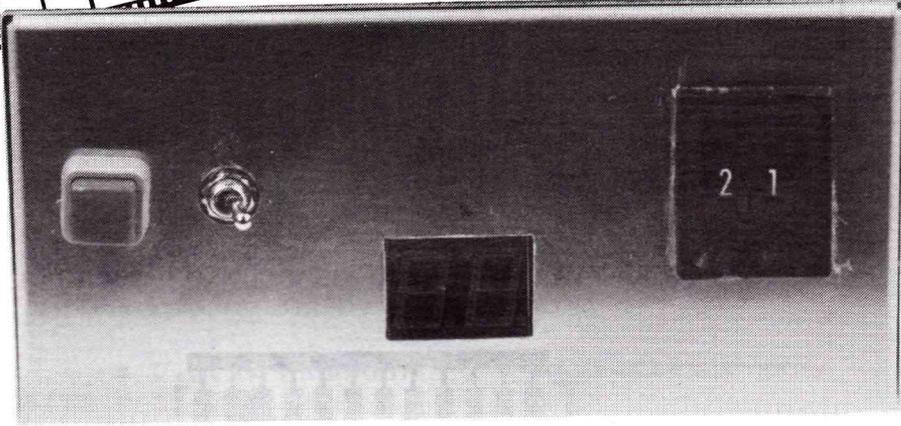


Figure 2. PCB layout

DIGITAL ENLARGER TIMER/ CONTROLLER



by David J. Silvester

Reversal colour printing does not permit the use of a safelight, whilst the safelight for negative colour work is so dim as to make exposure timing with a clock almost impossible. The only enlarger timers for sale were of a mechanical type and it was felt that using CMOS logic a suitable timer could be made at a cost below that of the 'off the shelf' item.

Given that the timer must be operated by feel alone the controls were reduced to a thumbwheel 'time set' switch and two control switches. This introduces two possible methods of operation. The timer may either count the elapsed time up or down, and it was felt that the up counting system which allows the time display to show the exposure time before operation would prevent the author from making too many exposure errors. The disadvantage is that when the timer is switched on or the thumb-wheel switches are altered the enlarger lamp will turn on until the display shows the same figures as the thumbwheel switch. Normally, however, more time is taken in preparing the darkroom or setting up the next print, so that in practice no time is actually lost.

Circuit Description

The main timing of the unit is derived from the 50Hz mains frequency via the transformer T1. Diodes D1, D2, capacitors C1, C2 and voltage regulator REG1 provide the 12 volt power supply, which is applied to all the IC's. The +12V is attached to the highest numbered pin of the IC's (14 or 16) and the 0V to the diagonally opposite pin (7 or 8). In all cases unused inputs must be connected to either high or low supply to ensure correct operation or freedom from oscillation.

The timing pulses are derived from the 15V/50Hz output of T1, ie. approximately 21V peak to peak. The zener diode D3, fed via R1, clips this voltage to +12V when the input is positive and to -0.6V when the input is negative. This clipped sine wave is then applied to a schmitt trigger IC1a, which provides a square wave at 50Hz with short rise and fall times on the logic transitions. This 50Hz square wave is fed to IC2a connected with IC3c and IC3d to act as a divide by 5 counter. IC2 has outputs in BCD (binary coded decimal) which will normally count from 0 to 9 (0000 to 1001) but at a

count of 5 (0101) IC3 resets the counter immediately to 0. In this way after every 5 input cycles the output of IC3c connected to the reset pin of IC2a, gives a single short pulse every 0.1 seconds.

The connections for the operating switches S1 and S2 pass through IC1b and IC1d to provide the logic levels required for the operation of the counter reset and output logic stages.

The 10 pulses per second from IC3c pass through a count inhibit circuit IC10a and then to IC2b which produces 1 pulse per second when input 1 of IC10a is high. IC4 acts as a 00 to 99 counter with BCD output lines. This BCD data is used to drive a 7 segment double digit display, via display drivers IC5 and IC6. It should be noted that the ballast resistors used with the display are of unusually high values (R4-17) so that the display will show only a dull glow in the darkroom.

IC's 7, 8 and 9 provide a system which checks whether the BCD data on the output of IC4 and from the BCD thumbwheel switches S3 and S4 are the same. IC7 and IC8 are quad exclusive NOR gates which act as comparators for each of the BCD data line pairs.

- ★ Accurate to 0.1 seconds
- ★ Timing range of 1 to 99 seconds
- ★ Cost below that of mechanical timers
- ★ Switching capability of 6 amps at 240V 50Hz

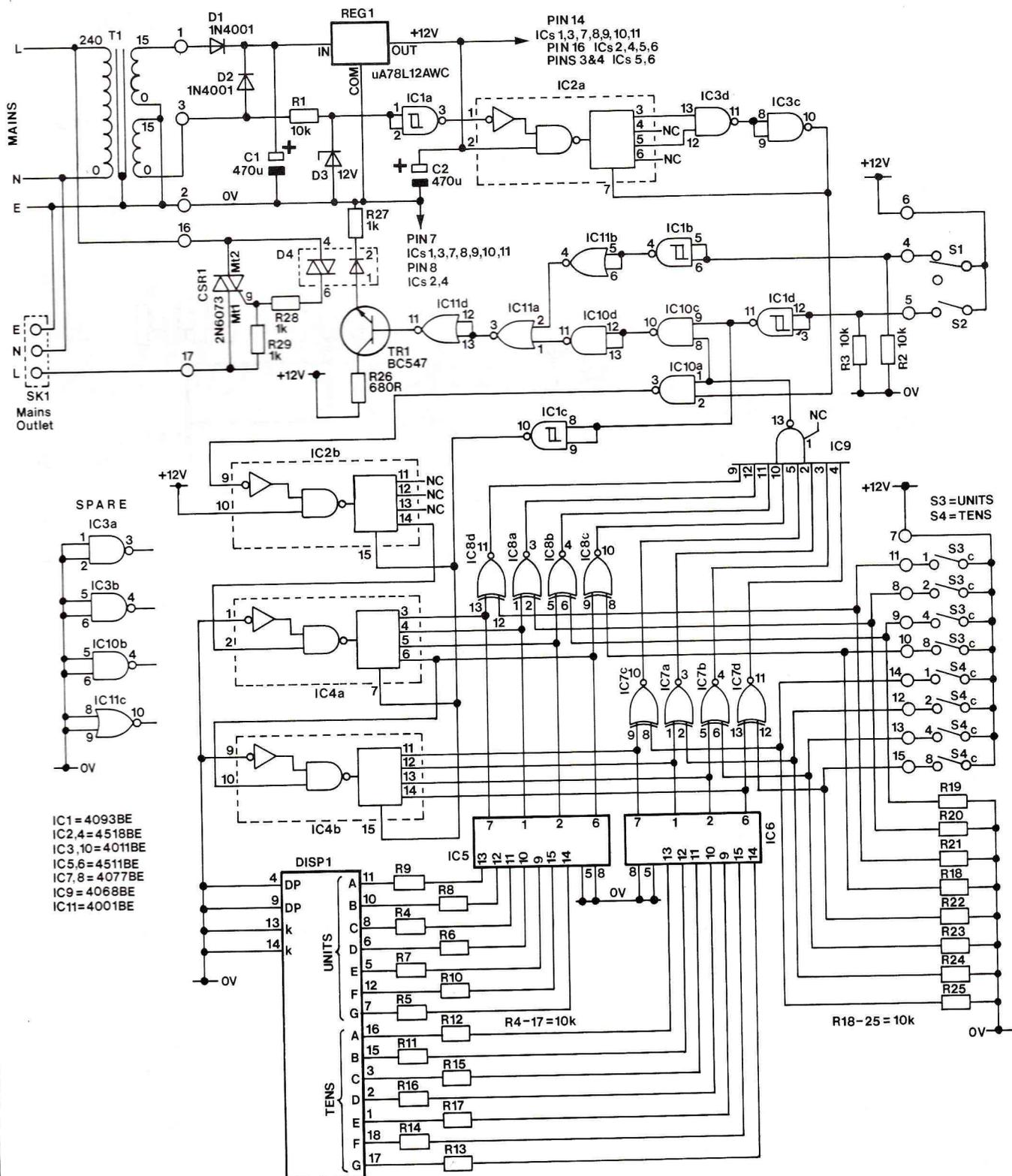


Figure 1. Circuit diagram.

When the values of BCD input are the same the output is high. IC9 is an 8 input NAND gate giving low output on pin 13 only when all of the 8 BCD input pairs are the same. It is this output which controls the counting and also the output circuitry when S1 and S2 are in their off positions. The output of IC9 is over-ridden by the logic levels derived from S1 or S2 when either switch is used.

The output logic circuit consists of IC11d, IC11a, IC11b, IC1b, IC10c, IC10d, IC1d, and TR1 which cause the opto-coupler diode to turn the output triac CSR1 on under the following conditions:—

1. If the system is counting, i.e. if pin 13 is high
2. If S2 is turned on, i.e. the input to IC1b is high.

If S1 is pushed the logic prevents the counter from operating and holds the triac off whilst resetting the counter to zero.

Assembly

Construction of the timer should cause no problems as all the components except for the switches, transformer and output socket are fixed to the PCB. The board is double sided and all components are mounted on side 2 of the board with most soldering carried out on side 1.

Insert the vertisocket into the board first as this will help with the identification of the other component locations, and solder into position noting that pins 1, 3, 6 and 8 going to resistors R8, R10, R11 and R13 must be soldered to both sides of the board. Insert and solder all of the IC sockets checking carefully the position of pin 1 as the IC's point in different directions, but DO NOT INSERT IC's.

Bend, insert and solder all of the resistors into their places noting that R8, R10, R11 and R13 will be soldered to both sides of the board, followed by capacitors C1 and C2. Next insert the opto-coupler, transistor, triac, regulator, and diodes and after checking orientation solder into place.

Attach a 30cm length of ribbon cable to the output holes for S3 and S4 and the 12V line on the right hand side of the board. It will be found that there is one spare wire and this may be pulled away from the rest of the ribbon cable. Then add further wires for the transformer, S1 and S2 connections, and short pieces of hook up wire to the mains input and output connections. If the board is now held up to the light there can be seen a large number of holes remaining and the track pins are inserted into these holes and soldered on both sides. If all of the pins are inserted before soldering it is very likely that a pin will be left unsoldered on one side of the board and this will cause problems later on. Personal experience has shown that it is best to insert about 6 pins and then count the solder joints being made on both sides of the PCB.

Assemble the thumbwheel switch from the component parts and identify

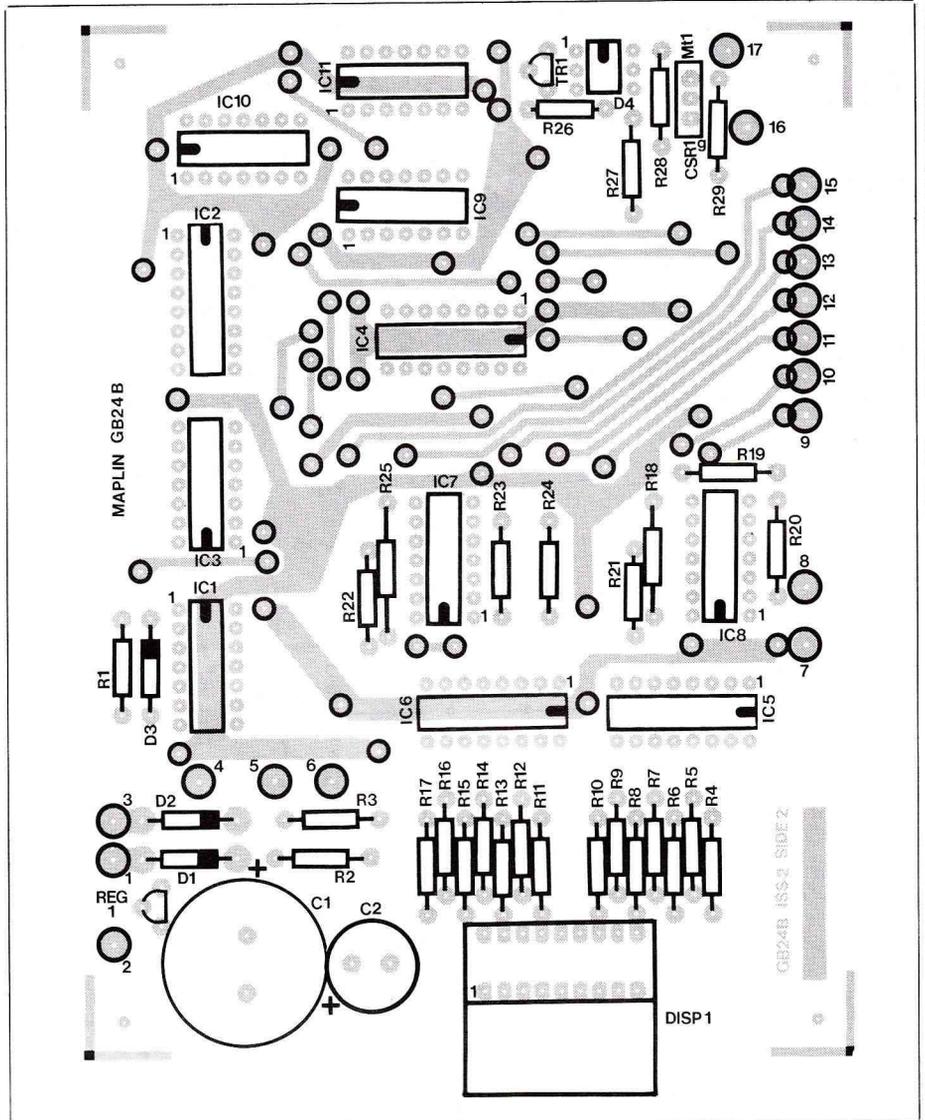


Figure 2. PCB layout.

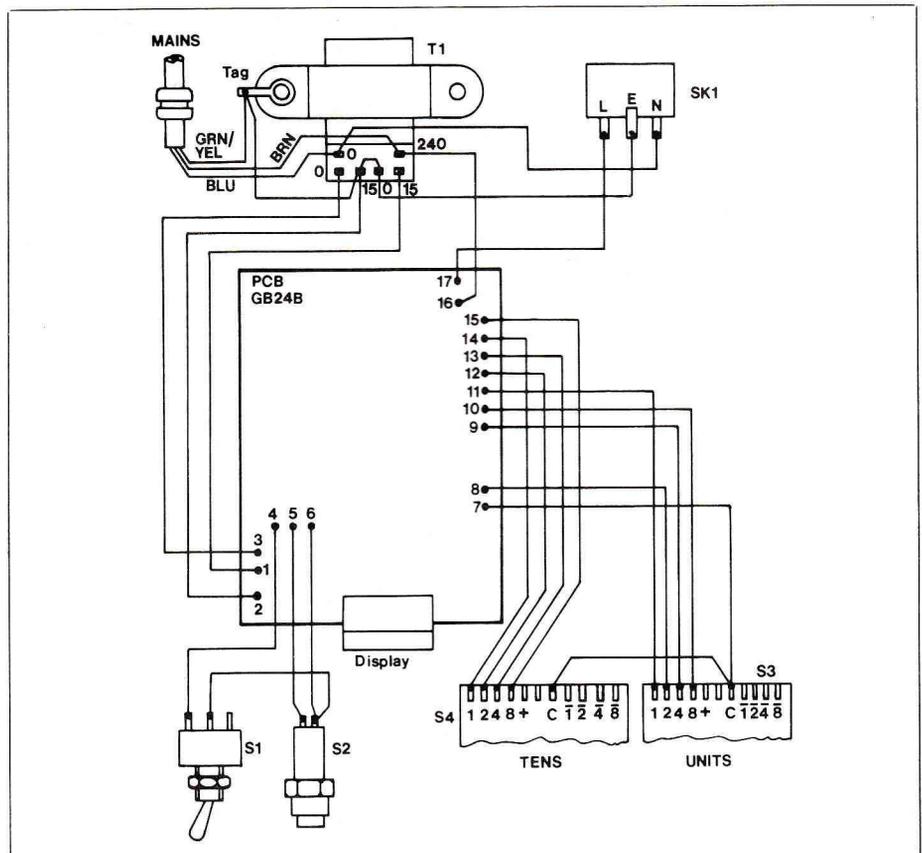


Figure 3. Interwiring diagram.

the 8, 4, 2 and 1 switch contacts as well as the common line C.

A suitable case should be chosen and drilled or cut to take the PCB with cut-out for the display, thumbwheel switch, Euro outlet, transformer, mains input grommet, and switches S1 and S2.

After mounting all of the components in the case connect these as shown in the wiring diagram Figure 3. The mains input earth MUST be connected securely to the metal case and to the Euro socket as failure to do this will make the timer dangerous to use in the wet atmosphere of the darkroom.

Circuit Testing

Insert a 3A fuse into the mains input plug. The constructor should remember that the large PCB carries mains voltages so extreme care should be taken whilst testing the circuits. First, and before inserting the IC's check that the 12V power supply is operating correctly by checking the voltage

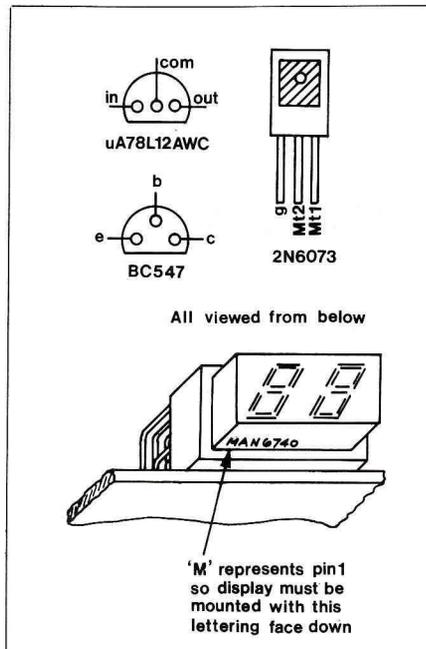
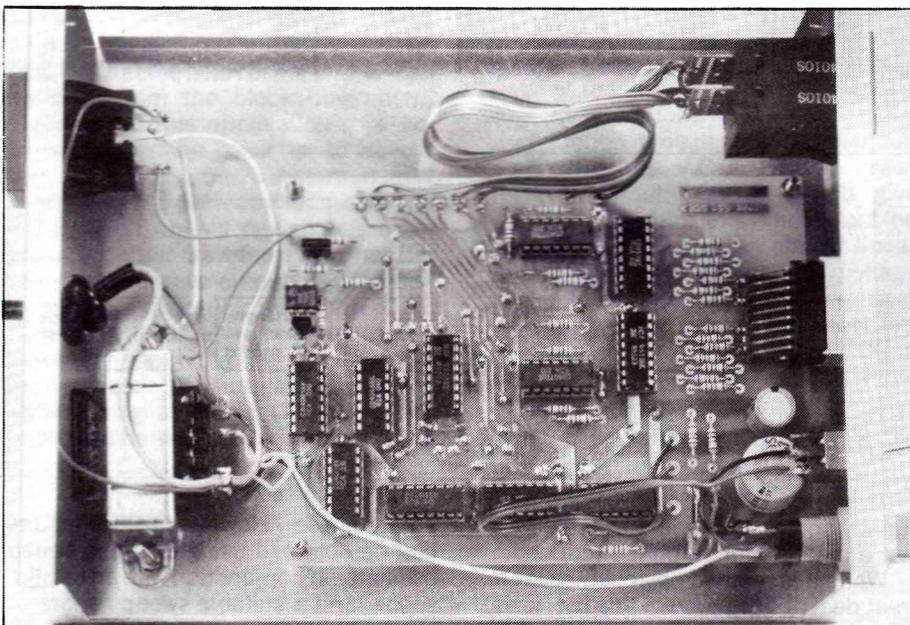


Figure 4. Pin configurations.



across pins 7 and 14 of IC1 socket.

Switch off and remove the mains plug. Insert all of the IC's and turn on again. The LED display should light (note the intensity of the lamps is low), count up to the number set on the thumbwheel switch at one count per second, and then stop. Also check that the thumbwheel switch has been connected correctly by making the counter stop at 0, 1, 2 to 9 and 10, 20 to 90 seconds. Finally pull out the mains plug and check that none of the components has become hot. Now connect a 100W/240V bulb across the output socket and repeat the above. During counting the lamp should light and go off when the count stops. Set S2 to the on position, the lamp should light but the display remain at the same setting. Press S1 and the display should reset to zero but the lamp remain off. Releasing the switch will allow the lamp to light for the required time.

Using the Timer

If all tests have proved satisfactory connect the timer to the enlarger, and set up the darkroom. Set the thumbwheel switch to the desired exposure time and switch S2 on, to prevent the lamp turning off whilst trying to set up the negative and baseboard. When you are ready, switch S2 on, place photographic paper in the baseboard, then press S1 and release to make the exposure.

Modifications Outside Great Britain

In countries with a mains frequency of 50Hz only T1 will need to be changed to a transformer having an input winding suitable for the local voltage.

In countries with 60Hz mains frequency the constructor must break the connection between IC2 pin 3 and IC3 pin 13. A new connection must be made between IC2 pin 4 and IC3 pin 13.

ENLARGER TIMER PARTS LIST

Resistors — All 0.4W 1% metal film.

R1-25 inc 10k 25 off (M10K)
R26 680R (M680R)
R27,28,29 1k 3 off (M1K)

Capacitors

C1 470uF 63V PC electrolytic (FF59P)
C2 470uF 16V PC electrolytic (FF15R)

Semiconductors

D1,2 1N4001 2 off (QL73Q)
D3 BZY88C12V (QH16S)
D4 Opto-triac-isolator (QQ10L)
CSR1 2N6073 (QR51F)
REG1 uA78L12AWC (WQ77J)
TR1 BC547 (QQ14Q)
IC1 4093BE (QW53H)
IC2,4 4518BE 2 off (QX32K)
IC3,10 4011BE 2 off (QX05F)
IC5,6 4511BE 2 off (QX31J)
IC7,8 4077BE 2 off (QW47B)
IC9 4068BE (QX24B)
IC11 4001BE (QX01B)

Miscellaneous

DISP1 DD Display Type C (BY68Y)
Vertisocket Type 2 (BK04E)

14 Pin DIL Skt 7 off (BL18U)
16 Pin DIL Skt 4 off (BL19V)
Veropin 2141 1 pkt (FL21X)
Track Pin 2 pkts (FL82D)
Transformer 15V (WB15R)
Sub-Min Toggle A (FH00A)
Square Push Red (FF98G)
Thumbwheel BCD 2 off (FF84F)
Thumbwheel End Cheeks (BK49D)
Grommet (FW59P)
Euro Facility outlet (HL42V)
Euro Facility plug (HL43W)
10-way Ribbon cable 1 metre (XR06G)
Min Mains Black 2 metres (XR01B)
Hook up wire 1 pkt (BL00A)
Case AB15 (XB71N)
PCB (GB24B)
Screws 6BA x 1 inch 1 pkt (BF07H)
Nuts 6BA 1 pkt (BF18U)
Spacer 6BA x 1/2 inch 1 pkt (FW35Q)
Screws 4BA x 1/4 inch 1 pkt (BF02C)
Nuts 4BA 1 pkt (BF17T)
Tag 4BA 1 pkt (BF28F)
Stick-on-feet (FW38R)

A complete kit of all parts, excluding the case, is available.
Order As LK07H (Enlarger Timer kit).

A SIMPLE SWEEP OSCILLATOR

by Robert Penfold

For frequency response measurements most electronics enthusiasts use an audio sinewave generator plus an A.C. millivoltmeter or some other piece of equipment capable of measuring audio frequency signals. A quicker way of obtaining audio frequency response graphs is to use a sweep oscillator plus a pen recorder. Here the audio oscillator is automatically swept up through the entire audio frequency band while the pen in the recorder responds to the output signal level from the equipment under test. As the oscillator is swept upwards in frequency the paper is moved past the pen so that the required frequency response graph is drawn out, and units of this type normally have the X and Y axes accurately calibrated in terms of fre-

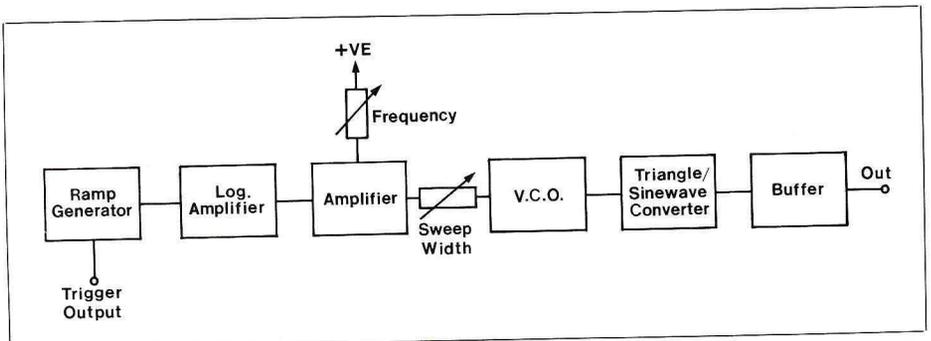


Figure 1. The simple sweep generator block diagram.

quency and relative gain in decibels so that a meaningful graph is produced.

While this method obviously saves a great deal of time by avoiding the need to write down numerous results and then (if necessary) draw a graph on the basis of these, the cost of such equipment makes it impractical for the

amateur user. However, useful results can be obtained using a simple sweep oscillator in conjunction with an oscilloscope, and a suitable sweep generator can be built at quite a modest cost. With this system the Y input of the oscilloscope is fed with the output of the equipment under test, and the spot is

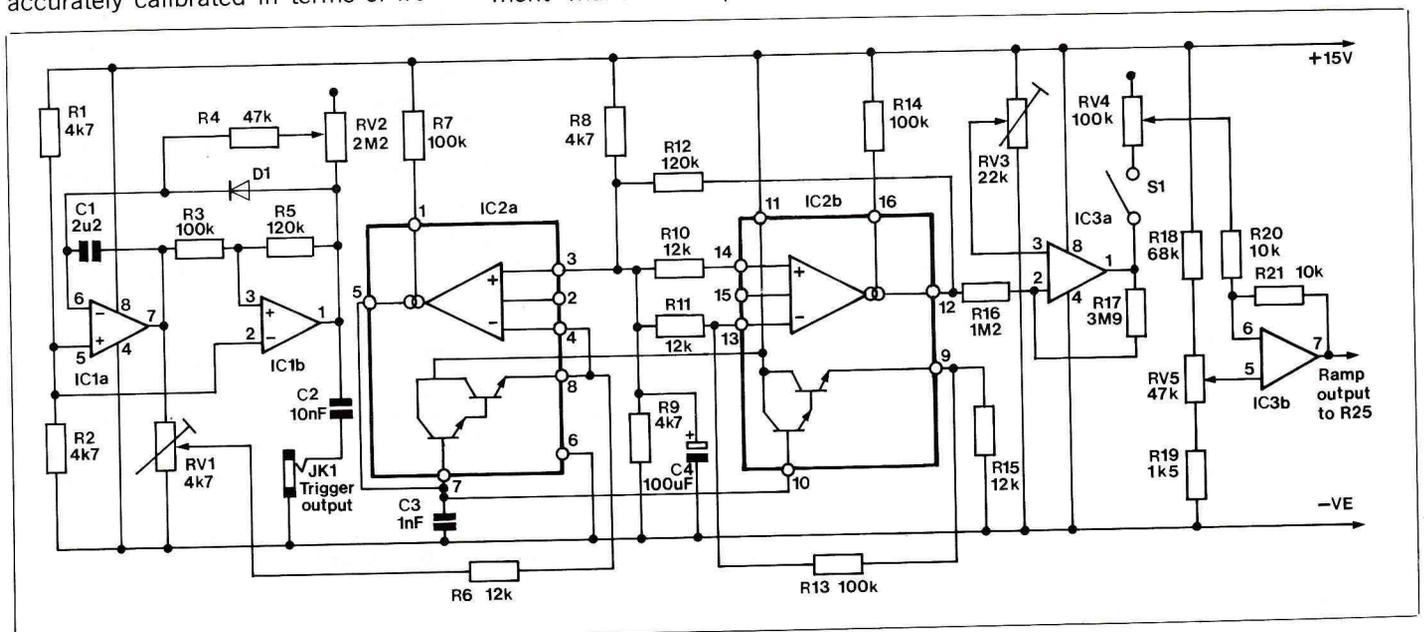


Figure 2. The ramp generator and log amplifier circuits.

swept across the screen as the oscillator is swept over the audio frequency range. The spot can either be swept across the screen using triggered sweep with the trigger signal being obtained from the sweep oscillator, or the ramp signal from the sweep oscillator can be fed to the X input of the oscilloscope.

This gives what is only a comparatively crude representation of the frequency response of the equipment under investigation, but the results obtained are perfectly adequate for making quick checks on tone controls, equalisation amplifiers, testing for irregularities in filter responses, and so on. If necessary, checks using the sweep oscillator and oscilloscope can be followed up by detailed measurements using an ordinary sinewave generator and a millivoltmeter. The accompanying oscillographs show a few examples of results obtained using the simple sweep oscillator featured in this article.

Block Diagram

A voltage controlled oscillator (V.C.O.) is at the heart of the unit, as can be seen from the block diagram of Figure 1. In this application it is not necessary for the oscillator to have a very pure output, and a distortion level of around 2% is perfectly adequate. The V.C.O. used in this design has a triangular output waveform and not the required sinewave output, and the distortion on a triangular waveform is too high to give really good results. A triangular waveform can be converted to a reasonable sinewave signal by either using a filter to attenuate the unwanted harmonics, or by using a soft

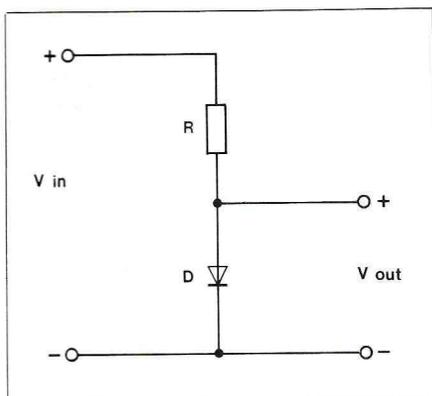
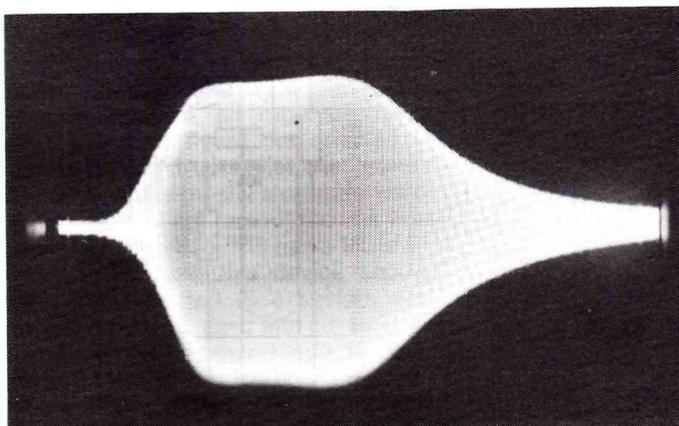
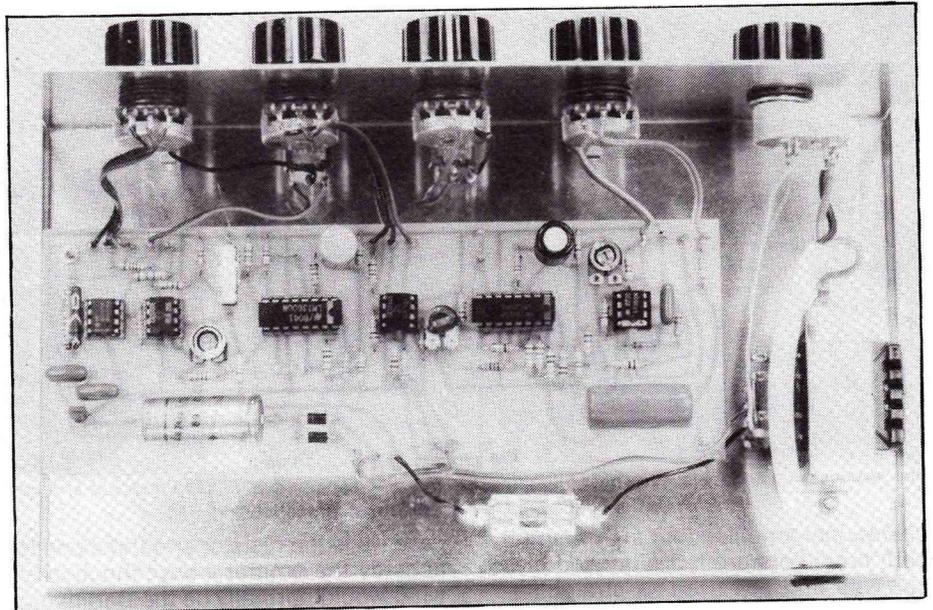


Figure 3. The basis of a log amplifier.



The response of a speech processor having high and low pass filters.



clipping circuit to round off the waveform to give the desired shape. In this circuit a soft clipping circuit is used, and one of the oscillographs shows the effect of this circuit. A buffer stage is used at the output of the unit to give a low output impedance.

Although it might at first appear that controlling the V.C.O. from a linear ramp (sawtooth) signal would give acceptable results, this is not in fact the case. The V.C.O. has an almost linear relationship between control voltage and output frequency, and the output frequency would therefore increase in a linear fashion using a linear ramp waveform as the control signal. Audio frequency response graphs are normally drawn with a logarithmic frequency scale so that (for example) 50Hz to 100Hz occupies the same space as 500Hz to 1kHz and 5kHz to 10kHz. Using a logarithmic frequency scale rather than a linear one gives results that are much clearer and easier to interpret, and ideally a sweep oscillator should have a logarithmic frequency scale.

A suitable sweep waveform is obtained by first generating a linear sawtooth waveform and then feeding this to a logarithmic amplifier which provides suitable shaping of this signal. One of the accompanying oscillographs shows the processed and unprocessed ramp waveforms.

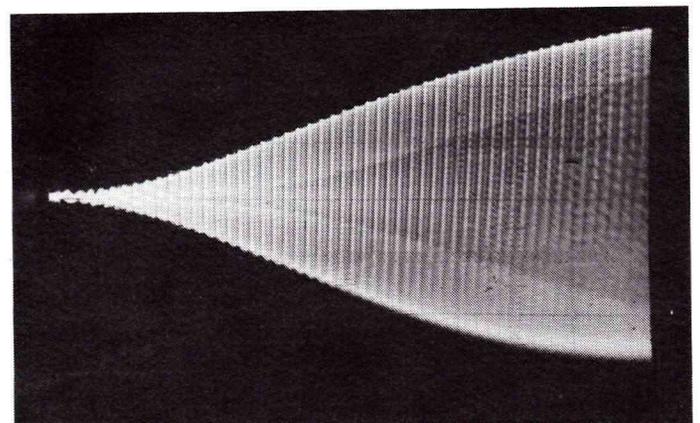
An amplifier is used to boost the output from the logarithmic amplifier to a suitable level, and this represents a convenient point in the unit to add frequency and sweep width controls.

The Circuit

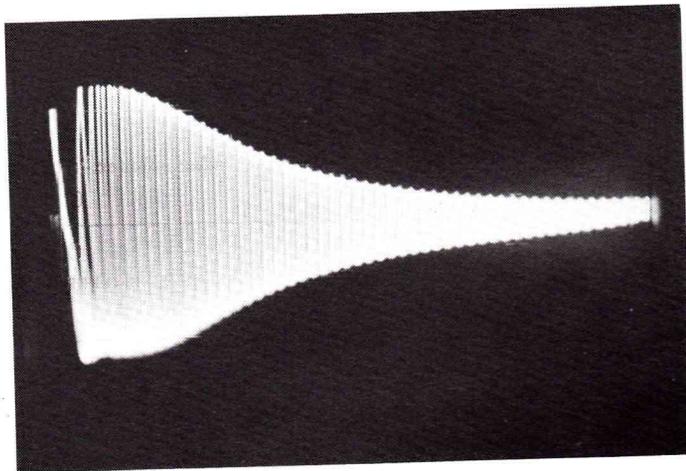
Figure 2 shows the circuit diagram of the ramp generator, logarithmic amplifier, and amplifier stages of the unit.

The ramp generator uses what is almost the standard triangular and squarewave generator circuit with IC1a acting as the integrator and IC1b operating as the trigger circuit. However, the inclusion of D1 in the charge path of C1 results in C1 charging almost instantly, giving a sawtooth waveform rather than a triangular output at the output of IC1a. RV2 controls the discharge time of C1 and acts as the sweep frequency control. This gives a frequency range of approximately 0.2Hz to 10Hz. The output waveform IC1b is a brief positive pulse, and this is used as the trigger signal for the sweep generator of the oscilloscope. The output from IC1a could be fed to the X input of the oscilloscope, but there could be problems in interfacing this signal to the X input. Using the triggered sweep method of operation should give good results with virtually any oscilloscope and is not difficult to set up.

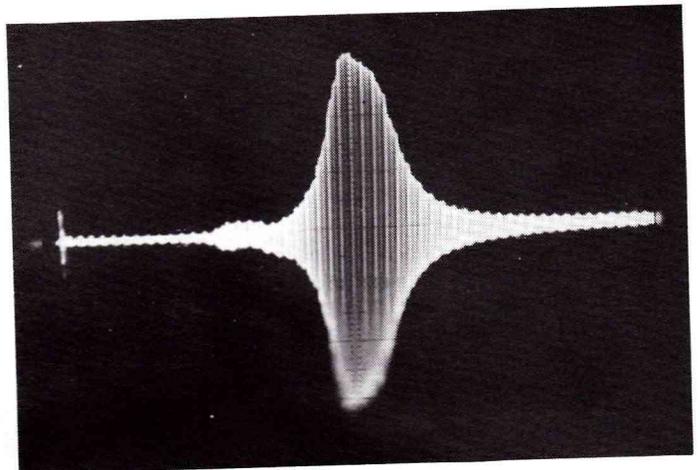
IC2 is a dual transconductance



The response of a 6dB/octave high pass filter.



The response of a 6dB/octave low pass filter.



The response of a narrowband bandpass filter.

operational amplifier, but in this circuit both amplifiers are fed with fixed bias currents and are used as straightforward operational amplifiers. These are used in the logarithmic amplifier, and Figure 3 shows the basic circuit which is invariably used in amplifiers of this type. This is simply a forward biased silicon diode, and this provides an output voltage of about 0.6 volts or so provided the input voltage is at about this figure or higher. Although this circuit is often used as a simple voltage stabiliser there is some change in output voltage with variations in input potential. In fact, raising the input voltage by a factor of ten gives an increase in the output voltage of about 100 millivolts, and successive increases in the input potential give an almost identical rise in the output voltage.

This gives a good logarithmic response, but the gain of the circuit is reducing with increased input voltage, whereas this application requires a circuit which gives increased gain with rising input potential. The necessary transformation is obtained by using the resistor and diode in the negative feedback circuit of an amplifier. In this

case R6 is the resistor and the diode is actually the emitter - base junction of what would normally be the Darlington Pair output buffer stage of IC2a.

Apart from bias current, the voltage across a forward biased semiconductor junction also varies significantly with changes in temperature, and the logarithmic amplifier incorporates a temperature compensation circuit to minimise drift. IC2b and its Darlington Pair are used to provide this temperature compensation, and excellent results are obtained since the amplifier and compensation components are on the same chip and are therefore maintained at the same temperature.

IC3a is used as a simple inverting amplifier which boosts the output from the logarithmic amplifier by a factor of just over three times. IC3b is used as an inverting amplifier which converts the negative ramp output of IC3a back to the required positive ramp signal. The closed loop voltage gain of IC3b can be varied from unity with RV4 at minimum value down to a loss of over 20dB with RV4 at maximum value, and this enables the sweep range to be adjusted. S1 enables the ramp signal to be disconnected from the V.C.O. so that

the oscillator can be used at a fixed frequency which is set using frequency control RV5.

V.C.O. Circuit

The circuit diagram of the V.C.O., waveform shaper and output stages of the unit are shown in Figure 4. The V.C.O. uses IC4a to charge and discharge C5 at a constant rate, and IC4b is used as a trigger circuit. The charge and discharge current of C5 (and the operating frequency of the V.C.O.) is controlled by the bias current fed to pin 16 of IC4a. A resistor is used in series with this input so that voltage rather than current controlled operation is obtained, and this resistor is fed from the output of IC3b. The V.C.O. provides two output waveforms; a roughly squarewave signal at the output of IC4b, and a good quality triangular waveform at the output of IC4a.

It is the triangular waveform that is used in this application, and it is fed to IC5 which is used as a triangle to sinewave converter. IC5 is another operational transconductance amplifier, and it is used here as a fixed gain amplifier which is overdriven by the triangular input signal. Unlike most

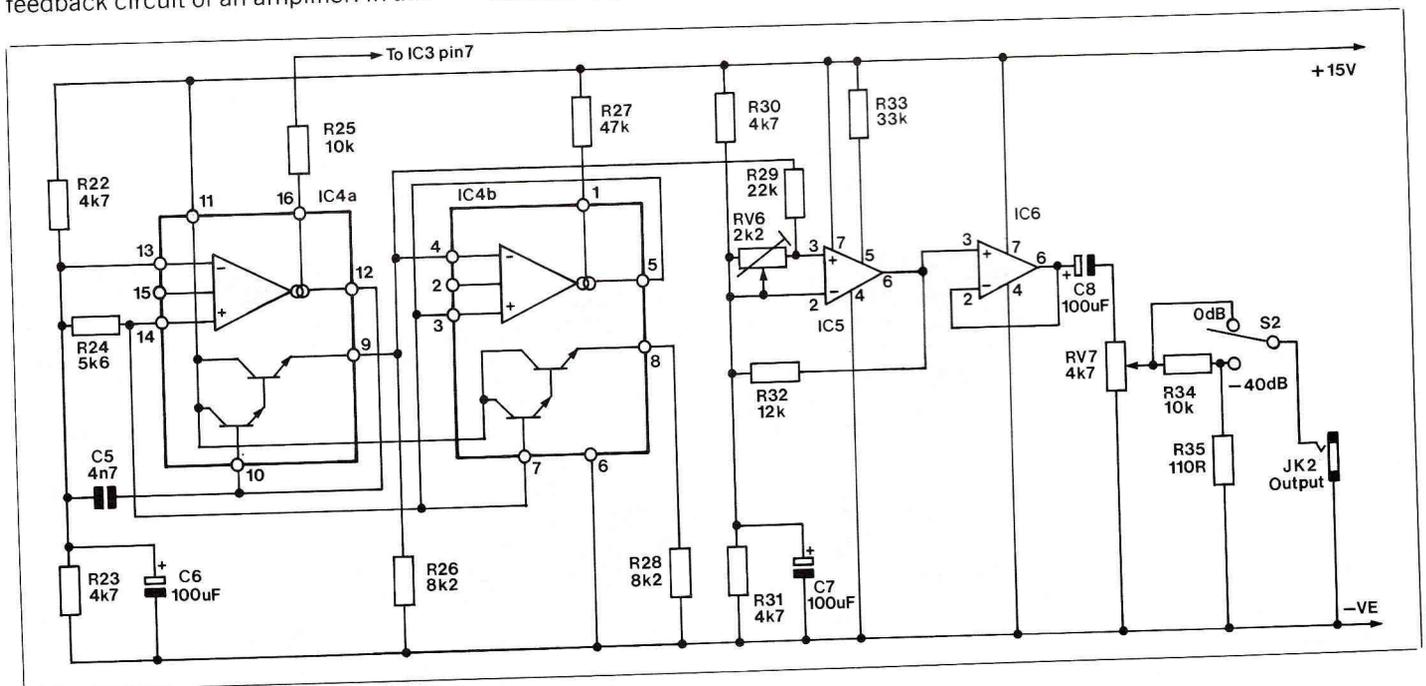
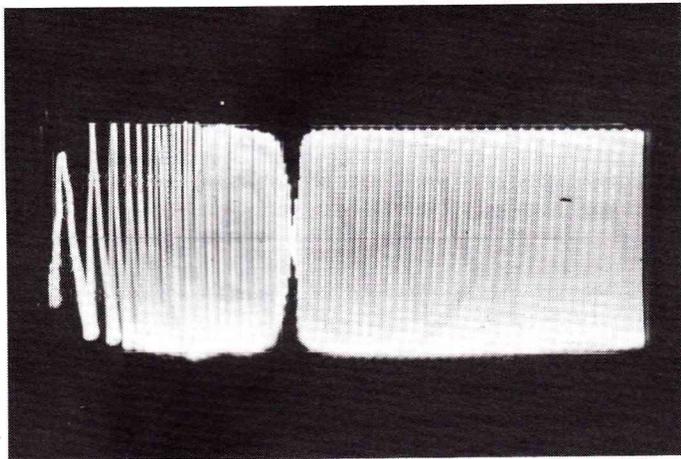
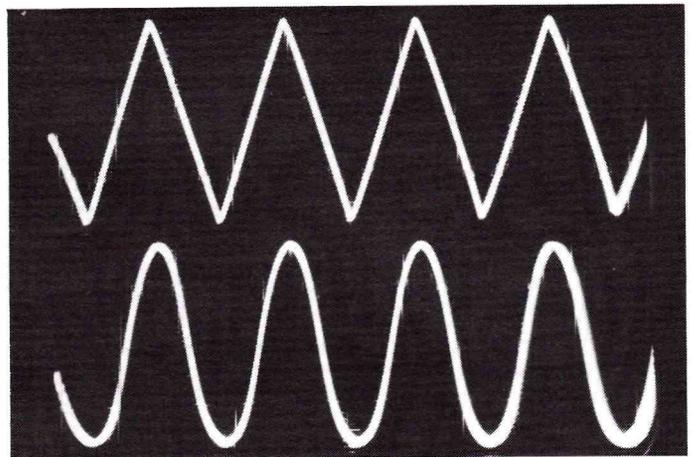


Figure 4. The VCO, waveform converter, and buffer amplifier circuits.



The response of a notch filter.



Top: The triangular output of the V.C.O.
Bottom: Output of the triangle/sine converter.

amplifiers, which provide hard clipping, an overdriven transconductance amplifier gives soft clipping, and in this case gives the required rounding of the input signal. RV6 is adjusted to give the best possible output waveform.

As the output impedance of IC5 is fairly high, IC6 is used as a straight forward unity gain buffer stage at the output. RV7 is the output level control, and S1 can be adjusted to reduce the output signal by about 40dB (by a factor of one hundred times). This makes it easier to adjust RV7 for very low output levels. The maximum output signal level is approximately ten volts peak to peak.

Mains P.S.U.

The unit requires a supply voltage of between about 12 and 18 volts, and a suitable 15 volt stabilised power supply circuit is given in Figure 5.

This is a straight forward circuit using a push-pull rectifier and a three terminal monolithic voltage regulator. A small (100mA) voltage regulator is more than adequate since the supply current is only about 15mA. C9 is the smoothing capacitor and C10 plus C11 are needed to aid the stability of voltage regulator IC7.

Construction

A metal instrument case which has approximate outside dimensions of 229 by 133 by 63.5mm is ideal for this project. The general layout of the front panel can be seen from the photographs, and the final wiring of the unit will be more straight forward if this layout is not radically altered.

Apart from T1, FS1, and the components fitted on the front panel, the components are all mounted on a printed circuit board, as detailed in Figure 6. Construction of the printed circuit board is mostly straightforward, but be careful not to omit the link wire (next to R28). Also, IC3 has a MOSFET input stage, and this device should therefore be fitted in a socket, and should not be plugged into circuit until the board is in other respects complete. Fit Veropins to the board at points where connections to the controls and other off-board components will eventually be made.

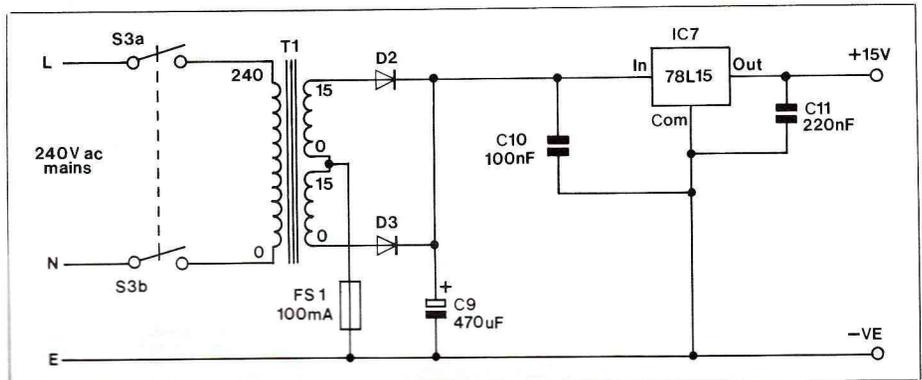


Figure 5. Mains power supply circuit.

The completed board is mounted on the base panel of the cabinet, on the right hand side, leaving space for T1 to be mounted on the left side of the board. The component panel is mounted using one inch 6BA bolts plus ½ inch 6BA spacers. The fuseholder for FS1, and T1 are both mounted using ¼ inch 6BA bolts. The mounting screws for the top and sides section of the case protrude about ½ inch into the case, and T1 must be positioned where it will not obstruct one of these fixing screws.

An entrance hole for the mains lead is made in the rear panel of the case near to T1, and this hole is fitted with a small grommet.

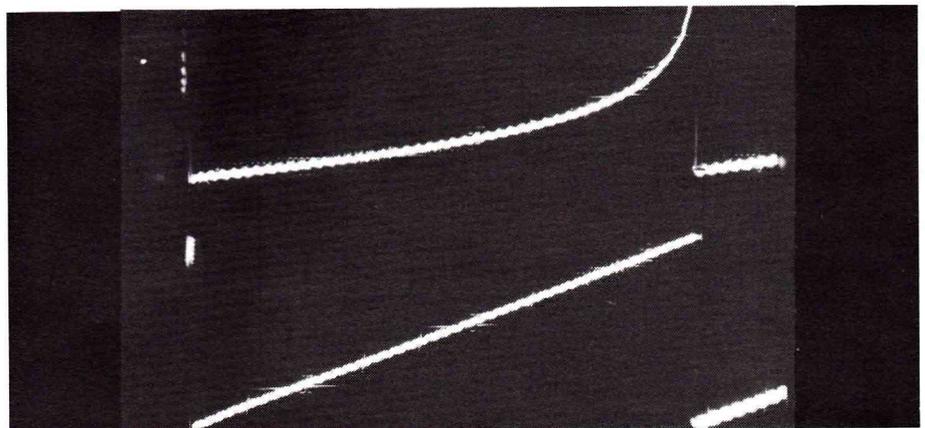
Figure 7 shows the point-to-point wiring of the unit. The identification letters in Figure 7 correspond with those in Figure 6, so that point 'A' in Figure 6 connects to point 'A' in Figure

7, point 'B' connects to point 'B', and so on.

Adjustment

Thoroughly check all the wiring before initially testing the unit, paying particular attention to the wiring around T1, S3 and FS1. Start with all three preset resistors at a roughly mid-point setting.

If an oscilloscope is used to monitor the signal at pin 12 of IC2 a non-linear ramp waveform should be present. If clipping of the signal is evident RV1 should be backed-off slightly in an anticlockwise direction so as to eliminate the clipping, but it should not be turned back much further than is absolutely necessary. If no clipping is evident, advance RV1 as far as possible in a clockwise direction without clipping being produced.



Top: Processed ramp signal.
Bottom: The linear ramp signal.

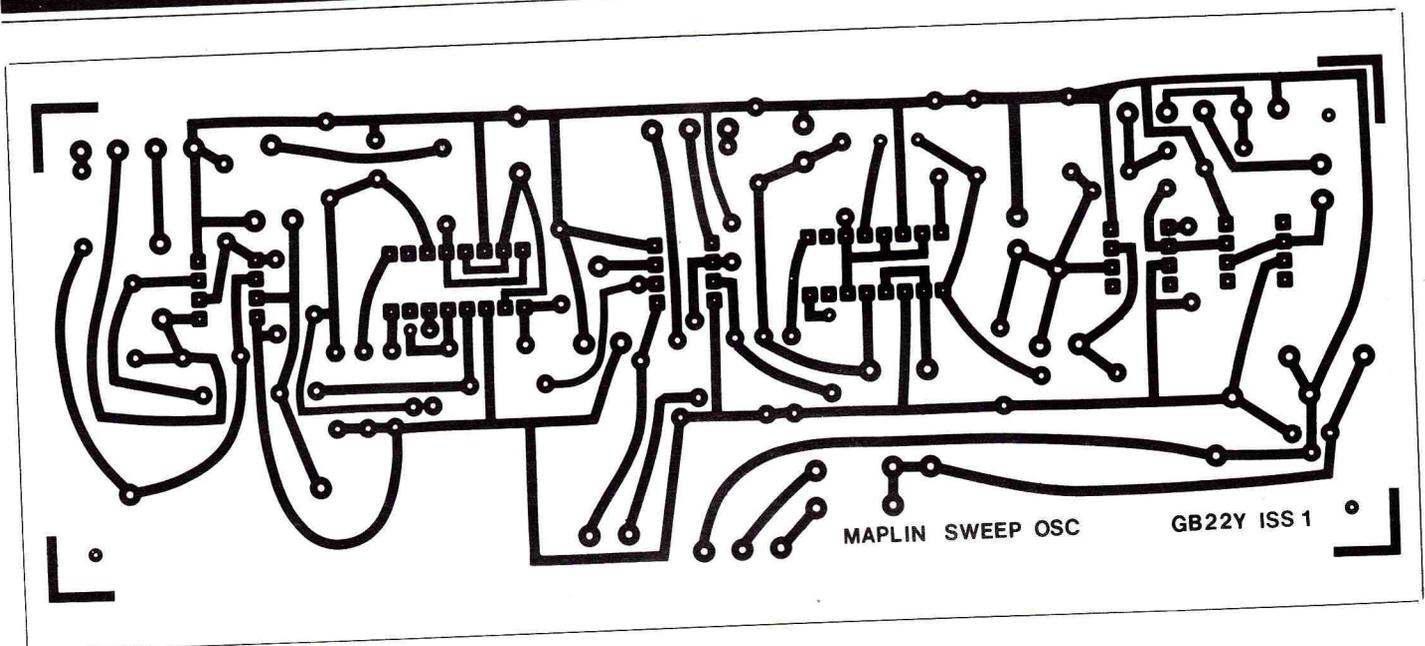


Figure 6. Legend and artwork.

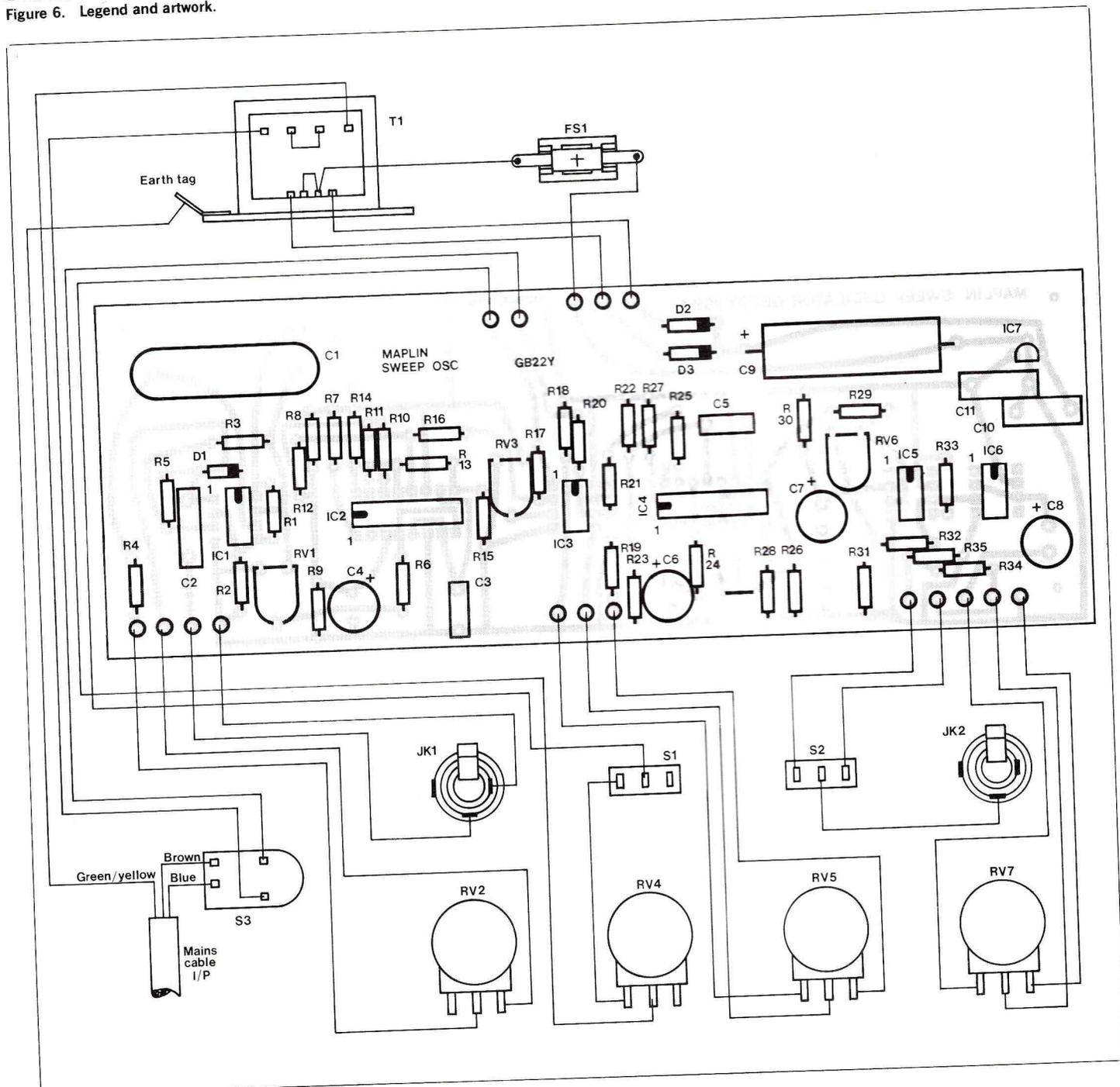


Figure 7. Wiring diagram.

RV3 is given a setting that gives an unclipped output signal at pin 7 of IC3, and the setting of this component will probably not be very critical.

With S1 set to cut off the V.C.O. from the ramp generator circuit so that a fixed output frequency is obtained, an oscilloscope is used to monitor the output waveform of the unit and RV6 is adjusted for the optimum output waveform. Alternatively a crystal earphone can be plugged into SK2 so that the output of the unit can be monitored by ear, and with RV5 set for a fairly low operating frequency it should be possible to hear the fundamental frequency plus the harmonics at higher frequencies. RV5 is then adjusted to minimise the harmonics.

Normally the unit will probably be used to cover the whole audio frequency over each sweep, and this requires RV4 to be set for maximum sweep range, or very nearly so (i.e. set in a fully clockwise direction). RV5 must

be set so that the unit is swept over the appropriate range of frequencies, and it is helpful here to use a slow sweep speed and to monitor the output of the unit using an earphone.

SK1 is coupled to the trigger input of the oscilloscope, and if the latter has a positive/negative trigger switch this should be set to the "positive" position. SK2 is coupled to the input of the equipment under test, and the output of this equipment is coupled to the Y input of the oscilloscope. S2 and RV7 are adjusted to give a suitable input signal level for the equipment under test, and the Y gain control(s) of the oscilloscope are set for a satisfactory trace height. A sweep speed of about 1HZ is suitable, and RV2 must be adjusted to match the sweep rate of the oscillator to that of the oscilloscope with reasonable accuracy. There is no real advantage in using a sweep frequency of less than about 1HZ. It is not advisable to use a higher sweep frequency since this would re-

sult in the oscillator being swept over the low frequency range before there had been any significant output at these frequencies, and misleading results would consequently be produced. A higher sweep frequency can be employed if the unit is only being used at output frequencies of a few hundred Hertz or more.

For detailed investigation over only a small section of the audio frequency band RV4 is backed off in an anti-clockwise direction and RV5 is adjusted to give coverage of the appropriate section of the audio spectrum.

Most oscilloscopes have a green medium persistence cathode ray tube, and with the low sweep speeds used in this application the left hand section of the trace fades out before the right hand portion is completed. Despite this the shape of the trace can be seen quite clearly without having to resort to a storage oscilloscope of some kind or oscillographs.

SIMPLE SWEEP OSCILLATOR

Resistors — All 0.4W 1% metal film

R1,2,8,9,22,23,

30,31	4k7	(8 off)	(M4K7)
R3,7,13,14	100k	(4 off)	(M100K)
R4,27	47k	(2 off)	(M47K)
R5,12	120k	(2 off)	(M120K)
R6,10,11,15,32	12k	(5 off)	(M12K)
R16	1M2		(B1M2)
R17	3M9		(B3M9)
R18	68k		(M68K)
R19	1k5		(M1K5)
R20,21,25,34	10k	(4 off)	(M10K)
R24	5k6		(M5K6)
R26,28	8k2	(2 off)	(M8K2)
R29	22k		(M22K)
R33	33k		(M33K)
R35	110R		(M110R)
RV1	4k7 min horiz preset		(WR57M)
RV2	2M2 lin pot		(FW09K)
RV3	22k min horiz preset		(WR59P)
RV4	100k lin pot		(FW05F)
RV5	47k lin pot		(FW04E)
RV6	2k2 min horiz preset		(WR56L)
RV7	4k7 lin pot		(FW01B)

Capacitors

C1	2u2 polyester		(BX84F)
C2	10nF polyester		(BX70M)
C3	1nF carbonate		(WW22Y)
C4,6,7,8	100uF 25V P.C. electrolytic	(4 off)	(FF11M)
C5	4n7 carbonate		(WW26D)
C9	470uF 25V axial elect		(FB73Q)
C10	100nF polyester		(BX76H)
C11	220nF polyester		(BX78K)

Semiconductors

D1	1N4148		(QL80B)
D2,3	1N4002	(2 off)	(QL74R)
IC1	LF353		(WQ31J)
IC2,4	LM13700N	(2 off)	(YH64U)
IC3	CA3240E		(WQ21X)
IC5	CA3080E		(YH58N)
IC6	741C (8 pin DIL)		(QL22Y)
IC7	uA78L15AWC		(QL27E)

Miscellaneous

S1,2	Min SPDT toggle	(2 off)	(FH00A)
S3	Rotary mains switch		(FH57M)
T1	Mains primary, twin 15 volt 200mA secondaries		(WB15R)
JK1,2	3.5mm jack sockets	(2 off)	(HF82D)
FS1	20mm 100mA quick-blow		(WR00A)
	Printed circuit board		(GB22Y)
	20mm chassis mounting fuseholder		(RX49D)
	Case type WB4		(LH39N)
	Knob type K7B	(5 off)	(YX02C)
	8 pin DIL skt	(4 off)	(BL17T)
	16 pin DIL skt	(2 off)	(BL19V)
	Hook-up wire black		(BL00A)
	Cabinet feet		(FW19V)
	Grommet small		(FW59P)
	Spacer 6BA 1/4in		(FW35Q)
	Bolt 1/4in 6BA		(BF05F)
	Bolt 1in 6BA		(BF07H)
	Nut 6BA		(BF18U)
	Tag 6BA		(BF29G)
	Veropins type 2145		(FL24B)

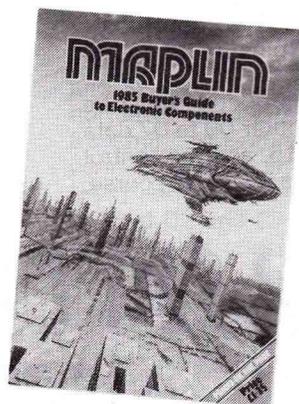
A complete kit of all parts, excluding the case, is available for this project.

Order As LK06G (Sweep Oscillator Kit).

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ZX81/MODEM INTERFACE

ZX81/MODEM INTERFACE

ZX81/MODEM INTERFACE

- ★ Connects ZX81 to Modem or other computers
- ★ TTL/RS232 compatible
- ★ Plugs into expansion socket via motherboard
- ★ 300 Baud standard transmission rate (adjustable)

by Dave Goodman

The immense popularity of our Modem project has prompted us to develop a series of connecting interfaces for most of the popular home microcomputers. This will enable two-way communication, either direct to other computers or via telephone links to systems such as the Maplin on line computer.

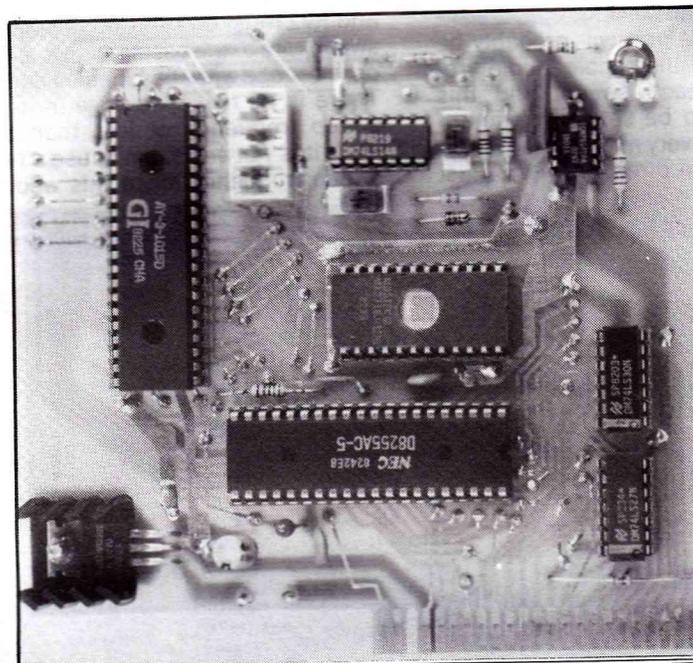
The ZX81/Modem interface utilises an EPROM code translator for converting ASCII coded signals to ZX code and vice versa, as the ZX81 is not ASCII coded.

Included in the article is a machine code program for running our interface with the ZX81. Perhaps the thought of machine code programming is anathema to many Sinclair BASIC users, but don't be put off. All that you need to do is type in the codes given, store the program on tape for future use, and RUN. If you so wish, the program can be used as a basis for further development by the more experienced programmer.

Circuit Description

REG 1 is fitted so that the power supply can be taken from the unregulated side of the computer PSU (+9V). This saves undue loading on the internal regulator of the ZX81, and, if link 1 is not used, any external supply of +8V to +30V may be connected to P2 instead.

Serial data transmissions enter the UART (IC6) via level change triggers from pin 3 and 5 (OV). All signals are TTL level, and may be connected direct or inverted by S7 to suit the system. IC7 is a 4.8kHz astable multivibrator, and supplies the UART, which needs a clock frequency of sixteen times the required Baud rate. Dividing 4800Hz by sixteen will give the standard Baud rate of 300.



Receive Mode

The I/O port IC3 has three ports designated A, B, and C. For the computer to access these ports it is necessary to make room in the memory map, so that IC1 and IC2 decode address lines A3 to A15 for addresses 8312 to 8315, which appear in the 'ghost' ROM area in the ZX81. D1 deselects the internal ROM area for use by the interface. IC3 is an 8255, which has quite a comprehensive operating instruction set, but for our application all that is necessary is to set Port A to output mode, Port B to input mode, Port C upper (pins 10 and 11) to input mode, and Port C lower (pins 14 to 17) to output mode.

To do this a control code must be placed on the computer D0 to D7 data lines at address 8315, and the control code to set the mode is 138. Of course,

setting the control code must be done immediately at the beginning of programs used to control the port, and would be something like POKE 8315, 138.

Port C, address 8314, is set next to disable the EPROM output (OE HIGH-IC4), and prevent IC6 from transmitting data DS HIGH and setting RDE low. This allows data from IC6 to be placed into Port B (address 8313). The DAV (data available) output goes high when serial data enters IC6, and this acts as a FLAG to tell the computer that information is ready to be read from Port B.

Unfortunately, the ZX81 code system is not compatible with ASCII, so received CHR\$ will need to be translated. Port B is read and this data is placed into Port A (address 8312) and EPROM IC4, where it is translated and

ZX81/MODEM INTERFACE

ZX81/MODEM INTERFACE

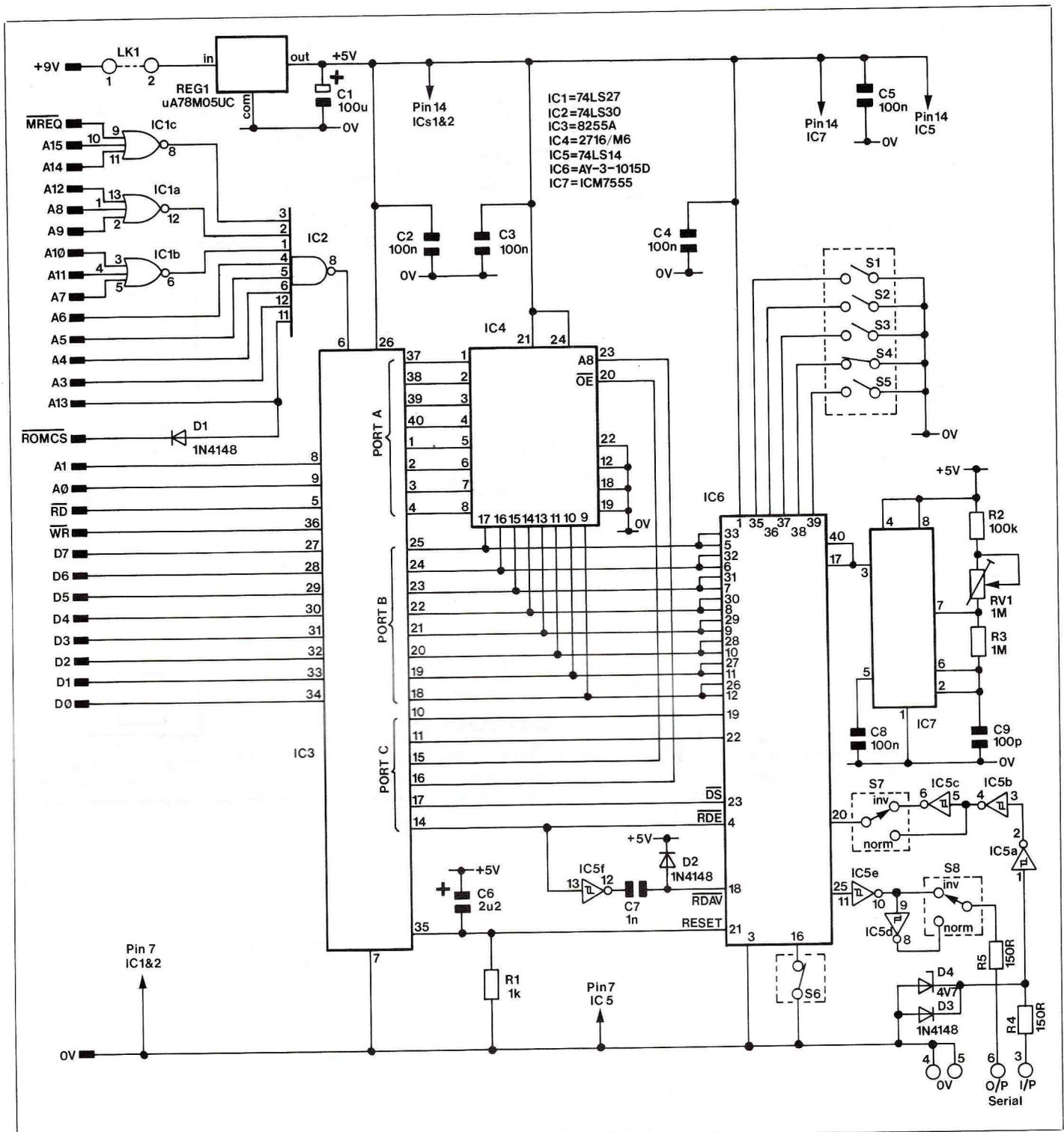


Figure 1. Circuit diagram.

placed into Port B again. Reading Port B will produce the required character for printing to the screen display. Using an EPROM for code translation makes programming much simpler and reduces memory requirements, although IC4 could be omitted and data read from Port B direct. This arrangement would be used when communicating with another ZX81.

Transmit Mode

Port C is used to reset the DAV output via IC5. Disable the receive data lines P5 to P12 by taking RDE high, hold IC4-A8 high (this address line must be high for Tx codes and low for Rx codes) and enable IC4 output by taking OE low. ZX codes for transmitting are then placed into Port A and IC4, and hence to

the UART. DS (transmit data strobe) is taken low, to latch data from pins 26 to 33 into IC6, then DS is taken high to transmit data in serial form via IC5, S8, to pins 6 and 4 (0V).

Switches S1 to S6 set various status bits, character length and parity as shown in Tables 1a and b. Switches S7 and S8 allow the user to select either normal or inverted signals for receive or transmit, depending on the system connected. R1 and C6 reset both UART and I/O port when first switched on, and D2 and C7 apply a fast negative pulse for resetting DAV output.

Switch	Closed	Open
1	parity	no parity
2	one stop bit	two stop bits
5	odd parity	even parity

Table 1a.

Bits per character	Switch 3	Switch 4
5	closed	closed
6	closed	open
7	open	closed
8	open	open

Table 1b.

A standard switch setting would be switches 1, 2, 3, and 5 open and switches 4 and 6 closed. This gives 7 bits per character, 2 stop bits and no parity. S6 would normally be left closed, as this places all status bits onto the output lines.

Address	Description	Function
8315	Control address	Data 138 — set mode
8314	Port C	Lower output — Upper input
8313	Port B	Input only
8312	Port A	Output only

Table 2. All Port addresses and their functions.

ZX81 MODEM INTERFACE PARTS LIST

Resistors — All 0.4W 1% Metal Film.

R1	1k	(M1K)	
R2	100k	(M100K)	
R3	1M	(M1M)	
R4,5	150R	(M150R)	2 off
RV1	1M Hor-sub min Preset	(WR64U)	
Capacitors			
C1	100uF 10V PC Electrolytic	(FF10L)	
C2-5 inc, 8	100nF Minidisc	(YR75S)	5 off
C6	2u2F Tantalum	(WW62S)	
C7	1nF Ceramic	(WX68Y)	
C9	100pF Silvered Mica	(WX13P)	
Semiconductors			
D1,2,3	1N4148	(QL80B)	3 off
D4	BZY88C4V7	(QH06G)	
REG 1	uA78M05UC	(QL28F)	
IC1	74LS27	(YF18U)	

IC2	74LS30	(YF20W)
IC3	8255A	(YH50E)
IC4	2716/M6	(QY52G)
IC5	74LS14	(YF12N)
IC6	AY-3-1015D	(WQ18U)
IC7	ICM7555	(YH63T)
Miscellaneous		
S1-6 inc.	DIL Switch SPST Dual	3 off (XX26D)
S7,8	DIL Switch SPDT Single	2 off (XX28F)
	8-Pin DIL Skt	(BL17T)
	14-Pin DIL Skt	3 off (BL18U)
	24-Pin DIL Skt	(BL20W)
	40-Pin DIL Skt	2 off (HQ38R)
	Vaned Heatsink	(FL58N)
	Bolt 6BA x 1/2"	1 Pkt (BF06G)
	Nut 6BA	1 Pkt (BF18U)
	Veropin 2141	1 Pkt (FL21X)
	Track Pin	2 Pkts (FL82D)
	PCB	(GB23A)

A complete kit of all parts is available for this project.
Order As LK08J (ZX81/Modem Interface).

position, and switches 7 and 8 to 'INV'. With no power attached, plug the interface PCB into your ZX81 or Extendo-board, and switch on. Use a voltmeter connected to 0V (pin 4/5), and check for +5V on the output pin (right-hand side) of REG 1. Switch off, insert ICs and re-apply power. You should be rewarded with a cursor on the screen, as normal. If a frequency counter or oscilloscope is available, check for a 4.8kHz signal on pins 17 and 40 of IC6, and adjust RV1 to suit. When testing programs, note that on a 1K only machine the interface will still function, although you will not be able to run the machine code program and have a full screen display.

Now enter and run test program 1. This will test all port locations, along with the EPROM addresses 0 to 511. The display data, printed in decimal and hexadecimal, shows ASCII and ZX81 CHR\$ codes stored in IC4.

After typing the program enter RUN/NEWLINE. The program will stop after printing EPROM address 511; with an error 9 at line 45, which is all right. If, however, your test program fails before this make sure that you have entered all eighteen lines correctly. If you still have

problems the Port may be faulty, in which case you will need to POKE data into Port A and PEEK Port B to get an indication of the failure.

Next, enter and run program 2. Connect pins 3 and 6 together on the module, and press any key. Data will be transmitted and received, then printed on the TV display, proving that the module is functioning correctly. The display is limited to around 400CHR\$ in 1KB.

Using the Interface

As mentioned previously, the program and working system require a minimum of 1050 bytes of memory, which means that to display a full screen of data a RAM extension is required. You could, however, write a simple receive only routine, for testing your interface with modem systems, but BASIC is too slow for this application, so machine code programs become necessary. Program 3, entered into a REM statement, will allow two-way communication with the Maplin on-line computer, and also several other commercial data links. The TV display will be blank until data is received, whereupon the bottom line

will fill with characters and scroll when full.

Carriage return codes will scroll the display while line feed codes are trapped and not used. Once you have established a data link, transmission can be direct from the keyboard — no transmit or receive mode control codes are required here. Provided that systems connected to the interface have echo facilities, you may print to the screen via the transmission path, not directly from the keyboard. Many shift characters are valid, but some of them will be decoded as question marks, along with all the unused EPROM address codes.

Function and Graphics modes are not used, and should generate either shifted or direct key characters. Facilities do not exist for deleting characters or for clearing the screen. The BREAK key returns a space and NEWLINE gives carriage return when typing program 3.

Once the last character has been entered the program will stop running. Return to SLOW mode and press NEWLINE. You will see line 20 full of characters and symbols. Parts of the line will be blank due to code 118 being entered, but this is all right. Now check the data by changing line 40 to PRINT I, and line 50 to PRINT PEEK I. Now RUN 30 and a check list giving each address and the number stored there will fill the screen. To continue press CONT-NEWLINE.

When you are happy with your efforts RUBOUT lines 30 to 60 and type in line 30 LET A=USR 16524. The function USR is below key L, and 16524 is the starting address of the machine code program. You would be well advised at this stage to save 'MI' on cassette a few times. 'MI' is short for Modem Interface, although obviously any recognition code could be used. If line 10 REM statement length is increased, the starting address 16524 will also be increased, so you must calculate this when changing the program name, or all will be lost!

To operate the system, hook up the modem, or whatever you are trying to communicate with, to pins 3 (serial input), 4 (0V), and 6 (serial output), and load the program. Type RUN-NEWLINE and make the communicating link. You may now receive or transmit data as required.

```
10 REM "MI"
20 REM (Type in 110 full
  stops)
30 FOR I = 16524 TO 16632
40 INPUT A
50 POKE I,A
60 NEXT I
```

On receiving this kit you should check the type code number on the package of IC3. If this number specifically reads as NEC D8255 A-C, you should slightly modify the board as follows. Leave out the track pin that connects MREQ to IC1 pin 9. Connect pin 9 to 0V (pin 7) and leave MREQ floating.

Go into FAST mode, press RUN then NEWLINE and enter the following Decimal codes. (Enter each code then NEWLINE.) Each code is a number between 0 & 255 inc.

THE CORRECTED VERSION IS AS FOLLOWS-

```
62 138 50 123 32 205 14 12 14 0 33 122 32 54 11 54 10
126 230 128 40 28 58 121 32 50 120 32 54 9 58 121 32
254 10 40 229 254 118 40 220 215 62 32 12 185 40 213
24 216 229 197 237 75 37 64 33 255 255 167 237 66 40
40 17 0 1 167 237 82 40 32 205 189 7 126 237 75 37 64
33 255 255 191 237 66 32 244 50 120 32 33 122 32 203
118 40 252 54 13 54 5 54 10 193 225 191 24 164
```

Program 3.

CMOS Crystal Calibrator

- ★ Enables calibration of receivers.
- ★ Checks the position of the edges of amateur band allocations.
- ★ Produces markers at switchable intervals of 1MHz, 100kHz, 12.5kHz, or 10kHz.



by A. J. Bell, BSc, GW4JJW

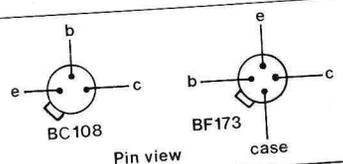
Introduction

This article describes a crystal calibrator designed around CMOS logic IC's, which produces markers switchable at intervals of 1MHz, 100kHz, 12.5kHz or 10kHz. When the calibrator was tested using a spectrum analyser, the markers were found to be complete to 300MHz - beyond this frequency they approached the spectrum analyser noise level. The markers can be amplitude modulated with a 1kHz tone, a facility which produces markers at 1kHz intervals. The current consumption

of the crystal calibrator is less than 3mA at 9V (27mW) - less power than would be consumed by a single 74-series TTL integrated circuit.

Operation

The circuit diagram of the crystal calibrator is shown in figure 1, and the various semiconductor pinouts and logical functions in figure 2. A stabilised voltage supply, comprising TR2 and D2, supplies power to all the CMOS logic. In order to reduce power consumption the zener diode is run at a lower current than normal. Three different zener



ADDRESS INPUTS		CONTROL INPUTS		OUTPUT
C	B	INHIBIT	\overline{OE}	Z
0	0	0	0	x0
0	0	1	0	x1
0	1	0	0	x2
0	1	1	0	x3
1	0	0	0	x4
1	0	1	0	x5
1	1	0	0	x6
1	1	1	0	x7
-	-	-	1	0
-	-	-	0	Hi Z

- = Dont care. Hi Z = Tristate condition

Figure 2. Semiconductor pinouts and logic function chart.

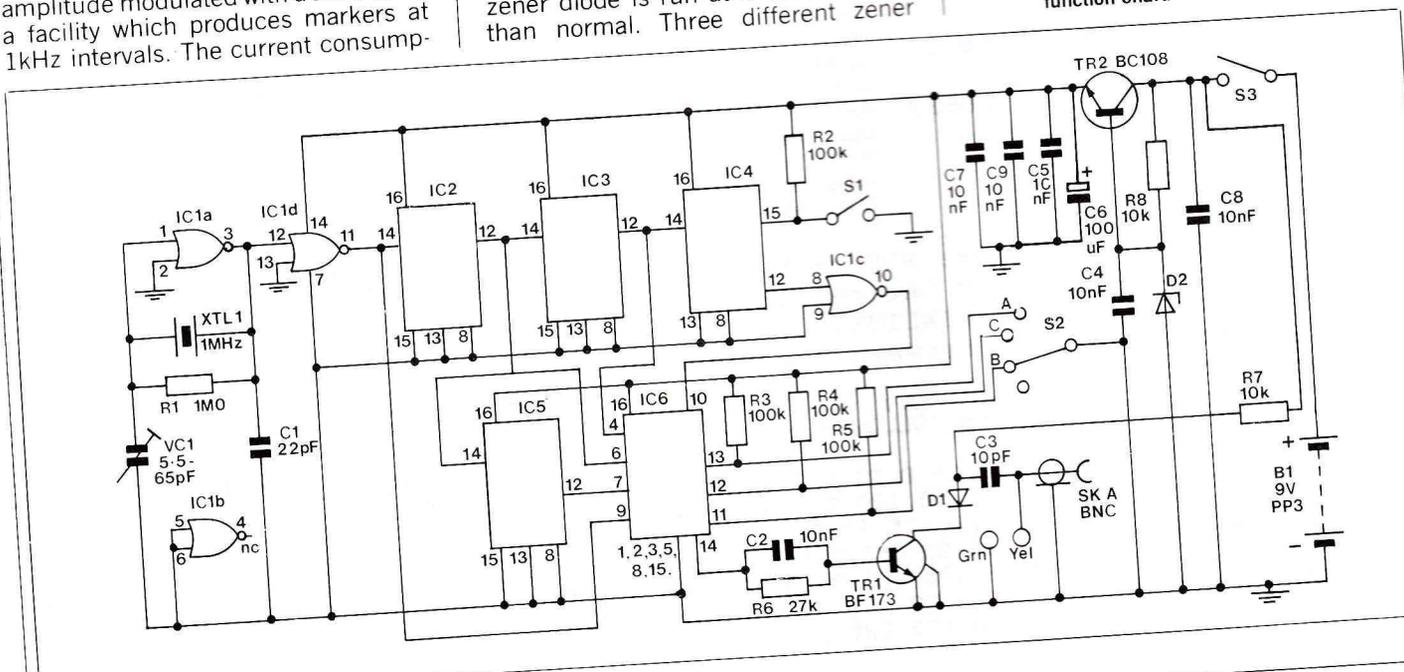


Figure 1. Circuit diagram.

diodes were tried under these conditions and all functioned satisfactorily. A single CMOS NOR gate (IC1a) is used as a 1MHz crystal oscillator, whose frequency may be trimmed using VC1. The output from the oscillator is buffered by another section of the NOR gate (IC1d) and then fed into a chain of dividers which produce frequencies of 100kHz, 12.5kHz and 10kHz. These, together with the original 1MHz, are fed into the data selector (IC6).

A "data selector" is a type of logic IC that selects only one of many inputs. The selection is performed according to the value set on its address line inputs. Figure 2 shows the logical functions of the data selector, type 4512, used in the crystal calibrator. It can be seen that if all address lines are high, data line "X7" will be selected. For the crystal calibrator, inputs X7, X6, X5 and X3 are used for the 1MHz, 12.5kHz, 100kHz and 10kHz signals respectively. These particular input lines were chosen because they can be selected by making none or any one of the address lines logical zero - this is the function of the interval switch SW2.

The use of a data selector allows the marker interval to be chosen by switching DC signal levels, instead of the standard method of switching the RF signals directly. This keeps the lengths of the wire carrying RF to a minimum, thereby reducing radiation or pickup.

When SW1 is closed, IC4 is freed from its reset state and produces a 1kHz signal which is inverted by IC1c and fed to the inhibit of IC6. This amplitude modulates its output which is fed to the base of TR1 via a 27k ohm

resistor and a parallel ceramic capacitor. TR1 is a UHF transistor with a very high ft. In its collector is a 1N914 diode, a non-linear load, which generates harmonics. Finally the RF output is taken via 10pF ceramic capacitor, C3, to both a BNC connector and a terminal post, thereby offering a choice of connection.

Construction

The calibrator was constructed on

double-sided, copper clad glass fibre epoxy board, size 100mm x 60mm. The top surface of the PCB was used as a ground plane and the underside for interconnections. The artwork for the PCB and the component layout are given in figures 3 and 4. If you drill the PCB, copper surrounding the holes on the component side should be removed by countersinking with a 3/16 inch drill. The author used IC sockets throughout, but there is no reason why the IC's could not be soldered directly on to the PCB provided a low leakage soldering iron is used and normal CMOS precautions are observed. The two capacitors, C2 and C3 must be low inductance type, such as disc ceramic, so as to obtain a good high frequency response from the calibrator. Although IC1 is specified as a quad NOR gate, it is used throughout as an inverter - one input of each of the three gates used being grounded.

The crystal calibrator described is possibly more comprehensive than will be required in some instances. Various functions can easily be removed from the circuit if required. For example, if IC5 is omitted then the 12.5kHz option will be unavailable. If IC4 is omitted and pin-12 of its socket is connected to Vdd via 100K ohm resistor, then the tone facility will be unavailable.

Alignment

The calibrator is best aligned when it has been installed in its working position (box or rig). The station RX is switched to AM and tuned to one of the standard frequency services, such as MSF on 5MHz. The calibrator is switched on and loosely connected to the RX antenna socket in parallel with the antenna used to receive MSF. If the RX uses "UHF" type connectors, unscrew the outer skirt and pull the plug half way out of the socket. Take a length of wire, strip both ends, connect one end to the terminal post and loop the

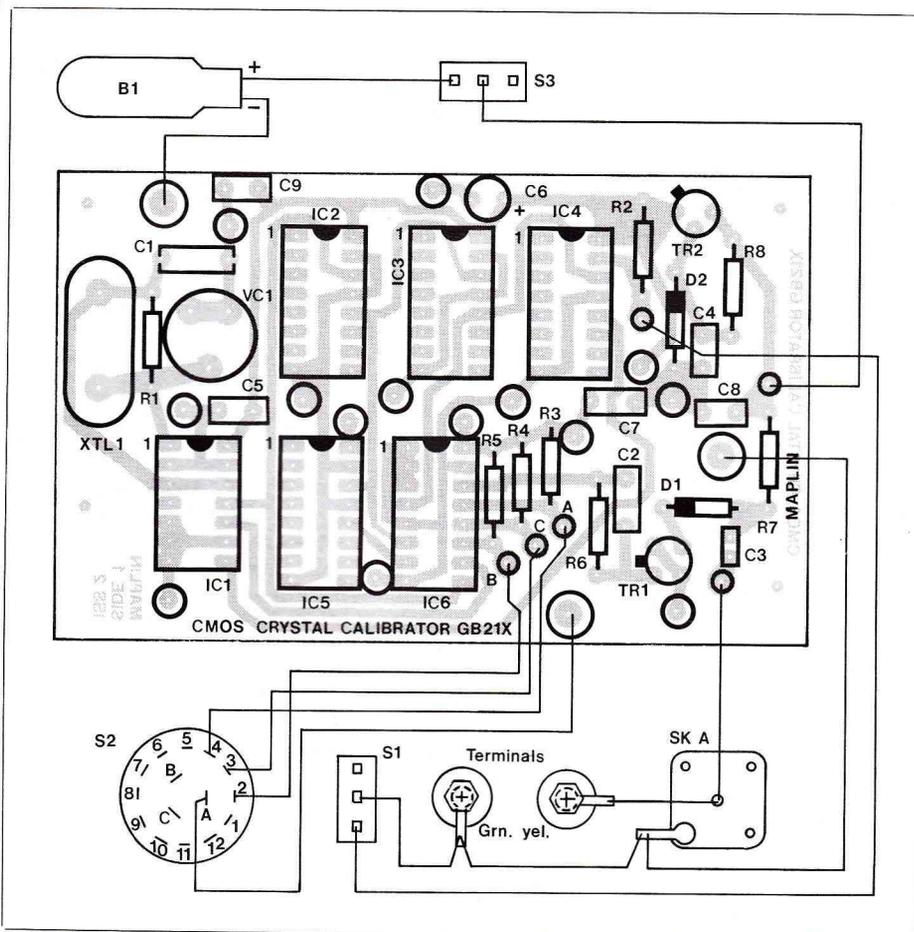
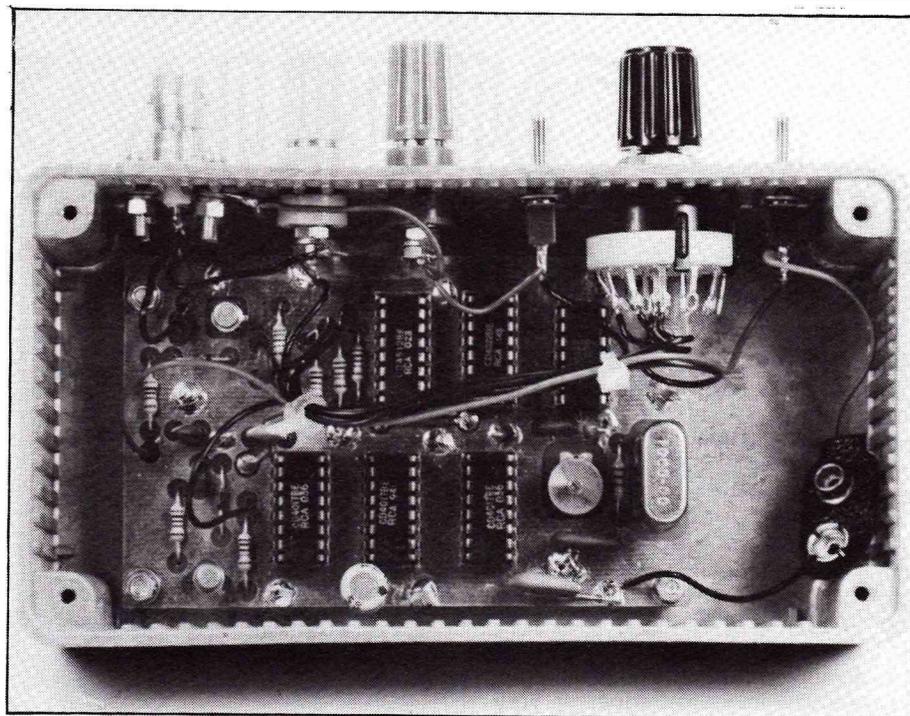


Figure 3. PCB layout and wiring diagram.

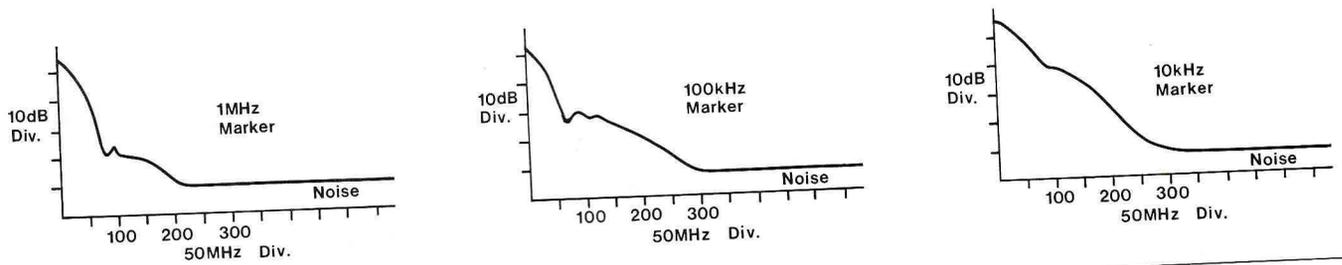
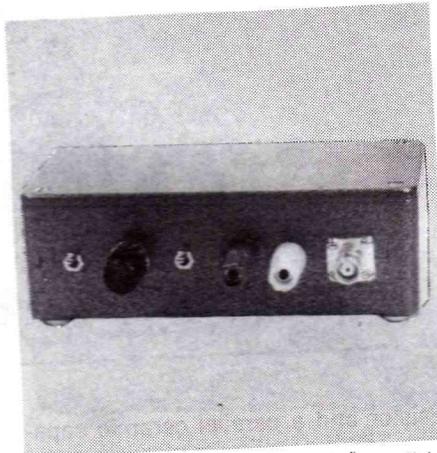


Figure 5. Test Graph.

other end over the exposed inner section of the plug. A beat note generated by the mixing of the standard service and the calibrator should be heard from the RX. To align the calibrator, trimmer capacitor VC1 should be adjusted to zero beat the two signals. An oscilloscope connected to the AF output from the RX is useful for monitoring the beat note frequency down to a few Hz. Zero beat is the position at which the beat note disappears after the note becomes progressively lower in frequency. Very low frequency beats, less than 1Hz, manifest themselves as a cyclic slow rise and fall in background noise level. The higher the frequency of the standard service used, the sharper, and hence more precise, will be the zero beat position. Note that an error of 10Hz at 5MHz will be multiplied to an error of 1kHz at 500MHz.

Applications

A crystal calibrator is used to check the calibration of receivers, and in the amateur sphere is particularly useful in checking the position of the edges of the amateur band allocations. To do this, the RX is tuned as close as possible to the required band edge. The calibrator is then loosely connected to the antenna socket of the RX. If the band edge is on a 1MHz boundary (28.0MHz) then 1MHz markers should be selected. Alternatively if the band edge is on a 100kHz boundary (3.5MHz-3.8MHz)



then select 100kHz. Failing this, 12.5kHz and 10kHz intervals are available for use. Receivers are usually calibrated according to the type of emission to be received.

For AM tune the RX for a peak S-Meter reading from the calibrator signal. If no S-Meter is available switch on the tone facility and tune for loudest tone. Using the tone facility, however, is of limited value as markers at 1kHz intervals tend to be generated but are lower in amplitude than the 100kHz and 1MHz signals. For SSB reception the RX should be set to receive the appropriate side-band and tuned so as to zero beat the calibrator signal. For CW, the situation is a little more difficult, as the RX is usually tuned about 800Hz lower in frequency than the incoming signal - this produces the

audible tone. Usually, however, receivers are calibrated such that SSB and CW give identical readouts, and therefore the RX should be set to receive CW and then tuned to zero beat the calibrator signal. It may not be possible to hear low frequency beat notes when using narrow CW filters. Note that a station transmitting on the same frequency as the calibrator would be inaudible, being zero beat, and the RX would normally be tuned about 800Hz away from the zero beat position in order to copy CW transmissions. It is important to remember that if the TX carrier is positioned close to a band edge care must be taken to ensure that no sidebands are radiated outside the authorised frequency band.

Acknowledgements

The author wishes to thank G3GIH, G3VMW, G3XAQ and GW4JJV for their comments and suggestions during the course of this project.

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- Radio Amateur's Handbook. 58th edition. ARRL, 1981. pp 16.12-16.16.

PARTS LIST FOR CRYSTAL CALIBRATOR

Resistors - All 0.4W 1% metal film unless specified.

R1	1M0		(M1M0)
R2-5	100k	4 off	(M100K)
R6	27k		(M27K)
R7,8	10k	2 off	(M10K)
Capacitors			
C1	22pF Mica		(WX05F)
C2,4,5,7-9	10nF Disc	6 off	(BX00A)
C3	10pF Ceramic		(WX44X)
C6	100uf PC elect.		(FF11M)
VC1	65pF Trimmer		(WL72P)
Semiconductors			
D1	IN914		(QL71N)
ZD1	BZY88C8V2		(QH12N)
TR1	BF173		(QY53H)
TR2	BC108		(QB32K)
IC1	4001BE		(QX01B)
IC2-4	4017BE	3 off	(QX09K)
IC5	4022BE		(QW19V)
IC6	4512BE		(QW84F)

Miscellaneous
S1.3
S2
SKA

SPST ultra min. toggle
Rotary SW4B
BNC square skt.
Terminal post green
Terminal post yellow
DIL socket 14 pin
DIL socket 16 pin
PP3 Clip
PP3 Battery
1MHz FS crystal
Crystal Socket 6u
PC Board
Box DCM5005
Collet knob black
15mm collet cap black
15mm collet nut cover
Tag 6BA
Wire black
Veropins type 2141
Track pins

2 off

5 off

1 pkt
1 metre
1 pkt
1 pkt

(FH97F)
(FF75S)
(YW00A)
(HF05F)
(HF09K)
(BL18U)
(BL19V)
(HF28F)
(HX62S)
(HX61R)
(GB21X)
(LH73Q)
(RX16S)
(WL45Y)
(RX18U)
(BF29G)
(BL00A)
(FL21X)
(FL82D)

A complete kit of all parts, excluding the case, is available.
Order As LK10L (X'tal Calibrator Kit).

DXER'S AUDIO PROCESSOR

- ★ Improved performance
- ★ Needs no modifications to receiver
- ★ High filter attenuation rate
- ★ Easy to build



by Robert Penfold

The performance of many communications receivers is not all that one would desire, and probably the most common failing is a lack of really good I.F. filtering which results in an excessive amount of adjacent channel interference. A simple way of obtaining improved performance is to use an audio filter to process the audio output of the receiver, and although this does not give a level of improvement equal to that produced by adding high quality I.F. filters to the receiver, it nevertheless gives a substantial improvement. An advantage of this system is that it avoids the need for any modifications to the receiver (which, even if successful, could reduce its resale value), and the filter is simply wired between an audio output socket of the receiver and the headphones or a loudspeaker.

This filter has a 36dB per octave lowpass filter with a cutoff frequency of about 2.5kHz, and an 18dB per octave highpass filter with a cutoff frequency at about 150Hz. This very restricted audio bandwidth helps to greatly attenuate adjacent channel interference but does not impair the intelligibility of speech signals. The high attenuation rate of the filters, particularly the lowpass type, gives the unit a level of performance which is superior to most audio processors of this type.

An additional and useful feature of this audio processor is an expander. In the presence of a reasonably strong signal this allows the signal to pass through to the output normally, but when the signal level is low (during pauses in a voice signal for example) the signal is severely attenuated. By reducing the noise during gaps in the wanted signal it is often easier to copy

the signal, especially where it is necessary to copy the signal for some time. Under some circumstances the use of the expander can produce an apparent boost in the signal to noise ratio of the processed signal, and it can make a worthwhile reduction in general background noise as well as adjacent channel interference.

Just how well or otherwise the unit performs depends almost entirely on the receiver with which it is used and on reception conditions. There is obviously more scope for the processor to produce an improvement if it is used with a wide bandwidth receiver under poor conditions than if it is used with one that has good I.F. filtering and under good reception conditions. However, the prototype has been tried over a period of a few months with a short wave receiver which has 7kHz mechanical I.F. filters, and a comparison of

the processed and unprocessed signals almost invariably revealed a substantial improvement with the processor in use, especially for S.S.B. reception. The unit has also been tried with an F.M. C.B. transceiver with similar results.

Block Diagram

Figure 1 shows the block diagram for the processor, and as will be apparent from this, the filtering is used before the expander stages. This is important as it helps to prevent unwanted signals from operating the expander, and it does so simply because the filtering prevents some of these unwanted signals from reaching the expander. A buffer stage is used at the input to ensure that the lowpass filter is fed from a suitably low source impedance, and the lowpass filter is actually two 18dB per octave filters in series rather than a single filter block.

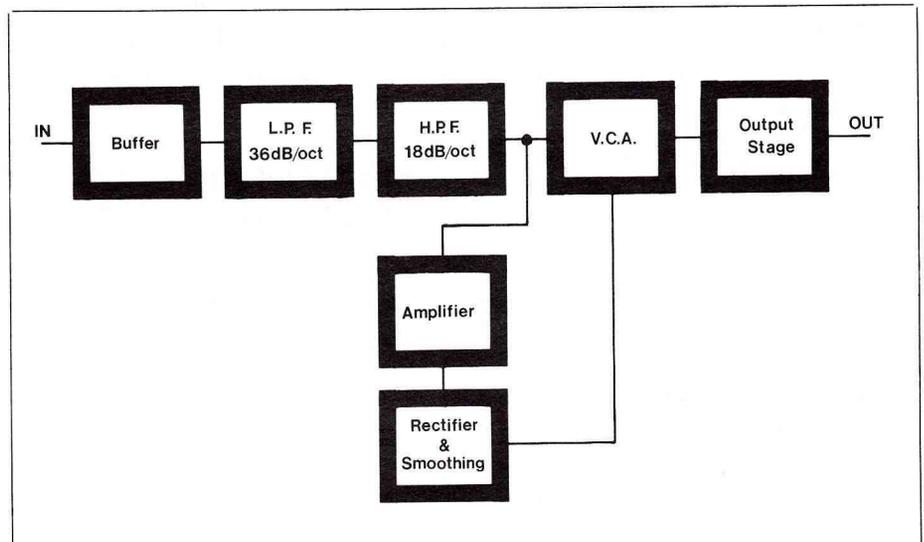


Figure 1. Block diagram.

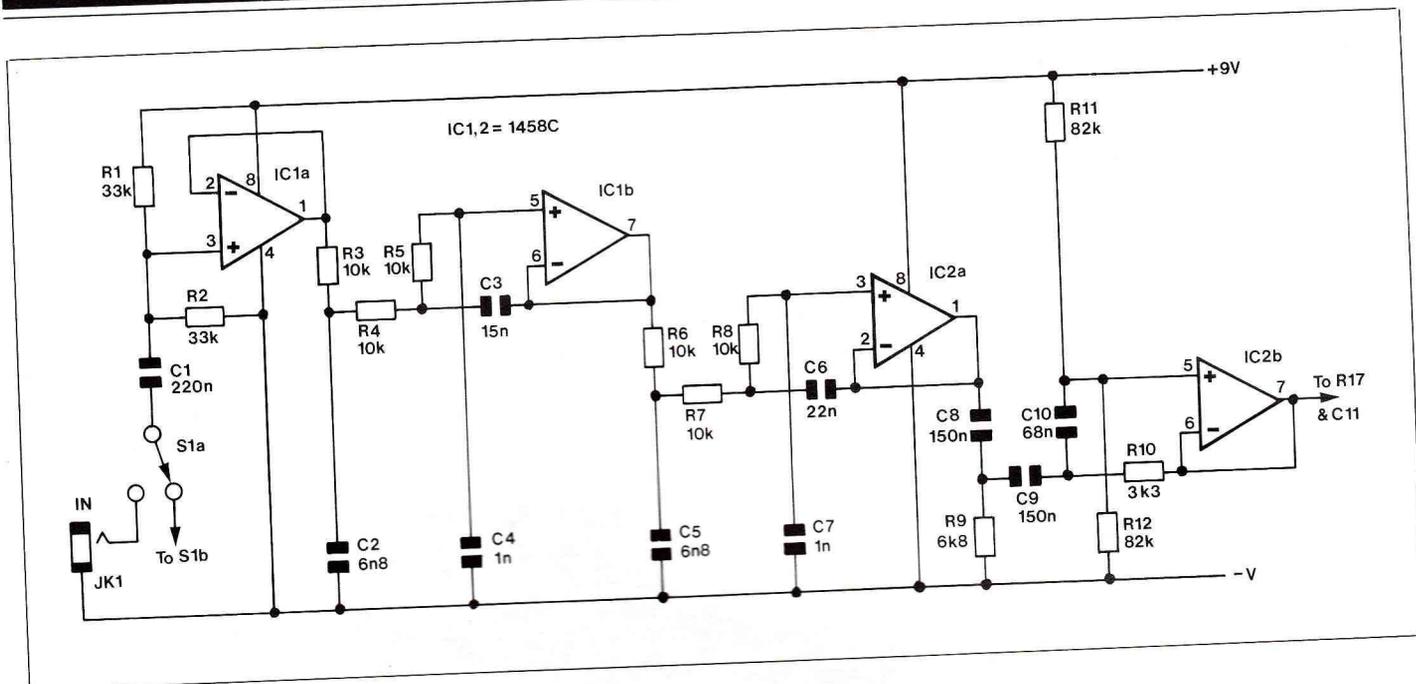


Figure 2. Circuit diagram of the filters.

After passing through the highpass filter the signal is fed through a voltage controlled amplifier (V.C.A.) which has only a small control voltage under quiescent conditions. It consequently attenuates the input signal. Some of the output of the highpass filter is fed to an amplifier, and then the amplified signal is rectified and smoothed to produce a D.C. signal which is roughly proportional to the amplitude of the input signal. This D.C. signal is fed to the control input of the V.C.A. and provides an increase in gain if the input signal is sufficiently strong. Thus the required action is obtained with low level signals being attenuated while high level signals are through the V.C.A. unattenuated.

The output stage will drive any normal type of headphones, and will also drive an 8 ohm impedance loud-speaker with an output power of up to about 500mW R.M.S.

The Circuit

Figure 2 shows the circuit diagram for the input buffer and filter stages of the unit. IC1a is the buffer stage and is a straightforward non-inverting unity voltage gain circuit which is biased by R1 and R2.

IC1b is used as the basis of the first section of the lowpass filter, and this uses a standard configuration. R3, R4, R5, C3 and C4 effectively form a second order active filter, but due to the high value of C3 a pronounced peak in the response is produced just below the cutoff frequency. R3 and C2 form a passive low pass filter which removes this peak and gives an excellent overall response with an abrupt introduction of the full 18dB per octave attenuation rate. The second lowpass filter stage is based on IC2a and is virtually identical to the first stage. The only difference is that C6 has a slightly higher value than its equivalent in the first filter section (C3), and this gives a slight improvement to the combined responses of the two filters.

The highpass filter uses IC2b, and the configuration used is essentially the same as that employed in each section of the lowpass circuit, but the resistive and capacitive filter elements are transposed to give a highpass and not a lowpass action. The final resistive element of the filter is formed by the parallel resistance of R11 and R12, and as there is no D.C. path through C8 to C10 to bias the non-inverting input of IC2b these are used to provide a suitable bias voltage.

Figure 3 shows the combined frequency response of all three filter sections.

Expander

The circuit diagram of the expander and output stages of the processor are shown in Figure 4. The V.C.A. is built

around IC3 which is an operational transconductance amplifier and IC4 which is merely used as a buffer amplifier. R17 and R19 form a negative feedback network which set the voltage gain of the V.C.A. at unity, but this assumes that the bias current fed to the amplifier bias input of IC3 (pin 5) is sufficient to produce unity voltage gain. With RV1 at minimum resistance this will indeed be the case and the expander action of the circuit is eliminated. However, with RV1 at maximum value the quiescent bias current is greatly reduced and there is a substantial amount of attenuation through the V.C.A. Intermediate settings of RV1 give a corresponding degree of attenuation through the V.C.A.

Some of the output from the final filter stage is taken via sensitivity con-

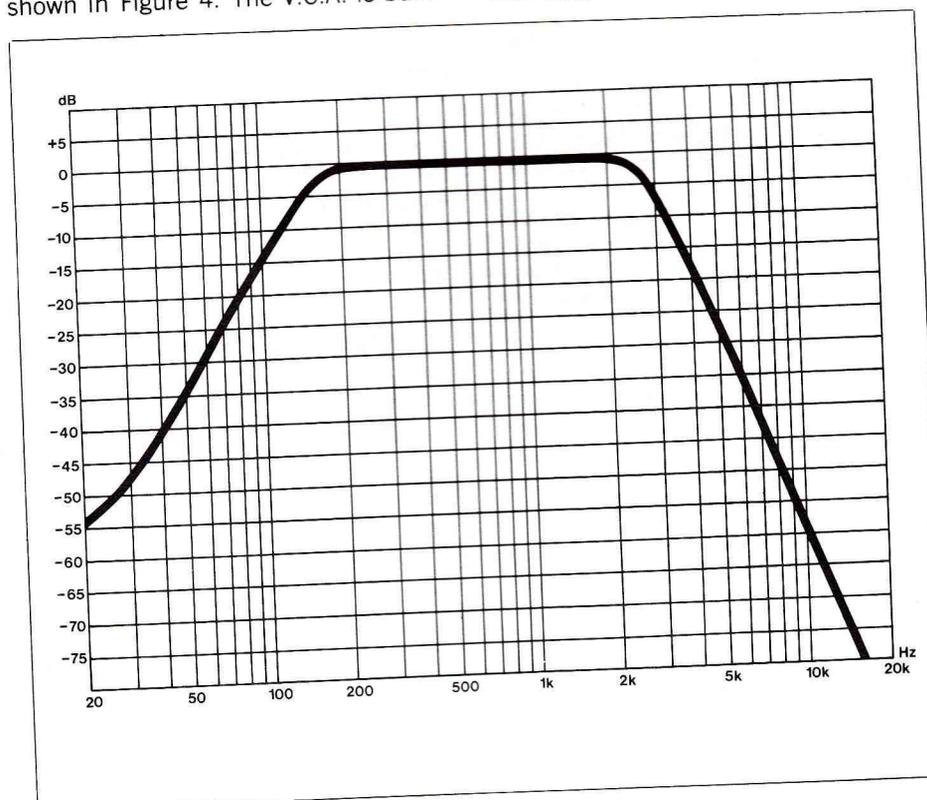


Figure 3. Frequency response of the unit.

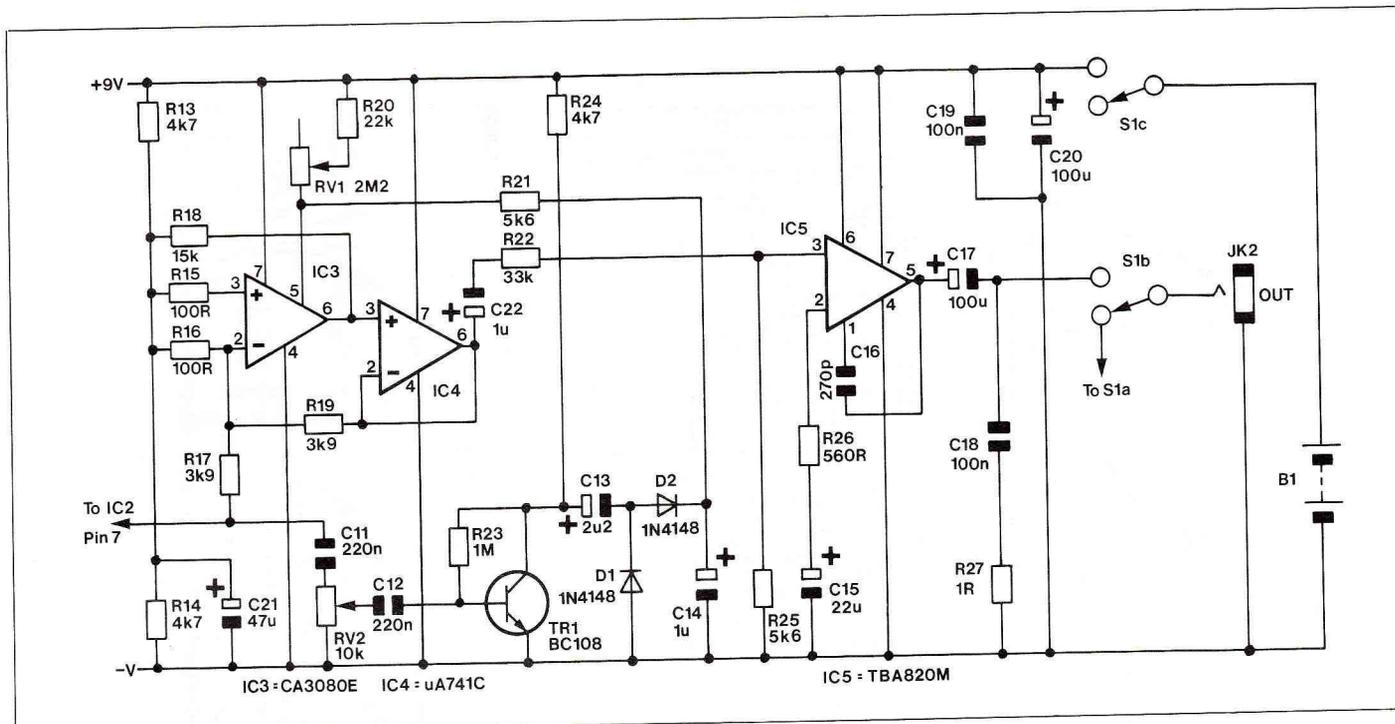


Figure 4. Circuit of the expander and output stages.

control RV1 to a high gain common emitter amplifier which uses TR1. The output of TR1 is rectified by D1 and D2, and smoothed by C14. The resultant positive voltage is fed to the V.C.A. by way of R21, and in the presence of a strong input signal boosts the gain of the V.C.A. to unity regardless of the setting of RV1. RV2 is adjusted so that the wanted signal operates the expander circuit but the background noise does not. In practice the circuit tends to operate for the majority of the time at full gain or the lower gain level set using RV1, and it therefore operates virtually as a noise gate. However, as the V.C.A. is not switched between two levels of gain and it can have intermediate levels of gain, strictly speaking the circuit is an expander and not a noise gate. The attack and decay times of the circuit are quite short so that the unit responds to changes in input level with adequate rapidity.

A TBA820M integrated circuit is used in the output stage and this device gives an output power which is more than sufficient for this application. R26 is a discrete feedback resistor which sets the closed loop voltage gain of the amplifier at a modest level of just over 20dB, but this is still excessive for this application. An attenuator consisting of R22 and R25 is therefore used to reduce the gain of the circuit to a satisfactory level.

S1 is a bypass switch which can be used to cut out the processor when it is not required, and one pole of S1 (S1c) is used to provide on/off switching. Power is obtained from a PP6 size 9 volt battery and the quiescent current consumption of the circuit is approximately 8.5mA. The current drain increases substantially, though, if the unit is used at high volume with an 8 ohm impedance loudspeaker, and if used in this way it would be advisable to use a larger battery, such as a PP9 size.

PARTS LIST FOR DXer's AUDIO PROCESSOR

Resistors — all 0.4W 1% metal film unless specified.

R1,2,22	33k	3 off	(M33K)
R3-R8	10k	6 off	(M10K)
R9	6k8		(M6K8)
R10	3k3		(M3K3)
R11,12	82k	2 off	(M82K)
R13,14,24	4k7	3 off	(M4K7)
R15,16	100R	2 off	(M100R)
R17,19	3k9	2 off	(M3K9)
R18	15k		(M15K)
R20	22k		(M22K)
R21,25	5k6	2 off	(M5K6)
R23	1M		(M1M0)
R26	560R		(M560R)
R27	1R (1/2W 5% carbon)		(B1R0)
RV1	2M2 lin pot		(FW09K)
RV2	10k lin pot		(FW02C)
Capacitors			
C1,11,12	220nF carbonate	3 off	(WW45Y)
C2,5	6n8 polycarb.	2 off	(WW27E)
C3	15nF polyester		(BX71N)
C4,7	1nF mylar	2 off	(WW15R)
C6	22nF polyester		(BX72P)
C8,9	150nF polyester	2 off	(BX77J)
C10	68nF polyester		(BX75S)
C13	2u2 63V elect		(FB15R)
C14,22	1uF 63V elect	2 off	(FB12N)
C15	22uF 25V elect		(FB30H)
C16	270pF ceramic plate		(WX61R)
C17,20	100uF 10V elect	2 off	(FB48C)
C18,19	100nF polyester	2 off	(BX76H)
C21	47uF 10V elect		(FB38R)
Semiconductors			
IC1,2	1458C	2 off	(QH46A)
IC3	CA3080E		(YH58N)
IC4	741C 8 pin DIL		(QL22Y)
IC5	TBA820M		(WQ63T)
TR1	BC108		(QB32K)
D1,2	1N4148	2 off	(QL80B)
Miscellaneous			
S1	4 way 3 pole rotary		(FF75S)
JK1,2	Standard 1/4in. jack	2 off	(HF90X)
B1	9V PP6 size		(XY45Y)
	Case		(HF28F)
	Battery connector		(HB26D)
	Control knobs	3 off	(GB19V)
	Printed circuit board		(BF06G)
	6BA 1/4in. bolts	1 pkt	(BF18U)
	6BA nuts	1 pkt	(FW34M)
	6BA 1/4in. spacers	1 pkt	(FL24B)
	Veropins type 2145	(as req.)	(BL00A)
	Wire		

A complete kit of all parts, excluding the case and knobs, is available.
Order As LK05F (D'Xers Audio Processor kit). Price £14.95.

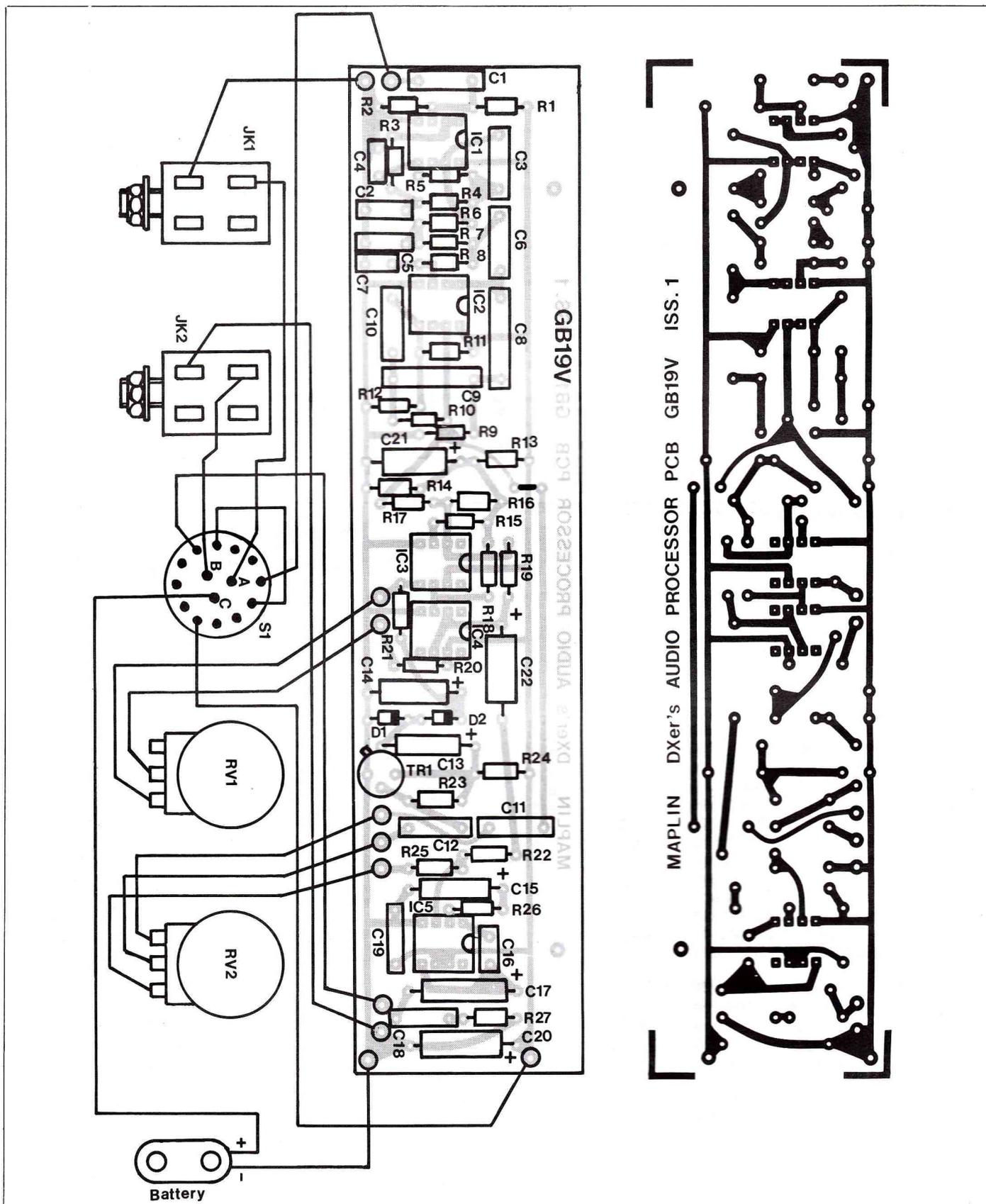


Figure 5. PCB layout and wiring.

Construction

Refer to Figure 5 for details of the printed circuit board and wiring of the unit. Veropins are used at points on the printed circuit board where connections to off-board components will be made. Be careful to fit the semiconductor devices onto the board with the correct orientation, especially the integrated circuits which would be difficult

to remove from the board once soldered into place. Note that there is a single link wire on the board (near to R13 and R16).

An instrument case having approximate outside dimensions of 200 by 125 by 75mm makes a good housing for this project, and a suitable front panel layout can be seen by referring to the photographs. S1 is a 4 way 3 pole rotary type having an adjustable end stop, and the latter is set for 2 way operation. The

recommended case has an aluminium chassis and the completed printed circuit board is mounted on this using ½ inch 6BA bolts plus ¼ inch 6BA spacers to hold the underside of the board well clear of the chassis. Mount the board towards the front of the chassis so that there is sufficient space for the battery to the rear of the board. The unit is then finished by wiring in the controls, battery connector, and sockets.

continued on page 28

With sales of the Commodore 64 steadily rising there must be a vast number of users becoming increasingly frustrated in the knowledge that they are the proud owners of a powerful and yet undocumented machine.

The users manual which accompanies the 64 is extremely basic, and continually makes reference to the Programmers Reference Guide for more information on the concepts of advanced operation. Where is this Oracle? No doubt it will materialise in time, but for all you Commodore 64 owners here are some routines to whet your appetites.

Joysticks

The 64 has two control ports which are controlled by one of two CIA chips. these are 6526's and control the I/O

and interrupts etc. CIA 1 handles IRQ whilst CIA 2 handles NMI. To read the joystick switches use the following

JY = NOT PEEK(56320) AND 15

this will yield 1 for UP, 2 for DOWN, 4 for LEFT, 8 for RIGHT, and the appropriate combinations for the diagonals. To read the fire button use

FB = NOT PEEK(56320) AND 16

(I have used Port B. Replace address with 56321 for Port A.)

High Resolution Graphics

Another feature of the Commodore 64 is its high resolution graphics facility. This is not even hinted at in the manual - so here it is. The screen has its

by Nigel Fawcett

Pixels arranged in a 320 by 200 matrix. In normal operation the screen requires 1000 bytes of RAM to hold the code for each of the 1000 possible character positions. In Bit Map Mode every Pixel on the screen needs to be addressable - 64000 bits are needed and one byte contains 8 bits - so 8000 bytes will be required in RAM to enable high resolution graphics. Program 1 is written in basic to demonstrate this facility.

You will notice that in this mode the screen memory starts at 24K, and the colour memory starts at 16K. The screen will be completely blank, but due to the slow nature of BASIC it adequately demonstrates how the screen is mapped. Program 2 executes the same function in machine code (somewhat faster), and then allows the screen to be used as a doodle pad with a joystick in control Port B.

USING THE COMMODORE 64

```

100 V1=56576:V2=53248
105 RESTORE
110 FOR I=0 TO 42
120 READ A:POKE 832+I,A
130 NEXT I
140 POKE V1,PEEK(V1) AND 254
150 POKE V2+24,8
160 POKE V2+17,PEEK(V2+17) OR 32
170 SYS 832
1000 C1%=0:C2%=0:B1%=0:B2%=0
1010 JY=NOT PEEK(56320) AND 15
1020 IF JY AND 1 THEN GOSUB 11000
1030 IF JY AND 2 THEN GOSUB 12000
1040 IF JY AND 4 THEN GOSUB 13000
1050 IF JY AND 8 THEN GOSUB 14000
1060 IF NOTPEEK(56320) AND 16 THEN 105
1070 GOTO 1010
2000 GOTO 2000
3000 DATA 162,32,160,0,169,0,141,0,96,238,71,3,136,208,245,238,72,3,202,208
3010 DATA 239,162,4,160,0,169,2,141,0,64,238,92,3,136,208,245,238,93,3,202
3020 DATA 208,239,96
10999 RETURN
11000 B1%=B1%-1:IF SGN(B1%)<>-1 THEN 11100
11010 B1%=7:C1%=C1%-1
11020 IF C1%<0 THEN C1%=24
11100 CH=C1%*320+C2%*8+B1%+24576
11110 POKE CH,PEEK(CH) OR (2*82%)
11999 RETURN
12000 B1%=B1%+1:IF B1%<8 THEN 12100
12010 B1%=0:C1%=C1%+1
12020 IF C1%>24 THEN C1%=0
12100 CH=C1%*320+C2%*8+B1%+24576
12110 POKE CH,PEEK(CH) OR (2*82%)
12999 RETURN
13000 B2%=B2%+1:IF B2%<8 THEN 13100
13010 B2%=0:C2%=C2%+1
13020 IF C2%>39 THEN C2%=0
13100 CH=C1%*320+C2%*8+B1%+24576
13110 POKE CH,PEEK(CH) OR (2*82%)
13999 RETURN
14000 B2%=B2%-1:IF SGN(B2%)<>-1 THEN 14100
14010 B2%=7:C2%=C2%+1
14020 IF C2%>39 THEN C2%=0
14100 CH=C1%*320+C2%*8+B1%+24576
14110 POKE CH,PEEK(CH) OR (2*82%)
14999 RETURN
32767 END

```

Program 2

```

100 V1=56576:V2=53248:
140 POKE V1,PEEK(V1) AND 254:
150 POKE V2+24,8:
160 POKE V2+17,PEEK(V2+17) OR 32:
170 FOR X=0 TO 8191:
180 POKE 24576+X,0:
190 NEXT X
200 FOR X=0 TO 1023:
210 POKE 16384+X,1:
215 REM:
220 NEXT X
300 GOTO 300:
32767 END

```

Program 1

```

REM POINTERS TO CIA AND VIDEO CHIPS
REM SET UP CIA CHIP
REM RECONFIGURE SCREEN MEMORY MATRIX
REM ENABLE BIT MAP MODE
REM 8K FOR SCREEN MEMORY MAP
REM CLEAR MEMORY

```

```

REM 1K FOR COLOUR MEMORY
REM SET COLOUR TO WHITE - CHANGE THIS
REM FOR ANY COLOUR CODE 0-15

```

```

REM RUN/STOP & RESTORE TO BREAK OUT!

```



```

1000 POKE 56334,PEEK(56334) AND 254: REM SET UP CIA CHIP
1010 POKE 1,PEEK(1) AND 251: REM SET UP I/O DIRECTION
1020 FOR I=0 TO 2047
1030 POKE 12288+I,PEEK(53248+I): REM COPY THE CURSOR UP MODE CHARACTER
1035 REM: SET INTO RAM STARTING AT 12K
1040 NEXT I
1100 POKE 1,PEEK(1) OR 4: REM RESET THE I/O DIRECTION
1110 POKE 56334,PEEK(56334) OR 1: REM RESET THE CIA CHIP
1200 FOR I=13312 TO 13327: REM ALTER THE CHARACTERS WHICH NORMALLY
1210 READ C: REM HAVE SCREEN CODES 128 & 129
1220 POKE I,C: REM (NORMALLY REVERSE @ AND REVERSE A)
1230 NEXT I
1300 POKE 53272,(PEEK(53272) AND 240)+12
1305 REM: REM TELL THE VIDEO CHIP WHERE THE NEW
1306 REM: REM CHARACTER SET IS
2000 PRINT "C": REM CLEAR SCREEN
2010 PRINT "##### !!!!!!": REM INVERSE @ AND INVERSE A !!!!
3000 DATA 0,0,0,0,3,12,48,192,3,12,48,192,0,0,0,0

```

Program 3

```

1000 POKE 52,48:POKE 56,48:CLR
1010 FOR I=832 TO 860
1020 READ A
1030 POKE I,A
1040 NEXT I
1050 POKE 56334,PEEK(56334) AND 254
1060 POKE 1,PEEK(1) AND 251
1070 SYS 832
1080 POKE 1,PEEK(1) OR 4
1090 POKE 56334,PEEK(56334) OR 1
1100 FOR I=13312 TO 13327
1110 READ C
1120 POKE I,C
1130 NEXT I
1140 POKE 53272,(PEEK(53272) AND 240)+12
30000 DATA 162,8,160,0,173,0,208,141,0,48,238,69,3,238,72,3,136,208,241,238
30010 DATA 70,3,238,73,3,202,208,232,96
31000 DATA 0,0,0,0,3,12,48,192,3,12,48,192,0,0,0,0

```

Program 4

Redefining the character set

The 4K of memory required to generate the 512 characters available resides in ROM starting at memory location 53248. This may come as a surprise to those who are already aware that the video chip controlling the sprites starts at the same address. Reading the character ROM can only be achieved when the I/O chips are correctly configured, as program 3 will show.

For those who were again disappointed by the slowness of BASIC, Program 4 performs the same function using machine code.

These demonstration programs do not by any means explain the full power or capabilities of the Commodore 64. There are many other places in RAM at which the character set can be set up and redefined. This is not the only method of creating a bit mapped screen - multicolour modes have not been shown nor has the ability to fine scroll or mix Hi-res graphics with text - this is just meant as an insight into the possibilities that exist when programming on this machine. Full details will be found in the Programmers Reference Guide and more programs and ideas will be given in future editions of Electronics. Good programming.

D'XERS AUDIO PROCESSORS

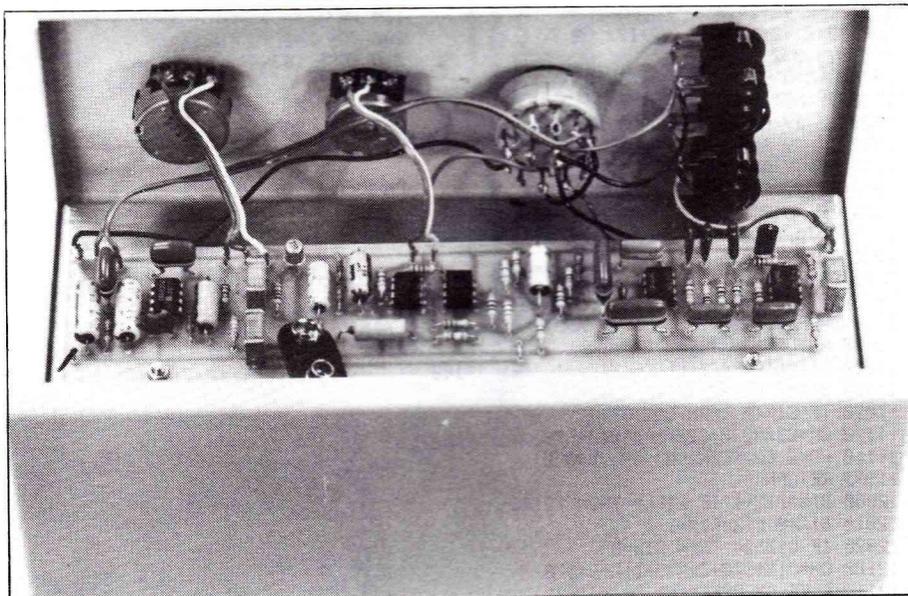
continued from page 26.

In Use

Satisfactory results will probably be obtained if the unit is fed from either a loudspeaker socket or a headphone output of the receiver. If fed from an output intended for low impedance headphones the unit may provide inadequate output for use with a loudspeaker or high impedance headphones. This is not likely to happen in practice, but if necessary R22 could be replaced with a link wire to provide an increase in gain.

The processor will drive any normal type of headphones, but with some low impedance types the output of the unit may be excessive. This can be overcome by adding a resistor of about 100 ohms in value in series with one of the leads to JK2. An 8 ohm impedance loudspeaker can be driven at good volume, and higher impedance loudspeakers are also suitable, but the maximum output power decreases roughly in proportion to any increase in loudspeaker impedance. The use of a speaker impedance of less than 8 ohms is not recommended.

When the expander is not required RV1 is set in a fully anticlockwise direction. It is not advisable to always use the expander section of the pro-



cessor since it will be of little or no benefit if the wanted signal is badly affected by noise or interference, and under these conditions the expander may be unable to function at all. It is not advisable to use the expander when trying to receive a station which is fading badly since the expansion will simply make the fading worse.

If reception conditions are not very poor and the expander is to be used, RV1 is advanced in a clockwise direc-

tion to give the desired degree of expansion (a roughly mid-point setting should be satisfactory). VR2 is then adjusted so that the wanted signal readily operates the expander and is reproduced at full volume, but during pauses in the wanted signal the background noise or interference does not and is consequently attenuated. After a little experimentation there should be no difficulty in setting these controls for optimum results.

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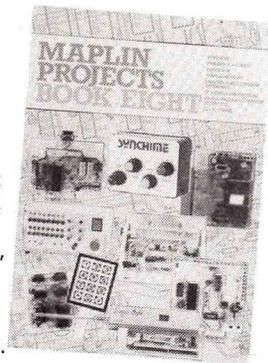
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