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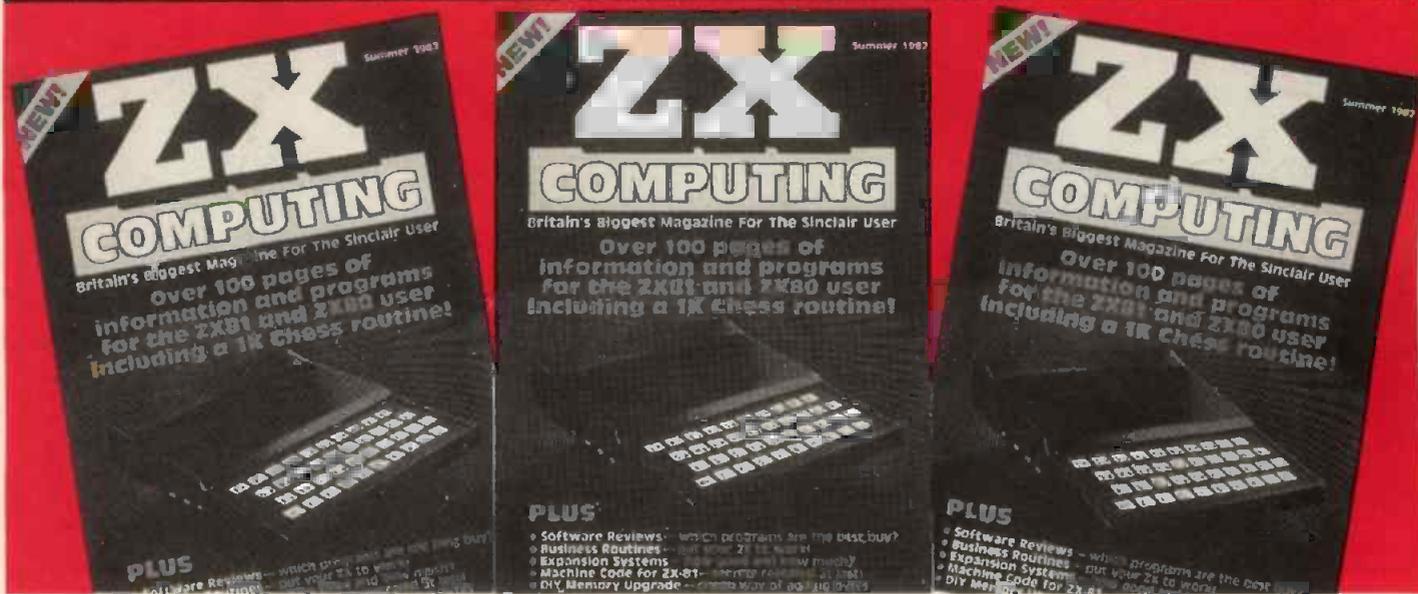
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Designer's Notebook

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Chapter 1

IMPEDANCE AND PHASE

Life would be a lot easier if all components behaved like resistors. Inductors and capacitors make life difficult by separating voltage and current, so how do you find the voltage or current at any point in a circuit? Phase diagrams to the rescue.

IN ELECTRONICS one often needs to know what the voltage of current at some part of a circuit will be, without actually building it to find out. When dealing with DC, this is usually pretty straightforward, using Ohm's law and a few rules of thumb. But AC signals in a circuit are a different matter, often reacting in totally different ways, predictable only by using impedance theory and phase diagrams. It is this type of theory and the calculations used to find voltages, etc., in circuits, that concern this article.

AC Signals

First let's remind ourselves what an AC signal actually is. Plotting voltage against time for a typical signal would give us a graph like that in Fig. 1. This particular variety of round wave is known as a *sinewave*, and in order to fully describe it we must outline two quantities: its rms value and its frequency. The former is a measure of the amplitude, or height of the wave, and for reasons that need not be gone into here, is, in the case of a sinewave, 0.707 times the maximum value of the wave. For instance, if, as in Fig. 1, the wave has a maximum value of 6 volts, the rms value of the signal is $0.707 \times 6 = 4.24$ volts. The other measure of the wave is the frequency. Take the interval between, say, A and B on Fig. 1. This interval, from one point to the next point where the voltage is acting in exactly the same way (in this case, from a point where it is zero and decreasing to the next point where it is both zero and decreasing) is called the period of the wave and is measured in seconds. During one period, the wave is said to have gone through one full cycle. The frequency of the wave, we can now say, is the number of cycles per second.

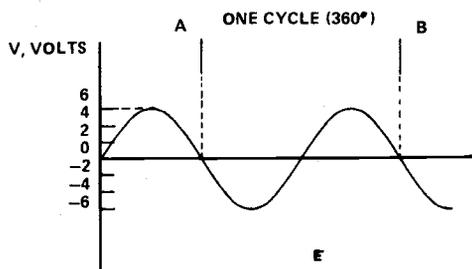


Fig. 1. A voltage/time graph for a typical AC signal.

Impedance

Impedance can be described as the *opposition to electrical current given by a circuit*. Of course, we know about ordinary resistance, but there are other varieties. For instance, a capacitor may have a very high opposition to DC current, but a very low opposition to AC signals of a suitably high frequency. This obviously isn't ordinary resistance, because if it was, it would remain the same for AC and DC. In fact, the amount of opposition given to a signal by a capacitor is measured by the ratio of voltage across it to current through it (V/I). This ratio is called the 'capacitive reactance' of the component, and is given the symbol X_c . Like resistance, reactance is measured in ohms. Capacitive reactance may be calculated from the value of a capacitor by using the formula $X_c = 1/2\pi fC$, where π is the Greek letter Pi, and

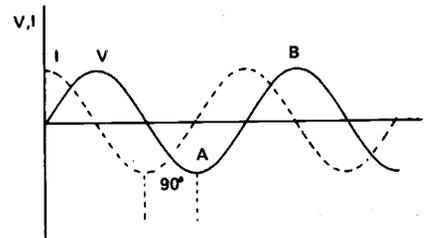


Fig. 2. Current and voltage plots for a capacitor, showing a phase difference between the two.

represents the number 3.14 . . . , f is the frequency of the signal being applied, and C is the value of the capacitor in Farads. Note that, as stated earlier, the opposition (reactance) of the capacitor becomes very small at high frequencies, but to DC (where the frequency is effectively zero) or to very low frequency signals, it becomes effectively infinite.

Inductors, too, have a variable reactance; in this case, the inductive reactance, X_L , which may be obtained from the value, L , in Henries of the inductor, from the formula $X_L = 2\pi fL$. Note that this reactance also varies with frequency, but here, it becomes greater at high frequencies, approaching zero only when f is very low, or when DC is encountered. Again, X_L is the ratio V/I in the inductor, and thus, given either the voltage or the current, it is possible to calculate the other in either a capacitor or an inductor, if we know the frequency at which the circuit is operating.

To conclude this section, we now give a rather more adequate definition of impedance than that which we began with. Impedance is the combined opposition to AC signals in a circuit given by the resistance and reactance of the circuit. If we represent it by Z , the resistance by R , and the reactance by X , then $Z = \sqrt{R^2 + X^2}$. We find that, in a combination circuit of several components, $Z = V/I$.

Phase Differences

In addition to information about voltages and currents in circuits, phase diagrams also give us information about phase differences in these circuits. What in the world is a phase difference? To answer that, we must return to the capacitor and inductor. Suppose that we are applying an AC voltage across a specimen of the former type of component. If we now look at the current flowing through it, we find that it is 'leading' the voltage by a quarter cycle. That is, although it goes up and down in the same way that the voltage does, the two quantities are not in time with each other. If the voltage has, say, gone up (as from point A to point B in Fig. 2), then the current did so 90° , or a quarter of a cycle earlier. (The figure 90 is used because a full cycle is taken as being divided into 360 degrees, as a circle is, and one quarter of a cycle is therefore, represented by $\frac{1}{4} \times 360 = 90$. The reason for dividing a cycle into 360 degrees will become apparent later). If we superimpose a graph of current against time on top of one of voltage against time, we get something like Fig. 2.

In the inductor, a similar effect occurs, but here it is voltage which leads current by 90° , rather than vice versa.

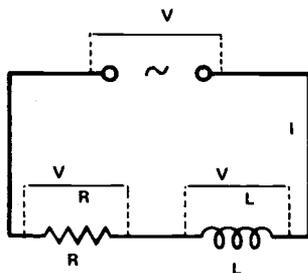


Fig. 3. A series circuit with a resistor and an inductor. Do you use voltage or current as the reference quantity?

The 'phase difference', as it is called, is given both in the case of the capacitor and the inductor, the symbol ϕ — the Greek letter Phi — and may also be measured in terms of radians, another unit of angle, rather than degrees.

To help remember that voltage leads current in the inductor, whereas current leads voltage in the capacitor, the mnemonic CIVIL is used. In a capacitor, (C) current (I) leads voltage (V), but voltage leads current, (I) in an inductor (L). Taken in order, the one-letter symbols for the components, voltages and currents spell CIVIL. (All right — I didn't think of it.)

Phase Diagrams

So far we have seen how voltage and current are related in terms of magnitude (size) and phase, in individual components. What happens, though, if we put two different components — a resistor and inductor — for example, in series or parallel? This is where the phase diagrams step in, folks.

Phase It

Let us suppose that these two components, each of known value, are connected in series, and that we know the current which is flowing through the combination, and this current's frequency. We wish to find the size and phase of the total voltage across the two components, and we might be misled into thinking that it would be just the sum of the two individual voltages across the individual components, but in fact, this will not be so. The current and voltage will be exactly 'in phase' in the resistor, but in the inductor, the voltage will be 90° out of phase; you can't just add voltages unless they are in phase with each other. Of course, we could find the magnitude of the total voltage by finding the total impedance of the circuit and multiplying this by the current, but we still wouldn't know the phase of this voltage with respect to the current, so a phase diagram is really our only option.

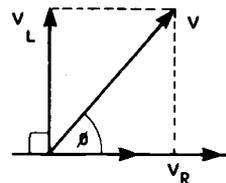


Fig. 4. The voltages across the resistor and inductor can be used to find the total voltage across the two components.

Which Reference

For our diagram, we shall want some quantity, either voltage or current, which will be the same for both components. Well, as we have just seen, the voltages across the individual components are definitely different, so that only leaves current. In fact, current serves as our 'reference quantity' in any series circuit, and voltage is used in parallel circuits. To represent the current, draw an arrow, pointing to the right. Now we must draw in arrows to represent the voltages across individual components. The lengths of these arrows will be made, using a suitable scale, to represent the rms values of the voltages. The phase of each voltage with respect to the current will be indicated by the angle, going anti-clockwise, which the voltage's arrow makes with that of the current, when both have their tails at the same place. Thus, the voltage across the resistor, which can be calculated by multiplying the current by the resistance, will be represented by an arrow actually on top of that showing the current, because the voltage and current here are in phase, so that the angle, ϕ , is zero. The voltage across the inductor can be calculated by finding the reactance of the component, and multiplying this by the current. This arrow will be placed at an angle of 90° to that representing the current (ie. it will point straight up), because the voltage in an inductor leads the current by 90° . Were the component a capacitor, ϕ would be -90° , because the voltage here lags by a quarter cycle, which is equivalent to saying that it leads by -90° . The arrow would, then, point down, rather than up, as it does now.

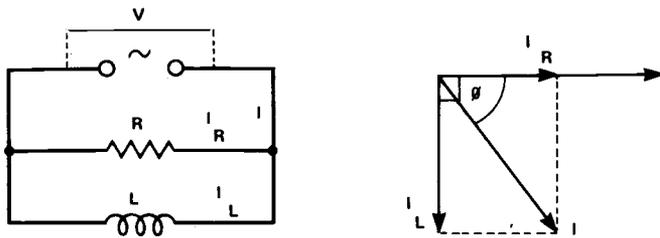


Fig. 5a. A resistor and an inductor in parallel. In this case voltage is used as the reference quantity. (b) The phase diagram for a parallel L-R circuit.

If we imagine our two voltage arrows to be two sides of a parallelogram (in this case, a rectangle, because we know that one of the angles is 90°), and draw in the other two sides parallel to the ones we have, as in Fig. 4, we find that the diagonal of the rectangle, drawn in as an arrow starting at the same place as do all the others, has a length that, on whatever scale we have used to draw the lengths of our arrows, gives the total voltage across the two components. In addition to this (yes, you guessed it) we find that the angle which this diagonal arrow makes with the horizontal gives the phase of the total voltage across the circuit, with respect to the current!

In fact, if we use Pythagoras' famous theorem about the squares of the lengths of the side of a right angled triangle (whew!), to find the length of this diagonal we find that, if we call the voltage across the resistor V_R , and that across the inductor V_L , then the total voltage, V , is given by the formula:—

$$V = \sqrt{V_R^2 + V_L^2}$$

Looking back to the section on impedance, we notice that this formula bears a remarkable resemblance to the one stated to give the combined impedance of a resistance and reactance; in fact, if we divide both sides of the equation by the current, I , then V becomes Z , V_R becomes R and V_L becomes X_L (since Z , R and X_L are all defined to be equal to V/I) and the two equations become one and the same (Howzatt!!!).

The phase of the voltage can also be calculated, rather than measured directly from the diagram. The appropriate formula is:—

$$\phi = \tan^{-1} V_L/V_R.$$

What about parallel circuits? The procedure this time is pretty much the same as for series circuits, but now the 'reference' arrow, pointing to the right, represents the total voltage, not the current. The individual arrows represent the currents through the individual components, rather than the voltages, and the diagonal arrow gives the total current, and the angle by which the current leads the voltage. Note that if this angle is multiplied by -1 , it then gives the angle by which voltage leads the current.

LC Circuits

There are two more circuits, that should really be treated by themselves. These are the combination of capacitor and inductor in series or parallel, and they possess some rather interesting properties. If we draw a phase diagram for either of these two types of circuit, we find that the two

arrows representing voltages or currents, as the case may be, in the individual components point in exactly opposite directions. To find the arrow that is the combination of these, we place the arrows end to end. That is, we place the tail of one of them at the head of the other, keeping them pointing in the same directions. An arrow starting at the beginning of the first individual one, and ending where the second arrow does, gives the total voltage, or current. It can be seen from this that if $V_C = V_L$, then the two will exactly cancel out, and in a series circuit, there will be no voltage across the two components, and the circuit will be effectively shorted across. In a parallel circuit, there will be no current flowing, and the total impedance of the circuit will be effectively infinite. Under what circumstances, then we may ask, will the two voltage (or current) arrows be of equal length, and cancel? It turns out that this is so if $X_C = X_L$, and using the formulae for the reactances of the

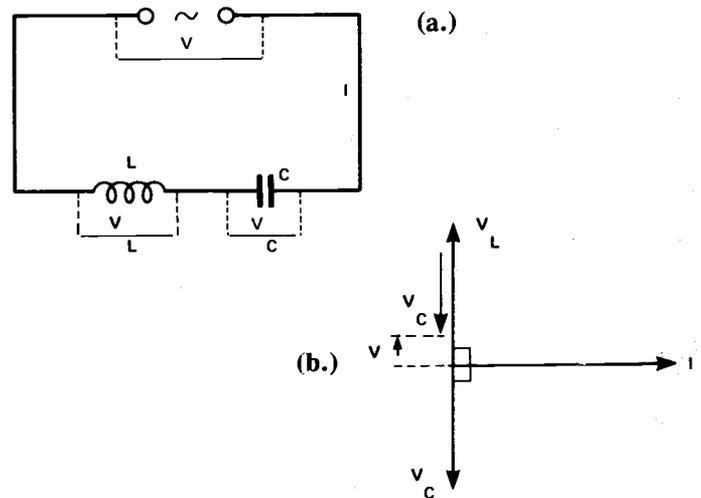
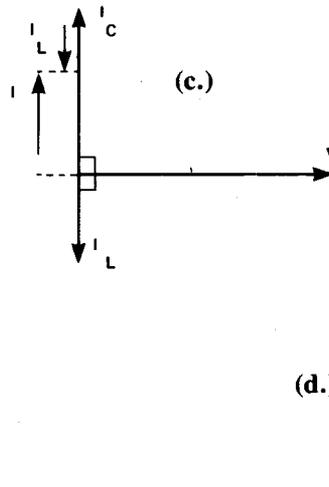


Fig. 6a. A series L-C circuit, where current is the reference. (b) Phase diagram for the series L-C circuit. Inductor and capacitor voltages are 180° out of phase. (c) A parallel L-C circuit. (d) With voltage as reference, inductor and capacitor currents are 180° out of phase.



components, from the section on impedance, we find that $2\pi fL$ must equal $1/2\pi fC$. Here we notice that for any named combination of values for L and C , it should be possible to find some frequency – the so called *resonant frequency* – for which the circuits should react in the way described above. Manipulating the equations, we come up with the formula:—

$$f = 1/2\pi\sqrt{LC}$$

Thus, in a series circuit, signals at this, and only this, frequency, will be able to pass through the circuit unimpeded, whereas in a parallel circuit, any other frequency will be allowed to pass. These circuits are called, respectively, a notch filter and a tuned circuit. The latter is of great use in radio receivers, where it is often used to short all signals at frequencies other than those wanted to earth. thus effectively sorting out wanted signals to be amplified and listened to. The frequency required may be selected by adjusting one or other of the two components, and, in fact, the capacitor in the tuned circuit of a radio is usually a variable type, and forms the tuning control.

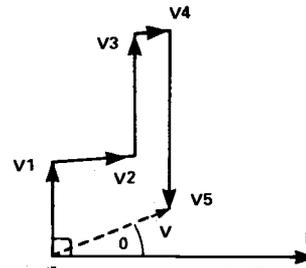


Fig. 7. In circuits with more than two components, the voltage or current arrows for the individual components can be found, then the final arrow will give the total voltage or current.

Two's Company . . .

Of course, you may want to find voltages or currents in circuits with more than two components, but this isn't as difficult as you might think. Just find the individual arrows of the separate components, and put them all end to end, as in Fig. 7. The final arrow, giving the total voltage or current, starts at the beginning of the first and ends where the last of the separate arrows does.

SPOT DESIGNS

Reverberation Unit

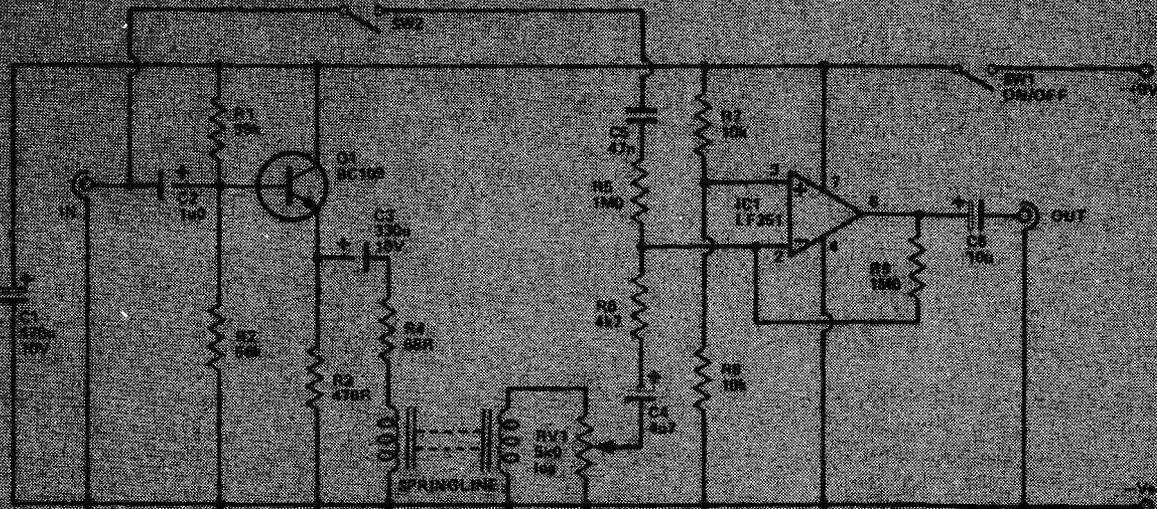
THIS UNIT SIMULATES the long reverberation time of a large hall (about 2.5 sec) and can be employed as a musical effect unit or as a special control type of home-recording. Reverberation is caused by sound being reflected around the interior of a room and in the case of a large hall the sounds are usually reflected many times before being sufficiently weak to render them inaudible. This, coupled with the fairly long distance covered by the sound waves between reflections, gives the long reverberation time, and reverberant sound of a large hall.

There are several ways of simulating reverberation, but the simplest and most commonly used is probably the springline based system. A springline consists of two transducers linked by one or two long springs. If a signal is fed into one transducer it produces a corresponding audio signal which is transmitted down the spring to the second transducer. Here it is reconverted into an electrical signal again. However, the sound signal travels

down the spring relatively slowly, and the signal is reflected backwards and forwards along the spring many times before it decays to an insignificant level. Thus, the output from the second transducer is a good simulation of natural reverberation.

In this circuit the input signal is fed to the low impedance input transducer of a short springline via an emitter follower which gives a reasonably high input impedance of about 10k or so. This uses Q1 in a conventional configuration. The output of the springline unit is fed to one input of a mixer circuit. This is based on IC1 and again uses a conventional and well known arrangement. There are substantial losses through the springline and so the mixer is designed to boost the output of the springline by over 46 dB (200 times). The other input of the mixer is fed with the input signal, but the high value of R5 gives only about unity voltage gain at this input, so that the main signal does not overwhelm the reverberation signal.

RV1 enables the amount of reverberation signal mixed into the main signal to be controlled. It can be reduced right down to zero by fully backing off RV1. SW2 can be used to cut out the main signal so that only the reverberation signal appears at the output, if desired. The only other control is on/off switch SW1. The current consumption of the unit is approximately 10 mA.



Chapter 2

ANALOGUE DELAY LINES

Don't do now what you can put off for a few milliseconds. Need to delay a signal? Here's how to do it, plus suggested applications for analogue delay lines.

THERE ARE MANY natural phenomena which are 'caused' by time delays. All acoustic instruments and, in fact, everything in acoustics is time related. It is, therefore, hardly surprising that several manufacturers produce electronic time delay integrated circuits. These are called *analogue delay lines* or sometimes, 'bucket brigade delay lines', as this accurately describes their operation.

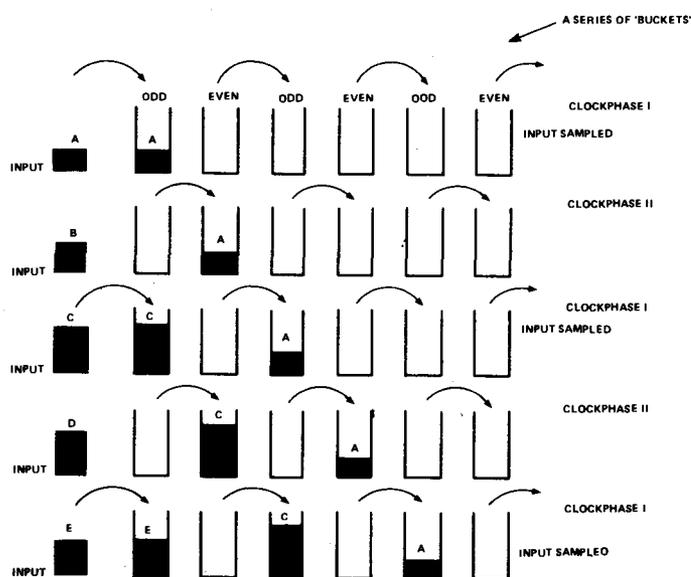


Fig. 1. Bucket Brigade delay lines.

Quantum Buckets

The device can be thought of as being a series of buckets containing water. (Actually it is a series of capacitors containing charge). The signal presented to the input fills up the first bucket to the level of that signal. This occurs on phase I of a controlling clock signal. On the second clock (phase II), all the *odd* buckets tip their water into the *even* buckets. No input sampling occurs on clock phase II. On the next clock phase (phase I) the input is sampled and all the *even* buckets tip their water in the *odd* buckets. In this way a signal propagates down the delay line which represents the input signal as a series of 'samples'. The buckets are really analogue sample and hold units and the tipping is

done with electronic switches. This technique is a cross between analogue and digital processes. The charge stored (which is proportional to the input voltage) is truly analogue, but it is quantised into small units of time and so, in that sense, it is digital. If the delay line is, say, 512 stages long and the clock frequency is 512 Hz, then the delay time will be

$$\frac{\text{number of stages}}{2 \times \text{clock frequency}} = 0.5 \text{ sec}$$

That is, after 0.5 sec a waveform representing the input signal of 0.5 sec earlier will appear at the output. In the example shown in Fig. 1, this signal would only appear at the output for the duration of clock phase II. To fill in the

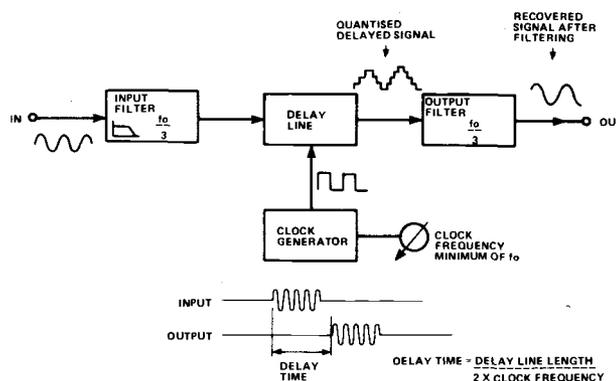


Fig. 2. Block diagram of a typical delay line system.

gaps, a second delay line connected in parallel with the first, but clocked in antiphase, is used, so that a delayed output signal appears on both clock phases.

Delay lines would seem to solve a myriad of electronic problems but with every solution comes a host of new problems. First, the maximum bandwidth of the delayed signal is proportional to the clock frequency. As the signal is sampled, then the 'sampling theorem' says that the signal bandwidth must be less than half the sampling frequency, which, for practical purposes, means about one-third. So, if you want to delay an audio signal of 10 kHz bandwidth by 1 second, then the number of stages delay needed is 60,000. This will cost you a few hundred pounds in delay lines. If

you choose a lower clock frequency requiring fewer delay lines then you will have to make do on a reduced bandwidth. If this bandwidth is not controlled by use of an external lowpass filter, then a phenomenon called *aliasing* occurs which makes the delayed signal sound as if it has been 'ring modulated'. A typical delay line structure is shown in Fig. 2. A lowpass filter is used to band limit the input signal which prevents the aliasing effects. A second filter is used to recover the quantised output from the delay line by rejecting all the unwanted high harmonics.

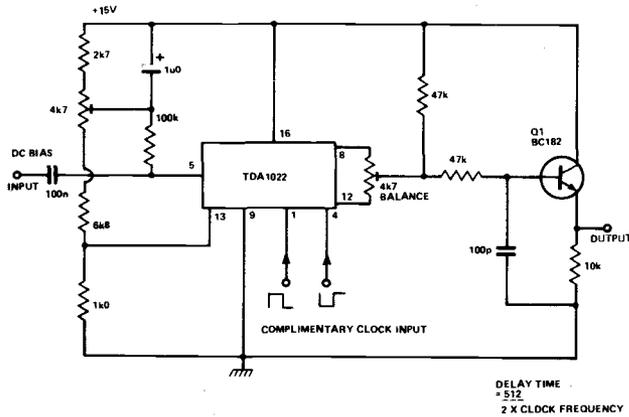


Fig. 3a. A delay line circuit based on the TDA 1022.

The input signal level is always larger than that of the output signal because the buckets are leaky, although the leaks occur in both positive and negative directions. Also, the slower the clock frequency the longer the leakage time is and so the loss is greater. This is a major noise generating mechanism. The noise is broad band, being strong in low frequencies (just the area you are listening to), and becomes louder and more bassy as the clock frequency is reduced. This results in signal to noise ratios of about 70 dB for maximum frequencies. To overcome the poor performance at low frequencies, a noise reduction system such as a compander can be used. The distortion caused by delay lines is typically about 1% and the overload characteristics are not at all good. Heavy overloads can cause the delay lines to stop producing any output at all. The solution is to limit the input level, with some simple sort of diode limiting. One other gremlin is that the output DC level varies with clock frequency which causes some awkward break-through effects. However, once you are fully aware

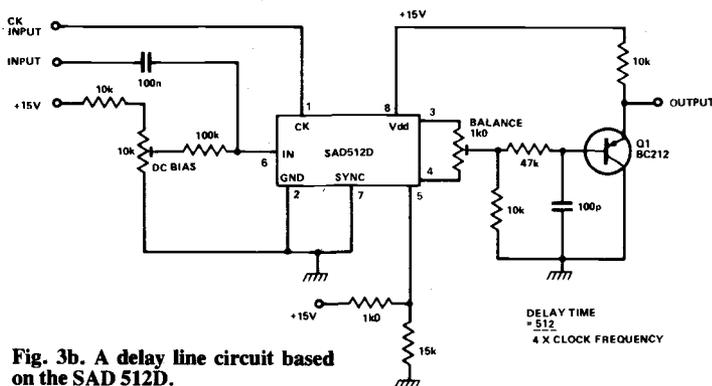


Fig. 3b. A delay line circuit based on the SAD 512D.

of the limitations of delay lines, it is possible to design a wide range of interesting devices. Delay lines work surprisingly well when you consider that they move a very small packet of charge through several hundred memory stages with a corruption of only one part in 10,000 to 100,000!

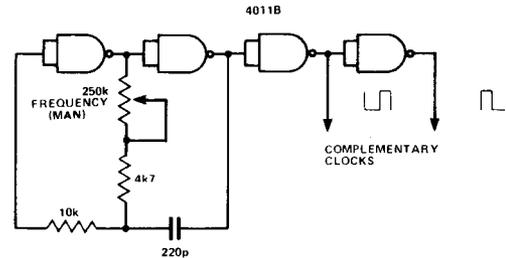


Fig. 4a. A standard CMOS relaxation oscillator.

Some Delay Line Circuits

Two delay line circuits are shown in Fig. 3. The top one uses a delay line made by Mullard/Signetics. A two phase clock is needed. A preset adjusts the input DC bias so that when the device is overloaded, the clipping is symmetrical. A balance control on the output balances the two outputs for a minimum clock breakthrough. This preset is particularly useful when long delay times with audible clock frequencies are used.

The second delay line is the SAD512D made by Reticon. This device has the same two preset controls but only requires a single clock signal. There is a complementary clock generator (a divide by two flip-flop) on the actual IC. The input clock must therefore be twice the calculated frequency.

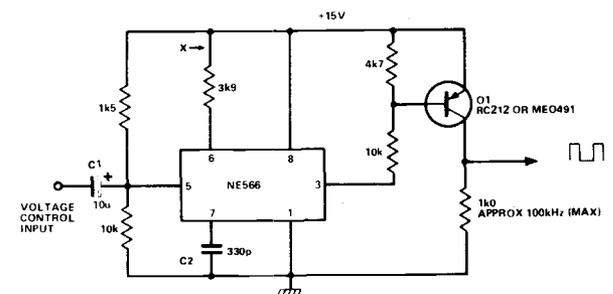


Fig. 4b. The frequency of this clock generator is determined by C1.

If long delay times are needed then there is the Reticon R5101 which will give you a 1 second delay at about 500 Hz bandwidth. This device gives a superb automatic double tracking effect (50 mS at 10 kHz bandwidth) but unfortunately it's rather expensive.

Clock Generators

A selection of clock generator circuits is given in Fig. 4. Circuit A is a standard CMOS relaxation oscillator. The IC costs only about 30p and generates complementary squarewaves; the minimum frequency of operation is about 1 MHz (with a suitable timing capacitor) and the manual

The following examples show delay line systems. The boxes depicting delay lines include suitable filters.

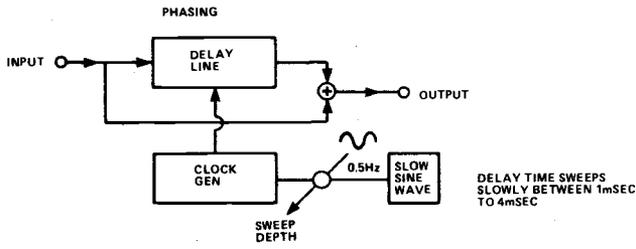


Fig. 7. Note that a long time delay produces lots of notches, a short time delay, only a few. A very popular musical effect is phasing. This uses a slowly sweeping comb filter. That is, the delay time, and hence the notch spacing, are modulated with a slow moving sine wave.

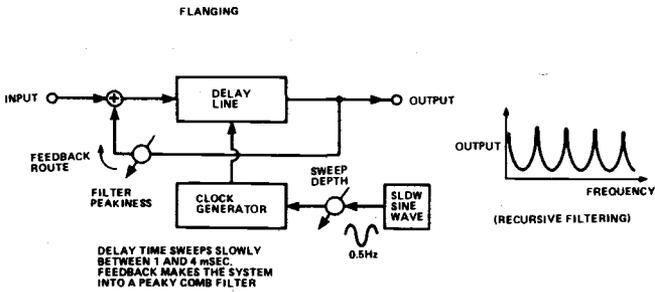


Fig. 8. Flanging is another similar effect, except that feedback is applied around the delay line. When this feedback is in phase with the input, a peak in the frequency response is generated. A pot is used to control the feedback and hence the amount of 'peakiness' of the filter. Flanging produces very strong colouration of the sound.

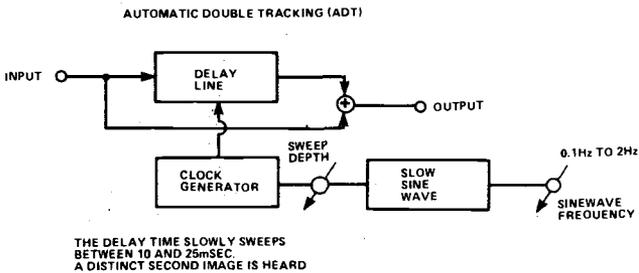


Fig. 9. Automatic double tracking (ADT) is used to add depth and a chorus quality to solo singers and musicians. The delay time is relatively long so that a distinct second image is heard. This image is slowly swept backwards and forwards in time thus adding to the chorus quality. It is such a useful effect that even my singing sounds good!

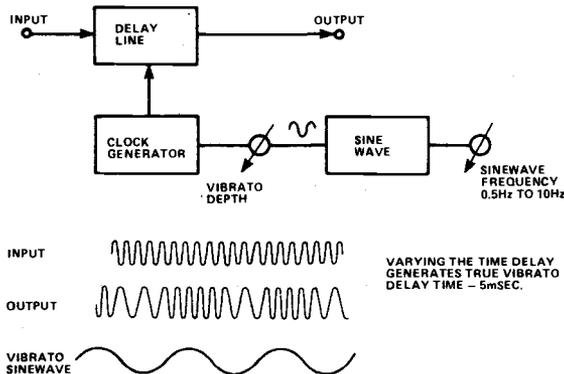


Fig. 10. A 'true vibrato' system. This produces a real frequency modulation acting upon all of the input signal. By rapidly modulating the clock generator frequency the time delay is similarly modulated. This causes the output signal to be compressed and expanded in time, resulting in vibrato.

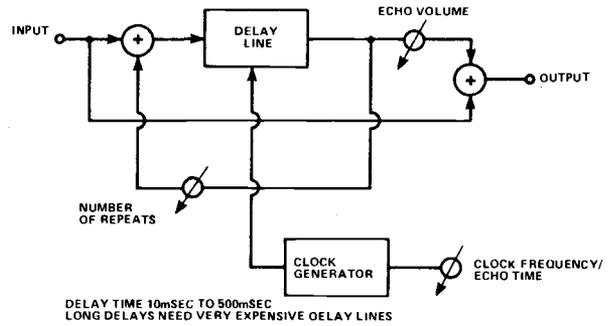


Fig. 11. All electronic echo is obtainable using long delay lines, although you generally have to trade off bandwidth for echo time. Electronic echo systems usually have three controls; time delay, echo volume and repeat level. This last control enables you to vary the echo from a single slap back echo to a long series of repeats.

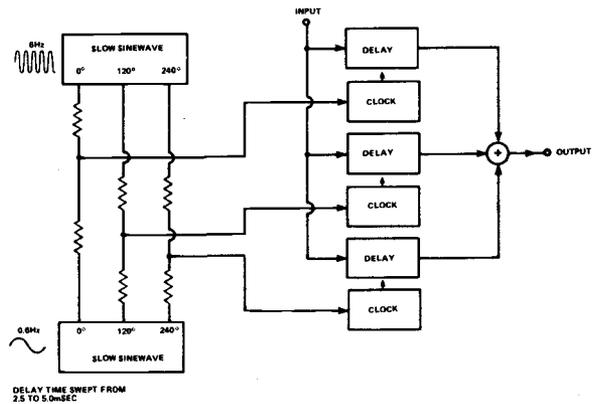


Fig. 12. Electronic string machines nearly always have a chorus/ensemble generator. This is a device that causes complex phasing on the string signal that converts it from a rather flat electronic signal to a rich string-like sound. This is done with three delay lines that have their delay times modulated by three low frequency sinewaves.

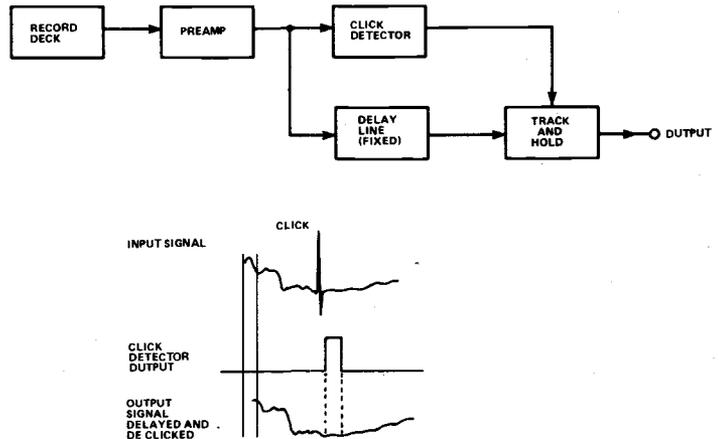


Fig. 13. It is possible to remove record scratches and clicks using a delay line. A scratch on a record is a relatively easy signal to discriminate from the music. However, once the scratch has been detected, the sound of the scratch has already left the loudspeakers and so it is too late to do anything about it. However if the sound is delayed then the scratch can be 'snipped out' using a track and hold circuit. The resulting gap is far less objectionable than the original scratch.

Chapter 3

RADIO PRINCIPLES

Dispelling rumours about a very widely misunderstood subject, *Radio . . .* including such diverse subjects as Varicap Tuning and Stereo FM.

OF THE TWO sound broadcasting systems, the AM (amplitude modulation) system is capable of far greater range of reception than the FM (frequency modulation) system. This has nothing to do with the type of the modulation but is related to the carrier frequencies involved. FM sound radio uses a part of the VHF (very high frequency) spectrum called Band II and covers approximately 88 to 108 MHz, though all of this is not yet used in the UK specifically for entertainment radio.

AM radio broadcasting occupies the long, medium and short wavebands which range respectively from about 50 kHz (6,000 metres) to 600 kHz (500 metres), 600 kHz to 1.5 MHz (200 metres), and 1.5 MHz to 300 MHz (1 metre). Conversion from frequency to wavelength merely involves dividing the propagation velocity (virtually 300 metres per microsecond) by the frequency, or from wavelength to frequency by dividing the velocity by the wavelength.

With increasing carrier frequency the waves tend more closely to follow the laws of light, and at VHF they emanate from the top of the transmitting aerial in rather the same way as light is radiated from the top of a lighthouse. They are less affected by obstructions, though, and are more prone to diffraction and refraction than light which to some extent allows them to pass round obstacles and penetrate walls, etc, but this accommodation is diminished at even higher frequencies. The reception distance of VHF waves, therefore, is limited to a little in advance of the 'line of sight' distance between the transmitting and receiving aerials, the extra being provided by atmospheric refraction and diffraction round the curved Earth.

On Reflection

However, VHF waves are less reflected back to Earth by the ionosphere, and most wave energy skyward-bound penetrates the ionosphere and vanished into space – which is just as well for space communications! At the lower AM broadcast frequencies the ionosphere acts more like a 'mirror' to the signals, which not only prevents them getting into space but it also reflects them back to Earth over ranges far in advance of the 'line of sight' distance. World-wide reception is thus possible by the waves undergoing a number of 'hops' between ionosphere and Earth.

At certain frequencies ionospheric reflection is enhanced as night falls which means that signals well outside the basic reception range appear and are likely to cause interference with the signals from wanted local stations. To some extent this is avoided by an international agreement of wavelength

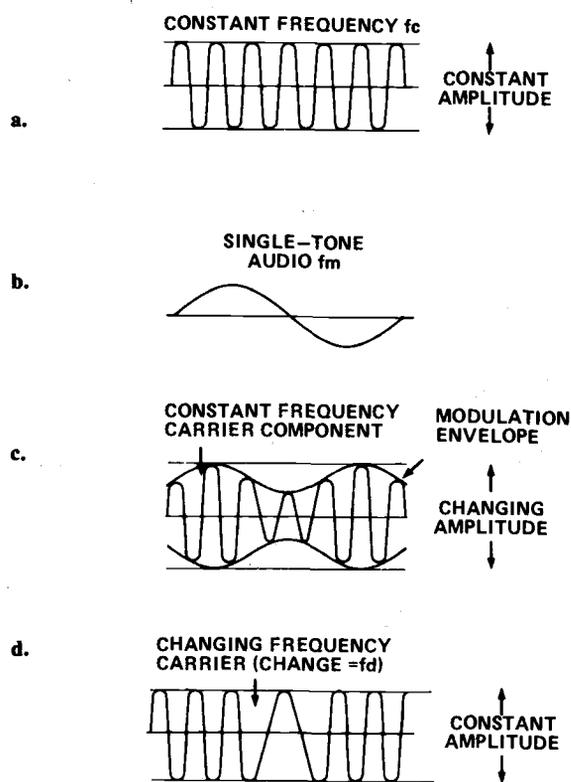
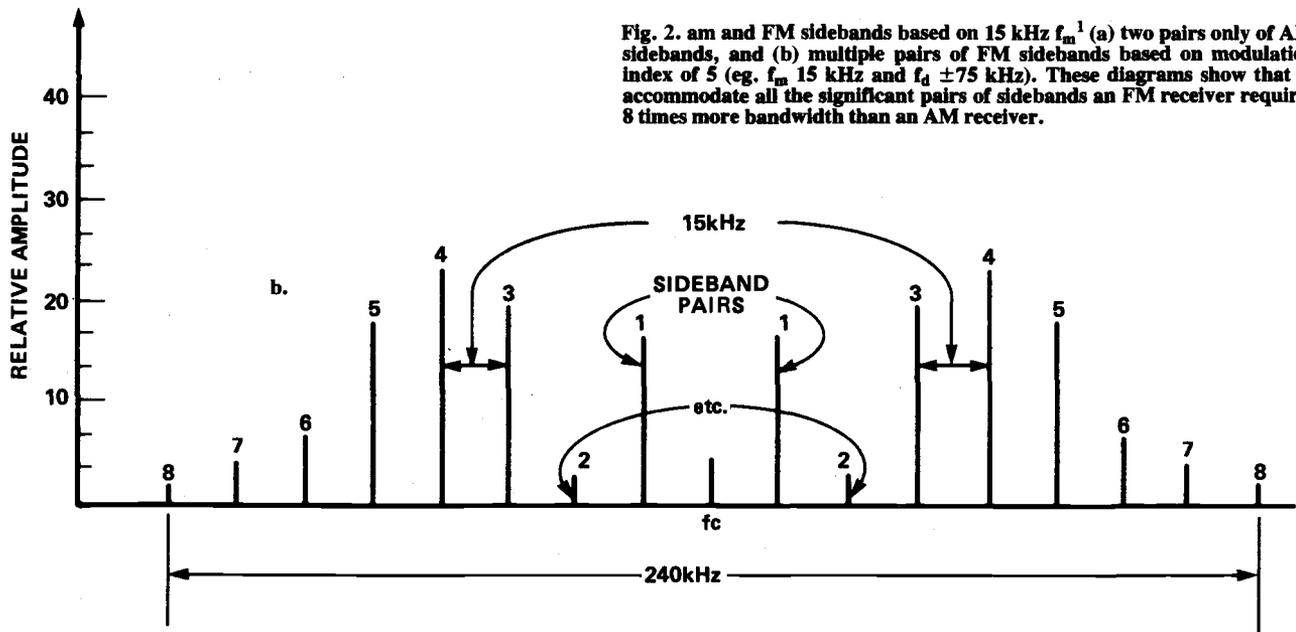


Fig. 1. Impressions of modulation (not to scale). (a) carrier wave, (b) single-tone modulation signal, (c) AM waveform, and (d) FM waveform.

spacing; but because there are so many medium-frequency stations to take account of, the spacings cannot be very wide. To reduce the effect of interference, the bandwidth of AM receivers is restricted. As this attenuates or deletes the higher-order sidebands, the quality of the reception is impaired. This is not necessary at FM because the stations can be adequately separated in Band II without the fear of distant stations producing signals which could interfere with those of the wanted signals. Moreover, FM has a far better immunity than AM as far as this sort of interference is concerned.

The FM system, therefore, is capable of far better audio quality than the AM system as it is currently exploited. It also carries an additional channel of information for stereo reproduction and is thus a 'hi-fi' broadcasting system as will be explained.



Sidebands

Audio information at AM is carried by the carrier wave being caused to change in *amplitude* in sympathy with the sound. The stronger the sound, the greater the amplitude change; and the higher the audio frequency the faster the rate of amplitude change.

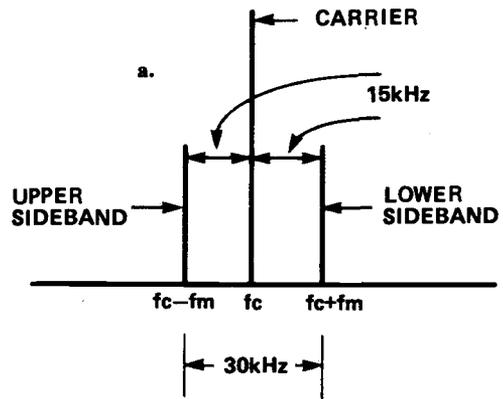
At FM it is the *frequency* of the carrier that is altered in sympathy with the sound. The stronger the sound, the greater the frequency change; and the higher the audio frequency the faster the rate of frequency change.

It is always instructive to look at a carrier wave modulated by a single-tone audio signal, as in Fig. 1, where at (a) we have the carrier, at (b) the modulation tone, at (c) the resulting AM signal and at (d) the resulting FM signal (not drawn to scale, of course!).

One-hundred percent AM occurs when the carrier amplitude dissolves to zero at the troughs of the modulation envelope. If the modulation level is increased beyond this point very severe distortion sets in owing to the carrier holding at zero for a period of time. With FM sound broadcasting 100% modulation is said to occur when the change in carrier frequency is ± 75 kHz on audio signal peaks. This is called the deviation frequency (f_d). It is noteworthy that with 625-line TV sound, which is also FM, f_d includes both the mono and stereo information, the latter occupying approximately 10% of f_d , so that approximately ± 67.5 kHz is available for the mono part.

Modulation

When a carrier wave (f_c) is modulated, sideband signals corresponding to every component frequency of the modulation signal (f_m) result. With AM and a pure single-tone f_m upper and lower sidebands at $f_c - f_m$ and $f_c + f_m$ occur, as shown at (a) in Fig. 2. With FM the resulting sideband structure per pure single-tone of f_m is far more complicated, as shown at (b). At 100% AM each of the sidebands is 50% greater in amplitude than that of the unmodulated carrier; but with FM f_d as well as f_m determine both the amplitude and number of the sidebands. Ratio f_d/f_m is the *modulation*



index which has a value of five at full deviation by the top audio frequency (15 kHz).

Fig. 2 (b) shows that FM yields a sideband structure which spreads out either side of the carrier over a far greater spectrum than AM, and for the least distortion all sideband pairs above 1% amplitude must be accommodated by the receiver. The multiple sidebands result from the change from sinusoidal form of the carrier as its frequency is changed by f_m , and Bessel functions are used to determine the sideband amplitudes and frequencies for any modulation index. It is not proposed to become involved in the deep mathematics of this, but it can be so proved that for top quality mono the bandwidth requirement is about 240 kHz, and a little greater than this for the best stereo.

Assuming a top modulation frequency of 15 kHz at AM, the total bandwidth requirement is a mere 30 kHz, some 8 times less than for FM. Sadly, 30 kHz spacing between stations just cannot be accommodated in the highly congested medium-frequency scene, and to avoid adjacent station

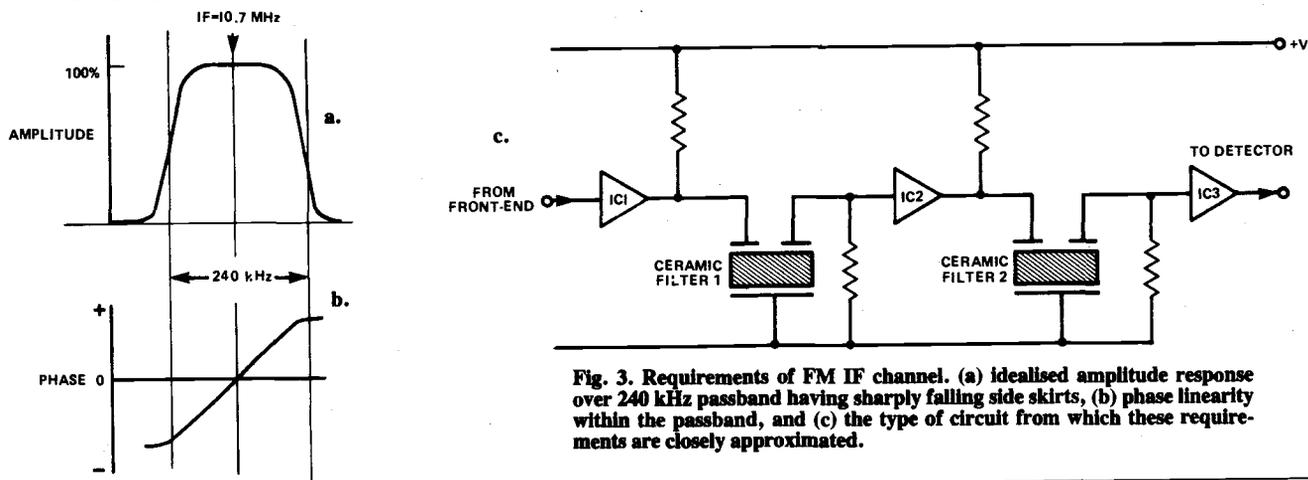


Fig. 3. Requirements of FM IF channel. (a) idealised amplitude response over 240 kHz passband having sharply falling side skirts, (b) phase linearity within the passband, and (c) the type of circuit from which these requirements are closely approximated.

interference the receiver bandwidth needs to be curtailed to 7 or 8 kHz at best with a consequent attenuation of the upper audio frequencies.

The Capture Effect

With FM, channel spacing is 200 kHz (there is much more elbow room at VHF), and local station groups use far greater spacings between transmitters (2.2 MHz) so there is very little danger of interference. Moreover, FM exhibits what is called the *capture effect* which itself avoids interference provided the wanted signal is a little stronger than the unwanted one, even when the two stations have the same frequency! This results from the insensitivity of an FM receiver to amplitude variations of the carrier. When two signals interact one tends to amplitude modulate the other, which means that on AM the wanted signal needs to be very much stronger than the interfering one to give the same interference immunity as FM.

Receiver Requirements

From Fig. 2 it is dramatically apparent that an FM receiver requires much more bandwidth than an AM counterpart to do full justice to the high quality audio signal. The bandwidth needs to be reasonably phase-linear to ensure the least distortion at high modulation index and for the best stereo performance (channel separation, distortion, etc). Latter-day creations employ phase-linear quartz, ceramic and surfacewave acoustical filters to achieve these requirements, as distinct from the earlier LC transformer couplings, as shown in Fig. 3.

To help maintain a high S/N (signal-to-noise) ratio the VHF front-end must employ low noise-figure transistors, especially for the RF (radio-frequency) amplifier, and have a good coupling match to the VHF aerial. Most of the

selectivity and response tailoring is undertaken in the IF (intermediate-frequency) channel at the standard IF of 10.7 MHz. Even so, a reasonable degree of front-end selectivity is desirable to restrict the amplitude of off-tune VHF signals arriving at the mixer from the aerial. A multiplicity of fairly strong signals here can generate intermodulation products of the 3rd-order variety and hence produce spurious which might detract from the quality of the wanted signal. RFIM (radio-frequency intermodulation) immunity is achieved by using two or more variable-tuned circuits between the aerial and mixer and VHF transistors of good linearity (eg. bipolars running at fairly high emitter current or FETs).

One important aspect of 3rd-order RFIM lies in the production of an interfering signal of $f_2 + f_4 - f_3$ where f_2 , f_3 and f_4 correspond to Radios 2, 3 and 4. This interfering signal lies in the f_3 transmission and is perturbed by the modulation of any of the three transmissions. In bad cases of this interference (stemming from a receiver with a poor RFIM performance) the only solution lies in attenuating the aerial signal.

Most front-ends use an RF amplifier followed by the mixer which may generate its own local oscillator signal (f_0) or call for a separate oscillator stage. Whatever the arrangement, the mixer receives f_c and f_0 and thus delivers $f_0 \pm f_c$. The vast majority of FM front-ends use an f_0 equal to $f_c + \text{IF}$, the IF thus corresponding to $f_0 - f_c$, and it is this signal only which is accepted by the IF channel, as shown in Fig. 4.

Thus, if the aerial signal is, say, Radio 2 from Wrotham at 89.1 MHz, the local oscillator will be 10.7 MHz above this at 99.8 MHz, so that 99.8-89.1 equals the 10.7 MHz IF. Both additive and multiplicative mixing are used, the former generally when the mixer has just one input port,

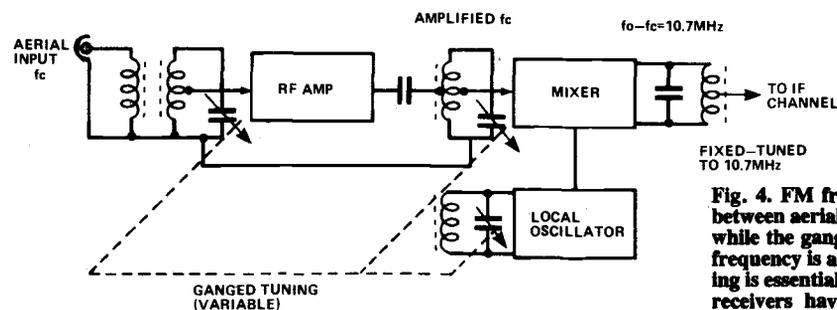


Fig. 4. FM front-end with RF amplifier using two variable-tuned circuits between aerial and mixer. The RF and mixer input circuits are tuned in step while the ganged oscillator tuning tunes over Band II so that the oscillator frequency is always 10.7 MHz above the carrier frequency. Accurate tracking is essential to avoid a decrease in sensitivity over the tuning range. Some receivers have double bandpass tuning between the RF amplifier and mixing for further improvement in front-end selectivity.

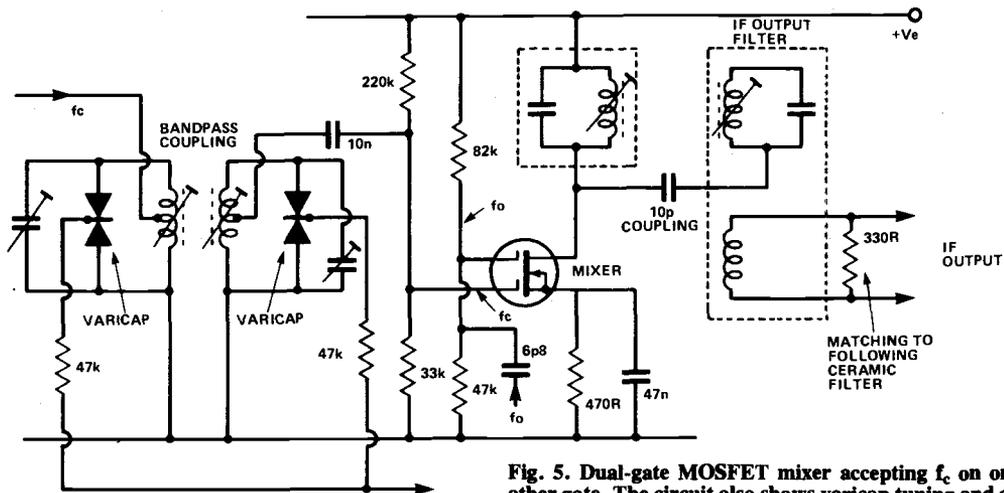


Fig. 5. Dual-gate MOSFET mixer accepting f_c on one gate and f_o on the other gate. The circuit also shows varicap tuning and a capacitively-coupled IF output filter.

and the latter when there are two inputs, such as with a dual-gate FET as shown in Fig. 5. This sort of FET (MOS) may also be used for the RF amplifier, with one gate accepting f_c and the other an AGC (automatic gain control) bias via an amplifier as shown in Fig. 6.

Varicap Tuning

Some contemporary receivers, especially of European origin, use varicaps (eg. capacitor diodes) instead of a mechanical tuning gang. The bandpass section in front of the mixer in Fig. 5 is tuned in this way. The varicaps are diode pairs arranged to neutralise non-linearity which, when biased for reverse conduction, exhibit capacitance of value which decreases as the reverse bias is increased. For continuously variable tuning, therefore, it is necessary merely to bias the diodes together from a potentiometer which is mechanically coupled to the tuning system. To eliminate capacitance change and hence tuning drift the tuning voltage is derived from a stabilizer or regulator. The scheme also lends itself to press-button station selection.

Also in Fig. 5 the IF signal is filtered out by a capacitively-coupled circuit. The 330 ohm resistor matches the output to

the following ceramic filter in the IF channel, as do the input and output filter resistors in Fig. 3. Unless this matching is correct the filters fail to provide the proper symmetry, selectivity and skirt sharpness.

Bandpass coupling at the output of the RF amplifier is also used in Fig. 6, but the tuning here is by ganged mechanical capacitor.

Oscillator Stage

To avoid oscillator 'pulling' on strong carriers, state-of-art FM receivers use a local oscillator followed by a 'buffer' stage, as shown in Fig. 7. Less elaborate models either use a separate oscillator coupled direct to the mixer, or a self-oscillating mixer.

AM Front-Ends

Exactly the same principles apply to AM, but because f_c is that much lower the design of the front-end section is less critical. The IF is generally around 455 kHz and, as with FM, f_o is often the IF above f_c ; but some models place f_o the IF below f_c , though this may reverse on some wavebands.

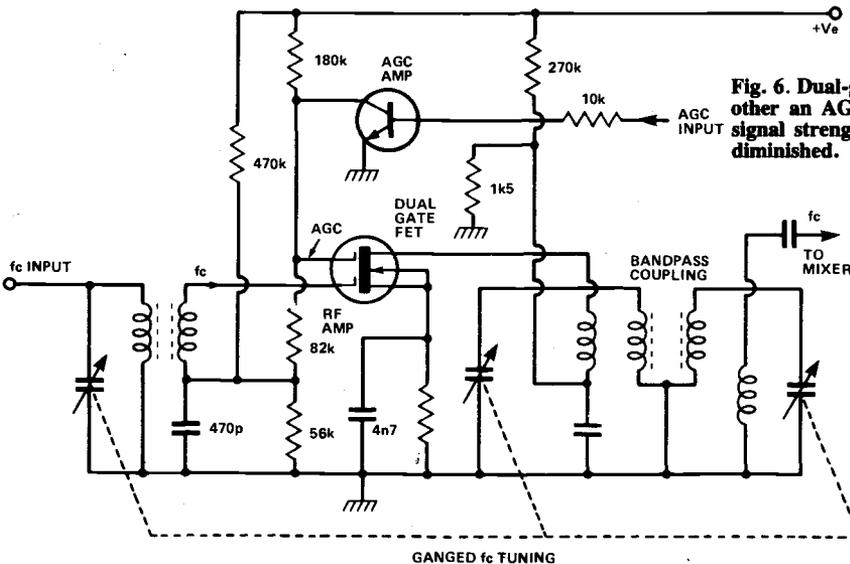


Fig. 6. Dual-gate MOSFET RF amplifier where one gate receives f_c and the other an AGC bias obtained from a bipolar amplifier. With increase in signal strength the bias increases so that the gain of the RF amplifier is diminished.

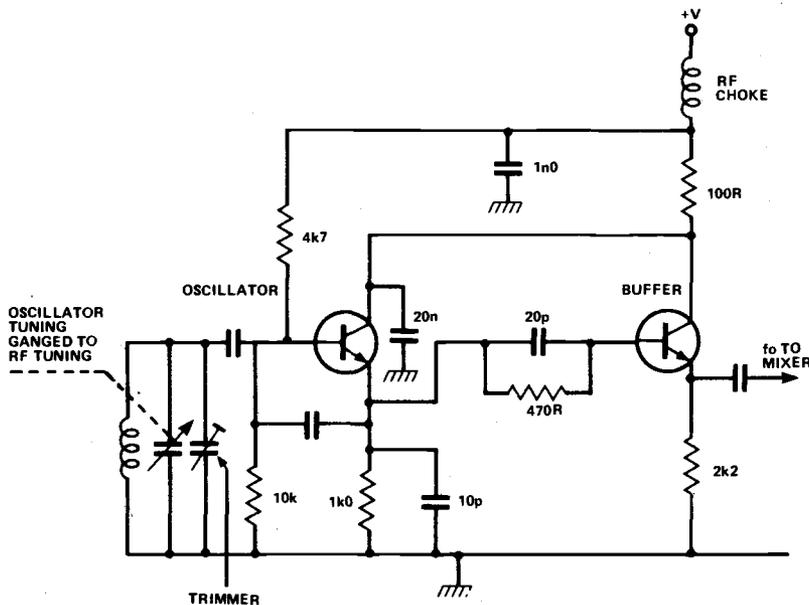


Fig. 7. FM local oscillator followed by buffer stage for feeding the mixer.

The majority of AM transistor portables employ a ferrite rod aerial which also serves as the input tuning. Only the more elaborate models boast an RF amplifier, and a self-oscillating mixer is commonly adopted, as shown in Fig. 8.

Receivers with poor front-end selectivity are relatively prone to spurious responses at frequencies removed from the tuned frequency. A typical one is the 'image' or 'second channel' response where the IF is produced from an input two times the IF above the tuned frequency when the oscillator is running at the IF *above* the signal frequency.

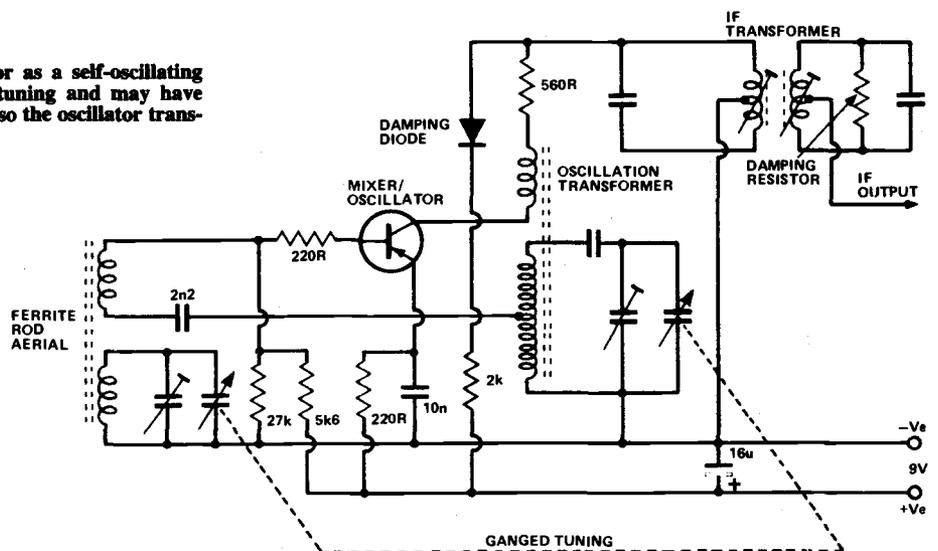
For example, if the receiver is tuned to, say, 1,000 kHz the oscillator will be running at 1,455 kHz, so an incoming signal at 1,910 kHz (two times the IF above the tuned frequency) will heterodyne with the oscillator signal to yield the IF in terms of 1,910-1,455. When the front-end selectivity is sharp, a signal two times the IF away from the tuned frequency would be well attenuated and not so likely to cause interference. Another is called the half-IF, or 'repeat spot', response which falls half the IF away from the tuned

frequency owing to the 2nd-harmonic of the oscillator heterodyning with the 2nd-harmonic of the off-tune signal from the RF stage and producing the IF again.

IF Channels

IF channels nowadays use ICs for the gain and resonant filters of the type already mentioned for the selectivity. FM IF channels employ amplitude limiting ICs or ICs deliberately arranged to limit above a certain signal amplitude. Although FM detectors are essentially insensitive to amplitude variations of the IF-converted carrier, especially ratio detectors, additional limiting is desirable in the IF channel further to enhance the AM rejection ratio and to help with the capture effect. A top-flight modern FM receiver will fail to rise in audio output level once the input carrier at the aerial has reached the 2 to 3 microvolt level, the effect then being a progressive improvement in S/N ratio with increasing level of aerial input, as shown by the curves in Fig. 9. Less exacting models will require an input of 100 microvolts or more before full limiting occurs. The action of

Fig. 8. AM front-end using single bipolar transistor as a self-oscillating mixer. The ferrite rod aerial serves as the input tuning and may have switched windings for long and medium waves, as also the oscillator transformer.



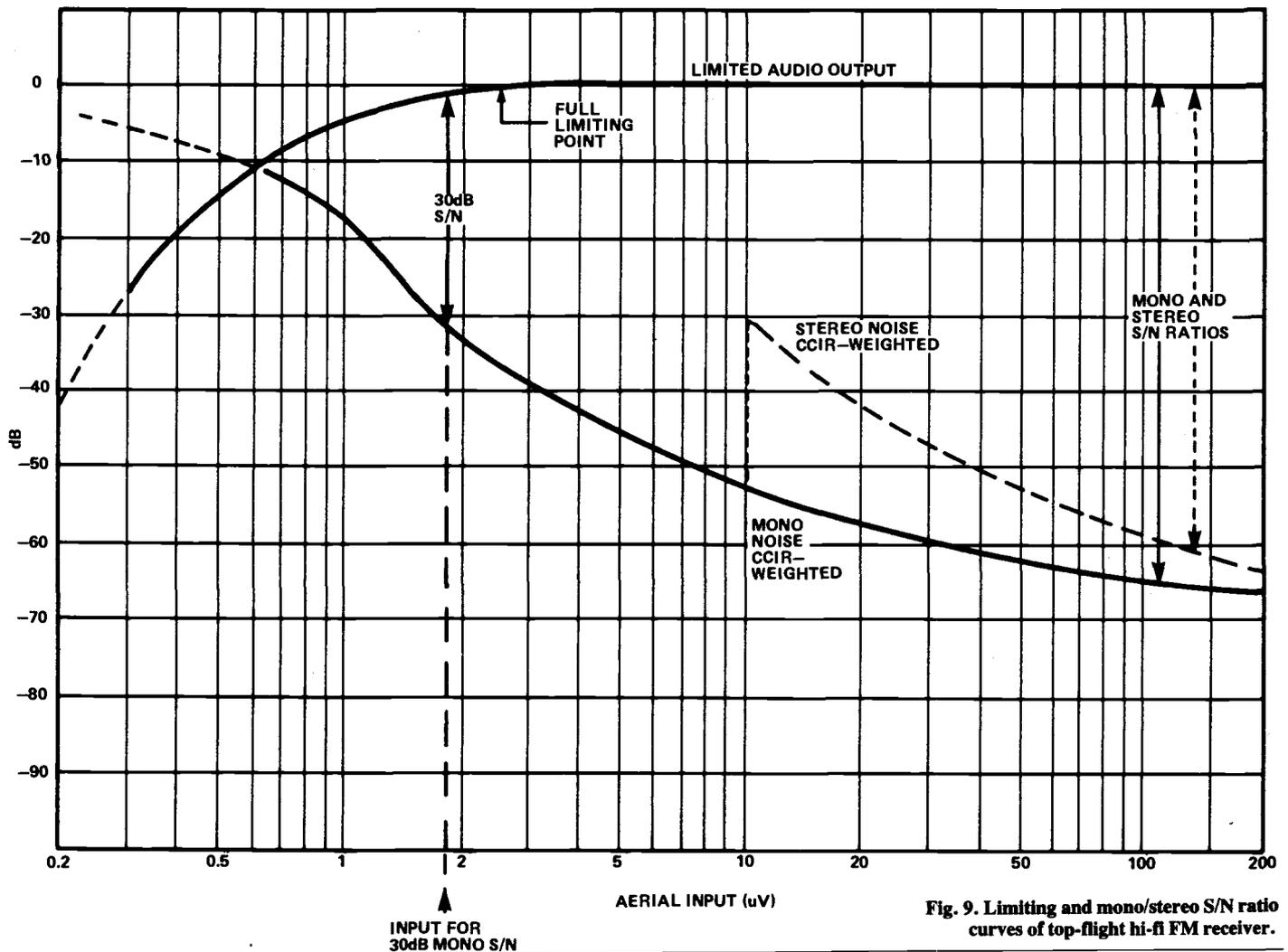


Fig. 9. Limiting and mono/stereo S/N ratio curves of top-flight hi-fi FM receiver.

the stereo decoder impairs the S/N ratio at the lower signal levels, catching up with though never reaching the mono ratio at higher inputs. There is always an ultimate S/N ratio impairment of about 2 dB on stereo with respect to mono, owing to approximately 10% of the available deviation being used for the stereo information and the greater noise power bandwidth of the receiver in stereo mode.

The FM IF channel also provides the AGC bias for the front-end (when used), AFC control voltage (automatic frequency correction potential derived from the FM detector or separate discriminator for application to the oscillator varicap to hold the carrier at the centre of the IF pass-band), signal strength and tuning metering, and interstation muting (where the audio output is disabled until the input reaches a pre-determined level as a means of cutting the noise when tuning between FM stations).

The most complex of FM IF channels may employ a cascade of ICs (three or four) feeding into a bipolar transistor which in turn drives the FM detector. Additional ICs and bipolar transistors may be used for front-end AGC, AFC, muting and metering. The simplest adopts a complex IC, such as the CA3089E, which provides IF amplification, limiting, FM detection and audio preamplification for driving the stereo decoder, as shown in Fig. 10. The device contains no fewer than 80 transistor integrations, and in-

cludes sections for delayed front-end AGC, AFC, signal strength meter drive, tuning indication and interstation muting. In the circuit the muting is operated by S5 and the threshold level set by RV7. S4 switches the AFC on and off, while coils L10 and L11 are concerned with the FM detection.

Quadrature FM Detector

The coils, in fact, are a part of a quadrature detector circuit, which is fast finding favour in FM receivers, facilitated by ICs, without which would demand a complex of discreet components. The arrangement is based on a 90° phase shift and synchronous detector, as shown in Fig. 11. FM IF signal is amplified and heavily limited, and the resulting 'clipped' signal is passed to one input of the detector direct and to a second input *via* the phase shift, which is merely an LC circuit such as L10/11 in Fig. 10. The detector is essentially a 'multiplier' which combines the two inputs vectorially. Owing to the relative phase shift and the deviating FM signal the output consists of varying width rectangular pulses, and from these the audio signal is obtained by low-pass filtering.

Ratio Detector

This is another very popular FM detector whose circuit is given in Fig. 12. When the primary and secondary of the

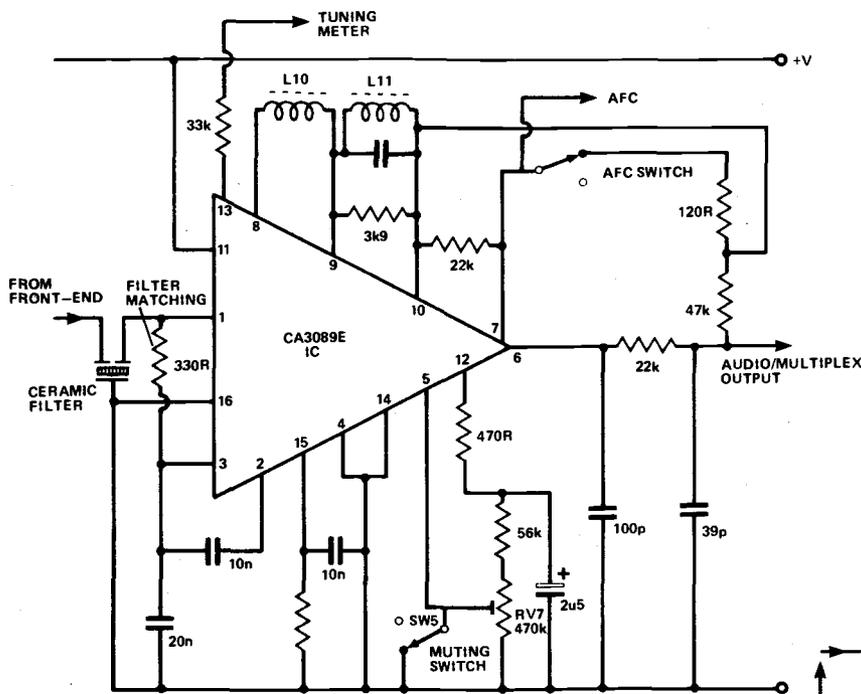


Fig. 10. FM limiting and detection by CA3089E IC (see text).

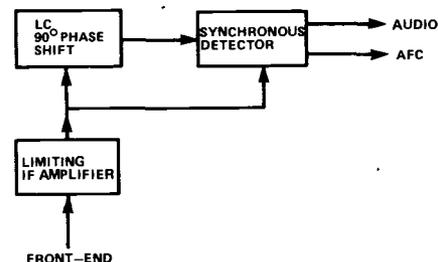
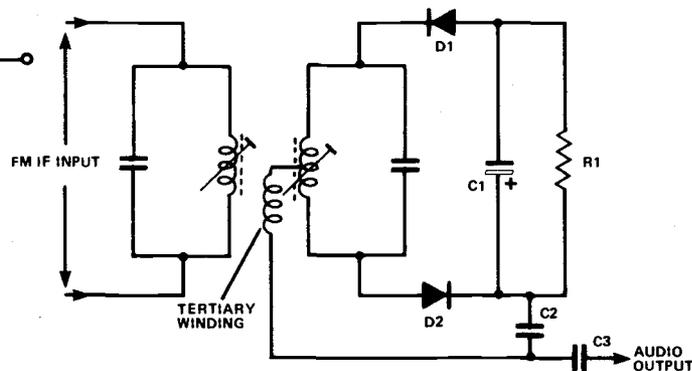


Fig. 11. Simplified quadrature detection.

Fig. 12. FM Ratio detector circuit.



tuned transformers are resonated to the undeviated carrier the two diodes conduct equally and since the diodes are connected in series a potential is developed across R1 which charges C1.

When the input deviates either side of its nominal frequency the balanced phasing condition is destroyed and the diodes fail to conduct equally. This results in current flowing out of the circuit through the 'phasing' or tertiary winding, and because this external current is geared to the deviation the audio signal develops across C2, which is fed out through C3.

An advantage of the ratio detector compared with the Foster-Seeley detector or discriminator (which also uses two diodes but connected back-to-back and is without the tertiary winding) is that it yields amplitude limiting. Provided time-constant R1/C1 is large enough the steady-state potential across R1 is substantially unaffected by faster occurring amplitude changes of IF signal such as caused by electrical interference, etc. A value around 200 milliseconds is a fair compromise between poor limiting and sluggish tuning.

FM detectors generally have a bandwidth in advance of that of the IF channel to ensure that at maximum deviation the signal remains on the linear parts of the 'S' characteristic and as an aid to the capture effect.

AM Stages

The IF channel is far simpler in AM than FM receivers. Gain is given by a couple of bipolars or an IC, and selectivity is introduced either by two tuned transformers or a ceramic filter (sometimes both). AM IF is around 455 kHz which, with the restricted bandwidth, makes it easier than FM to achieve the required gain with fewer devices.

Detection is invariably accomplished by a simple diode circuit as shown in Fig. 13. From the signal point of view this rectifies the AM waveform so that the average value varies in sympathy with the modulation. Subsequent filtering deletes the IF component. The rectified DC value of the

carrier is commonly used as an AGC potential automatically to control the gain of the IF amplifier. At the front-end a damping diode may be used to reduce the mixer output on very strong aerial signals. Such a diode is shown in Fig. 8. This conducts and thus damps the IF output when the signal level rises above the value established by the biasing. Figure 13 shows alternative biasing for this diode.

The tapped primary of the IF transformer ensures that the tuned circuit is not excessively damped by the output resistance of the transistor. This technique is also used in other sections as will be observed from the circuits.

FM Pre- and De-Emphasis

The S/N ratio of the FM system is further enhanced by the application of treble boost to the modulation signal at the transmitter (pre-emphasis) and compensating treble cut (de-emphasis) at the receiver. These are based on a time-constant which is 50 microseconds UK and 75 microseconds America. It thus refers to the 'turnover' frequency (that frequency where the boost or cut occurs) and is equal to $1/2\pi T$, where the frequency is in Hz and the time-constant (T) in seconds, which works out to about 3,184 Hz at 50 microseconds. The ultimate rate of boost or cut approximates 6 dB per octave (eg. single-pole filter). FM produces a triangular noise output because the output from the detector is proportional to f_d . Because f_d max is ± 75 kHz and f_m max 15 kHz the noise content is significantly reduced and is reduced by a further 4 dB or so by the pre- and de-emphasis.

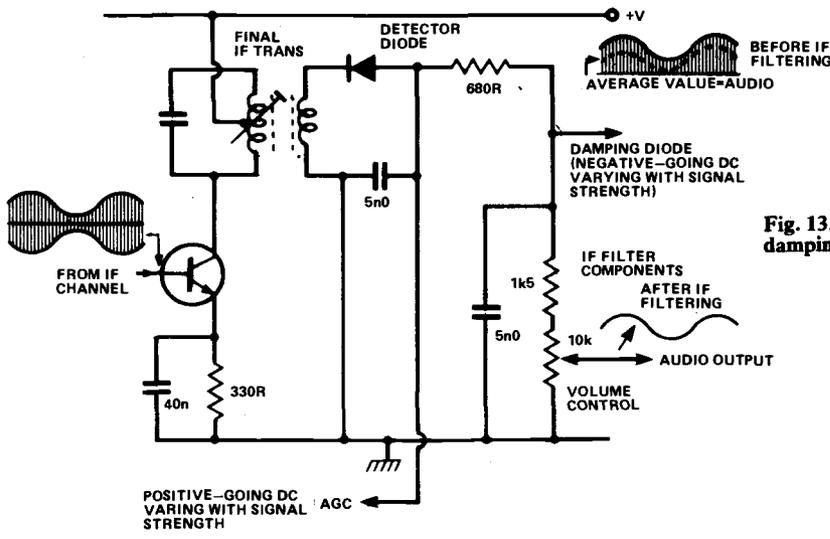


Fig. 13. AM detector circuit with feeds for AGC and damping diode (also see Fig. 8).

The de-emphasis consists of a simple RC time-constant at the detector output in the case of mono and at the decoder output in the case of stereo. It is not possible to apply de-emphasis at the detector when this is followed by a stereo decoder since the effect would be seriously to attenuate the complex stereo multiplex signal. The net result of the ± 75 kHz f_d and the pre-/de-emphasis is a weighted S/N ratio of 75 dB or more mono and just over 70 dB stereo, depending on the noise figure and quality of design of the receiver.

Stereo Encoding

After separate pre-emphasis of the left (L) and right (R) audio channels at the transmitter the signals are fed to a combined adder and subtractor (matrix) which yields L+R mono information and L-R stereo information. The mono signal is passed to the transmitter in the usual way (allowing receivers not equipped with a stereo decoder to work on the signal without undue loss, which is an aspect of system compatibility), while the stereo signal is separately processed and subsequently 'added' to the mono signal for transmission. It is applied to an *amplitude* modulator whose carrier frequency is 38 kHz but which is suppressed so that only the lower and upper *sidebands* of the stereo information remain (in practice the residual 38 kHz subcarrier accounts for no more than 1% of the maximum deviation – eg. less than ± 750 Hz). The stereo information sidebands along with the mono information are then applied to the normal VHF modulator of the transmitter.

For the detection of suppressed carrier AM, the carrier needs to be regenerated at the receiver (in the stereo decoder), and to facilitate this a 19 kHz pilot tone using up approximately 9% of the maximum deviation (eg. about ± 6.75 kHz) is also applied to the VHF modulator. The total modulation signal thus applied to the VHF carrier has the spectrum shown in Fig. 14. The L+R mono signal occupies the normal audio range from about 30 Hz to 15 kHz, next comes the 19kHz pilot tone and then the lower and upper stereo sidebands between which is the suppressed 38 kHz sub-carrier. At no time can the total deviation of all these signals exceed ± 75 kHz (eg. 100% modulation). In Fig. 14. the total modulation consists of 45% L+R mono, 22.5% L-R stereo in each sideband (45%

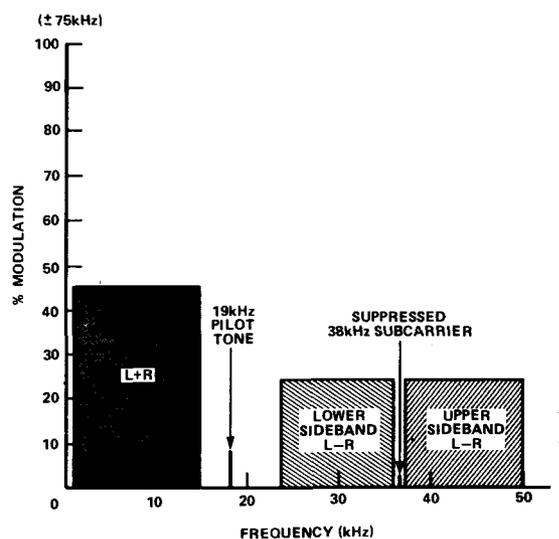


Fig. 14. Spectrum of multiplex signal at FM detector output on stereo signal when one channel only is modulated. See text for other modulation levels.

in all), 9% pilot tone and 1% residual subcarrier, adding up to 100%. This condition would obtain with an input only to one channel (eg, L or R 1 unit and R or L zero). With both inputs receiving the same intensity of 'in phase' signal (eg, stage-centre mono condition), the stereo information would be virtually zero so that a full 90% modulation capacity would be available for the L+R mono information (the remaining 10% being used by the pilot tone and residual subcarrier). With both inputs equal but in phase opposition (a very rare happening) all the information would be in the L-R stereo channel. Under normal music conditions, of course, the mono and stereo information is continuously changing, but the balance of 100% maximum is always maintained.

Stereo Decoding

The encoding system just described is based on the Zenith-GE developments which is universally adopted. Various schemes for decoding the signals back to the L and R channels for reproduction have been devised – the earlier ones using discrete components with valves and later transistors, and the latest ones using ICs specially developed for encoding. It is clearly outside the scope of this article to venture back into history, but a phase lock loop (PLL) IC decoder circuit used in many receivers is given in Fig. 15.

Multiplex signal (of Fig. 14 spectral form) is fed to pin 1 input via Q1. Inside the IC the PLL is formed by a 76 kHz voltage controlled oscillator (VCO), two divided-by-two stages yielding first 38 kHz and then 19 kHz, a 19 kHz

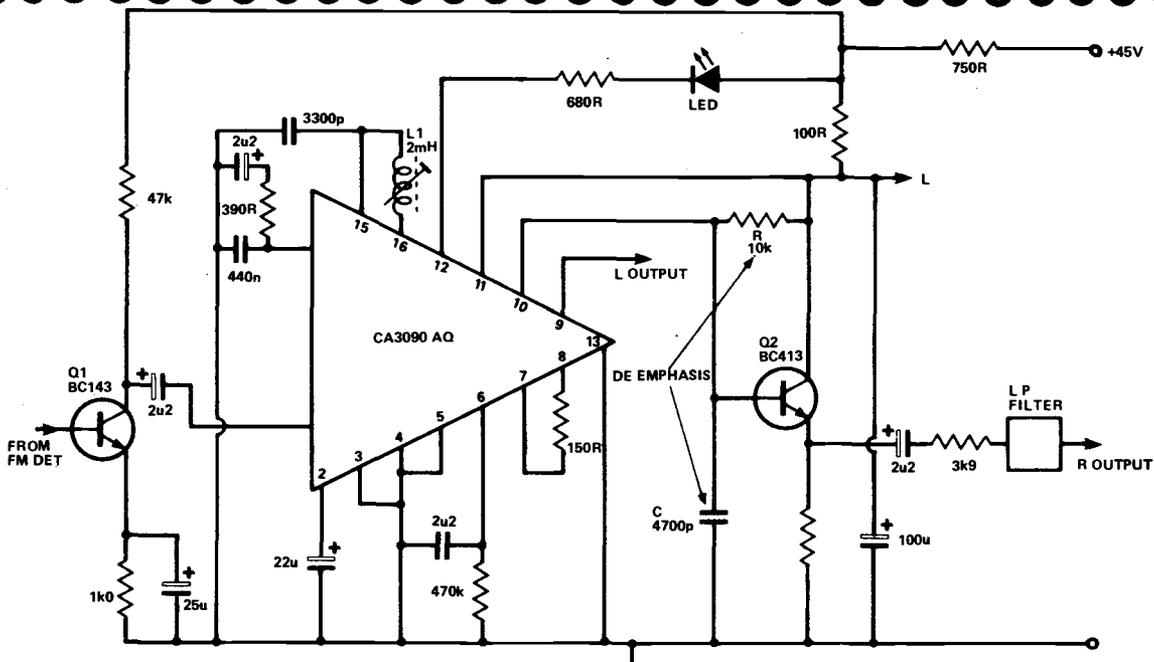


Fig. 15. Circuit of stereo decoder based on the CA3090AO IC. L1 is PLL tuning and RC the de-emphasis. One channel only is shown; the other channel is similar, however.

phase comparator, low-pass filter and DC amplifier whose output is fed back to the VCO for control, as shown in Fig. 16.

The multiplex signal is first buffered and then fed to the phase comparator where the pilot tone component is compared with the loop-derived 19 kHz signal. The loop is thus locked and the 38 kHz signal from the first divider constitutes the reclaimed subcarrier which, along with the multiplex direct, is applied to the decoder section. This can be regarded as an 'inverse' of the encode matrix which, after AM demodulation, yields the L audio from $(L+R)+(L-R)$ and the R audio from $(L+R)-(L-R)$. Each output is subjected to de-emphasis before being applied to the L and R audio amplifiers for driving the loudspeakers.

The IC is also equipped with automatic stereo switching so that on a non-stereo signal the two outputs deliver mono signal, and a stereo indicator switch which lights a small bulb or light emitting diode (LED) when stereo information (pilot tone) is detected. The circuit connections involved are shown in Fig. 15. The VCO locking is achieved by L1 which is a 2 millihenry inductor. Audio from each channel is 'buffered' by Q2 (same for the other channel though not shown) and passed through a low-pass filter for attenuating residual pilot tone and sub-channel spurious before arriving at the audio stages of the receiver. Some of the very recent ICs incorporate a pilot tone cancelling circuit so avoiding the need for low-pass filtering and maintaining an excellent response to 15 kHz or more.

Of course, all stereo receivers have two separate audio channels for the L and R signals. Hi-fi receivers employ the latest technology in this area, some models yielding 60 W per channel or more at remarkably low distortion. Less exacting receivers have relatively simple audio stages based on push-pull transistor pairs or hybrid power ICs.

There is no doubt that latter-day hi-fi receivers operating from off-air stereo signals (particularly when these correspond to 'live' transmissions) are capable of extremely high audio quality, on par with the best of most other programme sources.

Gordon King

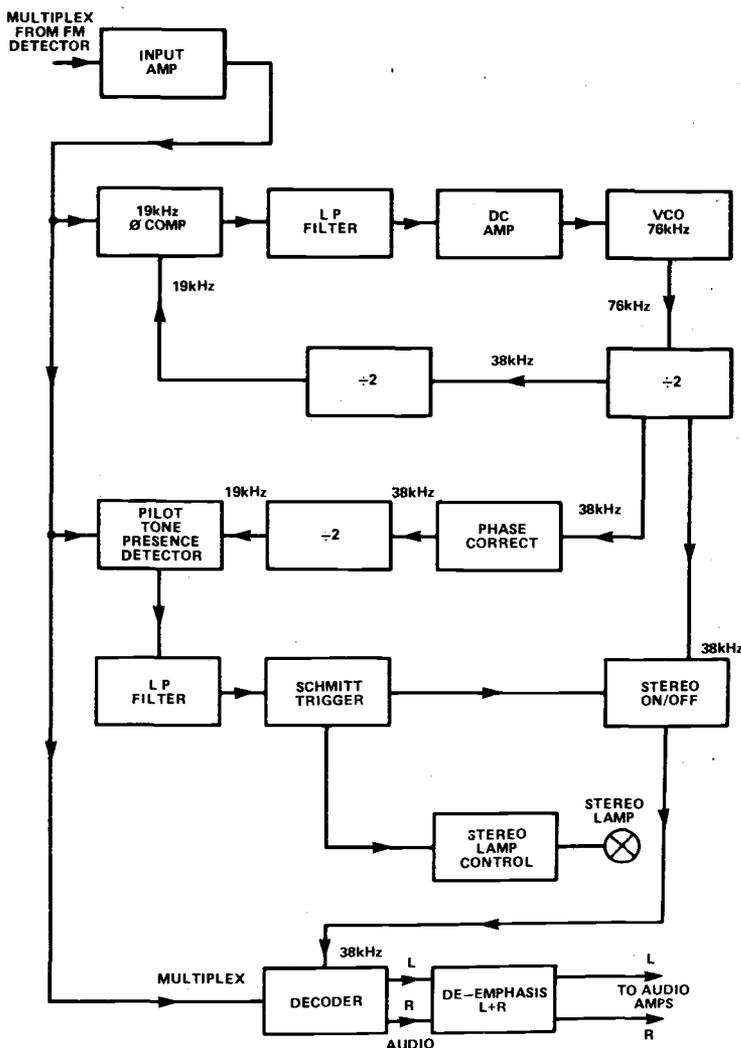


Fig. 16. Block diagram of PLL stereo decoder IC.

Chapter 4

SWITCH IN LINE SAVES NONE?

Here's a bit of insight into the faults inherent in many widely-used comparative hi-fit tests, with emphasis on switching methods.

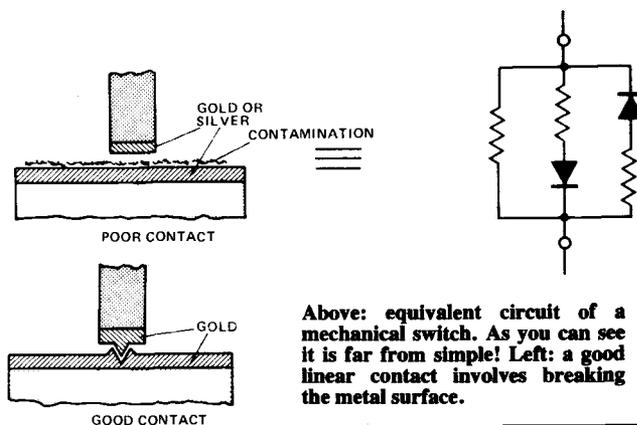
A SIGNIFICANT RE-APPRAISAL of amplifier design has been seen in the past few years. The revival of serious listening tests (so called "subjective" testing) has shown that laboratory measurements alone are not sufficient to indicate the performance of the amplifier when it is connected to real loudspeakers and pick-up cartridges and fed with a music signal. But it is crucially important that these listening tests be set up with great care. When different amplifiers are compared their gains should be equalised so that their outputs are within 0.1 dB of each other and preferably within 0.05 dB.

Such level changes could be incorrectly interpreted as differences in amplifier performance. The design of the passive attenuators is important to prevent any significant loading of the circuitry or any unbalancing of impedances which could upset passive filter roll-offs and so alter the frequency response of the system. Even the choice of test signal is important when setting levels. Traditionally a sine-wave of 1 Hz or 400 Hz has been used. However, the author prefers to use a noise source fed via a bandwidth limiting filter (to prevent any error by the different frequency responses of the amplifiers) as this more realistically simulates the dynamic conditions.

Care should also be taken in the interconnection of the different amplifiers. All connections should be as short as possible using very high quality and identical (in length and quality) cables. Wherever connections have to be made (other than at the amplifier or loudspeaker) high-quality gold-plated instrumentation connectors should be used in preference, to the rather suspect RCA Phono and DIN Connectors.

Switch Your Contacts

The next problem area is that of switching. Switching the outputs of the different amplifiers to a loudspeaker can be done using high-current, high-conductivity lever of knife switches. Relays can cause problems unless they have very strong springs, good contact design, high-current capability, and are new. The subject of switch contacts is quite complex but can be summed up as follows: A metal to metal contact is rarely a true "short circuit."



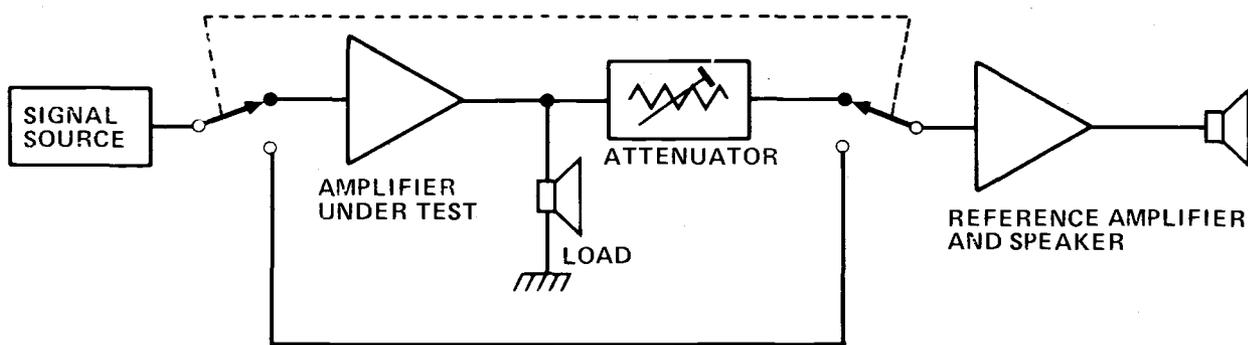
Above: equivalent circuit of a mechanical switch. As you can see it is far from simple! Left: a good linear contact involves breaking the metal surface.

An almost invisible layer of oxidation or contamination forms on the contacts. This oxidation increases the contact resistance but more importantly forms a non-linear junction that can in some ways be considered to be a voltage dependent diode-rectifier. The effect on the music signal at low levels can be imagined and – more importantly – heard! Even "pure" gold contacts and "self-cleaning" contacts suffer from this problem. A good contact can only be achieved when one contact breaks the surface of, and penetrates, the other contact metal. However, only a limited number of switching actions can occur before the contact material is sufficiently worn or damaged for inconsistent performance. Although this problem is discussed here in relation to testing, it has as much significance in the design of the switches used in the amplifier.

When it comes to switching the output of the cartridges the imperfections of the switches have so much effect upon the audible quality of the signal that the listening test ceases to have any real validity.

Test Point

The test itself needs further thought. The listening panel should be experienced listeners and yet not be part of a "clique" where views are remarkable for the way they follow the "party line." Testing should be conducted over two or more sessions. Short sessions to perceive the performance of the amplifiers before aural fatigue sets in; and



STRAIGHT LINE TEST

Fig. 2. The Straight Wire Test. First popularised by Peter Walker of Acoustical Manufacturing (or Quad!), this test method has gained wider acceptance as of late. It has its faults, however.

longer sessions with each individual amplifier to judge whether such fatigue is caused by the amplifier and to judge whether the apparent improvement it offered was a "flash in the pan."

During the initial sessions a number of "check" changes should be made to detect cheating (deliberate or involuntary) i.e. running amplifier No. 3 a second time as amplifier No. 7. Between each piece of music the reference numbers should be changed to minimise the effects of pre-conception. For example, if amplifier No. 3 is disliked for its reproduction of a bass drum, it may then be subconsciously disliked on other pieces of music. Of course the tests should be conducted blind as far as possible.

A popular "subjective" test in use is the *Straight Wire Test*. In this test the amplifier under evaluation is fitted with

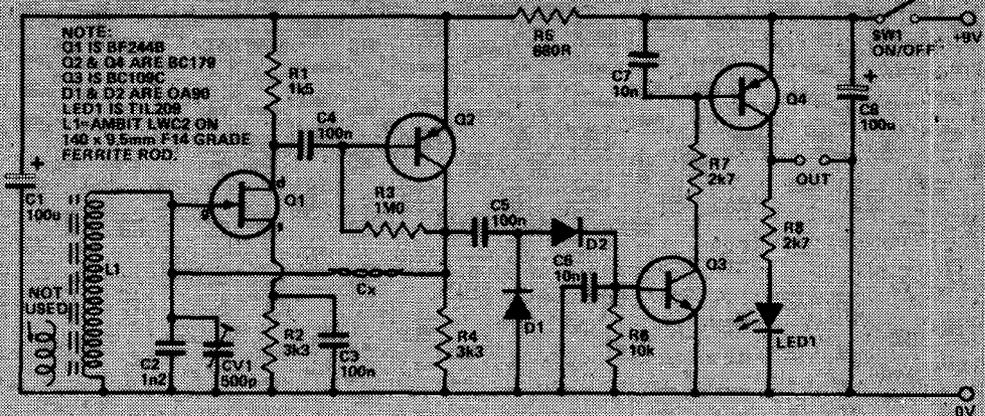
an attenuator at the output and substituted for a straight wire. The resulting signal is fed to a "reference" amplifier and loudspeakers of known performance. Such a test is of help in evaluating the dependence of the amplifier on the loading made by different loudspeakers. But otherwise this test must be considered suspect. The "reference" amplifier may be far from perfect and it may well mask subtle changes. The dynamic interactions of two units in series can be quite complex and very difficult to predict in advance.

The foregoing (brief and incomplete) discussion of subjective testing serves only to indicate the difficulties that can be encountered. The reader should only consider seriously those comparative reviews where considerable effort has been expended to eliminate errors due to equipment and human beings.

Stan Curtis

SPOT DESIGNS

60kHz Time Receiver



THIS RECEIVER gives reception of the atomic clock time signals transmitted by the Rugby MSF transmitter on 60 kHz. At this very low radio frequency it is not necessary to use a superhet. A ferrite aerial is used with L1, an ordinary LW broadcast band aerial coil, and the relatively high tuning capacitance of C2 and C3 is used to reduce the resonant frequency to the appropriate figure. The receiver is tuned by CV1 and by adjusting the position of L1 on the ferrite rod.

The output of L1 is direct-coupled to a straightforward common source JFET stage and this in-turn feeds a simple common emitter stage. Due to the relatively low frequency involved these can both provide good voltage gain without using tuned circuit loads. The collector of Q2 is in-phase with the gate of Q1 and if necessary, "twisted pair" Cx can be used to provide regeneration between these two points to boost the sensitivity of the set.

The output from Q2's collector is coupled by C5 to a simple diode modulator circuit which consists of D1, D2, C6 and R6. When the 60 kHz carrier is present a strong DC bias is produced across R6, but this potential quickly decays during the gaps in the carrier (the 1 S markers and other signals are modulated onto the carrier wave in the form of brief pauses in the signal).

Thus Q3 is switched on when the carrier is present, so that Q4 is in turn switched on, giving a high output and causing LED 1 to light up. In the absence of the carrier wave Q3, Q4 and LED 1 all switch off and the output of the receiver goes low.

When initially adjusting the set it is helpful to monitor the output of the detector using a crystal earpiece connected across R6.

Chapter 5

TIME CONSTANTS

Time constants and how to use capacitors in timing circuits.

THOSE LITTLE BROWN DISCS or large blue cylinders that do funny things to your multimeter if you try to measure their resistances are frequently used as AC coupling devices, but they are also of great use in timing circuits. A resistor and capacitor together can produce a changing voltage whose magnitude at any moment can easily be calculated.

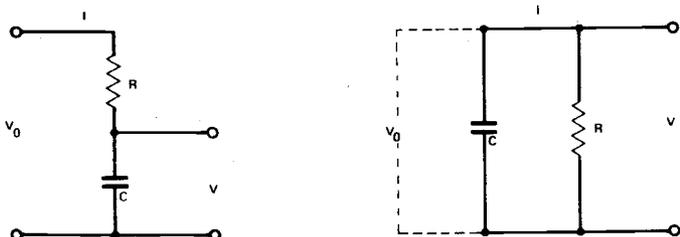


Fig. 1. Series and parallel RC networks.

First The Circuits

The first circuit in Fig. 1 consists of a resistor, R , in series with a capacitor, C . A voltage, V_0 , is applied across the combination and the output voltage (that across the capacitor) is monitored. The output voltage (V) slowly rises from zero, coming closer and closer to the value of V_0 , although it never actually quite reaches it. A graph showing output voltage plotted against time is shown in Fig. 2a. It is found by experiment that the rate of increase of voltage becomes smaller if either R or C are increased, and greater if either is decreased. That is, the voltage rises more slowly for large values of R and C than it does for small values of C . In fact, if we take the product $R \times C$, (R in ohms, C in Farads) we find that this gives the time (in seconds) required for the output voltage V to reach about two thirds the value of V_0 .

The second of the two circuits consists of capacitor and resistor connected in parallel. The capacitor is charged by an external source to a voltage V_0 , and then disconnected. The output voltage, V is monitored once again. Here, we find that V slowly decreases from V_0 to zero, getting smaller and smaller, but, again never quite making it (Fig. 2b). Again, it is found that the voltage changes more slowly if either the resistance or the capacitance (or both) are increased and changes faster if they are decreased.

Time Constant

The product $R \times C$ is called the 'time constant' τ (the greek letter Tau) of the circuit and it can be used to find rough values for V at different times. It turns out that, no matter how long the voltage has been changing in the circuit, it always takes τS for the voltage across the capacitor (in the first circuit) to increase by two thirds of the remaining voltage, eg. if V_0 is 9V, and the output voltage V at a time t is 4V, then after τS , at time $t + \tau$, V will have risen by two

thirds of (9 - 4) volts, or 3 1/3 volts.

This can be used to plot a graph of V against time. At τ seconds, V will be two thirds of V_0 . At $2\tau S$, V will have risen by two thirds of the remaining voltage, ie by two thirds of $1/3V_0$, and will thus have risen to eight ninths (approximately) of V_0 . Similarly, voltages at $3\tau S$, $4\tau S$ and so on may be calculated and plotted on a graph (Fig. 3). A line may then be drawn in freehand, joining the points, and approximate values for V at different times calculated.

This is all very well for rough values, but it is of considerably less use if we want to find exact figures — especially at times much less than the time constant. Figure 4 shows a freehand curve drawn onto the first three calculated points on a graph. We know nothing from our method about the voltage before it reaches 2/3 of its final value, except that it starts at zero. The correct graph could be A or B or anything in between — we have no way of knowing.

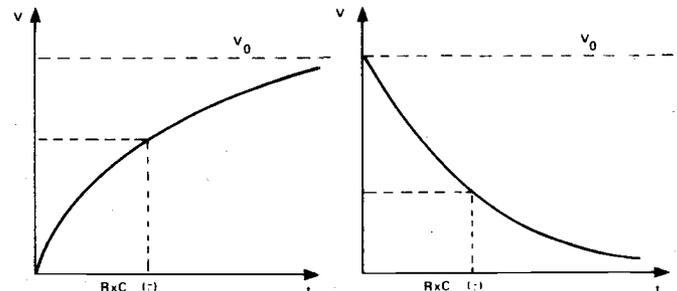


Fig. 2. The output voltages associated with the RC networks of Fig. 1.

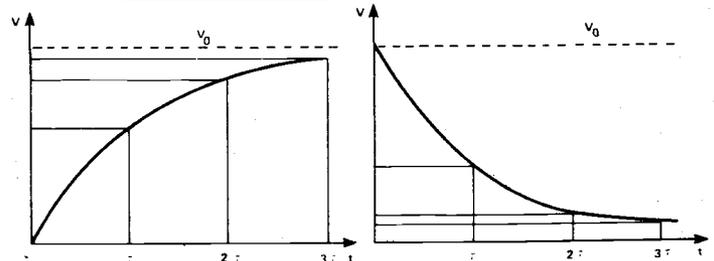


Fig. 3. Plotting graphs of output voltage against multiples of time constant.

Curve Drawing (No, Not . . .)

It is an interesting and useful property of the way in which the voltage changes in these circuits that, at any instant, if the voltage continued to increase (or decrease) at the same rate, it would reach its final value in exactly τS . The reason, why it doesn't actually do this is simply that the rate of increase is not constant. As the voltage becomes larger (Fig.1a) or smaller (Fig.1b) its rate of change decreases. However, as has been stated, if the rate of increase of the voltage, dV/dt was constant from any time t , then V would reach V_0 (or zero, as the case may be) at time $t + \tau$ (Fig.5).

We can make use of this property of the curve. Mark on the graph (Fig. 6) a line representing the final voltage, V_0 , of the system. Now mark along this line a distance τ from the beginning (point A) and draw in a straight line from this point to the origin, O. This, then, will give a fair approximation to the voltage as it changes in the first few moments. Now choose a point on this line, near the bottom (P1). Mark a distance τ along from P1 and find the point on the line representing V_0 directly above. Call this point B. Draw a line from P1 to B. Now choose a point P2, near P1 on this line, and repeat the same process. Eventually, the lines shape themselves round a curve, which turns out to be a fair approximation to the graph of voltage plotted against time.

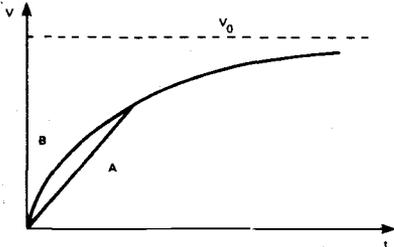


Fig. 4. A freehand curve drawn onto the first three points calculated.

This method is fine, but it has three great disadvantages; it takes a long time to draw the curve this way, it isn't very accurate beyond about 2τ and (as you will have realised if you had to read the last few paragraphs more than four times) it's complicated. If we want to find values of V beyond τ seconds, we can use the first method of drawing the graph and if we want values of V for times less than τ seconds, this second method can be used, but it is simpler, if we only want to know one value.

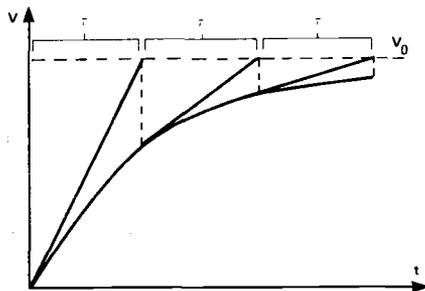


Fig. 5. V tends towards V_0 .

Capacitors

We are so used to thinking in terms of currents and voltages that it is very easy to forget the existence of a more basic quantity - charge. Charge is *what passes when a current exists*. Current, then, is actually *rate of passage of charge*. Now capacitance is defined as *the ratio of the charge stored in a component to the voltage developed across it*. That is, if C is the capacitance in Farads, Q is the charge in coulombs and V is the voltage,

$$\text{or } C=QN$$

$$Q=VC$$

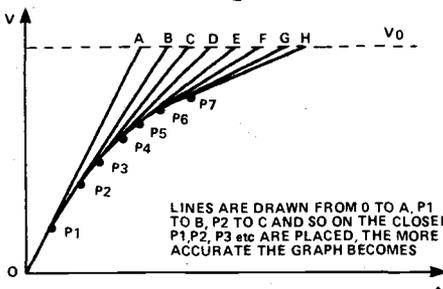


Fig. 6. This method of drawing graphs is reasonably accurate up to twice the time constant.

LINES ARE DRAWN FROM O TO A, P1 TO B, P2 TO C AND SO ON. THE CLOSER P1, P2, P3 etc ARE PLACED, THE MORE ACCURATE THE GRAPH BECOMES

We can differentiate each side of the equation

$$\frac{dQ}{dt} = \frac{d}{dt}(VC) = V \frac{dC}{dt} + C \frac{dV}{dt}$$

Now C is a constant, so dC/dt is zero

$$\frac{dQ}{dt} = C \frac{dV}{dt}$$

Finally, we can see that since current is rate of flow of charge, dQ/dt is the current flowing into the capacitor, so

$$I = C \frac{dV}{dt}$$

Now let's take another look at the circuit in Fig. 1a. If we assume that no current is being drawn from the output, then the current into the capacitor must equal the current through the resistor. The voltage across the resistor, though, V_R , is obviously equal to $V_0 - V$, and by Ohm's law

$$(V_0 - V)/R = I$$

Therefore,

$$(V_0 - V)/R = C \frac{dV}{dt} \quad V_0 - V = RC \frac{dV}{dt}$$

This is the differential equation that must be solved to find V . The mathematicians out there might like to show that the equation is solved by

$$V = V_0(1 - e^{-t/RC})$$

where e , as any scientific pocket calculator will tell you, is 2.7182818 and t is the elapsed time. This is the equation we can use for precise values.

We'll do an example: a 9 V power source is connected across a series combination of a 47k resistor and a 10 μ F capacitor. What is the voltage across the capacitor after 0.6 S? Fitting the values into the equation

$$\begin{aligned} V &= V_0(1 - e^{-t/RC}) \\ &= 9 \times (1 - \exp(0.6 / (4.7 \times 10^4 \times 10^{-5}))) \\ &= 6V49 \end{aligned}$$

(If you don't believe me, try it . . .)

A similar sort of argument works for the circuit in Fig. 1b. The output voltage V is given, by Ohm's law, by

$$V = IR$$

However, I in this case is the current flowing out of the capacitor, and so it is given by the relation

$$I = -C \frac{dV}{dt}$$

Hence we have

$$V = -RC \frac{dV}{dt}$$

And we find that this differential equation has the solution

$$V = V_0 e^{-t/RC}$$

where V_0 is the voltage to which the capacitor was charged.

Let us suppose we have a 200 μ F capacitor in parallel with a 330k resistor. The capacitor is charged up to 12 V and the supply removed. What is the voltage across it after 2 S? Well, plugging these values into our equation, V_0 is 12V, t is 2 S, R is 3.3×10^5 ohms, and C is 2×10^{-4} .

A. Lipson

Chapter 6

MPU

SUPPORT CHIPS

There's no shortage of technical tomes on microprocessors, but there is a distinct dearth of texts on chips that make the MPU do its stuff.

THE FIRST ESSENTIAL for a microprocessor is a clock pulse generator. A clock pulse is simply a rectangular pulse which repeats at a high frequency, usually 1 MHz or more. All microprocessors need clock pulses, because each operation within a microprocessor is triggered by a clock pulse, so no clock pulse – no action. Each little piece of a program will take a definite number of clock pulses to carry out.

How do we generate clock pulses? A few microprocessors, notably the much-loved INS8060 (SC/MP Mk. II) used in the Science of Cambridge Mk. 14 kit, can generate their own clock pulses. The INS8060 has two terminals which can be connected to external components as shown in Fig. 1. Either RC or crystal oscillator circuits can be used, providing the frequency is fairly high – the internal circuits simply won't oscillate if the time constants are too large. Keep to the values suggested by the manufacturer and you should have no problems.

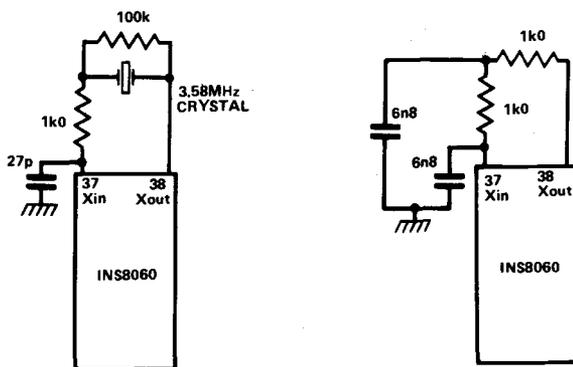


Fig. 1. Using a built-in oscillator – the INS8060 (SCMP II) can use its built-in oscillator along with a crystal or a simple R-C network.

Phase Relations

Most microprocessors, however, can't spare the extra pin for connections to a built-in oscillator and instead use only a single pin or a pair of pins for clock pulses. When a single pin input is used, the clock is a single phase clock (a straightforward oscillator). This can be obtained from a multivibrator or by squaring the output of a sinewave oscillator, but it's very important that the waveform should be steep-sided (Fig. 2). If you use a waveform which has long rise or fall times, so that its sides appear to slope when you

view the waveform on the oscilloscope, then you'll have trouble when you try to use the microprocessor. The reason is that some gate circuits will oscillate if they are switched over too slowly and that can cause chaos. Don't be tempted to economise on circuits.

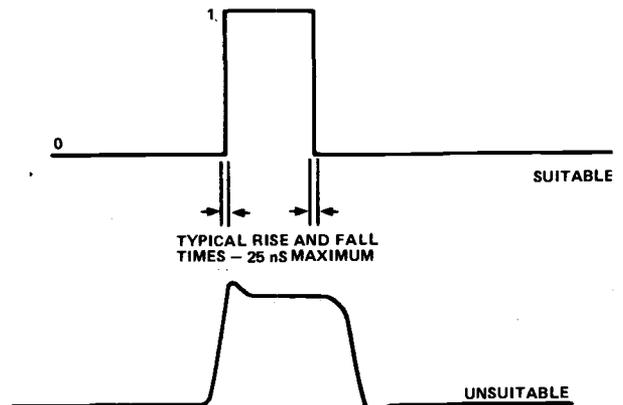


Fig. 2. Clock-pulse shapes. Most discrete-transistor oscillators and certainly all linear IC oscillators (such as 555) cannot generate sufficiently steep-sided clock pulses when driving a capacitive load. A TTL pulse generator is ideal, or a generator which is buffered by a Schmitt inverter, such as the 74LS14.

One particularly useful way of ensuring that all signals entering the microprocessor have short rise and fall times is to use a type of TTL IC called a *Schmitt trigger*. Typical of these are the 74LS13 quad two input Schmitt NAND. Each of these chips has a Schmitt trigger built in, so the output will always be steep-sided even if the input is not. It's often easier to use a cheap 'n' simple oscillator and a Schmitt IC than to build an elaborate transistor oscillator.

Refreshment Is Served

Several types of microprocessors, notably the 6800 and 6502, use two pins for the clock input. This is because the clock pulses have to be two-phase. One pin is being pulsed positive at a time when the other pin is at logic 0. Just to give one example, the 6800 carries out only internal actions on the second phase of its clock, so that during that phase all outputs are isolated. This means that you can run a low-cost memory system using dynamic RAM. Dynamic RAM needs refresh pulses and these can be delivered during the second phase of the clock pulse, when the memories are not connected to the microprocessor in any case.

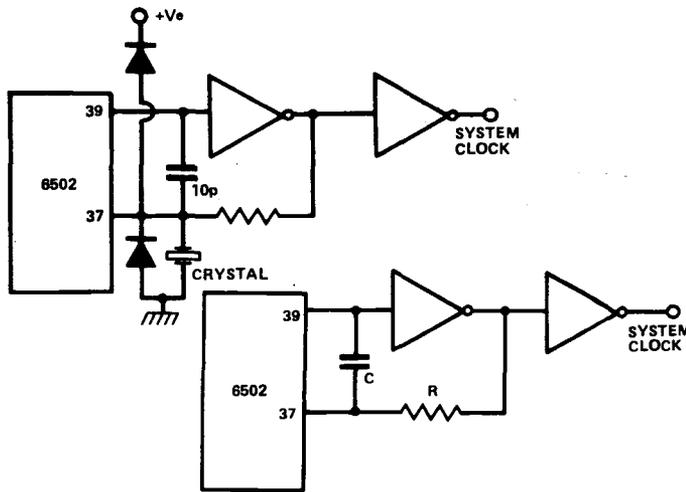


Fig. 3. The clock-pulse generator of the 6502. Either a crystal or R-C circuit can be used, but the external inverters are necessary, though they need not be Schmitt types.

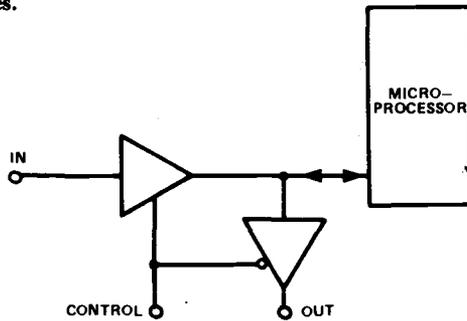


Fig. 6. Using three-state buffers. In this example, when the control signal is at logic 1, the input buffer is enabled and the output disabled. With the control signal at logic 0, the output buffer is enabled and the input disabled. The output of the disabled buffer acts like an open-circuit.

Buffers

Buffers are the next group of ICs which have to be used in practically all microprocessor circuits. A buffer is basically an amplifier circuit with a three state output — explanation coming up. There are two reasons for using buffers. One is that microprocessor circuits use PMOS, NMOS or CMOS circuits, which can't sink or source much current, usually a couple of milliamps at the most. A lot of the circuits which will be connected to the microprocessor will need quite a bit more current, so a buffer is needed — a current amplifier which can be comfortably driven by the microprocessor and which will sink or source enough current at its output to drive a lot more circuitry.

Buffers can also be used as switches. To take one example, the eight data lines of a microprocessor are used for feeding bits in *and* out. Since they can't do both at the same time, we need some method of switching so that input circuits are not connected at a time when the microprocessor is putting bits out on the data lines. This is another job for the buffer — in this case a three-state type of buffer.

The term three-state sometimes causes a bit of confusion. It means simply that the output of the buffer amplifier can be 0, 1 or isolated from all other circuits. In the type of output circuit shown in Fig. 7, for example, the output can be floated by connecting both the bases of the output pair to earth. This needs extra circuitry inside the IC and an extra 'state' pin on the package, but the advantages of having the floating state are enormous.

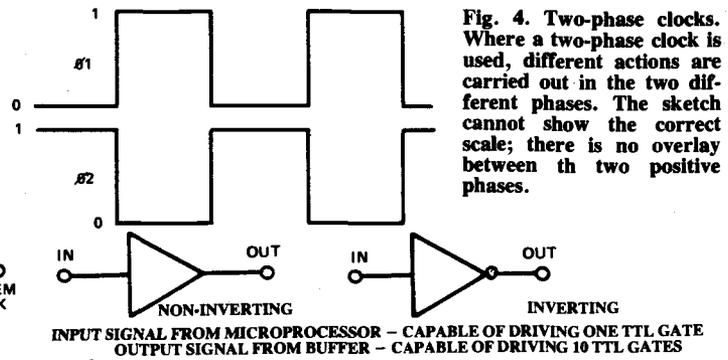


Fig. 4. Two-phase clocks. Where a two-phase clock is used, different actions are carried out in the two different phases. The sketch cannot show the correct scale; there is no overlay between the two positive phases.

Fig. 5. Buffers, inverting and non-inverting. The MOS circuits of most microprocessors cannot provide enough current drive to activate more than one standard TTL gate and a buffer must be fitted between the MOS microprocessor and the TTL circuits if expansion is contemplated.

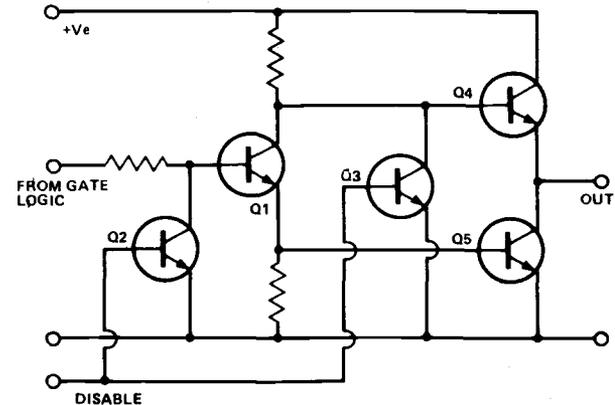


Fig. 7. A simplified form of three-state control. The normal gate output circuit consists of Q1, 4 and 5. When the disable pin is high, Q2 and Q3 conduct, shorting the bases of Q1 and Q4, so that both transistors are cut off. This isolates the output completely.

Buffers may be used unidirectionally or bidirectionally. A unidirectional buffer deals with the flow of signals in one direction *only*, perhaps from an input circuit to the data lines. Most of these are made in two versions, the difference being in the polarity of the three-state control pin. For example, one buffer may go open circuit at the output for a 1 at the three-state control pin and another type may go open circuit for a 0 at the control pin. When the buffer is being used unidirectionally, it's purely a matter of convenience which type is used. For example, if the buffer is used to connect input signals to the data lines and the microprocessor puts out a negative pulse at the time when it is ready to take in such information, then a buffer which is open circuit on a 1 signal and operates for a 0 signal at the state pin is ideal. If the other type of buffer is used, an inverter will need to be incorporated in the control line.

Much more common is bidirectional buffering, where a buffer amplifier is needed for both inputs and outputs. One single buffer can't do this, so a very common method is to use two lots. One lot is isolated by a 1 on its state pin, the other by a 0 on its state pin, so that the outputs of one set of buffers can be connected safely to the inputs of the other set as shown in Fig. 8, with the state pins connected together. In this way, the combined buffers conduct one way when the state pins is at 1 and the other way when the state pin is at 0.

Ah Yes, I Remember It Well

Most books on microprocessors assume that the readers know all about memory ICs. Assuming that you don't, point number one is that we make use of two types of memory systems, ROM and RAM. You can get bits out of ROM (Read Only Memory) but you can't, in normal operation, put any bits in. ROM is used for 'non-volatile memory', so that the data bits are still stored even when the whole system is switched off.

RAM (Random Access Memory) is misnamed, because practically all the memory ICs we use have random access, meaning that we can get at any one set of bits in the memory without having to sort through all the others.

There are several different types of technology which are used to make these memory chips, but the two important varieties are the two types of RAM (static and dynamic). Static RAMs are based on flip-flops (bipolar or MOS) which will flip over one way or the other when set or reset by an input. Dynamic RAMs are based on storage of charge in capacitors and this charge is called 'refreshing'. A dynamic memory is refreshed by applying a refresh pulse to each memory cell which stores a 1.

Organisation

Apart from the question of whether to use static or dynamic RAM, the main factor we need to take into account when dealing with memory is the way in which the memory is organised. Organisation in this sense means the way in which the memory cells are grouped. For example, one very popular way of organising memory is to have 1024 cells, each using a single common data input/output pin. This is classed as a $1K \times 1$ memory, the 1K (K in memory size means 2^{10} (1024), not 1000) referring to the total number of groups of memory cells and the 1 meaning the

number of data lines. A memory like this would (normally) need ten address lines (because $1024 = 2^{10}$) so that 1024 different address numbers can be coded in binary on the lines.

A 512×4 memory, on the other hand, would have 512 groups of four cells each, with four data pins for input and output signals. With only 512 groups, only nine address lines are needed ($2^9 = 512$), but at each address number, four bits are being written or read. The total number of bits stored in such a memory is 2048 (512×4).

Chip-Ability

An essential feature of all memory types is a chip-enable pin. At one logic voltage on the chip-enable, the memory can be used for reading or writing in the usual way, but with the chip-enable shut off, the memory data pins go 'floating' as if a three-state buffer were in circuit. This saves using an additional buffer chip and enables us to use large numbers of memories connected together without any other form of buffering.

How, then, do we connect memory chips to the main microprocessor (or CPU) unit? There's no simple answer, because it depends on how the memory chips are organised. Take, for example, the use of $4K \times 1$ chips. Each chip will provide one bit of data, so that we need eight chips to give a complete byte of memory data, 4K in this example. The data connections are simple, each data line from the CPU goes to a different memory chip. The memory lines are equally easy. 4K is 2^{12} , so that twelve address lines of the microprocessor are connected to all twelve address pins on each memory unit (Fig. 9). This would be the normal layout for a medium sized system using the INS8060, for example, which has only twelve address lines' other microprocessors which use 16 address lines would have four address lines left spare. The lines which are left spare are, of course, the higher order address lines numbered A12 to A15 (they start at A0, so the twelfth line is A11), because the lower order ones are the first to be connected.

The shape of the circuit board would have to be rather different if we were using, say $2K \times 4$ memories. Each memory chip would have four data pins, so that a complete data byte would need only two chips, and with only 2K to address, only 11 address lines would be needed. On the other hand, had we used $1K \times 8$, a single memory chip would be connected to all eight data lines and 10 of the address lines.

That's simple enough, but suppose we wanted more memory than could be supplied by a single band of memory ICs? We might, for example, find that 2K of memory

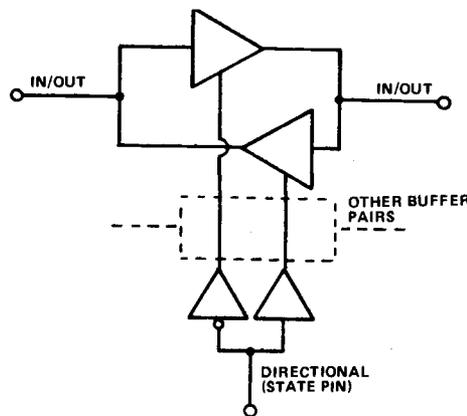


Fig. 8. The bidirectional buffer. The buffer stages are connected input-to-output with the enable lines driven so that the two buffers of a pair cannot be enabled at the same time. This arrangement is sometimes described as a 'transceiver' - an example is the quad transceiver 74LS243. An octal buffer such as the 74LS241 can be used in this way by connecting the enable inputs together.

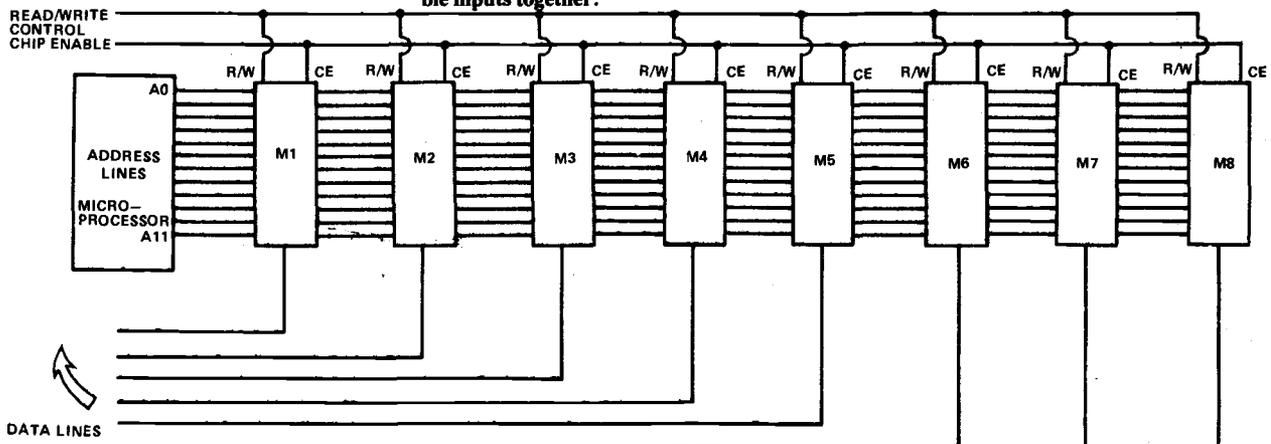


Fig. 9. Using single-bit memory chips. Eight chips are needed to form a memory bank and the read/write and chip-enable signals for each chip must be taken from the microprocessor - they will probably need to be buffered.

obtained from two of the $2K \times 4$ chips was insufficient and that we needed another $2K$. How do we cope with the extra? The answer is that we use one lot (two of $2K \times 4$) for the first $2K$ of memory addresses and the other lot for the second $2K$ of memory — but how? When we have two identical lots of memory chips they will all use the same address lines and the same data lines. In our example using $2K \times 4$ chips, we want to use the first two chips for the first $2K$ of memory and the second two for the next $2K$. Each chip, being a $2K$ chip, has 11 address lines and four data lines, and all the address lines will be paralleled. In other words, the A0 pin of each chip is joined and connected to the A0 pin on the CPU, the A1 pins of the RAM are similarly connected to the A1 pin of the CPU and so on. The data pins 0 to 3 of chips 1 and 3 are connected to data pins D0 to D3 of the CPU and the data pins 0 to 3 of chips 2 and 4 are connected to data pins D4 to D7 of the CPU.

Bits Of Memory

If these were the only connections, we wouldn't have a workable system, because a given address, say 10010110110, would fetch data from (assuming that we're reading memory) both lots of chips and something would end up frying tonight. 'Address decoding' solves the problem. The simplest method is linear address decoding. The highest address for chips 1 and 2 is 1111111111. The next number above this is 10000000000. The lower address lines are now all at 0, so that both lots of memories 1 and 2 along with 3 and 4 are fetching from address 0.

This is where the chip-enable pin comes into the picture. Suppose line A11 is connected to the chip-enable pin of memory chips 1 and 2, and an inverter, whose output is connected to the chip-enable pins of memory chips 3 and 4.

Consider what happens if the chip-enable is active, allowing the chip to operate, when it is at zero. Addresses 0000 up to 07FF (that's all zeros up to all 1s) will be fetched from chips 1 and 2 only, because line A11 is low, activating the chip-enable of those two chips. Because of the inverter, the chip-enable of memory chips 3 and 4 is high, putting their data outputs into the floating state. The data bytes for the first $2K$ of addresses are, therefore, read from memory chips 1 and 2 only. When the address number reaches 10000000000 (0800 in hexadecimal), the A11 line goes to 1, so that the chip-enable pin of memory chips 1 and 2 goes high, putting the data outputs of those chips into the floating state. The inverter action ensures that the chip-enable pin of memory chips 3 and 4 will be low, so that the next $2K$ of address numbers are read from these chips only.

Partial Control

This system is only a partial solution, though, because the decoding does nothing about lines A12 to A15. As the program count proceeds, these lines will be activated and if nothing is attached to them, the memory chips will be controlled purely by the lower lines.

Since the upper four lines can have $2^4 = 16$ possible addresses on them for any given address on the lines which we're using, the sequence of use of memory can be repeated 16 times.

All this address decoding business, incidentally, applies equally to ROM or RAM. The only extra complication which is present in RAM chips is the read/write pin which has to be taken to one logic voltage for writing data from the microprocessor to memory and to the other logic voltage for reading data from the memory to the microprocessor.

The microprocessor CPU will control such pins directly from its read/write control pin, or pins, which will be indicated on the pinout diagram.

Any Port In A Storm

Most microprocessor systems need nothing like the $64K$ of memory which could be addressed by sixteen address lines. Even a computer with fairly extensive capabilities may use only $16K$ of RAM, though its ROM and other use of memory addresses can bring the total up to $32K$. All in all, then, there are several address lines floating about if we want to load data into the CPU directly or feed data out. An address-decoded or memory-mapped input/output system makes use of buffers and latches which are controlled by a signal gated out from the address lines.

For example, suppose the ROM and RAM that we use in a system take up a total of $8K$. $8K$ of memory needs addresses up to 2^{13} , so that it uses 13 of the 16 memory lines and there are three left. Now three lines can be used in $2^3 = 8$ different sets of addresses, of which we have used one set in the $8K$ of memory addresses. That leaves seven sets of $8K$ ($56K$) of addresses which are spare if the top lines are fully decoded!

We can, for example, choose to use an address such as 36D6, which involves decoding all the address lines, or more simply, use any address which has line A13 high. Normally this would activate the memory, but we can easily arrange things so that when A13 is high, a gate circuit will disable all the memory chips, making use of the chip-enable inputs. That way, any memory address which has line A13 high can be used to activate a buffer and so connect the data lines to a connecting strip. The buffer would also be controlled by the read/write signals to ensure that signals were going in the right direction. A more common type of interface is an eight-bit latch, which holds data temporarily stored until either the CPU or any external circuits can deal with the bits.

Map Reading

Memory-mapping is a very common method of making use of the address lines to control inputs and outputs; porting is another. A port is usually a separate IC which is connected to the data lines and also to the control lines of the CPU, though most CPUs use some of the address lines. A typical port or PIO (Peripheral Input/Output) will have one or two sets of input or output pins — the usual eight connections to the data bus, and several (typically six) pins for control signals. It's a one-chip method of obtaining input or output at a time when the memory chips are not being used and because it's a single IC, manufacturers usually load on a lot of extra functions, such as being able to use some bits for inputs and others for outputs simultaneously.

Port ICs are generally designed specifically for one particular CPU, though they are capable of a remarkable number of actions. No two are completely alike and there are always some restrictions on their use as compared to memory mapping. For this reason, memory mapping is used much more.

There's no end to the number of specialised chips which are produced for use with CPUs like the Z80. Even the humble SC/MP has a combined port/memory chip, the INS8154, which almost needs an instruction manual of its own. The units dealt with here are, however, the ones you're most likely to find in smaller systems and, more important, the chips you will use if you start designing your own microprocessor systems. Good luck!

Ian Sinclair

Chapter 7

ANALOGUE SWITCHING

Analogue signals – how to switch and with what.

THERE ARE MANY electronic functions that need to be able to turn off and on analogue signals just as they would be by conventional mechanical switches. The relay used to perform that task but it has almost entirely been superseded by electronic analogue switches. The relay is still in use but it is now generally used to handle heavy voltages and currents. A small version of the relay, the reed relay (Fig. 1), still has many advantages that have not yet been overcome by electronic technology, these being very

low contact resistance, virtually zero noise generation and distortion and almost total isolation between the control and switching section.

These features make the reed relay an ideal switch for high quality audio signal routing. The device drawbacks are, that it is physically large, heavy, expensive, consumes considerable power, is susceptible to vibrations and generates interference.

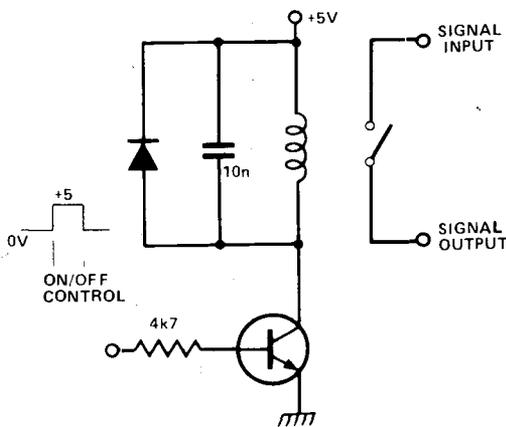


Fig. 1. A typical reed relay.

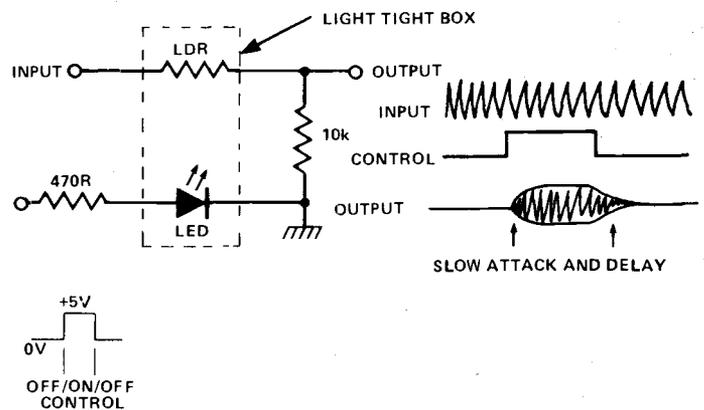


Fig. 2. A light dependent resistor can be used to make an analogue switch.

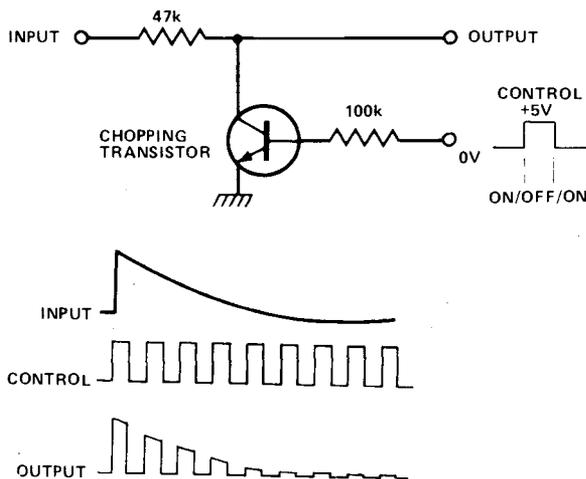


Fig. 3. A transistor chopper, often used to turn off an analogue signal.

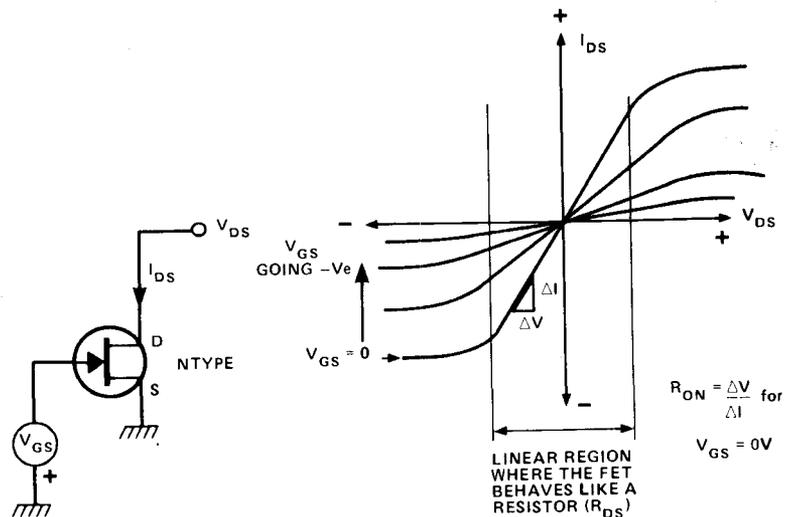


Fig. 4. N-type JFET characteristics.

Dependable Resistor

A simple electronic analogue switch can be made from a light dependent resistor (Fig. 2). When light from the LED shines on to the LDR, the resistance drops from a few megohms to a few hundred ohms. The device generates very little distortion and noise and is thus suitable for routing audio signals.

The response time of the LDR is very slow, sometimes taking 100 mS to switch, it is both relatively expensive and large and it consumes a large LED current. The transistor chopper, (Fig. 3), is often used as a simple device to turn OFF an analogue signal. This is done by turning ON the transistor and driving it hard into saturation, which in turn shorts the signal to ground. The transistor chopper is often used in organ and electronic piano circuits to produce audio tones by chopping the envelope waveforms with square-waves generated by a tone divider network. It is not easy to use the bipolar transistor as a floating switch, as most applications require but the JFET lends itself readily to this purpose. The characteristics of a JFET (Fig. 4) show that in the region where the curves pass through the origin the device is behaving very much like a voltage controlled resistor.

When V_{GS} is 0 V, the curve passing through the origin is at its steepest, the FET having at this point its lowest Drain Source resistance (R_{DS}), known as R_{ON} . This is typically a few hundred ohms. However, as V_{GS} is increased nega-

tively for an N type FET, the slope resistance increases until the pinch off voltage is exceeded. The FET is then 'PINCHED OFF' and the effective R_{DS} is typically a few hundred megohms. The JFET can be used as a variable resistance device changing from a few hundred ohms to a few hundred megohms in times much shorter than a micro-second. This, combined with smallness of size, low cost, low power consumption, a very high impedance at its control input and the ability of the drain and source to float, makes the JFET an ideal analogue switch.

The series switch (Fig. 5) passes the signal with very little attenuation when the FET is on and stops the signal when the FET is off. There is a small stray capacitance (a few picofarads), between the drain and source and this causes high frequency breakthrough when the switch is off.

The shunt mode shorts the signal to ground when the FET is turned on (switch off). The attenuation in this mode is R/R_{ON} which requires large values of R to get a large attenuation. To get the advantages of both types of arrangement, a series/shunt switch can be constructed using two FETs (Fig. 6).

When a FET switch is rapidly turned on there is often a click generated, partly as capacitive breakthrough from the gate and partly as an abrupt amplitude modulation of the analogue signal. This can be greatly reduced by band limiting the gate voltage (C2, R3) and by removing any DC component from the analogue signal (Fig. 7).

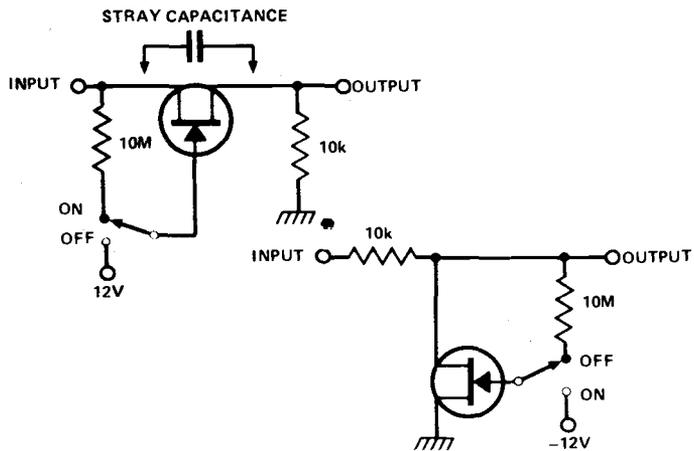


Fig. 5. The series switch (top) passes the signal when the FET is on and stops it when the FET is off. The shunt switch (above) shorts the signal to ground when the FET is turned on.

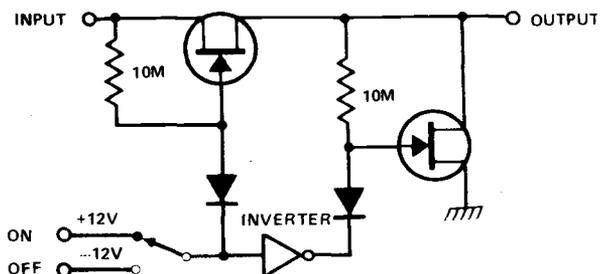


Fig. 6. This series/shunt switch combines the advantages of the two-circuits shown above.

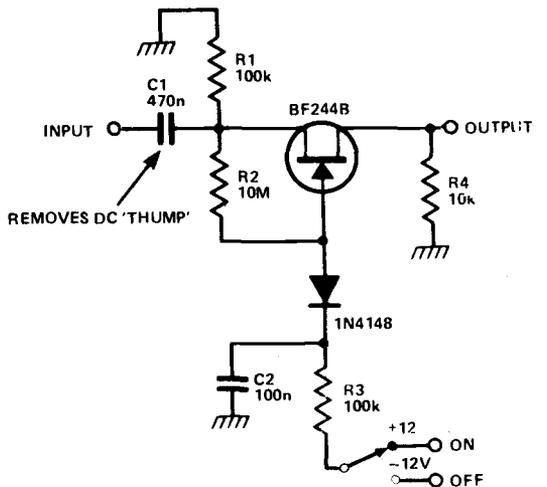


Fig. 7. A silent series switch for audio applications.

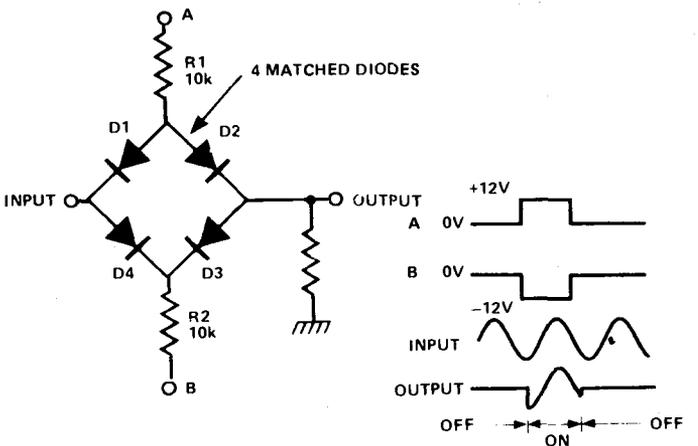


Fig. 8. The diode ring switch can operate at very fast speeds.

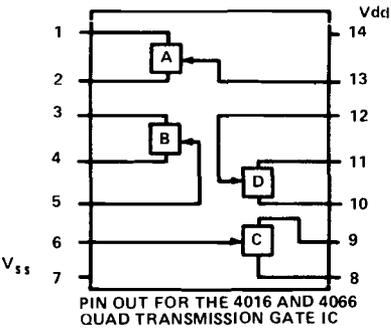
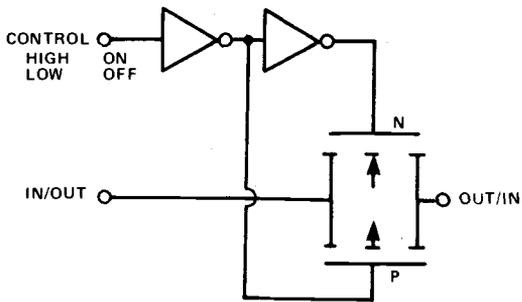
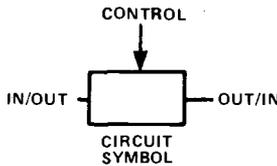


Fig. 9a. The CMOS analogue transmission gate (top) with 4016 and 4066 pin-outs (left).



* THE INPUT VOLTAGE MUST NOT EXCEED THE POWER SUPPLY VOLTAGE LEVELS OF THE 4016

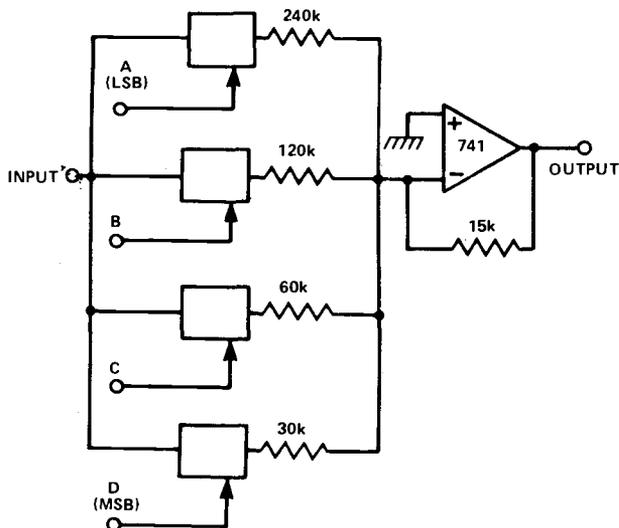


Fig. 9b. The 4016 can be used to construct a 4-bit multiplying DAC.

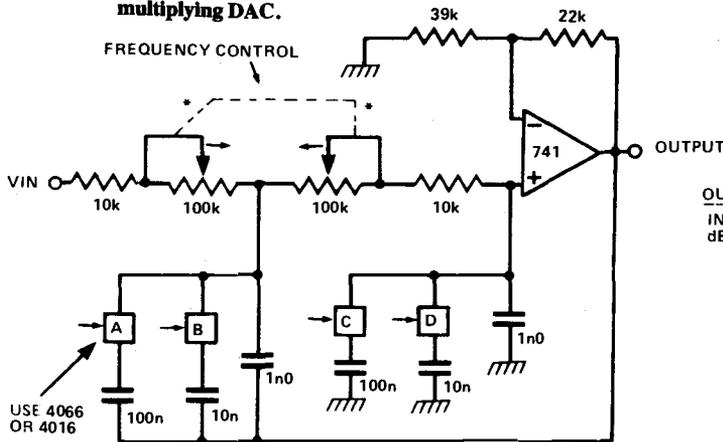


Fig. 10b. The low pass filter frequency response.

Ring An Ode

The diode ring switch (Fig. 8) is very simple in concept and can be operated at very fast speeds. When A and B are both at 0 V no signal can pass through the ring switch because there is always a reverse biased diode in the route. When A is +ve and B -ve (both with same amplitude), then the 4 diodes are all conducting. Any voltage at the input of this bridge will cause the same voltage to appear at the output.

Switch In Packs

It is now possible to buy a wide variety of integrated circuits that perform analogue switch functions. There are perhaps over a hundred different types available, many of which are JFET configurations. These are usually rather expensive and I shall only discuss the more common (and relatively inexpensive) CMOS devices. The CMOS analogue transmission gate (Fig. 9) is a bidirectional switch element, having a relatively low on resistance of a few hundred ohms and a high off resistance.

Gain Code

The 4016 is a very versatile electronic building block. It can be used to construct a simple multiplying DAC (Fig. 9). The gain of the amplifier is linearly proportional to the size of the 4 bit digital code and can be programmed to give any one of sixteen gains. A low pass filter (Fig. 10) can have its break frequency programmed by switching in timing capacitors. When all the gates are OFF, the timing capacitors are 1n. The low pass filter can then be tuned by the dual gang pot over the range 1.5 kHz to 15 kHz. When gates B and D are on, the timing capacitor is 11n and so the frequency range is 150 Hz to 1.5 kHz. Also, when A and C are on, the timing capacitor is 101n and so the filter range is 15 Hz to 150 Hz. It is possible to build quite elaborate filter structures, fourth or even sixth order designs and to make them programmable with analogue switches.

The analogue switch can be used to modify the parameters of an integrator (Fig. 11). The integrator slew rate can be programmed by a combination of RA,B,C and the output may be reset to zero using gate D, which shorts out the timing capacitor.

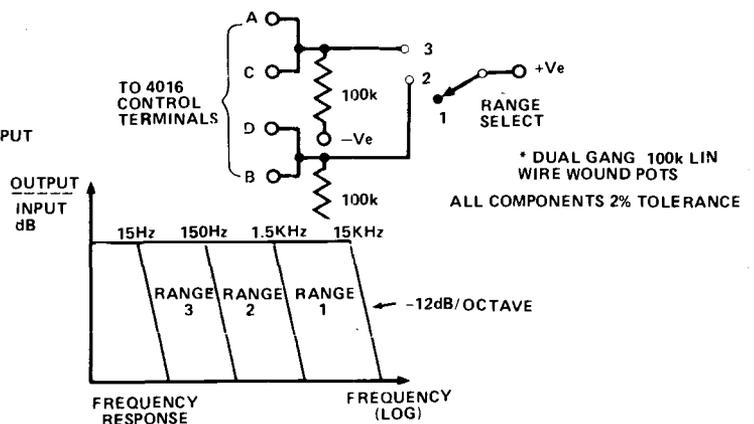


Fig. 10a. A switched-range low pass filter.

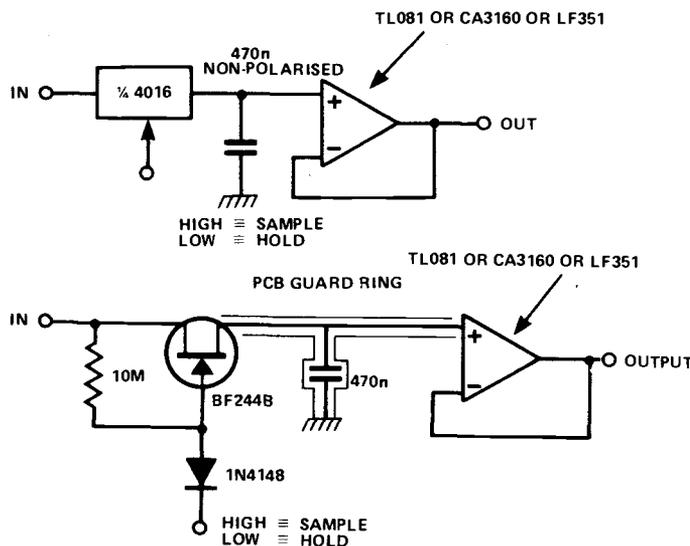


Fig. 12a. Sample and Hold circuits.

Hold On To It

Sample and Hold circuits also employ analogue switches. During the sample period, the storage capacitor is connected to the input voltage via the switch which is turned on. When the switch is turned off (Hold period) the voltage on the capacitor has got three possible discharge routes:

1. As leakage across the printed circuit board. This can be greatly reduced by provision of a guard-ring that surrounds the capacitor with a potential exactly the same as that on the capacitor. Surface leakage which is a function of potential difference is thus reduced by removing the potential difference.
2. The switch can discharge the capacitor with leakage currents. These are generally very small and insignificant.
3. The input bias current of the op-amp can discharge the capacitor, but if a FET op-amp is used the effect can be insignificant.

More and Mode

The 4051 is an 8 way multiplexer (Fig. 13). This device has a 3 bit binary code input which it decodes internally to turn on one of the eight analogue switches. The 4051 is effectively an 8-way single pole, code selected switch. There is also an inhibit input; a logic 1 at this pin turns off all the switches.

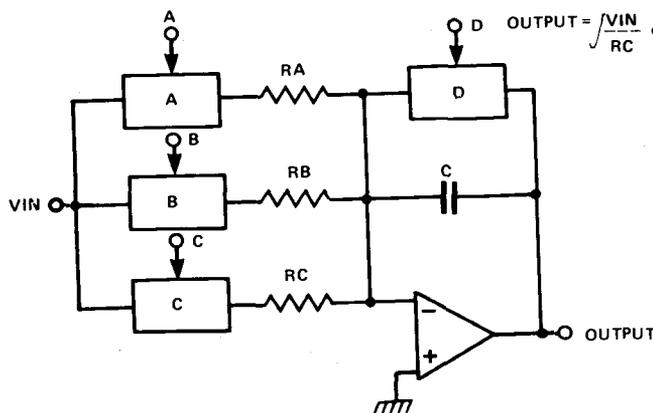


Fig. 11. A programmable integrator with reset to zero.

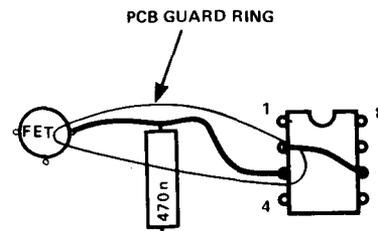


Fig. 12b. A guard ring surrounding the capacitor can reduce leakage across the PCB.

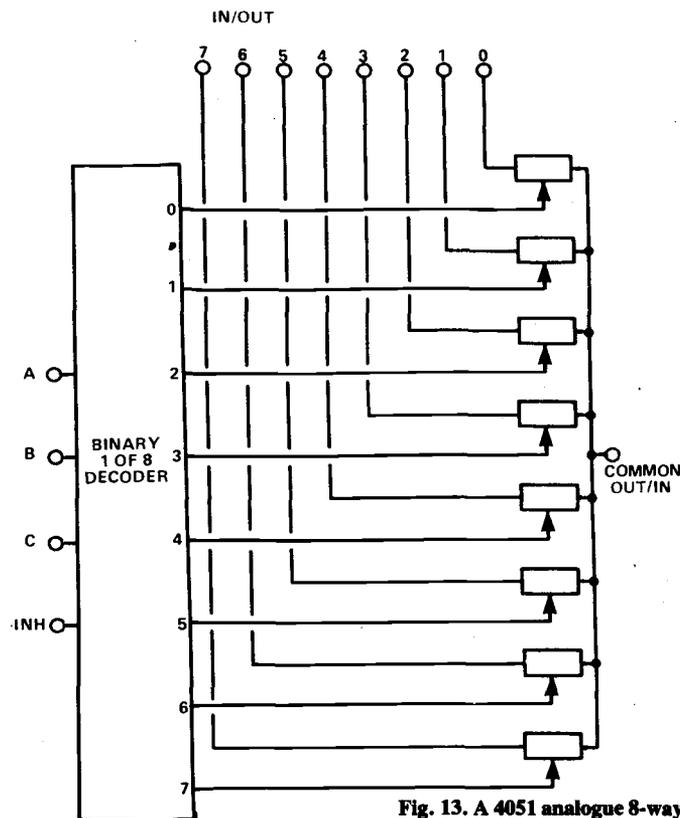


Fig. 13. A 4051 analogue 8-way multiplexer/demultiplexer

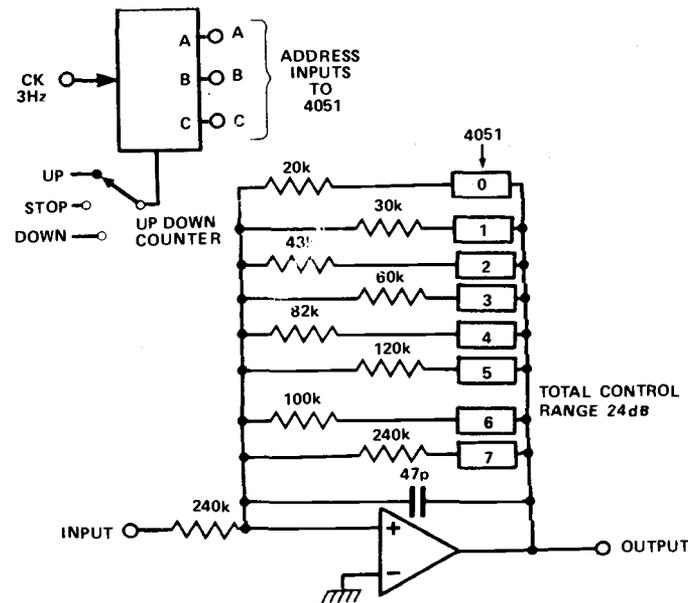


Fig. 14. An audio volume control with 3 dB steps.

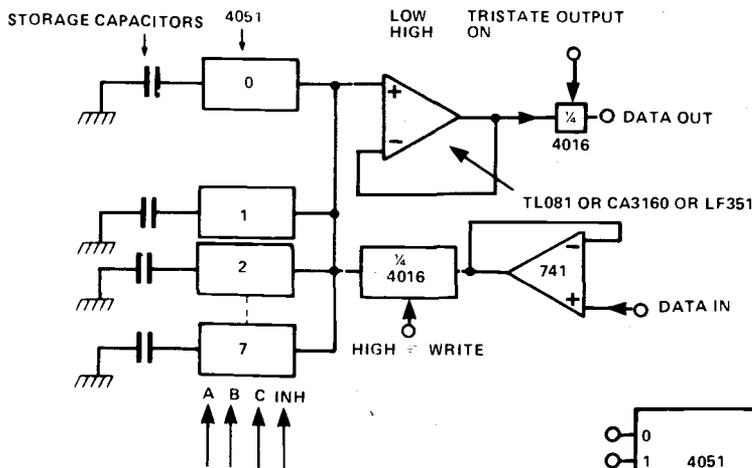


Fig. 15. (left). An 8-bit analogue RAM using a 4051.

Fig. 16. (right). A microprocessor data acquisition system using analogue switches.

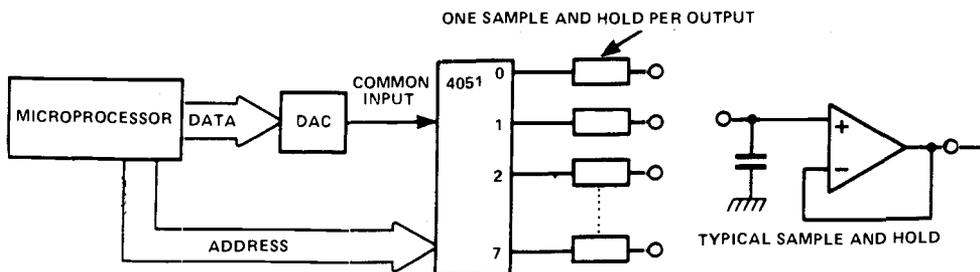
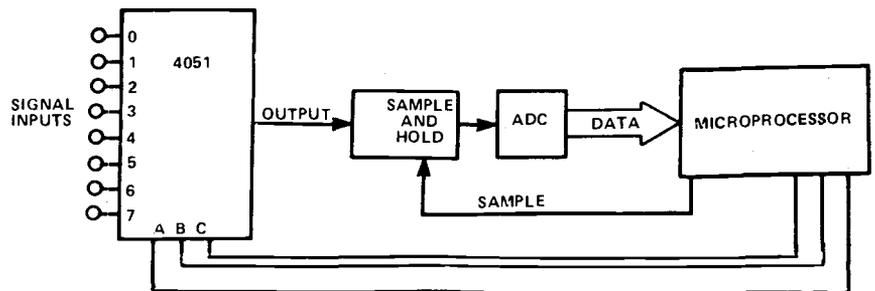


Fig. 17 (left). Analogue switches can also be used in a microprocessor data distribution system.

There are some problems to be encountered when using this device. The internal decoding exhibits some race conditions when the input address changes which may cause switches to momentarily overlap in their ON states.

If the 4051 is used a demultiplexer with sample and hold outputs, then the data on each output capacitor gets spread around to other outputs during the overlap periods. This 'make before break' effect can cause serious problems to occur. (There are JFET 'break before make' multiplexers but these tend to be rather expensive).

Louder Yet

A programmable volume control can be constructed with a 4051 and an up down counter (Fig. 14). The state of the count at any point in time determines which resistor is in the feedback loop of the op-amp. The resistors are arranged such that there is a 3 dB change in gain for each LSB change in the address code. By making the counter count up the gain will increase and vice versa. It is necessary to stop the counter at 000 and 111 otherwise the gain will roll round giving an abrupt change in level.

It is possible to construct an 8-bit analogue Random Access Memory using a 4051 (Fig. 15). Analogue information is written into memory by first selecting the address and then enabling the 'write' switch. The capacitor at this address is charged up to the voltage level of the data in signal. Reading is performed continuously using a FET op-amp so as not to discharge the storage capacitors.

This gives the RAM a tristate output capability, which when used with the INH input allows several RAMs to be built into a larger memory system.

MPUs Get Theirs

Analogue switches are used in microprocessor data acquisition systems (Fig. 16). An input multiplexer, addressed by the microprocessor selects which channel to look at. A sample and hold then freezes the selected input signal so that the ADC can perform a conversion on it. National Semiconductors make a single chip that performs most of this data acquisition. The chip, the ADC0817 has a 16 channel multiplexer, an ADC and output latch, but you have to provide your own sample and hold. Analogue

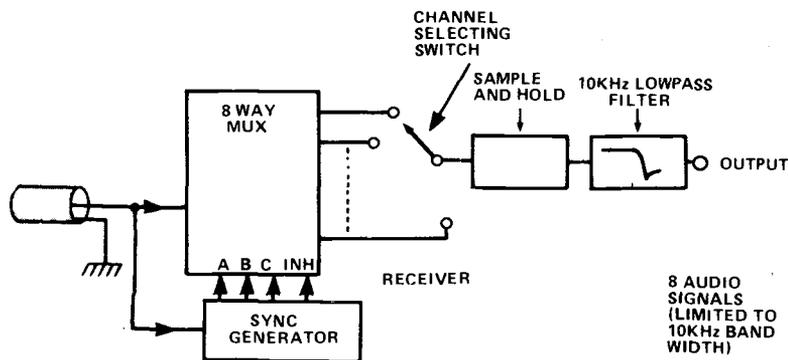


Fig. 18a. The receiver used in a pulsed amplitude modulation (PAM) multiplexed sound system.

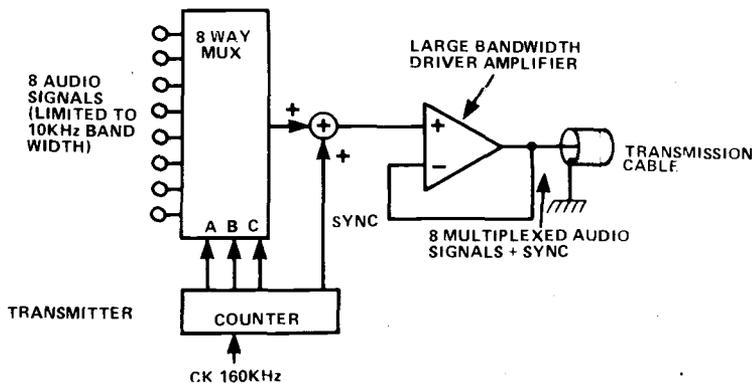


Fig. 18b. The multiplexed sound system transmitter.

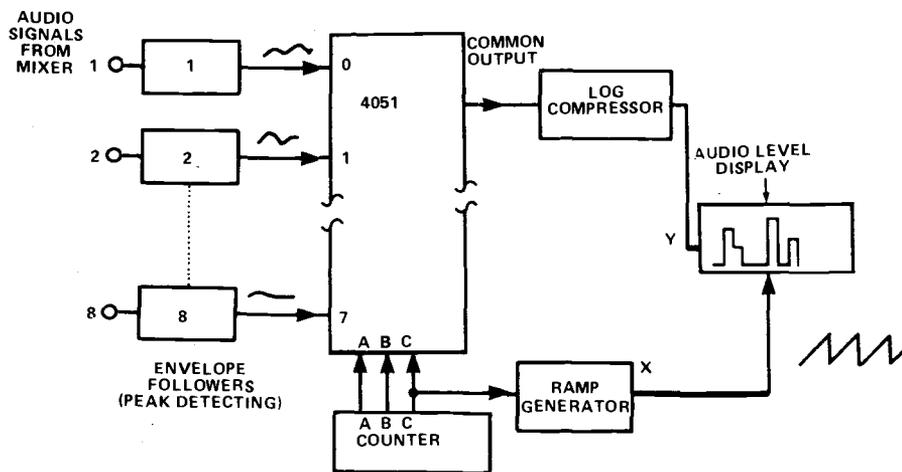


Fig. 19. (left). The levels of any number of mixer channels can be displayed on one screen with this multiplexed system.

switches are also used in microprocessor data distribution systems (Fig. 17). Data generated by the microprocessor is converted into an analogue voltage by the DAC and is then multiplexed into sample and hold circuits. This is a common technique for systems that require a large number of analogue parameters such as microprocessor-controlled music and speech synthesisers.

Plexing Info

In most telecommunication systems, a major cost is that of the wire that links transmitter to receiver. If several channels of information can be transmitted down one wire then the cost of the overall system may be considerably reduced (Fig. 18).

Eight audio channels, band limited to 10 kHz in this example, are fed into an 8-way analogue multiplexer. Each channel is sampled every 50 nS for a duration of 6.25 nS. The eight audio signals can thus be fed down one wire pair as a sequential series of pulses that represent the instant values of the signals in the eight channels. The process is known as *Pulse Amplitude Modulation (PAM)*.

Decoding is performed by stripping off the sync signal and using it to address the demultiplexer. The required channel can then be selected by monitoring the respective demultiplexer output with a sample and hold followed by a 10 kHz lowpass filter. It is important that the sampling frequency is at least twice the audio bandwidth so that aliasing effects can be avoided.

Mixing It In

Monitoring the signal levels in an audio mixer can cause problems, due to the large number that have to be observed. There are now several devices that use a conventional oscilloscope or TV to display all the information on one screen (Fig. 19). Each audio channel is processed by a peak detecting envelope follower. This generates a signal that describes the peak signal amplitude in that channel and it is known as a PPM (Peak Programme) response. These PPM signals are then multiplexed and passed through a single log compressor to give a display of level in dBs versus channel number on an XY screen.

Tim Orr

Chapter 8

BATTERIES

In this article we give enough information on the many different types of battery available to allow the right one to be selected for any particular application.

BATTERIES may be divided into two general classes; primary batteries and secondary batteries. Primary batteries or cells (strictly speaking, a battery is a group of cells connected together, but the term battery is commonly used for either form), only have a single working life. In general, once discharged their capacity to provide useful power ceases and they must be discarded. A primary cell can provide power as soon as it is assembled and requires no initial charging current.

Five types of primary cell are currently available. These are – Leclanche (or carbon-zinc) cell, Mercury cell, Alkaline cell, Zinc-Air cell and the Weston Cadmium cell.

Secondary batteries or cells require an initial charging current before they can be used, in the opposite polarity (or direction) to their discharge current. They can go through many charge-discharge cycles throughout their useful life, and can be stored for considerable periods in a discharged condition without deteriorating. Secondary batteries are also referred to as storage batteries. Two types of secondary battery are in common use – Lead-Acid battery and the Nickel-Cadmium battery (familiarily called the Ni-cad).

The Leclanche Cell

The construction and composition of a cylindrical Leclanche cell is as follows. The cell's outer casing is formed from zinc and this acts as the negative electrode. A central carbon rod, which is connected to an external metal cap, forms the positive electrode. The carbon rod is surrounded by a mixture of manganese dioxide and powdered carbon in a porous sack. This is called the *depolariser*. The rest of the cell is filled with paste of ammonium chloride – the *electrolyte*. The Leclanche or carbon-zinc cell, is commonly known as a dry cell.

These cells have a no-load terminal voltage of 1V5 to 1V6. The energy that they can supply is related to their size. Under-loading the terminal voltage of dry cells gradually decreases and internal resistance rises. When the load is removed, terminal voltage rises again but not to the original value. Over a number of discharge-rest periods, the no-load terminal voltage will gradually decrease as will the amp-hour capacity of the cell (Fig. 1). Once the no-load voltage drops to 1 volt or so the cell has come to the end of its useful life and should be given a decent burial. Leclanche cells are best suited to applications that require intermittent use or low-drain use for long periods.

Heavy-duty dry cells are available that will provide much higher discharge currents. These will supply several hundred milliamps for four to five hours at a time, whereas the ordinary cell will typically provide 100 mA or less for

similar periods. As might be expected, they cost more than ordinary dry cells. The heavy-duty dry cell deteriorates more slowly than conventional cells and will undergo more discharge-rest cycles before requiring replacement. These are sometimes marketed as 'Longer-Life' batteries. Conventional and heavy duty dry cells are compared in Fig. 1.

Size is not the only factor which governs the life of a dry cell. The ratio of the period of use to the rest period is an important factor. The old door-bell batteries which were about the size of a drink can would last for years. They could supply up to one amp but their rest-to-use ratio was very high. Temperature also affects the performance of dry cells. Optimum is between 20°C and 27°C. Terminal voltage and capacity is drastically reduced below 15°C, and almost useless below 5°C. Leclanche cells deteriorate when stored for long periods. Generally, the larger the cell, the less the deterioration.

Leclanche cells have a serious drawback. When left for long periods in a discharged condition, the other zinc container is gradually eaten away by the electrolyte which then finds its way to the outside, corroding surrounding equipment. Leak resistant versions are available, but these should not be left too long discharged either.

The internal resistance of a Leclanche cell rises steeply as it discharges. This can give rise to low frequency instability ('motorboating') in amplifiers. A large value electrolyte (1000 u+) across the supply rail will often eliminate this problem, and will often dramatically improve the sound reproduction from a transistor radio.

For applications requiring six volts or more at low currents, the layer battery has been developed. These are made up of square or rectangular layer cells, their shape enabling them to be grouped together with minimum waste of space. The common 9 V transistor radio battery is of this type. They suffer less deterioration than the round style dry cell. They are relatively low current devices. Round cells are better where fairly heavy consumption for fair periods is required.

The Mercury Cell

The mercury cell was invented in World War II by Dr Samuel Ruben. It has an anode of high purity amalgamated zinc and a cathode of compressed mercuric oxide-graphite separated from the anode by an ion-permeable barrier. The cathode is in contact with a steel container which provide the terminal connection. The electrolyte is a solution of alkaline hydroxide, the ions of which act as carriers for the cell's chemical action. The electrolyte is not consumed during discharge. The cell containers are nickel plated steel

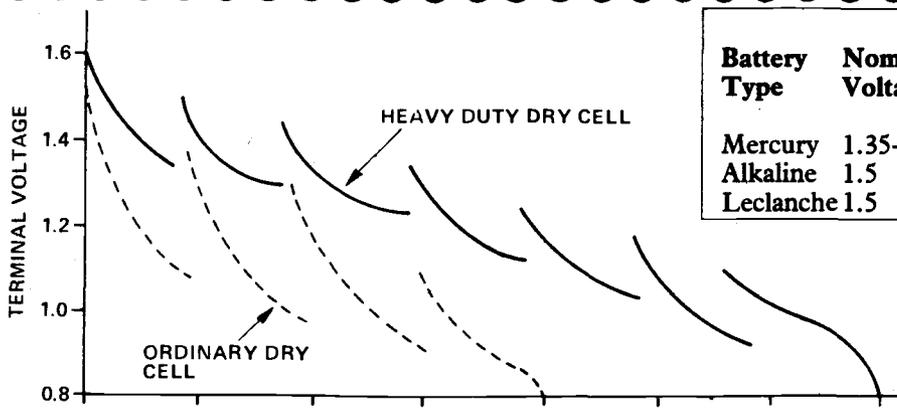


Fig. 1. Performance of ordinary and heavy duty dry cells discharged for several hours per day at fairly heavy current.

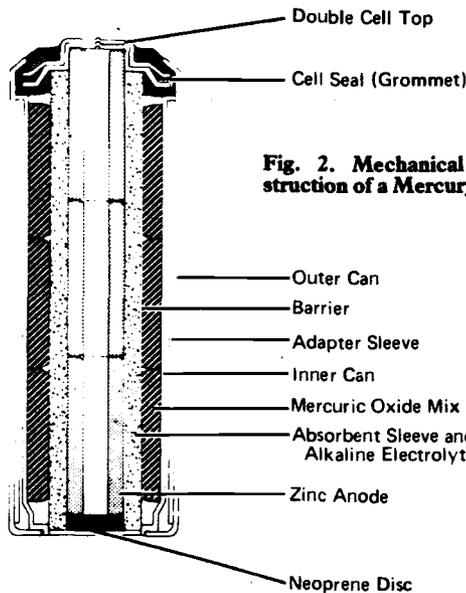
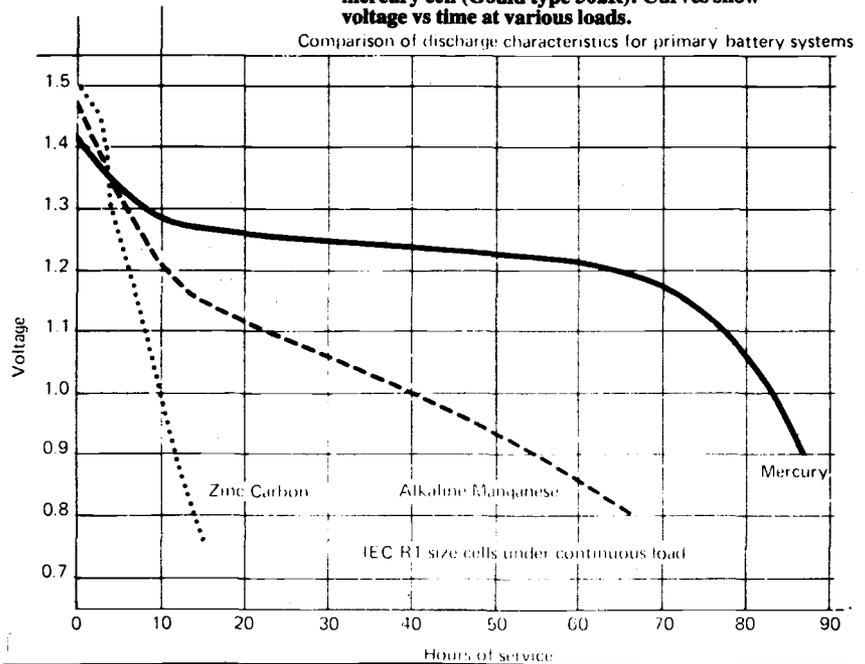


Fig. 2. Mechanical construction of a Mercury cell.

Fig. 4. Graph shows discharge performance of zinc-carbon, alkaline manganese and mercury batteries.



and thus do not corrode. Mercury cells are produced in a variety of forms, one of the most common is shown in Figure 2.

The no-load terminal voltage of mercury batteries is 1V35. This drops about 0V05 to 0V1 under load, but unlike Leclanche cells remains very steady throughout the greater part of its life. At the end of its life the terminal voltage falls away with increasing rapidity to less than 1V0. Typical discharge curves are shown in Fig. 3.

Mercury batteries may be stored for up to three years with only slight deterioration in terminal voltage and amp-hour capacity. Maximum storage temperature is 30°C, optimum is 21°C. The characteristics of these batteries are little affected by extremes in temperature. They work well down to -20°C and some at temperatures in excess of 100°C. Mercury cells are capable of discharge rates much greater than equivalent Leclanche cells, the internal resistance being maintained until near the end of their working life. Mercury cells do not leak if left for long periods. However, their price is several times that of equivalent sized Leclanche cells.

A range of voltages is available; typically 1V35, 2V5, 4 V and 8 V, in different sized packages. A new cell may be used as a voltage reference with an accuracy of 0V02 or better. Mercury batteries should always be used within the recommended discharge rate for which they are intended - they

TABLE 1

Battery Type	Nominal Voltage	Storage to 80% Capacity (months)	Watt-hours per kilogram	Watt-hours per cm ³
Mercury	1.35-1.4	30	101	98.3
Alkaline	1.5	30	77	57.4
Leclanche	1.5	6-12	48	32.8

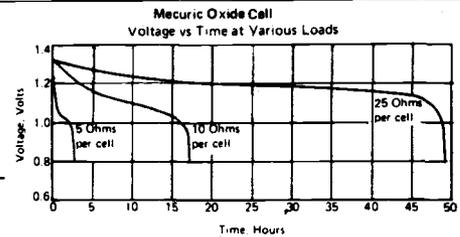


Fig. 3. Discharge characteristics of a typical mercury cell (Gould type 502R). Curves show voltage vs time at various loads.

cannot be recharged. Mercury batteries are used where voltage stability and long life are required. Their small size and high capacity are also advantageous in some applications.

The Alkaline Cell

Alkaline-manganese cells are constructed similarly to mercury cells, and have similar characteristics in that their terminal voltage is much more constant than Leclanche cells and that they are largely unaffected by temperature extremes. Their energy capacity is also similar to mercury batteries. A typical alkaline cell features a steel container which also forms the positive contact. This is in contact with the cathode which is a mixture of manganese dioxide and graphite compressed into cylinders that fit around the anode. The electrolyte is potassium hydroxide; the anode consists of zinc pellets. No-load terminal voltage of alkaline batteries is normally 1V5. They cost more than conventional Leclanche cells but less than mercury cells. Table 1. compares alkaline, mercury and Leclanche cells on the basis of storage and energy capacity for given size and weight. The discharge characteristics of these three types of battery are illustrated in Fig. 4.

The Zinc-Air Cell

Zinc-air cells are an outgrowth of research into fuel cells.

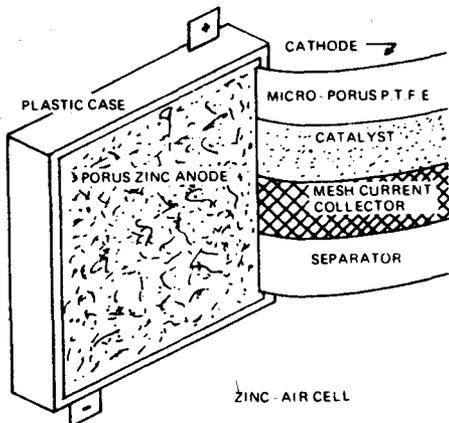


Fig. 5. Section of rectangular zinc-air cell.

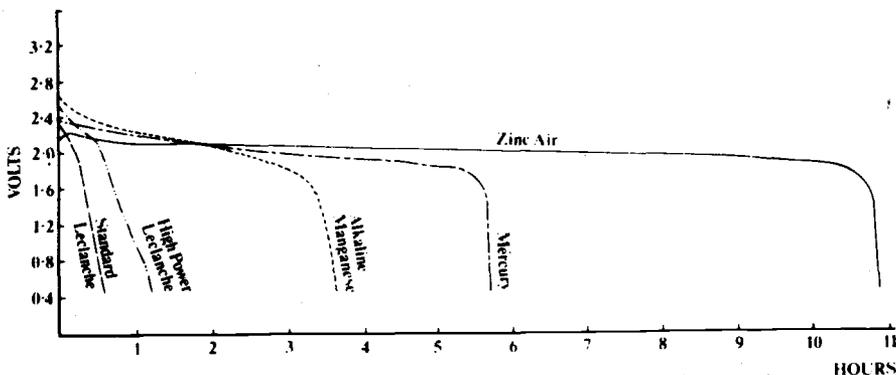


Fig. 6. Discharge curves of various types of cell compared to a zinc-air battery of the same physical size.

They were invented by Leeson Moos Laboratories in the USA and are now manufactured under license by various US and Japanese companies. Figure 5 shows the basic construction. The anode is amalgamated zinc powder and incorporates the negative terminal. The electrolyte, a concentrated solution of potassium hydroxide, is in contact with the anode. This construction allows large discharge currents without serious polarisation of the anode occurring. The anode structure is held in a tough plastic case. The cathode is constructed in several layers, held in a plastic frame. The outermost layer is a micro-porous PTFE plastic film. This allows atmospheric oxygen to come in contact with the electrolyte. The PTFE will allow air into the cell but will prevent the electrolyte escaping. Thus, the battery may be used in any position. On the inner face of the PTFE is a layer of catalyst. This is also in contact with the electrolyte and aids the chemical action of the cell without itself being consumed. The catalyst used provides a high current density at the cathode. A metal mesh collects the current generated by the cell and is the positive terminal connection. A permeable separator allows free passage of ions within the cell but prevents direct electrical contact between anode and cathode.

Zinc air cells find most use in applications requiring continuous or semi-continuous service at high currents. They have high energy to weight and volume ratios and have higher current output and amp-hour capacities than equivalent size alkaline or mercury cells. The maximum current capability of zinc-air primary cells is dependant on cathode area. Their amp-hour capacity is dependant on the volume of the zinc anode. The cathode will operate continuously provided its surface has sufficient access to the air.

Depending on the application, a zinc-air cell may produce six to eight times the output of an equivalent high power Leclanche cell or a weight saving of the same order for equivalent power outputs. (Leclanche cells are not of course capable of the high discharge rates of the zinc-air cells).

Zinc-air cells can deliver high currents continuously at a voltage which remains nearly constant throughout the discharge system. A comparison of the discharge characteristics of various cells and zinc-air batteries of equivalent size is given in Fig. 6.

Zinc-air cells have a nominal terminal voltage of 1V4 on no-load dropping to 1V2-1V1 under load with an end point voltage of 0V9 (discharged). Very small cells (AA size) can provide continuous discharge currents of 250 mA and up to 500 mA peak. This size cell would typically have a capacity

of 2.5 amp-hours after three months storage. Leclanche cells of equivalent size have a capacity measured in milliamp-hours. Zinc-air cells can provide 185 watt-hours per kilogram – compare this with the other primary cells in Table 1. Their main drawbacks are cost and availability.

The Weston Cadmium Cell

This cell is used *only* as a primary voltage standard or reference. It is unable to supply useful current – in fact a discharge current greater than about one milliamp will ruin it. The terminal voltage of a Weston Cadmium cell is 1V01864 at 20°C. It's not what you would call a handy figure to work with (especially using it in calculations!), its advantage lies in the fact that it can be quoted within plus or minus ten microvolts. The cathode (+ve) of the weston cell is mercury and mercurous sulphate paste. The anode (-ve) is an amalgam of cadmium and mercury in saturated cadmium sulphate. The cell is usually contained in an H-shaped glass vessel as illustrated in Fig. 7. To maintain the accuracy of the output voltage, the cell is often constructed in a temperature regulated container.

The Lead-Acid Battery

We shall now deal with the two most common types of secondary cell. The lead-acid battery has a long and honourable history. The car battery is probably the most familiar example. High current capabilities, long life and relatively low cost are attractive advantages. A forty amp-hour capacity car battery can supply several hundred amps for periods of a few seconds (ie. for a car starter motor).

The lead-acid cell consists of a lead and litharge (lead oxide) anode and a red-lead cathode immersed in

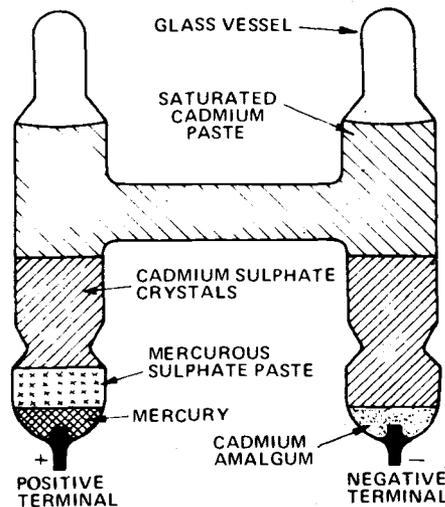


Fig. 7. The Weston Cadmium cell.

a liquid electrolyte of dilute sulphuric acid. This is contained in a hard rubber or polypropylene case. A filler cap for the electrolyte is provided and a vent hole for the release of gas during charging. For this reason, conventional lead-acid batteries can only be used in the upright position.

Lead-acid batteries are obtainable in a wide variety of sizes and amp-hour capacities. Some are designed for heavy duty service while others are designed for light or intermittent duty.

They are of course produced for innumerable applications other than the starting, lighting and automobile ignition applications.

The fully-charged, no-load terminal voltage of a lead-acid cell is between 2V3-2V4 volts. This drops under load to about 2V0-2V2. When discharged the cell voltage is typically 1V85. The amp-hour capacity is determined from a 10-hour discharge rate. The current required to discharge the battery to its end-point voltage of 1V85 per cell is multiplied by this time. eg. a 40 AH battery will provide 4 A for 10 hours before requiring recharge. Note however that the amp-hour capacity varies with the discharge current. The same battery discharged at a rate of 10 amps will not last four hours; on the other hand if it is discharged at 1 A it will last somewhat longer than 40 hours. The discharge characteristics are shown in Fig. 8.

Lead acid batteries may be operated over a wide range of temperatures, from -20°C to $+35^{\circ}\text{C}$. At low temperature, amp-hour capacity and discharge current are reduced and there is the possibility of the electrolyte freezing, depending on the specific gravity of the electrolyte. Preferred operating temperature is about $+20^{\circ}\text{C}$ to $+25^{\circ}\text{C}$.

Grave Matters

A direct indication of the state of charge in a lead-acid battery is the specific gravity of the electrolyte. This is

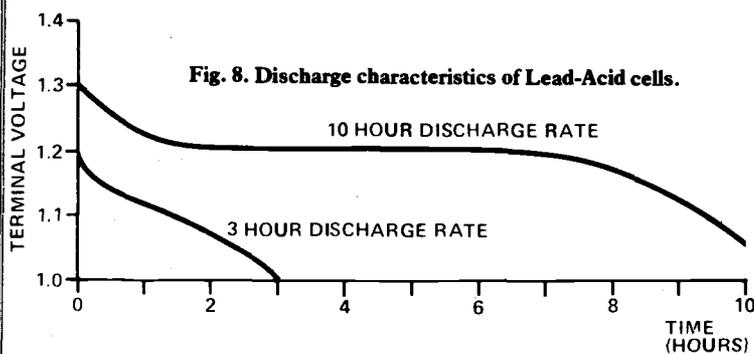


Fig. 8. Discharge characteristics of Lead-Acid cells.

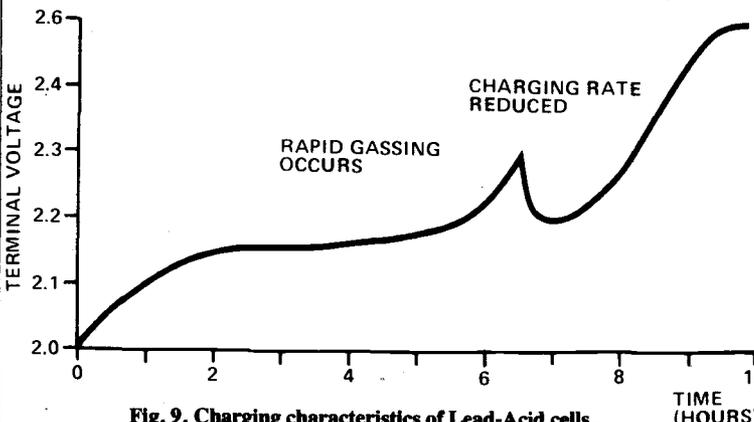


Fig. 9. Charging characteristics of Lead-Acid cells.

measured with a hydrometer. These can be obtained calibrated specifically for use with lead-acid batteries. The hydrometer reading for full charge will lie somewhere between 1.210 and 1.275, depending on the type of service for which the battery was intended. Table 2 shows the values of specific gravity expected in the various types of Lead-Acid batteries.

Charging is a fairly simple operation. The unfiltered output of a rectifier (dirty DC) may be used or any power supply that will provide the appropriate current at a voltage a little above the battery's fully-charged terminal voltage. Some means of varying the charging current is necessary. High wattage, low voltage lamps in series with the battery are suitable for the raw DC type of charger. The initial charging current for the fully discharged battery (cell voltage under 2V0), should be about 20 A per 100 amp-hours of capacity (ie. 8 A for a 40 AH battery). Once the electrolyte begins to gas rapidly, the cell voltage will be around 2V3 and rising rapidly. At this point, the charging current should be reduced to somewhere between 4-8 A per 100 AH until charging is complete. Check the specific gravity at half-hourly intervals. At the end of charging, cell voltage may rise to about 2V6 or more but this decreases slowly after the charger is removed, the terminal voltage then usually reading around 2V4 per cell (Fig. 9).

Peaceful Charge

Slower charging rates can be used, the battery taking longer to recharge. A continuous low-rate charge can be used ('trickle charging'). A constant current charger is best in this application, providing between 100 mA and 300 mA per 100 AH capacity. During charging, the electrolyte temperature should not be allowed to rise above 38°C (100°F). If the battery is hot and gassing rapidly, reduce the charging current. Hydrogen is released during charging. This is highly explosive. Keep flames and cigarettes away and avoid electrical sparks by turning off the charger when connecting or disconnecting leads to the battery terminals.

Lead-acid batteries should be charged in an open area where small electrolyte spillages and fumes cannot affect nearby materials. Cotton and synthetic materials are attacked by sulphuric acid and mysterious holes appear where the material has come into contact with battery electrolyte.

TABLE 2

S.G.	USE
1.210	emergency lighting, low duty.
1.245	light and intermittent duty.
1.260	car batteries.
1.275	heavy discharge, truck and tractor batteries.

The level of the electrolyte in each cell of a battery must be kept above the top of the plate. The loss of water by evaporation and decomposition during charging should be made up with distilled water. Do not use tap water as it usually contains minerals and traces of chemicals that contaminate the electrolyte. Distilled water is best added when the cells are gassing to ensure thorough mixing.

Light Work

If a lead-acid battery is used at relatively light duty then it should be periodically discharged through a dummy load, at

Q1 - Q7 2N3819 OR SIMILAR
 Q1, Q2 SELECTED FOR LOW
 I_{ds} ON TEST (≈ 8 mA)
 Q3, Q7 SELECTED FOR HIGHER
 I_{ds} ON TEST (10-18 mA)

*MORE FETS MAY BE PARALLELED TO
 INCREASE CHARGE CURRENT
 *THE ZENER VOLTAGE SHOULD BE 1.2
 TIMES THE BATTERY VOLTAGE.

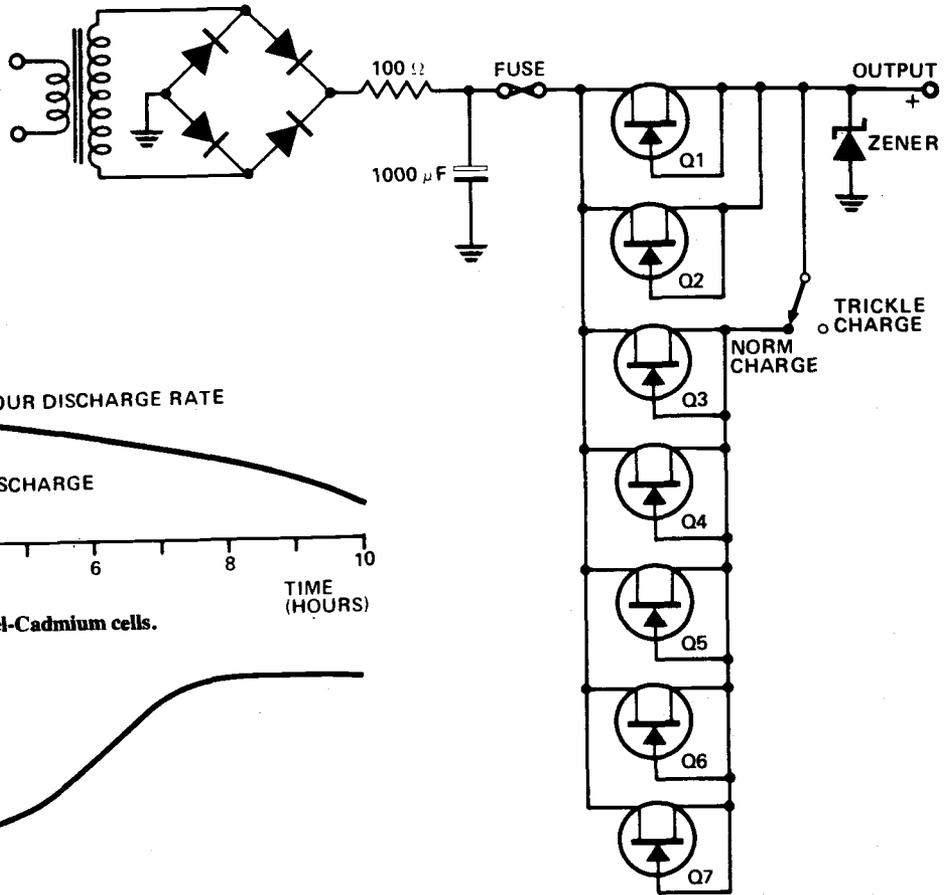


Fig. 12. Constant-current charger for Nicad Batteries

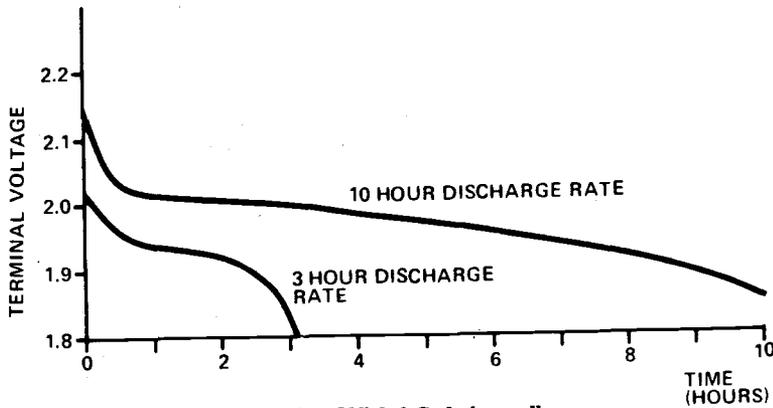


Fig. 10. Discharge characteristics of Nickel-Cadmium cells.

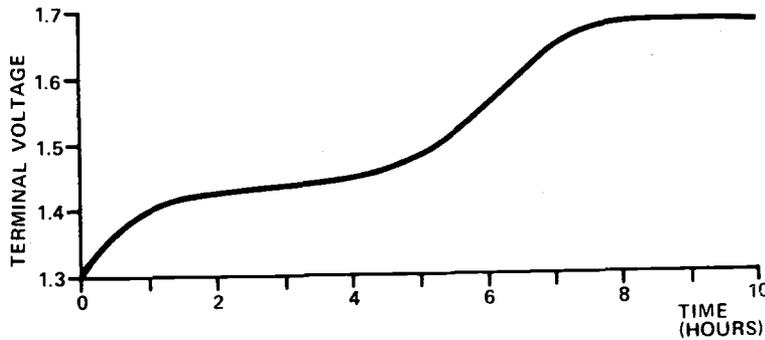


Fig. 11. Charging characteristics of Nickel-Cadmium cells.

its normal rate and then immediately recharged. Lead-acid batteries should not be overcharged at high current as this causes the plates to buckle and slake (which may result in a short circuit). Neither should they be left in a discharged state as the lead sulphide produced during discharge may undergo a generally irreversible physical change resulting in reduced battery capacity. Batteries in this condition are referred to as *sulphated*. This condition may sometimes be remedied, at least partially, by trickle charging for a considerable period. Eventually, sulphated cells self-discharge.

In normal operation, lead-acid batteries should be overcharged from time to time, at about half the normal rate, until half-hourly readings of the terminal voltage and electrolyte specific gravity show no further increase. This action removes sulphate and restores the plates to their normal condition. Spilled electrolyte should be neutralized with an alkali solution. This is simply made by dissolving 4-6 tablespoons of common baking soda (sodium bicarbonate) per litre of water, using as much water as necessary. When applied to spilled electrolyte, foaming occurs. When the foaming has stopped the residue should be washed away with clean water. If washing down the top of a battery with this solution, do not let any into the cells!

The Nickel-Cadmium Cell (Nicad)

Nicad cells use a potassium hydroxide electrolyte. In a typical unit the positive and negative plates are both perforated steel. The positive plate is filled with nickel hydrox-

ide, the negative plate with finely divided cadmium mixed with a little iron to prevent it flaking and losing porosity. The electrolyte has a specific gravity of 1.15-1.2, depending on the type of service, it does not undergo any chemical change during discharge. Very little electrolyte is needed and the positive and negative plates are very closely spaced.

Nicad batteries are made in a wide variety of sizes and amp-hour capacities; miniature ones for use in cameras, calculators, etc., up to large heavy-duty types similar to car batteries. They may be operated over a wide temperature range - similar to that of lead-acid batteries. At low temperatures, the amp-hour capacity does not diminish as much as with lead-acid batteries. However, the electrolyte may freeze. As Nicad batteries may be sealed, they can be used in any position. The no-load terminal voltage of a nickel-cadmium cell is typically 1V3-1V4. This drops to about 1V2 volts when discharged. As the electrolyte does not change during discharge (as it does in lead-acid batteries), the number of amp-hours obtained from a Nicad battery is much less affected by the discharge rate than are lead-acid batteries (Fig. 10).

As Nicad batteries can be made quite small, and can be recharged, they are eminently suitable for use in portable electronic equipment such as calculators, tape recorders, hand-held transceivers, camera flash units, etc. They can withstand considerable vibration, are free from sulphating or similar problems, and can be left in any state of charge without ill effect. Charging should be done with a constant-

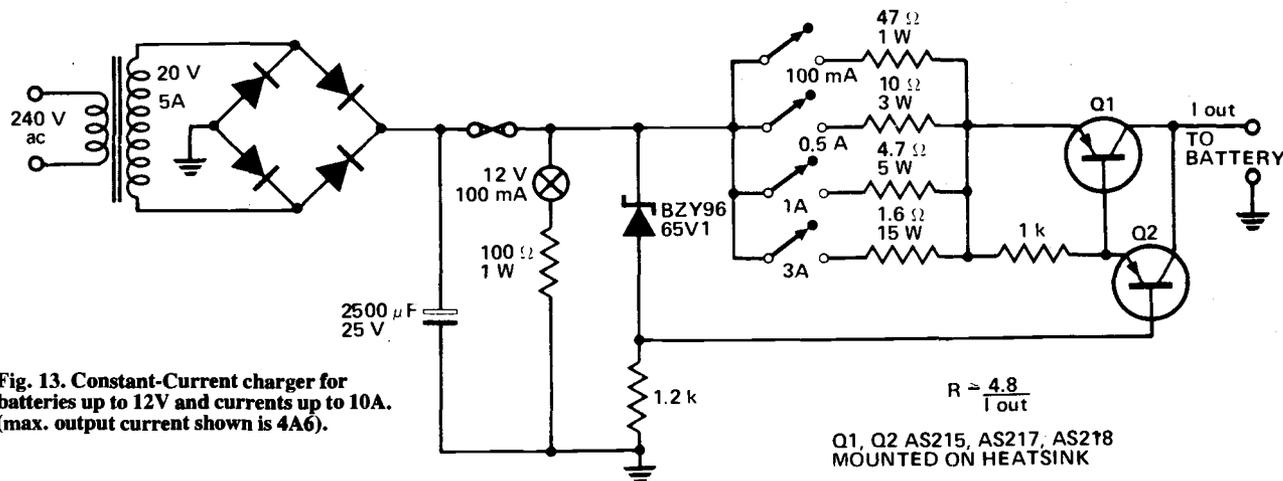


Fig. 13. Constant-Current charger for batteries up to 12V and currents up to 10A. (max. output current shown is 4A6).

current charger. The charging rate for the quickest charge should be no more than 1.5 times the 10-hour discharge rate. Most manufacturers recommend a charge rate and a trickle or float charge rate and this is best adhered to. Charging characteristics are shown in Fig. 11.

One method of producing a constant current charger is to place a resistor in series with a supply having a voltage three or four times the battery voltage. A better method is shown in Fig. 12. Junction FETs are selected on test for similar I_{DSS} currents and a number are connected in parallel as shown to supply the rated charge current. The FETs are in series with the rectifier output and the drain-source characteristics provide a constant current output. The maximum output voltage should be limited by a zener diode to about

1.2 times the rated battery voltage.

Another constant-current charger is shown in Fig. 13. This will charge batteries up to 12 V at currents up to 10 A with a suitably-rated transformer and rectifiers. The output current is selected by closing one or more switches. Lower values of R, with values according to the formula given, will provide increased output current.

Nickel-cadmium batteries should *never* be short circuited. This causes internal overheating and the battery may explode.

Never dispose of Nicad batteries in a fire or incinerator. This too will cause them to explode! The nickel-iron battery is an earlier counterpart of the Nicad and has similar characteristics.

SPOT DESIGNS

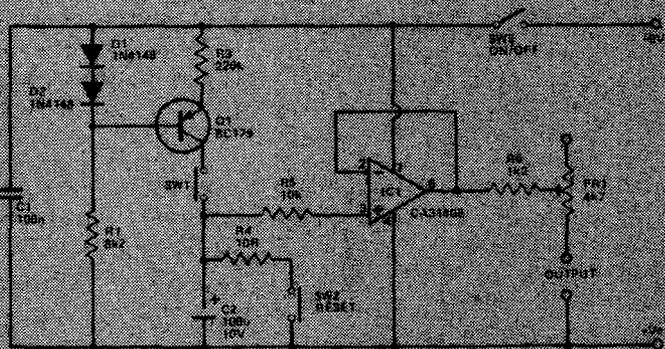
D.M.M. to Stopclock Converter

THIS SIMPLE add-on circuit can be used with a DMM switched to the 1 mA range to give a stopclock having a range of 0-99 S (or 0-199 S for a 3½ digit instrument). It can also be used with an ordinary analogue multimeter or panel meter, giving a range of 0-100 S, but the resolution will be lower than with a digital instrument.

The unit relies on the fact that a linear rise in voltage is produced across a capacitor if it is fed with a constant charge current. The capacitor (C2) must be a high quality type. The use of a tantalum bead component is therefore recommended. C2 cannot simply be charged from the supply lines via a resistor, since the voltage across the resistor would drop as the voltage across C2 increases. This would give a decreasing charge current as C2 charges exponentially and the required linear voltage slope would not be produced. C2 is, therefore, charged from a conventional constant current source which is based on Q1, D1, D2, and R1 form a simple shunt regulator circuit which bias the base of Q1 approximately 1V3 below the positive supply potential. There is a voltage drop of about 0V65 across the base-emitter terminals of Q1, giving about 0V65 across emitter resistor R3. This gives an emitter current of roughly 3mA and, as the collector and emitter currents of a high gain device (such as the BC179 used in the Q1 position) are virtually identical, a constant charge current of about 3 mA is fed to C2 when SW1 is operated. This low charge current together with the fairly high value of C2 produces a suitably long time constant.

It is essential that the voltmeter circuit takes no significant current from C2 as this would affect accuracy and would result in a decaying reading at the end of a timing run. Operational amplifier IC1 is, therefore, used as a unity gain buffer stage which gives an input impedance of about 1.5 million megohms and ensures that there is no significant loading on C2. FR1 enables the sensitivity of the voltmeter circuit to be adjusted to the correct level. In practice, SW1 is depressed for (say) 90 S and then FR1 is adjusted for the appropriate reading on the DMM.

SW2 is a reset switch and this discharges C2 (via current limiting resistor R4) if it is briefly operated. SW3 is an ordinary on/off switch. The current consumption of the circuit is only about 4.5 mA.



Chapter 9

G_m REVISITED

(Nothing to do with American car manufacturers) G_m is in fact a throwback from the days of valves, now finding a new lease on life with up-to-date semiconductor devices.

MANY A LONG YEAR AGO, when transistors were an item which hadn't been dreamt of by science fiction writers, we all used valves, and we all knew the magic letters G_m. G_m stood for a quantity called mutual conductance, and it measured an important feature of the valve from which we could work out how much voltage gain we could get out of a given bottle. Well, the years have passed, and valves are dead for many purposes, but G_m lives and is back working for us.

It's odd that G_m should have gone out of fashion for so long, because the idea of G_m is even more useful in transistor amplifier circuits than it ever was in valve circuits. Still, the idea seems to be coming back in a big way, so let's take a look at it.

Mutual conductance of any electronic device means the ratio of signal current at the output to signal voltage at the input. For a transistor, this is the ratio $\tilde{I}_c / \tilde{V}_{be}$. \tilde{I}_c being the collector current and \tilde{V}_{be} the voltage between base and emitter, Fig 1. The squiggle above the letters means that it's AC signal voltage and currents we're talking about not the steady bias voltages and currents.

Using G_m therefore allows us to represent a valve or transistor as a generator of signal currents, the amount of signal current being G_m V_{in}. Now a current generator means a device which will deliver its current into any load, high or low. No valve or semiconductor is really like this, but for most of the uses we make of transistors, the idea of a current generator is not far from the mark.

Current Generators

If a transistor were a perfect current generator, it would have an infinite resistance at its output. That means just that a signal voltage applied between the collector and the emitter would cause no collector signal current. Once again, it's not quite correct but not far from the truth. A bit of collector signal current does flow, but not very much,

about as much as would flow if there were a resistor of around 40k between collector and emitter.

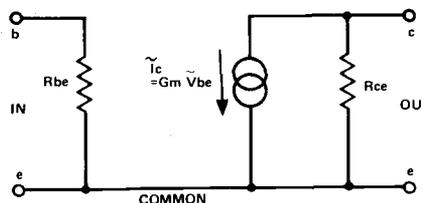


Fig. 2. An equivalent circuit for a transistor.

Now the usefulness of all this is that it allows us to draw an equivalent circuit for a transistor. An equivalent circuit is a circuit made of simple components which behaves in just the same sort of way as some device which is, in reality, much more complicated. A simple equivalent circuit for a transistor is, therefore, as shown in Fig 2. It consists of a current generator, which generates a signal current G_mV_{be}, and a resistor of about 40k in parallel. This simple circuit accounts for the size of the signal current at the output (the collector) and the output resistance between collector and emitter.

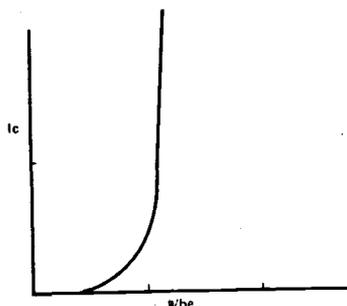
How does this help us? Quite a lot if we remember all the time that equivalent circuits are about signal currents, not about bias currents. As far as signal currents are concerned, the positive supply line of an amplifier is just as earthed as the earth line. Why? Because in the power supply there's a smoothing capacitor of several thousand microfarads, connected between the +ve and -ve lines. As far as DC is concerned, this capacitor is an insulator; but for AC signals the capacitor is just a short circuit, shorting the +ve line to the -ve line. When we connect a load resistor between the collector terminal of a transistor and the positive line, then, as far as signals are concerned the load resistor is connected between collector and emitter. Draw this into the equivalent circuit, and the result is Fig. 3. Back in the old days of valves (nostalgia corner, this!) we found the sum of these two resistors in parallel, which was

$$\frac{R_{ce} \quad R_L}{R_{ce} + R_L}$$

and then the voltage signal out was just the current signal times this resistance (Ohm's Law still rules, OK?) giving

$$\frac{G_m \quad R_{ce} \quad R_L}{R_{ce} + R_L}$$

Fig. 1. Mutual conductance, I_c/V_{be} for a transistor.



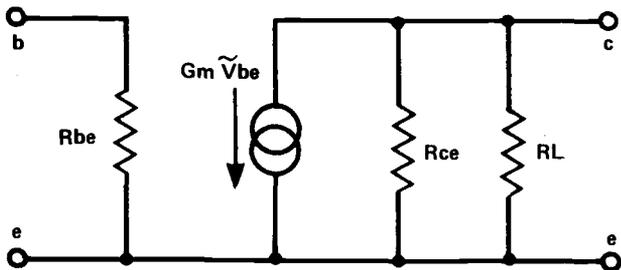


Fig. 3. For AC signals, a load resistor connected between collector and positive supply behaves as if connected between collector and emitter.

e = CHARGE CARRIED BY AN ELECTRON
 k = BOLTZMANN'S CONSTANT
 T = TEMPERATURE IN KELVIN SCALE
 I_c = STEADY (BIAS) COLLECTOR CURRENT

Simple Silicon

One of the things that makes life simpler in these days of silicon transistors is that the quantity R_{ce} , the output resistance of the transistor, is quite a large value compared to most of the load resistors we use. An output resistance (the usual symbol is h_{oe}) of 40k is quite a bit larger than the 3k3 or so we use as a load, so that most of the signal current from the transistor is through this resistor in the equivalent circuit. That simplifies the output voltage to $G_m R_L$ so that the gain of a transistor amplifier is just $G_m R_L$.

If it's as easy as that, why don't we see it in text books? The reasons are historical — we didn't start with silicon transistors, and a transistor, unlike a valve, doesn't have a constant value of G_m . If we plot a graph of collector current against base voltage (as in Fig. 1), the result is not the nice straight line we get when we plot such a graph for a valve, or the not-too-crooked line we get when we plot the graph for an FET, but a very curved line indeed. This indicates that the value of G_m is not constant, but a value which changes as the current through the transistor changes. This, coupled with the rather low output resistance of the early germanium transistors, seemed to seal the fate of G_m for good.

Ebers Moll

A few years back, though, the Ebers-Moll equation was noticed. If you've never heard of it, you're not alone; very few text books mention it, and some mention it without explaining it. Very briefly, it's an equation which links the collector current with the V_{be} value for a transistor. In other words, it's the equation for finding G_m . Now the full equation is a fearsome looking thing, full of mathematical symbols you may never have seen before. It repays close attention, though, because most of the symbols are of quantities that are pretty well constant, and only two of them vary very much. One of them is the steady bias current, I_c , and the other is temperature. As it happens, temperature, for the purposes of the Ebers-Moll equation, is measured in

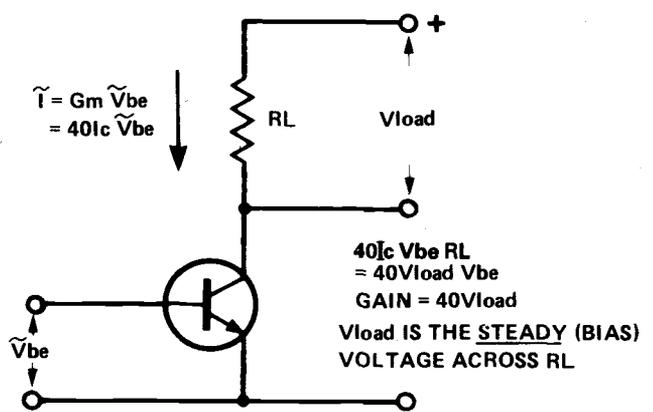


Fig. 4. Transistor circuit with load resistor (R_L). G_m can be replaced by $40I_c$.

the Kelvin scale, which starts at the absolute zero of temperature around -273°C . Room temperature is therefore around 293K (no degrees sign) in the Kelvin scale, and a few degrees above or below doesn't make much difference to the equation.

That leaves I_c as the one thing that really affects G_m , and the relationship works out at approximately

$$G_m = 40I_c \quad (I_c \text{ in mA})$$

Put in words, that means we can take a G_m value of 40 times the steady bias collector current in milliamps. For a bias current of 1 mA, the G_m value of a transistor is 40 mA/A. Looks too good to be true, but it really does apply to any silicon transistor, apart from a few freak types.

This brings back the G_m idea in a big way, and we can forget a lot of the old formulae we once used in calculating the design of transistor amplifiers. The fact that G_m is not constant but varies with the bias current is, oddly enough, a help rather than a hindrance.

Gain

Going back to our equivalent circuit, and ignoring the large output resistance of the transistor, we can now write $40I_c$ in place of G_m (fig 4). This makes the gain of a transistor with load resistor R_L become $40I_c R_L$. But I_c in this equation is the *steady* bias collector current, and so $I_c R_L$ must be the steady DC voltage across R_L , the load resistor. This makes calculating the gain of transistor amplifiers with resistive loads a bit easier than falling off a log. Pick a value of voltage across the load resistor, multiply by 40, and that's your value of gain!

For example, we very often design voltage amplifiers so that about half of the supply voltage is dropped across the load resistor. For a 9 V supply, that's 4V5. Do this, and you can expect a voltage gain of $40 \times 4.5 = 180$ times. Don't believe it? It works all right, and tests on a single transistor amplifier confirm it as a rule of thumb. You don't, of course, expect to get a gain of *exactly* 180 in the case illustrated — there are 20% tolerances on load resistors apart from anything else, but you're never far out; that's what a rule of thumb is for.

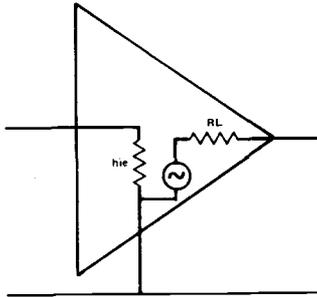
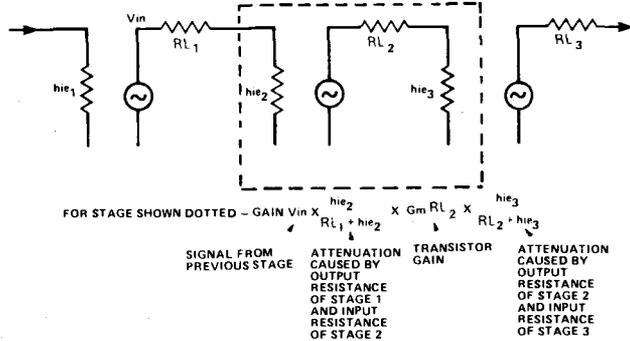


Fig. 5. Calculating how much signal is passed on to subsequent stages.



When you couple a single transistor amplifier to another stage, of course, that's another story. You may have set the gain of the first stage to 180 times, but not all of its output signal ends up usefully at the input of the next stage.

Reason? The next stage has a rather low input resistance, and feeding signal from the collector of one transistor into the base of another, even if they are directly connected, is rather like feeding signal through a voltage divider. There are, in fact, two ways of calculating how much of the signal is passed on. One simple way is to imagine a voltage divider (Fig 5) in which the load resistance of the first stage forms the upper resistor and the input resistance h_{ie} of the second stage. The quantity h_{fe}/G_m , where h_{fe} is the current gain of the transistor, a quantity which *does* vary between one transistor and another. For a transistor with $h_{fe}=100$, G_m set to 40 (1 mA collector current) h_{ie} is $100/40=2k5$. If we feed this from a transistor with a 4k7 load resistor, the amount of signal reaching the second transistor is

$$\frac{2.5}{2.5+4.7} = .35$$

of the signal at the output of the first. This brings the gain of the first transistor stage down to $180 \times .35 = 63$ which is the sort of value we usually measure for one stage of a multi-stage amplifier.

With all this going for it, G_m is coming back, folks. As Sam Goldwyn is supposed to have said, "simplicate and add lightness". Let's hope we've added a bit of lightness.

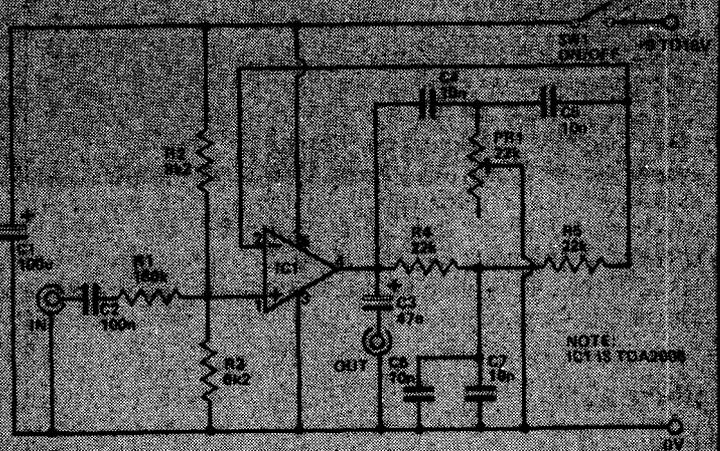
K. T. Wilson

SPOT DESIGNS

CW Filter

One of the most desirable features of a communications receiver is a set of really good IF filters for the various modes of modulation. Presumably due to the expense and complexity of such circuits, this is lacking in many sets. In such cases it is often possible to obtain a worthwhile improvement in performance by using an audio filter with a response tailored to suit the required mode of reception. A filter of this type is most helpful for CW (Morse) reception, where only a very narrow bandwidth is needed. In fact, an infinitely narrow bandwidth is the theoretical ideal, since the CW signal is just a single frequency! In practice, a bandwidth of a few hundred Hertz is necessary, since it is very difficult to tune to a signal and stay accurately tuned to it with a narrower bandwidth.

The circuit uses an integrated circuit audio amplifier (TDA2006) in the non-inverting mode, with R2 and R3 being used to bias the non-inverting input. C4 to C7, R4,5 and PR1 form a T-notch filter, which provides frequency selection negative feedback over IC1. R4 and R5 also bias the inverting input of the device. A T-notch filter allows most frequencies to pass readily, but at the close to its operating frequency it gives a high level of attenuation. Thus, in this case it gives virtually 100% negative feedback and only about unity voltage gain at most frequencies. However, at its operating frequency there is little feedback and high voltage gain. This gives the required narrow passband.



PR1 controls the bandwidth of the filter and a fairly flat response will be obtained at maximum resistance. Decreasing its resistance gives a sharper and narrower response, but too low a resistance will give an unusably sharp response. The circuit might even start to oscillate. R1 attenuates the input signal to a level that gives roughly unity gain at the centre of the passband, but the exact voltage gain depends on the setting of PR1. The output can be fed to low, medium, or high impedance headphones, or a loudspeaker. Current consumption is about 15 mA.

Chapter 10

I²L

I²L is being used for mass production of LSI ICs, but little has been said about the theory behind this new technology. This article explains how it works.

INTEGRATED INJECTION LOGIC or I²L can provide serious competition to CMOS circuits where minimum current and high component packing density is required. Devices using I²L circuitry can be produced very economically and the speed of operation rivals that of TTL. This new technology is being used by some of the major semiconductor manufacturers for products ranging from microprocessors to quartz-controlled electronic watch devices. All I²L devices are large scale integration LSI products — they contain a very large number of components on a single silicon chip.

I²L was developed quite separately (in Europe) by Philips and IBM around 1972. It employs bipolar devices (that is, devices like conventional transistors rather than FETs) in circuits which have been derived from the early DCTL (Direct Coupled Transistor Logic). It is only quite recently that developments in the I²L production processes have made this circuit technique economically attractive.

A DCTL circuit is shown in Fig. 1. Three transistors are shown in each of the three NOR gates with the output of Gate 1 feeding one of the inputs of both gates 2 and 3. Other connections, which are not shown, are made to the other inputs of the gates. Circuits of this type were used in simple SSI (Small Scale Integration) devices, but suffered from the disadvantage that the current was unequally divided among the transistors in any one gate owing to minor differences in their base-emitter voltages. In addition, the load resistor had to be separated from the trans-

istors and this used up a considerable area of the chip.

Note that in the circuit of Fig. 1 there are direct connections between corresponding regions of the transistors: all of the emitters are joined together, whilst the two bases which are driven from the collectors of gate 1 are common. The current to these bases passes through the load resistor of the gate 1 circuit. In an I²L circuit, these common electrodes share the same area on the chip. A cross section through an I²L gate is shown in Fig. 2 and the circuit is shown in Fig. 3. A single pnp transistor is employed as a current source to supply current to many transistor bases without the use of a load resistor. The whole of the emitter region is a common one beneath the surface structure on the chip. This eliminates the need for surface metallisation for each separate ground connection. In addition, the area required per transistor is greatly reduced. IBM initially used the name Merged Transistor Logic (MTL) instead of I²L.

It should be noted that the pnp transistor is formed laterally along the surface of the silicon chip. The other component is a multi-collector npn transistor characteristic of I²L devices. However, this npn transistor is formed vertically in the silicon. The n-type epitaxial layer acts as the grounded emitter of the npn transistor and also as the grounded base of the lateral pnp device. The p-type base of the multi-collector transistor also serves as the collector of the pnp device. Thus the two devices do not exist as separate structures.

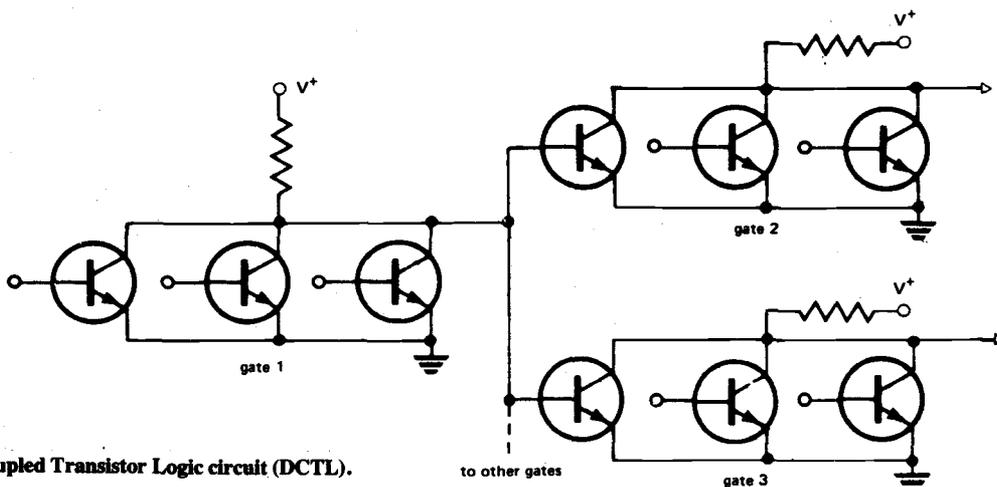
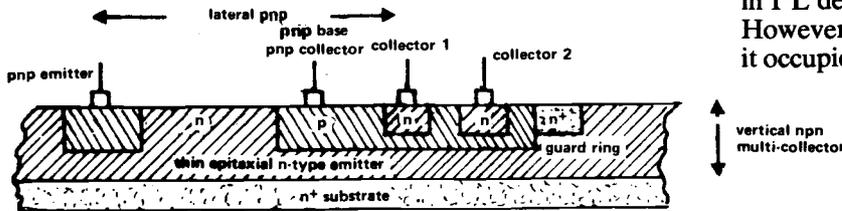


Fig. 1. A Direct Coupled Transistor Logic circuit (DCTL).

Injection

The pnp transistor 'injects' current into the base of the multi-collector transistor — hence the name Integrated Injection Logic. Current from a current source (not shown in Fig. 3) passes to the emitter of the pnp transistor and hence to the collector. Switching of the logic state occurs when this current is switched to or from the base of the multi-collector transistor.

Fig. 2. Cross section through an I²L gate.



If the input at the base of the multi-collector transistor is low (less than about +0V7), this potential will be inadequate to overcome the natural forward junction potential of the npn base-emitter junction and the npn device will be non-conducting. The injected current will flow out of the input connection to the collector of the previous circuit (not shown in Fig. 3). The multi-collector transistor outputs will therefore rise to the 'high' logic level, this voltage being determined by the collector circuitry.

If the input voltage now becomes 'high' (that is, over +0V75), the npn transistor will be biased to saturation and the output of the collector will be 'low'. This low value can be about 0V02. Thus the change of the logic level is represented by a voltage swing of around 0V7.

Power Supply

The positive power supply line of I²L circuits is connected only to the emitters of the pnp injection transistors. The base of these transistors is earthed, so the I²L circuit as viewed from the power supply line is effectively just a forward-biased silicon diode. The total power supply current is therefore the sum of the currents fed to the injection transistor emitters.

The voltage levels in I²L circuits can be very low; indeed, such circuits can operate from a supply of 0V85 upwards. The supply current per gate can be very low (about 1 nA), but the injected current can be increased in value up to about 1 mA to permit switching of the circuit at a much higher speed.

Although the I²L circuits can operate at such low voltages, the input and output circuits normally included in the same package require a higher supply voltage and their requirements normally determine the operating voltage of the whole device. A series voltage-dropping resistor is used in the power supply line of some I²L devices, whilst other devices incorporate a voltage regulator on the chip to eliminate the need for an external resistor.

The use of an internal regulator circuit also enables various injector current levels to be obtained at different points in the circuit so that each part can operate at the minimum power level for the switching speed required by that particular part. For example, the fast frequency divid-

ing circuits of a quartz controlled watch can operate at a high injection current for a satisfactory performance at 32 kHz, whereas the following frequency dividing circuits operating at a low frequency can use lower injection current levels. The increased cost of fabricating such circuits may be well worth while when current consumption must be minimised.

In many applications a single dry cell can be an ideal power source for I²L circuitry.

A guard ring of n+ material (shown in Fig. 2) is required in I²L devices to reduce cross-talk between adjacent gates. However, this ring can touch the base of the npn device and it occupies little surface area.

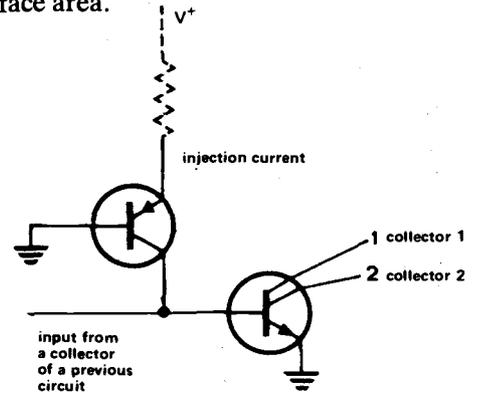


Fig. 3. The circuit represented by the I²L gate shown above in Fig. 2.

Gates

I²L gates can be made by "wire-ORing" the isolated collector outputs as shown in Fig. 4. Similarly NAND gates can be made by using the multiple collector outputs of the npn transistor connected as shown in Fig. 5.

Input/Output Circuits

I²L is almost always used in conjunction with other circuitry. The voltage change when an I²L circuit switches is only about 0V7 at current levels which may be very low. If the inputs and outputs of the I²L circuits were brought out directly to external connecting pins, any small stray noise pulses or interference picked up by the circuit would be likely to trigger the I²L circuitry, owing to its great sensitivity to low amplitude pulses.

Buffer interfacing circuits are therefore used between the input and output connections of a device and the I²L circuitry itself. A typical input buffer which can accept TTL input pulses and convert them into pulses suitable for the operation of an I²L circuit is shown in Fig. 6. The input buffer circuit used with some of the older logic systems can be even simpler.

An output buffer circuit which can amplify the low voltage pulses from the output of an I²L circuit and provide enough current and voltage to drive a TTL input is shown in Fig. 7.

Technology Comparison

An I²L gate can be made with what is effectively a single component on a chip area about one tenth of that required for a normal three-component CMOS gate. In addition, I²L is one of the most economical technologies used in device fabrication, since the number of masking and diffusion

operations on the silicon slices are less than in most comparable techniques.

One of the advantages of I²L technology is that it is so very similar to that of other standard linear and Schottky TTL manufacturing processes that it is easy to fabricate other type of component on the same chip. For example, light emitting diode driver circuits can be built on the same chip as I²L circuitry; this enables a single chip to be used to drive the display of a watch or a calculator as well as to carry out the required logic operations. Operational amplifiers, oscillators, voltage regulators, etc., can be fabricated on chips containing I²L circuitry.

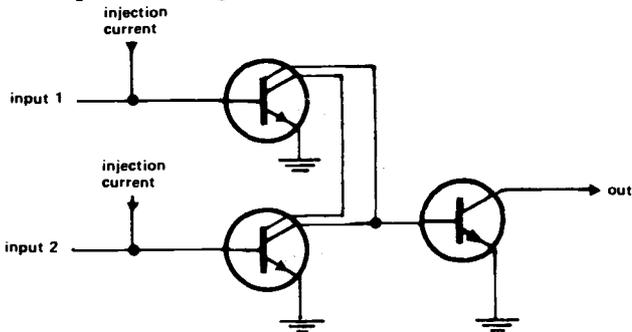


Fig. 4. (above) I²L gates can be made by 'wire-ORing' the isolated collector outputs.

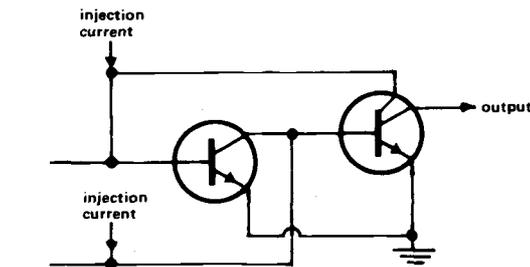
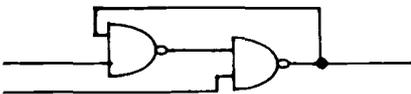


Fig. 5. (above) NAND gates can be made by using the multiple

The CMOS process is essentially suitable only for the production of purely digital devices, although simple devices such as transistors and diodes can be fabricated on the chip. In contrast, Schottky TTL devices can be combined with I²L circuits on a single chip to produce products which are faster and which have higher component densities than can be achieved in other ways. The Texas Instruments SN74S201 and SN74S301 356 bit random access memories are examples of such products.

The power consumption of I²L circuits increases linearly with the speed of operation required and in practice you can use the minimum injection current required for maximum speed at which the circuits will ever operate. CMOS circuits consume very little power in the quiescent state, but the power required increases with the switching speed. Thus no circuit adjustments or settings need be made if minimum power consumption is important and the maximum operating speed is always available. In other words, CMOS circuits always consume minimum power at low operating speeds, but have a high speed capability "on demand" whereas I²L circuits must be adjusted for low power or high speed or some intermediate value of power

Type of logic	Packing density (Gates/mm ²)	Typical Quiescent dissipation per gate	Typical Dissipation per gate at 1MHz	Logic voltage swing
I ² L	140 to 220	5 nW	100μW	0.7 V
CMOS	70-80	5 nW	150μW	Varies with supply voltage
TTL	20	10 mW	10 mW	3.5 V

Fig. 7. An output buffer which can amplify I²L pulses to feed to TTL circuitry.

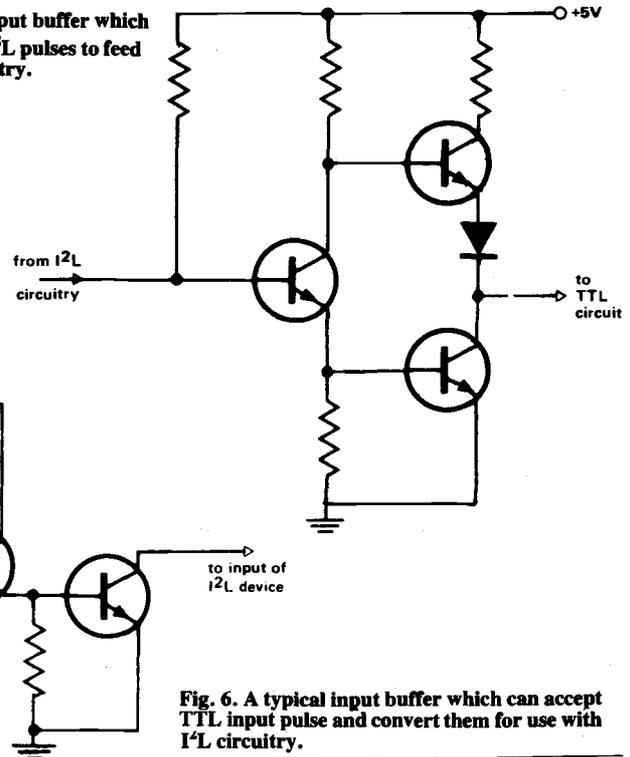


Fig. 6. A typical input buffer which can accept TTL input pulse and convert them for use with I²L circuitry.

consumption and speed.

I²L is faster than CMOS, whilst Schottky-clamped I²L is even faster still. The silicon-on-sapphire version of CMOS is another way of obtaining faster logic devices, but Emitter Coupled Logic (ECL) offers the highest speed at the expense of ease of use.

The susceptibility of I²L devices to noise pulses has already been mentioned. CMOS devices require input pulses with an amplitude of about half the supply voltage used and are therefore very resistant to spurious operation by stray noise pulses. It is difficult to see how future I²L can be fabricated without input and output buffer circuitry because of the noise problem.

A comparison between the various logic systems is given in Table 1.

Applications

I²L is employed in a wide range of applications which require large scale integration. It is unsuitable for making devices with only a few gates so it seems most unlikely that simple I²L logic devices will become available (like those one meets using CMOS and TTL technologies).

Brian Dance

Chapter 11

CMOS 555

APPLICATIONS

The result of bipolar versus CMOS in the 555 league.

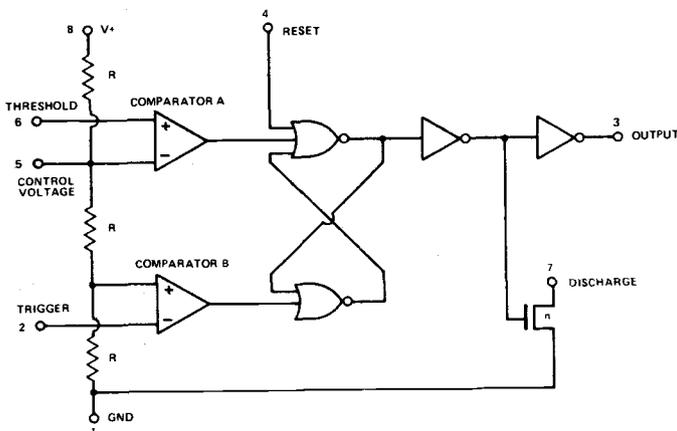
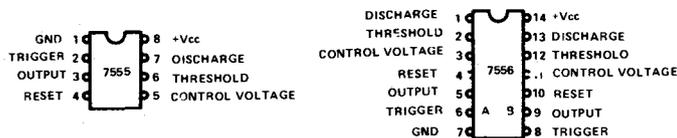


Fig. 1. The pin-out and internal configuration of the CMOS 555.

PARAMETER	ICM 7555 TYPICAL	BIPOLAR 555C TYPICAL
QUIESCENT CURRENT $V_{cc} + 15 V$	120 μA	10 mA
INPUT CURRENT	50 pA	0u5 A
TRIGGER THRESHOLD	50 pA	0u1 A
RESET	100 pA	0m1 A
MAX. OPERATING 500 kHz	FREQUENCY	500 kHz
4 VS \rightarrow 16 V	POWER SUPPLY RANGE	2 \rightarrow 18 V
370 mA	PEAK SUPPLY CURRENT	10 mA
100 nS	TRANSIENT RISE AND FALL TIME AT OUTPUT	40 nS

Fig. 2. A comparison between the Bipolar and CMOS version of the 555.

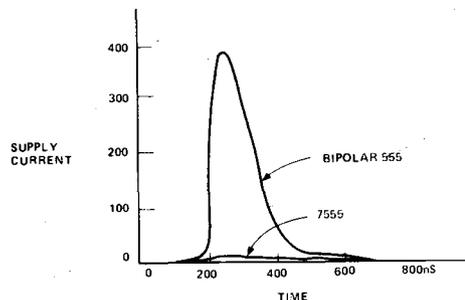


Fig. 3. The CMOS 555 displays an impressive reduction in supply current transient during an output transmission.

THE BIPOLAR 555 TIMER CHIP has been around for many years, but there is also a CMOS version that has some very significant design improvements. The two devices are functionally very similar, being interchangeable in most applications.

The operation of the 555 is very simple (Fig. 1). It consists of a pair of comparators that operate at $\frac{1}{3}$ and $\frac{2}{3}$ of the supply voltage, this being set up by a resistor chain. These comparators set and reset a flip-flop which in turn drives the output stage. A second output is available which is an electronic switch (Discharge) to ground. Other features include access to the resistor chain via the control voltage pin and an extra reset input to the flip-flop.

This simple network readily lends itself to all sorts of oscillators and timer circuits.

The bipolar 555 has a few parameters that can make it difficult to use, but which have been improved in the CMOS version (Fig. 2). The bipolar quiescent supply current is generally about 10 mA which negates their use in small battery units. The CMOS version consumes a mere 120 μA .

Also the CMOS inputs are very high impedance having input currents down in the pico amp region. Another major improvement is the reduction in the power supply current transient during an output transmission. The bipolar is very noisy in this respect and can often be the cause of lots of 'funnies' in nearby circuits.

The CMOS 555 is a low power, high input impedance, device that should be used where low current consumption is at a premium. The following circuits illustrate some possible uses of the device:

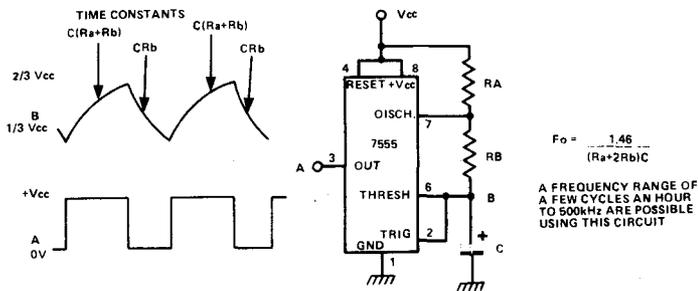


Fig. 4. (above) A simple oscillator can be constructed using two resistors and a capacitor. Due to the high input impedance of the CMOS device, resistor values up to 100 M may be used. The operation is as follows: Capacitor C is charged up via Ra and Rb and so rises with a time constant of C(Ra + Rb). When the voltage B reaches 2/3 Vcc, the threshold hold comparator goes high causing the output (pin 3) to set low. Also the discharge FET (pin 7) is turned on. This discharges the capacitor via Rb with a time constant of CRb, until the voltage B reaches 1/3 Vcc.

This causes the trigger comparator to go low which sets the output high and turns off the discharge FET. Thus, the voltage B oscillates between 1/3 and 2/3 Vcc. The waveform is asymmetric but due to the nature of its generation its frequency is virtually invariant with regards to supply voltage changes. It is possible to generate a sawtooth waveform by reducing Rb to a short circuit. This causes the reset time to be very fast, of the order of a few microseconds.

However, there is a propagation delay through the device from the trigger comparator to the output which causes the discharging waveform to overshoot the 1/3 Vcc limit, thus making the waveform at B larger. This will cause the oscillation frequency to be lower than calculated. To maintain the calculated frequency, the discharge period should be 5 uS seconds or longer.

$$f_o = \frac{1.46}{(R_a + 2R_b)C}$$

A FREQUENCY RANGE OF A FEW CYCLES AN HOUR TO 500kHz ARE POSSIBLE USING THIS CIRCUIT

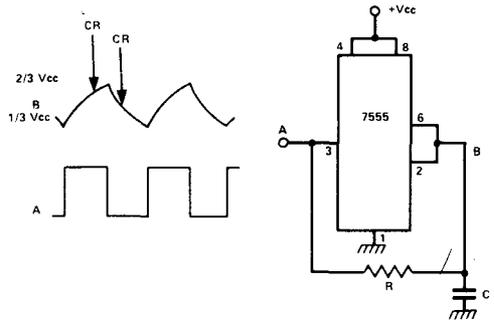


Fig. 5. (above) This oscillator has a symmetrical output because the charge and discharge paths are the same and the portion of the exponential curve that is used is symmetrical. Note that in this circuit, the discharge pin (7) is available to do other jobs, such as drive a LED or some other device. The timing resistor R should be kept relatively high (above 10k) to prevent loading of the output.

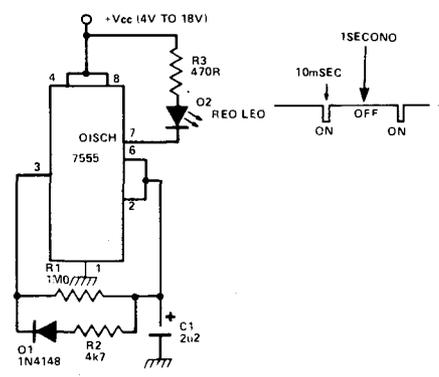
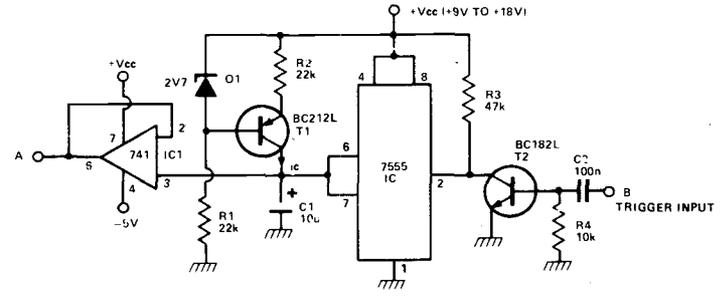


Fig. 6. (above) This circuit is an oscillator that has a wide mark to space ratio. It is OFF for approximately 1 second and then turns ON for about 10 mS. During this latter period the LED is turned on by the discharge FET. The long OFF period is generated by the R1, C1 time constant, whereas the

short ON period is produced by D1 (which is forward biased) and R2, C1. The average current consumption is relatively low. If the unit were powered from a 9 V battery, then the current would be 120 uA for the ICM 7555 and an average of 140 uA for the LED, making 260 uA total. This would give a lifetime of a few months for a PP3 which would be extended by lengthening the OFF period (increase R1) and reducing the LED current (increase R3).



$$\text{SWEEP TIME } T = \frac{V_{cc} \times 2/3 \times C1}{I_c}$$

$$\text{AND } I_c = \frac{(2.7 - 0.7)}{R2}$$

Fig. 7. (above) The 7555 is used to initiate and terminate a triggered sweep. Normally the discharge FET (pin 7) is ON and so C1 is shorted to ground. When a trigger is applied to the input, the collector of Q2 momentarily goes low which sets pin 7 of the 7555 in its OFF condition. Q1, R1, R2 and D1 form a current generator that drives C1. Once the discharge FET has been turned OFF, the voltage on C1 rises linearly. When this voltage reaches +2/3 Vcc, the threshold comparator sets the discharge FET into its ON state and so C1 is shorted to ground. IC1 is used to buffer the voltage on C1. The sweep generator is not retriggerable and is only initiated on fast positive going inputs. To vary the sweep rate, alter C1 and/or R2.

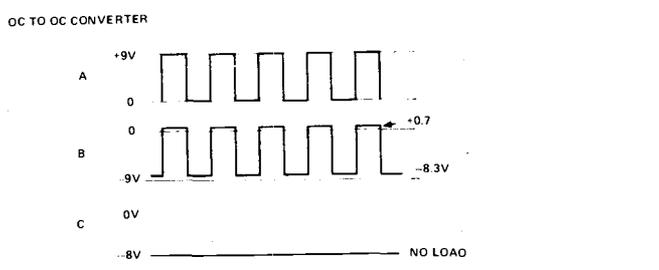
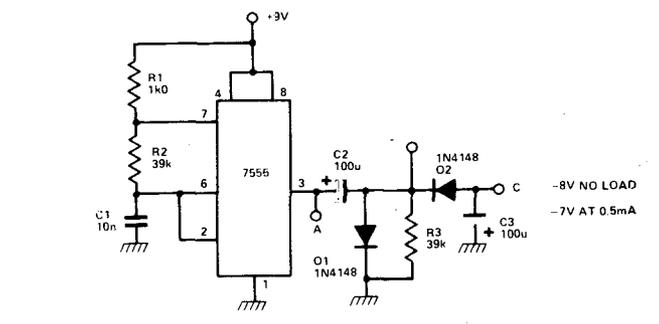


Fig. 8. (above) A DC to DC converter can be constructed from an oscillator and a diode charge pump. The 7555 forms a high frequency square wave oscillator. The squarewave from pin 3 is AC coupled via C2 to the charge pump. The voltage on the negative side of C2 is prevented from going more than 0V7 positive by D1 and so the squarewave on this side of the capacitor biases itself so that it moves from +0V7 to -8V3. D2 charges up C3 on the negative excursion of this waveform and so a negative rail of about -8 V is generated. The current that can be taken from this rail is rather low, being determined by the oscillation frequency and C2. Generally DC to DC converters have a poor transfer efficiency.

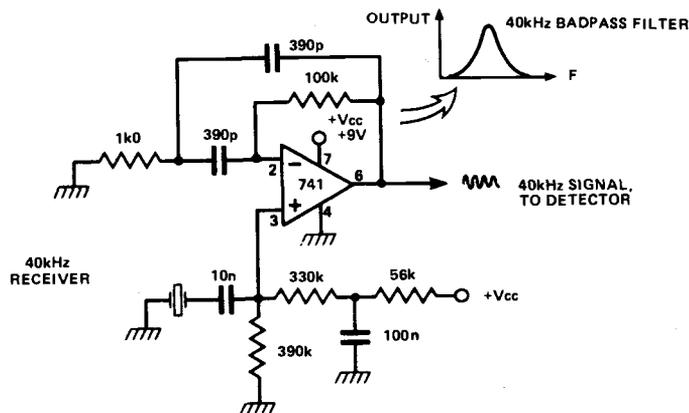
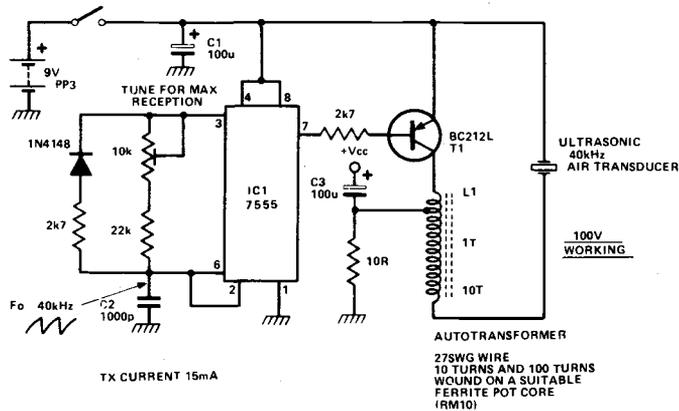


Fig. 9. (above) The 7555 can be used as the driving oscillator in an ultrasonic remote control system. The oscillator generates a thin pulse about 2.5 μ s long at the natural resonant frequency of the transducer. This short pulse is used to turn on a transistor (Q1) which drives an auto transformer with a 10 to 1 step up ratio. The output of the transformer is connected to the transducer and when the oscillation frequency is correct a 100 V peak to peak sine wave will be produced at this point. The transducer is usually a crystal with a high impedance and so a high operating voltage is required to produce any power output. The receiver is a 40 kHz bandpass filter. This will amplify any audio signals at this frequency, which can then be sent to a detector circuit.

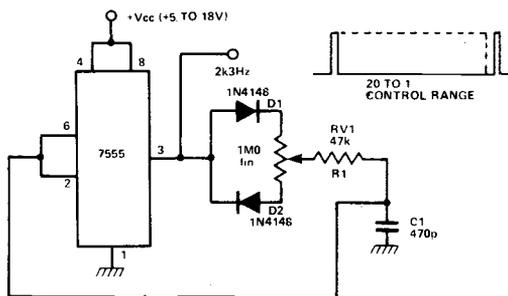
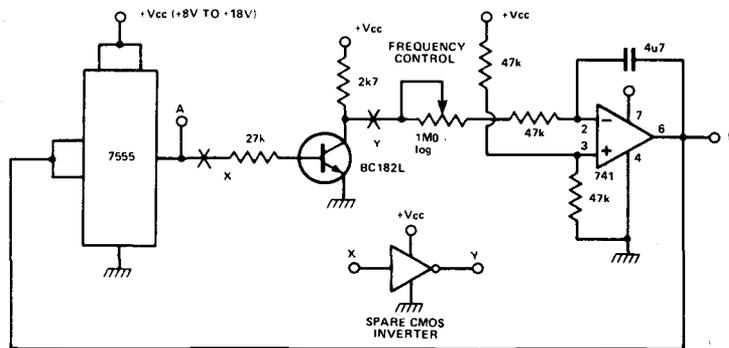


Fig. 10. (above) This oscillator allows the mark space ratio at pin 3 to be varied from 1 to 20, to 20 to 1, by using two feedback routes. When pin 3 is high, C1 is charged via D1, part of RV1 and R1. When it is low, C1 is charged via D2, the other part of RV1 and R1. Thus the position of the RV1 wiper determines the ratio of the charge and discharge periods. The oscillation frequency is slightly dependent on this ratio.



TO INDEPENDANT OF VCC



Fig. 11. (above) By making a loop out of a 7555, an inverter and an integrator, a triangle/squarewave oscillator is produced. To operate well at high frequencies (up to 40 kHz) a CMOS inverter should be used to replace the transistor inverter. The op-amp provides a low impedance triangle output, the frequency of which may be controlled with the 1M log pot.

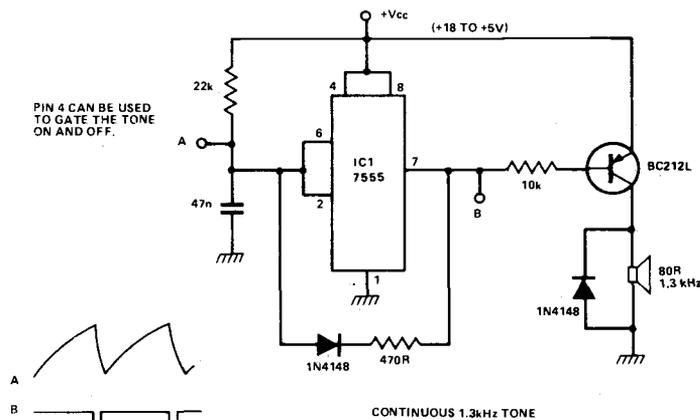


Fig. 12. (above) The 7555 can be used to generate an acoustic tone. The oscillator is set to run at 1.3 kHz which has a low period of about 15 ns and a high period of about 75 ns. During the low period the transistor is turned ON and so the loudspeaker is connected across the power supply and sinks at about 100 mA (for a 9 V supply). This gives it a 'kick' on every cycle of the oscillation. As the transistor is only on for 15 out of every 770 ns, the average current through the speaker is quite small - about 1.95 mA. Therefore, the total current consumed by the whole system is only about 2.5 mA (at 9 V), and yet the 20 mW output signal is quite audible.

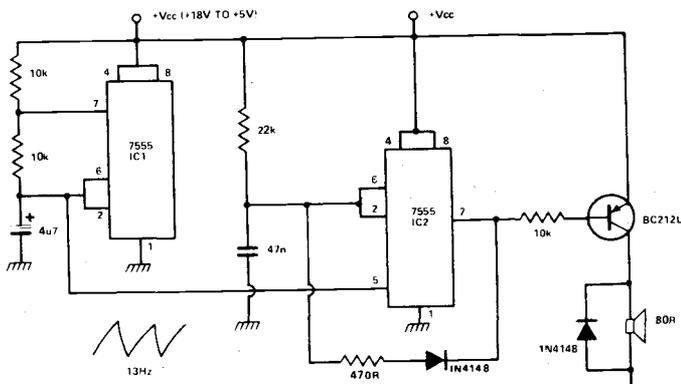


Fig. 13. A warbling tone can be generated by using two oscillators. The warble is produced by IC1 which generates a 13 Hz wave form that is used to frequency modulate the tone generator as described in the previous example. Pin 5 of a 7555 is connected to the $+2/3 V_{cc}$ tap on the resistor ladder. By tying it to a 'warble' waveform, frequency modulation of the final output tone is produced. A 7556 could be used instead of two 7555's.

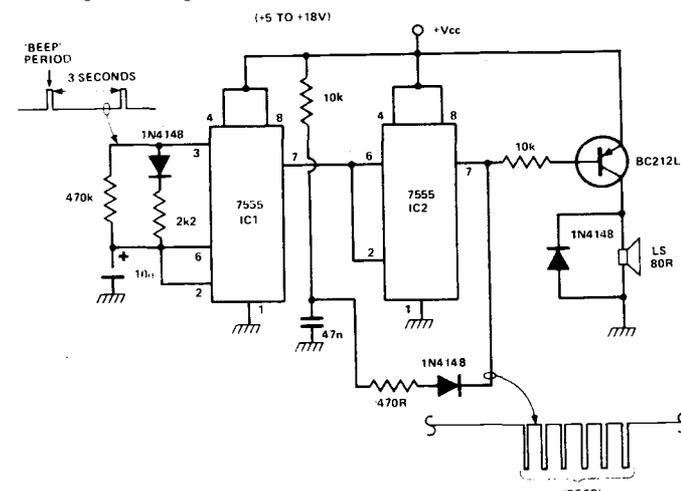


Fig. 14. (above) The police and other emergency services use a repeating high frequency 'beep' on their radio networks. This doesn't interfere with the normal radio traffic and allows the listener to be certain that he is still tuned in correctly to that channel. The circuit generates a similar 'beep' and yet consumes only a couple of milliamps. IC1 is a slow oscillator (3 second period) with a large mark/space ratio. The discharge FET is on for most of the time and only goes OFF for about 15 milliseconds in every 3 seconds. This FET is connected to the tone generator in such a manner that when the FET is ON the tone generator is inhibited. When the FET goes OFF the generator produces a burst of 3 kHz oscillations which are heard as a 'beep'.

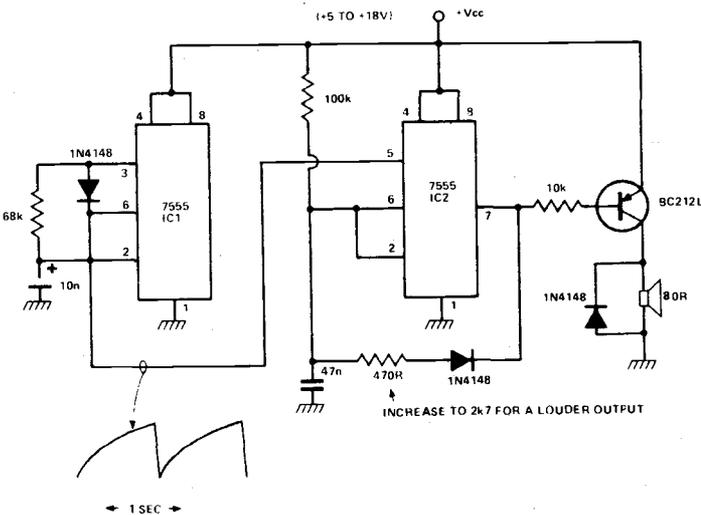


Fig. 15. (left) The last type of sound generator to be described is a simple siren. IC1 generates a sawtooth waveform which is used to frequency modulate, via pin 5, the tone generator (IC2). As the sawtooth voltage rises (with a period of 1 S) so does the tone generator frequency.

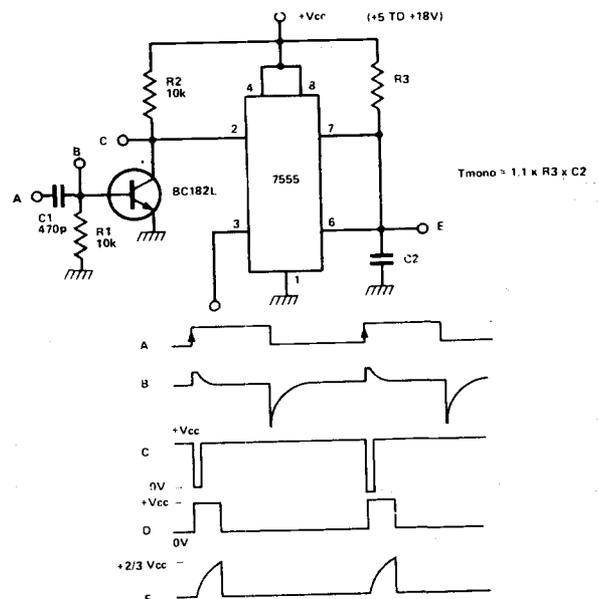


Fig. 16. (above) The 7555 can be made into a monostable, although some problems may occur in its use. A negative going pulse on the trigger input (pin 2) can be used to start the monostable period. It is important that this pulse goes high again before the end of the monostable period, or else it may prolong the period. To this end an AC coupled transistor inverter has been used so that a rising positive signal will initiate the event. Initially C2 is discharged to ground. When pin 2 is taken low, the discharge FET is set to be OFF and so the voltage at E rises with a time constant of C2, R3. When this voltage reaches $+2/3 V_{cc}$, the discharge FET is turned ON. C2 is discharged to ground and the monostable period is finished. During this period the 7555 produces a high output at pin 3.

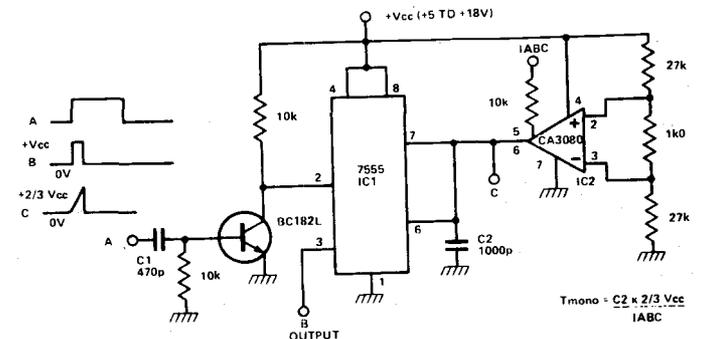


Fig. 17. (above) The previous circuit has been modified. The timing resistor has been replaced with a programmed current source, IC2. Whatever current is put into pin 5 of the CA 3080 (the I_{ABC} current) will appear at its output. This will linearly charge up C2 when the FET switch is turned OFF. The monostable action will be the same as in the previous example. The monostable period is linearly proportional to the I_{ABC} current so by programming this current the period is controlled.

Fig. 15. (right) The last type of sound generator to be described is a simple siren. IC1 generates a sawtooth waveform which is used to frequency modulate, via pin 5, the tone generator (IC2). As the sawtooth voltage rises (with a period of 1 S) so does the tone generator frequency.

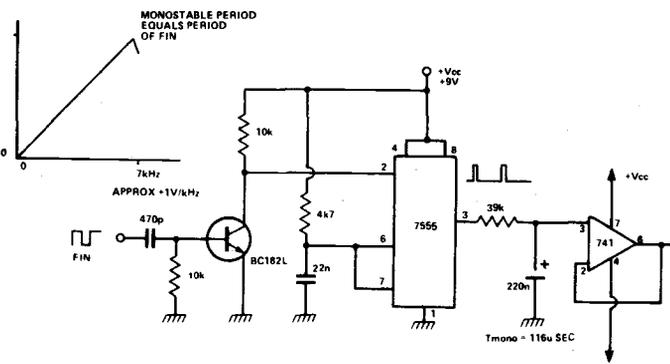
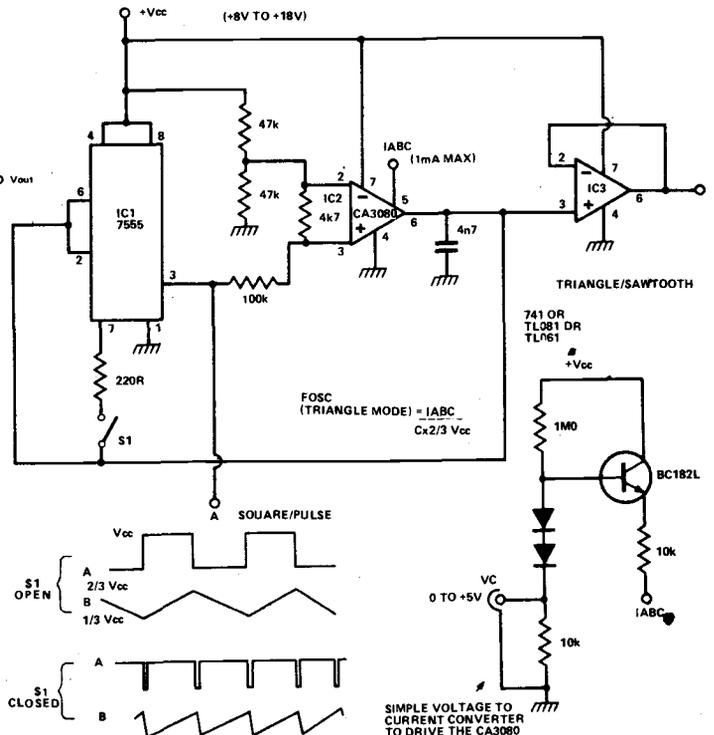


Fig. 18. (above) The monostable can be used to linearly convert a frequency into a voltage. The pulses at the output pin of the 7555 in this circuit are fixed in length but occur at the fundamental frequency of the input signal. Thus the average equivalent DC voltage of these pulses will be linearly proportional to their frequency. This averaging can be performed very simply with a CR low pass filter. This filter determines the response time of the circuit and the ripple. A long constant will have little ripple and respond slowly and vice versa. Care must be taken to not exceed the range of the monostable. When the period of monostable exceeds that of the input signal, the circuit will miss every other period and will drop its apparent output by an octave.

Fig. 19. (right) IC1 and 2 form a triangle/squarewave oscillator. IC2 is a non-inverting, programmable rate integrator and its output ramps up and down between the $\frac{1}{3}$ and $\frac{2}{3}$ V_{CC} limits set by IC1. The rate at which the integrator ramps up and down hence the oscillation frequency, is determined by the I_{ABC} current. Because the input impedance of IC1 is so high, it is possible to directly connect the timing capacitor to it, without any unwanted loading effects. This circuit has excellent high frequency performance producing good quality triangle wave forms at 40 kHz. The circuit can also produce very low frequency signals by making C a 100nF tantalum and I_{ABC} a current of say, 1 nA. This oscillator would then have a period of 800 seconds. IC3 is used to buffer the triangle to the outside world. If a 741 is used, then the waveform will become asymmetrical at low I_{ABC} currents (below 1 uA) due to the input bias current needed to run a 741. A TL081 has very little input current and so could be used for both low I_{ABC} currents and high frequency performance. If low power is needed,



then a TL061 (200 uA quiescent) could be used. By closing switch S1, the oscillator will produce a sawtooth waveform and a pulse.

Tim Orr

SPOT DESIGNS

Simple Preamplifier

THIS PREAMPLIFIER has two inputs, one for a magnetic cartridge and the other is an "aux" input for a tuner, tape deck, etc. Although the circuit is very simple, it uses an IC which is specifically designed for this application and provides low levels of noise and distortion. The unit is suitable for stereo operation and both the required amplifiers are contained within a single LM382 IC.

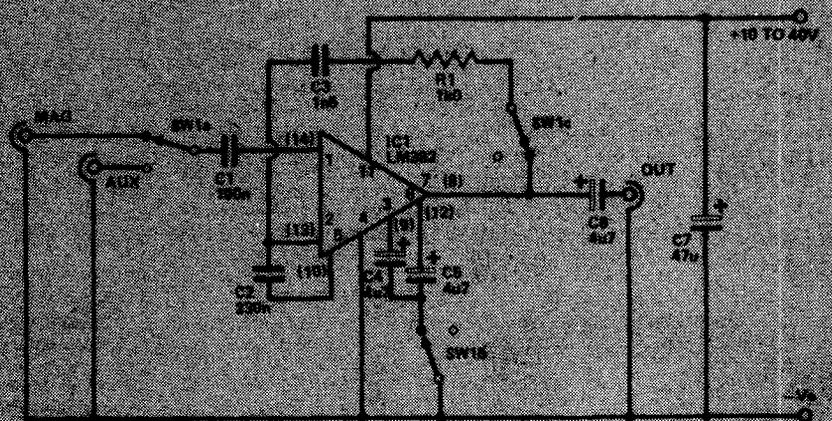
The circuit diagram is for one channel only, but apart from the IC pin connections the other channel is identical. The numbers in brackets show the pin connections for the other channel. The supply connections of IC1 are common to both channels.

The LM382 has an internal biasing circuit which sets the quiescent output voltage at approximately 6 V and no discrete biasing components are required. C6 provides DC blocking at the output. When switched to the "Mag" mode, external feedback components are required in order to shape the frequency response characteristic of the amplifier in the required way. Bass cut and treble boost are applied to the signals transferred onto

records so as to prevent excessive low frequency groove modulations and give an improved signal to noise ratio. The preamplifier must give corresponding bass boost and treble cut in order to give a flat overall frequency response to the system. C2, C3 and R1 are the discrete feedback components and the LM382 itself contains some feedback resistors. C4 and C5 provide DC blocking for two shunt resistors in the feedback network.

When switched to the "aux" mode, most of the feedback components are not required and are switched out of circuit by SW1a and SW1c. C2 is left in circuit, but is superfluous. In this mode the circuit has a voltage gain of only about four and is really just operating as a buffer stage. SW1a connects the input of the amplifier to the appropriate input socket and C1 provides DC blocking at the input. Of course the input wiring must all be screened to prevent stray pick-up of mains hum, etc.

The current consumption of the circuit is about 12.5 mA. Due to the high supply ripple rejection of the LM382, it is not necessary to have a highly smoothed and decoupled supply.



Chapter 12

TV PRINCIPLES

Ever wondered just how your TV actually works – all those cunningly interconnected and interrelated bits of high-voltage circuitry? Stay tuned for enlightenment.

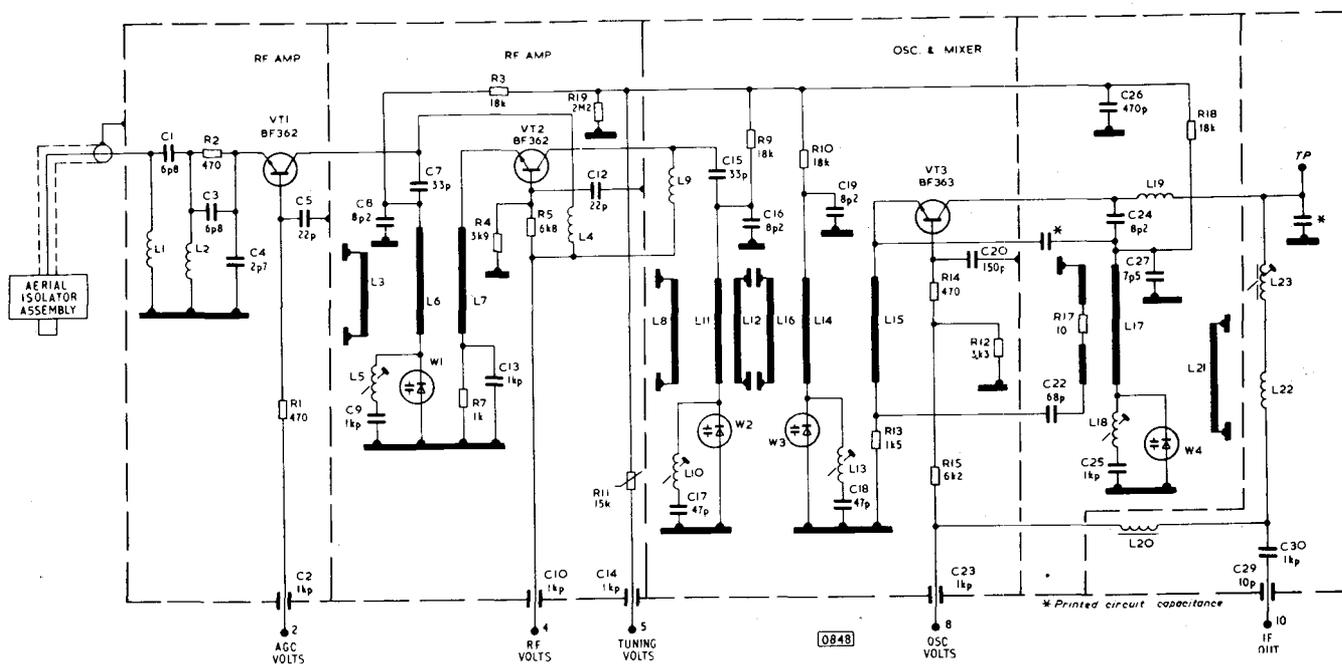


Fig 1. Circuit diagram of UHF varicap tuner, which uses two RF amplifiers and a mixer stage. Resonant lines tuned by capacitor diodes select the required channel and provide the necessary front-end selectivity.

THIS ARTICLE looks at monochrome television based on a mains/battery chassis from Thorn Consumer Electronics. In addition to producing an insight into modern television technology, the article also gives a fair impression of how the picture is developed on the screen of the picture tube. The basic principles are common to all receivers except that for the reception of colour there are circuit additions for the decoding of the colour information (and a tricolour tube for display!)

Sound and vision signals are modulated on to two carrier waves, the former using frequency-modulation (FM) and the latter, amplitude-modulation (AM). On the prevailing UK 625-line system the signals are transmitted in Bands IV and V which are located in the UHF spectrum. Each channel occupies a width of 8 MHz with the sound carrier being 6 MHz above the vision carrier. For example, Channel 21 has sound and vision frequencies of 477.25 and 471.25 MHz respectively, while the frequencies for Channel 68 are 853.25 and 847.25 MHz.

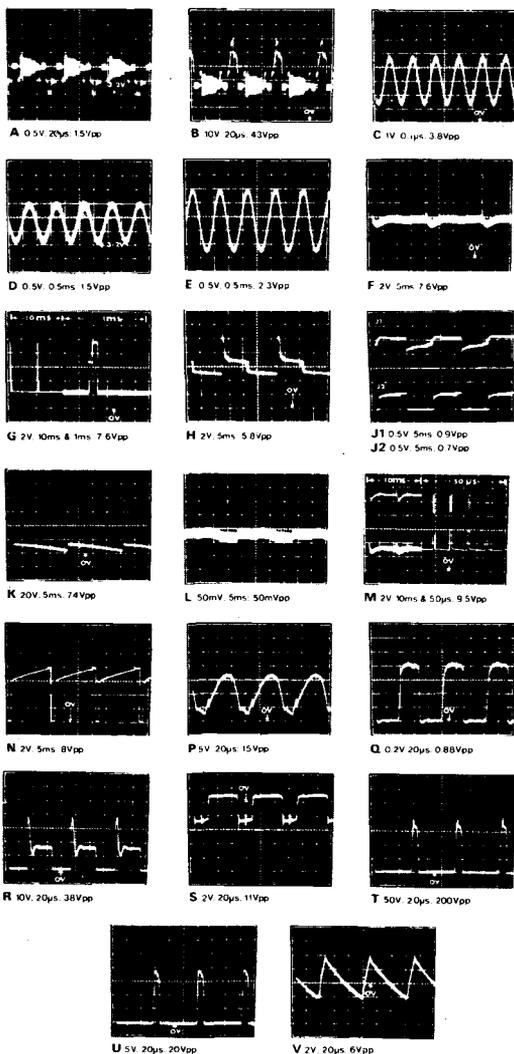
Vision modulation is negative-going (See Fig. 3), and is transmitted in 5.5 MHz upper sideband and 1.25 MHz lower sideband. Peak FM deviation is 50 kHz (as distinct

from 75 kHz on FM sound radio) based on 50 μ S pre-emphasis. Ratio of peak vision to peak sound power is 5.1. Further information on the signal is given later.

Tuner-Front-End

The start of any television receiver is the 'front-end' or tuner (Fig 1), whose job it is to select the required channel and to convert the sound and vision carriers to lower frequency ones for subsequent intermediate-frequency (IF) amplification and response tailoring. In Fig. 1, the aerial signals are coupled to an aperiodic RF amplifier, VT1, through an 'isolator' for preventing spurious mains voltages in the receiver from reaching the aerial at lethal power! The transistor is in common-base mode so that the input is applied to the low-impedance emitter. Further input matching is provided by the emitter components and the base is biased either from a constant potential or from an AGC potential (see later).

VT2 is a tuned RF amplifier, also in common-base mode, but the tuning is by resonant lines rather than coils. Any transmission line whose length is adjusted to correspond to



Oscillograms

These were taken from a typical receiver at the points indicated by corresponding letters in the circuit diagram. The voltage and time figures refer to the sensitivity per division of the graticule. The receiver was set up for normal reception (test card with tone on sound) and the oscillograms were taken via a +10 probe having an input capacitance of 12pF in parallel with 10MΩ. The mixed mode timebase facility was used for G and M.

a tuned frequency is the equivalent of a tuned LC circuit. An open-circuit line is resonant at 1/2, 3/2, 5/2, etc. wavelength. Excluding velocity factor, the physical length of a line for, say, Channel 33 would be around 280 mm. Happily, it is possible to reduce the physical length while retaining the required electrical length by cutting off the ends of the line and replacing them with capacitance, which reduces the physical length to about 50 mm. Moreover, tuning the channels then become a question of varying the capacitance at one end.

Looking at line L6 in Fig. 1 shows that the bottom connects to varicap W1 and the top to C8 and VT1 collector capacitance. A varicap is essentially a junction diode. As the reverse bias is increased so the depletion region widens, and as this constitutes the dielectric between the n and p regions. The effect is tantamount to the two plates of a

capacitor being moved away from each other, with a consequent reduction in capacitance. The four varicaps in Fig. 1 are biased by a positive potential being applied to the 'tuning volts' input. The potential is obtained from a stabilised (by IC1) supply in the main chassis (Fig. 2) via tuning potentiometer R39. Thus as this control is tuned so the resonance frequency of the lines alter in step and tune over the UHF channels.

The second RF amplifier stage VT2 starts to give selectivity. Emitter coupling is via low impedance aperiodic line L7. Further selectivity is provided by the bandpass coupling between VT2 collector and VT3 emitter formed by lines L11, L12, L16 and L14, tuned by varicaps W2 and W3. Common-base VT3 uses collector/emitter feedback for the local oscillator tuned by line L17 and varicap W4. Line L15 couples the RF signal to the oscillator/mixer stage. The circuits are trimmed by L5, L10, L13 and L18 (so they all tune in step), while the closed lines L3, L8 and L21 also assist with the tuning and matching.

The oscillator is arranged to operate at the IF frequency above the input frequency, and additive mixing yields the IF output, which is resonated by L23 and associated components. The IF signal is coupled to the IF input of Fig. 2 via C30. The high degree of selectivity minimises spurious responses such as image, IF, repeat spot, etc., while also providing a good 3rd-order intermodulation rejection ratio. This is further aided by the nature of the transistor and design of the first stage VT 1.

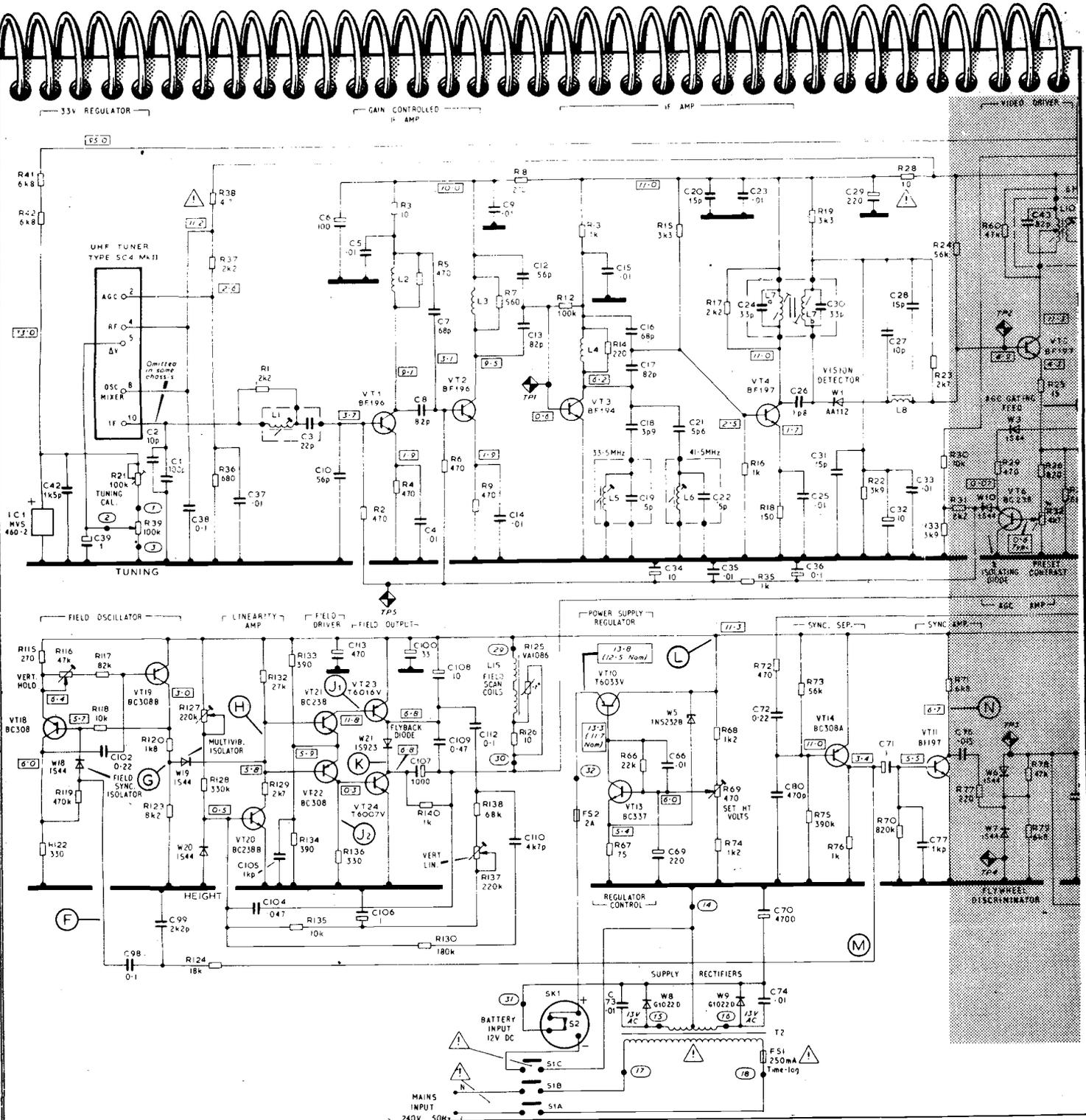
The circuit also reveals various signal coupling, decoupling and isolating components, which are essential for the stable performance of this important part of the receiver. The tuner is built into a fully screened box with feed-through capacitors for the inputs and outputs.

IF Channel

Sound and vision signals of the selected channel undergo amplification with band pass and selectivity tailoring in the IF channel comprising VT1/2/3/4. Tuner signal is applied to VT1 base from the tuned coupling L1/C3, and the amplified and bandpass defined output is yielded by transformer L7a/b. Gain is controlled automatically (AGC) to suit the level of the input signal by a bias fed to the bases of VT1 and VT2. The four stages are each in common-emitter mode, and impedance matching at the couplings is achieved essentially by capacitor divide-down.

The bandpass characteristic is provided in the main by L1/C1/C3/C10/R1 at the input and by a L7a/b at the output. Additional selectivity is provided by collector inductor L2/L3/L4, while sound and adjacent channel sound rejections are introduced at 33.5 MHz by L5/C18/C19 MHz and at 41.5 MHz by L6/C21/C22.

With the 625 line system (system 'I' is used in the UK) the sound carrier is 6 MHz above the vision carrier, but because the local oscillator of the tuner is working at IF above the signal frequencies, the IF appears at 33.5 MHz for sound, which is 6 MHz below the 39.5 MHz vision IF. The sound and vision signals are handled simultaneously by the IF channel, which is possible because frequency modulation (FM) is used for the sound signal. Vision bandwidth of the 'I' system is 5.5 MHz upper sideband, accommodated by the IF bandwidth, and overall channel width 8 MHz.



Vision Detector

Sound and vision signals from L7b are coupled to vision detector W1, which yields a changing amplitude output corresponding to the picture information (Fig. 3) and also an output at 6 MHz resulting from intermodulation of the sound and vision signals by the diode nonlinearity, the difference frequency of the two signals being 6 MHz. The intercarrier sound signal (as it is called) retains the FM of the sound signals because this is one of the components from which it is derived.

If the ratio of the levels of the sound and vision signals is incorrect a buzz occurs on sound — called intercarrier buzz. Hence the reason for the 33.5 MHz trap, which sets the sound signal level below that of the vision carrier while helping to establish one side of the bandpass. The 41.5

MHz trap avoids the sound signal from the next channel causing interference while helping to establish the other side of the bandpass. The vision carrier is set 6 dB down the response to equalise for the single side band signal.

Video Channel

Picture and intercarrier signals from W1 are directly coupled to the base of the video driver VT5 via low-pass filter L8/C27/C28, which removes residual IF signal. VT5 collector is loaded into transformer L10 which tunes the 6 MHz intercarrier signal and couples it to the sound section for FM demodulation and subsequent pre and power amplification for driving the loudspeaker.

VT5 also serves as an emitter-follower for the video signal with network R26/R27/R32 as the load. The signal

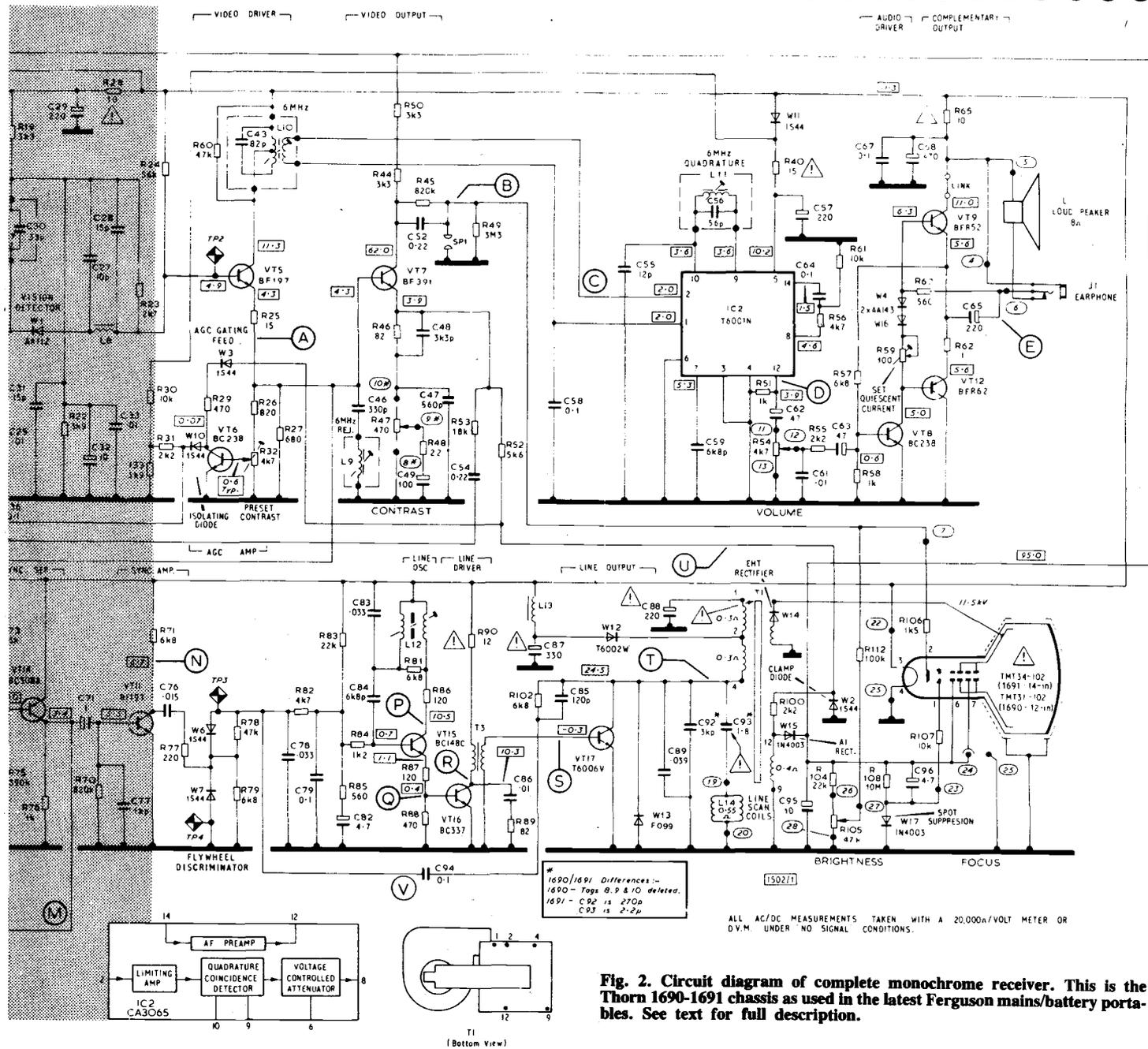
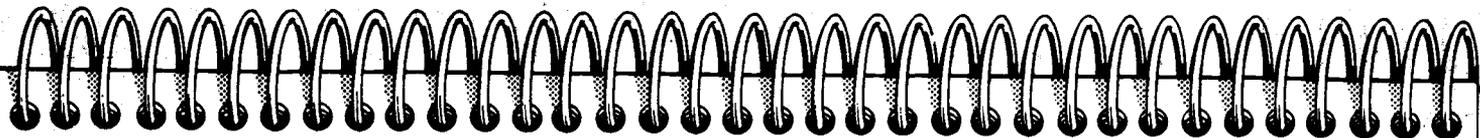


Fig. 2. Circuit diagram of complete monochrome receiver. This is the Thorn 1690-1691 chassis as used in the latest Ferguson mains/battery portables. See text for full description.

across this is directly coupled to the base of the video output transistor VT7, which feeds negative-going picture signals to the cathode of the picture tube from its collector. A series rejector L9/C46 tuned to 6 MHz is also active at VT7 base to prevent intercarrier signal from getting into the video output stage, where it would cause picture interference. The level of video signal reaching the tube is adjustable by R47, the contrast control, which is a kind of current feed-back control working by the progressive shunting effect across R47 emitter resistor by R48. C49 is a DC isolator. Video-frequency compensation is also provided by capacitors in the feedback loop.

VT5 base is biased from a resistive divider complex (R24/R33/R22/etc.) from the supply rail. It is also partly biased from rectified IF signal at W1 anode, and since

direct-coupling is used an increase in IF signal level results in a reduction in positive bias at VT5 base and hence a fall in potential across VT5 emitter load.

The voltage across R32 (the preset contract control part of the load) is fed to the base of the AGC amplifier VT6 at a level established by the setting of the control. Because VT6 collector is energised via W3 from positive-going 5 Vpp pulses derived from a winding on the line output transformer (bottom right-hand corner of Fig. 2, next to the picture tube), the transistor conducts only during the line sync pulses when there is no picture content which the AGC circuit might otherwise falsely read. The degree of conduction and hence the level of the collector potential are determined by the DC level of the line sync pulses at VT6 base. This is called line-gated AGC.

Thus with increase in input signal level (such as when tuning to a strong channel) VT6 is turned down and the positive potential at its collector rises. This is reflected via forward conducting W 10 to the bases of VT1 and VT2 by way of R2/R6 and the filter consisting of C34/C35/C36/R35, which removes line pulses. The small-signal transistors VT1 and VT2 are the type designed for forward AGC; that is, increased gain reduction resulting from positive-going AGC potential.

The preset contract control R32 sets the operating range of the AGC. With a test card signal of average strength the control is adjusted for 1.5 Vpp picture plus sync signal at VT5 base.

Some sets include delayed AGC for the tuner RF amplifier which comes into effect after the gain has been reduced initially on a strong signal by the IF AGC; but for the monochrome portable this is barely necessary as maximum front-end gain is generally necessary for most of the time for the best signal-to-noise ratio when a simple set-top aerial is utilised. It will be seen that the tuner 'block' in Fig. 2 has an AGC input which, in this model, is terminated to a supply potential-divider.

Field Timebase

The electron beam needs to be deflected both vertically and horizontally to build up the raster upon which the picture appears. The vertical deflection is handled by the field timebase which deflects the beam from the top to the bottom (scanning stroke) and then very swiftly back to the top again (retrace) at 50 Hz repetition rate.

This is achieved by a 50 Hz sawtooth current passing through the field scan coils (L15) on the tube neck. The oscillatory requirements are provided by the field oscillator VT18/19, which is an RC multivibrator. The retrace is initiated by the arrival of a field sync pulse at VT18 base (see later), while the repetition rate is determined by the vertical hold control R116 with R117/118 and C102.

Consider the circuit during the scanning stroke when a rising voltage (ramp) occurs at the base of high-gain amplifier VT20 owing to C104 charging through R127/128. This turns on VT20, VT22 and VT24, and turns off VT21 and VT23. At the conclusion of the stroke VT24 is fully 'bottomed', at which time a positive-going pulse from VT19 collector 'hits' the bases of VT21 and VT22 via the multivibrator isolating diode W19. The pulse is initiated from the field sync action. The retrace is thus triggered by VT21 and VT23 tuning on, and VT22 and VT24 turning off.

During the retrace, VT24 collector voltage rises at a rate established by the L/R ratio of the scan coils, and when the supply line voltage is exceeded W21 goes into reverse condition and VT23 is isolated. The rate of rise is then defined by C109. After a peak, the retrace voltage falls until W21 goes into forward conduction again. This allows the remainder of the retrace energy to be fed back into the supply line, after which the scanning stroke recommences.

The resulting rise in current through the field scan coils during the scanning stroke produces a magnetic field such that the electron beam is drawn downwards. To avoid vertical non-linearity to the display the *rate of change of current* must be linear. Owing to resistive losses in the scan coils and circuit non-linearities, a slight correction to the

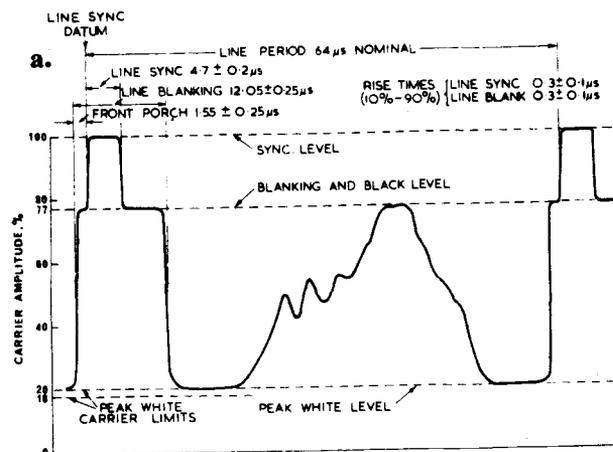
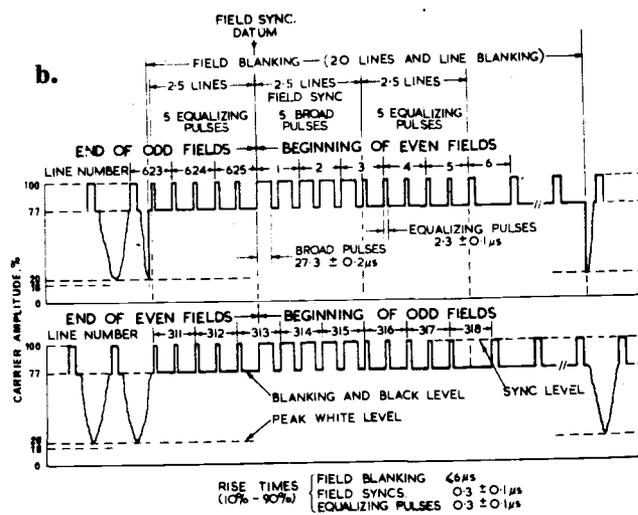


Fig 3. BBC 625-line television signals. (a) One line of signal showing sync pulses. These keep the line scan in step with that at the transmitter, while the picture signal causes the deflected scanning spot on the face of the picture tube to change in brightness at a rate determined by the detail of the transmitted picture and by an amount governed by the brightness of the transmitted scene at any instant. (b) Pulses transmitted during the synchronising period at the end of one field scan and the start of the next (upper end of odd fields and beginning of even ones). The pulses provide correct interlacing while keeping the line timebase in sync during the field synchronising period (see text).



current waveform is required, and this is achieved by a parabola waveform produced by R138/R137/C106 being added to the ramp via the linearity amplifier VT20. The degree of correction is adjustable by the vertical linearity control R137.

When the retrace is initiated, the rapid reversal of scan coil current deflects the beam swiftly upwards to start a new downward scan, and during the retrace diode W20 goes hard into forward conduction so that the base of VT20 is clamped to earth.

Line Timebase

Horizontal deflection of the beam is achieved by the line timebase driving a sawtooth current wave through the line scan coils (L14) during the scanning stroke. Deflection is from left to right, and at the end of the scanning stroke a swift reversal of current deflects the beam back to its starting point again. During the retrace a considerable amount of energy stored in the inductive elements of the line output stage is released to provide the extra high tension (EHT) for the final anode and the high voltage for the first anode (A1) of the picture tube. Boosted voltage is also used to energise the line output transistor VT17 once the line oscillator has started.

Line repetition rate of the 625 line system is 15625 Hz. Thus the horizontal rate is significantly greater than the vertical rate. We have seen that in the UK the vertical rate is 50 Hz. This means, then, that a raster of $312\frac{1}{2}$ lines is produced ($15\ 625/50$). For a complete picture there are two vertical scans, each producing a raster of $312\frac{1}{2}$ lines, so that the complete picture is made up of 615 lines and produced every twenty-fifth of a second (in actual fact not all the lines are used for the picture as some occur during the field sync period when the electron beam is cut off).

A complete full-line picture is achieved because the scanning lines of one field *interlace* in the spaces between the lines of the partnering field. To obtain 625 lines without interlacing the line frequency would need to be increased to 31 250 Hz. This in turn would call for a greater rate of change in beam intensity and hence spot brightness to trace out the fine detail over each line, and because a greater rate of change or signal amplitude involves a greater bandwidth, more radio space would be needed to accommodate the picture detail of each channel. With the 5.5 MHz vision bandwidth of the 'I' system good definition is obtained at the 15 625 Hz line rate.

Interlacing *could* be avoided without using up extra radio space by reducing the field rate to 25 Hz, but then the picture would suffer bad flicker (subjectively apparent up to about 45 Hz). Interlacing thus solves the problems of bandwidth and flicker without unduly detracting from the displayed information.

Returning to the circuit in Fig. 2, the line frequency is established by a blocking oscillator incorporating VT15 forward base bias through R83 turns the transistor on so that the current through the collector winding of L12 rises. The reversed phase of the other winding puts a negative-going pulse on the base which cuts the transistor off. The on/off cycles are timed by L12/C83/C84 with the oscillator on the free-running mode, the frequency being set by L12 core. The oscillator is synchronised to the line pulses of the signal (as will be explained later).

VT16 amplifies and shapes the pulses from VT15 emitter and transformer T3 couples them to the base of output transistor VT17. The pulses switch this transistor on during the scan so that current flows through the upper left-hand windings of the line output transformer (LOT) T1 and scan coils L14. Because the coils are essentially inductive the current rises as a fairly linear ramp. However, because the effective length of the beam changes with scanning stroke owing to the wide scanning-angle and flat screen of a

contemporary tube, 'S-correction' is required. This is achieved by C93 which reduces the rate scan at the start and end of a line with respect to the centre. Further linearity correction and width adjustment are provided by a closed-loop sleeve set under the scan coils. The field produced by the current induced into this counteracts the non-linearity of the field produced by the scan coils themselves.

VT17 switches off at the end of a scan and the swiftly collapsing current through the scan coils and LOT windings returns the beam to its starting point and yields a high voltage pulse owing to the sudden release of the inductively-stored energy. The repetitive pulses are increased in voltage by the overwind at the top right-hand side of T1, rectified by W14 and smoothed by a capacitance formed by the inner and outer conductive layers on the tube flare, the inner connected to the final anode. The result is a potential of 11.5k V for the final anode. After rectification by W15, pulses from the lower right-hand winding charge C95 to yield a 95 V line for the tube first and third anodes, video output VT7 (to provide about 50 V video swing for the tube) and varicap tuning.

Oscillatory energy is rectified by the booster diode W12 conducting during the retrace to charge C87/C88. This not only damps the unwanted energy which would otherwise cause vertical lines at the left of the picture, but the potential developed from it is used to energise VT17 collector, and contribute to the line scan, thereby improving the efficiency of the line output stage. The stage also adopts 3rd harmonic tuning of the pulses. This tends to flatten the tops of the pulses, which leads to improved EHT regulation. The tuning capacitor is C89 in parallel with a low-induction disc capacitor C92 providing flashover protection.

Sync Stages

Video signal at VT5 emitter is coupled to the base of the sync separator transistor VT 14 through R72/C72. On the 625 line system the picture signal is negative-going (modulation level falling with increasing brightness), and at the end of each line sync pulse occurs whose tip reaches 100% amplitude, as shown in Fig. 3a.

Composite video (picture plus sync) from VT5 emitter is fed to the base of VT14 (sync separator) which is biased to conduct only during the sync pulses so that line sync, coupling is to VT11 (sync amplifier/inverter), whose output drives 'flywheel' discriminator W6/W7, etc. The discriminator is also fed positive-going line pulses from the LOT via C94 which, after RC integration, form a ramp whose phase is compared with that of the line sync pulses. Phase error results in a potential at the top of R78 which, after being filtered by C78/C79/R82 to remove pulse residual is applied to the line oscillator. As this is a VCO, frequency correction and hence line synchronisation are achieved.

From the end of one field scan to the start of the next one, five narrow equalising pulses are followed by five broad field sync pulses and then by another five equalising pulses. The width and spacing of the pulses keep the line synchronised during the field sync period, while the equalis-

ing pulses ensure equal blanking on both even and odd fields, and also identify the two fields for accurate interlacing by cutting off the picture half way through a line at the end of odd fields and starting it after a line is half over at the beginning of even fields, as shown in Fig. 3 (b).

It is worth noticing that test signals and certain teletext data are transmitted on blank lines – the latter at a bit rate of 7 megabits per second. The 1.55 and 5.8 us front and back porches to the line sync pulses provide time for the line retrace, and it is the 5.8 us porch which carries colour burst signal.

The positive-going field sync pulses at VT14 collector are integrated by C99/R124 and applied to VT18 base through W18. The integration builds up a composite pulse for triggering the field retrace and attenuates line pulses.

Tube Biasing and Video Feed

During normal working the tube grid is held at chassis potential by W17. When the set is switched off W17 is reverse-biased and the charge held by C96 drives the grid negative, thereby suppressing the beam, while the supply voltages collapse.

Beaming current cut-off is set by R105 (brightness control) which merely adjusts the tube cathode potential. Video signal from VT7 collector is also applied to the cathode, and as the signal is negative-going the beam current increases with increasing picture brightness. Beam cut-off or black-level is set by the brightness control so that the sync pulses drive the tube below black.

Sound Channel

Intercarrier signal from L10 is fed to IC2 which incorporates a 6 MHz limiting amplifier; quadrature coincidence detector tuned by L11; voltage-controlled attenuator operated by the volume control R54 and an audio preamplifier for driving the class B push-pull output transistors VT9/VT12 via driver VT8. The bases of the output transistors are driven together from VT8 collector, which is possible because VT9 is NPN and VT12 PNP (a complementary pair). Quiescent current is set by R59 at 8 mA. Negative feedback is from the emitters of the output pair via R57 to VT8 base. Since the mains supply is isolated by transformer T2 it is possible to use a headphone set or earphone connected to jack J1.

For those not familiar with the quadrature FM detector the following brief description may help. After passing through the limiting amplifier chain, the inter-carrier signal is changed to squarewave and the signal fed two ways: one way to a synchronous detector and the other way to a 90-degree phase shift circuit and thence to the synchronous detector. The synchronous or coincidence detector combines the two inputs vectorially so that the output consists of the vector sum which, relative to the fixed 90-degree phase shift, changes with the FM deviation. The result is a variable width squarewave (pulse width modulation) which, after integration, yields the audio signal.

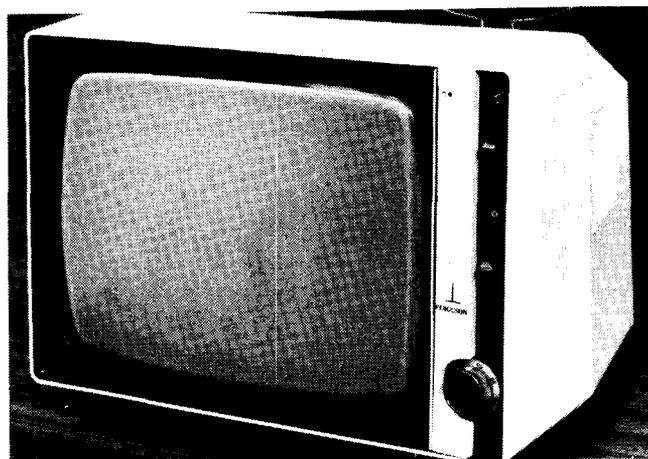
Power Supplies

The receiver can be operated from a 12 V car battery or the mains supply. On mains, isolation is provided by transformer T2 and full-wave rectification by W8/W9, with C70 the reservoir. The supply is fed to the emitter of series regulator VT10. VT13 is the error amplifier which compares a

ratio of the collector output voltage with a reference potential provided by zener W5. Starting current is provided by R66 and the base potentiometer R69 sets the output voltage for the correct value of EHT voltage. Stabilisation is effective over a mains input of 220-264 V. The high V_{be} rating of VT10 provides automatic protection against reversed battery polarity.

Finally, one or two minor points: SP1 at VT7 collector is a spark gap which liberates energy in the event of a flashover inside the tube, directing current away from VT7 collector. The tube is a quick-heat type whose heater is energised from the 11.3 V line and one which is happy with a relatively low focus electrode voltage.

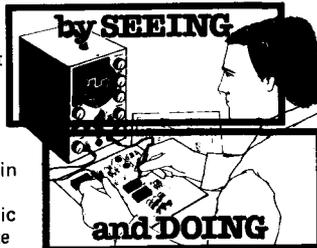
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Chapter 13

OP-AMPS AND INTEGRATORS

Although we're dominantly digital these days, there are some applications where the trusty op-amp is cheaper and easier – differentiating and integrating circuits, for instance.

DIGITAL COMPUTERS, folks, are not always fastest or cheapest. No, don't faint. No kidding – those amazing digital circuits do not always get the jobs done first! They're fine, of course, as long as we stick to straightforward arithmetic, but unfortunately, there are occasions when we want to do other things such as integration or differentiation. Circuits performing these functions are not only of use in computers, however, they are of great use to those of us who are just simple mortals, as well. For instance, in function generators, a squarewave may be changed to a triangular wave merely by integrating.

Now, while digital circuits can perform these functions, they do tend to get a bit bulky and expensive. It's very much easier to use analogue circuits. As it happens, we have very simple networks that make passable integrators and differentiators for very little money. They're capacitor-resistor series circuits, and their operation is quite easy to understand.

Differentiators

We can make quite a serviceable differentiator circuit from the series combination of resistor and capacitor shown in Fig. 1. Now from our original definition of capacitance: the current flowing through a capacitor is given by

$$I_c = \frac{dV_c}{dt}$$

But in the case where we are driving a load with very high input impedance, I_{OUT} will be negligible, and I_R will be very close to I_c . We can say, without too much inaccuracy, that $I_R = I_c$. I_R , however, is given by Ohm's law, $I_R = V_{OUT}/R$. Thus $V_{OUT} = RI_R$. Since I_R is the same as I_c , however, this gives

$$V_{OUT} = RI_c = RC \frac{dV_c}{dt}$$

and so the output voltage is effectively the voltage across the capacitor, differentiated and then multiplied by a scale factor RC . If we don't want this scale factor, we can just arrange matters so that $RC = 1$.

The main problem with this circuit, of course, is that it is, indeed, the voltage across the capacitor, and not that across the input, which is differentiated. However, as long as we don't let the output voltage get too large, V_c will be very close to V_{IN} , and this error will not matter too much.

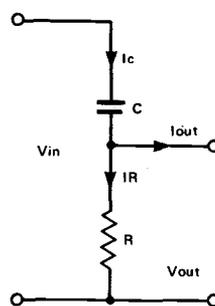


Fig. 1. Basic differentiator.

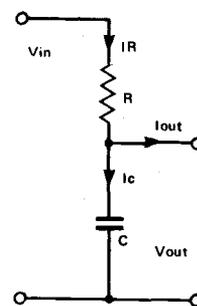


Fig. 2. Basic integrator.

Integrators

The basic integrator circuit is very similar to that of the differentiator – the resistor and capacitor just swap positions (Fig 2). Now we can find the circuit's action in the same way as we did before

$$I_c = C \frac{dV_{OUT}}{dt}$$

Integrating both sides of the equation

$$\int I_c dt = CV_{OUT}$$

But I_c is the same as I_R , provided we are driving a load with high enough input impedance. From Ohm's law, we have $I_R = V_R/R$, and thus

$$1/R \int V_R dt = CV_{OUT}$$

Dividing both by C

$$V_{OUT} = 1/RC \int V_R dt$$

Again, the voltage being integrated is the voltage across only one of the components – the resistor – and not that across the entire circuit. However, as long as we again arrange that V_{OUT} , that is, V_c , never gets *too* large, V_R is very close to V_{IN} , and we have a fair approximation to an integrating circuit with a gain of $1/RC$.

Bigger and Better

So far, the circuits we have looked at have had two main disadvantages; they are accurate only when driving circuits

which have very high input impedances, and their output voltages cannot be allowed to become very large, or the difference between the input voltage and the voltage actually being acted on becomes too large to be ignored. (This in turn puts restrictions on the allowable values of RC time constants and thus the components themselves, but we won't go into that.) How can these problems be solved? Did the man at the back mention op-amps? Dead right, friend. To see how they might be useful, however, let's do a quick bit of revision on them. (Those familiar with op-amps skip the next section.)

Op-Amps

Op-amps are famed for three major properties. The first of these is a very *high input impedance*, the second is a very *low output impedance* and the third is a *gain so high* that it may be approximated to infinity without too much inaccuracy for most purposes. It is this last property which leads to the 'virtual earth', a very useful concept in analysis of op-amp circuits.

The voltage gain of an amplifier is, by definition, *the ratio of its output voltage to its input voltage*. If the gain is m , then the output voltage V_{OUT} is mV_{IN} , or, if we are using the inverting input of an amplifier, $-mV_{IN}$. However, as we have stated, the gain of an op-amp is close to infinity. Thus, its output voltage is infinity times its input voltage, or, putting it another way, the input voltage is equal to the output voltage divided by infinity. Since the output voltage must be finite, the input voltage, or, more accurately, the difference in voltage between the inverting and non-inverting inputs, of an op-amp, must be zero. (Yes, I know it looks as though I've cheated somewhere, but I can assure you that it works.) Since this difference in voltage is zero, it follows that if we ground one input of an op-amp, the other input automatically goes to zero potential. This is not to say that it automatically gets shorted to earth — there is still a very high resistance between the two points — it just means that no voltage will be present; there is a 'virtual earth'. This concept, as has been stated, is a very useful one. Now we can apply it to our integrator and differentiator circuits.

The New Improved . . .

We saw in the last section that an op-amp has a very high input impedance and a very low output impedance. It was a very high input impedance, you will remember, that we needed for our basic circuits to drive, so suppose we put some sort of unity gain voltage amplifier on the outputs. It wouldn't affect the signal in any way, but it would mean that we could drive circuits with lower input impedances.

Well, using an op-amp, a unity gain voltage amplifier has a circuit something like that shown in Fig. 3. It's easy enough to understand; the output is shorted to the inverting input and the voltage present at each is identical. However, the difference in voltage between the two inputs must be zero and so the same voltage is present at the input to the amplifier as is at the output. In practice, this means that the output voltage follows the input voltage. Amplifiers like this are often used as 'buffers' — allowing high output impedance circuits to drive low input impedance ones.

If we put one of these buffer amplifiers on the output of each of our circuits, we have the circuits shown in Fig. 4, and we have, indeed, solved one of our major problems; the circuits no longer need to drive into high impedances. The other problem is still present, however. Is it possible to improve our circuits again? Well, yes.

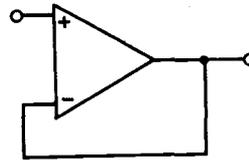


Fig. 3. Unity gain voltage amplifier.

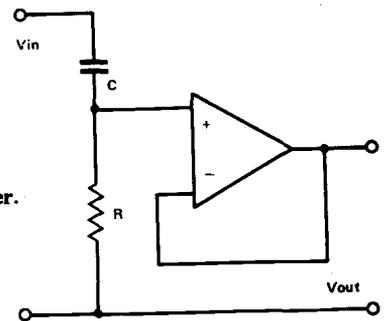


Fig. 4. A differentiator with buffer.

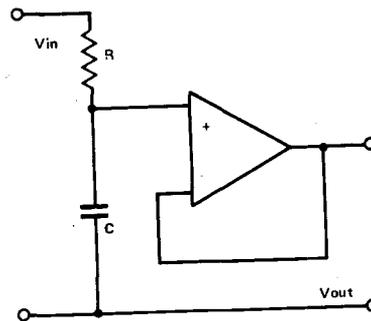


Fig. 4b. Integrator with buffer.

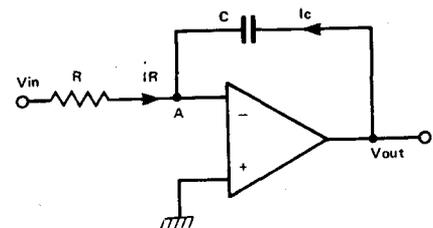
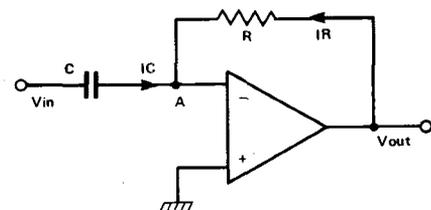


Fig. 5a. (above) Integrator circuit using an op-amp, and b. (below) differentiator circuit using an op-amp.



At Last . . .

We'll look at the integrator first. The circuit is shown in Fig. 5a, and does not use an op-amp tacked onto the end, but instead, as an integral part of the circuit. (Yes, that's right, it's an integrated integrator). Its action is as follows:

Since the input impedance of the op-amp is very high, it follows that the current actually flowing into it is very small, and hence $I_R = -I_C$, to a first approximation, in order to keep the currents flowing into point A sum to zero. (Kirchhoff's first law - the algebraic sum of all the currents flowing into a point of a network is zero. This is the same as saying current in = current out.)

However, Ohm's law tells us that the current flowing through the resistance is given by the voltage across it, divided by the resistance. Now, the voltage at A is zero (virtual earth), so the current through the resistor is V_{IN}/R . The current through the capacitor is given by

$$I_C = C \frac{dV_{OUT}}{dt}$$

Hence, we have, since current through the resistor equals current through capacitor

$$V_{IN}/R = -C \frac{dV_{OUT}}{dt}$$

and so

$$V_{IN}/RC = -\frac{dV_{OUT}}{dt}$$

Integrating both sides of the equation, we obtain

$$\frac{V_{IN}}{RC} dt = -V_{OUT} \text{ or } V_{OUT} = -1/RC \int V_{IN} dt.$$

Since R and C are constants, and can thus be moved out of the integration sign.

Hence we have effectively a circuit which integrates input voltage with respect to time, and which has, once again, a gain given by $-1/RC$. The integrating action may be seen if we apply a squarewave to the input. We obtain a triangular wave as output, and one which compares very favourably with that obtained from our original circuit (Fig. 6).

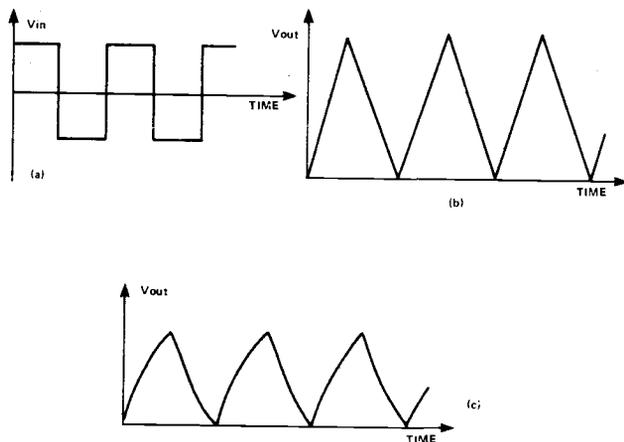


Fig. 6a. Input squarewave signal; b. output from op-amp circuit; c. output from original circuit.

Differentiator Mark 3

The action of the differentiator circuit (Fig. 5b) can be explained similarly. Again, current through the resistor is equal to that through the capacitor, because of the very high input impedance of the op-amp.

$$I_C = -I_R$$

But I_R is given by $(V_{OUT} - V_A)/R$ and V_A is zero (virtual earth again). Similarly, I_C is given by CdV_{IN}/dt . Therefore

$$V_{OUT}/R = -C \frac{dV_{IN}}{dt}$$

multiplying both sides of the equation by R, we get

$$V_{OUT} = -RC \frac{dV_{IN}}{dt}$$

And we have a differentiating circuit, the gain of which is given by $-RC$. We can see the differentiating action if we apply a squarewave to the circuit as in Fig. 7.

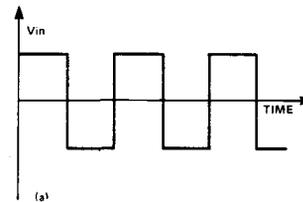
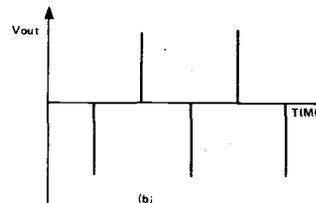


Fig. 7a. (above) Input squarewave signal, and b. (below) output from op-amp circuit.



Howzat!

With these two circuits we have overcome the difficulties experienced with our original RC combination series circuits. The voltage being acted on is the input voltage actually and, thanks to the low output impedance of the op-amp, we can use these circuits to drive many more circuits. The output voltage, which we were forced to restrict in our original circuits for fear of affecting the action of the circuits, is now restricted only by the supply voltage to the op-amps.

The outputs of these circuits are, of course, inverted, as is shown by the minus signs in our equations. This is because of practical difficulties incurred when a non-inverting circuit is used, and can easily be solved by tacking a unity gain inverting voltage amplifier onto the output - surely a small price to pay for all the advantages that these circuits give us over the originals.

A. Lipson

Chapter 14

EDDY CURRENTS

The life story of Eddy Current, last known to be circulating in the region of discs and transformers.

THE BRANCH OF PHYSICS now known as *electromagnetism* can be said to have been born in 1819. It was in that year that Professor Oersted of the University of Copenhagen discovered that electricity and magnetism are related – that a current flowing in a conductor produces a magnetic field in the close neighbourhood of the conductor. Later, around the 1830s, the reverse effect – that an electrical current can be produced in a conductor by a changing magnetic field – was discovered simultaneously, and quite independently, by Faraday in England and Henry in America.

Both of these effects are used, for example, in the transformer; an alternating current in a coil creates a changing magnetic field, which, in turn, is used to produce an EMF (and hence a current, should a circuit be connected) in another coil. However, rather less people are aware of another, very closely related, and extremely interesting, effect – the phenomenon of eddy currents.

What's In A Name

Magnetic fields are not usually quite as selective as we would like them to be. A changing magnetic field will not only produce an EMF in any coils in its vicinity, but it will also produce EMFs, and hence currents, in any conductor around – even any old lumps of metal that may be just hanging about. These currents don't actually go anywhere – they just circulate round and round within the conductors, like eddy currents in a liquid. Hence the name – eddy currents.

Since eddy currents are the result of induced EMFs in conductors, and because resistances within conductors, can be very small, the current can on occasion be quite sizeable, and so the effects produced by them can be very significant. In fact, eddy currents are far more than just a scientific curiosity. Depending on exactly where they are, and what they are doing, they can be either a curse or a blessing. However you view them, though, they are an interesting phenomenon, and can produce some fascinating effects, not all of which are totally useless!

Count Your Blessings . . .

One of the more striking experiments on eddy currents is shown in Fig. 1. A horseshoe magnet is suspended on a thread, above an aluminium disc which is itself free to turn about its centre. If the magnet is now spun round, the aluminium disc starts to rotate with it (although it never quite catches up with the magnet). Similarly, if you spin the aluminium disc, the magnet above it also starts to turn. This obviously cannot be due to ordinary magnetic effects –

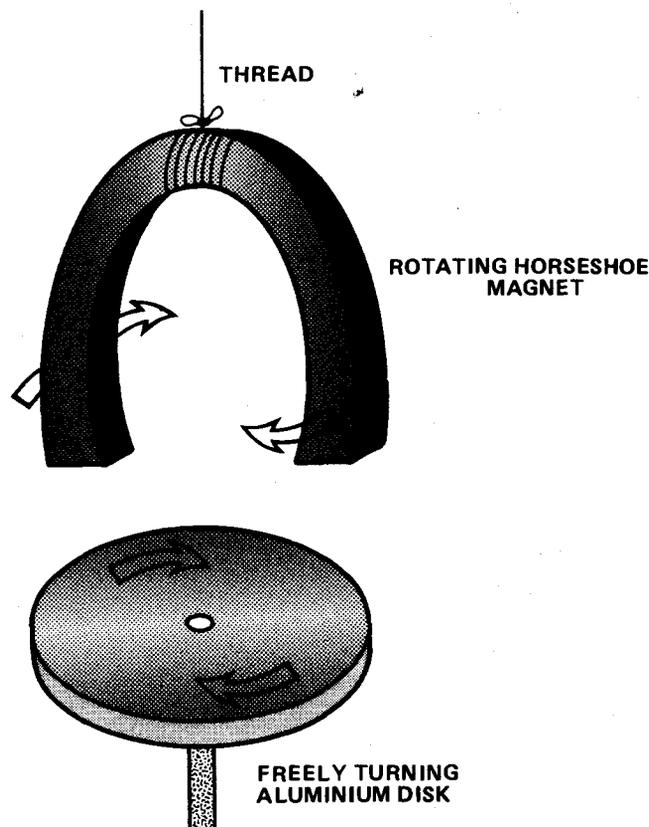


Fig. 1. The rotating magnet induces eddy currents in the aluminium disc.

aluminium is non-magnetic, and if you try to pick up the disc with the magnet, you will find that you are unable to. It is apparent that something funny is going on. (No, air currents aren't dragging the disc round when the magnet rotates – you can put a sheet of paper between the two, and the effect still works!)

Field Study

The relative movement between the magnet and disc is inducing eddy currents in the aluminium. These, in turn, create other magnetic fields, and it is these that cause the magnet and disc to move together – the magnetic field of the magnet interacting with the fields caused by the eddy currents (sounds a bit like pulling yourself up by your bootstraps, but it's correct). An interesting follow-up to this experiment is to replace the disc with one cut as shown in Fig. 2. The slots tend to get in the way of the eddy currents and prevent them from flowing, so such a disc is not

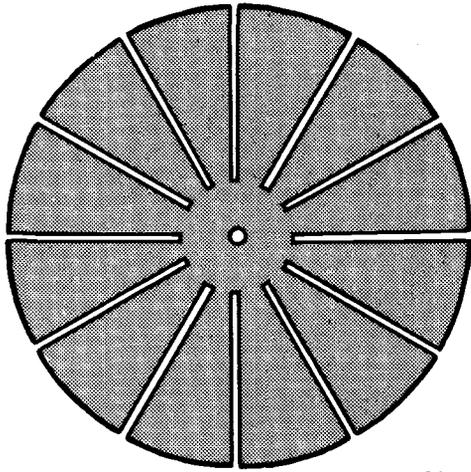


Fig. 2. If the disc in Fig. 1 is replaced with one cut like this, the drag effect is greatly reduced, or even stopped.

dragged round so easily by a magnet (which is another way of showing that air currents don't do the work – the slots shouldn't make any difference to them).

Interestingly enough, this apparently insignificant effect actually has some practical application. It is used, for instance, in the normal car speedometer! The rotation of the wheels is transmitted, by various means, to a magnet, which itself rotates, with a speed proportional to that of the wheels. This rotating magnet induces eddy currents in an aluminium disc (or its equivalent) and tries to drag it round. However, a spring is used to hold the disc, so it is unable to turn very far. The faster the car goes, though, the faster the magnet rotates, the greater the eddy currents, and the further round the aluminium disc is pulled. By attaching a little red or orange needle to this disc and seeing how far this needle rotates, we can work out how far the disc has turned, and hence the speed of rotation of the magnet. Thus, we find out the speed of the car. Yes, I wish I'd thought of it first, too.

Cutting Your Losses

Besides being useful, though, eddy currents can also be very annoying. They could justly be called the transformer designer's nightmare. The transformer is, basically, two coils close together. However, in the middle there's a dirty great lump of metal (the core) and it doesn't just sit there doing nothing, with all those magnetic fields about. No prizes for guessing what happens. It might not seem that eddy currents in the transformer core would be much of a

problem, but they are, for two main reasons. Firstly, the eddy currents mean a loss of power in the transformer and hence reduced efficiency. It stands to reason that if power is being used to drive currents around in the core, then that much less power is going to be available for use from the secondary coil. The second problem is no less serious, especially in large-scale transformers. The power being wasted in the core, driving eddy currents round, quite naturally ends up as heat, and consequently transformers are liable to get very hot. Indeed, large transformers, such as those on the national grid, may be oil-cooled, to prevent overheating.

It is obvious that, in transformers at least, eddy currents are not wanted. So what can be done about them? Well, if you've ever taken an old transformer apart for the wire, or even just out of curiosity (naughty, naughty) you will probably have noticed that the core is not just one solid lump; it is built up of flat metal laminations. This is not because they make the cores out of flattened baked bean tins. The laminations are separated by varnish or paper or some other insulator and this greatly increases the internal resistance of the cores, reducing eddy currents. Hence, both the loss of power and the unwanted heatings are reduced.

Even the heating effect of eddy currents can be put to use, though. It is used in the production of pure crystalline samples of conductors like metals or semiconductors – germanium, for example. The impure sample of the material is passed in a crucible, through a coil, which has passing through it a high frequency alternating current. The magnetic field produced by this current induces eddy currents in the specimen and the heating effect is great enough to melt it! As the sample passes through the coil, the molten zone within it is carried to one end (Fig. 3). Impurities within the sample are accumulated in the molten zone and hence get taken to one end of the specimen. This end is later removed. What is left is a very pure, crystalline sample of the substance. So eddy currents can be surprisingly useful!

Footnote

There is one final point which must be at least mentioned in connection with eddy currents. This is the induction motor, an indispensable servant of industry. It depends for its operation on eddy currents . . . full explanation of that, though, is another story altogether.

A. Lipson

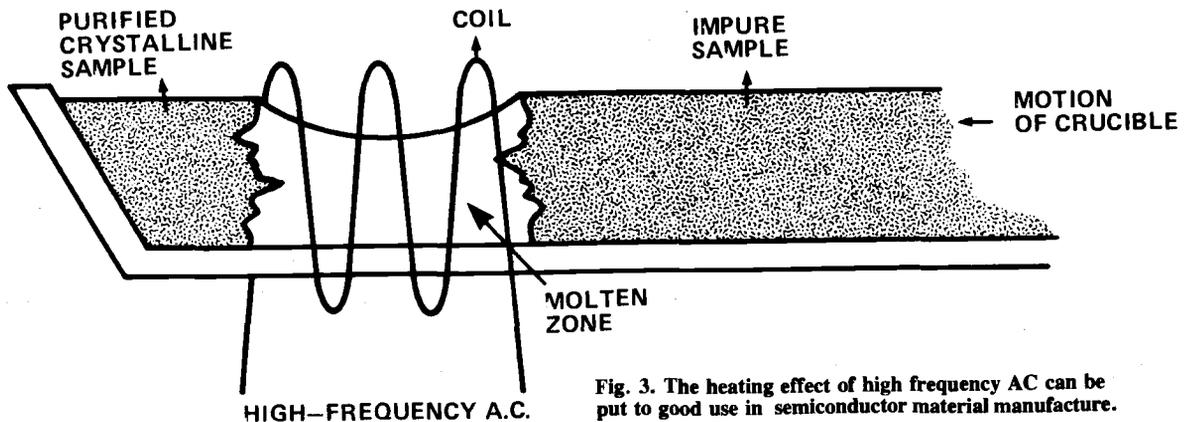


Fig. 3. The heating effect of high frequency AC can be put to good use in semiconductor material manufacture.

Chapter 15

HEAD AMPLIFIER DESIGN

How to design your own headamp – plus insight into low-level audio design

OVER THE PAST FIVE YEARS there has been a tremendous upsurge of interest in new methods of extracting the musical information from the depths of the record groove. Along with this has come a re-appraisal of the relative merits of the moving coil and moving magnet pickup cartridges. Each has a great deal to recommend it and we should start by comparing the two, albeit briefly.

The principle of operation is the same, ie. a current is inducted in a coil by a (relatively) moving magnetic field. In the moving magnet type it is, as the name suggests, the magnet that moves because it is mounted on the opposite end of the cantilever to the stylus.

Mass Tendencies

This system works well, but the mass of the magnet/stylus assembly has a nasty tendency to resonate within or just above the audio band. With careful design this effect can be minimised, but some colouration of the sound still occurs. Another problem is that the high impedance of the cartridge, due to the high number of turns required to achieve a usable output, also causes matching problems, leading to high frequency losses in the signal lead capacitance.

Role Playing

Technology, however, has made possible an effective reversal of the roles of magnet and coil, neatly overcoming the problems just mentioned, as it is now the coil which moves inside a static magnetic field. (It is only fair to mention at this point that Ortofon have been producing very underrated moving coil cartridges for many years and are generally considered to be the pioneers of the field). The coil can be made very light, reducing the resonance problem and the output impedance is low due to the small number of turns used, which cures the lead losses.

All is not quite sweetness and light, however, as the system brings its own set of problems, which can be summarised as:

1. Low output – 150 μ V nominal
2. Very low source impedance
3. Expensive to manufacture

These problems *can* be overcome at a price, however, and if it is perfection for which you strive, the moving coil cartridge can be considered the best method of transferring data from the record to your ears at present. It is interesting to note that most of the current batch of professional Hi-Fi reviewers use a moving coil cartridge against which others are judged.



Coming Up in the World

A step up device is required to match the low output impedance of the cartridge and to raise its meagre output to a point comparable with the universal moving magnet input or amplifier at approximately 5 mV. One way to achieve this is by the use of a matching transformer similar to those used with low impedance microphones. This solution, however, brings in problems such as secondary load matching, third harmonic distortion, frequency response limitations and hum pickup, all of which require careful and thus expensive design to overcome successfully. An active amplifier is a more cost effective (the watchword of the eighties) solution and has the added advantage of being within the design capabilities of the home constructor.

Design Criteria

The criteria to be considered in the design of such a pre-amplifier are *primarily noise, frequency response and distortion*. If we consider a general MC (Moving Coil) cartridge with an output of 150 mV, source impedance of 10 R, and frequency response of 20 Hz to 25 Hz, a matching head amp would have to have at least the following characteristics to achieve Hi-Fi standards:

1. Gain x 30 for nominal 4.5 mV output into 47k
2. Signal to noise ratio better than 60 dB

3. Distortion less than 0.05%
4. Overload factor better than 40 dB
5. Frequency bandwidth better than 20 Hz to 20 kHz

The input impedance should theoretically be the same as the cartridge source impedance for maximum power transfer, but it has been argued that MC cartridges work best into loads somewhat higher than this, as it reduces the power dissipation in the (cartridge) coil. Manufacturers differ widely in their recommendations for input impedance, but values between 100R and 470R are most commonly quoted. These values are normally determined by audition, but in my experience strict adherence to the recommended value is by no means as important as one is lead to believe, the differences in sound being more likely due to circuit variation than to mismatch. A good general purpose design *should*, therefore, be suitable for all MC cartridges.

Noise Model

Noise can be thought of as an additional voltage appearing at the input of an amplifier, the ratio between this voltage and the input signal voltage being measured signal to noise ratio. It is assumed in this model that all noise introduced by the amplifier is added to this input noise voltage and that subsequent amplification of both signal and noise takes place equally and noiselessly. If we wish to achieve a signal to noise ratio of better than 60 dB, this implies an equivalent input noise voltage of around 150 nV. As a comparison, a moving magnet input stage with a signal to noise ratio of 80 dB would have an input noise level of 450 nV and only the very best amplifiers ever achieve anything like this kind of noise figure.

There are three main sources of noise in a transistor amplifier, thermal noise, flicker noise and shot noise. The first two are common to all electronic components, both active and passive, whereas the last is produced in active devices only. Without getting too bogged down in active semiconductor physics, shot noise is caused by random fluctuations in the diffusion of minority carriers at the base/emitter junction of the transistor and also by recombination effects within the base region.

Suffice it to say that this type of noise is proportional to the emitter current flowing through the transistor (or diode) and is broadband. Flicker noise is present in semiconductors, resistors and thin metal films, and is produced by skin effects in the surface of the conducting regions of the device. The noise level depends upon the

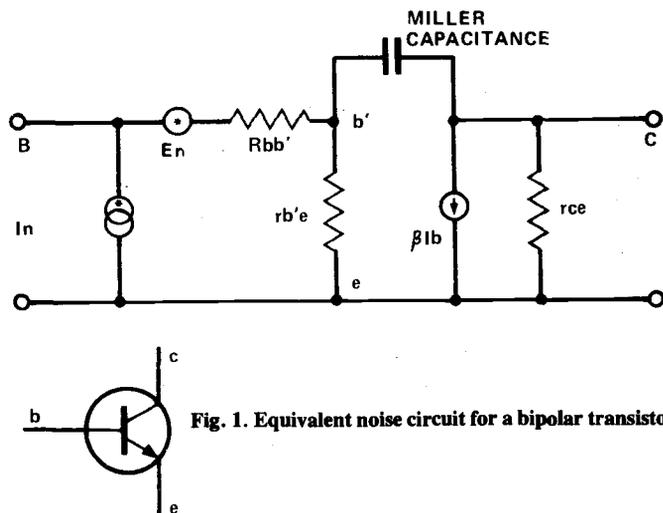


Fig. 1. Equivalent noise circuit for a bipolar transistor.

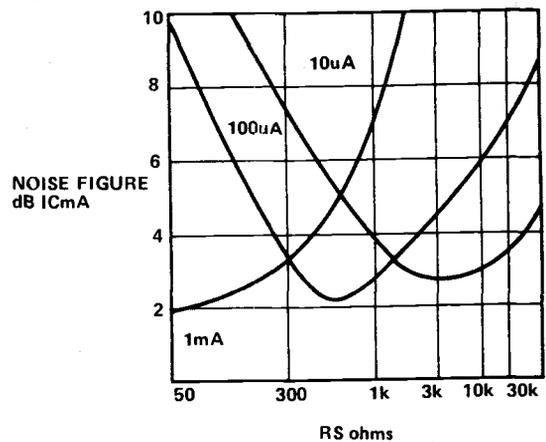


Fig. 2. Noise curves for the BC413.

material, but is typically proportional to I^2/F , where I is the current flowing, and is thus often called I/f noise. Thermal noise is, as the name suggests, produced by thermal agitation within the component material and is again broadband in character and proportional to the temperature of the device. The level of noise can be calculated from the equation: $e^2 = 4KTBR$

- where
- e = generated noise voltage
 - K = Boltzman's constant
 - B = frequency bandwidth over which to noise is measured
 - T = temperature in degrees Kelvin
 - R = the resistance value

Armed with this knowledge, the potential noise generated by any component used in our proposed head amp can be measured and steps taken to reduce its contribution to the total noise produced by the circuit.

In general there are four ground rules which should be followed to help achieve good performance:

1. Choose low noise components
2. Pay careful attention to transistor biasing arrangements.
3. Keep resistor values as low as possible
4. Pay careful attention to avoid the pickup of external noise sources.

Couldn't be simpler could it?

Low noise types of resistors are metal oxide, close tolerance metal glaze, or thick film. Avoid the use of large electrolytics as the (inevitable) leakage currents generate noise. Tantalum or polycarbonate types are best for the higher capacitance values and polystyrene or silver mica the best cost/size/noise level compromise for lower values. PTFE is the best of all, however, but tends to be on the expensive side. The noise levels produced by transistors are normally obtained from the manufacturer's data and there are several factors to be considered.

Equivalent Thinking

If we refer to the equivalent circuit for a transistor in common emitter configuration shown in Fig. 1, and then consider the various noise sources contained within this circuit, a mathematical expression for the total noise generated can be derived. The exact form of this equation requires far too much deep thought for us to deal with it in detail here, but note that both noise voltage and noise current terms would be involved. It is also immaterial because transistor manufacturers are kind enough to measure it for us and provide noise versus frequency, and noise

versus source resistance plots which take the general form shown in Fig. 2.

The overall noise level is dependent upon the collector current flowing and for the lowest noise there is an optimum source resistance.

For use in our head amplifier, this should be ideally be the same as the source impedance of a moving coil cartridge, (about $10R$) but due to the need to optimise other parameters it is more likely to be between $1k$ and $10k$ for a typical audio low noise transistor. This is because the vast majority of uses for these devices involve higher source impedances, ie $47k$ and the manufacturers do not see a sufficient market to justify production of a special low noise, low source resistance type, except, that is, for the ever-industrious Japanese.

A Nipponese semiconductor firm introduced the answer to the head amp designers dreams with its range of low noise transistors with optimum source resistances as low as $2R$! This ability to cobble up a special device to order, where no standard model is adequate, is one reason why the Japanese rule the audio kingdom.

Phenomenal

All is not yet lost, however, as there are two phenomena which may be used to advantage when designing a low noise amplifier with standard components. The first is that some medium power transistors exhibit better noise figures when driven from a low source resistance than normal low noise, low level types. This is mainly due to the need to keep r_{bb} low (see Fig. 1) in order to obtain good h_{fe} figures when operating at relatively high collector currents (values between 1 mA and 10 mA are common), which tends to rule out battery operation.

This brings the additional problem of the mains supply, of which more later. Suitable transistors for this type of use are 2N4405 or BC361, both of which have been successfully used in commercial designs.

The second possible answer is the use of a parallel transistor stage. This is where several transistors are wired in parallel, obvious really isn't it? The main advantage of which lies in the fact that in common emitter mode the base/emitter junctions are in parallel and thus the noise currents and voltages produced by each transistor are summed together (See Fig. 3). The basic rule for communications engineers considering the noise levels of their systems is that noise signals from several separate sources, feeding into a common input, *add* by power.

Therefore, the total noise voltage for our parallel stage

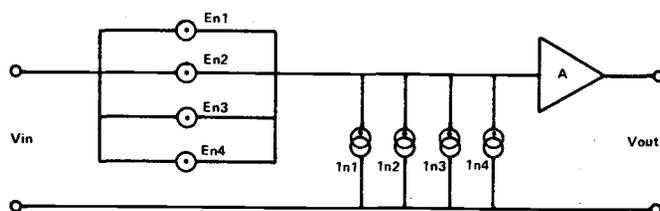
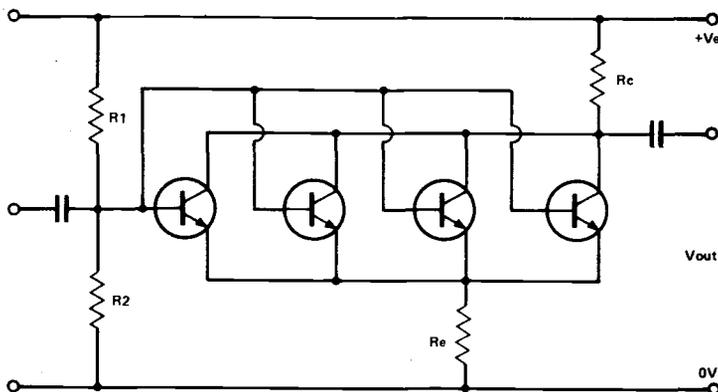
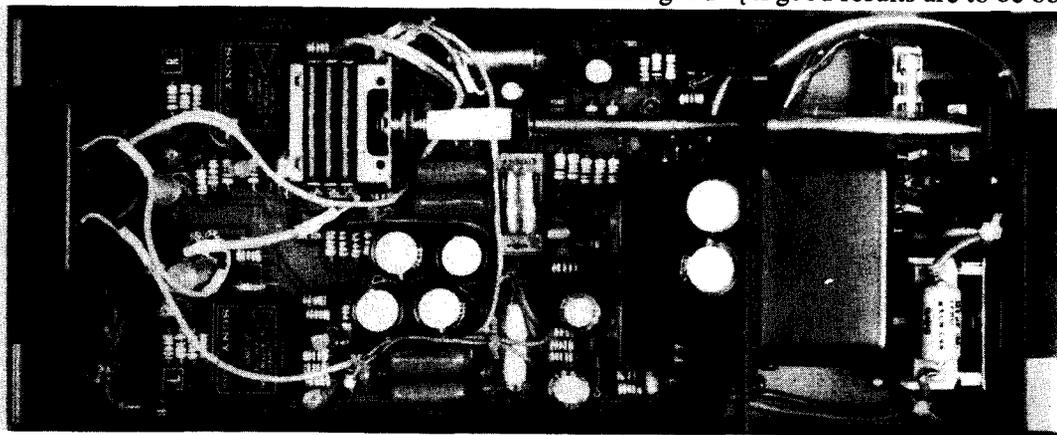


Fig. 3. Noise model of parallel stage.

will be given by the equation $E_{nt} = E_n/N$ where N is the number of transistors. Similarly the total noise current will be given by $I_{nt} = NI_n$. Now the best noise source resistance for a transistor is given by $R_o = E_n/I_n$ and so for our parallel stage this is $R_{ot} = E_{nt}/I_{nt} = R_o/N$. R_{ot} is thus dependent upon the number of transistors used in parallel, the greater the number used the lower the best source resistance becomes.

Let us now consider a typical low noise transistor with a best source resistance of $2k$ to be used with an MC of source impedance $10R$. The number of parallel transistors required for the best match is given by $2000/10 = 200$. This is clearly impractical for reasons of cost, the physical space required and, more important, the high value of Miller capacitance that would result. As can be seen from Fig. 1, the Miller capacitance introduces feedback between the collector and base of the transistor and is the factor which limits the high frequency response. It would be a major problem if this many transistors were used. In practice eight transistors seems to be the best compromise and is the number most commonly used. Even so it is important to choose a transistor with both a low best source resistance and a good F_t if good results are to be obtained. The F_t of a



transistor is the frequency at which the gain becomes unity and should be in the region of 200 MHz. Suitable types for this type of use are BC413, BC415, BC337, 2N4148.

Circuit Options

So much for the theory, we come now to consider the options open to us, in terms of the circuit configurations, which may achieve the required specifications for our head amplifier. Something to remember here is that any biasing components used will also add to the noise. Take a standard common emitter circuit, for example, with feedback to counteract thermal changes as shown in Fig. 4. The noise voltages produced by R1, R2 and R3 all contribute to the overall noise of the stage. The base resistors are particularly important as their noise voltages are effectively in parallel with the input signal and will be amplified by such. The contributions of these biasing components can be reduced by decoupling as shown in Fig. 5. The biasing under DC conditions remains the same, but the equivalent noise circuit is as shown.

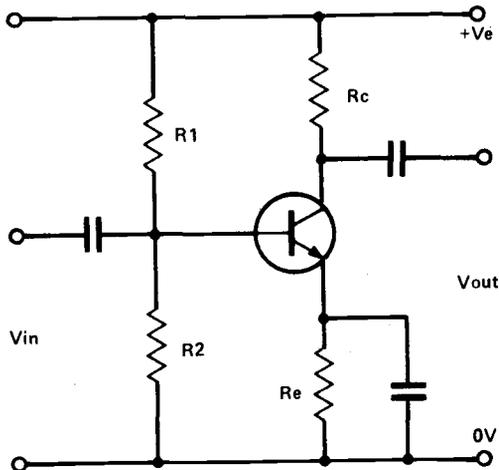


Fig. 4. A standard common emitter circuit.

Note that only the noise associated with R3 will contribute to the input noise and this may be made low in value reducing the thermal noise from this component.

These examples serve to illustrate the principle because a single stage circuit is unsuitable for use as a high quality head amp. The main reasons for this are the variations in gain due to the spread of H_{fe} values in any transistor type and the relatively high values of distortion which are produced. Some form of feedback is required to stabilise and reduce both these parameters and, in general, at least a two stage circuit must be used to produce an acceptable performance.

Controversial Distortion

There is no "best" circuit but there are, as always, some points to bear in mind. In order to reduce the distortion to an acceptably low level, a fair amount of feedback is required and care should be taken to avoid Transient Intermodulation Distortion (TID). This particular form of distortion has proved to be somewhat difficult to define rigorously and there is not an inconsiderable amount of controversy as to exactly what it is and how to avoid it.

Nevertheless it is generally accepted that TID is reduced by ensuring that any amplification stage has a greater gain

bandwidth than the stage preceding it. TID also depends on the amount of overall feedback applied around the circuit and careful design of each individual stage to control the amount of harmonic distortion produced will reduce the amount of overall feedback required and hence reduce the circuit susceptibility to TID.

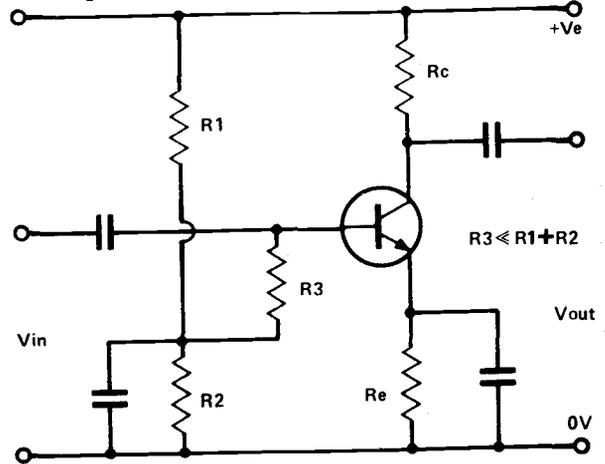


Fig. 5. Low noise base bias circuit.

Breakthrough

The frequency response of the design is also important for two reasons. Apart from the obvious need to keep it wide enough to encompass the whole audio band (traditionally 20 Hz to 20 kHz), it also plays a part in the circuit's susceptibility to Radio Breakthrough. This is a problem because of the high sensitivity of the front end coupled as it is to what is in effect a tuned circuit made up of the cartridge inductance and the input capacitance. My extensive, but completely unintentional, researches into this subject have shown that the two most popular sources of RF interference are Radio 4 at 200 kHz and the local Police/Fire/Ambulance/Taxi Services at anything between 90 and 120 MHz, though the latter is normally only a problem if the offending transmitter is passing close to your Hi-Fi. So, don't put your new moving coil set-up in the front room, folks, if you live on a busy road. The installation of a Mu metal garden gate and front door might also help. Another potential source of RF comes from Citizen's Band transmitters on 27 MHz.

The offending RF signal is normally received by the first stage acting as a simple diode detector and can be tackled by careful attention to earthing and by the provision of RF filters in the input and supply lines. The input loading capacitor provides good RF decoupling only if a type with good high frequency characteristics is used. Ferrite beads on the input connecting leads can also be used to increase their inductance.

Breakthrough occurring from supply line pickup requires further decoupling to eliminate it. Large electrolytics have a substantial impedance at high frequencies and so should be shunted by a capacitor with better characteristics. A 100 n ceramic is suitable here and a small inductor in the supply line is also good practice.

Passing the Buck

Another method of avoiding breakthrough is to make the bandwidth of the head amp wide enough to include any potentially troublesome frequencies. A bandwidth of, say, 10 MHz, would include most national AM stations and any

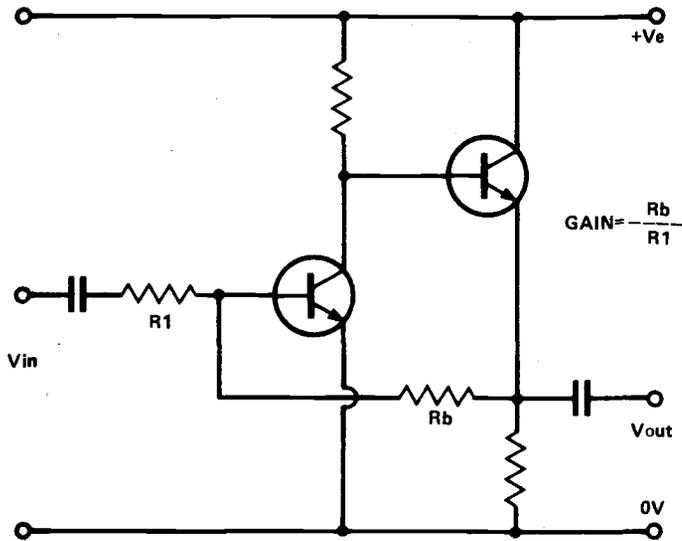


Fig. 6. Common emitter/emitter follower amplifier configuration.

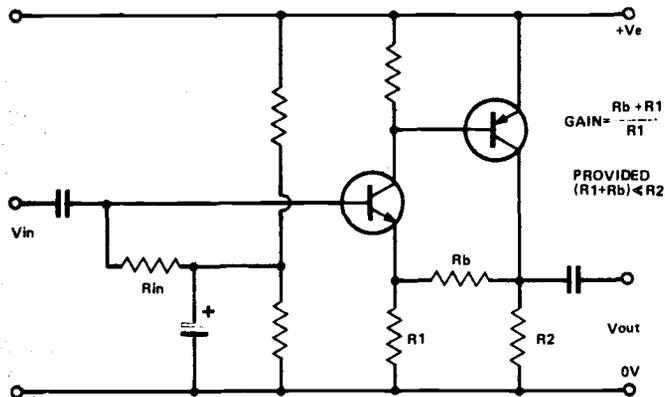


Fig. 7. Common emitter/common emitter amplifier configuration.

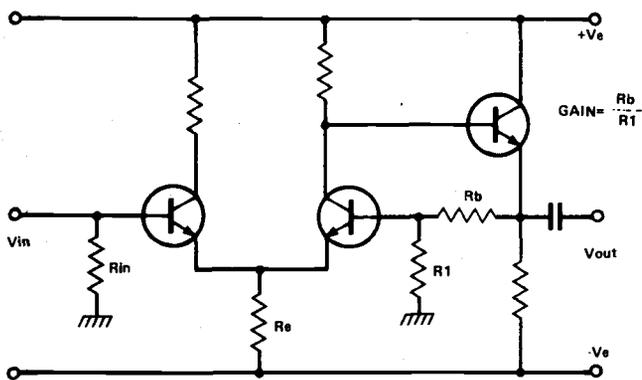


Fig. 8. Differential input circuit.

signal picked up would simply be amplified without being detected and passed into the main amplifier. This is known as "passing the buck" in the trade and relies upon the better RF rejections characteristics of the RIAA equalisation stage.

And So To Details

A typical two stage amplifier is shown in Figs. 6 and 7. These are of the common emitter/emitter follower and common emitter/common emitter types respectively and serve as good examples of typical designs. Both circuits are direct coupled and have overall negative feedback to set the required gain and reduce distortion.

The effect of temperature on biasing is also minimised and note that the low noise method of biasing is used in Fig. 7. To reduce noise to a minimum the feedback components should be kept as low in value as possible, preferably around the 1-10R mark, though this is only practicable in the latter circuit as R1 in Fig. 6 is also the input impedance presented to the cartridge and thus should be somewhere near 100R.

This resistor is in series with the base of the first transistor, however, and as this is probably near to the best source resistance for this stage, assuming the use of parallel transistors, can provide a trade-off with the noise contributed by the relatively high values of the feedback components.

When using low feedback resistor values make sure that there is sufficient drive capability in the circuit. A feedback resistance of 10R in Fig. 7, for example, will require a drive of 100 mA for a 1 V swing and would, therefore, require the use of a medium power transistor in the second stage.

This component may also contribute its fair share of noise and some degree of experimentation will be required to reach the best compromise.

Redundant Capacitor

A differential input stage as shown in Fig. 8 may be used to great effect. The input is referenced to signal earth, eliminating the need for an input capacitor. The resistance to supply-borne interference and hum is also greater with this kind of configuration and can be further improved by replacing Re with a constant current generator. This is just as well because the need for a differential supply makes battery operation expensive and somewhat impractical.

A second gain stage may be added to increase the amount of feedback applied and so reduce distortion. This may be another differential stage or even an operational amplifier (Fig. 9). This latter option may suffer a noise penalty due to the inherent noise output of the op-amp but there are some good low noise types now available, such as the TDA1034N and TL071.

Design Examples

The head amplifier design published in ETI in January (1980) is a gold example of a differential input stage (Fig. 10), which also makes use of a symmetrical output stage. A different approach is shown in Fig. 11, that of the

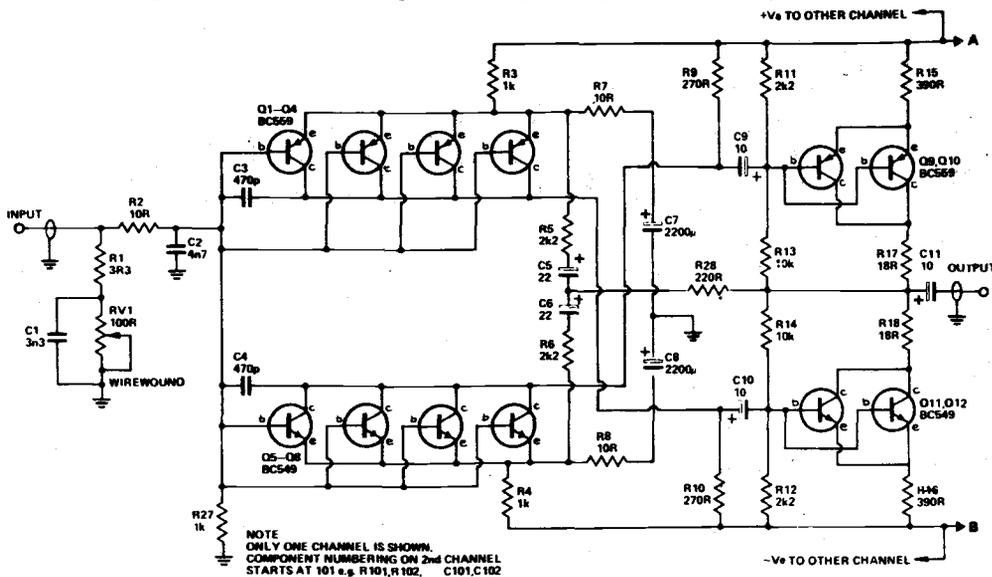


Fig. 10. For full details of the ETI Moving Coil Preamplifier, see ETI January 1980.

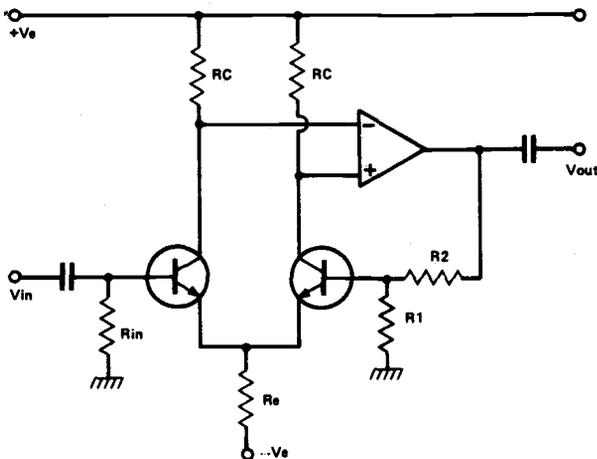


Fig. 9. Differential input with op-amp.

Videotone H300 amplifier. This is a refined version of the circuit in Fig. 6 and is based on a simple parallel transistor pair.

Eight transistors are used for Q1 and two for Q2 and a boot-strap capacitor is employed to increase the open loop gain and so keep the distortion well below the noise level.

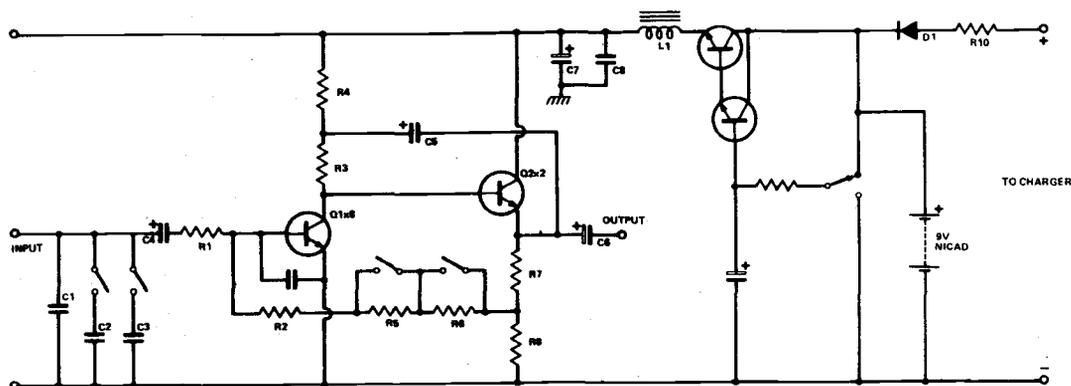
The design also features switchable gain and input capacitance to allow many different cartridges to be catered for. The commercial unit is powered by a rechargeable battery which is put on trickle charge when the head amp is switched off. This neatly removes both the need for a sophisticated mains power supply and the tedium of changing batteries.

Any output spikes produced on power up or down, so prevalent in other designs, are also eliminated by the use of a darlington pair to slowly raise and lower the supply rail when the power switch is operated. The time constant of this rise and fall is far greater than any others in the circuit and so the unit switches on and off without damaging your precious speaker cones if you inadvertently leave the volume turned up.

Another advantage of this particular configuration is that the feedback resistor provides the bias for the first stage so that potentially noisy input bias resistors are not required. The common emitter second stage gives a low output impedance, which enables relatively long signal leads to be used and renders variations in main amplifier input impedances unimportant. The frequency response extends well up into the MHz region to reduce susceptibility to RF pickup and note also the use of an inductor in the supply line.

Andy Sykes

Fig. 11. The Videotone H300 uses a different approach from the ETI design.



Chapter 16

CURRENT AFFAIRS

We seem to take for granted that circuits work, but why is it that conductors, semi-conductors and insulators do just what their names imply? Read step by step through the whys and wherefores of atomic structure.

MOST OF US are reasonably familiar with what electricity is – the movement of electrons through a conductor. But there are some things that we tend to take for granted. For instance, why is it that some materials, like metals, conduct easily, whereas others (insulators) don't, and still others (semiconductors) seem to be somewhere in the middle – conducting, but not as well as metals? In order to find out why, we'll first have to learn something about atomic structure . . .

First Theory

Essentially, the atom consists of a central, very small positively-charged lump called the nucleus, surrounded by negatively charged electrons. Many books – particularly old ones – tend to give the impression that the electrons are just like little planets orbiting a sun (the Nucleus) and that the atom is like a miniature solar system. This is *wrong*. Electrons do not behave just like little billiard balls, or little solid lumps. It is in fact more accurate (although not quite so simple) to visualise the electrons in an atom as being spread out 'charge clouds' around the nucleus, with most of this charge being concentrated at specific distances from the nucleus. The comparison between the two points of view is made in Fig. 1.

The electrons within an atom can have different energies. If they obtain more than a specified amount of energy (for any particular type of atom), then they can actually break free from the atom. It is clear that the more energy a particular electron has within an atom, the less energy that electron will need to have added to it in order for it to break away from the atom; in other words, the easier it will be for that electron to escape.

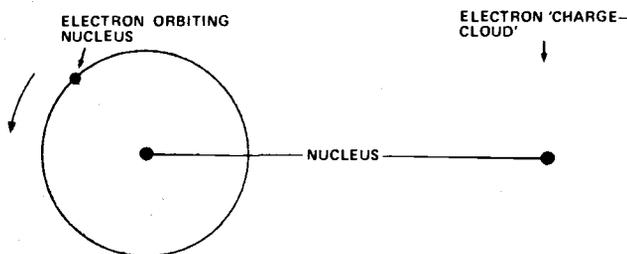


Fig. 1. A hydrogen atom according to (a) The 'Solar System' model (b) The 'Charge Cloud' model.

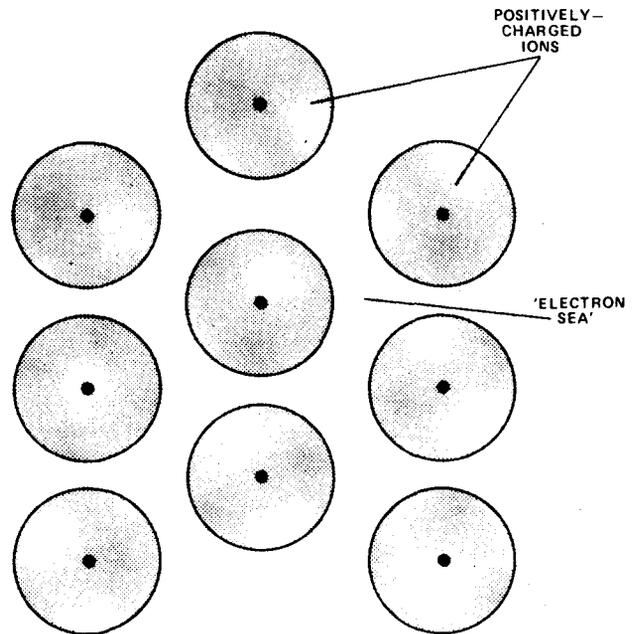


Fig. 2. The structure of a metal. Positively charged ions are surrounded by an electron 'Charge Cloud'.

Conduction and Insulation

But what has all this to do with conduction of electricity? In metals, some of the outer electrons present have quite high energies within their atoms and, in a solid lump of metal, one or two electrons from each atom are more or less free of their own atoms, although they are held into the metal as a whole. The positively charged ions left when electrons are removed from atoms are packed closely together and, in between them, the free electrons move about at random, (acting as a sort of 'atomic glue'). This negative charge attracts the remaining positive charge on the ions, and holds the whole thing together (See Fig. 2.) The charge clouds of all the free electrons join together, and form what is often known as an 'electron sea'. Because of this structure – the way that they are held together – metals can conduct electricity. Why?

What About Semiconductors?

Semiconductors are really an 'in-between' case. Like insulators, very pure semiconductors such as silicon or germanium have empty conduction bands when the temperature is 'absolute zero' (about minus 273°C), separated from the other energy bands by a forbidden gap. At normal temperatures the conduction bands are not

completely empty. Why? Because in semiconductors the forbidden gap is much smaller than in insulators – about 1 eV. It is so much smaller, in fact, that at normal temperatures, the vibration of the atoms in the semiconductor is sufficient to give enough energy to a few electrons to reach the conduction band. Eventually they fall back to the lower energy bands – but more electrons are entering the conduction band all the time, so eventually a balance is struck, with the number of electrons entering the conduction band in any period of time being equal to the number falling back. At normal temperatures, therefore, there are always just a few electrons in the conduction band of a semiconductor, and so it is able to conduct electricity. Though it conducts less well than a metal, since there are far fewer electrons in the conduction band.

But That's Not All

There is, however, another means by which a semiconductor can carry electricity. Every time an electron leaves a lower energy band for the conduction band, it leaves an electrically neutral space where there was previously some negative charge. These neutral spaces, surrounded by negatively-charged electrons, can behave almost like a positively charged particle, and when a potential difference is applied, this 'hole' as it is called, travels in the opposite direction to that of the electrons. To understand how this happens, imagine a row of chairs with someone sitting in each of them except the one at the end (Fig. 5). If the first person in the row moves into the empty chair, the next person moves into the chair left empty by the first person, and so on, the 'space' where no one was sitting appears to move in the opposite direction to the people, and that's exactly how it works with 'holes' in semiconductors. While it appears that the hole is moving in one direction, carrying positive charge, what is really happening is that the electrons in the lower energy bands are travelling in the other direction, carrying negative charge, and are moving into the spaces left by electrons which have gone into the conduction band.

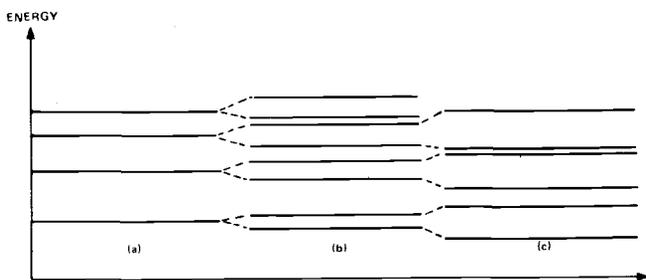


Fig. 3a. The electrons within atoms can exist only at set levels. b) When two atoms interact with each other, their energy levels are split. c) In a solid, millions of atoms all interact with each other, and the energy levels are split into so many 'sub-levels' that they behave like continuous bands.

Conclusion

Therefore, in a semiconductor, there are two types of charge carriers involved in the conduction of electricity; electrons and 'holes'. Various experiments indicate that in germanium, for example, about one third of all the current is carried by the 'holes'!

You will remember that, in semiconductors, electrons reach the conduction band because of the vibration of the atoms. This fact is quite important. At higher temperatures the atoms vibrate more, and so more electrons (and 'holes') are available for conduction purposes. To the extent that above about 100°C for germanium, and 150°C for silicon, the conduction is no longer really under control, and so devices like transistors, which use semiconductors, have to be kept below these temperatures, if they are to remain reliable during operation. The fact that silicon is useful as a semiconductor at higher temperatures than germanium, was the major reason for the increased use of silicon rather than germanium devices!

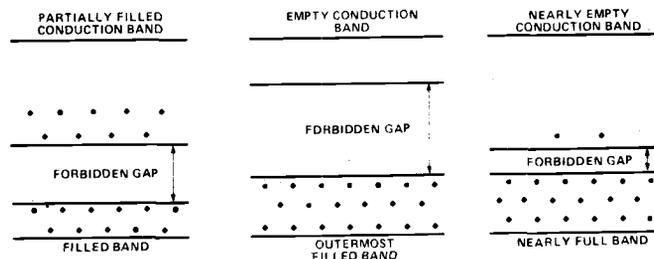


Fig. 4. Comparison of the forbidden gap position and magnitude in the three basic types of material. Far left: a conducting substance. The lower energy bands are full of electrons and the forbidden gap is easily bridged by sufficiently energetic electrons which then enter the conduction band. Centre: insulators. Note the empty conduction band and the wide forbidden gap in which there are no permissible energy levels. On the right: semiconductor materials in which the energy gap is around 1 eV and at room temperature sufficient energy is imparted by heat action to allow some electrons to cross the gap into the conduction band.

Because of all those free electrons, which aren't held by any particular atom, only by the metal as a whole. They are so loosely attached that if you apply a potential difference across the metal, they can drift along under its influence, and so cause a current to flow. In insulators, on the other hand, the electrons are held much more tightly by the atoms, there is no 'electron sea', and the atoms are bonded together by other means. Consequently, if a potential difference is applied, the electrons are unable to break free from their atoms, and so no current can flow. Our problem is thus solved – we now know how electrical current is conducted in metals, and why it isn't in insulators. Or do we? This theory was widely accepted for some time, and in fact it's still accepted as being broadly true, but there are just one or two things it doesn't explain – semiconductors, for instance? And why should metals hold their electrons less tightly than non-metals? Our theory is obviously incomplete.

The New Approach

. . . It was the physicists (naturally) to the rescue, so we must once again return to the atom . . .

In the first decades of this century, a startling new branch of physics, Quantum Mechanics, made its debut. This was the work of several men, including Einstein, Heisenberg and Schrodinger. One of the first results Quantum Mechanics produced was embodied in a conclusion that Niels Bohr published in 1913. This was that, contrary to

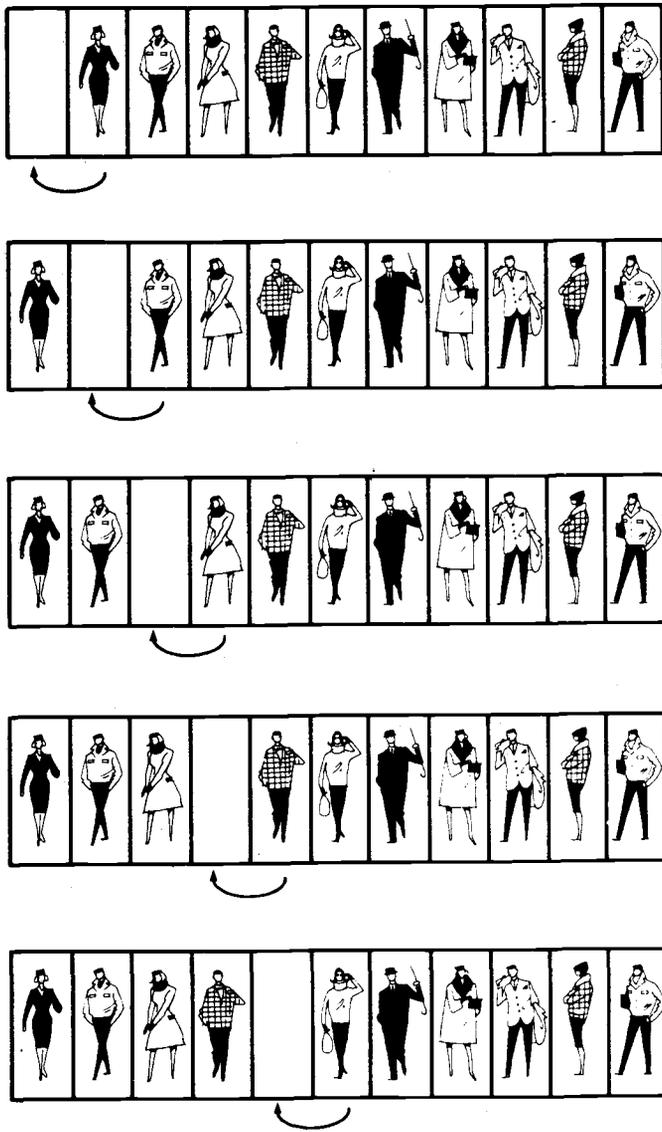


Fig. 5. As each person moves into the space next to them, it appears that the gap moves in the other direction. In the conduction band this is an electrically neutral space where there was previously a negative charge. These 'holes' can behave almost like a positively charged particle. When a potential difference is applied this 'hole' moves in the opposite direction to the electrons.

what had previously been assumed, the electrons within an atom could not have just any energy level, but could only exist at certain set energy levels (See Fig. 3a). This was a radical departure from what had been believed up until then, but it has been proved and is now unquestioned by physicists.

So electrons in atoms can only exist at certain set energy levels. But if you get more than one atom together, the situation changes again – energy levels are split. If, for example, you put two atoms close together and then look at what has happened to a particular energy level in each atom, you will find that, in one atom, it has shifted up fractionally; in the other atom, it has shifted down slightly. The two atoms act as though the single energy level has

been split into two (See Fig. 3b), one very slightly higher than the other. In a solid, where there are millions of atoms all together, the energy levels are split into so many 'sub-levels', all very close in energy, that they act like continuous bands (Fig. 3c). In a solid, instead of there being several separate energy levels at which the electrons can exist there are, instead, several energy 'bands' within which electrons can have a whole range of energy levels. Between these bands however – and this is the important bit – there are still 'forbidden gaps'; energy ranges in which electrons cannot exist because there are no allowable energy levels present. So how does all this help us to understand electrical conduction? Patience . . . we're just coming to that.

Electron Distribution

The way a material behaves electrically, whether it acts as a conductor or an insulator or whatever, depends on the arrangements of its energy bands, and the way that the electrons are distributed within them. The energy bands of a) a conductor b) an insulator, and c) a semiconductor are shown in Fig. 4. Firstly we will deal with the conductor. The energy bands shown in Fig. 4a are fairly typical of a material like copper. As in any material, the lower energy bands tend to fill up with electrons more easily than the higher energy bands, and consequently, they contain all the electrons that they can possibly hold. There is then a 'forbidden gap' of energies, and above this is another band known as the conduction band. This band, unlike those below it, is not full, but is capable of holding more electrons than it in fact does. An electron in this band is relatively loosely held by this atom and so it requires only a very small amount of energy, which can be obtained from an applied potential difference to raise it to a higher energy *but still within the conduction band*.

It can now drift along within the metal under the influence of the potential difference. Thus, in a metal, which has either a partially-filled conduction band (eg. copper) or an empty conduction band which overlaps a full energy band, (as in magnesium) it is possible for current to flow quite easily. So far, so good. What about insulators? The energy-band theory can also explain the behaviour of non-conducting materials (Fig. 4b). In such substances, there are still full energy bands at the lower energy levels, but the conduction band is empty. In other words in insulators, electrons do not normally exist with enough energy to be in the conduction band. And it is only in this conduction band that electrons are free enough to take part in a flow of electrical current. If it were possible to get the electrons out of the lower energy bands into the conduction band then these materials could conduct electricity, but in order for that to happen electrons would have to cross the forbidden gap, and the energy required to make them do this is much more than can be supplied by a normal potential difference. In terms of eV (the eV, or 'electron-volt', is a measure of energy which atomic physicist find it convenient to work with, 1 eV being the energy picked up by an electron in passing through a potential difference of 1 volt), the forbidden gap in insulators is normally about 5 eV, hence, under normal circumstances, insulators do not carry electricity.

A. Lipson

Chapter 17

BANDPASS AND BEYOND

A closer look at the development of bandpass design, switched capacitor techniques and some new ICs.

MANY MACHINES such as spectrum analysers and vocoders use analysing filter banks, these are often quarter octave devices extending over six octaves. If quarter octave filtering is to be successful then the bandpass filter responses must be very sharp, having almost flat tops and a fast roll-off slope at either side. A poor slope would mean that the filter bank would not be able to resolve incoming signals; for example a sinewave might give a high output in several of the channels. Also, a very peaky response would give large interfilter 'dips' in the overall response (Fig. 1). An approximation to the square ideal response can be obtained by using multiple tuned filters. The response of a single pole bandpass filter is shown in Fig. 2.

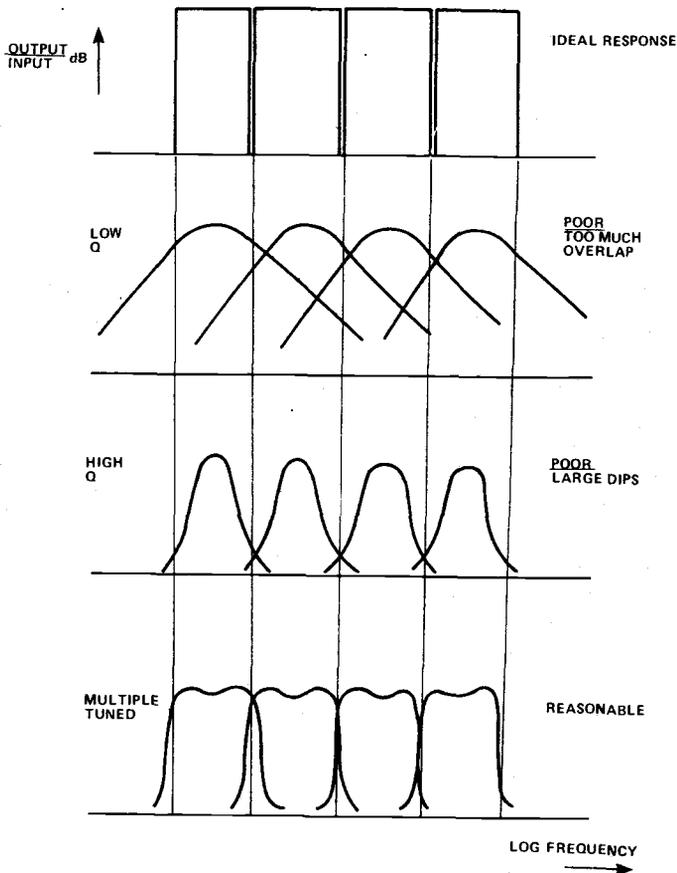
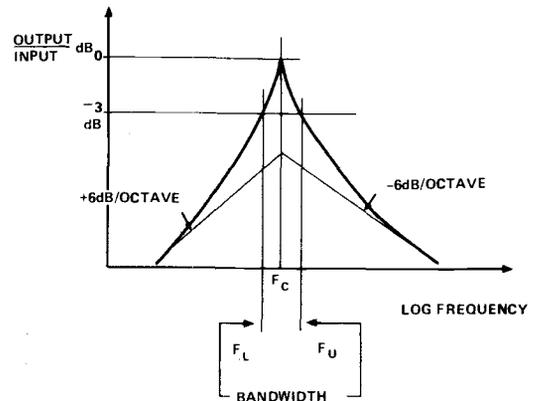


Fig. 1. Various responses of an analysing filter bank.



$$3\text{dB BANDWIDTH} = (F_U - F_L)$$

$$Q \text{ FACTOR} = \frac{F_C}{(F_U - F_L)}$$

$$\text{ALSO, } F_C \approx \sqrt{(F_U F_L)}$$

$$\text{FINAL ROLL OFF SLOPES} = \pm 6\text{dB/OCTAVE}$$

Fig. 2. Single pole bandpass response.

By Design

When designing bandpass filters it is important to decide what type of filters to use. Figure 3 shows two bandpass responses. Response A is a peaky filter, whereas B has a flat top to it, but still has the same roll off as A. One sensible design solution would be to use bandpass filters for A, and a highpass/lowpass structure for B. A rule of thumb for making this decision is to calculate the fractional bandwidth:—

$$\frac{F_U - F_L}{F_U + F_L}$$

If this is greater than unity, then use lowpass/highpass filters; if it is less than unity use multiple tuned bandpass filters. Some standard bandpass filter designs are shown in Fig. 4. The multiple feedback circuit requires only one op-amp, but is limited to low Q operation (less than 5) and the centre frequency and Q are interactive.

The state variable design can produce high Q factors of the order of several hundred. Tuning is performed by changing the R and/or C components. The Q factor is independently variable and is invariant with changes in frequency.

The biquadratic design is similar to the state variable filter. Tuning is performed by changing the R and/or C

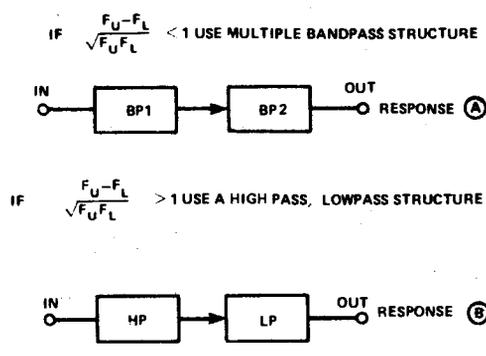
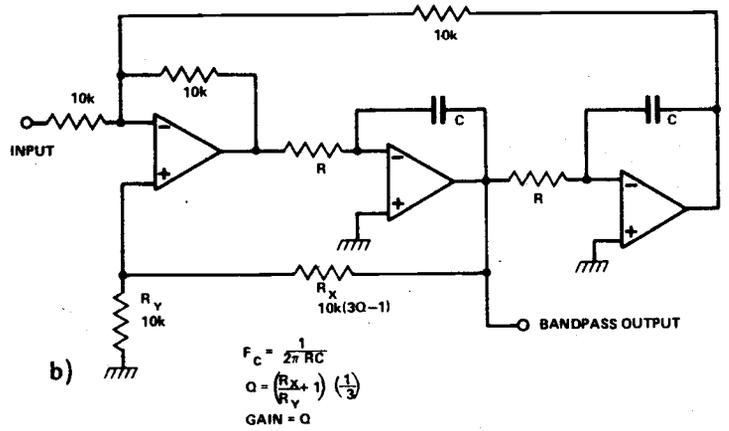
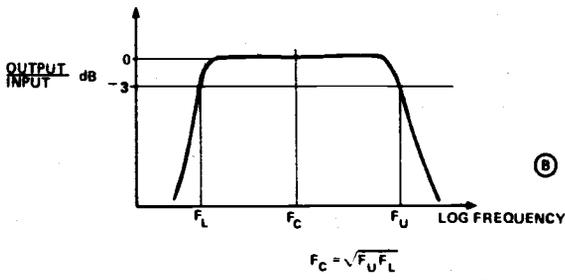
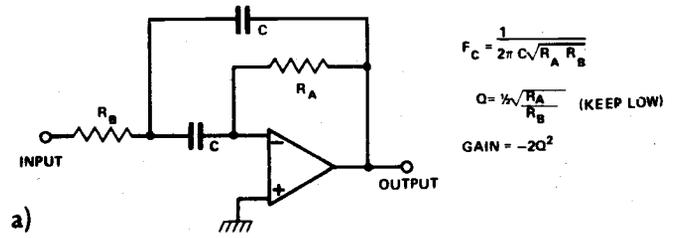
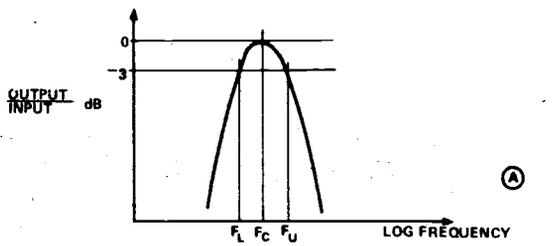


Fig. 3. Two bandpass responses and how to realise them.

components and the Q factor is determined by the ratio of R_q to R . As it is tuned to operate at higher frequencies the Q factor will increase linearly in proportion to that frequency.

A voltage controlled biquadratic filter is shown in Fig. 5. This employs the relatively new CA3280, which is a dual improved performance version of the CA3080. As the Q factor is a function of frequency, the useful operating range is about 20 to 1.

A simple analysing octave filter bank is shown in Fig. 6. This is implemented using double tuned filters with Q factors of five. The component values for two channels are shown in the table of Fig. 6a. Note that some compromises will have to be made in order to implement the design using low cost E24 resistors. For example, a 255k resistor could be made using two 510k resistors in parallel. The filter bank is converted into a spectrum analyser by adding an envelope follower to each channel and then multiplexing the envelope voltages into an XY display (Fig. 6c).

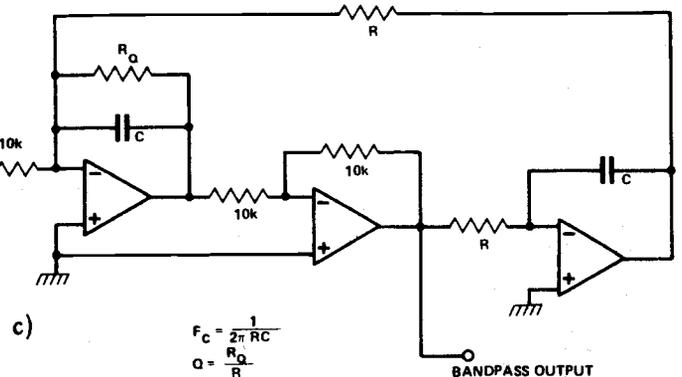


Fig. 4. Standard bandpass filter designs. a) Multiple feedback. b) State variable. c) Biquadratic.

Other Design Applications

Figure 7 shows a design for a parametric audio equalizer. This device has variable cut and lift and a resonance and frequency control. The resonance control is arranged such that as the Q increases, the input signal is attenuated (RV2a), thus maintaining the same overall gain at resonance, independent of the Q setting. The filter is a state variable design which is situated in the feedback/feedforward loop of an op-amp. Thus RV3 controls whether overall response is a bandpass cut or lift. The resonant frequency is tuned by RV1 and SW1 is used to switch frequency ranges. The Q factor is set by RV2.

The TCA580N (Signetics) is an IC that can be used to simulate an inductance and in doing so may be used to synthesize many conventional LCR filter circuits (Fig. 8). The device has a pair of floating input terminals which generate the impression of being an inductor. This inductor is programmed by three passive components, R_{G1} , R_{G2} , C_2 .

By connecting a capacitor (C_1) across the input terminals, a parallel resonant circuit (C_1L) is produced.

Moving Story?

The SSM2040 is a four section mobile filter that can be exponentially voltage-controlled over a 10,000 to 1 frequency range. The device contains an exponential function generator that controls four variable transconductance amplifiers each having their own output buffers. The IC may be used for electronic music synthesis, musical effects, tracking filters and many other applications where filter mobility is needed.

A four pole lowpass filter for electronic music is shown in Fig. 9. Each stage is a single pole mobile lowpass filter, four of these filters are connected up in cascade and fed into an output amplifier. A resonance feedback route is provided so that the Q factor may be manually controlled. The voltage control of frequency is set to -1 V/octave.

By modifying the external components, the device can be transformed into an all pass filter (Fig. 10). This filter has a flat amplitude response and a phase shift that changes by 180° as a function of frequency. As the SSM2040 has four stages, the whole filter has a variable 720° phase shift. When the filter output is mixed with the original signal, two notches are produced in the frequency response occurring when the phase between the original and phase shifted signal is 180° and 540° .

As the phase shift is slowly modulated up and down in frequency, the notches also move producing the characteristic phasing sound.

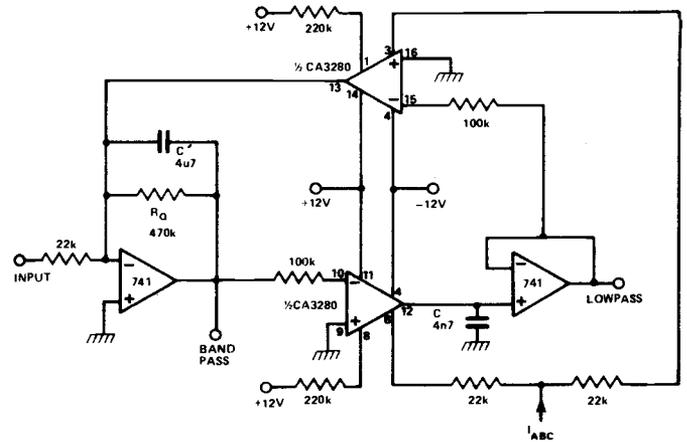


Fig. 5. A voltage-controlled biquadratic filter. Note that the CA3280 has two $+12$ V supplies (pins 14 and 11) but only one -12 V supply (pin 4). (We don't know why either.)

R_A	R_B	C	F_1	Q	R_C	R_D	C	F_2	Q	
3k8	360k	15n	290Hz	5	5k1	510k	15n	205Hz	5	FILTER D
1k8	180k	15n	580Hz	5	2k55	255k	15n	410Hz	5	FILTER E

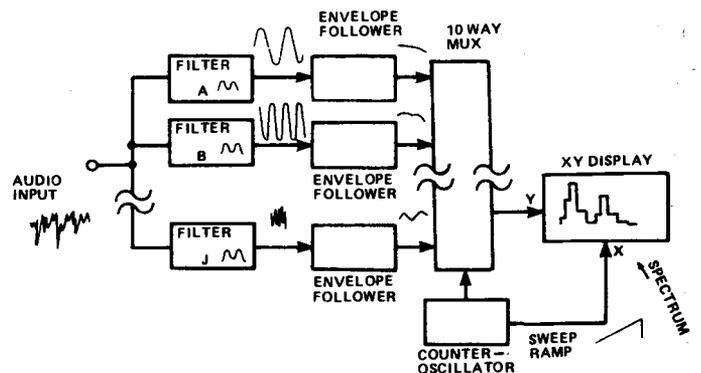
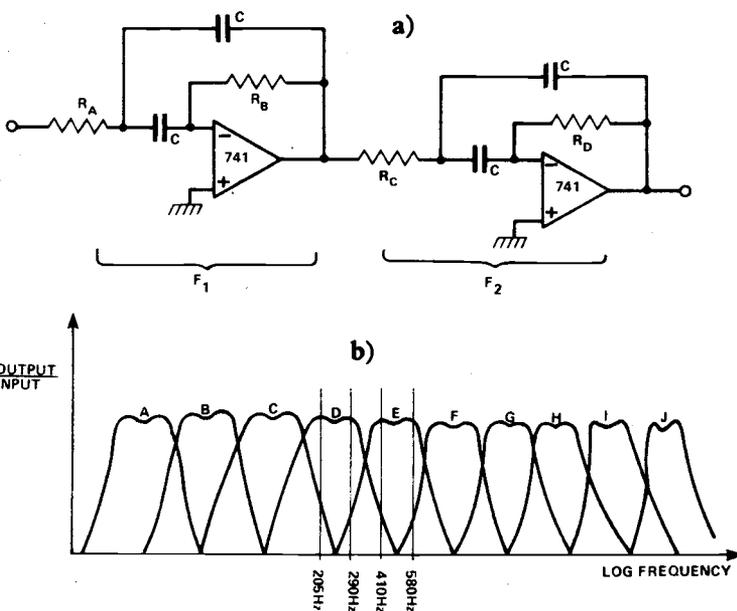


Fig. 6. An analysing filter bank suitable for a spectrum analyser. a) Circuit for each of the ten filter stages (A to J), and component values for two of the stages. b) Graph of the ten filter responses. c) Block diagram of the spectrum analyser and a suitable circuit for the envelope follower.



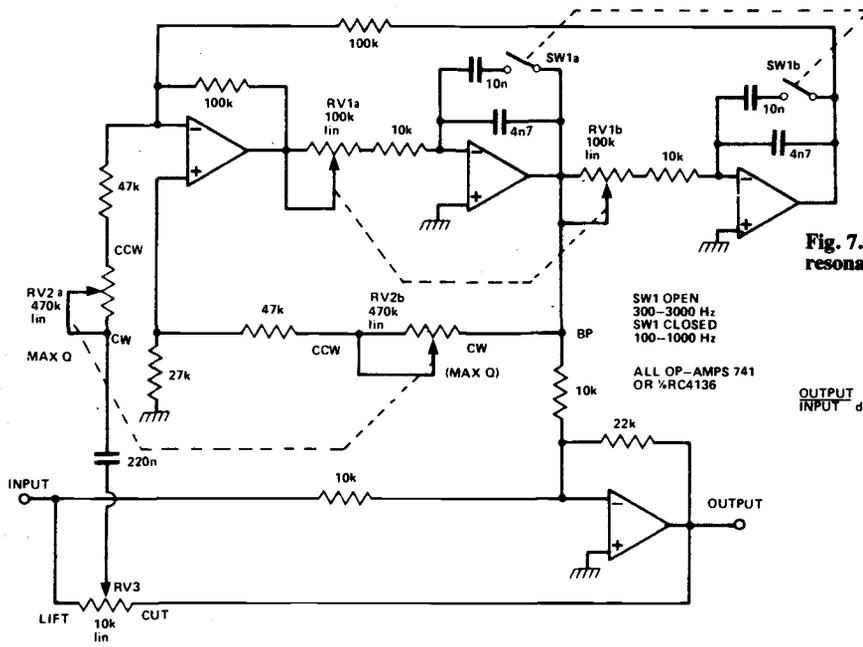
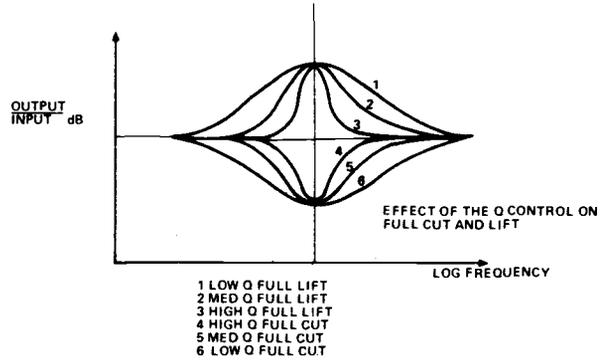


Fig. 7. A parametric audio equaliser with variable cut and lift and a resonance and frequency control.



Monomania

Monolithic filters are becoming more and more common. One such device that lends itself to integration is the transversal filter (Fig. 11a). This device can produce a steep roll-off slope, a high out-of-band attenuation and most significantly a linear phase response. The transversal filter is a tapped analogue delay line. The input signal is sampled and this sample moves down along a bucket brigade delay line. Each bucket has a separate output so that the signal may be monitored at each stage via a weighting resistor. It is possible to weight the resistors such that they draw out the impulse response of the required filter performance.

When fed with an input signal that is being shifted down a delay line, this impulse response results in it being converted into a frequency response. The filter frequency is directly linked to the clock frequency, and thus it is impossible to make the transversal filter mobile.

It is necessary, as with all sampled data systems, to precede the device with an antialiasing filter and to recover the signal. There are now several transversal filters available, but they are still relatively expensive and are best used only where linear phase response is of prime importance.

Recent Monos

A more recent monolithic device is the switched capacitor filter, which can be used to implement many standard lowpass and bandpass filter structures (Fig. 12). The problem with producing monolithic recursive filters is that stable high tolerance components such as resistors and capacitors are very difficult to make, and the filter performance depends heavily upon these tolerances. However, it is possible to simulate resistors with switched capacitor techniques. With the switch as shown in Fig. 12a, C_1 is charged up to V_1 . When the switch is thrown to its other position the capacitor is discharged into V_2 . By continually switching the switch, a current I can be made to pass from V_1 to V_2 . This simulates a resistance R (where R equals the period of the switch divided by C_1). The switching is performed by two MOSFETs (Fig. 12c) driven by antiphase clock signals.

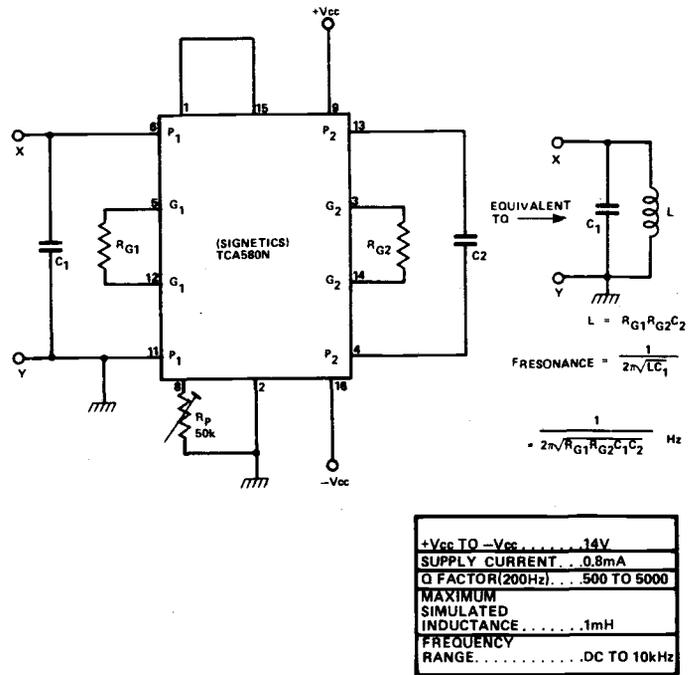


Fig. 8. A monolithic gyrator using the TCA580N. It can simulate inductances up to one millihenry.

The simulated resistor can be used to construct an integrator (Figs. 12d,e) which can then be used to build up conventional filter structures. For example, a state variable filter would have a resonant frequency F_c where

$$F_c = \frac{1}{2\pi RC_2}$$

$$\text{but } R = \frac{T}{C_1}$$

$$\text{therefore } F_c = \frac{C_1}{2\pi C_2 T}$$

Note that F_c is linearly proportional to $1/T$, which is the clock frequency.

Reticon make a switched capacitor bandpass filter which contains three filters at one-third octave spacing, thus making filterbank design relatively simple (Fig. 13). Maybe in a few years' time it will be possible to purchase a wide range of low cost monolithic filters.

Tim Orr

Fig. 9. A four pole lowpass filter using the SSM2040. The transconductance amps are labelled G and their output buffers B.

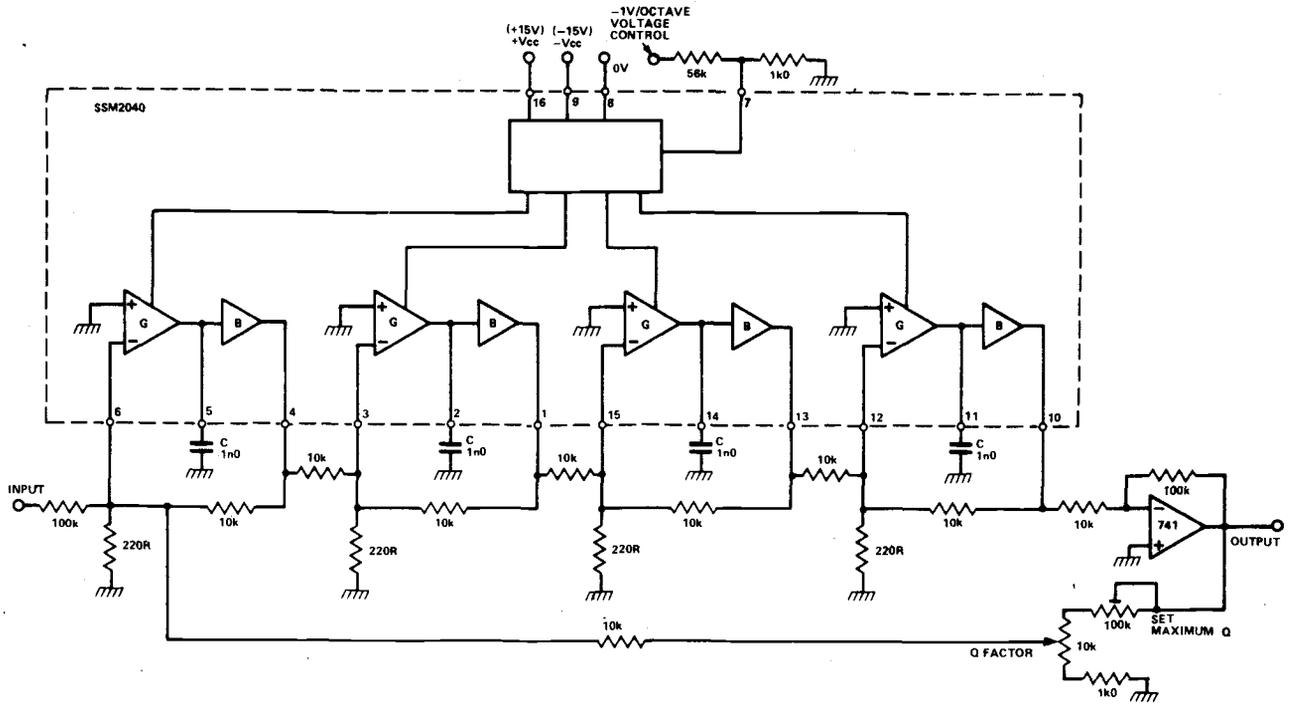
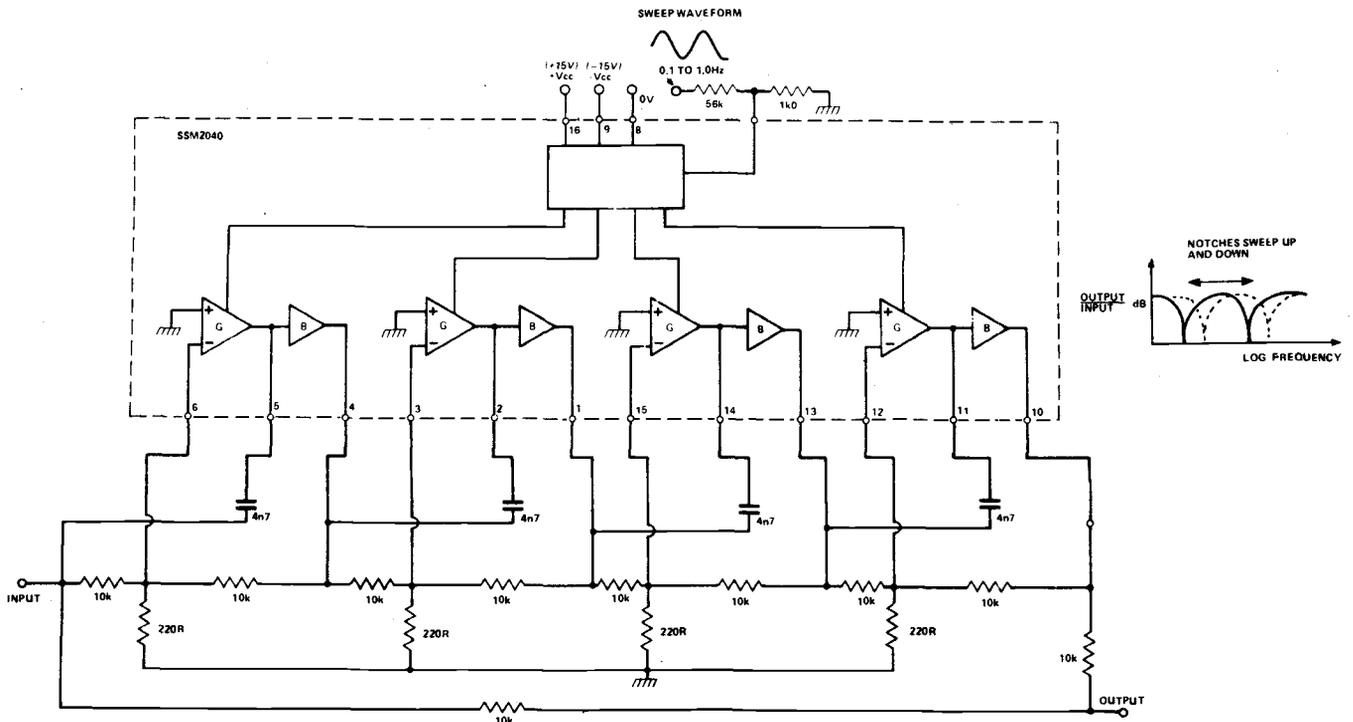


Fig. 10. The SSM2040 connected as a two-notch phasing unit.



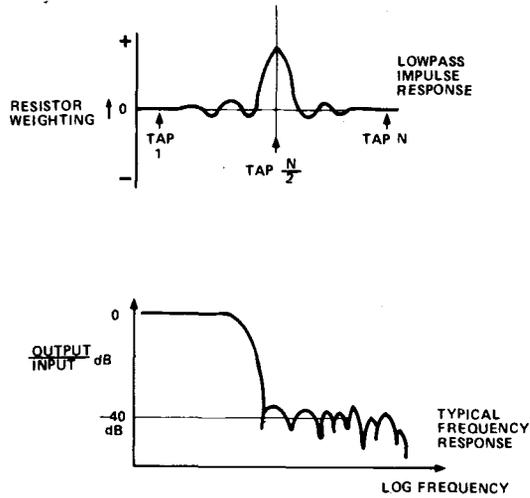
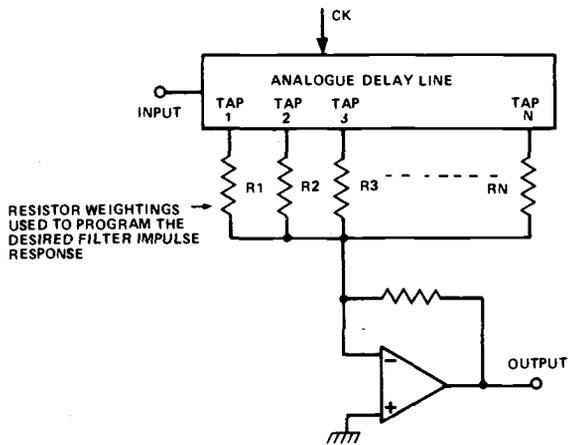


Fig. 11. The transversal filter, with graphs of impulse and frequency responses for a lowpass design.

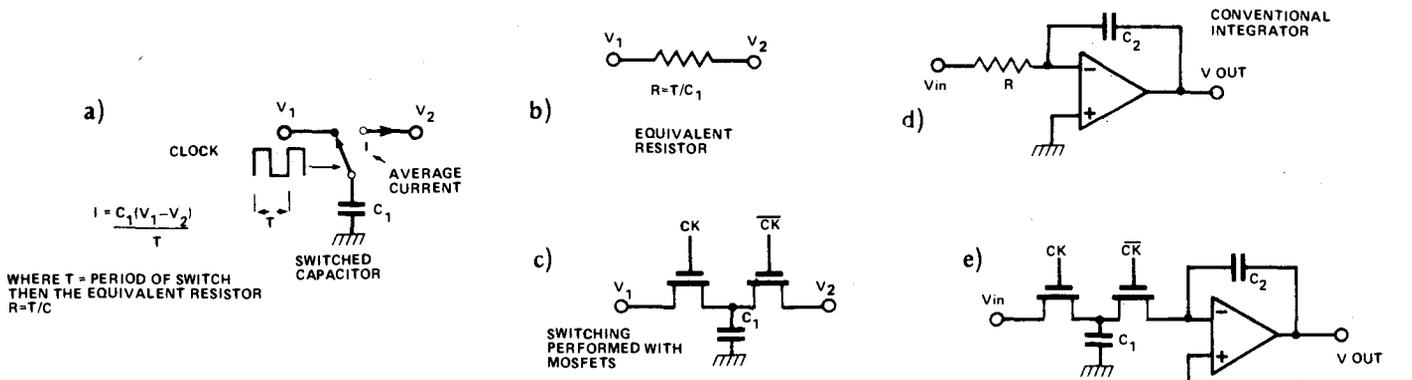


Fig. 12. Switched capacitor filters. a) Basic circuit. b) The equivalent resistor. c) Practical design using MOSFETs. d) Conventional integrator. e) Replacing R with a switched capacitor enables a filter to be easily produced in IC form.

SPOT DESIGNS Crystal Set

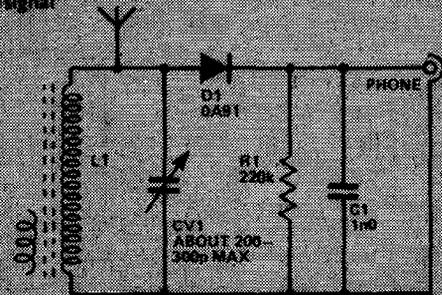
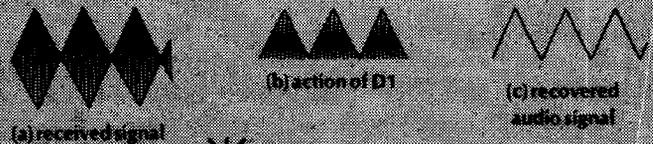
THE MOST SIMPLE form of radio for receiving broadcast stations is the crystal set, or more precisely, a modern equivalent using a semiconductor diode to provide detection. This simple set covers the normal medium wave broadcast band, has an output for a crystal earpiece and, in most cases, should give reception of Radios 1, 2 and 3 at reasonable volume (plus any local radio stations where these are in operation on the medium waveband). It requires no battery or other form of power source since energy derived from the received transmission is used to drive the earpiece. However, this does bring the disadvantage of needing an external longwire aerial to operate the set, as an ordinary ferrite aerial does not give sufficient pick-up.

The tuned circuit is formed by L1 and CV1. This selects the desired transmission and rejects other stations. CV1 permits full coverage of the normal medium wave broadcast band to be achieved. In order to obtain good volume from the main it is necessary to directly couple the aerial to the tuned circuit. For the same reason it is necessary to take the output to the detector direct from the tuned circuit. This inevitably gives the set rather poor selectivity, but it should still be adequate in this respect.

The form of modulation used on the medium wave band is AM (amplitude modulation). This consists of varying the strength of the RF signal in sympathy with the amplitude of the modulating audio signal. D1 half wave rectifies the RF signal to leave only the positive half cycles. R1 and C1 are used to smooth the RF half cycles, but their time constant is too short to produce a steady DC output. Instead the output rises and falls in sympathy

with the mean RF signal level, so that the original audio signal is recovered at the output and fed to the earpiece.

The only adjustment the finished unit requires is to slide the aerial coil (L1) along the ferrite rod to find a position that permits full coverage of the medium wave band. The coil is then taped or glued in this position. The smaller winding of the ferrite aerial is not required and is either removed or just ignored. The aerial should preferably be an outdoor type about 10 m or so long, but a few metres of hook-up wire fixed around the walls of a room or in a loft should give reasonable results.



Chapter 18

HEISENBERG'S UNCERTAINTY PRINCIPLE

It affects all aspects of electronics. It is a fundamental concept as basic as ABC to a physicist. Here is the easiest way to find out more about it.

MOST PEOPLE WHO READ a lot of science fiction have probably heard of Heisenberg's Uncertainty Principle at some time or other, but the vast majority are (pardon the pun) very uncertain as to its nature. Well, never fear; a paragraph or two hence you, too, will be able to confuse friends, relatives and the cat. . . .

Exactly Where?

The uncertainty principle as such was first stated by a German physicist, Werner Karl Heisenberg, in the late 1920s. He said, essentially, that it is *impossible to measure both the position and momentum of a particle simultaneously*. Now this wasn't quite such a stupid statement as it sounds. What he actually meant by this was that, in measuring either the position or momentum of a particle, you must necessarily be affecting the other in a way which is unpredictable and, in the case of small particles such as electrons, significant. At this point the reader may feel inclined to cry out 'Ah, but I can tell exactly where something is just by looking at it and that doesn't affect its momentum, does it?'. Well, sorry to disappoint you, but you're wrong on two counts. You cannot tell *exactly* where something is just by looking at it – there is a slight uncertainty of the order of the wavelength of the light you are using – and even looking at a thing *does* affect its momentum. Light, you see, is made up of particles. In order to look at an object, it is necessary to bounce some light particles (called photons) off that object. Now these particles carry momentum, and so when they bounce off the object, they must necessarily change its momentum, as well. For normal objects, as large as the ones we're used to, this doesn't make a lot of difference, but if you start working on the atomic scale, with electrons, etc, then a photon or two can make a lot of difference. Before we say any more, let's have a look at the basic equation that Heisenberg actually used. (No need to get worried, it's the only equation we'll see . . . and isn't all that difficult to understand.)

$$\Delta p \times \Delta x \geq h/2\pi$$



Chapter 19

ATTRACTIVE AMPS(?)

Exploring the all too frequently ignored and misunderstood field of Magnetic Amplifiers.

THINK OF AMPLIFICATION, and you automatically think of transistors. Perhaps if you're a bit longer in the tooth you remember valves. Have you ever thought of large amounts of power gain being obtained without using either transistors or valves? It's power gain we're talking about, too, not just voltage gain. A transformer will give voltage gain, up to 100 times, but at the expense of current, so that the power out is never quite as much as the power in. There's no *Power* gain there, but a device called the magnetic amplifier, which looks very like a transformer, can give very large values of power gain, can control AC power into a load very smoothly, and is used in the sort of applications where thyristors would be a natural choice for many.

The magnetic amplifier has been used in industrial control for decades, yet has never really caused any stir of interest anywhere else. Perhaps it's because it's always a ready-made item, but then so is an IC amplifier, and everyone seems to make use of those. Perhaps it's just because so very few people outside the ranks of professional engineers know just what a magnetic amplifier is. Let's remedy that!

Induced Knowledge

To start with, we need a pretty clear idea of what happens inside an inductor. A simple inductor has a winding which consists of insulated wire wound round a core of a soft magnetic material. Soft doesn't mean that you can spread it on your bread, but that the material magnetises easily, and demagnetises just as easily. Take a piece of this material, hold a magnet near it, and it's magnetised. Take a magnet away and it's demagnetised. This material we use for the cores of inductors, transformers, electric motors, relays, etc.

An inductor makes use of this 'soft' magnetism. The winding has an alternating current flowing in it. This alternating current (changing smoothly from a peak in one direction to a peak in the opposite direction and back) causes the core of the inductor to magnetise. The magnetism isn't steady like a bar magnet, but alternating, which is the point of using soft magnetic material. A graph of the magnetism (called flux density) of the core plotted against time would, ideally, have exactly the same shape as that of the waveform of the AC applied.

So far so good – it's an alternating magnet. But we've known for about 150 years (or someone has) that wherever

there's an alternating magnetic field, any piece of wire or other metal will have an alternating voltage induced.

Stick a piece of wire near your alternating magnet and you'll find an alternating voltage across the ends of the wire. The voltage is small if you use just a few centimetres of straight wire, but if you wrap several metres or wire round the core, so that all the magnetism of the core is at the centre of the coil of wire, then you find quite a respectable amount of AC. Recognise it? It's a transformer.

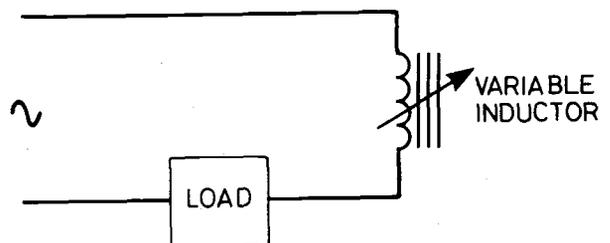


Fig. 1. Control of a load using a variable inductor, this configuration has very little power lost as heat, unlike a resistive controller.

Laying Down the Laws

The laws of Electricity are very consistent, though, *any* coil of wire around a core that has an alternating magnetic field will have an AC voltage induced. That means that if we have only one coil, and we send AC through to generate the magnetism, it will *also* have an AC voltage induced in it. This voltage which the text books call a "back EMF", opposes the current which causes the magnetism which causes the voltage. It's a darn sight more difficult to pass AC through an inductor than it is to pass DC!

When we use an inductor in a DC circuit, then apart from some effects at the moments of switch-on and switch-off the thing behaves like a resistance, good old Ohm's Law and all the rest, and a fairly low value of resistance at that.

Now you might think that it should pass the same amount of current for AC as for DC, but it doesn't. Imagine that the resistance of $2R$, so that 10 V DC passes 5 A. Apply 10 V AC and the current's nothing like 5 A. It's not because Ohm's law stops working, it's because of the induced voltage. We're trying to push AC through with one voltage and the induced voltage is opposing our efforts. It's only the difference between the two voltages that has any effect at all.

Impedance Impediment

Suppose for example that with 10 V AC applied, the induced voltage is 9V9. This makes the difference equal to 0V1, and the current is

$$\frac{0.1}{2} = 0.05 \text{ A, (by Ohm's Law)}$$

Now these are calculations we seldom bother to make. Instead we measure a quantity called the inductance, L , of the coil and use this quantity and the resistance value to calculate impedance, which is the ratio

$$\frac{\text{AC voltage}}{\text{AC current}}$$

for the coil. In our example, 10 V causes 0.05 A flow, making the impedance $10/0.05 = 200 \text{ R}$, not a particularly large impedance, but much greater than the resistance of 2 R.

The useful thing about an impedance is that there's practically no loss of power in it. Pass a current through a 200R resistor, and you lose energy in the form of heat the amount of heat lost per second is $200 \times (\text{current})^2$ joules for a 200 R resistor. The same current through the inductor in our example doesn't look anything like this — only its resistance loses heat, and that's only $2 \times (\text{current})^2$ joules, because the resistance is only 2R.

We can therefore use an inductor to control the flow of AC in a circuit (see Fig. 1) with none of the power loss that a resistor would cause. Now if we could just have a variable inductor, we could very neatly control the flow of current in that circuit. Of course, we could use an inductor with tapped turns and slide contacts, built like a potentiometer, and we make use of just such a device, the familiar Variac. It's possible though, to control the inductance of a winding with no mechanical movement at all, and what makes it possible is the effect called saturation.

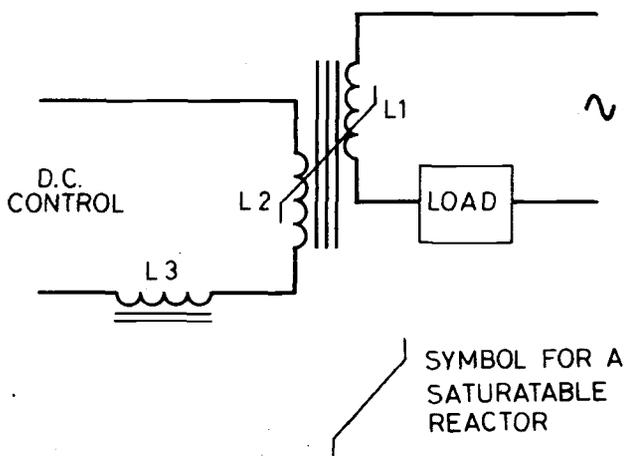


Fig. 2. Simple magnetic amplifier circuit showing DC control winding.

Control-A-Coil!

When we send a current, AC or DC, through a coil of wire which is wound round a magnetic core, we can't pass as

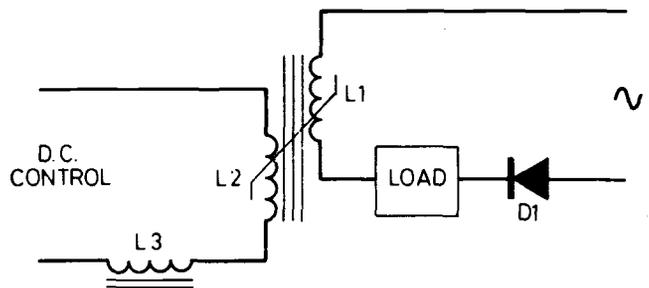


Fig. 3. Half-wave control using self-saturation.

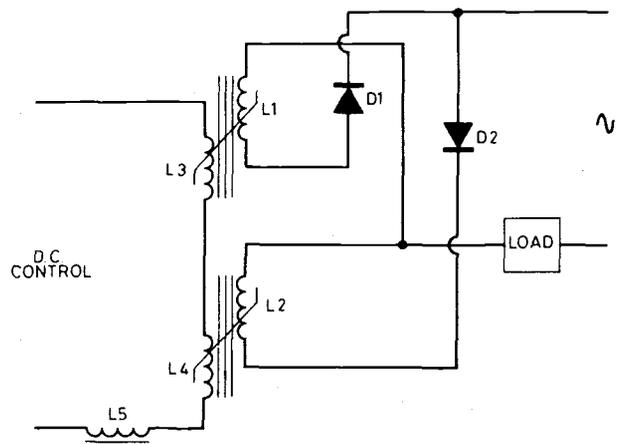


Fig. 4. Full-wave amplification with self saturation, by positive feedback.

much current as we like and expect the magnetism to keep pace. At some stage in the game the core saturates, which means that it's as magnetised as it's ever going to be, no matter *how much* current is used. Now when a core is saturated like this, a change of current doesn't cause a change in the magnetism so there's no more induced voltage. In other words, the inductance is no more and the impedance is practically zero.

Let the AC flow to its load through an inductor whose core we can cause to saturate. How? By passing DC through another winding, by making the core of material which saturates easily, and making the core continuous with no air gap.

That's our recipe for a magnetic amplifier.

Amps For Amps

Figure 2 shows a simple magnetic amplifier circuit. The inductor L1 has a large inductance when the core is not saturated, because of that, its impedance is very large, enough to make the current in the circuit very small. Now let DC flow through the second winding L2, and the core saturates.

If we can keep the core saturated for the whole of the AC cycle, then the inductance of L1 is almost zero, and the full amount of AC current flows through the load.

We don't of course, have to switch between saturation and no-saturation. We can adjust the control current so that the core saturates only on half of the AC cycle, or in peaks so that the average current through the lead is controlled.

Self Satisfied

Even such a simple magnetic amplifier has a lot of advantages, such as low power dissipation and high power gain, but better results are possible by using what is called a self-saturating design. Self-saturation is a form of positive feedback, using some of the signal current to assist the DC control current. Figure 3 shows a half-wave self-saturating circuit. The rectifier D1 ensures that only one direction of current flows through the coil L1 and the rated load current will cause the core to be close to saturation. The DC control current in winding L2 need only be quite small to cause the core to saturate on peaks, so that less power is needed to control the load current, and power gain is much higher.

Only half cycles are passing into the load, however, so that a full wave version is more desirable.

A full-wave self-saturating magnetic amplifier is shown in Fig. 4. Two sets of windings are used, each handling half of the wave, with rectifiers ensuring that the AC wave is split into its two halves.

In all these circuits, an additional inductor is used in the

DC control line to prevent AC appearing in the control circuit because of transformer action.

Going Straight

DC amplification is simple enough — just rectify the output of the magnetic amplifier (the full-wave self-saturating type already has two rectifiers included in the circuit and only two more are needed). More sensitivity? Add another winding to pass DC bias current, and the sensitivity increases because the bias can be set so that the core is very close to saturation.

Nothing could be *that* perfect, there has to be a snag somewhere, and response time is it for magnetic amplifiers. Being slow beasts, a sudden change of control signal may not cause much change in the output current until several cycles of AC have passed through. Nevertheless for stabilising AC supplies, for control of large AC loads and for high power gains magnetic amplifiers are not so easily displaced by electronics. There's not much to go wrong, they can be built to order, and they can be repaired.

Ever tried to put a new junction into a thyristor?

K. T. Wilson

MOST POWER SUPPLIES incorporate some form of protection circuitry so that an excessive output current cannot flow in the event of an overload. However, these protection circuits are often designed merely to prevent the supply circuitry from sustaining damage, and in the event of an overload, permit a level of current flow that is sufficient to damage the circuit being powered. This overload current trip can be used between the powered equipment and the power supply and will cut off the supply almost instantly if a pre-set threshold current is exceeded. The trip current can be varied from just a few to a few hundred millamps. The unit will work with supply voltages of 5 to 40 V.

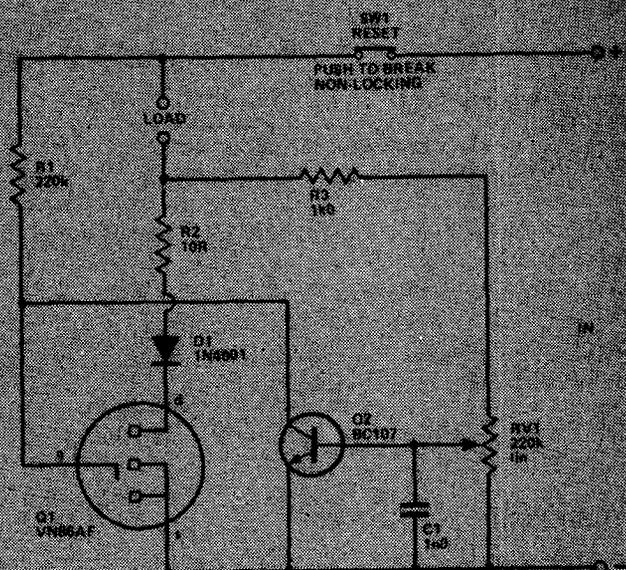
When power is first applied to the circuit, power FET Q1 will be biased into conduction by bias resistor R1. Power is, therefore, supplied to the load via Q1, D1 and R2. There will be a voltage drop across these components, and to some extent this varies with changes in the supply current. At low output currents there is likely to be a voltage drop of something in the region of 0V7, but this increases to a volt or so at high currents.

RV1 is adjusted so that at output currents below the required threshold level the proportion of the voltage dropped across Q1, D1 and R2 (and fed to Q2's base terminal) is not sufficient to switch on Q2. If the threshold current is exceeded, the voltage fed to Q2's base is then adequate to switch the device on and it diverts the bias current that formerly went to Q1's gate terminal. Q1 then switches off and cuts the supply to the load. Q2 remains switched on as it receives a strong base bias from the positive supply through the load, current limiting resistor R3 and RV1. Once tripped, the circuit thus latches in the "off" state. It can be returned to the "on" state by clearing the overload and then briefly operating SW1 so that the supply is momentarily disconnected from the unit. When the supply is restored it then starts at the "on" state once again. C1 ensures that the circuit does not always initially assume the correct state and it also helps to prevent spurious triggering of the unit.

When using the unit it should be kept in mind that about 1 V is lost through the device and the output voltage from the supply must be adjusted to compensate for this. The current trip inevitably causes some loss of regulation efficiency, but this is only marginal. If the unit is to have a trip current of about 100 mA or more, R2 can be reduced to about 1R6 in order to maintain the low voltage drop and marginal degradation of regulation efficiency.

SPOT DESIGNS

Overload Current Trip



Chapter 20

THE 1537 VCA

Some background information on this offspring of the silicon chip family – complete with practical applications.

THERE IS ALWAYS a great deal of excitement generated in electronics on the arrival or introduction of a new circuit, concept or chip, particularly if the system is potentially a field leader. The 1537A chip is just that! The specifications which the device can offer in situ are well above those of any similar preceding systems. Table 1 gives a listing of specifications, which can be obtained in the correct applications.

Parameter	Specification
Bandwidth	DC-200 kHz
T.H.D., 20 Hz-20 kHz	0.004%
I.M.D. (SMPTE TEST)	0.03%
Noise	-90 dBv, ± 1 dB (worst case, unity gain)
Overshoot and Ringing	None
Slew Rate	>10v/usec, symmetrical & constant
Input Impedance	20 K Ω
Maximum Input Level	+20 dBv
Gain	0 dB (Unity)
Maximum Attenuation	>94 dB
Control Voltage	0 to +10 V
DC shift vs. Attenuation	≤ 5 mV
Power Requirements	Regulated ± 15 V at +25, -33 mA

Table 1. The maximum possible specifications available from a 1537A system.

With harmonic distortion of 0.004% and a signal/noise ratio of over 90 dB the system is of course well suited to studio applications, although use in this environment is by no means its only area of involvement. The IC itself seems at first glance, somewhat highly priced, but nevertheless, it requires few extra components to produce a VCA system of the superb quality (suggested in the specifications of Table 1) and overall represents good value for money to the amateur and professional engineer alike.

Amplifier Or Attenuator

The term VCA is normally used as an abbreviation of the phrase *Voltage Controlled Amplifier*, but in its simpler modes the 1537A is, strictly speaking, a voltage controlled attenuator, ie with a maximum gain of unity. The inventors do, however, stress that connection of the 1537A into the feedback loop of an amplifier (such as an op-amp) produces a voltage controlled amplifier. The applications section of

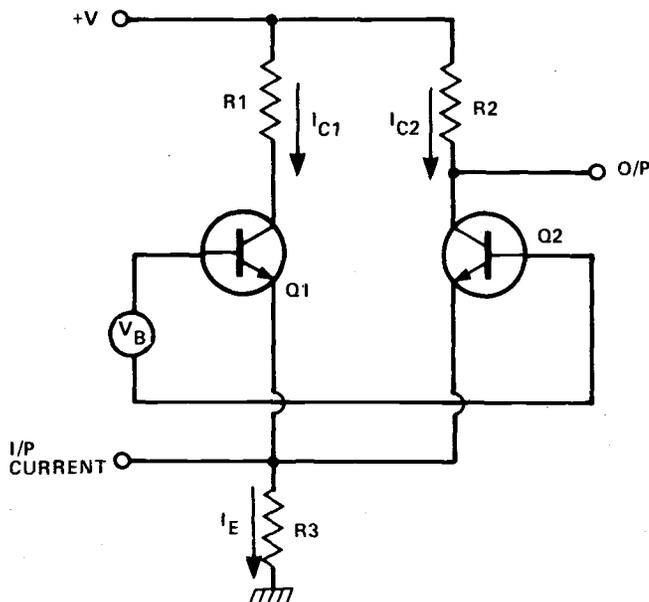


Fig. 1. A differential pair of transistors – the basis of a VCA.

this article show how this can be achieved. The operation of the 1537A VCA depends upon the gain control function of a differential pair of transistors as in Fig. 1. The transistors in Fig. 1 are connected at their emitters. The current through R3 (I_E) is, therefore, approximately equal to the sum of their two collector currents I_{C1} and I_{C2} through R1 and R2 respectively. The relative bias voltage, V_B , between the two bases determines the relative collector currents. If we now apply an input signal current to the joined emitters we obtain output signal currents through R1 and R2, the sizes of which are determined by the bias voltages. In other words, by altering this bias voltage we alter the size of the output signals.

Figure 2 shows a simplified internal circuit of the 1537A chip giving pin numbers and external load and emitter resistors necessary for operation. There are two basic gain control circuits within the chip, similar to that in Fig. 1 (built around Q1, 2 and Q5,6) except for three main differences:

- the diode connection of the transistor pair not used for signal output, ie Q1 and Q6, which reduces the distortion due to transistor gain differences.
- the addition of buffers around Q4 and Q8 to reduce loading for the output collectors of the gain transistors, in turn allowing idealised characteristics over the full gain range.
- the use of transistors Q3 and Q7 as voltage to current converters enabling the input to be applied as a voltage rather than as a current.

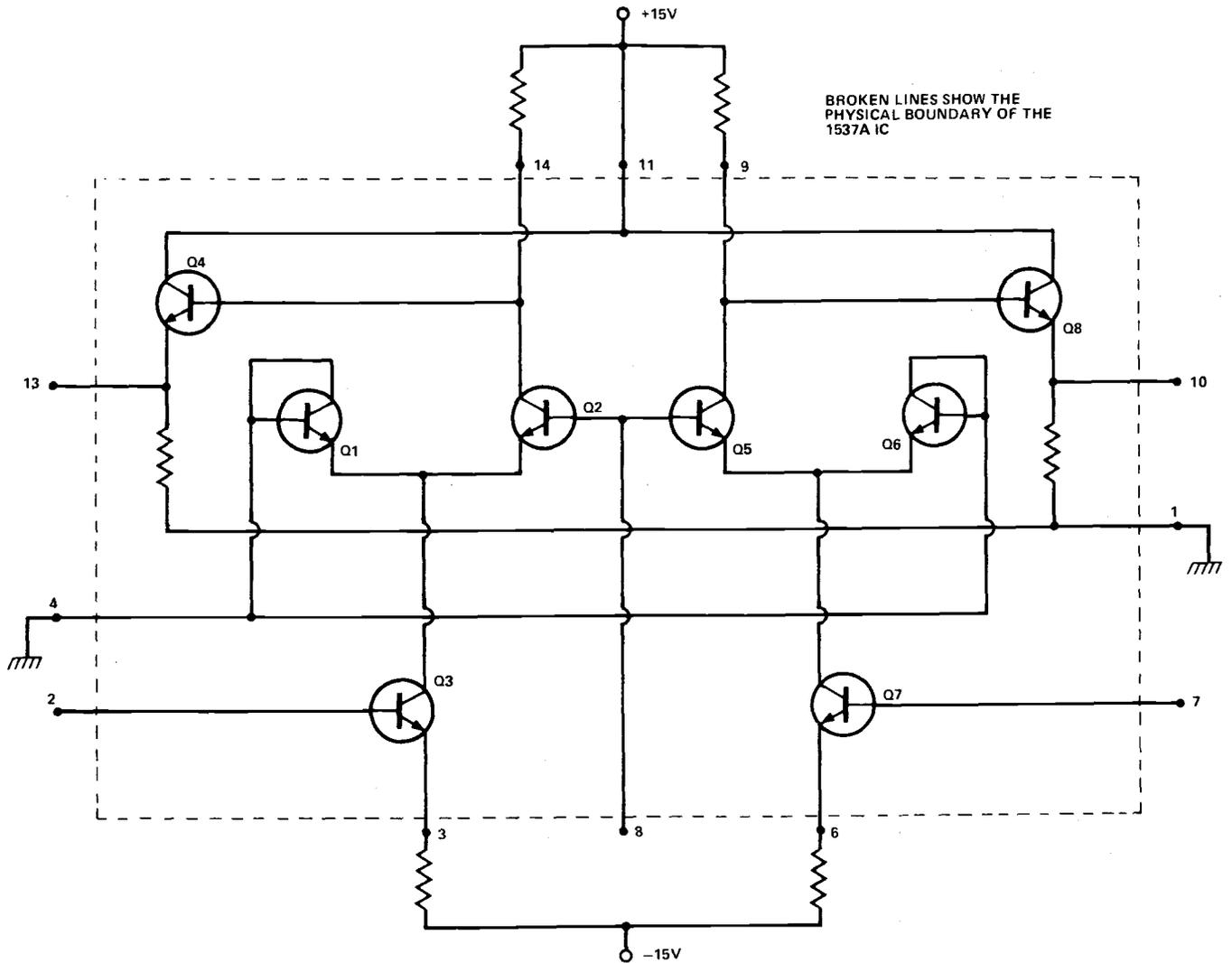


Fig. 2. A much simplified internal circuit of the 1537A IC, showing external load and emitter resistors.

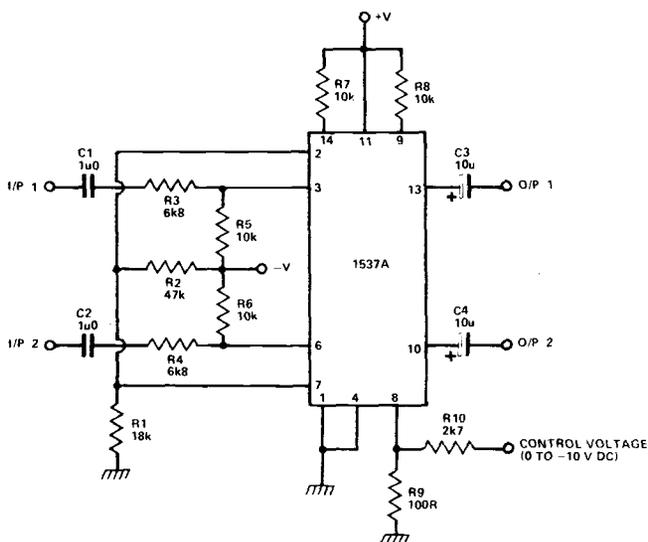


Fig. 3. The simplest mode of operation of the 1537A - a low input impedance stereo VCA with a negative going control voltage.

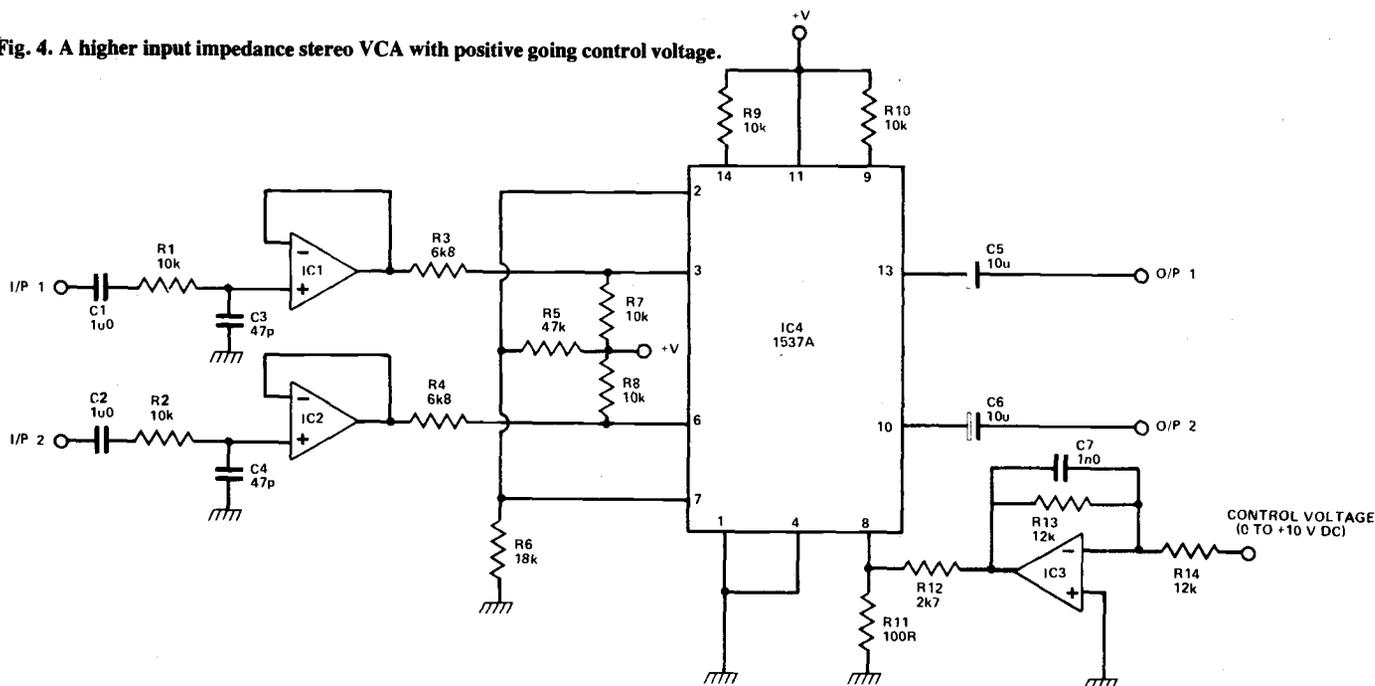
There is, however, a much more subtle difference, on top of this and that is the use of large geometry transistors. The effect of larger geometry transistors can improve second order intermodulation by as much as ten times for a tenfold increase in transistor size. Noise can also be reduced by about 10 dB for a similar increase in geometry. This leads us now to the simplest mode of operation of the 1537A using each gain control circuit individually, although the control voltage affects the gain of each circuit simultaneously (Fig. 3).

The ratio of R9 and R10 is calculated to allow a control voltage range of 10 volts (ie 0 to minus 10 V), altering the gain of the system from 0 dB to about -90 dB. The input impedance of the circuit to applied signal is low and ideally buffers should be placed before this circuit. Although this circuit does not give studio quality specifications it will, however, still produce results in the "high fidelity" range, providing impedance matches are considered.

Figure 4 shows a circuit application which gives a higher impedance input. Also included is an inverting stage in the control voltage link which allows a voltage of 0 to + 10 volts to be used for controlling attenuation.

Although any operational amplifier could be used for ICs 1, 2 and 3 in the previous circuit, it should be fairly

Fig. 4. A higher input impedance stereo VCA with positive going control voltage.



apparent that the noise, distortion and bandwidth specs of the circuit are limited to those of the op-amps used.

Either of the two circuits of Figs. 1 and 2 can be adopted as the voltage controlled gain heart of a stereo system. Their outputs are about 10 dB down on the inputs so necessary amplification should be given before or after the attenuator.

Coming Up To Scratch

Now, three more developments to the circuitry can be undertaken to improve the specifications to those of Table 1. Figure 5 shows the circuit of the ideal system capable of these high specs.

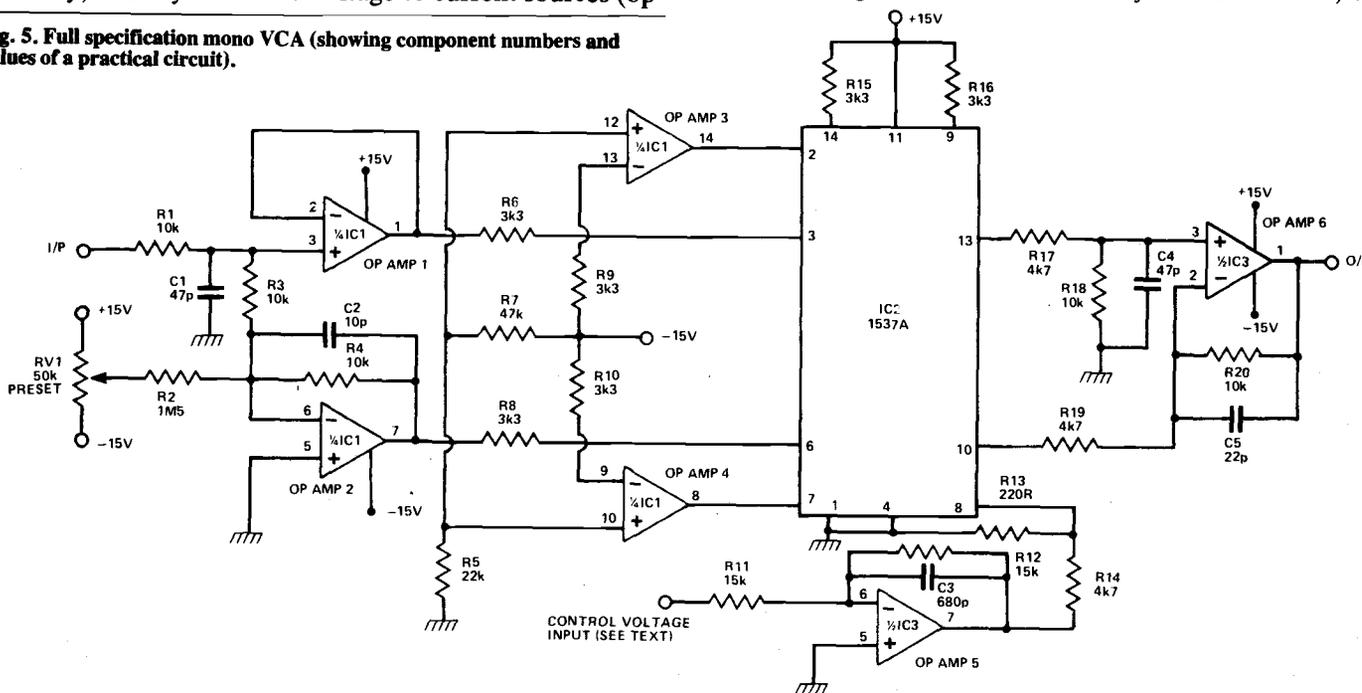
Firstly, actively linearised voltage to current sources (op-

amp 3 and 4 in Fig. 5) improve distortion figures when using a wide range of input signal voltages.

Secondly, paralleling of the two individual gain control circuits (ie the same input signal is fed to both devices at their inputs and mixed at their outputs) gives a 3 dB improvement in S/N ratio.

Finally, a technique is utilised which is complementary to the previous development of parallel devices, whereby the same input is applied to both gain control devices but 180 degrees out of phase. The two outputs are combined in a differential amplifier to give a single ended output. The differential amp is formed around op-amp 6. This technique has the effect of reducing DC shift caused by bias and control voltages and with careful adjustment of RV1, the

Fig. 5. Full specification mono VCA (showing component numbers and values of a practical circuit).



minimal DC shift now left at the output can be reduced even further to near (if not actually) zero. The prototype circuit shown, upon testing, actually gave no DC shift at all (or at least none measureable on our test equipment).

The complete circuit can be used as an exceptionally high quality VCA whose signal input can be anything from a few millivolts through to about 20 volts pk to pk without distortion. The lack of DC blocking capacitors at the input and output means that the system can be used to control a DC voltage applied to the input. AC signals up to well over 200 kHz are easily catered for, due to the system's wide bandwidth. The overlay in Fig. 6 shows the component layout on printed circuit board of the circuit. The PCB design is given in the Foil Pattern section of this issue and will enable those interested to build the system and get firsthand experience of it.

Construction

If the circuit board layout is followed then there should be no problems. IC holders are advisable though by no means necessary. RV1 should be a good quality type (cermet), to assist in setting up the output offset shift to zero, cheaper

quality presets can sometimes be tricky to adjust in low voltage DC applications of this nature. Op-amps 1 to 4 in the circuit are combined in IC1 and can be of a wide range of types from a quad 741 type (3403) upwards. Obviously, if you wish to obtain the best specs the quality of the op-amps are critical. LF 347 or TL 074 will give the best results.

Similarly op-amps 5 and 6 are included in IC3 and LF 353 or TL 072 are of optimal quality.

Setting Up

The system should work without any adjustment for an AC signal and varying the control voltage from 0 to 10 volts should give total control over the output amplitude. Some setting up will be required if the input is to be DC, though. This is best achieved by earthing the input. Measure the output voltage using a high impedance voltmeter (it should only be the order of a few millivolts). Adjust RV1 until a complete sweep of control voltage, ie from 0 to 10 volts produces only minimal change in DC output voltage. The circuit is now completely set up to accept an input signal in the frequency range DC to 200 kHz. At minimum attenuation the system operates as a unity-gain wide range, high

Parts List

RESISTORS All 1/4W, 5%

R1,3,4,18, 10k
20
R2 1M5
R5 22k
R6,8,9,10,15,16 3k3
R7 47k
R11,12 15k
R13 220R
R14,17,19 4k7

PRESET

RV1 50k min horiz cermet

CAPACITORS

C1,4 47p polystyrene
C2 10p polystyrene
C3 680p polystyrene
C5 22p polystyrene

SEMICONDUCTORS

IC1 TL074, LF347, etc.
IC2 1537A
IC3 TL072, LF353, etc.

MISCELLANEOUS

IC Holders
PCB

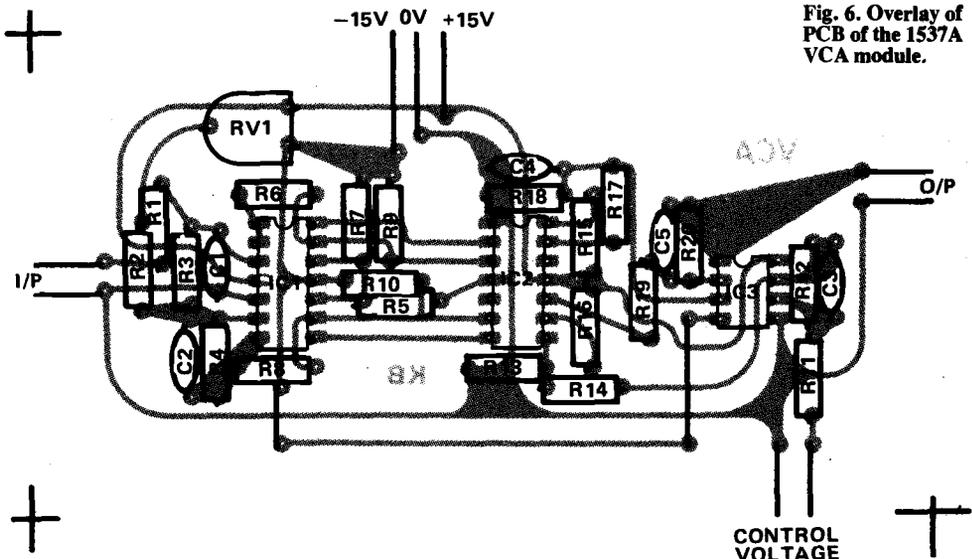


Fig. 6. Overlay of PCB of the 1537A VCA module.

quality buffer, with a reasonably high input impedance and low output impedance. Variation of the DC control voltage over the range 0 to 10 volts will produce over 90 dB of attenuation of the output signal.

If an overall gain is required in the circuit, resistors R18 and R20 can be changed as in Table 2.

The control voltage range of 10 volts can be altered as required simply by changing the ratio of resistors R13 and R14 to suit.

To our knowledge, there is no officially recognised standard symbol for a VCA and rather than redraw the whole circuit of Fig. 5 upon every reference to the circuit we thought it better to invent a symbol for the purposes of this article. A horizontal trapezoid shape appeared to be the ideal symbol, as shown in Fig. 7. It symbolizes the system as a modular buffer amplifier, whose output (symbolized by the top line) decreases as the control voltage (the bottom line) increases. We shall use the modular symbol of a VCA whenever reference is made to the circuit of Fig. 5, although any VCA module of another design should function in the applications which we give.

Buylines

Most of the larger mail order companies will be able to help with the quad and dual op-amps if you experience any difficulty in obtaining them.

The 1537, however, is presently obtainable only from AKG Acoustics Ltd, 191 The Vale, Acton, London, W3 705, Tel. 01-749-2042, for £7 (plus VAT).

All other components should be easily obtainable.

Use of the 1537A system module as a DC controlled analogue gate can produce many effects. Amplitude modulation of the signal occurs and the usual associated effects are observed. For instance, in Fig. 8 we can see a simple but high quality tremolo unit. Transistors Q1 and Q2 are connected as a phase shift oscillator and buffer, with speed and depth controls whose varying DC output is connected directly to the control port of the 1537A module. The frequency range of the oscillator is approximately 2 to 5 Hz.

GAIN	R18 & R20
0dB	10k
6dB	22k
10dB	33k
15dB	56k

Table 2. The values of R18 and R20 to give the required overall gain in the VCA system of Fig. 5.

Altering the values of all three capacitors will change the main frequency, though that stated will give the best results.

The control voltage in the last application was varied as a sine wave of course, but there is no reason why other waveforms, eg. square, could not be used for control purposes. Figure 9 shows a 555 operating in the astable mode with a frequency range of approximately 5-50 Hz. The output signal will be modulated with the square wave and the overall product is a Dalek type sound if a vocal signal is applied to the 1537A module.

This squarewave control can be taken one stage further if the control voltage is the output from a monostable as in Fig. 10. A tone burst generator can be very easily con-

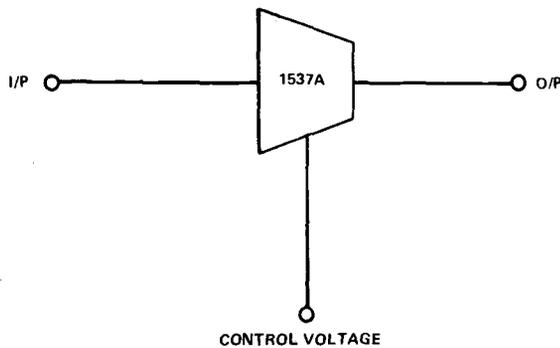


Fig. 7. The Electronics Digest symbol of a VCA module.

structed with this mode of operation. In a tone burst generator, a rectangular envelope 50-200 μ s long is formed around a single sine wave frequency of normally 1 kHz. Tone burst generators are useful for testing the transient response of speakers. A push to make switch is used to provide the trigger to fire the multivibrator, producing the correct length pulse which in turn is inverted to form the control voltage pulse, applied to the control port of the 1537A.

The previous applications have all used automatic waveform control of the applied signal to produce the required attenuation characteristics, but this is not a necessary trait. The control voltage can be simply tapped off a variable resistor having the maximum control voltage range (ie. 10 volts) across it. In this way, altering the position of the

wiper alters the attenuation of the applied signal. The pot acts quite simply as a volume or level control. Ordinary non-DC volume controls can suffer from pick-up problems because the signal itself is being rotated through the pot. As

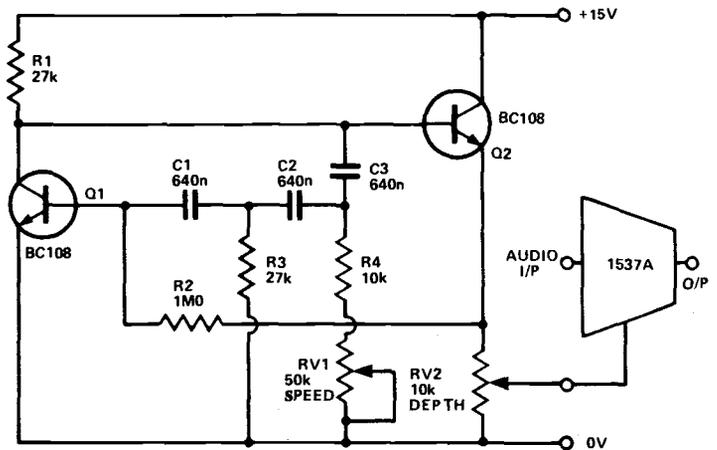


Fig. 8. A simple tremolo circuit.

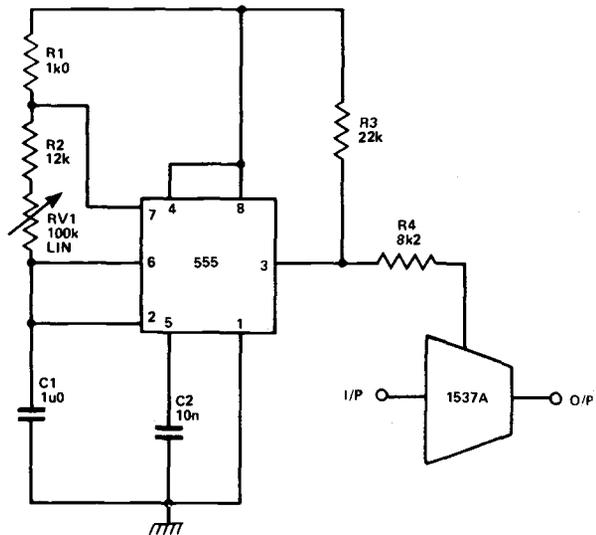


Fig. 9. A Dalek type sound generator.

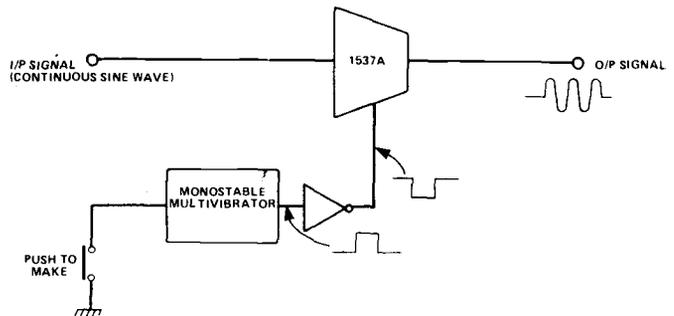


Fig. 10. A simple system enabling the construction of a tone burst generator.

only DC is applied to the pot in this application no pick-up can occur and the control can be remotely mounted from the module with no screened cable being necessary. Figure 11. shows such a volume control.

This remote control facility can be utilised in an audio mixer which includes remote faders for each channel. Figure

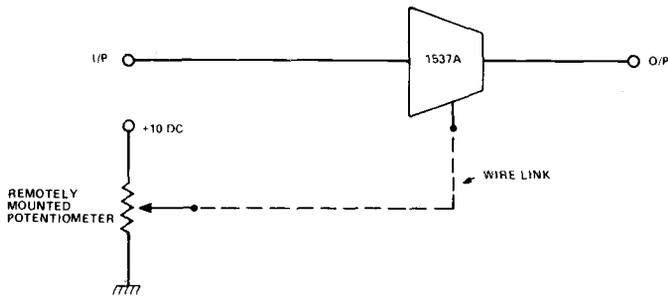


Fig. 11. Remotely (wire-linked) controlled volume control.

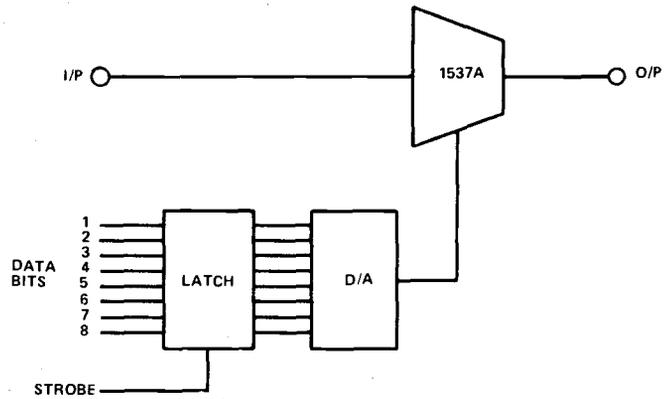


Fig. 13. Main components of a digitally controlled attenuator.

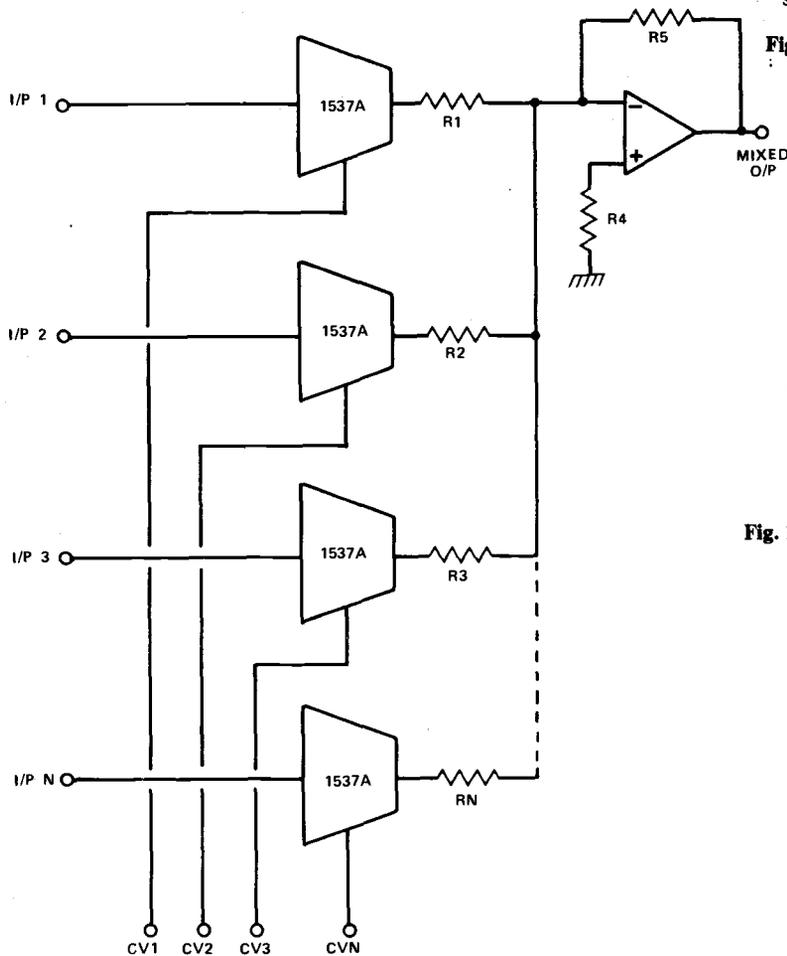


Fig. 12. High quality, remote fader controlled mixer.

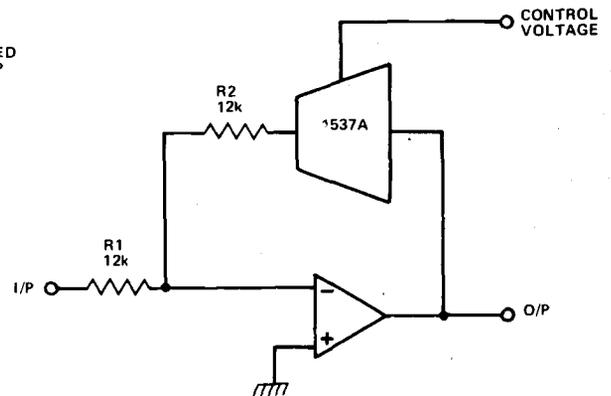


Fig. 14. A non-inverting controlled attenuator.

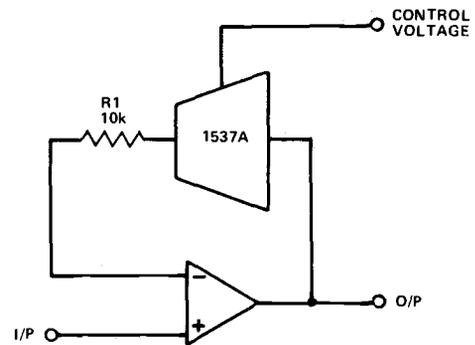


Fig. 15. A non-inverting voltage controlled amplifier.

12. shows the general idea of such a circuit. An op-amp is used as a summing amplifier into which the output of each channel's VCA is fed and mixed. The mix is relative to the control voltage applied from the remote faders to each VCA. The circuit allows for up to N inputs, where N to practical limits will probably be a maximum of about 12, but with careful layout techniques, there is no reason why this cannot be increased further.

Figure 13. shows an interesting outline to enable digital control of the VCA, say from a computer link. In order that the computer can operate in real-time, i.e. control of the VCA is not just its only job, it is necessary for the interface to provide a latch for the digital word. The output of this latch is changed to a linear DC voltage by the D/A (digital

to analogue) converter whose output is taken to the control port of the VCA.

The digital latch, once set by a strobe pulse, provides the facility that after the volume required has been found the computer is free to perform other tasks. When the volume is to be altered, the latch is reset to the new digital input.

Conclusions

The applications given in this article show the 1537A chip to be a very versatile device. It is remarkably easy to work with, a fact which is borne out by the quality (in technical terms) of the circuitry in the breadboarded fashion of our experimental design work, let alone in the modular fashion allowed by the use of our PCB layout. **Keith Brindley**

Chapter 21

DIGITAL DESIGN PRINCIPLES

The arrival of increasingly complex digital chips brings sophisticated designs within the scope of the hobbyist.

THE INPUT TO A TTL DEVICE is a single or multiple emitter. For the 7410, all the inputs must be high before the output will go low. The maximum current needed to pull an input low is 1.6 mA, but the high input current is 0.04 mA. If a TTL input is left open circuit, it will automatically float high, although for proper operation all unused gates must be tied high and not allowed to float. The output of a TTL device is capable of sinking more current than sourcing it. For the 7410 it is a maximum of 16 mA (low) and 0.4 mA (high). This implies that the 7410 is capable of driving 10 input loads (fan-out of 10). The typical high output voltages is +3V5 and the low is +0V2.

When testing TTL it is important that 'sanitary' logic levels are observed. The signals should always be above +3 V and below +0V5. Signals between these may well produce unpredictable results. Short glitches can also generate problems. One source of glitches is a power supply with too high an impedance. As a TTL gate switches, it generates a short current surge on the supply rail which can produce large voltage spikes. This problem can be overcome by using thick ground and V_{CC} tracks and by regularly decoupling the power supply. Use a 10 to 100 nF fast ceramic or 470 nF tantalum capacitor for decoupling on every four or five packs.

CMOS

TTL can operate at frequencies as high as 50 MHz, but for higher frequencies ECL (Emitter Coupled Logic) devices should be used. These extend the range to as much as 1 GHz. For lower speed applications CMOS devices can be used. Maximum operating speeds of 5 MHz can be obtained. One tremendous advantage of using CMOS is that it consumes only micro-power. For example, the maximum quiescent current for the 4049 device is 20 μ A. Also, the output voltage swing goes within 10 mV of either supply rail (no load). The inputs are very high impedance, having typical input currents of a mere 10 pA. The output stages can usually deliver currents of 0.5 mA, giving CMOS an enormous fan-out capability, limited by speed rather than DC drive.

The B series of CMOS can run on supply rails between 3 and 18 V, making them ideal for battery operation where dropping supply voltage and low current outputs make TTL

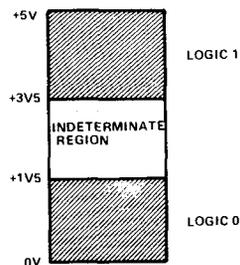


Fig. 1. CMOS operation on a 5 V rail.

designs impossible. The CMOS transfer function shows a wide spread from device to device, which results in an indeterminate region of operation of about 60% of the supply voltage. As the input impedance is so high, the input terminals can often act as sample and hold devices. If your bias one to +3 V, say, and then let it float, it may well remain charged at this voltage. Unlike TTL, unused inputs can float anywhere. Some may well float into a region where both output FETs are partly on, thus presenting a load of a few kilohms across the supply rails, destroying the low power condition. Unused inputs should be tied high or low, depending on the desired circuit operation. The CMOS range of devices is different in pinout and part number to TTL devices. However, there does exist a CMOS copy of TTL known as the 74CXX series. Decoupling should be used for CMOS designs, but it is less of a problem than for TTL.

CMOS/TTL Interfacing

Interfacing to either TTL or CMOS can cause problems. To operate TTL a simple pull down transistor (Fig 2a) will suffice. When TTL is driving CMOS it is necessary to put the TTL output high, because the usual +3V5 high signal is just on the intermediate region of operation for the CMOS device (Fig. 2b). CMOS cannot pull down TTL. The typical 1.6 mA pull down is well beyond the output drive capability.

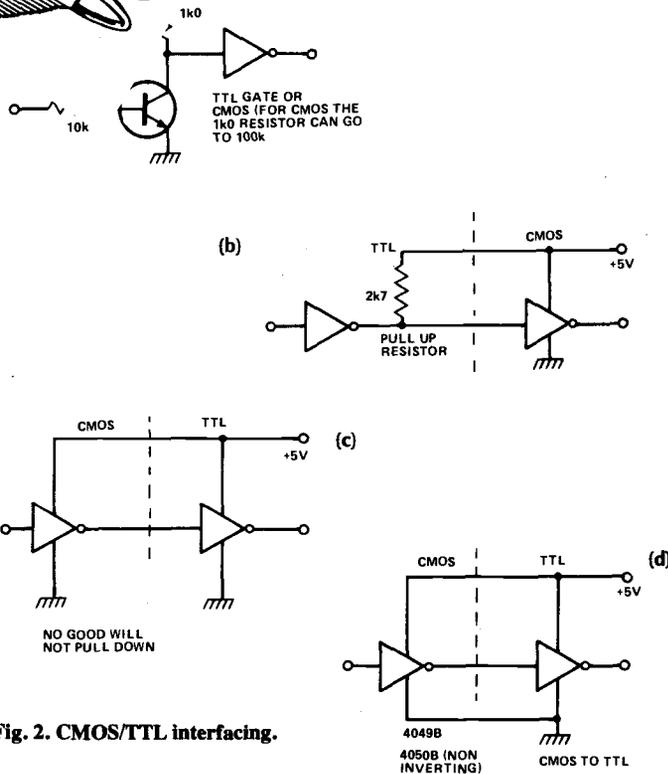


Fig. 2. CMOS/TTL interfacing.

ties of most CMOS outputs (Fig. 2c). The 4049 and the 4050 are buffer/converters, which can drive up to two TTL loads each. When powered from +5V they can even accept CMOS levels up to +18V (Fig. 2d). In doing so they are converting high level CMOS signals to low level TTL drives. Another CMOS converter is the 4041.

Logic Probes

If you don't have an oscilloscope then a simple logic probe can be a useful tool for debugging digital circuits. A simple probe is shown in Fig. 3a. If all six of the inverters are wired up, then the probe can diagnose the logic state of six signals simultaneously, making it very useful for examining data blocks. A logic 1 is represented by the LED being on. Probe B detects the presence of a clock signal. On the falling edge the monostable is fired and the LED turns on. Note that to drive LEDs directly from TTL a pull down circuit must be used. Probe C is for CMOS circuits. The 3mA drive from the 4050 is not sufficient to light the LED.

A set-reset flip-flop can be implemented using NAND or NOR gates. This device can be used to debounce switch actions or as a single bit memory. Note that positive-going pulses are needed for the NOR version and negative-going pulses for the NAND version.

Switch Debouncing

Contact bounce from a mechanical switch can cause problems in digital circuits; it can be seen as a multiple entry. By

filtering the signal and then Schmitting it, the bounce can be reduced to a single transition. Note that the TTL device needs a low value resistor to ensure that the logic low is reached.

Edge Delay

This circuit is sometimes used to generate a short delay to help prevent a race condition between two signals. A Schmitt trigger gives sharp output waveform. If an ordinary gate is used then the output will have a slower falling edge.

Often a digital signal is very thin (50-100 ns), difficult to see on an oscilloscope and impossible on a logic probe. The monostable action of the pulse stretcher enables the pulse to become visible.

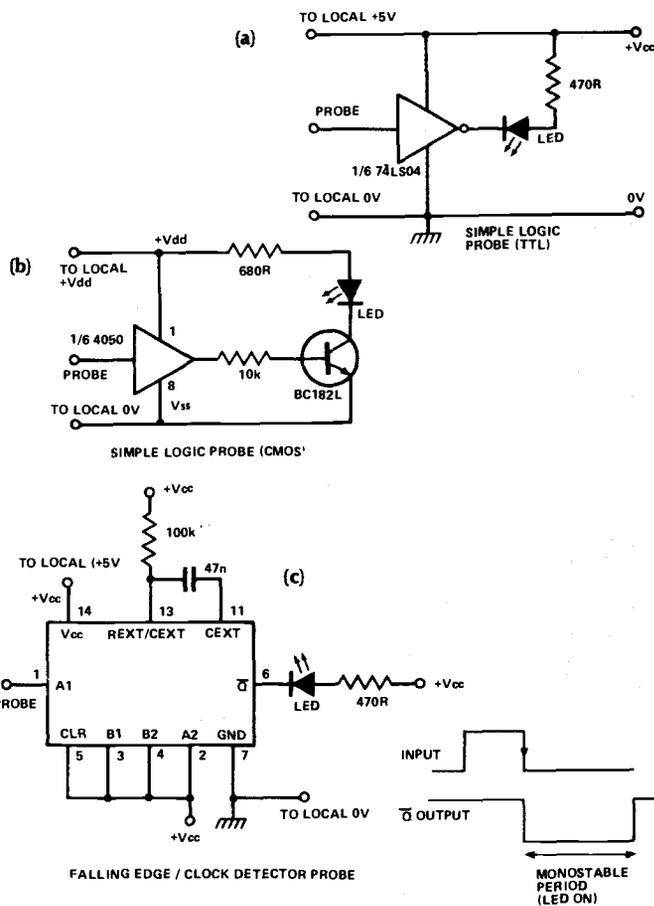


Fig. 3. Three simple logic probes.

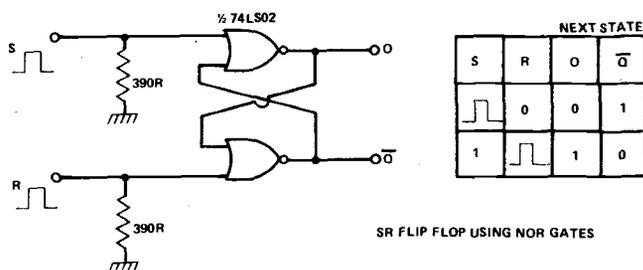
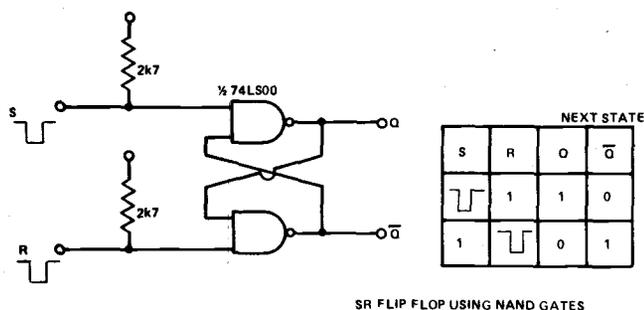
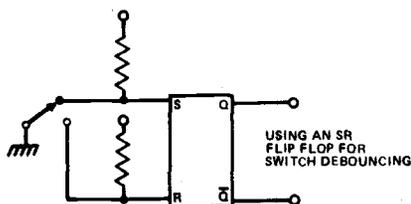


Fig. 4a. SR flip-flop using NOR gates.



SR FLIP FLOP USING NAND GATES



USING AN SR FLIP FLOP FOR SWITCH DEBOUNCING

Fig. 4b SR flip-flop using NAND gates.

16 Key Encoder Chip

The 74C922 generates a four bit output code representing the last key pressed. The keyboard can be scanned by an external clock or by its own internal oscillator. All the switches are internally debounced by the IC. The output can drive low power TTL. The device can be used to encode a Hex keyboard or any other switch matrix. For 20 note operation the MM74C923 can be used.

D-Type Flip-Flop

The 4013 is a CMOS dual D-type flip-flop. Data present at the D input is transferred to the Q output on the positive transition of the clock. The clock waveform should have a rise time of greater than 5 uS. By programming the Set and Reset pins the outputs may be preset to any state. The device may be used as a single bit memory, or by connecting the D input to the Q output a divide by two counter may be built.

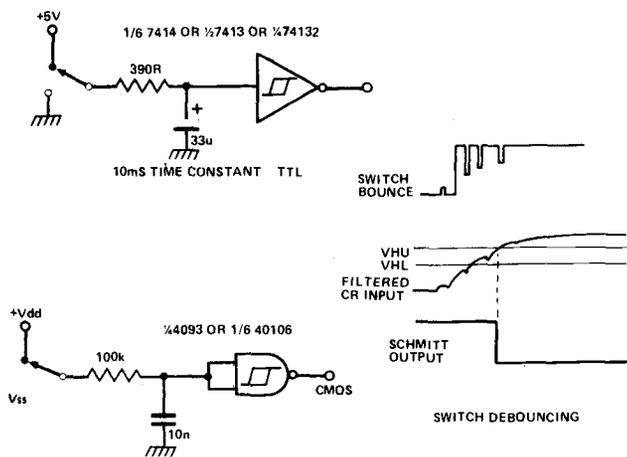


Fig. 5. Switch debouncing.

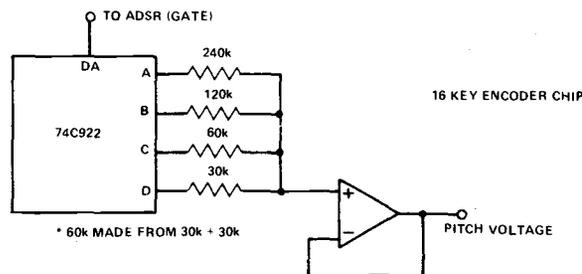
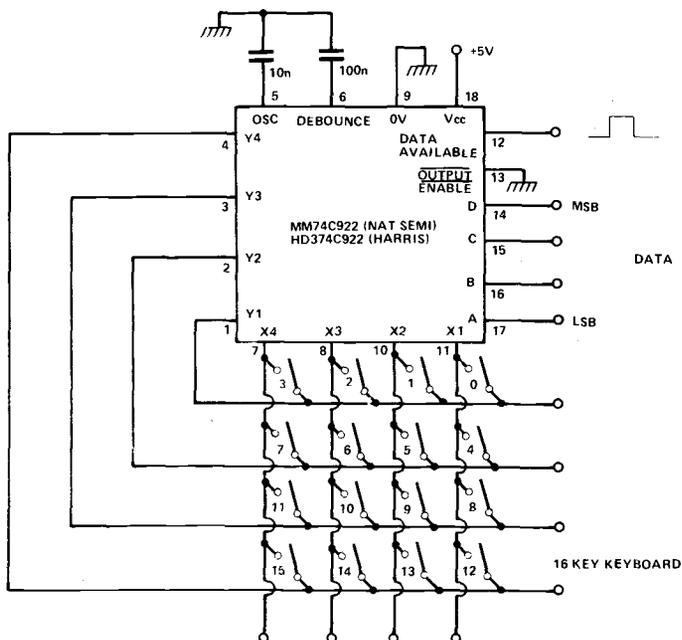


Fig. 6a. A 16 note keyboard for music synthesiser.

The two halves of a 4013 are used as a two stage binary counter with complementary outputs. The four signals '0', '1', '2' and '3' are known as decoded outputs. These are obtained with two input AND gates. Let's see how decoded output '2' is obtained. Looking at the timing diagram, '2' occurs when Q2 is high and Q1 is low. We can, therefore, generate the waveform by ANDing together Q2 and the inverse of Q1, that is Q1. *The timing diagram is the most important tool for designing logic systems.* Just by drawing out the timing that you need, it becomes very easy to both understand and implement the system. There is no need to even consider using Karnaugh maps or logic equations.

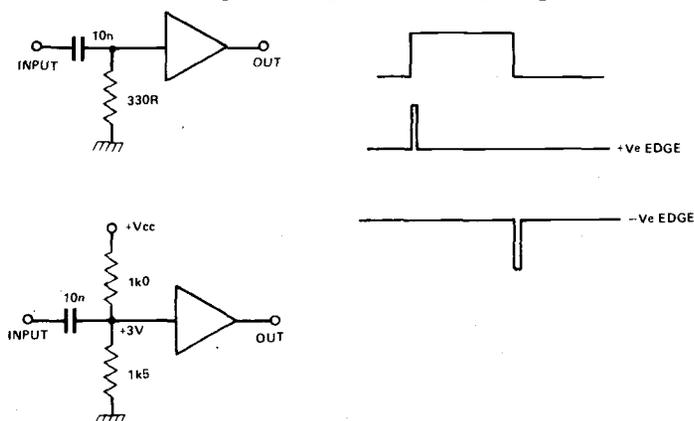


Fig. 7. TTL gates can be used to detect positive and negative edges by using simple CR input networks.

The last part of the circuit is the multiplexer. This is a digitally selected, analogue single pole four-way switch implemented with the 4016 analogue transmission gate. A logic 1 at the switch control pin turns the switch on, a logic 0 turns it off. Of course, there is a better way of implementing this design. The 4052 is a differential four channel MUX with its own decoding. Thus, the 4081 and the 4016 are replaced with a single 4052. Other multiplexers include the 4051 (eight way MUX) and the 4053 (triple two way MUX).

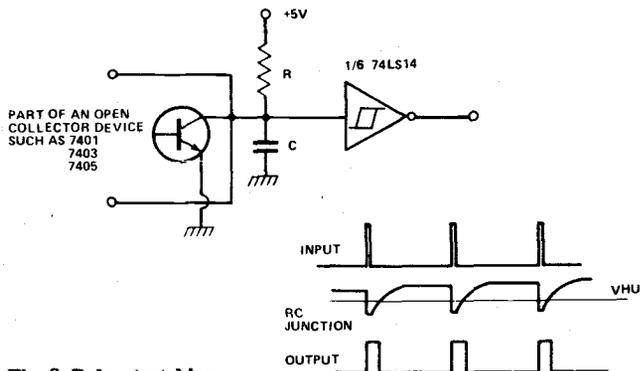


Fig. 8. Pulse stretching.

CLK	D	R	S	Q	\bar{Q}
0	0	0	0	0	1
0	1	0	0	1	0
1	X	0	0	0	0
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

CMOS 4013 X = DON'T CARE STATE

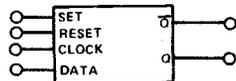


Fig. 9. D-type flip-flop.

In fig. 11 – is a decade counter with 10 decoder outputs. A high on the reset line clears the counter back to zero. The decoded output is high, all the other outputs are low. The simple transistor circuit enables the counter to drive LEDs.

Counting And Decoding

Another counter/decoder circuit is shown, but this time it uses TTL. The 74LS93 is a four stage binary counter. The four outputs are shown on the timing diagram and three decoded outputs '0', '1', and '11' are shown below them. To obtain these, all four outputs must be decoded. For example, to decode '11' we need to look at the timing diagram. Outputs A, B, D are high and C is low. Therefore, a four input AND gate must be driven with A, B, D and C. This could also be determined by studying the truth table. The decoded outputs will probably contain what are known as glitches. These are very thin (100 ns) pulses, which can cause problems in some designs. The outputs of the counter do not all change state at exactly the same time. The outputs further down are later in changing due to the time delays in the system. This counter is known as a ripple counter.

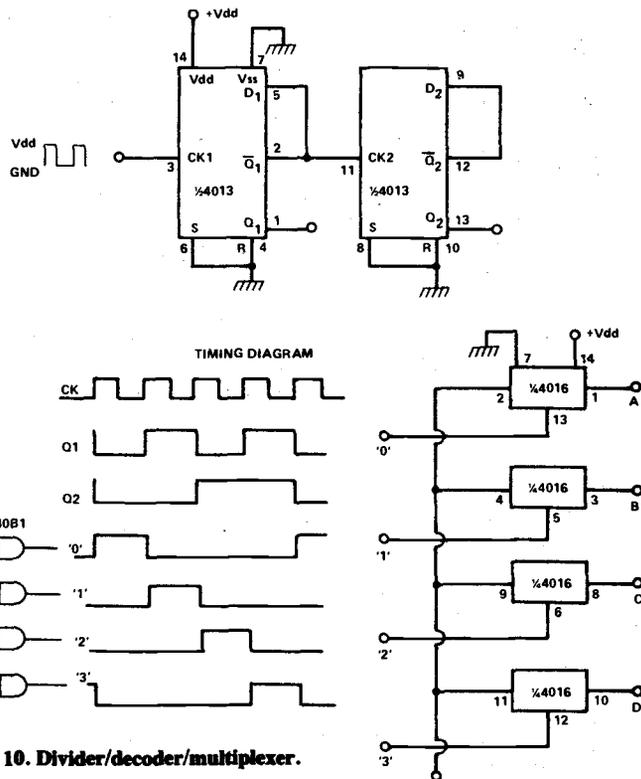


Fig. 10. Divider/decoder/multiplexer.

When the counter is clocked, the first stage changes state, which, after another short delay, sends a clock pulse to the second stage, which, after a short delay, sends a clock pulse to the next stage, etc, so the information ripples down the counter causing a skew in the total output. If the output is then decoded, it is possible to get a momentary illegal state caused by the time delays. These effects have been overcome in synchronous counters, which use synchronous clocking of all their storage elements. In these devices the skew time is very short.

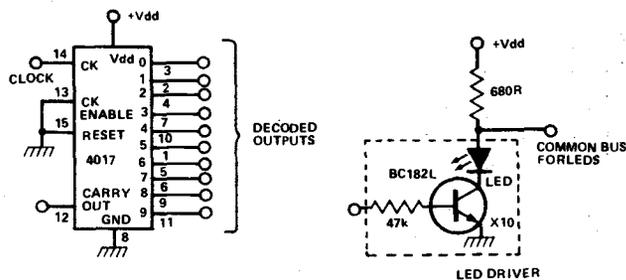


Fig. 11. CMOS counter/decoder.

Schmitt Trigger Oscillator

Using a simple RC timing circuit, a Schmitt trigger can be made to oscillate. The capacitor is exponentially charged and discharged between the hysteresis levels of the Schmitt trigger. If a TTL device is used, then the squarewave output will be asymmetric, mainly due to the relatively large input current of the TTL gate. A simple resistor/diode network will restore the symmetry. The resistor value must be kept low, otherwise the circuit will not be able to pull the input

TRUTH TABLE

COUNT	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

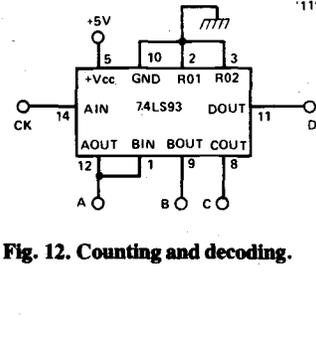
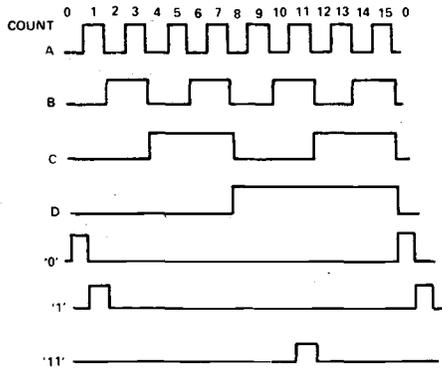


Fig. 12. Counting and decoding.

sufficiently low and will not then oscillate. Using a 7413 the maximum frequency obtainable is 50 MHz, which uses the stray capacitance of the package as the timing capacitor, C. The same circuit will oscillate using CMOS Schmitts (4903 or 40106). The waveform will be inherently more symmetrical and, of course, the device has a very high input impedance. This will enable the use of timing resistors of up to 10 to 100 M.

Bit Rate Generator

When computer terminals and data terminals 'talk' to each other, they do so at standard bit rates. The MC14411 is a bit rate generator IC that produces 14 standard frequencies, with the option of times 8, 16 and 64 rates. If your computer has a serial interface, then it is likely that it has a bit rate generator controlling the data rate.

Pseudo-Random Generator

It is possible to generate noise digitally. A random binary sequence has most of the characteristics of a noise source. This random sequence may be produced by taking exclusive OR feedback from selected points in a shift register. The sequence that is produced does, in fact, regularly repeat itself, but the repetition rate is relatively slow. The longer the shift register length, the longer the repeat time. Also, by choosing the best feedback points, the sequence length will be maximally long. The chart shows the best feedback points for a selection of shift register lengths. Note that incredibly long sequences may be generated very easily.

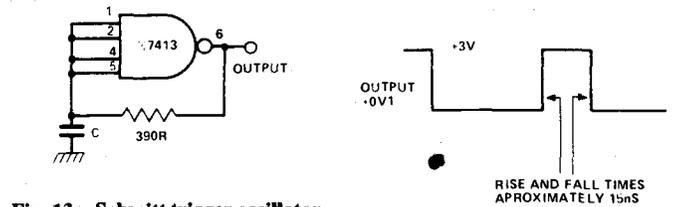


Fig. 13a. Schmitt trigger oscillator.

C	OSCILLATION FREQUENCY
0p	50 MHz
1000p	2.2MHz
10n	250kHz
100n	25kHz
1u	2.5kHz
10u	250Hz

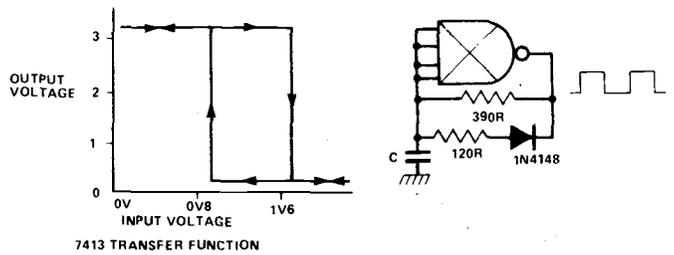


Fig. 13b. Modifying the feedback network to give a 1 to 1 output.

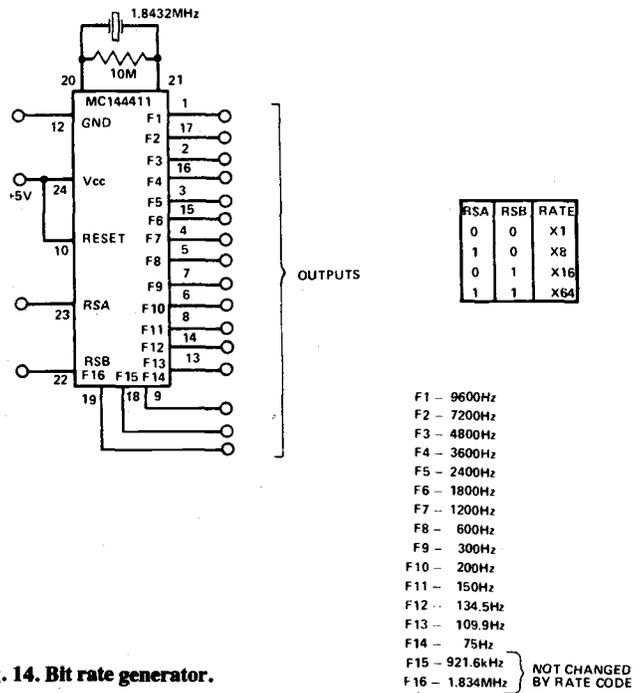


Fig. 14. Bit rate generator.

A pseudo-random noise generator can be made from two CMOS chips. The output may be filtered to give any desired spectrum. There are also two noise generator chips available, the MM5837 and the S2688. The uses of pseudo-random generators include constant noise spectrums for audio testing, noise sources for music synthesizers and random number generators for premium bond pickers!

Memories

Memory circuits are becoming cheaper. Static RAMs (Random Access Memories) are the easiest memories to design into systems. Dynamic RAMs are, in fact, less expensive and more dense than static ones but they need extra support circuitry. The information they contain is very volatile and every piece of the memory must be refreshed every few milliseconds. A static RAM has no need to refresh its memory.

Memory is organised into 'handy' sizes. The 2101 has four data inputs and four outputs plus an eight bit address input. The 2102 has only one data input and one data output, but it has a 10 bit address input. The 2114 has four data terminals and a 10 bit address input. Note that the data terminals for the 2114 act as both inputs and outputs. The write cycle for the 2114 is as follows:

Set up the memory address and take \overline{WE} low. Set up the data and take \overline{CS} low. The RAM has now been written into. Take \overline{CS} and \overline{WE} high. The RAM is now in its read mode (that is, it is outputting data) but it is disabled. To read data, set up the address, leave \overline{WE} high and take \overline{CS} low. The relevant data will appear at the data I/O pins. The 2114 is a convenient size for microprocessor memories. By using two of them, eight bit words can be stored. When the power is removed from a RAM all the information stored is lost.

Some systems employ low power CMOS RAMs with a back-up battery. When the power is removed the battery keeps the RAMs powered up. CMOS RAMs are at present very much more expensive than the common 1K and 4K devices.

Tim Orr

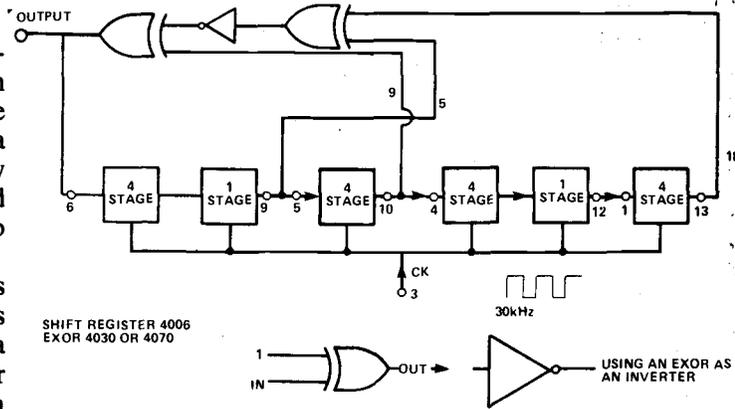


Fig. 15a. Pseudo-random noise generator using CMOS.

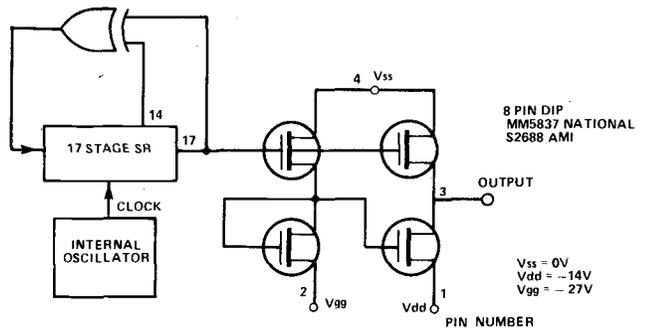
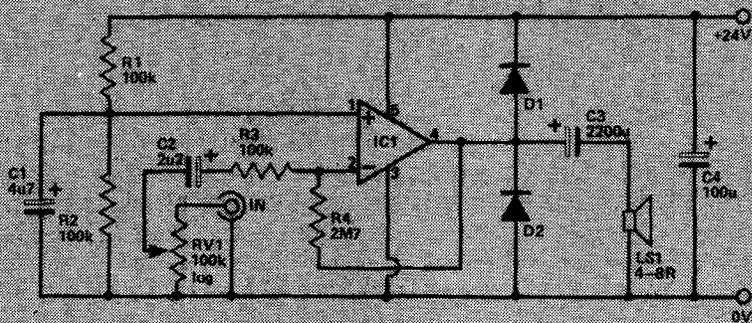


Fig. 15b. Using a special function chip.

USING A MODERN audio power amplifier IC, it is easy to produce an amplifier giving several watts of output with quite good quality. The amplifier is based on the TDA2006 and gives about 8 W RMS into an 8R speaker, or 12 W when using a 4R load. At most output powers significantly at higher output levels.

The TDA2006 is in many ways like an operational amplifier, but it has a class B power output stage. In this circuit it is used in the inverting amplifier mode with R1 and R2 forming a potential divider that biases the non-inverting input to half the supply voltage. C1 filters out hum and noise which might otherwise be coupled from the supply lines to the non-inverting input via the bias circuit. The inverting input is biased by R4 and together with R3 this resistor forms a negative feedback circuit which sets the voltage gain and input impedance of the amplifier. As would be the case with an operational amplifier, the voltage gain is equal to R4 divided by R3 and the input impedance is equal to R3. With the values shown this gives a voltage gain of 27 times and an input impedance of 100k. However, within reason these figures can be modified by changing the values of R3 and R4. RV1 is the volume control and does of course shunt the input impedance of the circuit as a whole (down to as little as 50k with the specified values).

NOTE
IC1 IS TDA2006
D1 & 2 ARE 1N4148



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8 Watt Audio Amplifier

As the TDA2006 has a supply ripple rejection ratio of 50 dB, it is not essential to use a very well smoothed supply, but it is important that the device's 30 V maximum supply voltage rating is not exceeded. The maximum average supply current is a little over 500 mA when using an 8R speaker and about 800 mA when using a 4R load. The TDA2006 should be mounted on a substantial heatsink, but has thermal shutdown circuitry which protects it against overheating. It also incorporates output current limiting circuitry.

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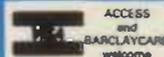
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