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RCA REVIEW

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FOREWORD

EPITAXIAL GROWTH, a new and useful technique employed in preparing novel, intricate, and precisely controlled semiconductor devices, is the subject of the first twelve papers presented in this issue of RCA REVIEW.

The term "epitaxy," coined from the Greek roots *epi* = upon and *taxis* = arrangement, is used to describe crystal growth of a special kind: When atoms from a fluid phase condense on a crystalline substrate to form a crystalline layer whose *orientation* is controlled by the substrate, the layer is said to be "epitaxial."

Of the many techniques for achieving epitaxial growth, various methods for deposition from the vapor phase are the most popular, and some of these are described in the majority of the papers in this issue. This popularity can be ascribed to the relatively low temperatures at which epitaxial growth can be obtained from vapor-phase systems, and to a consequent improvement in the purity of the deposited layers.

Epitaxy adds new dimensions of freedom in the design and fabrication of semiconductor devices. Epitaxial layers can be given desired electrical properties by introducing small amounts of doping agents during the growth. Hence, the relatively thin active volumes and interfaces of transistors and other solid-state devices can be custom made, with abrupt or graded changes in electronic properties and with controlled thicknesses, as required. Furthermore, large numbers of devices having uniform electrical characteristics can be made simultaneously using masking coupled with epitaxy. In many instances, epitaxial growth of one semiconductor on another can be achieved; with some semiconductors the composition, as well as the doping, of the growing layer can be altered during growth to permit the fabrication of new kinds of semiconductor crystals and junctions. The versatility and power of the epitaxial growth process is, perhaps, revealed to best advantage in the preparation of integrated circuits where many active and passive devices are formed and interconnected on the same small-area substrate.

This collection of papers signals more than the advent of new and useful epitaxial growth techniques. It demonstrates, in addition, the

need for interdisciplinary effort in developing the techniques required for the fabrication of full-fledged integrated circuitry. Thus, the accomplishments described in this issue are a testimony to the fruitfulness of the coordinated teamwork of persons versed in several scientific disciplines—chemistry, metallurgy, physics, and electronics—when directed toward a common objective.

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THE ETCHING OF GERMANIUM SUBSTRATES IN GASEOUS HYDROGEN CHLORIDE*†

By

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Summary—A technique for preparing chemically etched, mirror-smooth surfaces on (111) oriented germanium wafers is described. These surfaces, which are essentially structureless, appear to be ideal for use in epitaxial growth. The influence of etching gas composition, temperature and etching time on the etching rate are reported.

Introduction

THE substrate surface is of critical importance for the preparation of epitaxial deposits since this surface plays a major role in the nucleation process taking place during the initial stages of growth. Ideally, this surface should be free of major crystalline defects such as the work damage left by mechanical polishing. It should be free of chemical impurities such as oxide layers. It is also desirable that the surface be extremely flat, smooth, and structureless. The techniques used in preparing the substrate surface for epitaxial growth should be highly reproducible and should eliminate any contamination of the substrate caused, for instance, by exposing it to the atmosphere during the interval between etching and epitaxial growth.

It has been found that all of these requirements can be met for (111) oriented germanium substrates by etching them in flowing gaseous HCl at temperatures above 800°C in the same apparatus in

* A portion of this paper was presented at a conference on Single Crystal Thin Films held at the Philco Scientific Laboratory, Bluebell, Pa., May 13-14, 1963, and will appear in the proceedings of this conference.

† Note added in proof: A kinetic study of the HCl etching of germanium substrates was presented as a "Recent News Paper" at the semiconductor session of the Electrochemical Society Meeting, Sept. 29 to Oct. 3, 1963, by K. J. Miller and M. J. Grieco.

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which growth is to take place.†† The reaction is easily controlled, and thicknesses of 1 mil or more can be rapidly removed from the substrate leaving a bright, mirror smooth, structureless surface. HCl reacts with germanium oxide to form germanium chloride and water which are removed from the apparatus. Chlorine, the major impurity present on the etched germanium surface, causes no serious problem since epitaxial growth is often carried out by the reduction of chlorides.

Germanium (111) oriented wafers, prepared in this manner, have been used as substrates for the epitaxial growth of germanium[3] and of gallium arsenide.[4] The preparation of these layers is described in other papers.

Apparatus

Two different types of apparatus have been used for etching germanium substrate wafers in gaseous HCl. In one of these the wafer is mounted on a susceptor block and heated by r-f induction,[3] the walls being kept relatively cool. In the other, the wafers are mounted on a quartz support rod and heated by a furnace surrounding the quartz etching chamber.[1] Results obtained with both types of apparatus are equivalent. Since the greater portion of the etching information was obtained with the first of these two systems, it will be described in more detail.

Figure 1 shows the apparatus in which the etching of germanium substrates was carried out prior to the growth of germanium layers.[3] The manner in which the germanium substrate and the susceptor block are mounted is seen in Figure 2. The etching chamber and the susceptor support are of quartz while the remainder of the system is Pyrex. Palladium-diffused hydrogen or tank helium are admitted to the system by way of a 1/4-20 flowmeter.* HCl is introduced directly into the

†† Etching of germanium and silicon in HCl, chlorine and mixtures of these gases has been mentioned in several publications.[1,2] The nature of the surface so prepared and the conditions under which the etching is carried out have not previously been described, however.

[1] G. W. Cullen, J. A. Amick and D. Gerlich, "The Stabilization of Germanium Surfaces by Ethylation," *Jour. Electrochem. Soc.*, Vol. 109, p. 124, Feb. 1962.

[2] K. O. Seiler, U. S. Patent No. 2,744,000, May 1, 1956.

[3] E. A. Roth, H. Gossenberger, and J. A. Amick, "The Growth of Germanium Epitaxial Layers by the Pyrolysis of Germane," *RCA Review*, Vol. 24, p. 499, Sept. 1963.

[4] J. A. Amick, "The Growth of Single-Crystal Gallium Arsenide Layers on Germanium and Metallic Substrates," *RCA Review*, Vol. 24, p. 555, Sept. 1963.

* Fischer and Porter Co., Hatboro, Pennsylvania.

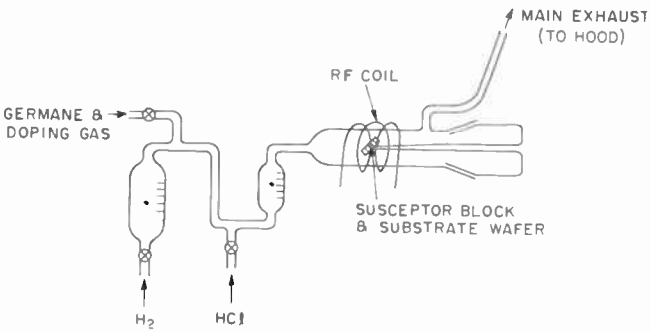

Fig. 1—Diagram of apparatus for etching of Ge substrate wafers prior to epitaxial growth.

hydrogen stream from a lecture cylinder and monitored by passing the mixture through a second 1/4-20 flowmeter. In this manner the HCl present in the short link between the tank valve and the apparatus is rapidly removed from the system once the valve is shut off. Furthermore, the second flowmeter introduces turbulence into the gas stream which helps to ensure thorough mixing of the gases. The exhaust gases pass through a three-foot length of 1/2-inch outside diameter Pyrex tubing and are then burned in a hood. As etching proceeds, the smoothness of the surface can be followed visually through the optical flat sealed into one end of the etching chamber.

The temperature of the substrate is determined with an optical

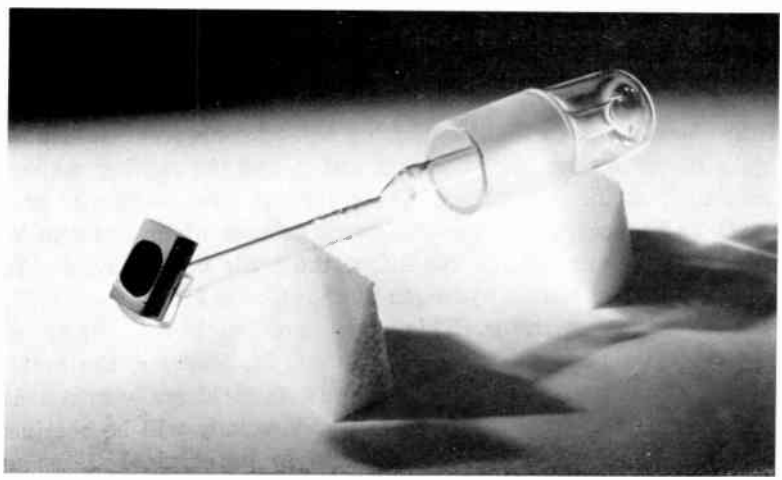

Fig. 2—Close-up view of susceptor block, with mounted substrate wafer and quartz support rod.

pyrometer so placed that the hot substrate can be observed reflected in a mirror mounted in front of the optical flat. To provide a fixed reference point for the temperature measurement, the melting point of an old susceptor block was determined. The temperature read on the pyrometer was 840°C when the instrument was focussed on a molten area of the block. Since the accepted melting point of germanium is 936°C a temperature correction of 96° was added to each pyrometer reading.

The etching zone of the second apparatus, that used for depositing gallium arsenide layers on germanium substrates,[4] is shown schemati-

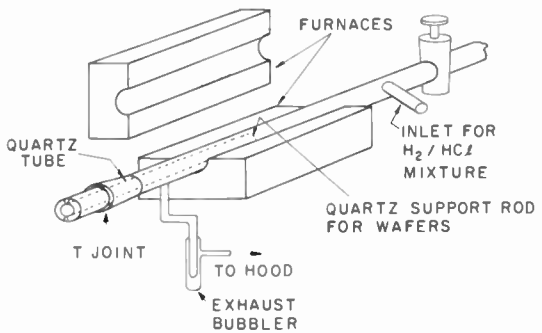

Fig. 3—Diagram of HCl etching apparatus using external furnaces.

cally in Figure 3. The etching chamber and wafer support are constructed of quartz, and the gas-inlet system is similar in design to that of the first apparatus described above. Exhaust gases leave the system by way of a bubbler containing fluorocarbon oil.

It has been observed that the etching will be nonreproducible unless the walls of the system, the substrate wafer, and the etching reagents are extremely clean. The walls of the apparatus must be free of products such as hydrocarbon oils and stopcock greases which are attacked by the HCl. To ensure this condition, the walls of the system are normally flamed out with a hydrogen torch, prior to etching, while HCl flows through the apparatus. This step is not required if the system is used two or three times during one day. If, however, the system stands over a weekend, or if stopcock grease is accidentally introduced into the system, cloudy nonuniform surfaces usually will be obtained. Flaming the walls will return the system to its original state, and smooth structureless germanium surfaces will again be obtained following etching.

Materials

The (111) germanium substrates used in this work were approximately 10 mils thick, and mechanically polished on one surface to an optical finish. Most of the etching experiments were carried out on p^+ material gallium doped to about 7×10^{-4} ohm-cm, as these were to be employed subsequently in the epitaxial growth studies; p and n type wafers of both high and low doping concentration were also etched and their surfaces were found to be comparable to those of the etched p^+ germanium substrates.

The germanium susceptor blocks (Figure 2) were prepared from intrinsic germanium according to a design suggested by N. Ciampa. A square bar of heavily doped germanium at the upper right of the block serves as an "igniter."

The hydrogen used in this work was obtained from standard tank hydrogen by passing it through a palladium diffusion apparatus.* The purity of this reagent is higher than can be obtained by any other standard technique. The helium used in this work was taken directly from a standard cylinder. Since this reagent is used only for the initial displacement of air from the system and is not present during etching, it was not purified prior to use.

The hydrogen chloride was originally obtained from Matheson† lecture cylinders. No reduction valve was used and all connections were of Teflon or Pyrex except the cylinder valve which was Monel. Analyses have shown that this reagent contains impurities in variable amounts.[5] These were found to give nonreproducible results, especially when an exhausted cylinder was replaced with a fresh one. Recently, HCl has been obtained from the Stauffer Chemical Co.‡ in much higher purity; infrared absorption analyses showed no detectable carbon dioxide and no acetylene.[5] This HCl has given consistently excellent surfaces.

Precleaning Steps

Precleaning of the substrate wafer, susceptor block, and quartz support was found to be essential. It is especially important to remove any traces of the wax used to mount the germanium single-crystal boule during the slicing operation. If this wax is not removed, the surface

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* Engelhard Industries, Inc., Newark, New Jersey.

† Matheson Co., Inc., East Rutherford, New Jersey.

[5] G. A. Lang and T. Stavish, "Chemical Polishing of Silicon with Anhydrous HCl," *RCA Review*, Vol. 24, p. 488, Sept. 1963.

‡ Textile Chemical Co., Reading, Pa.

of the etched wafer will be hazy and nonuniform, and a carbonized residue of the wax will be present at the edge of the wafer. The wax used to mount the single-crystal boules was soluble in chlorinated hydrocarbons and could be removed by immersing a wafer in boiling trichloroethylene for a few minutes, then rinsing in fresh hot trichloroethylene. The germanium wafer was then washed in an aqueous detergent solution, rinsed in deionized water, then in absolute methanol and finally in carbon tetrachloride. Following the carbon tetrachloride rinse, the wafer was placed in a flowing stream of filtered tank helium and allowed to dry.†

The susceptor block, after use, was cleaned and made planar by grinding its surface against a plate glass flat using silicon carbide 305 abrasive.‡ It was then washed in aqueous detergent, rinsed in deionized water, methanol and carbon tetrachloride and dried in filtered helium, as described for the substrate wafers.

The quartz support rod was cleaned either by heating it in a hydrogen–oxygen flame or, if necessary, by first etching it in a mixture of HF and hydrogen peroxide to remove any germanium deposit, then rinsing it in deionized water and finally heating it in a hydrogen–oxygen flame.

Prior to beginning an etching or growth run, the standard taper joint was carefully cleaned with trichloroethylene to remove all traces of stopcock grease. The inner member (on the support rod) was then greased with silicone stopcock grease, the susceptor block and the substrate were mounted on the support, and the assembly was inserted into the apparatus. In this way, contact of the substrate and susceptor block with stopcock grease could be avoided during insertion of the assembly into the apparatus.

Etching of the Substrate Wafers

The air initially present in the etching apparatus is first displaced by helium which, in turn, is displaced by hydrogen flowing at about 10.8 liters per minute. After a few minutes, the r-f generator is turned on and the susceptor block and substrate wafer brought up to the desired temperature, as determined with the pyrometer. Generally this temperature is about 830°C (corrected). A few minutes is allowed

† This sequence is based partly on suggestions by W. Kern and was designed to minimize contaminants on the surface prior to beginning the HCl etching.

‡ Centriforce 305, American Optical Co.

for the block, the wafer, and the reaction zone to reach a thermal steady state.

To begin the etching, the HCl valve is opened and HCl is introduced into the system at a rate of about 2.2 liters per minute to give an etching gas composition of approximately 85% H_2, 15% HCl. Etching is allowed to continue for as long as necessary to remove a desired amount of material from the substrate surface. Under these conditions, approximately 135 seconds of etching are needed to remove 1 mil from the substrate wafer. The HCl valve is then shut off and the etching gas is displaced by the pure hydrogen which continues to flow. After three to five minutes, the r-f generator is turned off if no deposition is to take place. Approximately 20 minutes is required for the block and the substrate wafer to cool to room temperature. The hydrogen is then displaced with helium and the block, wafer, and support rod are removed from the system. The standard taper joint is immediately cleaned to prepare the system for the next run.

Nature of the Etched Surfaces

Two typical germanium wafers etched in this manner are shown in Figures 4 and 5. In each figure, a low-magnification photograph of the wafer is shown. Although it is difficult to convey an impression of the surface finish which is achieved with this etching technique, these photographs were taken with the wafers mounted on a piece of graph paper so that the mirror reflection of the graph paper in the substrate surface could be seen. The central bright area, which is actually circular, appears elliptical in the photograph. In this area a 1000 Å silver film has been deposited by evaporation so that the surface could be examined by the multiple-beam interference technique.[6]

Also included in each figure are five micrographs; at the top are the micrographs obtained by the multiple-beam interference technique. In the center are micrographs obtained on a Leitz metallograph using incident vertical illumination. To the left is a bright-field micrograph, to the right is a micrograph obtained under phase-contrast conditions, each at 1000× magnification. For comparison, a bright-field micrograph obtained at 65× magnification is included at the lower right.

From these micrographs it is seen that the surface is essentially structureless even at 1000× magnification and is flat to within a few hundred Å over areas of about 1/10 inch on a side. Over larger areas, a gentle slope is observed in the interference fringes but no fine struc-

[6] A. Tolansky, *Surface Microtopography*, Interscience (Wiley), New York, 1960.

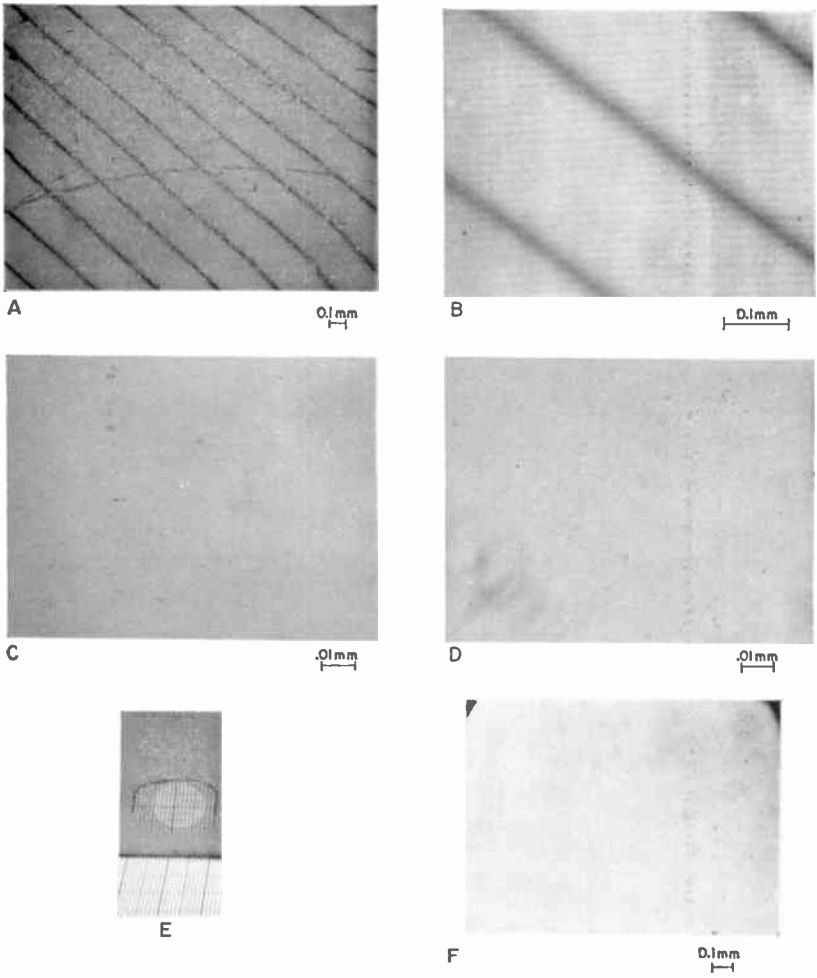

Fig. 4—Micrographs of a mirror smooth Ge surface produced by etching in HCl: (A,B) multiple beam interference micrographs; (C,D) micrographs of surface (left—bright field, right—phase contrast); (F) 65 × bright-field micrograph; (E) photographs of graph paper reflected in wafer surface.
wafer: 11/21/62-2, Ge doped with Ga to 7×10^{-4} ohm cm (S-7 wafer)
gas composition: 19.3% HCl, 80.7% H_2
gas flow rate: 12.89 liters/min
substrate temperature: 850°C (corrected)
etching time: 110 sec
thickness removed: 17.2 microns

ture can be detected. These surfaces, which are representative of those obtained routinely, are about as optically flat as finely mechanically polished germanium specimens except at the outer edge of the wafer.

Figure 6 shows a surface which was etched at too low a temperature. The structure on the surface is apparent in all micrographs but is especially noticeable in the multiple-beam interference micrographs.

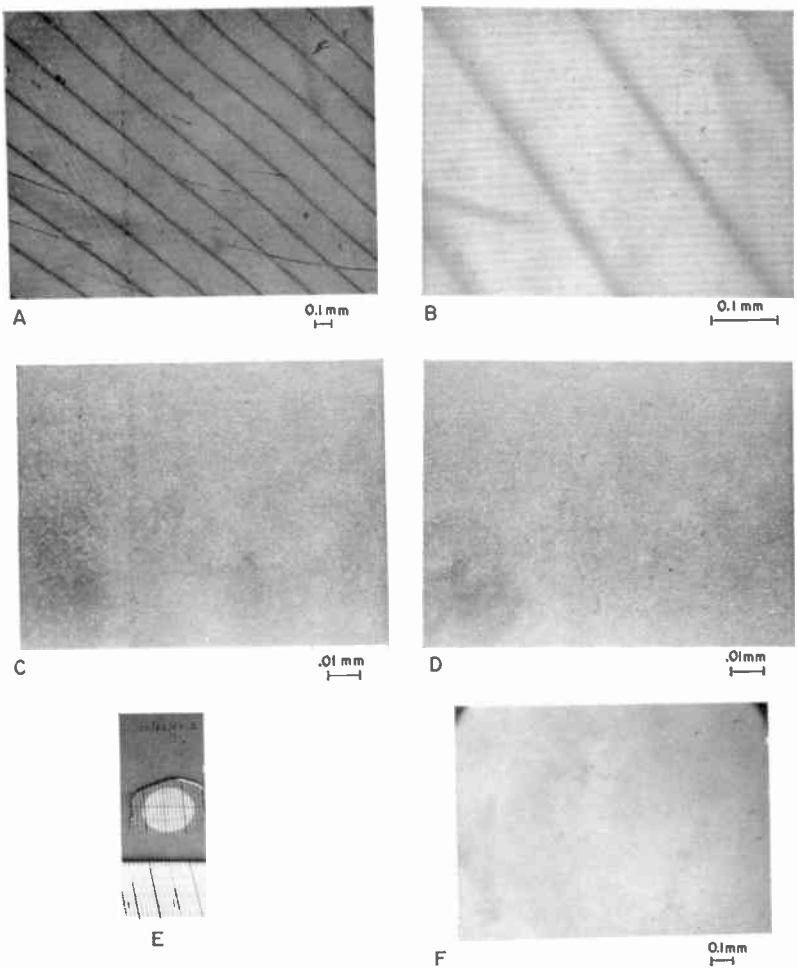

Fig. 5—Micrographs of Ge surface of wafer, 12/26/62-2, produced in the same manner as that shown in Figure 4, except that substrate temperature was 815°C (corrected) and the thickness removed was 19.2 microns.

At these temperatures the etch becomes selective, and pronounced pitting and haziness can be observed. Increasing the HCl concentration for a given etching temperature can also lead to selective etching, especially for the leading edge of a germanium wafer, as shown in Figure 7.

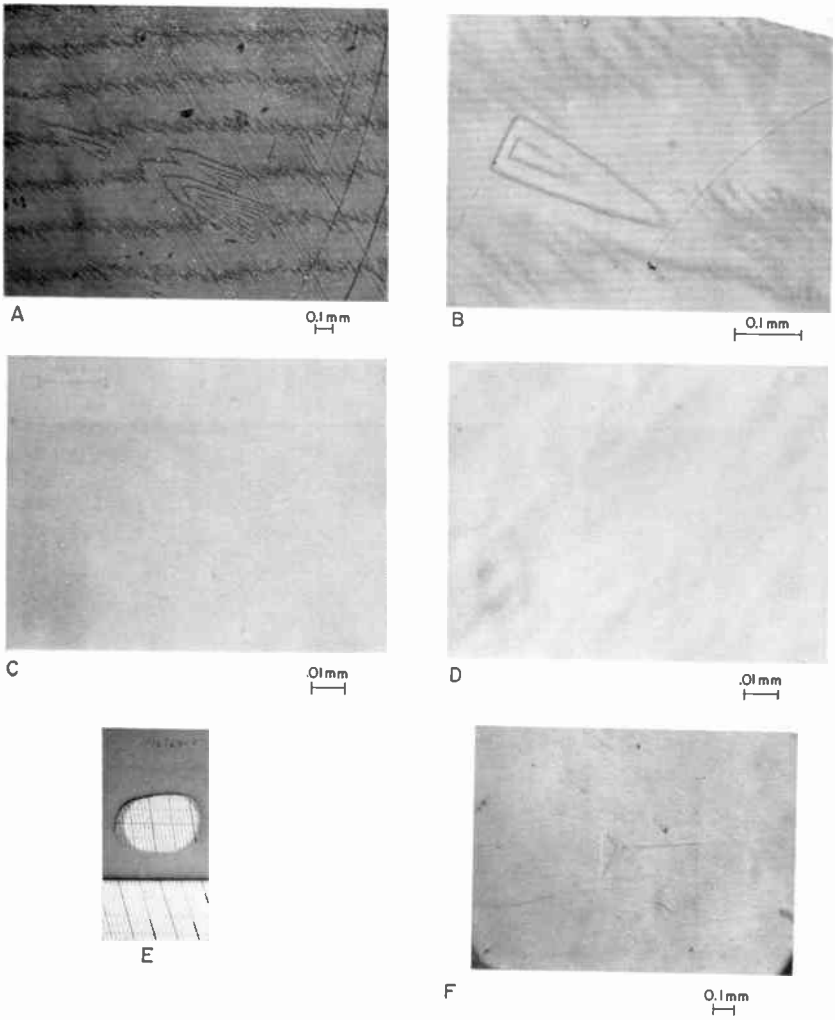

Fig. 6—Micrographs of mirror-smooth Ge surface of wafer, 1/16/63-1, produced in the same manner as those shown in Figures 4 and 5 except that substrate temperature was 790°C (corrected) and the thickness removed was 11.5 microns.

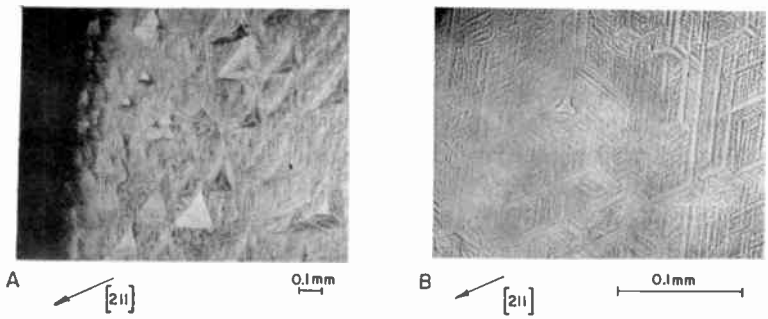

Fig. 7—Effect of increasing HCl concentration (for a given etching temperature).

Comparison of HCl Etching with Other Chemical Etches

A marked smoothing action has been noted for the gaseous etching of germanium wafers in HCl, as illustrated in Figure 8. A (111) oriented, p+ germanium substrate wafer was divided into halves; one half was etched in the gaseous HCl, the other in a reagent composed of

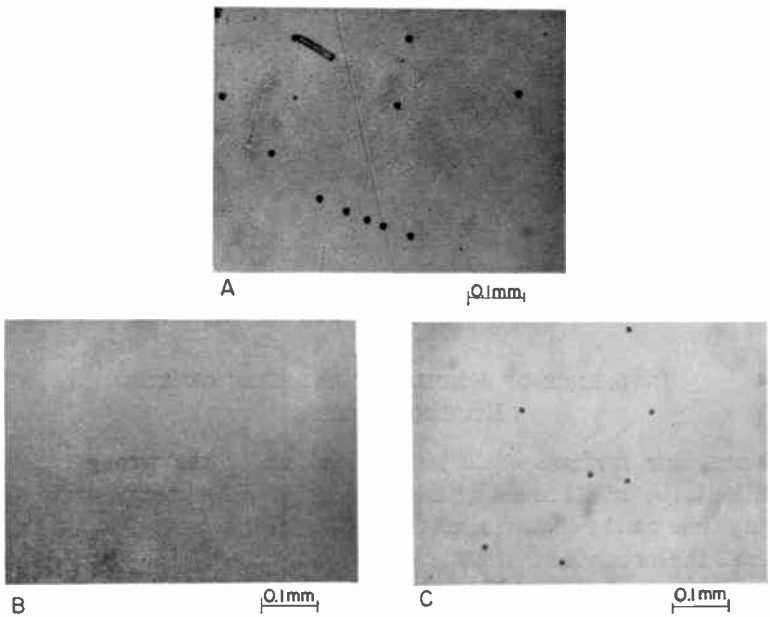

Fig. 8—Comparison of the surfaces left on a Ge wafer by etching: (A) one half of Ge wafer in 95 HNO_3-5 HF; (B) second half etched in HCl gas; (C) second half subsequently etched in 95 HNO_3-5 HF. (Wafer 1/30/63-1, Ge doped with Ga to 7×10^{-4} ohm cm (S-6 wafer); etching conditions standard; thickness removed during HCl etch not measured directly, estimated 15-20 μ; thickness removed during 95/5 etch not measured directly, estimated at 5-10 μ.)

95 parts by volume of concentrated HNO_3, 5 parts 49% HF (95/5 etch). Etching in this reagent was carried out because a treatment of this type is commonly used to prepare germanium substrate surfaces for subsequent epitaxial growth. After etching for a total time of 3 minutes, the wafer was rinsed and dried. This etch usually reveals scratches and pits in the substrate surface (Figure 8A). Close examination of the wafer etched in gaseous HCl reveals that almost no structure is present. (Figure 8B). The HCl etched surface was subsequently etched in the 95/5 reagent (Figure 8C) and it can be seen that the scratch marks are less pronounced than in Figure 8A, but the deep pits are again visible.

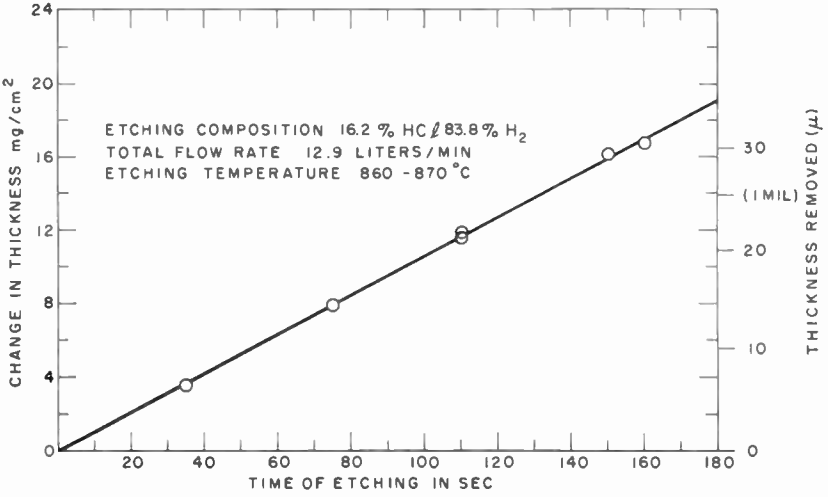

Fig. 9—Germanium removed during HCl etching versus etching time.

Influence of Etching Parameters on the Etching Process

Since poor surfaces could be obtained under the wrong etching conditions, the influence of gas flow rate, composition, temperature and etching time on the character of the etched surface were examined. In Figure 9 the amount of material removed from the surface as a function of etching time is plotted for a given temperature of etching and a particular composition of the etching gas. In Figure 10 the influence of etching-gas composition on the rate of removal of germanium is given. Finally, the amount of germanium removed from the surface as a function of temperature is plotted in Figure 11. These experiments show that the amount of germanium removed from the surface is

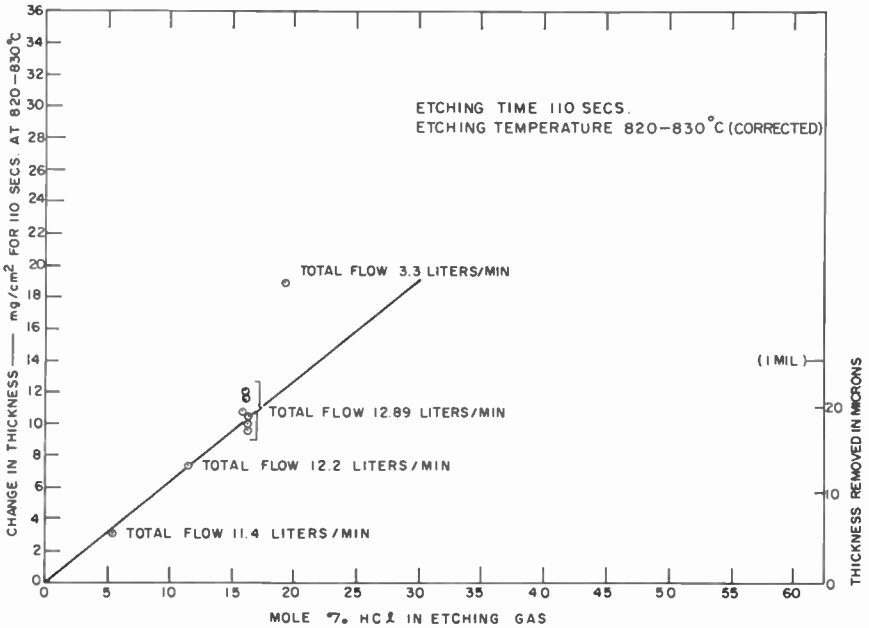

Fig. 10—Germanium removed during HCl etching versus composition of etching gas.

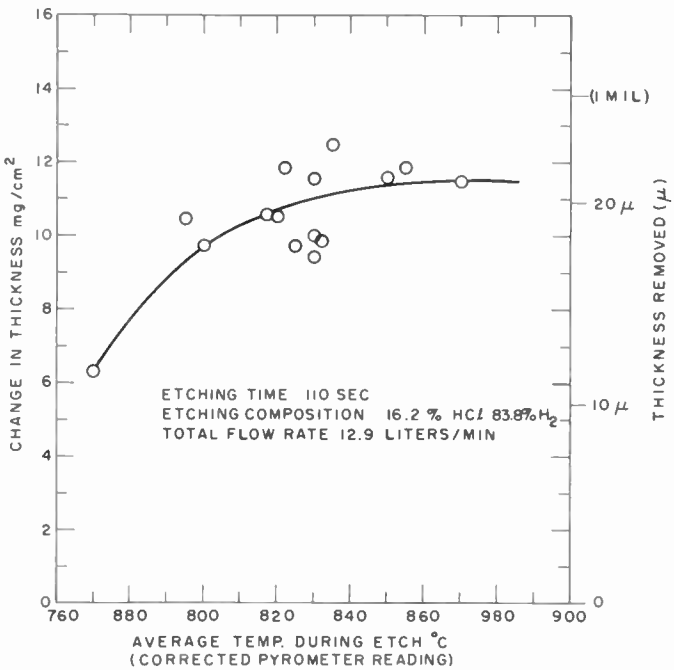

Fig. 11—Germanium removed during HCl etching versus temperature of etching.

linearly proportional to the time of etching and to the concentration of HCl in the etching gas, so long as the total gas flow is approximately constant. Furthermore, the amount of germanium removed from the surface is independent of the temperature of the etching, so long as the (corrected) temperature is above about 800°C. Reproducibility in the amount of the material removed during a given etch is observed to be about 10%.

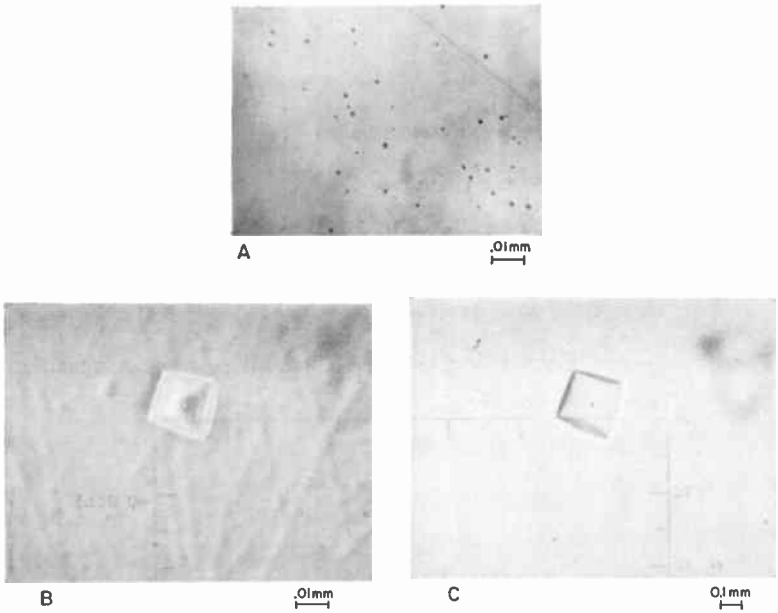

Fig. 12—Optical micrographs of a (100) germanium wafer etched in HCl under the same conditions as in Figure 4. (Wafer 1/15/63-1, Ge doped with As to 0.05 ohm cm (UW-6); thickness removed 16.1 microns.)

For all of the points plotted in Figures 9, 10, and 11 the surfaces from the etching were equivalent, having a mirror bright, optically flat finish similar to those shown in Figure 4 and 5, except for the surfaces prepared at too low a temperature which gave results similar to those of Figure 6. To obtain the best structureless surfaces at etching rates of about 1/2 mil per minute, the temperature must be above 800°C. Below this temperature the etch becomes selective and pits appear.

Surfaces obtained under the conditions described above but on germanium substrate wafers having different doping concentrations and different orientations, are not all alike. In every case the surface was shiny, but for some wafers surface structure was visible micro-

scopically and to the naked eye. 25-mil-thick phosphorus-doped germanium wafers having a resistivity of about 0.01 ohm-cm and 25-mil-thick wafers doped with gallium to about 1 ohm cm yielded excellent, mirror-finish surfaces. Wafers doped with arsenic to 0.06 ohm-cm, however, showed a distinct waviness similar to orange peel, apparent to the naked eye and visible under the microscope at low magnification. The surfaces did not have fine structure, however, and appeared quite bright and smooth over a short range.

When a (100) orientation wafer is used, square etch pits and marked background structure becomes visible, as seen in Figure 12. Other orientations have not yet been examined, but it is inferred that they will not etch as satisfactorily as the (111) oriented wafers.

ACKNOWLEDGMENTS

We would like to express our appreciation to B. R. Czorny, E. Cave, A. F. Mayer and N. Ciampa of RCA Electronic Components and Devices, Somerville, for their helpful discussion and suggestions, to A. Revesz, H. Hook, R. Evans and D. Kupper of RCA Laboratories who aided us in obtaining the multiple beam interference micrographs, and to G. W. Neighbor of RCA Laboratories for his help in setting up and using the Leitz Metallograph.

CHEMICAL POLISHING OF SILICON WITH ANHYDROUS HYDROGEN CHLORIDE*

By

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Summary—Clean, structureless surfaces have been prepared on silicon (111) wafers by means of etching in anhydrous HCl. The influence of temperature and gas composition on the etching rate has been determined. Commercially available cylinders of HCl have been analyzed to correlate the etching results with the purity of the HCl reagent used. The precautions necessary for obtaining smooth, structureless surfaces are described.

Introduction

THE PREPARATION of clean, structureless silicon surfaces is of great importance when these surfaces are to be used as substrates for the epitaxial deposition of silicon layers. To minimize defects in the epitaxial layers, it is essential to remove any oxide deposit as well as any mechanically worked region resulting from polishing of the substrates. Aqueous etches of hydrogen fluoride are normally used for this purpose, but the resulting surfaces are not structureless. Both fine pits and "orange peel" can usually be observed on such chemically polished silicon wafers, even when the rotating-beaker technique[1] of polishing is employed. Cave and Czorny have found that extremely smooth, structureless surfaces can be obtained on silicon substrates if anhydrous hydrogen chloride is used as the etching agent.[2] An investigation of the parameters influencing the etching has been undertaken, therefore, to determine the optimum values for these parameters and to devise better methods of controlling the polishing rate and the smoothness of the surface finish.

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* The etching of silicon wafers in $SiCl_4$ and in $HCl/SiCl_4$ mixtures was described in a "Recent News Paper" by K. Bean and P. Gleim, at the Electrochemical Society meeting September 30-October 3, 1963, in New York City. Their results, obtained in a different type of apparatus, are qualitatively similar to those reported here.

[1] D. L. Klein, G. A. Kolb, L. A. Pompliano, and M. V. Sullivan, "Electropolishing of n-Type Germanium and p- and n-Type Silicon," Abstract No. 46, Spring meeting of Electrochemical Society, May 1961.

[2] E. F. Cave and B. R. Czorny, "Epitaxial Deposition of Silicon and Germanium Layers by Chloride Reduction," *RCA Review*, Vol. 24, No. 4, p. 523, Dec. 1963.

APPARATUS

The etching experiments described in this paper were performed in a quartz tube that had an inner diameter of 1⅜ inches and was 30 inches long. This tube was centrally located in a 16-inch resistance-heated furnace. Over the central 2 inches of this furnace the temperature was constant within 5°C of the furnace-temperature setting of 1217°C. The inlet side of the quartz tube was joined to a Pyrex manifold that permitted the introduction of nitrogen, used as a purging gas, or of the hydrogen chloride in a hydrogen diluent, used for the etching. Gas flows were monitored with flowmeters and regulated by needle-bore stopcocks. All connections to the manifold were made of Monel,* Teflon,* or Pyrex* to reduce the probability of any chemical reaction between the apparatus and the hydrogen chloride. The outlet side of the quartz tube was open to the atmosphere, and the effluent gases were burned as they emerged from the tube. The spent gases were then carried away by a small exhaust hood placed over the outlet end of the tube.

A simple technique was used to properly position the silicon wafers inside the polishing apparatus. First, the substrate wafers were placed face down on a quartz flat attached to a hollow quartz push-rod. The assembly was then inserted into the etching tube through the open (exhaust) end and located within the furnace by means of the push-rod. A thermocouple inserted through the center of the hollow push-rod was used to monitor the temperature near the location of the wafers.

MATERIALS

The silicon used in this work was obtained in the form of (111) oriented slices about 10 mils thick. Their surfaces were either mechanically polished, using a 0.3-micron abrasive, or were lapped, using a 12- to 14-micron abrasive.

The anhydrous hydrogen chloride was obtained from two main sources. Initially, nine different samples were obtained from one supplier in lecture cylinders. These samples were analyzed by infrared absorption measurements, as described by Pierson.[3] Four of the samples were found to contain acetylene as a major impurity in concentrations of 0.1 to 0.2 per cent; four others were found to contain

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* Trade mark.

[3] R. H. Pierson, A. N. Fletcher, and E. St. Clair Gantz, "Catalog of Infrared Spectra for Qualitative Analysis of Gases," *Anal. Chem.*, Vol. 28, p. 1218, 1956.

carbon dioxide as the major impurity in concentrations of 0.3 per cent; and the ninth sample was found to contain no impurity in concentrations greater than 0.01 per cent. Acetylene proved to be particularly undesirable in the hydrogen chloride samples because discolored or matte surfaces were obtained when the samples containing this impurity were used for the chemical polishing. All the data on etching rate and surface finish reported in this paper were obtained with a tank of hydrogen chloride containing 0.3 per cent carbon dioxide, but no detectable acetylene.

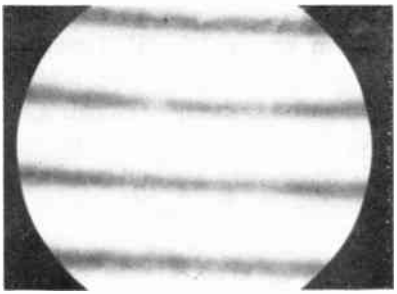
More recently, samples of Stauffer Chemical Company's anhydrous hydrogen chloride have been obtained. This material has been found to contain less than 0.01 per cent each of acetylene and carbon dioxide, and excellent results are obtained when it is used to polish silicon wafers.

Procedure

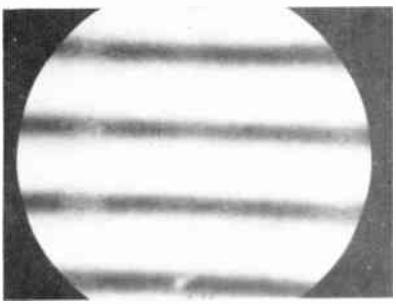
In the first step of the anhydrous hydrogen chloride method of polishing silicon wafers, the furnace and the quartz reaction tube are brought up to the desired etching temperature while a flow of nitrogen is passed through the apparatus. When the desired temperature has been reached and the apparatus has come to thermal equilibrium, a flow of about 8 liters of hydrogen per minute is established (this value provides a flow rate past the wafer of 14 centimeters per second) and the nitrogen flow is shut off. The silicon wafer on its quartz support is then introduced into the etching chamber and allowed to come to thermal equilibrium. An interval of about 5 minutes is sufficient for this purpose. The valve on the cylinder of hydrogen chloride is then opened, and the desired flow of this reagent is established. Etching usually proceeds for about ten minutes, after which time the hydrogen chloride valve is closed. The wafers are withdrawn from the furnace into the cooler region of the quartz tube, and after they have cooled to about 100°C, they are withdrawn from the apparatus.

Results

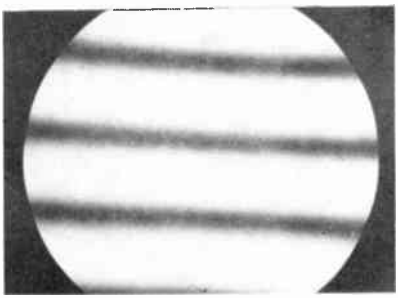
An impression of the types of surfaces obtained by mechanical polishing, by aqueous chemical etching and by anhydrous hydrogen chloride etching of silicon wafers is given by the series of interference micrographs shown in Figures 1-3. All the interference micrographs were obtained at 250× original magnification on a Zeiss interference microscope. Figure 1a shows the interference pattern obtained on a mechanically polished silicon wafer, Figure 1b shows the same wafer after 0.3 mil has been removed by etching in anhydrous 0.45%



(a)

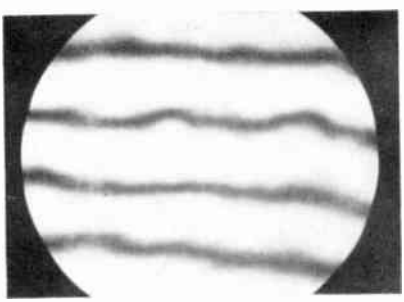


(b)

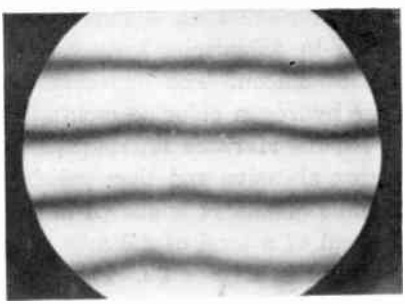


(c)

Fig. 1—Interference micrographs of a mechanically polished silicon surface before and after two degrees of hydrogen-chloride polishing: (a) mechanically polished wafer, (b) same wafer after 0.3 mil of hydrogen chloride polishing, and (c) same wafer after a total of 1 mil of hydrogen chloride polishing.



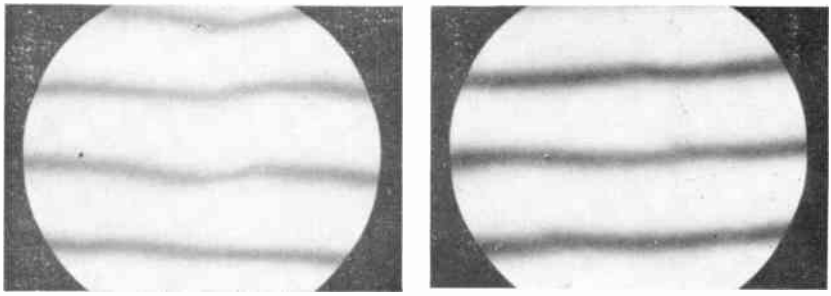
(a)



(b)

Fig. 2—Interference micrographs showing the combined effects of an aqueous chemical etch and anhydrous hydrogen chloride on a lapped silicon surface: (a) lapped silicon wafer after 4 mils of chemical polishing and (b) same wafer after 2.4 mils of hydrogen chloride polishing.

hydrogen chloride at 1275°C, and Figure 1c shows the wafer after a total of 1.0 mil has been removed by HCl etching. This amount (1 mil) of material is generally removed from a silicon wafer to ensure that all mechanical damage has been removed. Surfaces equivalent to those described above were obtained for silicon wafers etched at 1175°C at the same HCl concentration and for wafers etched at 1275°C in 3.0% hydrogen chloride. Thus, there is a range of parameters in which excellent surface finishes can be obtained from the anhydrous hydrogen chloride etching of mechanically polished substrates.



(a) (b)

Fig. 3—Interference micrographs showing two degrees of hydrogen chloride polishing of a lapped silicon surface: (a) 2.8 mils removed from the lapped surface and (b) 4.2 mils removed from the lapped surface.

An interference micrograph of a silicon wafer lapped with a 12- to 14-micron abrasive and then chemically polished for forty minutes with an iodine polishing etch is shown in Figure 2a. This procedure removed more than 4 mils of material. The same wafer was then etched in anhydrous hydrogen chloride to remove an additional 2.5 mils of silicon. The improvement in the smoothness of the surface after hydrogen chloride etching is apparent from Figure 2b.

An interference micrograph of a wafer lapped with a 12- to 14-micron abrasive and then polished with hydrogen chloride to remove 2.8 mils of silicon is shown in Figure 3a. The same wafer, after the removal of a total of 4.2 mils of silicon by hydrogen chloride etching, is shown in Figure 3b. The surface smoothness is much superior to that obtained by aqueous chemical polishing of the same type of lapped surface (cf. Figure 2a).

Figure 4 shows the etching rate of mechanically polished silicon wafers as a function of the concentration of hydrogen chloride present in the etching gas. These rates were derived from observed weight

losses during etching and are normalized to unit area. This graph shows that, except for very low concentrations of hydrogen chloride where the conditions probably approach true thermodynamic equilibrium, the etching rate is a linear function of the concentration over the range of concentrations studied.

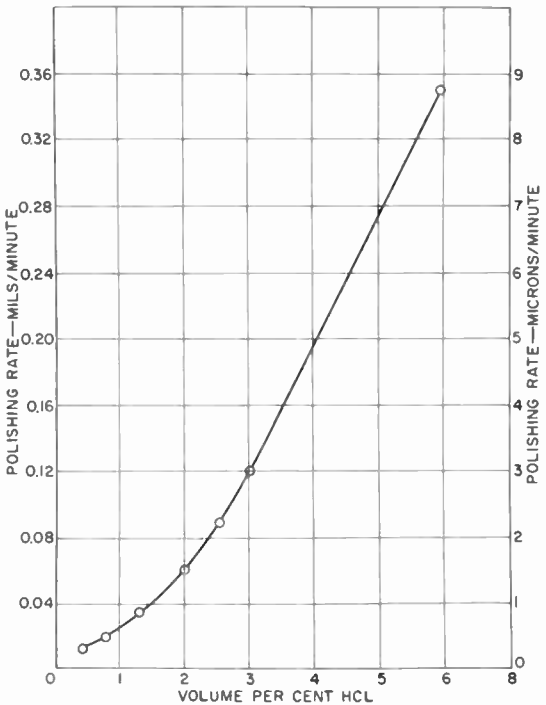


Fig. 4—Polishing rate as a function of the per cent (by volume) of hydrogen chloride in the etching gas at 1275°C.

The etching rate for mechanically polished silicon wafers as a function of temperature, for several different compositions of etching gas, is shown in Figure 5. These curves show that the etching rate is not strongly influenced by temperature. No influence on the etching rate was observed for different resistivity types or different resistivity levels, or different initial surface finishes. The mechanically polished wafers and the lapped wafers behaved identically at both high and low etching rates. For these experiments, a temperature of 1275°C and a hydrogen chloride concentration of 0.6 per cent were used.

Figure 6 shows the useful polishing region for the system investigated. The maximum polishing rate is defined by the upper boundary

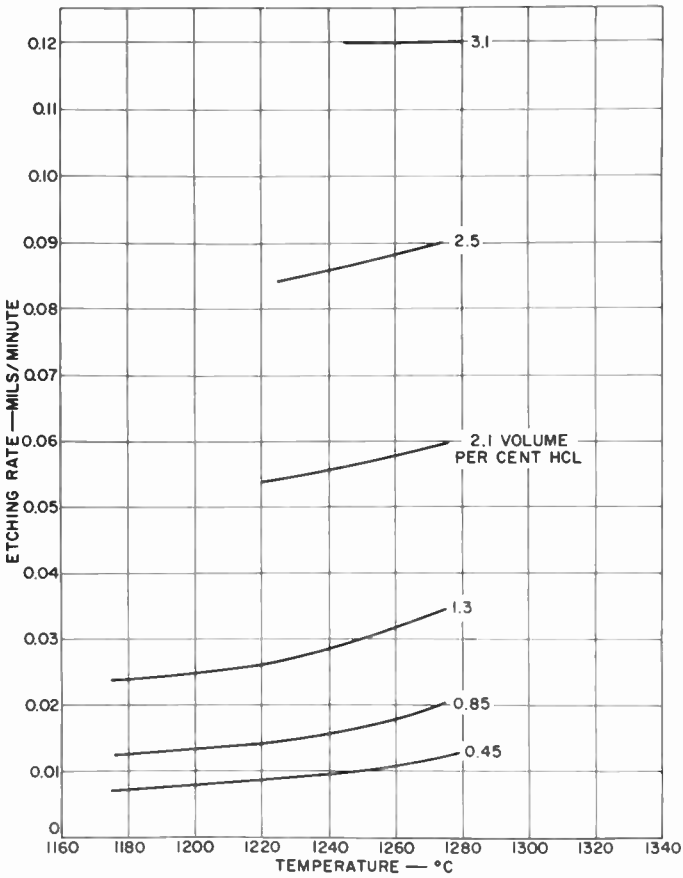


Fig. 5—Etching rate of the silicon wafers as a function of temperature for various concentrations of hydrogen chloride.

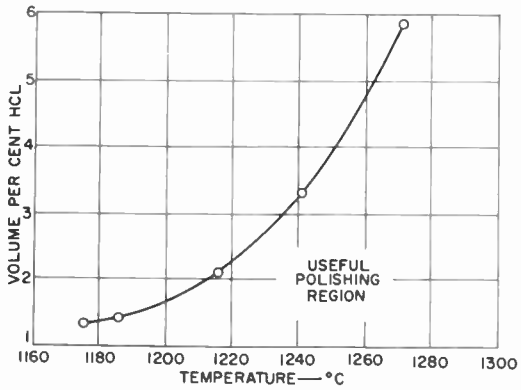


Fig. 6—Maximum per cent (by volume) of hydrogen chloride in the etching gas as a function of temperature.

of the useful polishing region and is found to be a function of temperature. If this rate is exceeded by increasing the flow rate of the hydrogen chloride (increasing the concentration of hydrogen chloride in the etching gas), the gas will selectively etch the silicon, and the polished surfaces become pitted, as shown in Figure 7. The hexagonal pits shown in this figure are similar to the ones that, as described below, are formed when the warm-up time of the wafers prior to etching is too short. Thus, for 8 liters per minute of hydrogen flow, any hydrogen chloride flow rate up to and including the maximum flow

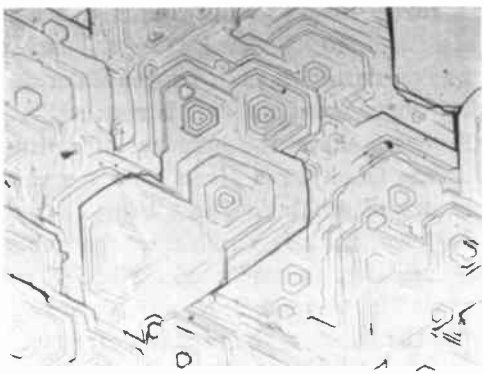


Fig. 7—Pitting of the silicon wafers that results from an excessive flow of hydrogen chloride.

will produce a polished surface at any given temperature. It is the limitations on the hydrogen chloride flow rate that form the area termed "useful polishing region" in Figure 6.

The maximum polishing rate, although primarily limited by temperature, is also influenced by the following factors.

(1) *Moisture Content of the Etching Mixture*—Any leak in the apparatus effectively introduces moisture into the system and limits the maximum useful polishing rate. The maximum polishing rate could be increased at low etching temperatures by inserting a methanol dry-ice trap (at —60°C to —70°C) into the hydrogen chloride gas line. The increase in maximum polishing rate apparently results from a reduction in the moisture content of the hydrogen chloride.

(2) *Purity of the Hydrogen Chloride*—As described earlier, the purity of hydrogen chloride varies from cylinder to cylinder and from vendor to vendor. The variation in the purity of hydrogen chloride affects the values of the maximum polishing rate given in Figure 6.

Thus, when different cylinders of hydrogen chloride are used, the useful polishing regions will generally be somewhat different from that shown in Figure 6. For example, at 1217°C, a variation in the maximum polishing rate by a factor of 2 was observed among several different cylinders of hydrogen chloride. These differences depended to a large extent on the carbon dioxide content of the gas—the higher the carbon dioxide content, the lower the maximum useful polishing rate. The carbon dioxide probably reacts with hydrogen in the furnace to form water, which has already been shown to be undesirable.

(3) *Warm-up Time of the Wafers*—If the silicon wafers are introduced into the furnace while the hydrogen chloride gas is flowing, their surfaces are found to be pitted after the etching operation is completed. If the concentration of hydrogen chloride in the etchant gas is increased, a longer warm-up time is required before the etching can be begun. Figure 8 shows the influence of warm-up time on the quality of the surface finish for a given hydrogen chloride concentration and temperature of etching. The pitting that occurs when the warm-up time is insufficient is similar to that obtained when the etching rates are excessive, as mentioned earlier. Figure 8 shows that as the warm-up period increases and the wafer more closely approaches the temperature of the furnace, the pitting decreases. Similar pitting can occur if the wafer is withdrawn from the furnace while the hydrogen chloride is flowing.

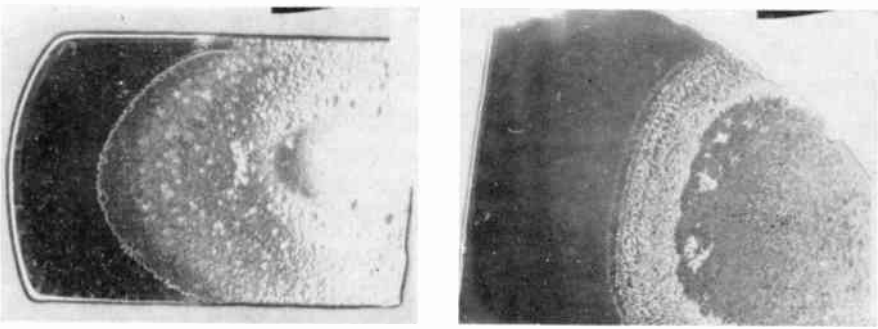
Limitations of the Anhydrous HCl Polishing Method

Two factors tend to limit the use of anhydrous HCl for polishing silicon wafers. First, when this polishing technique is employed, the leading edge of the wafer (the one nearest the HCl source) is etched more rapidly than the trailing edge. However, if a turbulence is introduced into the gas stream, this difference in etching rate can probably be eliminated.

Second, because of the high temperature required to obtain smoothly etched surfaces, the application of the anhydrous HCl polishing technique is restricted primarily to undiffused substrate wafers. This restriction results from the fact that when a diffusion step has been performed on the wafer prior to etching, the etching cycle must be substantially shortened to ensure that further diffusion of the wafer is held to a minimum.

In an attempt to overcome the limitation imposed by the high-temperature requirement of hydrogen chloride polishing, a chlorine etchant was tested as a substitute for the hydrogen chloride. Although

chlorine attacks silicon at lower temperatures than hydrogen chloride, the surfaces were always found to be attacked preferentially, as reported by Gualtieri.[4] This behavior was also observed for etching mixtures of chlorine and nitrogen over the entire composition range at temperatures from 500°C to 900°C.



30 sec. warm-up 60 sec. warm-up

90 sec. warm-up 120 sec. warm-up

Fig. 8—Pitting of the silicon wafers that occurs when the flow of hydrogen chloride is begun before the wafers have been allowed a sufficient warm-up period.

CONCLUSIONS

The polishing of silicon wafers in anhydrous HCl has been found very satisfactory for several reasons:

(1) The polishing rate can be accurately controlled, and the

[4] J. G. Gualtieri, M. J. Katz and G. A. Wolff, "Gas Etching and Its Effect on Semiconductor Surfaces," *Zeitschrift für Krist.*, Vol. 114, p. 11, 1960.

polycrystalline p-type germanium layers having an average crystallite diameter of 0.3 to 0.5 micron, a resistivity of about 0.02 to 0.05 ohm-cm and a mobility of 20 to 140 cm^2/volt-sec. By adding arsine to their germane, they obtained n-type deposits. The surfaces of their films appeared reasonably smooth at 15,000× magnification.

In an attempt to deposit smooth, single-crystal layers of germanium epitaxially on germanium substrates, Davis and Lever[2] employed the pyrolysis of germane. Although they were unsuccessful in preparing smooth surfaces, they did obtain single-crystal deposits when the substrate was held at a temperature of approximately 900°C. Their depositions were carried out at reduced pressures in a vacuum system whose ultimate vacuum was stated to be 10^{-6} mm Hg. Their substrates were cleaned by chemical etching followed by baking in hydrogen at about 900°C. No electrical measurements were reported for these layers, nor was the purity of their germane given.

With the recent improvement in the synthesis of germane in high yields reported by Macklen,[3] and by Griffiths[4] and with the newly developed technique of etching germanium substrates in gaseous HCl at high temperatures,[5] a reinvestigation of the preparation of germanium layers by pyrolysis of germane seemed warranted. Additional information which has been published by Boudart et al,[6,7] on the kinetics of the pyrolysis of germane was also very encouraging. They found that decomposition on the surface proceeds an order of magnitude faster than the homogeneous gas-phase reaction. They also postulated that during the decomposition, GeH_x radicals migrate freely on the germanium surface, a situation which should be favorable for the deposition of layers having smooth surfaces and high crystalline perfection.

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[2] M. Davis and R. F. Lever, "Vapor Phase Crystal Growth of Germanium from Thermally Decomposed Germane," *Jour. Appl. Phys.*, Vol. 27, No. 7, p. 835, July 1956.

[3] E. D. Macklen, "Preparation of Germane. Part I. Reaction between Lithium Aluminium Hydride and Germanium Tetrachloride," *Jour. Chem. Soc.* (London), p. 1984, April-Aug. 1959; "Preparation of Germane. Part II. Reaction between Sodium Borohydride and Germanium Tetrachloride," p. 1989.

[4] J. E. Griffiths, "Mongermanes—Their Synthesis and Properties," *Inorganic Chemistry*, Vol. 2, p. 375, April 1963.

[5] J. A. Amick, E. A. Roth, and H. Gossenberger, "The Etching of Germanium Substrates in Gaseous Hydrogen Chloride," *RCA Review*, Vol. 24, No. 3, p. 473, Sept. 1963.

[6] K. Tamaru, M. Boudart, and H. Taylor, "The Thermal Decomposition of Germane. I. Kinetics," *Jour. Phys. Chem.*, Vol. 59, No. 9, p. 801, Sept. 20, 1955.

[7] P. J. Fensham, K. Tamaru, M. Boudart, and H. Taylor, "The Thermal Decomposition of Germane. II. Mechanism," *Jour. Phys. Chem.*, Vol. 59, No. 9, p. 806, Sept. 20, 1955.

The Synthesis of Germane

Until 1957, the production of germane was severely limited because it was obtainable only in low yields from starting materials which were themselves difficult to prepare. With the availability of the powerful reducing agent lithium aluminum hydride, it was expected that larger yields of germane could be obtained. However, the reducing power of this mixed hydride is so great that the reduction product consists mostly of elemental germanium. In 1957 Piper and Wilson[8] showed that sodium borohydride is a more-satisfactory reducing agent for this synthesis, being much milder than lithium aluminum hydride. Using germanium dioxide as the starting material, they obtained yields of germane in excess of 50%.

In the preparation of reagent germane used here, germanium dioxide was again employed as the starting material. When the oxide is added to concentrated aqueous HCl,* conversion of some of the oxide to chloride takes place. Addition of aqueous sodium borohydride dropwise to this combination results in the liberation of a germane–hydrogen mixture.

Figure 1 shows a schematic of the reaction apparatus used in the preparation of germane. A solution of about 110 grams of sodium borohydride† in 450 ml of water is filtered into the dropping funnel, (A). This solution is then added dropwise to a slurry consisting of 104 grams of GeO_2‡ in a solution of 365 grams of constant boiling (20.24 wt.%) HCl in 300 ml of water. The concentration of HCl is not critical but at higher concentrations the formation of hydrogen is favored over the formation of germane and at lower concentrations the conversion of germanium dioxide to germanium tetrachloride becomes inefficient, especially after most of the HCl has been consumed in the reaction. During addition of the borohydride, the slurry is constantly stirred with a magnetic stirrer in the flask (B). The resulting gaseous products, mostly hydrogen and germane, are dried by

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[8] T. S. Piper and M. K. Wilson, "The Preparation of Germane," *Jour. Inorganic and Nuclear Chem.*, Vol. 4, p. 22, 1957.

* In 1961, Drake[9] published a modification of Macklen's method in which acetic acid was substituted for the HCl. With this substitution, the reaction becomes more efficient in terms of the borohydride required.

[9] J. E. Drake, "The Preparation of Some Germanium Hydrides," U. S. Atomic Energy Comm., Univ. of California Radiation Lab, UCRL 9709, May 18, 1961; J. E. Drake and W. L. Jolly, "Hydrides of Germanium," *Jour. Chem. Soc.* (London), p. 2807, Part III, 1962.

† Sodium Borohydride, 98%+ from Metal Hydrides, Inc., Beverly, Mass.

‡ Eagle-Picher Company, Miami, Oklahoma.

passing them through the dry-ice traps (C). A silicone oil bubbler (D) is provided as a safety valve in the event that a block occurs in the purification train during operation. The gas mixture is next passed through a 36-inch column of molecular sieve (E),* which serves to dry the gases still further and to remove any hydrogen chloride from the gas stream. Before beginning a run, this column is heated to 350°C and purged with flowing helium for 24 hours and then cooled to room temperature. Germane condenses in the liquid nitrogen traps (F) and by-product hydrogen leaves the system through bubbler (G) filled with silicone oil.

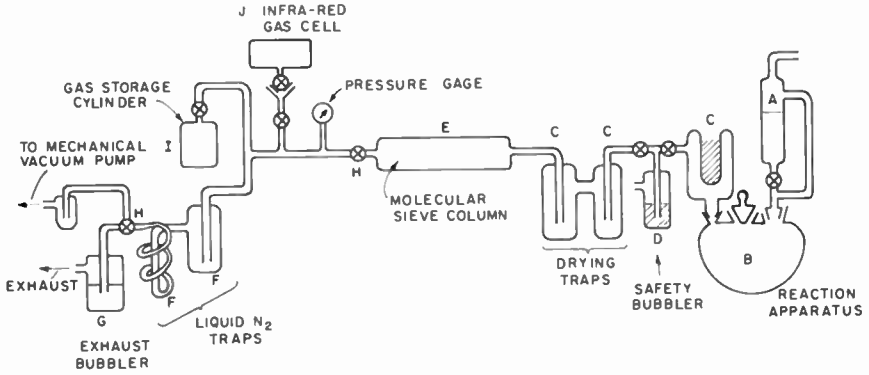


Fig. 1—Apparatus for the preparation and purification of germane.

At the conclusion of the reaction, the germane retained in the molecular sieve column is displaced with flowing helium and condensed in the liquid nitrogen traps (F). The system between the stopcocks (H) is then evacuated and sealed off while the germane is held at liquid-nitrogen temperature. Finally the germane is transferred into the gas cylinder (I) which has previously been evacuated and cooled to liquid-nitrogen temperature. An infrared sampling cell (J) is used to collect samples for analysis. After all of the germane has been transferred to the gas cylinder, the system is again pumped down to a pressure of less than 1.0 micron to remove any noncondensable gases, primarily hydrogen. The cylinder is then closed off and allowed to warm to room temperature. It is then cooled again to liquid nitrogen temperature and again pumped down. After two or three cycles, the pressure in the system no longer rises when the valve between the

* 5A Molecular Sieve, Linde Co. Division, Union Carbide Corp.

cylinder and the system is opened, the cylinder being at liquid nitrogen temperature. The relative concentration of noncondensable gases in the cylinder at room temperature should then be well below 1 part per million.

The germane which collects in the liquid nitrogen traps is a white solid which melts, on warming, to a colorless liquid. The yield for the synthesis reaction described above is generally about 35% calculated on the germanium oxide used. A large quantity of a reddish brown solid usually forms in the flask (B) as the reaction proceeds. This is presumed to be the polymeric germanium hydride $(GeH_2)_x$ which has been reported by earlier workers.[3] This by-product is probably the cause of the low yields obtained.

Analysis of the Germane

The germane was analyzed by three techniques: gas chromatography, infrared spectroscopy, and mass spectrometry. The gas chromatograms were obtained with a Perkin-Elmer 154 C Vapor Fractometer using a silica-gel column. This analysis showed that the germane had less than 1% hydrogen and no trace of water. Because air is invariably introduced into the Fractometer during sampling, it can only be stated from this analysis that its concentration is less than 1%. No peaks were observed which could not be interpreted. The infrared analyses were obtained using a Perkin-Elmer 221 infrared spectrophotometer and a 10-cm gas cell. The only absorption peaks observed were those previously reported for germane.[10,11] No water or HCl absorption peaks were detected. Neither oxygen nor nitrogen have characteristic absorption bands in the infrared.

Mass spectrometric analyses were obtained using a Consolidated 21-620 mass spectrometer. These spectra showed that the concentration of air in the germane was less than 0.02%. Small peaks characteristic of hydrocarbons, water and carbon dioxide were present as background in the instrument. If any of these were present in the germane, their concentration was well below the level of 0.02%.

Results from these three analytical techniques thus confirm the purity of the germane. The contaminant present in the greatest amount is probably hydrogen. Since the depositions were to be carried out in hydrogen, this was not troublesome. Other than hydrogen, the con-

[10] W. B. Steward and H. H. Nielsen, "The Infrared Absorption Spectrum of Germane," *Phys. Rev.*, Vol. 48, No. 11, p. 861, 1935.

[11] J. W. Straley, C. H. Tindal and H. H. Nielsen, "The Vibration-Rotation Spectrum of GeH_4," *Phys. Rev.*, Vol. 62, p. 161, 1942.

tamination level is below 2 parts in 10,000. Water and oxygen are below this level by at least one order of magnitude. No diborane (from the decomposition of sodium borohydride) or HCl are present in detectable amounts.

Deposition of Germanium Layers

The apparatus in which the germanium layers were deposited is shown in Figure 2. In this apparatus, provision is made for etching the substrate surface in gaseous HCl just prior to growth. Following

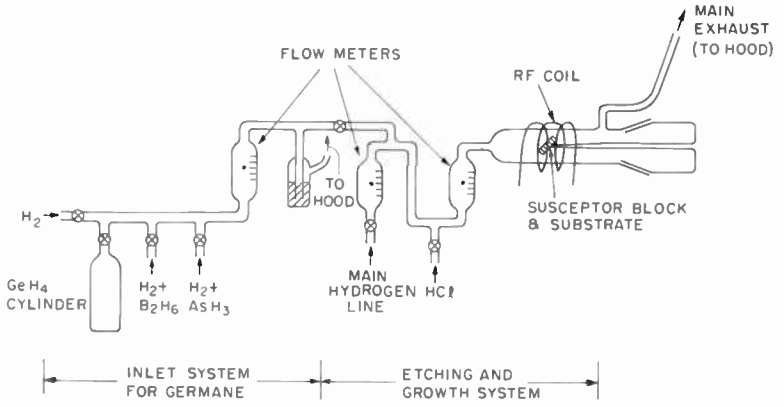


Fig. 2—Diagram of apparatus for the growth of germanium layers by the pyrolysis of germane.

the HCl etch, the substrate has a clean, brightly polished surface which is ideal for epitaxial growth. The manner of preparing these germanium substrates and the characteristics of the HCl etched surfaces prepared in this apparatus have already been described.[5]

The reagents employed in the growth include germane, synthesized as described above, and palladium-diffused hydrogen.* When it was desired to produce doped layers, either arsine diluted in hydrogen to 50 ppm or diborane diluted in hydrogen to the same concentration were employed.† Substrates were (111) oriented single-crystal slices of germanium doped to a resistivity of about 7×10^{-4} ohm-cm with gallium or to about 0.05 ohm-cm with arsenic. The susceptor block on which the substrates were heated was described earlier.[5]

* Palladium diffuser from Engelhard Industries, Newark, N. J.
† Air Reduction Company, Jersey City, N. J.

The concentration of germane in the entrant gas was kept low, typically about 0.005% by volume, so that the same gas flows could be used for the growth of single-crystal germanium layers over a wide temperature range. For growth in the neighborhood of 800°C, this concentration could be increased by a factor of at least 10 without affecting the crystalline nature of the deposit perceptibly.

The best growth conditions required rapid flows of hydrogen to minimize decomposition of the germane in the gas phase. If gas phase (homogeneous) nucleation takes place upstream from the substrates, randomly oriented crystallites may settle onto the substrate surface and polycrystalline layers usually result. With sufficiently high hydrogen flow, pyrolysis of the germane is minimized until the reagent impinges on the substrate surface. Hydrogen flows were typically about 10 liters per minute which, in this apparatus, corresponds to a linear velocity of about 8 cm per sec.

Before growth of a germanium layer on a freshly etched substrate, the r-f generator is adjusted, while the hydrogen stream is flowing, so as to bring the temperature of the substrate from that used in the etching to that desired for growth. A few minutes are then allowed for the substrate to come to a steady-state temperature. During this interval, a flow of germane and, if desired, dopant gas is established in the inlet system. The flow rate of each of these gases is adjusted to desired values with the help of the flow meter, and the effluent is allowed to pass out through the inlet bubbler (cf. Figure 2). About 50 cc/min of hydrogen is added to this gas stream to ensure thorough mixing of the gases and rapid attainment of a constant composition.

To begin growth, the stopcock separating the inlet apparatus from the growth apparatus is opened. At this time, the column of liquid in the bubbler provides sufficient back pressure so that all of the gas now enters the main hydrogen-gas stream and passes through the deposition chamber. The presence of germane in the deposition chamber can readily be detected by the appearance of the flame of the exhaust gases. The flame, upon addition of the germane, acquires a yellow inner cone similar to that obtained with methane.

A run typically lasts about one hour with approximately 1/4 mil of germanium being deposited in that interval. At the conclusion of a run, the stopcock connecting the inlet system with the main hydrogen flow is turned off. The disappearance of germane from the system can be observed by watching the flame of the effluent gases and, about 5 minutes later, the r-f generator is turned off and the substrate is allowed to cool to room temperature in flowing hydrogen.

Characteristics of Deposited Germanium Layers

Initially, approximately 1/4-mil thick layers were prepared from the pyrolysis of germane without introducing any additional doping agent. Over the temperature range ~ 700°C to 900°C, (corrected) bright, mirror smooth deposits were obtained, as shown in Figure 3. The pyrometer used in this work cannot be read precisely for true temperatures below 750°C. Therefore, the lower temperature limit at which smooth deposits are obtained was not estimated accurately.

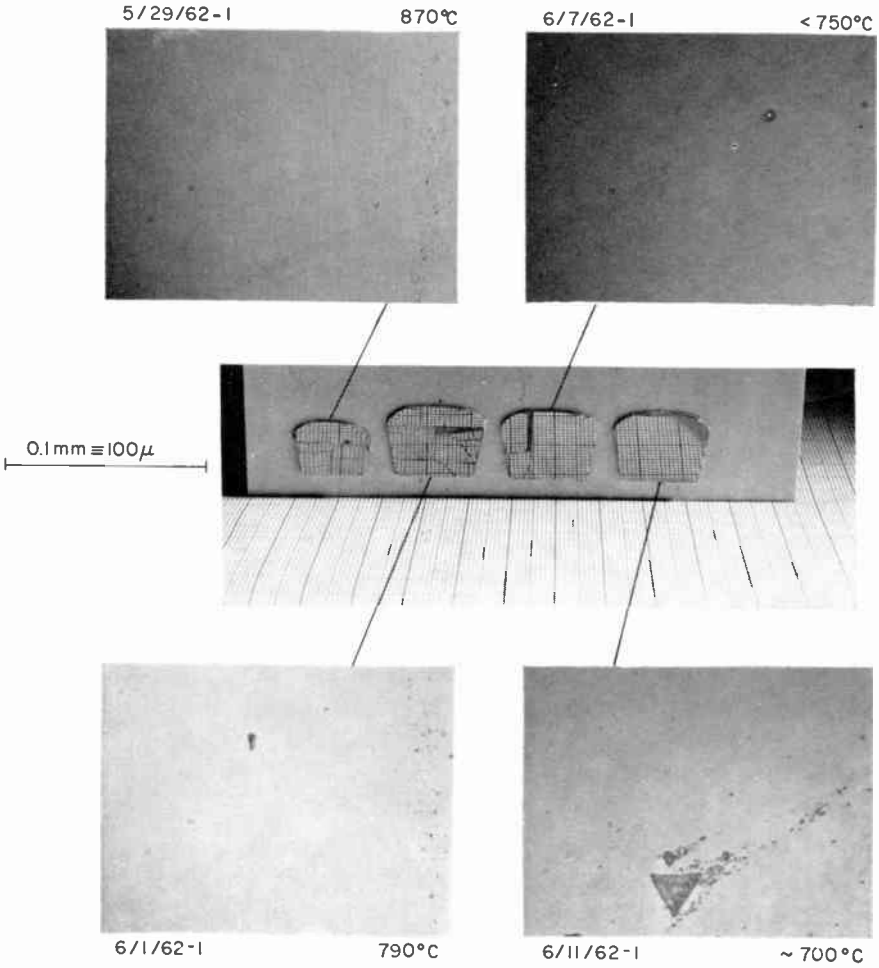


Fig. 3—Micrographs and photograph of the "as grown" surfaces of germanium epitaxial layers prepared by pyrolysis of germane at different temperatures (corrected) (original magnification ×650; thickness of layers about 6 microns).

Defects begin to appear in the grown layers at temperatures estimated as in the neighborhood of 700°C (corrected).

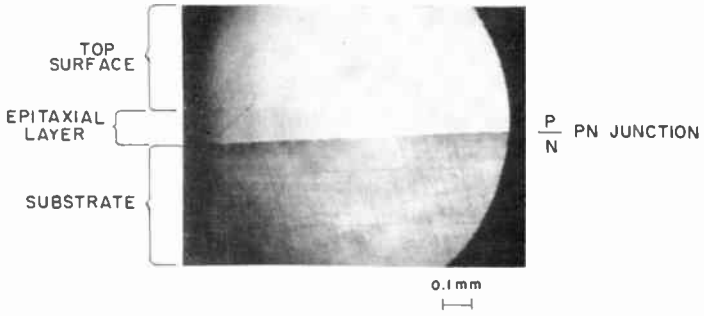
In order to give an impression of the surface finish of the grown layers, a photograph of the wafers is included in Figure 3. Prior to obtaining this photograph, several of the wafers were cut apart and angle lapped. The cracks where the pieces have been rejoined can readily be seen. The surrounding micrographs, obtained at an original magnification of 650× show that the surfaces of the layers have very little structure. The characteristic triangular defects seen by Davis and Lever[2] are absent in these micrographs except for a few scattered defects seen in the deposits prepared at the lowest temperature.

The crystallinity of the layers was evaluated by two techniques. Laue back-reflection patterns were obtained which give information about the crystallinity to a depth of approximately 1 mil. Selective chemical etches were also used to reveal etch pits in the deposited layers. Both of these techniques show that the layers are highly crystalline and oriented in the same sense as the substrate. Electron diffraction has also been attempted with these layers but the results have been ambiguous. The layers are apparently so smooth that the patterns originate from small projections on the surface, possibly oxide particles.

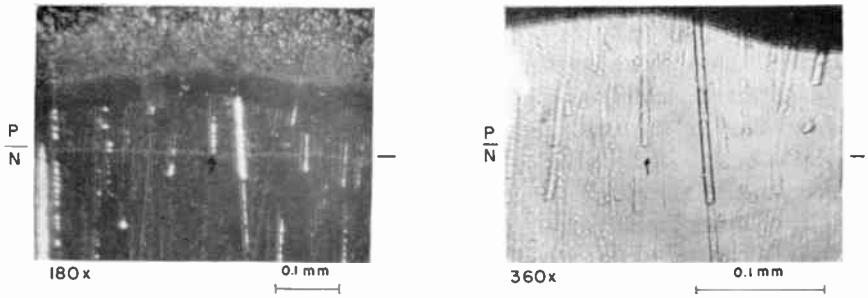
The interface region between the substrate and the grown layer is shown in Figure 4 for a p-type layer grown on an n-type substrate. In Figure 4a, the junction is delineated by angle lapping the wafer at 2° followed by copper staining the junction region. In Figure 4b the same wafer has been etched to reveal dislocations. The etch pits are seen to be triangular, of the same orientation and approximately the same concentration on both sides of the junction.

The thickness of the deposited layers was determined both by angle lapping/staining (Figure 4a) and by infrared interference (Figure 5). The maxima and minima in the infrared interference pattern are quite pronounced, indicating that the layer is uniform in thickness and that the surfaces are essentially plane parallel.

Resistivities of the germanium layers prepared by pyrolysis of germane without deliberate addition of doping agents were about 1 ohm cm p-type and were measured by two methods. For the deposits on n-type substrates, a four-point probe was used to estimate the resistivity. For deposits prepared at about 850°C (corrected) on heavily doped p-type substrates, a different technique was used. A junction was prepared within the epitaxial layer by in-diffusion of arsenic. Mesas were then etched in the layers to give diodes. The capacitance–voltage characteristics of these diodes were determined



(a) ANGLE LAPPED(2°) AND STAINED WITH COPPER



(b) ETCHED TO BRING OUT DISLOCATIONS

Fig. 4—Typical epitaxially grown layer of germanium prepared by pyrolysis of germane (growth temperature 860°C (corrected); thickness about 6 microns).

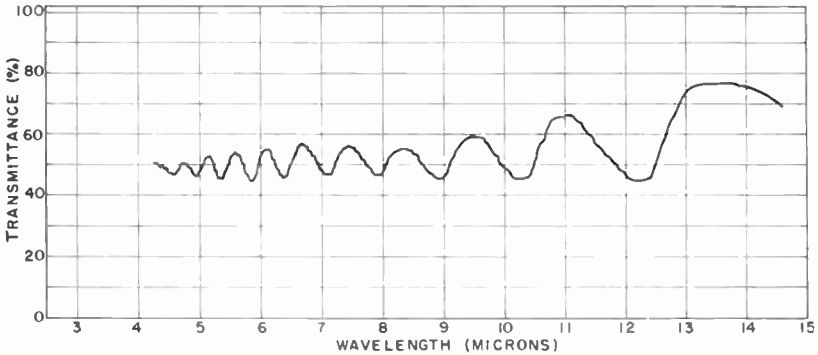


Fig. 5—Typical infrared interference pattern from an epitaxially deposited germanium layer prepared by pyrolysis of germane.

(Figure 6) and, knowing the area of the junction, the resistivities were calculated.[12] The agreement between these two types of measurement suggests that very little dopant is transferred from the substrate or susceptor into the growing layer during deposition. The capacitance–voltage characterisics of Figure 6 all show excellent square-root-law

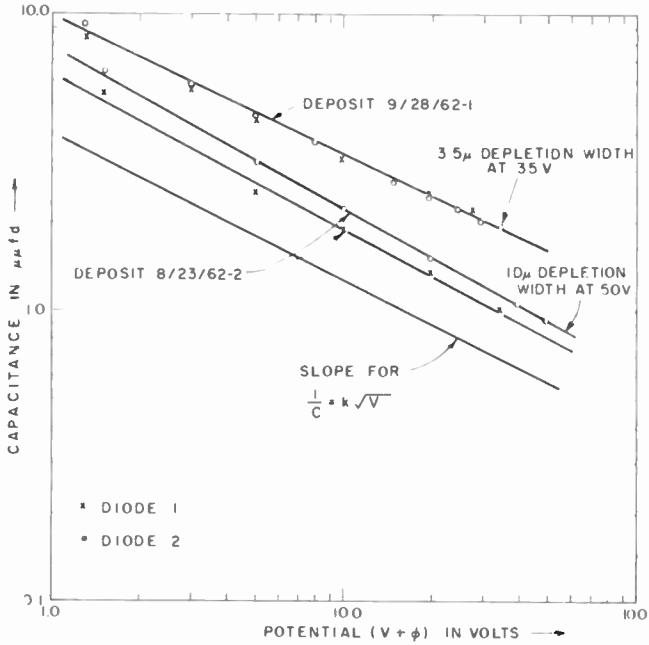


Fig. 6—Capacitance versus voltage characteristics for diodes prepared in epitaxial germanium deposits. Deposit 8/23/62-2: growth temperature 860°C (corrected); thickness 20 microns (infrared interference). Deposit 9/28/62-1: growth temperature 845°C (corrected); thickness 7 microns (infrared interference).

curves, demonstrating that the doping concentration is uniform throughout the region in which the space-charge depletion layer forms.

The current–voltage characteristics of these junctions formed within the epitaxial layer were also determined, as shown in Figure 7. Reverse breakdowns are observed to be very sharp, and the breakdown potential is in good agreement with that calculated for avalanche breakdown in the epitaxial layer. Saturation currents are low and uniform from diode to diode.

[12] J. Hilibrand and R. D. Gold, "Determination of the Impurity Distribution in Junction Diodes from Capacitance-Voltage Measurements," *RCA Review*, Vol. 21, No. 2, p. 245, June 1960.

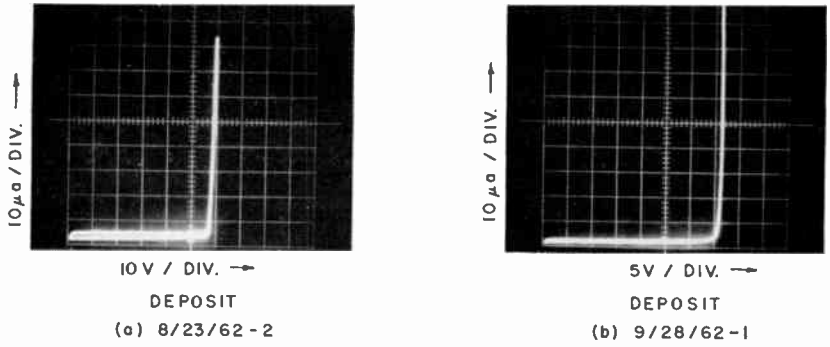


Fig. 7—Reverse-bias characteristics of diodes formed in germanium epitaxial layers prepared by pyrolysis of germane (cf. Figure 6). (Courtesy of B. R. Czorny).

These diode characteristics are reported to be as good as for diodes prepared in the best germanium epitaxial layers produced by reduction of germanium chloride with hydrogen. It is therefore concluded that germanium epitaxial layers equivalent in a crystallographic and electrical sense to layers prepared by reduction of germanium chloride can be prepared by the pyrolysis of germane. A discussion of the properties of the doped layers and the relationship between the concentration of dopant in the gas stream and the doping concentration in the deposited layers is planned for a future paper.

Acknowledgment

For the fabrication of diodes and the measurement of their capacitance–voltage and current–voltage characteristics, we are indebted to B. R. Czorny of RCA Electronic Components and Devices. The mass spectrometric analyses of the germane were carried out by I. Stacy, and the gas chromatograph was kindly made available by H. Hyman and P. A. Hoss, also of RCA Components and Devices. We would also like to thank A. F. Mayer and W. Kern for their many helpful comments and suggestions, and M. Coutts, G. W. Neighbor, and W. Roth for their aid in obtaining x-ray and electron-diffraction patterns.

EPITAXIAL DEPOSITION OF SILICON BY THERMAL DECOMPOSITION OF SILANE

By

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*Summary—Pyrolysis of silane diluted with hydrogen is shown to be a safe, simple, and convenient method for the epitaxial deposition of silicon. Large-area microwave diodes made by this process have excellent electrical properties. Almost abrupt high-low and p-n junctions can be grown at rates of 0.02 to 1 micron per minute at 1080 to 1130°C. Gas-phase doping with diborane, phosphine, and arsine permits close resistivity control in the range 0.001 to 30 ohm-centimeters.**

Introduction

THE EPITAXIAL DEPOSITION of single-crystal silicon layers on silicon substrates has become an established step in the routine production of various semiconductor devices. Common practice is to use a vapor-phase reaction, at 1150 to 1250°C, between silicon tetrachloride ($SiCl_4$) and hydrogen to form the elemental silicon which deposits on the substrate wafer; the other reaction products are mainly hydrogen chloride and lower silicon chlorides. Other silicon halides ($SiHCl_3$, $SiBr_4$, SiI_4, etc.) may be used in place of the tetrachloride. The process is well suited for the routine production of many types of transistors, diodes, and rectifiers.

However, at the relatively high concentration required for the deposition reaction, halide ions can transport and deposit unwanted impurities at the growing face. In some semiconductor devices, abrupt changes in dopant concentration and in the type of conductivity are desirable, and it was thought probable that such structures could be prepared more advantageously by the thermal decomposition of silane (SiH_4).

Silane can be obtained from the hydrolysis of calcium or magnesium silicide or from the reaction of silicon tetrachloride with

* The silane process was described brieby in a "Recent News Paper" entitled "Silane Epitaxial Silicon for Microwave Diodes," by M. A. Klein, H. Kressel, and A. Mayer at the Electrochemical Society Meeting, Pittsburgh, April 1963.

lithium aluminum hydride.[1,2] It is a colorless gas which ignites spontaneously when released into the atmosphere. (It has a boiling point of 112°C, a freezing point of —185°C, a critical temperature of —3.5°C, and a critical pressure of 47.8 atmospheres.) Mixtures of silane and air are explosive over a wide range of composition. When prepared by either of the methods mentioned above, the silane usually contains traces of other hydrides, such as arsine, borane, phosphine, and the like. It can be purified by chemical absorption, by condensation and distillation, by the use of suitable cold traps, or by the selective adsorption of impurities on active carbon or a molecular sieve;[3-5] borane impurities can also be removed catalytically by contact with platinum or Raney nickel.[6]

Silane has a positive free heat of formation, ΔHf_{298}, which is about +7.5 kilocalories per mole.[7-9] The pyrolytic reaction, $SiH_4 \rightarrow Si + 2H_2$, is appreciable at temperatures above 600°C and is probably accompanied by the formation of small amounts of polymers, such as disilane (Si_2H_6), trisilane (Si_3H_8), etc.[10] The standard free energy of decomposition for this reaction is —12 kilocalories per mole at 300°K and —40 kilocalories per mole at 1400°K.

The decomposition of pure silane at reduced pressure has been the basis for the production of bulk silicon for many years,[11] but because the process is hazardous and necessitates burdensome safety precau-

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[1] J. M. Wilson, "Large-Scale Preparation of Ultrapure Silicon," *Research*, Vol. 12, p. 91, March 1959.

[2] C. H. Lewis, H. C. Kelly, M. B. Giusto, and S. Johnson, "Preparation of High-Purity Silicon from Silane," *Jour. Electrochem. Soc.*, Vol. 108, p. 1114, Dec. 1961.

[3] H. C. Kelly, T. J. Flynn, C. W. Davis, and S. Johnson, AFCRC-TR-57-198; AD 133701, 1957; C. W. Lewis, M. B. Giusto, and S. Johnson, AFCRC-TR-58-354; AD 228538, 1959.

[4] E. G. Caswell and R. A. Lefever, U.S. Patent 2,971,607 (1961).

[5] R. G. Beckenridge, U.S. Signal Corps Contract DA 36-039-SC-90734, Quarterly Reports June 1962 onward.

[6] T. A. Jacob and N. R. Trenner, U.S. Patent 3,019,087 (1962).

[7] T. R. Hogness, T. L. Wilson, and W. C. Johnson, "Thermal Decomposition of Silane," *Jour. Amer. Chem. Soc.*, Vol. 58, p. 108, Jan. 1936.

[8] E. O. Brimm and H. M. Humphreys, "The Heat of Formation of Silane," *Jour. Phys. Chem.*, Vol. 61, p. 829, June 1957.

[9] S. R. Gunn and L. G. Green, "The Heats of Formation of Some Unstable Gaseous Hydrides," *Jour. Phys. Chem.*, Vol. 65, p. 779, May 1961.

[10] K. Stokland, "The Thermal Decomposition of Disilane and Trisilane," *Trans. Faraday Soc.*, Vol. 44, p. 545, Aug. 1948.

[11] H. F. Sterling and F. J. Raymond, Brit. Patent 745,383; U.S. Patent 3,044,967; see also 2,841,860; 2,871,533.

tions, most producers have turned to other methods. It has been found, however, that silane diluted with hydrogen or a rare gas to a concentration of less than 5% by volume is not pyrophoric and can be stored at a pressure of 1000 psi in a standard gas cylinder. It is now available commercially in this form. The silane epitaxial system described

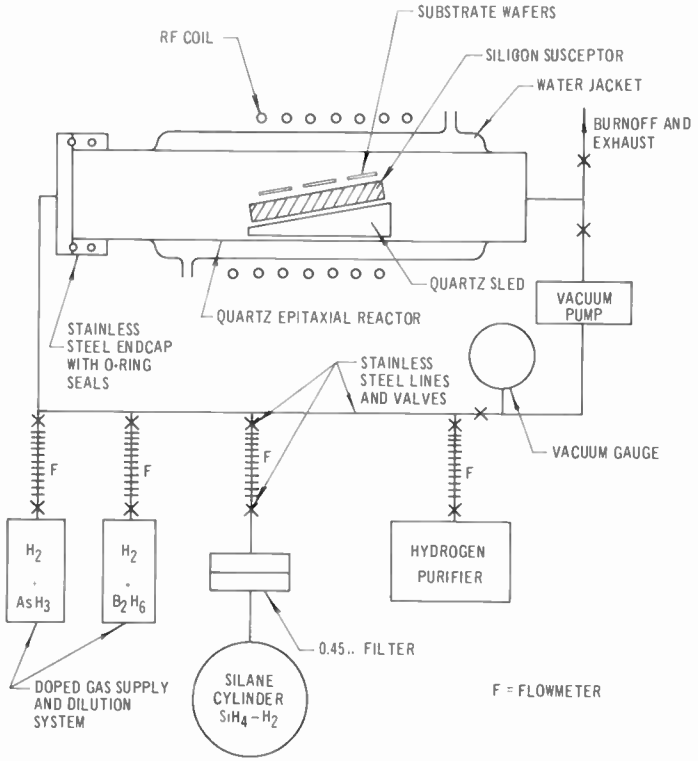

Fig. 1—Schematic diagram of silane epitaxial system.

in this paper has been operated daily for 18 months without accident, using the same safety precautions as those recommended for hydrogen.

Apparatus

The apparatus used to achieve the epitaxial deposition of silicon from the pyrolysis of silane is shown schematically in Figure 1. All lines and valves of this apparatus are made of stainless steel and are connected by Teflon compression and Viton "O" ring fittings. The

reactor tube is made of quartz. The water jacket is used to keep the temperature of the wall of the reactor tube low enough so that the pyrolysis of the silane is confined to the r-f heated silicon susceptor block upon which the substrate wafers are placed. The block is supported on a quartz sled in an inclined position which helps to assure over-all uniformity of the silicon deposition.

The system is checked for leaks with a helium mass spectrometer detector and, on a more routine basis, by evacuating the system with the rotary vacuum pump attached to it and observing the vacuum gauge after the pump has been isolated. It is important that oxygen, in particular, be eliminated from the system, because traces of oxygen interfere with the doping and react with silicon to form silicon monoxide particles which can become embedded in the deposit. Silicon monoxide deposits also form on the apparatus wall, obscuring vision and interfering with the optical pyrometer readings used for temperature control.

The hydrogen diluent for the silane and doping gases is used in relatively large volumes to ensure uniformity in the thickness and in the doping of the deposit. A palladium diffuser can be employed to obtain a reliable source of oxygen-free and dust-free hydrogen, although its use is not mandatory.

A submicron filter is used to remove any dust that comes from the compressed-gas cylinders that supply the diluted silane and dopants. Diborane and arsine or phosphine at concentrations of 200 to 500 parts per million in hydrogen are used as the dopants. The required dilution of the dopants with hydrogen is accomplished by expansion of a known quantity of the doping gases into evacuated stainless-steel tanks and addition of hydrogen until the pressure in the tanks rises to a predetermined level (3 to 6 atmospheres). The diluted dopant gases are then allowed to flow from their respective reservoirs through flowmeters to the main gas feed. This dilution system can provide a wide range of dopant concentrations and yet uses only one flowmeter for each dopant gas, so that automatic and programmed flow control becomes feasible.

Operation

The prepared silicon wafers are inserted into the reactor on a high-resistivity silicon block as shown in Figure 1. A small piece of low-resistivity silicon is placed in contact with the susceptor block to act as a starter for r-f coupling. The apparatus is evacuated to remove

air and the last traces of moisture, and hydrogen is admitted until atmospheric pressure is reached. The exit valve is then opened and the hydrogen flow is adjusted to 10 to 30 liters per minute. The susceptor is heated to 1200°C* for 10 to 15 minutes to remove the natural oxide film on the substrate wafer. The temperature is reduced to 1100°C and, when thermal equilibrium is reached, the silane flow (and dopant flow) is started. After the deposition process has proceeded for the time necessary to produce the desired thickness, the silane flow is stopped, and the wafers are cooled in hydrogen.

Surface Preparation

The final lapping of the substrate is done with an abrasive having a grit size less than 5 microns. After the lapping has been completed, 8 to 10 microns are etched from the silicon substrate with hydrogen chloride gas at 1200 to 1250°C. The combination of lapping and gas etching produces a mirror-like surface finish on which equally mirror-like, high-resistivity epitaxial deposits can be grown. By contrast, hydrogen heat treatment or silane epitaxial growth on chemically, electrolytically, or mechanically polished surfaces often results in the appearance of p-type regions with surface concentrations up to 10^{18} atoms per cm^3. Presumably, these regions are caused by particles of lapping compound being buried in the surface, either by the reduction of alumina or of impurities associated with it. Hydrogen chloride etching apparently proceeds faster than indiffusion of such impurities so that surfaces free from contaminants can be prepared. Gas etching is, therefore, the preferred method of surface preparation. This process is described in detail by Stavish and Lang.[12]

Results Obtained

Crystalline Quality

The deposition of the epitaxial silicon layers (5 to 30 microns) was made on (111) oriented single-crystal silicon substrates. X-ray diffraction patterns were sharp and showed Kikuchi lines; this indicated a high degree of crystal perfection. Substrate wafers had dislocation densities of less than 5×10^3 per cm^2. Epitaxial layers grown on substrates that had been properly cleaned and heat treated (to remove oxide) had dislocation densities of the same order and showed hardly

* All temperatures were measured with an optical pyrometer and were corrected for emissivity and absorption.

[12] T. Stavish and G. A. Lang, "Chemical Polishing of Silicon with Anhydrous HCl," *RCA Review*, Vol. 24, p. 488, Dec. 1963.

any stacking faults. However, when the heat treatment was omitted or when the pre-cleaning treatment was poor, pronounced stacking faults were observed as shown in Figure 2. These results confirm the observations of Finch et al.[13]

Fig. 2—Stacking faults in epitaxial layer on a silicon wafer not heat treated before deposition.

Deposition Rate, Temperature, and Uniformity

For a hydrogen–silane mixture in the deposition zone of 0.2 volume per cent, the rate of deposition was found to be 0.8 micron per minute at 1050 to 1070°C, and 1.12 microns per minute at 1100 to 1140°C. At lower temperatures, an increase in the number of imperfections was observed, and the epitaxial layers tended to become polycrystalline when they were deposited at temperatures below about 1000°C. Calculations showed that more than 60% of silicon introduced into the system as silane was deposited. A reduction in the silane content resulted in a corresponding reduction in the deposition rate. Thus, layers 1 micron thick having high crystalline perfection, good surface finishes, and excellent electrical properties can be grown in 10 minutes with the same accuracy (±10%) as much thicker layers.

Resistivity and Type

Undoped Layers—The pyrolysis of silane–hydrogen gas from cylinders has consistently produced n-type silicon layers having resistivities

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[13] R. H. Finch, H. J. Queisser, G. Thomas, and J. Washburn, "Structure and Origin of Stacking Faults in Epitaxial Silicon," *Jour. Appl. Phys.*, Vol. 34, p. 406, Feb. 1963.

of 25 to 35 ohm-centimeters. Cylinders of the gas have been stored for periods up to 4 months without any apparent change in carrier level or effective silicon concentration, but it was noticed that the resistivity tended to decrease to about 8 to 10 ohm-centimeters when the cylinder pressure dropped to between 200 and 300 psi. This decrease in resistivity is probably caused by an adsorption–desorption effect of an n-type dopant on the cylinder wall.

Doped Layers—Arsine or phosphine and diborane were used to deposit reproducibly n- and p-type layers in the range of 5×10^{14} to 5×10^{19} atoms per cm^3. To achieve the high doping levels, the phosphine concentration in the deposition zone was 1 part per million compared to 1700 parts per million of silane. The doping efficiency is, therefore, close to 100%. The doping efficiency for arsine at carrier concentration levels of 3×10^{14} to 10^{16} atoms per cm^3 was calculated to be about 25%; for diborane, it was 10% in relation to the silane input.

Evaluation—Evaluation of carrier concentration in the silicon layers was made by a four-point probe in conjunction with angle-lap and infrared-interference measurements of the layer thickness, and by the double-angle-lap-diffusion technique. The values agreed with those obtained by plotting capacitance–voltage curves on mesa diodes. Also, they were found to be in good agreement with data computed by a method suggested by M. Klein and H. Kressel[14] which involves measurement of the resistance of a diode at 2 gigacycles under reverse bias. Figure 3 shows a plot of this type for two diodes—one fabricated on material made by the silane process and the other on material made by a commercial silicon tetrachloride process.

High-Low Junction Profiles—When work on the deposition of silicon from silane was first begun, epitaxial deposits, obtained from the reduction of a silicon halide, of high-resistivity layers on highly doped substrates tended to show considerable intrusion of the dopant into the high-resistivity region. The two major reasons for this intrusion were: (1) transport of the dopant by the halide from the substrate to the colder growing face and (2) diffusion. As shown by Cave and Czorny,[15] considerable improvement in the halide process has been made since then, and for many devices the outdoping effect is negligibly small. However, one example of a device which benefits substantially

[14] M. A. Klein and H. Kressel, "Determination of Epitaxial Layer Impurity Profile by Means of Microwave Diode Measurements," *Solid State Electronics*, Vol. 6, p. 309, May-June, 1963.

[15] E. F. Cave and B. R. Czorny, "Epitaxial Deposition of Silicon and Germanium Layers by Chloride Reduction," *RCA Review*, Vol. 24, p. 523, Dec. 1963.

from an abrupt n^+-n transition is a microwave diode having a high reverse breakdown voltage (greater than 150 volts), as discussed by Klein and Kressel.[16]

Because of the low deposition temperature and the absence of transport agents in the silane process, epitaxial silicon deposits obtained by this method have almost abrupt high-low transition regions and are essentially uniformly doped, as illustrated in Figures 3 and 4. The

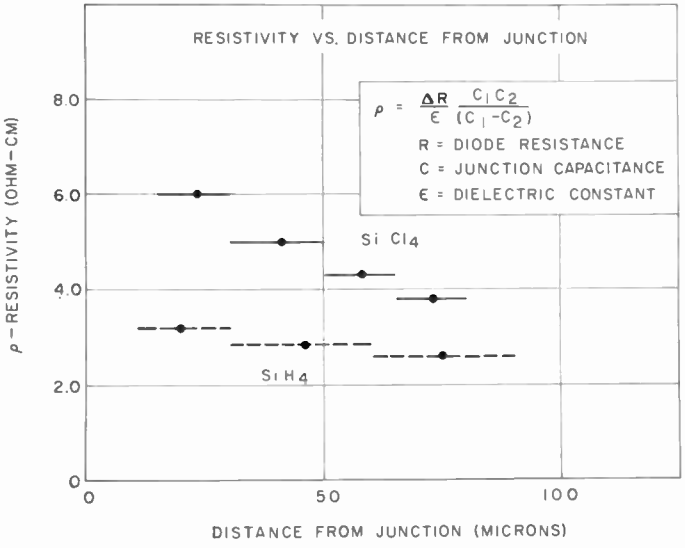

Fig. 3—Resistivity profile for diodes made by deposition from silane (SiH_4) and silicon tetrachloride ($SiCl_4$).

$SiCl_4$ curve in Figure 4 illustrates the distribution for silicon layers prepared by a halide reduction process in which no special precautions were taken to prevent dope transport. The points were obtained by evaluation of the capacitance–voltage curves of diodes from epitaxial layers grown successively under similar conditions in which only the deposition time, and hence the thickness of the deposit, was varied. The SiH_4 curve in Figure 4 shows the distribution for epitaxial layers deposited on arsenic-doped substrates by the silane process. It is evident that very little outdoping occurred in the silane process; this was attributed to the fact that no active chemical species were present.

Diffused mesa diodes made on highly doped substrates with a de-

[16] H. Kressel and M. A. Klein, "High-Power Epitaxial Silicon Varactor Diodes," *RCA Review*, Vol. 24, p. 616, Dec. 1963.

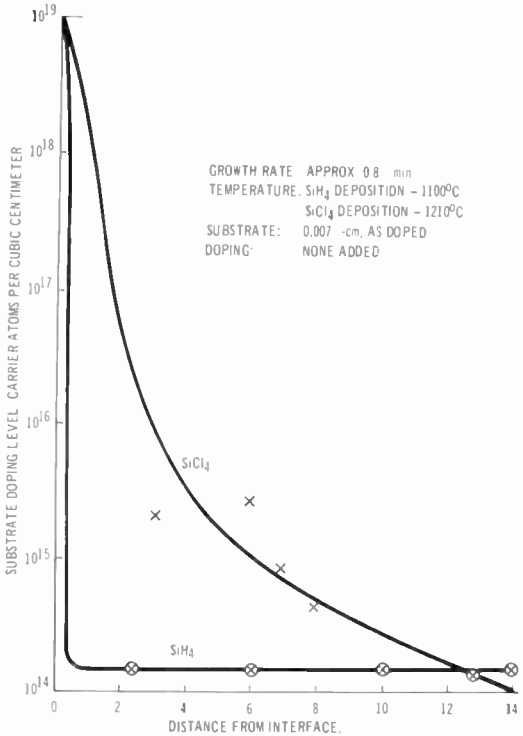

Fig. 4—Measured doping profiles for silane (SiH_4) versus silicon-tetrachloride ($SiCl_4$) systems.

posit of the same conductivity type have shown excellent electrical properties. The reverse breakdown voltages were usually close to those expected in theory (i.e., thickness-limited), and the reverse saturation currents were low, as shown in Table I.

Finally, large-area (1600 square mils per mesa) high-voltage diodes

Table I—Thickness-Limited Reverse Breakdown Voltage on Diodes made by Shallow Boron Diffusion into $n+-n$ (Epitaxial) Wafers

T (microns)	V_B (observed)	V_{max} (calculated)	N_D (atoms/cc)
6.6	120	132	2.5×10^{14}
10.9	210	218	2.8×10^{14}
21.5	400	430	2.8×10^{14}

T = thickness of n-type epitaxial layer.

were obtained in excellent yield over the whole epitaxial wafer area, as shown in Figure 5. This result implies that the epitaxial deposits are uniform with respect to both thickness and doping level, and that they are reasonably free from structural defects. Microwave diodes having electrical properties that are in close agreement with theoretical predictions are being fabricated from this material.[16]

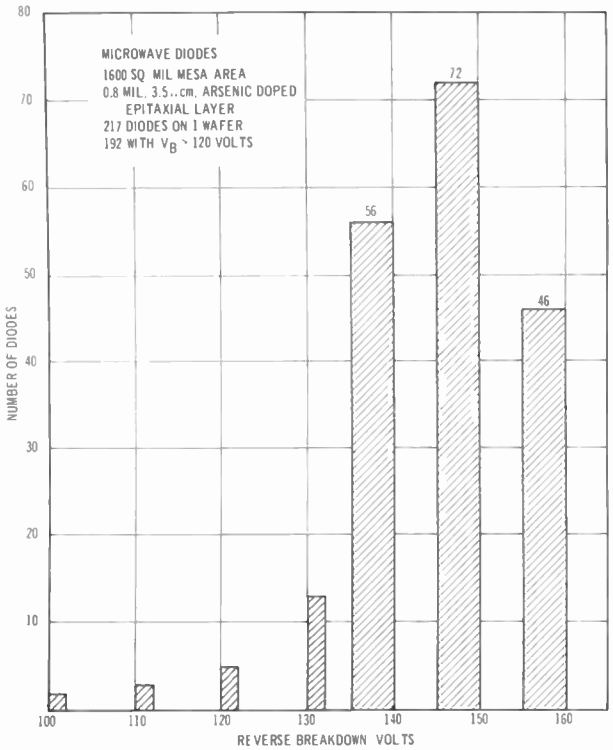

Fig. 5—Distribution of the reverse breakdown voltage in a group of microwave diodes prepared from a silane-grown epitaxial wafer.

P-N Junction Deposition

Diode junctions made by mesa etching of epitaxial deposits on opposite-type substrates were sharp, had high reverse breakdown voltages, and had low reverse saturation currents. Similar characteristics were obtained with p-n layers on n+ substrates. A change of the type of deposit was made simply by stopping the flow of silane and doping gas simultaneously, allowing hydrogen to sweep for 5 minutes, and then turning on the opposite type of doping gas together

with the silane. In this manner all-epitaxial transistor structures were grown with good control over layer thickness and resistivity. A typical program consisted of depositing the following layers on an n^+ substrate: a 15-micron, 20-ohm-centimeter n-type layer as the collector; a 5-micron, 0.8 ohm-centimeter p-type layer as the base; and a 2 micron, 0.002-ohm-centimeter n-type layer as the emitter.

Discussion

From the data presented it is clear that the objective of the investigation was achieved; the silane process can be used to obtain epitaxial growth of all types of doping profiles, from abrupt to linear or exponentially graded p-n or high-low junctions. When no chemically active species such as chloride ions are present, evaporation and thermal diffusion are the only mechanisms for dope transfer. S. E. Mayer and D. E. Shea[17] observed some dope intrusion in their work on silane epitaxial deposition at 1200°C which they indicated could not be accounted for by evaporation from the front surface. They also found that the effect can be reduced markedly by masking the back side of a highly doped substrate.

In the work described in this paper, the effect was observed only with substrates that were highly doped with phosphorus, and was attributed to the relatively high vapor pressure of phosphorus over silicon. Very little cross doping was observed with arsenic- or antimony-doped substrates. It is also possible that a trace of oxygen (or water vapor) could act as a transport agent, but the residual oxygen level in the system described here may have been too low to initiate dope transfer.

Because no corrosive ion species are present in a silane system, such a system can be constructed readily using stainless steel in such a way that it is vacuum tight. The use of a palladium diffuser as a source for pure hydrogen then ensures that the residual oxygen content is very low.

Although the growth through oxide-mask patterns was not investigated extensively, the lower deposition temperature of the silane process compared to that required for the halide process is advantageous.

Finally, it should be pointed out that surface contamination of substrates exerts a pronounced effect on the resistivity of silane-grown layers. Only the hydrogen chloride gas-etching process was found to

[17] S. E. Mayer and D. E. Shea, "Recent News Paper," "Epitaxial Deposition of Silicon Layers by Pyrolysis of Silane," Electrochem. Society Meeting, Pittsburgh, April 1963.

be consistently capable of removing contaminants to a level less than about 10^{14} atoms per cm^3.

On the basis of the high degree of uniformity in the electrical parameters of devices made from silane-grown high-resistivity epitaxial layers, it can be concluded that the essential variables of the process are now understood and can be controlled with a high degree of precision.

ACKNOWLEDGMENT

The contributions made by D. Kenney to the deposition of highly doped layers in transistor structures is gratefully acknowledged.

EPITAXIAL DEPOSITION OF SILICON AND GERMANIUM LAYERS BY CHLORIDE REDUCTION

By

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Summary—The status of the technology of the formation of epitaxial silicon and germanium films by reduction of chlorides is described, especially as this technology applies to the preparation of semiconductor devices. The processes and the systems used for the growth of epitaxial layers are considered in detail. The characteristics of these epitaxial layers and methods of evaluating them are discussed. Present and potential applications of structures prepared by epitaxial techniques are given as illustrations of the versatility of the method.

Introduction

THE EPITAXIAL DEPOSITION of thin, single-crystal films of semiconductor materials has recently achieved commercial significance in the manufacture of transistors and diodes. A broad and diverse technology has been developed among the various manufacturers and suppliers of semiconductor devices and materials. The epitaxial-growth process in most widespread use within the industry is the chemical reduction of the tetrachlorides of silicon and germanium by hydrogen at elevated temperatures.[1,2] The popularity of the chloride-reduction process results from its simplicity and from the availability of adequate raw materials. Epitaxial growth of germanium and silicon has also been achieved by many other techniques. These include deposition from their respective hydrides,[3,4] chlorohydrides, or other halides; the use of disproportionation or transport

[1] N. N. Sheftal, N. P. Kokorish, and A. V. Krasilov, "Growth of Single Crystal Layers of Silicon and Germanium from the Vapor Phase," *Izvest. Akad. Nauk. SSSR Ser. Fiz.*, Vol. 21, p. 140, 1957.

[2] H. C. Theurer, "Epitaxial Silicon Films by the Hydrogen Reduction of $SiCl_4$," *Jour. Electrochem. Soc.*, Vol. 180, No. 7, p. 648, July 1961.

[3] J. A. Amick, "The Growth of Single-Crystal Gallium Arsenide Layers on Germanium and Metallic Substrates," *RCA Review*, Vol. 24, No. 4, p. 555, Dec. 1963.

[4] A. F. Mayer and R. Bhola, "Epitaxial Deposition of Silicon by Thermal Decomposition of Silane," *RCA Review*, Vol. 24, No. 4, p. 701, Dec. 1963.

reactions;[5,6] regrowth from solutions;[7] and vacuum evaporations.[8] This article describes the technology of the chloride-reduction process, discusses the new developments currently being investigated, and concludes with an account of the present and the potential applications for epitaxial techniques in the semiconductor industry.

Description of the System

The over-all formation of silicon and germanium layers from the reduction of their tetrachlorides is achieved by the following vapor-phase reactions:

$$SiCl_4 + 2H_2 \rightleftharpoons 4HCl + Si_{(s)}$$

$$GeCl_4 + 2H_2 \rightleftharpoons 4HCl + Ge_{(s)}$$

These reactions are thermodynamically reversible and their equilibriums have been studied by Schafer *et al.*[9-11] At elevated temperatures, the presence of several other species, such as the dichlorides, trichlorosilanes, and various chloropolymers, have also been reported.[9-14] All these species are gaseous at the deposition temperatures, and only elemental silicon or germanium will deposit on the hot surfaces. Under

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[5] *IBM Jour. Research and Development*, Vol. 4, No. 3, p. 248 *et seq.*, July 1960.

[6] R. C. Newman and J. Wakefield, "The Formation of Thin Films of Germanium by the Disproportionation of Germanium Di-Iodide," Brussels Int. Conf. of Semiconductors, June 1958.

[7] H. Nelson, "Epitaxial Growth from the Liquid State and Its Application to the Fabrication of Tunnel and Laser Diodes," *RCA Review*, Vol. 24, No. 4, p. 603, Dec. 1963.

[8] E. T. Handelman and E. I. Povilonis, "Epitaxial Growth of Silicon by Vacuum Sublimations," Boston Meeting Electrochem. Soc., Sept. 16, 1962.

[9] H. Schafer and J. Nickl, "The Equilibrium: $Si + SiCl_4 \rightleftharpoons 2SiCl_2$ and the Thermochemical Properties of $SiCl_2$ Gas," *Z. anorg. u. allgem. Chem.*, Vol. 274, p. 250, 1953.

[10] H. Schafer, "Formation of Silicon Chlorides of Higher Molecular Weight in the Hot-Cold Tube," *Z. anorg. u. allgem. Chem.*, Vol. 274, p. 265, 1953.

[11] H. Schafer, H. Jacob and K. Etzel, "I. The Transport of Solids in a Temperature Gradient with the Help of Heterogeneous Equilibriums," *Z. Anorg. u. allgem. Chem.*, Vol. 286, p. 27, 1956.

[12] *Gmelins Handbuch d. anorg. Chemie.*, Vol. 15, B, Silicon, Verlag Chemie, GMBH., Weinheim/Bergstrasse, 1959.

[13] *Gmelins Handbuch d. anorg. Chemie*, Vol. 45, Germanium, Verlag Chemie, GMBH., Weinheim/Bergstrasse, 1958.

[14] O. H. Johnson, "Germanium and Its Inorganic Compounds," *Chem. Rev.*, Vol. 51, p. 421, 1952.

normal conditions of deposition, no gas-phase reaction occurs for either silicon or germanium, because the reaction is surface catalyzed.

A typical epitaxial deposition system is shown in Figure 1. The systems are basically simple and are designed to prevent leaks, to permit trouble-free operation, and to provide for ease of maintenance. The quartz reactor tube contains a susceptor which supports the substrate wafers and is heated by inductive coupling with an external r-f

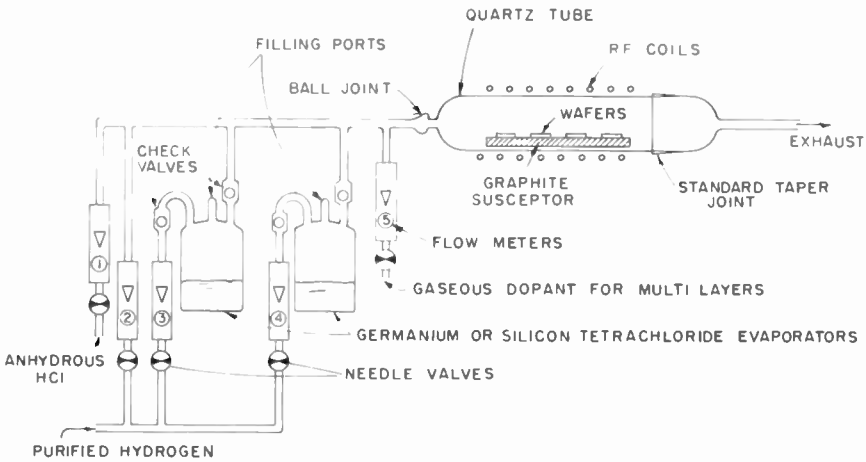

Fig. 1—A typical epitaxial deposition system.

field. Hydrogen (2), which has been purified by catalysis over palladium and passage through a molecular-sieve adsorbant, passes over the wafer during the entire deposition cycle. A stream of pure hydrogen chloride gas (1) is used for the preparatory etching of the substrates at high temperatures prior to the deposition of the epitaxial layers.[15,16] Hydrogen streams, either (3) or (4), deliver the silicon or germanium tetrachloride. These compounds are commercially available in adequate purity.

The tetrachlorides are liquid at room temperature and have sufficient vapor pressure to permit the rate of delivery of the halide to the reactor to be controlled by regulation of the flow of hydrogen over the liquid. In this manner, a more precise control of the delivery of the

[15] T. Stavish and G. A. Lang, "Chemical Polishing of Silicon with Anhydrous HCl," *RCA Review*, Vol. 24, No. 4, p. 685, Dec. 1963.

[16] J. A. Amick, "The Growth of Single-Crystal Gallium Arsenide Layers on Germanium and Metallic Substrates," *RCA Review*, Vol. 24, No. 4, p. 555, Dec. 1963.

halide has been achieved than is possible when the delivery is accomplished by bubbling through the liquid, and the evaporation rate is less sensitive to the source temperature. Doping is achieved either by the addition of a volatile impurity to the tetrachloride or by the introduction of a gaseous impurity by means of a separate stream (5). All stream flows are controlled by needle valves and monitored by gas flowmeters. These features permit the interruption of any flow at any time, as might be required for multi-layer growth, and allow the blending and programming of streams as required for multiple doping of single layers and controlled-layer impurity distributions. Because the system is operated by various independent gas streams, it can be easily adapted for automatic programmed control.

Processing Techniques

Substrate

The subsequent discussion refers to epitaxial growth on substrates whose surfaces are within 3 degrees of the (111) plane. The silicon substrates are prepared by the Czochralski technique, and the germanium substrates by zone-leveling. A clean, damage-free substrate wafer is essential to good single-crystal epitaxial growth because even atomically small imperfections or impurities will be propagated into the epitaxial layer. Several techniques are used for substrate preparation, and the choice depends to some degree on the ultimate application of the wafer. For small geometries where photolithographic definition is a problem, a fine mechanical polish followed by cleaning with a very light chemical etch is essential.

In p-type germanium, adequate surfaces are obtained by electrochemical polishing;[17] where surface planarity is not important, wet-chemical etching of lapped wafers will provide adequate surfaces. Anhydrous hydrogen chloride etching of fine-grit lapped wafers produces surfaces approaching a mechanical polish[15,16] and is an inexpensive method of substrate preparation. Any of the gas- or solution-etching techniques must produce surfaces free of irregularities, because any deformations in the substrate surface will be reproduced by the epitaxial deposit.

Anhydrous hydrogen chloride etching of the substrate wafers in their normal position inside the quartz reactor, just prior to deposition, is very effective for removing surface impurities and mechanical work damage. This etching also improves layer perfection, atomically,

[17] M. Sullivan, K. L. Klein, R. M. Finne, L. A. Pampliano, and G. A. Kolb, "An Electropolishing Technique for Germanium and Silicon," *Jour. Electrochem. Soc.*, Vol. 110, No. 5, p. 412, May 1963.

by reducing stacking fault density in the epitaxial layer and, macroscopically, by reducing the subsequent formation of bumps and other types of surface defects to a minimum. This technique is applicable to both silicon and germanium wafers and provides typical etching rates of 0.5 to 2.0 microns per minute for hydrogen chloride concentrations in hydrogen of 1 to 5 per cent. For more rapid etching, temperatures higher than the normal deposition temperatures are required to retain a smooth surface. For rapid etching, it is also essential that the hydrogen chloride be low in both hydrocarbon and moisture content.[15,16] The etching is controllable even at very low rates; the use of this technique in conjunction with silicon-dioxide masking is discussed later in this article.

Susceptors

The susceptor, which supports the substrate wafers and supplies the heat required for the deposition reaction, is an important factor in the epitaxial process. The deposition temperatures for germanium are low, and susceptors made of high-purity graphite are adequate. However, the deposition temperatures for silicon are substantially higher, and volatile impurities in the porous graphites will frequently contaminate the deposits. When the silicon wafer is heated in contact with graphite, an undesirable silicon carbide deposit forms on the back side of the wafer; therefore, in the silicon deposition system, the graphite susceptor is normally coated with silicon carbide or silicon.

Quartz-enclosed susceptors have been used; however, if the deposition takes place on highly doped substrates, the down-stream doping is increased. This increase in down-stream doping is caused by the reaction of the quartz with the silicon to form a volatile monoxide[9-11] ($SiO_2 + Si \rightarrow 2SiO\uparrow$) which liberates the substrate dopant into the flowing gas stream. This type of impurity liberation, probably caused by a chloride transport mechanism, also occurs with the other coatings but to a lesser degree. In the case of silicon-coated susceptors, a sealing of the back side of the substrate occurs because of thermal transport of silicon from the block to the under side of the wafer. The transport reaction, which is controlled by the temperature difference existing between the hot susceptor and the cooler wafer, is given by[9-11]

$$Si + SiCl_4 \rightleftharpoons 2SiCl_2.$$

The equilibrium is driven to the right with an increase in temperature. The $SiCl_4$ in this reaction can be obtained by the attack of HCl on elemental silicon, and thus the HCl can serve as a transport medium.

Heavily doped substrates are required for low-resistance-contact applications, and substrate dopants are selected on the basis of low diffusion coefficients and a lack of any tendency to escape into the deposition stream. These characteristics are necessary to prevent autodoping of the deposits.[18,19] In the case of n-type impurities in silicon, the autodoping has been observed to increase with the volatility of the impurity element in the sequence phosphorus, arsenic, antimony. High-resistivity n-type deposits require 0.01 to 0.02 ohm-centimeter antimony-doped substrates to minimize this autodoping.

In p- and n-type germanium, autodoping is usually not troublesome and substrate resistivities as low as 0.001 ohm-centimeter are typical. A further discussion of autodoping and layer homogeneity is given in the section on layer evaluation.

Deposition Conditions

Table I lists conditions under which the epitaxial layers are grown. The temperature ranges shown have resulted in specular reflecting layers of good crystallinity, as determined by crystal diffraction and dislocation etching techniques. The lowest practical deposition temperature is determined by reasonable growth rates and by the mobility of the atoms on the growing surface. Because of the stability of silicon dioxide (SiO_2) at the deposition temperatures, the hydrogen used in the epitaxial growth of silicon must be low in oxygen and moisture content to obtain good single-crystal growth. The initial thin oxide present on the surface of silicon can be removed by treatment in hydrogen at 1300°C to promote the reaction $SiO_2 + Si \rightarrow 2SiO\uparrow$. The silicon monoxide (SiO) is volatile and evaporates into the gas stream. Specular deposits of germanium have been obtained at 600°C at mole ratios of 10,000 molecules of hydrogen to 1 molecule of germanium tetrachloride. Because surface contaminants reduce mobility, production systems are, in practice, operated at the higher temperature to reduce the influence of potential contaminants and system leaks on the crystallinity of the layer.

A decrease in film thickness along the length (away from the entrance) of the reactor is prevented by reducing the halide depletion. This reduction in halide depletion is accomplished by use of a rapid

[18] H. Basseches, S. K. Tung, R. C. Manz and C. O. Thomas, "Factors Affecting the Resistivity of Epitaxial Silicon Layers," *Proc. Conference on Metallurgy of Semiconductor Materials*, Los Angeles, Sept. 1961, Ed. J. B. Schroeder, Interscience Publishers, New York, N. Y., 1962.

[19] D. Kahng, C. O. Thomas and R. C. Manz, "Epitaxial Silicon Junctions," *Jour. Electrochem. Soc.*, Vol. 110, No. 5, p. 394, May 1963.

hydrogen flow and low reaction efficiencies (typically 5 per cent). At high temperatures, the effect of temperature on growth rate is slight in high-flow systems.

Table I—Comparison of Processes for Producing Silicon and Germanium Epitaxial Deposits by Halide Reduction

	$SiCl_4$		$GeCl_4$	
	Range	Typical	Range	Typical
Deposition Temperatures °C	1120-1350	1200	600-920	875
Growth Rates μ/min	0.1-3	0.7	0.1-8	0.5
Mole Ratios H_2/Halide	50-500	200	50-10,000	200
Hydrogen Flow Velocities cm/min	1000-3000	2000	1000-3000	2000
Present Capacities Per Run	1-12	10	1-12	10
Susceptors	Silicon Silicon-Coated Graphite Silicon-Carbide-Coated Graphite Quartz-Covered Graphite		Graphite	
Thickness Capabilities μ	0.1 to 50		0.2 to 25	
Impurities in Substrate for Low Resistance Contact	N+Sb, As P+ B		N+ P P+ Ga	
Control Capabilities in Production	Resistivity ±20% Thickness ±10%			

Doping

The doping impurity is incorporated into an epitaxial layer by introduction of an appropriate Group III or V impurity into the gas stream. Two doping techniques have proven most successful in providing the desired degree of reproducibility and stability. In the first technique, called solution doping, a volatile impurity is added to the

liquid chloride source. This impurity evaporates with the source and provides doping of the layer. Impurity chlorides such as PCl_5 and $SbCl_5$ are preferable because there is no exchange reaction between them and the solvent which could lead to changes in partial pressure of the impurity over the source and, thereby, cause erratic doping.

Table II—Techniques of Doping Epitaxial Deposits

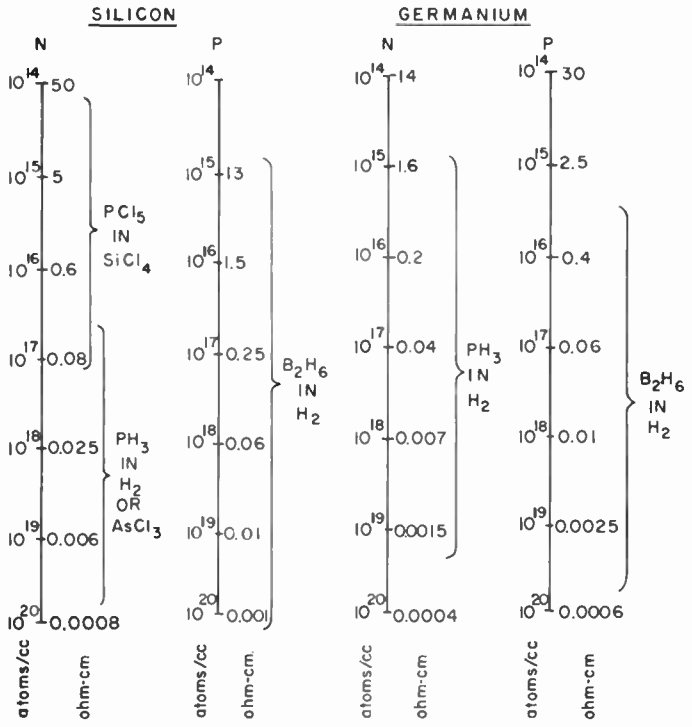

Table II shows the types and the concentrations of the dopants when solution doping is used. This technique is not suitable for p-type doping because most of the compounds that are available as impurity sources are extremely sensitive to traces of moisture which cause degradation of the dopant.

The most successful application of solution doping with PCl_5 and $SbCl_5$ is in n-type silicon to obtain resistivities greater than 0.1 ohm-centimeter. Figure 2 shows the variation in deposit resistivity as a function of deposition temperature for both of these impurities when all other deposition conditions are held constant. Each point is the

average of several runs made at the particular temperature. The variation of resistivity with temperature is larger for antimony. Because this effect is in the reverse order to the volatility of phosphorus and antimony, it is believed to be the result of the greater chemical affinity of phosphorus for silicon. A similar effect has been observed in the

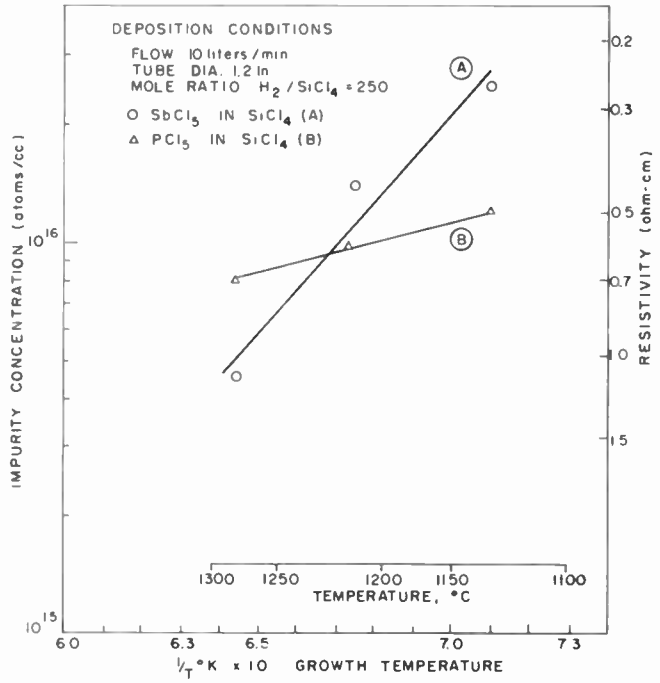

Fig. 2—Variation of the impurity concentration in n-on-n+ silicon layers as a function of the growth temperature.

evaporation rate of these impurities from the melt.[20] It has also been observed that the impurity concentration of phosphorus and antimony in the deposit is proportional to their impurity concentration in the gas stream as calculated from Raoult's law and, for a fixed temperature, is independent of the $SiCl_4$ concentration and growth rate. This observation indicates that a dynamic equilibrium exists between the impurity in the solid and in the gas phase. For antimony and phosphorus, the activation energies for this equilibrium are —5.3 kilocalories per gram mole and —1.2 kilocalories per gram mole, respec-

[20] S. E. Bradshaw and A. I. Mlavsky, "The Evaporation of Impurities from Silicon," *Jour. of Electronics*, Vol. 2, p. 134, Sept. 1956.

tively. If it is assumed that Raoult's law and ideal-solution behavior apply, the concentration of antimony in the gas stream must be approximately 2500 times that of phosphorus to produce the same level of doping. This requirement for high concentrations to produce doping can account for the reduction of down-stream doping by dopant impurities present in the substrate when antimony-doped substrates are used.

The extreme stability of very dilute dopant solutions is another reason that solution doping is preferred when high resistivities are desired. This stability is also very advantageous in production systems where a given level of doping is desired. Reservoirs containing the impurities are large, so that refilling is not frequent and the increase in the concentration of the dopant because of solvent evaporation is small. A typical system will have two or more sources of doped chlorides, and the blending of different proportions of impurity from each evaporation permits versatility in the levels of doping available from a system.

In the second doping technique, the dopants are introduced by means of an independent gas stream. This technique is called gas doping. Diborane (B_2H_6) and phosphine (PH_3) diluted in hydrogen in the 100 to 1000-ppm range are available commercially and are being used particularly for p-type doping and for more heavily doped n-type layers in both germanium and silicon. Both of these compounds are reasonably stable at these dilutions and permit considerable doping-level versatility. At light doping levels, fine needle valves and other techniques for the control of small gas flow are essential. If high doping levels and low diffusion rates are required, the use of an evaporator containing pure $AsCl_3$ is desirable. Ranges of impurity concentrations that are feasible at present are shown in Table II. The maximum impurity concentrations that have been achieved are somewhat less than the maximum solubility values reported in the literature.[21] Crystal structure and surface perfection are not affected by these doping levels.

Operation of the system to produce light doping, or high resistivities, is determined to a large extent by system contaminations. As discussed previously, contamination introduced from the susceptor is of serious concern in silicon. Contaminants on the substrates (such as polishing and etch residue), on and within the susceptors, and on the quartz tubes are, at present, limitations to high resistivities in silicon. Clean systems produce layers of 50 ohm-centimeters or better.

In germanium, thermal conversion caused by a p-type contami-

[21] F. A. Trumbore, "Solid Solubilities of Impurity Elements in Germanium and Silicon," *Bell Syst. Tech. Jour.*, Vol. 39, p. 205, Jan. 1960.

nant,[22] probably copper or nickel, prevents resistivities of more than about 10 ohm-centimeters from being obtained. Thermal conversion of germanium is extremely difficult to avoid at high temperatures.

Evaluation and Layer Characteristics

Resistivity

Resistivity is a measurement of impurity concentration in the deposited layer. When low-resistivity substrates are used, standard techniques cannot be employed to measure the resistivity directly on the epitaxial wafer because of shorting effects, and generally the measurement is made indirectly on "control" chips. Consequently, when a single layer is to be grown, chips of high resistivity and opposite conductivity to that of the layer are included in various places on the susceptor block. For example, in the growing of n-type layers, 50-ohm-centimeter p-type control chips are included in the reactor with the substrates. The sheet resistance can, therefore, be determined from a four-point probe measurement of the n-type deposition,[23] which is isolated from the p-type control chip by the p-n junction formed by the growth. The thickness of the grown region can be determined by angle lapping and staining of the control chip. Since the layer is homogeneous, simple multiplication of sheet resistance and thickness gives the layer resistivity.

When heavily doped layers are grown at high temperature, corrections must be applied to the thickness determined from angle lapping because of the diffusion of impurities from the epitaxial layer into the control chip. If this precaution is observed, the resistivities obtained by the control-chip technique are in close agreement with the resistivities determined by other techniques on the wafer itself.

The measurement of junction capacitance as a function of reverse-bias voltage is a very useful technique in comparing layer-resistivity values obtained from direct measurements on the wafer with values estimated from measurements on a control chip. In this technique, a shallow p-n junction is formed, by diffusion or alloying, on a portion of the deposited wafer, and measurements of junction capacitance as a function of reverse bias are made to determine resistivity at various depths in the epitaxial deposit. The curves shown in Figure 3 were obtained in this way from measurement of layers in which high-

[22] W. Albers, "Thermal Conversion of Germanium," *Jour. Elec. and Control*, Vol. 10, No. 3, p. 197, March 1961.

[23] F. M. Smits, "Measurement of Sheet Resistivities with the Four-Point Probe," *Bell Syst. Tech. Jour.*, Vol. 37, p. 711, May 1958.

surface-concentration shallow boron diffusions onto n-on-n+ silicon were used to create near-abrupt one-sided junctions. Mesa diodes were etched to form a junction area of 2.5×10^{-3} cm^2. Because the junction is one sided, a capacitance–voltage curve on logarithmic coordinates is a straight line having a slope of —1/2; this type of curve indicates a

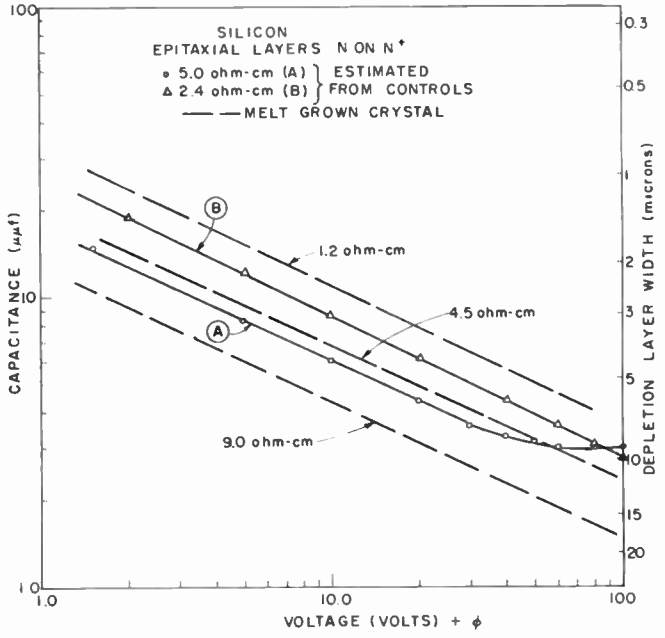

Fig. 3—Curves of junction capacitance as a function of reverse-bias voltage used to prove validity of control-chip resistivity measurements by a comparison of the capacitance–voltage relationships of layers of known resistivities with those for which the resistivities were estimated by the control-chip technique. (Diode area is 2.5×10^{-3} cm^2.)

square-root relationship. Melt-grown homogeneous wafers of known resistivity were diffused simultaneously with epitaxial wafers (A) and (B) to reduce errors caused by variations in capacitance that may occur because of deviations in the diffused junction. The resistivity of wafer (A) is estimated at 5.0 ohm-cm from the control chip; this value provides a good capacitance comparison with the 4.5- and 9.0-ohm-cm melt-grown wafers. Wafer (B), estimated to be 2.4 ohm-cm, compares favorably with the 1.2- and 4.5-ohm-cm melt-grown wafers. This type of comparison, for many depositions, along with the correlation of device electrical parameters, has proven the validity of the control-chip technique for measuring epitaxial resistivity.

The capacitance measurement also reveals other information about the epitaxial layer. The curve for wafer B in Figure 3 shows that the square-root relationship is maintained to a depth of 10 microns; this result indicates that the layer is uniform in resistivity to that depth. The curve for wafer (A) shows a square-root relationship to a depth of 8 microns, at which point curvature occurs. The capacitance becomes constant at a depth of approximately 9 microns indicating that the diode depletion edge has reached the n+ substrate. An impurity gradient exists in the 1-micron region above this n+ region. This impurity gradient can be calculated quantitatively from differential capacitance–voltage measurements.[24-26] It should be noted that although wafer (A) has a higher resistivity than wafer (B), it will break down under reverse bias at a lower voltage than wafer (B), as the electric field that produces the avalanche of the junction builds up faster once the depletion-layer width stops spreading because of punch-through to the n+ substrate.

A further illustration of the use of diode capacitance to determine the impurity distribution in epitaxial layers is given in Figure 4. The curve for wafer (C) shows a square-root relationship to a depth of 4.4 microns at which point breakdown occurs, indicating a uniform impurity density to that point. The curve for wafer (D) shows a change in square-root slope at 3.3 microns and the capacitance becomes constant at 5.0 microns. These results indicate that an impurity gradient exists in wafer (D) in a region 1.7 microns above the substrate. The curve for wafer (E) does not have a square-root slope and indicates that a gradient exists through the entire deposit. Such a gradient could occur on an 0.008-ohm-cm, or lower, arsenic-doped substrate on silicon carbide or quartz-coated susceptor. Wafer (F) is an example of a deposit made on a silicon-coated susceptor which permits sealing by the transport of silicon to the under side and edges of substrate wafer. The capacitance–voltage relationship is square root to 17.4 microns and becomes constant at 19.4 microns. The layer is therefore uniform to a depth of 17.4 microns. A gradient which could exist in the region 2 microns above the n+ substrate, although no experimental points are available to confirm this, could be accounted for by out-diffusion of impurity in the substrate into the epitaxial layer.

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[24] J. Hilibrand and J. D. Gold, "Determination of the Impurity Distributions in Junction Diodes from Capacitance–Voltage Measurements," *RCA Review*, Vol. 21, No. 2, p. 245, June 1960.

[25] H. Lawrence and R. M. Warner, Jr., "Diffused Junction Depletion Calculations," *Bell Syst. Tech. Jour.*, Vol. 39, p. 389, March 1960.

[26] C. O. Thomas, D. Kahng, and R. O. Manz, "Impurity Distribution in Epitaxial Silicon Films," *Jour. Electrochem. Soc.*, Vol. 109, p. 1055, Nov. 1962.

It should be noted that when punch-through occurs, as in (A) of Figure 3 and (D) and (F) of Figure 4, capacitance measurements permit the thickness of the electrically useful epitaxial layer to be measured independently. Because of the close relation between capacitance–voltage data and device characteristics, this is a very useful measurement.

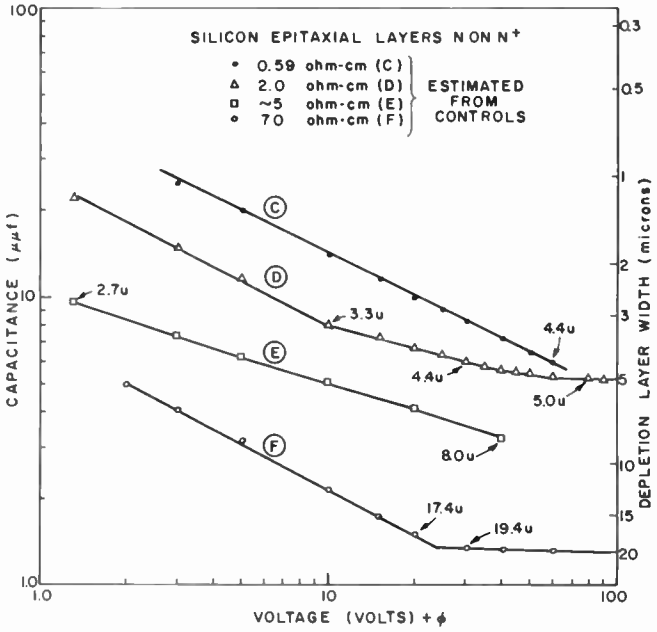

Fig. 4—Capacitance–voltage curves used to analyze the variation in impurity distribution with depth into the epitaxial layer. (Diode area is 2.5×10^{-3} cm^2.)

Another technique which has found general use in the measurement of layer resistivity is point-contact-diode breakdown. The three-point probe[27] is a refinement of this technique in that it is potentiometric. The method consists of empirically calibrating the reverse point-contact-diode breakdown on melt-grown material of known resistivity. Measurement of reverse breakdowns on epitaxial layers can, therefore, be related to layer resistivity by means of a calibration curve. This method is semiquantitative, in that it is somewhat affected by the

[27] P. A. Schumann, Jr. and J. F. Hollenback, Jr., "A Novel Four-Point Probe for Epitaxial and Bulk Semiconductor Resistivity Measurements," *Jour. Electrochem. Soc.*, Vol. 110, No. 6, p. 538, June 1963.

pressure and the area of the contact, but has the advantage of being nondestructive and rapid.

All the techniques described above can be applied to multiple layers. Runs can be interrupted and control chips removed or inserted into the reactor prior to the start of growth of new layers. Mesas etched an appropriate depth into multiple layers permit capacitance measurements in different regions. Small-angle beveling of multiple layers also permits point-contact probing.

Thickness Measurements

The thickness of epitaxial layers grown by the hydrogen reduction of silicon or germanium tetrachloride can be measured in two ways. One technique involves mounting a chip of the wafer on a suitable jig, lapping the chip at a small angle (1 to 5 degrees), staining the junction, usually under bright illumination, and measuring the thickness with a calibrated microscope. A typical stain used is a 10-per cent hydrogen-fluoride water solution saturated with cupric sulphate. The differences in chemical potential in layers of different conductivity and type cause selective electroplating of the copper,[28] and layers as thin as 2000 angstroms can be measured. This or other types of staining techniques are the only means available for the measurement of multiple layers. Because it is possible to delineate high-low junctions as well as p-n junctions, the method is nearly universal.

The thickness of the layers can also be measured by infrared interference.[29,30] In this method, which is applicable to layers as thin as 2 microns, a variable-frequency sweep is required to produce an interference curve by interactions of infrared reflections from the substrate and from the top of the film. This technique is effective only if the difference in carrier concentration across the interface is sufficiently great so that enough reflection occurs at the interface to produce a readable pattern; usually, one to two orders of magnitude difference in concentration is satisfactory. For practical purposes, 0.01 to 0.02 ohm-cm is the upper limit of resistivity, because sufficient reflection will not be obtained from more-lightly doped substrates. Poor inter-

[28] D. R. Turner, "Junction Delineation on Silicon in Electrochemical Displacement Plating Solutions," *Jour. Electrochem. Soc.*, Vol. 106, p. 701, Aug. 1959.

[29] W. G. Spitzer and M. Tannenbaum, "Interference Method for Measuring the Thickness of Epitaxially Grown Films," *Jour. Appl. Phys.*, Vol. 32, p. 744, April 1961.

[30] M. P. Albert and J. F. Combs, "Thickness Measurement of Epitaxial Films by the Infrared Interference Method," *Jour. Electrochem. Soc.*, Vol. 109, p. 709, Aug. 1962.

ference curves also result if out-diffusion from the interface occurs because the wafer is subjected to prolonged high temperatures or if the growth rate is too slow. The best infrared contrast of a high-resistivity layer on a low-resistivity substrate is achieved by the lowest growth temperature, together with the fastest growth rate. The infrared contrast on graded layers is improved if longer incident wavelengths, in the 10- to 35-micron range, are used. However, staining and infrared reflections will not always discriminate the same interface, and values obtained by one method may differ slightly from those obtained by the other. Beam condensation permits scanning of individual wafers to determine uniformity, and the infrared method, which is nondestructive, has been very useful in the control of the factory products used in transistor fabrication.

When either the staining or the infrared-interference method is used, the thickness of layers can be measured and controlled to within ± 10 per cent on a routine basis.

Crystalline Perfection

As described previously, the perfection of layers grown by the hydrogen reduction of silicon or germanium tetrachloride depends on the growth rate, the growth temperature, and the quality of the original surface. In general, two types of faults are found in epitaxial layers[31,32]—those which are atomic in nature (stacking faults and edge dislocations) and those which are macroscopic in nature (polycrystalline nodules, scratches, holes, cleaning stains, etc.). Almost all these imperfections originate at the interface between the epitaxial layer and the substrate. In good deposits, the number of dislocations in the layer is primarily determined by the dislocations inherent in the substrate rather than by ones introduced during the growth process. The number of stacking faults is controlled by general surface contamination at the start of the growth. It has been found that with silicon, surface oxidation contributes to the generation of stacking faults.[32] In both silicon and germanium, any work damage left on the substrate wafer as a result of polishing or handling will induce stacking faults, and heavy mechanical damage will cause polycrystallinity. Polycrystalline nodules are caused by some localized foreign matter such as lint or air-borne dust that is present on the substrate surface before

[31] T. B. Light, "Imperfections in Germanium and Silicon Epitaxial Films," *Proc. Conf. on Metallurgy of Semiconductor Materials*, Los Angeles, Sept. 1961, Ed. J. B. Schroeder, p. 137, Interscience, New York, N. Y., 1962.

[32] H. J. Queisser and R. H. Finch, "Stacking Faults in Epitaxial Silicon," *Jour. Appl. Phys.*, Vol. 33, p. 1536, April 1962.

growth. These gross imperfections are more of a problem with germanium than silicon; however, the growth of silicon layers one mil or more in thickness requires careful cleaning and protection of the layers from dust until the wafers are in the reactor. The best wafers will show no visible gross imperfections and a very low density of atomic faults. Typical deposits will have in the order of two or three thousand stacking faults and/or dislocations per square centimeter. Normal crystallographic etching and diffraction techniques show no detectable difference between the crystalline perfection of epitaxial and melt-grown silicon, with the exception of stacking faults. No significant electrical defects attributable to stacking faults at low densities have been observed. Macroscopic faults, such as polycrystalline bumps, have been observed to degrade p-n junctions.

Lifetime

The minority-carrier lifetime in the epitaxial layers was not measured during this investigation. This measurement is difficult because recombination is primarily controlled by layer thickness and an estimate of the lifetime parameter, based on device electrical characteristics, was considered sufficient. Transistors having a 0.2-mil base width show normal gains, and there is no indication that lifetime in the epitaxial layers is less than that needed for the manufacture of commercial epitaxial transistors, in either germanium or silicon. A lifetime of the order of 1 to 5 microseconds seems a reasonable estimate of this parameter.

Mobility

Direct mobility measurements on the epitaxial layers were not made because a comparison of resistivity and capacitance measurements was considered sufficient to provide an adequate evaluation of this parameter. The resistivity of the layers depends on both mobility and impurity concentration, while the capacitance depends on the concentration only; the agreement between these measurements provided indirect evidence that epitaxial silicon is not significantly different from the material prepared in other ways, and there is no evidence that it contains any abnormal scattering mechanisms.

APPLICATIONS

Transistors

The most extensive use of epitaxial layers at the present time is to provide thin 2 to 20-micron high-resistivity collector layers on low-

resistivity substrates (n on n^+ and p on p^+) for the manufacture of epitaxial transistors.[33] The heavily doped degenerate substrate provides a low-resistance contact to the collector and, thereby, reduces the stored charge. Most silicon and germanium high-speed computer-type switching transistors and certain types of power transistors use epitaxy to achieve a lower collector saturation voltage, a lower stored charge, and faster switching characteristics. Epitaxy is also used in silicon power transistors as a substitute for triple diffusion for the same reasons and because it permits use of thicker wafers to reduce breakage, provides better thickness control of the high-resistivity region, and produces less degradation of bulk properties by elimination of the long costly back-diffusion and lapping process.

Epitaxy can also be used advantageously in much more sophisticated ways. For example, grown-base n-p-n germanium transistors have been made in production quantities at RCA for nearly a year. The grown-base device is in every way equal to or better than the best double-diffused device. Another advantage of growing the base is that it avoids a long complicated p-type diffusion. Grown p-n junctions, fabricated completely by epitaxy, exhibit normal characteristics compared to other techniques of abrupt-junction formation. The epitaxial junctions can be graded by diffusion to increase breakdown or to provide an accelerating field in the base. Partially grown epitaxial junctions, in which the interface between the epitaxial layer and the substrate forms the junction, have also been fabricated successfully; however, unless special care is taken to reduce interface contamination or imperfections, the interface junctions may give rise to soft electrical characteristics. This effect is especially true for germanium. Again hydrogen chloride etching has been found very useful in improving interface diodes.

Other types of epitaxial multilayer devices have been fabricated, including a transistor made completely by epitaxial methods for use as a horizontal-deflection amplifier in television receivers. This device is shown in Figure 5. The photograph in the figure shows a 2-degree beveled section of the transistor, and the isometric schematic shows the details of the over-all structure. Some of the requirements of this transistor that were difficult to meet by diffusion have been achieved epitaxially, particularly that of a large current-handling capacity and low collector saturation resistance.

From a theoretical point of view, a homogeneous base–emitter con-

[33] M. J. Bentivegna, L. L. Lehner, and P. D. Lynch, "The Epitaxial Transistors," *Trans. IEEE Communications and Electronics*, Vol. 64, p. 393, Jan. 1963.

figuration has certain advantages over the exponentially graded base–emitter regions obtained by double diffusion.[31] In the homogeneous-type emitter, current crowding can be reduced by increasing the number of impurities under the emitter and, hence, reducing the base

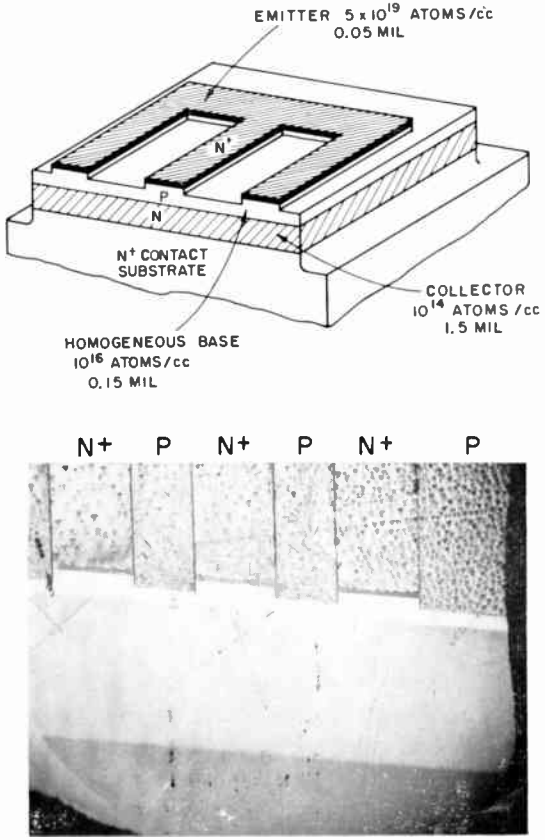

Fig. 5—An all-epitaxially-grown double-mesa power transistor.

resistance. This feature is shown in Figure 6. The emitter-to-base impurity ratio does not have to be reduced by this action; in fact, it can be increased if the base edge doping is reduced. This reduction in base doping increases the base resistance, but it increases the emitter efficiency. By contrast, deep diffusions decrease the net doping at both the emitter and base edge and, thereby, decrease the impurity ratio.

[31] A. R. Phillips, *Transistor Engineering*, Chap. 7-17, McGraw-Hill Publishing Co., Inc., New York, N. Y., 1962.

The reduction in the impurity ratio causes a corresponding decrease in emitter efficiency.

Homogeneous doping in the base should improve second break-down because of lower resistance, less current pinching, and reduced heating, and thus should permit the fabrication of transistors having narrower base widths, without punch-through, which improves current gain and frequency response. In all epitaxial transistors, base widths are independent of collector and base concentrations. An increase in the num-

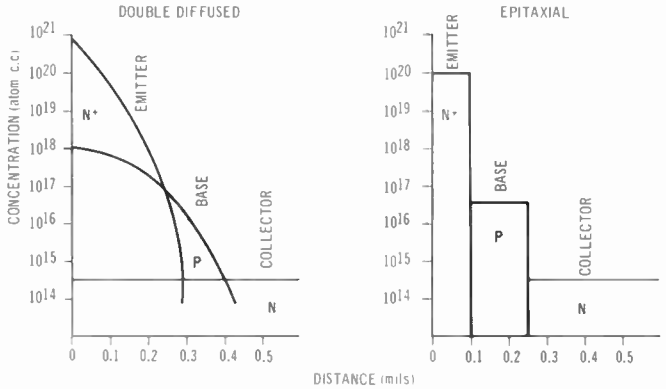

Fig. 6—Comparison between the impurity distribution in double-diffused and homogeneous epitaxial transistors.

ber of impurities in the base also reduces conductivity modulation of the base at high currents, and a decrease in impurity concentration under the emitter reduces the emitter capacitance. In addition, doping profiles in the emitter, the base, and the collector can be used as design parameters. In many cases, epitaxy could well provide a significantly less expensive method of fabrication. For these reasons, epitaxy can be an extremely important factor in transistor fabrication.

Another technique which may be useful in device fabrication is shown in Figure 7. An oxide-masked wafer has had areas in the mask opened. HCl, which does not attack the oxide, has been used to etch holes into the silicon wafer. The holes have then been refilled by epitaxial deposition. For thin depositions, the silicon grows preferentially in the opened areas. In this manner mesa, planar, or submerged structures have been created. Combinations of limited area growth and multiple layer growth makes possible three-dimensional structures heretofore unattainable by other fabrication techniques.

Diodes

Epitaxial techniques have been used advantageously in certain types of diodes. These techniques have been applied successfully to reduce the series resistance of silicon varactor diodes in a manner similar to that used in transistors.[35] Hyper-abrupt-type junctions in which impurity concentration decreases away from the junction are easily

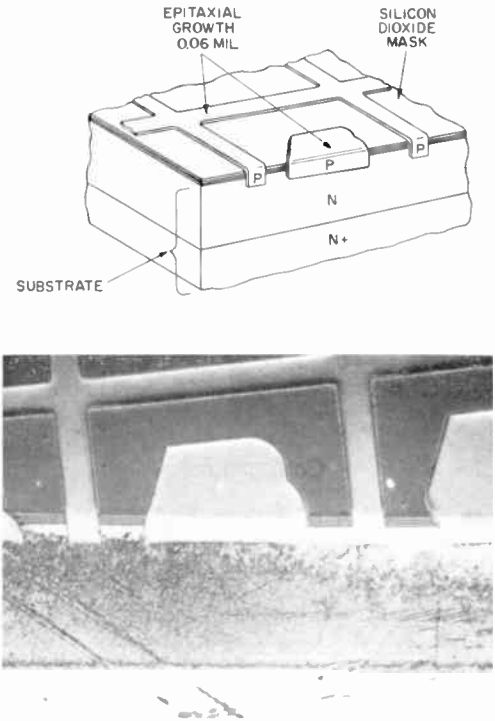

Fig. 7—Patterns cut into silicon substrate by high temperature HCl etching through oxide masks and refill with p-type preferential epitaxial growth.

fabricated epitaxially. One technique is to program an increase in doping as the layer growth progresses. Capacitance–voltage relations on layers with such retrograde doping show greater than square-root dependence. Other types of required impurity distributions can be similarly obtained. For example, if the impurity distribution is incorporated into the layer in a way that would cause the capacitance-

[35] H. Kressel and M. Klein, "High Power Epitaxial Silicon Varactor Diodes," *RCA Review*, Vol. 24, No. 4, p. 616, Dec. 1963.

voltage relation to become linear, the diode could be used to advantage as a tuner.

Metal-Oxide Semiconductor

Conduction channels have been grown for the metal-oxide field-effect transistor which have resulted in operable devices. Typical layers required for this type of device are in the order of 1000- to 25,000-angstrom n-type silicon on high-resistivity p-type wafers. The use of epitaxial techniques to produce this type of permanent channel shows potential for substantially improving the reproducibility of channel formation and for increasing stability.

Solar Cells

Epitaxial techniques have been used in the fabrication of solar cells. The impurity gradient in the bulk material can be graded so that minority carriers are accelerated toward the p-n junction. This type of grading decreases the dependence of the cell on minority-carrier lifetime and, therefore, improves its radiation resistance. Multiple junctions within the bulk of the cell can also improve radiation resistance by limiting the minority-carrier diffusion to a p-n junction.

Conclusions

The hydrogen reduction of silicon and germanium tetrachlorides to obtain epitaxial depositions has been developed into a reliable and controllable production process. The epitaxial processes reproduce the crystal characteristics of the substrate and produce single-crystal layers that have electrical properties equivalent to crystals produced by other techniques.

Hydrogen chloride etching is a highly desirable method for cleaning and polishing the substrates prior to the deposition of the epitaxial layers. Essentially, two techniques—solution and gas doping—are used to add the dopant impurities into the epitaxial layers. The doping concentration can be controlled over six orders of magnitude; this control is as good as or better than that for standard methods of doping semiconductors.

The necessary measurements for thin-film evaluation can be made although the techniques present some problems in production control. Measurements of junction capacitance as a function of reverse bias, although destructive, are extremely useful for analyzing the impurity distribution in the epitaxial layers.

Techniques have been developed that produce near-abrupt transi-

tions at the interface of the substrate and epitaxial layer by providing a means of sealing the back of the substrate prior to deposition in the epitaxial system. Controlled multiple-layer growth has been achieved, and silicon power transistors having an improved current-handling capacity have been fabricated wholly by epitaxial techniques.

Although, at present, epitaxy is used primarily to permit low-resistance contact to devices, it is felt that other device applications of epitaxy are significant and will lead to further exploitation of the processes.

ACKNOWLEDGMENTS

The authors wish to express appreciation to U. Roundtree for his contributions to the development of these techniques, to D. Kenney for the preparation of multilayers and for fabrication of the power transistor, to F. Yole for the fabrication and the evaluation of the power transistor, to the many device designers who have investigated the epitaxial materials, and to N. Ciampa and D. Boyer for their assistance during this program.

VAPOR-PHASE SYNTHESIS AND EPITAXIAL GROWTH OF GALLIUM ARSENIDE*

By

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***Summary**—Epitaxial layers of gallium arsenide have been grown from the vapor phase on (100) and (111) oriented gallium arsenide substrates. The gallium arsenide is synthesized in an open tube by the reaction of gallium trichloride (or hydrogen chloride) with gallium metal, followed by reaction with arsenic. The apparatus and conditions used to obtain single-crystal growth are described.*

The electrical characteristics of n-type layers, as derived from measurements on diodes, are shown to be dependent upon the partial pressure of arsenic within the system. Methods for producing p- and n-type layers by doping are discussed.

Introduction

TO ACHIEVE epitaxial growth of gallium arsenide from the vapor phase, it is necessary to introduce the components of the compound into the vapor phase in a form that allows them to combine and form a single crystal of the compound at the substrate surface. Gallium, unlike arsenic, is not easily vaporized and must be introduced in the form of one of its volatile compounds.

The most commonly reported method for the epitaxial growth of gallium arsenide employs the following reaction:

$$GaX_3 + 2GaAs \rightleftharpoons 3GaX + \tfrac{1}{2}As_4 \quad (X = Cl, Br, I). \qquad (1)$$

This reaction proceeds as written with increasing temperature, and reverses on cooling. The transport of gallium arsenide by this means has been studied in both closed-tube[1-4] and open-tube systems.[5-7]

* The work described was performed under the sponsorship of the Manufacturing Technology Laboratory, Aeronautical Systems Division, Air Force Systems Command, United States Air Force.

[1] V. J. Lyons and V. J. Silvestri ,"Vapor Growth of GaAs," *Jour. Electrochem. Soc.*, Vol. 108, No. 8, p. 177C, Aug. 1961.

[2] R. R. Moest and B. R. Shupp, "Preparation of Epitaxial GaAs and GaP Films by Vapor Phase Reaction," *Jour. Electrochem. Soc.*, Vol. 109, No. 11, p. 1061, Nov. 1962.

The closed-tube systems are inherently limited in their production capabilities, while the open-tube systems require a source of exceptionally pure gallium arsenide. This disadvantage of the latter type is offset by the fact that the chemical synthesis of gallium arsenide can be accomplished in an open tube,[8,9] and the open-tube system is well suited for preparing production quantities of epitaxial layers of controlled types and resistivities.

Description of the System

A schematic of the basic system used for the synthesis and epitaxial growth of gallium arsenide is shown in Figure 1. This system consists of a tee-shaped quartz tube that contains gallium in one arm and arsenic in the opposite arm. A mixture of gallium trichloride and hydrogen flows over the heated gallium, and the following reaction occurs:

$$GaCl_3 + 2Ga \rightleftharpoons 3GaCl. \qquad (2)$$

The arsenic from the opposing arm is sublimed in a second stream of hydrogen. The two streams mix at the center of the tee to form gallium arsenide, as in Equation (1). The mixed gas stream then flows down the third arm of the tee and over the wafers. The temperature of the wafers is kept below that of the tee, and more gallium arsenide is formed and is deposited epitaxially on the wafers.

There are many reasons for the selection of this arrangement to obtain epitaxial layers. First, high-purity gallium and arsenic are

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[3] N. Holonyak, Jr., D. C. Jillson, and S. F. Bevacqua, "Halogen Vapor Transport and Growth of Epitaxial Layers of Intermetallic Compounds and Compound Mixtures," *Proc. AIME Tech. Conf. on Metallurgy of Semiconductor Materials*, Los Angeles, Aug. 30-Sept. 1, 1961, Vol. 15, p. 49, John Wiley & Sons, Inc., New York, N. Y., 1962.

[4] G. R. Antell, "Investigation of a Method of Growing Crystals of GaP and GaAs from the Vapour Phase," *Brit. Jour. Appl. Phys.*, Vol. 12, No. 12, p. 687, Dec. 1961.

[5] F. V. Williams and R. A. Ruehrwein, "Mechanism for the Vapor Transport of Gallium Arsenide with Hydrogen Chloride," *Jour. Electrochem. Soc.*, Vol. 108, No. 8, p. 177C, Aug. 1961.

[6] R. L. Newman and N. Goldsmith, "Vapor Growth of Gallium Arsenide," *Jour. Electrochem. Soc.*, Vol. 108, No. 12, p. 1127, Dec. 1961.

[7] F. W. Tausch and T. A. Longo, "An Open Tube GaAs Epitaxial Process," Los Angeles Meeting of Electrochemical Society, May 1962.

[8] D. Effer and G. R. Antell, "Preparation of InAs, InP, GaAs, and GaP by Chemical Methods," *Jour. Electrochem. Soc.*, Vol. 107, No. 3, p. 252, March 1960.

[9] S. W. Ing, Jr. and H. T. Minden, "Open Tube Epitaxial Synthesis of GaAs and GaP," *Jour. Electrochem. Soc.*, Vol. 109, No. 10, p. 995, Oct. 1962.

commercially available and high-purity gallium trichloride is readily prepared.[10-11] Second, relatively low temperatures are used which, for the most part, need not be accurately controlled. Third, the use of two gallium arsenide deposit zones has the advantage that because the components of the gas stream leaving the tee are very close to thermodynamic equilibrium, the degree of supersaturation of reactants over

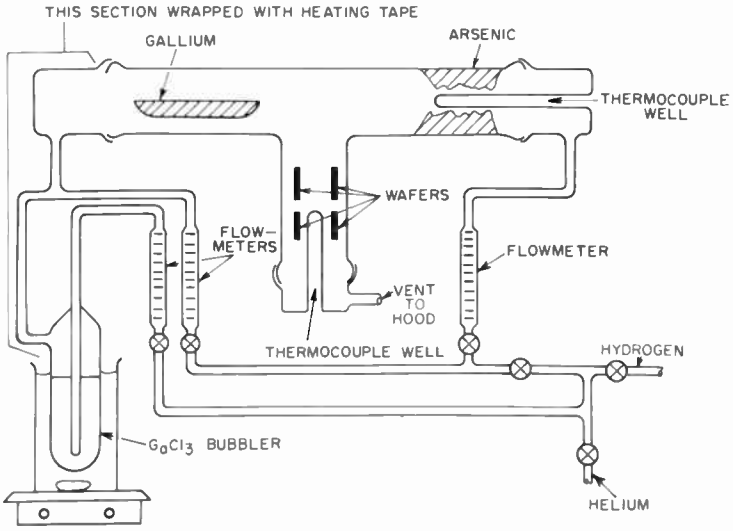

Fig. 1—Schematic of gallium arsenide vapor-phase-deposition apparatus.

the growing layer can be controlled, within limits, by fixing the difference in temperature between the two zones. In addition, the first zone can be used as a dump point for impurities which may have been introduced into the system. Fourth, as is shown subsequently, the resistivity of the layers can be controlled by varying the partial pressure of arsenic independently.

Materials and Techniques

In the synthesis and epitaxial growth of gallium arsenide, the

[10] N. Goldsmith, A. Mayer, and L. Vieland, "Preparation of High-Purity Gallium," *Jour. Less Common Metals*, Vol. 4, p. 564, 1962.

[11] W. Kern, "Zone Refining of Gallium Trichloride; Radiochemical Method for Determining the Distribution of Components in a Column and Its Application in Analyzing the Zone Refining Effectiveness in Purifying Gallium Trichloride," *Jour. Electrochem. Soc.*, Vol. 110, No. 1, p. 60, Jan. 1963.

gallium used is 99.9999% pure, and the arsenic is 99.999% pure. The transport agent, gallium trichloride, is prepared by the reaction of gallium with chlorine, followed by distillation and zone refining. Because gallium trichloride is hygroscopic and reactive, the zone-refining tube is sealed onto a side arm of the bubbler. The bubbler is filled periodically by melting a section of the chloride in the zone-refining tube. Pure hydrogen is obtained from a palladium diffusion furnace. Hydrogen chloride, bromine, and iodine have been used in place of gallium trichloride, but will not be considered here.

In a typical run, hydrogen is passed through the gallium trichloride at a flow rate of 50 cm^3/minute and the resulting mixture is diluted with a bypass stream of hydrogen at the rate of 250 cm^3/minute. The flow rate of hydrogen over the arsenic is maintained at 250 cm^3/minute. The gallium is maintained at 750°C, the center of the tee at 800°C, the arsenic at 425°C, the wafers at 725°C, and the gallium trichloride at 85°C. Resistance heaters controlled by autotransformers are used for furnaces. All the equipment including the gas lines is checked for leaks with the aid of a helium leak detector.

Experimental Results

Growth Characteristics

In the initial work of growing the epitaxial layers, (111) oriented gallium arsenide substrates were used. The $(\bar{1}\bar{1}\bar{1})$ face was chemically polished, and the (111) face was mechanically polished. Growth rates of 25 microns per hour were measured on the (111) face but the layers were irregular and the epitaxial interfaces poor. Although some difficulty was encountered, smooth growth was obtained on the $(\bar{1}\bar{1}\bar{1})$ face at a growth rate of 2.5 microns per hour. It was necessary to stand the wafers in pairs on edge in a slotted boat with their sides parallel to the gas stream and with their polished faces separated by 20 to 50 mils.

The devices for which these layers are intended are diffused, not alloyed; therefore, it is not necessary to restrict the layers to the (111) plane. Of the other major planes, the (100) plane is easy to polish chemically and yields very smooth surfaces at a growth rate of 13.5 microns per hour. When examined by x-ray and electron-diffraction techniques, the layers deposited on the (100) oriented substrates were shown to be monocrystalline. Unfortunately, no etch for revealing dislocations on the (100) plane has been found; as a result, no information could be obtained about the dislocation density.

Irregularities in the growth on the (100) face are generally of two types. One type consists of small circles that are most probably the

result of improper cleaning of the substrate. The other type, small hillocks extending across the wafer surface that are associated with small leaks in the gas lines, are most likely caused by oxygen. A leak rate of about 10^{-4} standard cm^3 of air per second causes sufficient interference with the reactions involved so that the growth rate is reduced to virtually zero. The growth rate is also relatively sensitive to gallium temperature, approximately doubling for each 50° rise in the range 700 to 850°C.

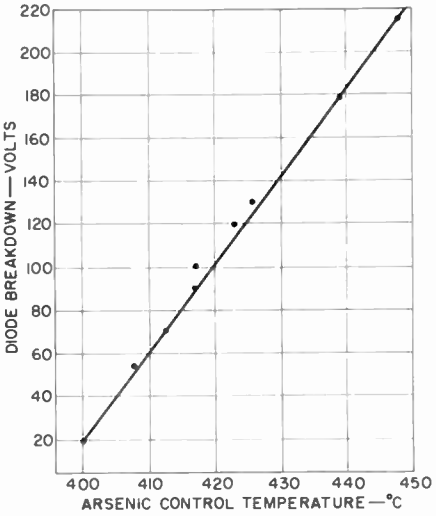

Fig. 2—Gallium arsenide epitaxial diodes reverse breakdown versus arsenic temperature.

Electrical Properties

The electrical properties of the epitaxial layers can be conveniently evaluated from measurements of small-area diodes.[12] The diode breakdown is indicative of the net carrier concentration, and a detailed plot of the capacitance–voltage curve for the diode will reveal any nonuniformity of the layer. Measurements of the small-area diodes showed that undoped layers, grown under normal conditions, are n type and have carrier concentrations in the low 10^{16} cm^{-3} range. However, if the partial pressure of the arsenic within the system is changed by changing the control temperature of the arsenic zone, the net carrier concentration varies. This effect is best illustrated by the curve in Figure 2 which shows the diode breakdown as a function of the arsenic

[12] H. Kressel and N. Goldsmith, "High-Voltage Epitaxial GaAs Microwave Diodes," *RCA Review*, Vol. 24, No. 2, p. 182, June 1963.

control temperature. This sensitivity of the concentration to the arsenic pressure is not understood. It has even been possible to produce p-type layers by using relatively high arsenic pressures, but this effect is not reproducible.

Because small changes in temperature of the arsenic during the preparation of the layers have a profound effect upon their electrical properties, the temperature in the arsenic zone of the system must be precisely controlled. The problem of maintaining a zone at temperatures near 425°C which is in contact with a zone at 800°C was solved by dividing the arsenic zone into two individually controlled sections. The arsenic is placed in the section further from the center of the tee.

The slope for a log–log plot of capacitance as a function of voltage for diodes fabricated before this change was made was typically 0.2, which indicated that the layer increased in carrier concentration with depth, or, viewed another way, that the average arsenic temperature increased with time. The average slope of the capacitance–voltage curve for diodes fabricated after the change was made in the method of temperature control was 0.47.

Doping

Three materials—sulfur monochloride, hydrogen sulfide, and tellurium—were investigated to determine which would be most suitable for the n-type doping of the epitaxial deposits. Of the three, hydrogen sulfide, diluted with hydrogen, was found to be the most easily controlled. For this purpose, a stainless-steel dilution system was built and connected so that a measured flow of doped gas could be introduced into the main gas stream on the arsenic side of the system. The curve in Figure 3 shows the control obtainable using this method. The concentration of hydrogen sulfide in the dopant gas was about 0.0015 per cent.

Carrier concentrations were measured using a technique similar to that described by Kudman.[13] A Beckman IR 5-A having a microreflectance attachment was used to obtain the reflectance curves. Samples of known carrier concentration were used to construct a calibration curve, shown in Figure 4, for the wavelength of the reflection minimum as a logarithmic function of the concentration. Three points from the work of Spitzer and Whelan[14] are included in this plot.

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[13] I. Kudman, "A Non-Destructive Measurement of Carrier Concentration in Heavily Doped Semiconducting Materials and Its Application to Thin Surface Layers," *Jour. Appl. Phys.*, Vol. 34, p. 1826, June 1963.

[14] W. G. Spitzer and J. M. Whelan, "Infrared Absorption and Electron Effective Mass in n-Type Gallium Arsenide," *Phys. Rev.*, Vol. 114, No. 1, p. 59, April 1, 1959.

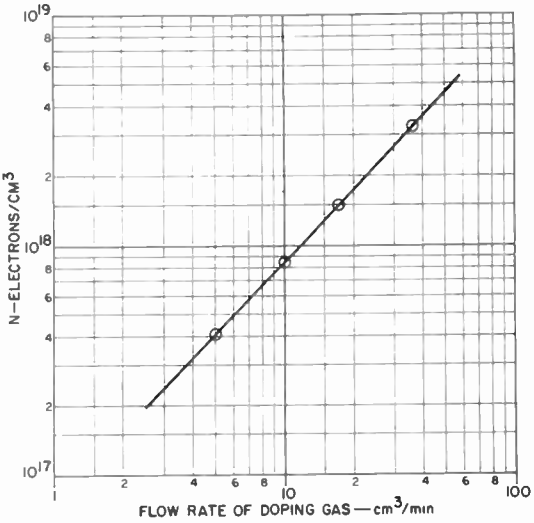

Fig. 3—Electron concentration versus flow rate of 0.0015% H_2S in H_2.

It is difficult to estimate the amount of sulfur that remains in the system as a background. The doping experiments were performed in a system that used hydrogen chloride as the transport agent. The lowest carrier concentration attained in this system for undoped runs

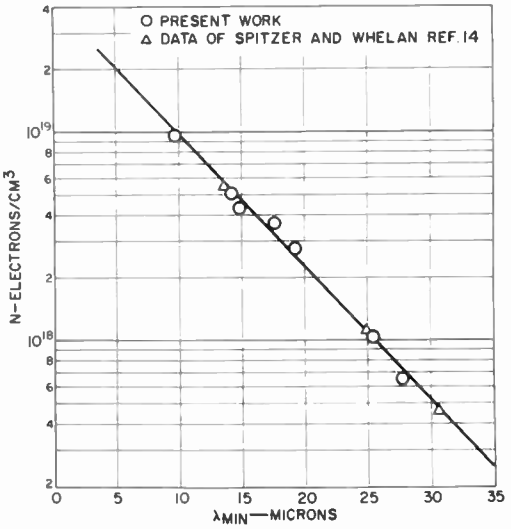

Fig. 4—Electron concentration versus wavelength of minimum reflection.

was in the mid to high 10^{16} cm^{-3} range. However, it is important to note that the point corresponding to the lowest carrier concentration was obtained on a run directly following the one for which the highest carrier concentration was obtained. This result indicates that the "memory" effect is not severe. The maximum carrier concentration attainable using sulfur as a dopant was found to be 4.0×10^{18} cm^{-3}.

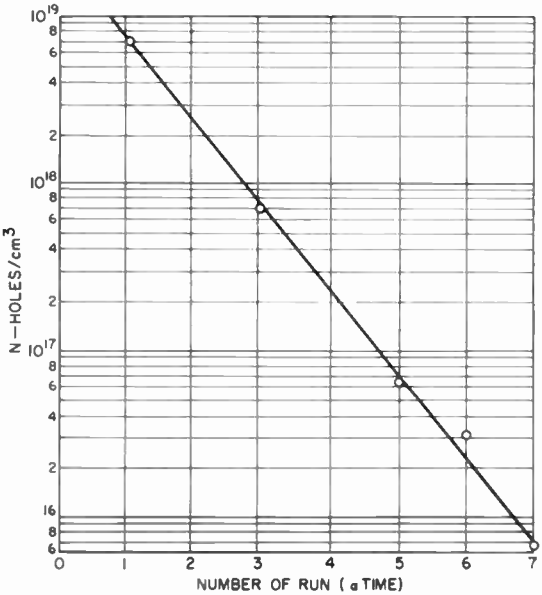

Fig. 5—Hole concentration versus running time (zinc-doped GaAs).

The p-type doping of the gallium-arsenide deposits was found to be more difficult. In the initial work, weighed quantities of zinc were placed directly in the boat containing the gallium. In a typical experiment, 6 milligrams of zinc was placed in 20 grams of gallium. The system was then operated in a series of one-hour runs until n-type layers were produced. Measurement of the p-type layers obtained showed a steady decrease in carrier concentration as a function of running time (Figure 5).

Other Applications

The deposition of epitaxial layers of gallium arsenide on germanium using the system discussed in this paper is described by

Amick.[15] By use of phosphorus in place of arsenic, the synthesis of gallium phosphide under almost identical conditions has been accomplished. It should be pointed out that the method is general and should be easily applicable to the arsenides and phosphides of indium and aluminum, as well as to compounds such as the selenides and tellurides of group III. The extension of this work to the preparation of mixed crystals of gallium arsenide and gallium phosphide, for example, with definite or continuously variable proportions is obvious.

ACKNOWLEDGMENTS

The authors thank I. Kudman for suggesting the use of infrared reflectivity for the determination of carrier concentration and A. Mayer and J. A. Amick for their helpful discussions.

[15] J. A. Amick, "The Growth of Single Crystal Gallium Arsenide Layers on Germanium and Metallic Substrates," *RCA Review*, Vol. 24, p. 555, Dec. 1963.

THE GROWTH OF SINGLE-CRYSTAL GALLIUM ARSENIDE LAYERS ON GERMANIUM AND METALLIC SUBSTRATES*

By

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Princeton, N. J.

Summary—A new apparatus is described for the deposition of gallium arsenide layers on freshly cleaned substrates. In this apparatus, gallium arsenide layers have been deposited on (111) oriented single-crystal substrates of germanium and on molybdenum and tungsten substrates. On germanium substrates, both smooth and "grainy" deposits are obtained, both of which appear to be essentially single crystal, as determined from Laue patterns. The method of etching the germanium substrate prior to growth is described, and the crystallographic, chemical, and electrical properties of the deposits are presented.

Gallium arsenide layers on molybdenum are randomly oriented polycrystals, but on tungsten the layers consist of highly oriented crystalline grains.

Introduction

THE deposition of gallium arsenide layers on germanium substrates affords a unique opportunity to study epitaxial growth; this combination of materials is truly unusual in that the physical and crystallographic properties of the deposit and the substrate are almost identical, while their chemical and electrical properties are dissimilar. As a consequence, it is possible to remove one of the components by chemical etching and to correlate defects observed on the surface of the epitaxial layer with irregularities appearing at the interface between the two materials. This information will be especially helpful in interpreting unusual electrical properties of gallium arsenide–germanium junctions.

In this paper, a new apparatus for the deposition of gallium arsenide layers on freshly cleaned substrates is described. Preliminary observations are reported for the microscopic and crystallographic character

* Much of the information contained in this paper was presented at a conference on "Single Crystal Thin Films" held at the Philco Scientific Laboratory, Bluebell, Pa., May 13-15, 1963 and will appear in the proceedings of this conference to be published early in 1964.

of gallium arsenide layers epitaxially grown on germanium substrates. Gallium arsenide layers have also been deposited on molybdenum and tungsten substrates; these will be discussed briefly.

Mismatch between Gallium Arsenide and Germanium

The excellent match in physical and crystallographic properties of these two semiconductors is shown in Table I. According to recent measurements by J. G. White, their lattice constants differ by less than 0.1% at room temperature and, over the range 0° to 600°C, their linear thermal coefficients of expansion differ by less than 4%. Thus, even

Table I

Semiconductor	Lattice Constant (Angstroms)	Thermal Coefficient of Expansion† (cm/cm per °C)
Germanium	5.6576*	6.19×10^{-6}
Gallium Arsenide	5.6534	5.93×10^{-6}

* This value from M. E. Straumanis and E. Z. Aka, "Lattice Parameters, Coefficients of Thermal Expansion, and Atomic Weights of Purest Silicon and Germanium," *Jour. Appl. Phys.*, Vol. 23, p. 330, March 1952.

† Over the temperature range 20°C to 600°C.

at the growth temperatures used to deposit gallium arsenide layers, the mismatch in lattice constant is only about 0.1%. On a simple atomistic model, this mismatch could be met by inserting, for the first monolayer only, extra rows of atoms on a linear array having a repeat distance of about 5000 Å. This is equivalent to the insertion of about 4×10^4 such extra rows per square centimeter. Actually, van der Merwe[1] has proposed that for such a small mismatch as 0.1%, the deposit will grow to a characteristic thickness without introducing dislocations until the increasing strain energy requires their formation.

Chemical Reactions Used in Gallium Arsenide Growth

Gallium arsenide layers have been deposited on germanium substrates by a number of workers. Holonyak et al[2] used a sealed-tube reaction similar to that described by Marinace[3] who had previously

[1] J. H. van der Merwe paper No. 18, Conference on Single-Crystal Films, Blue Bell, Pa., May 13-15, 1963.

[2] N. Holonyak, Jr., D. C. Jillson, and S. F. Bevaqua, *Metallurgy of Semiconductor Materials XV*, p. 49, Interscience Pub. (John Wiley & Sons), New York, 1949.

[3] J. C. Marinace, "Epitaxial Growth of Ge Single Crystals in a Closed Cycle Process," and, "Tunnel Diodes by Vapor Growth of Ge on Ge and GeAs," *IBM Jour. of Research*, Vol. 4, p. 248 and p. 280, July 1960.

carried out the inverse sequence of depositing germanium on gallium arsenide substrates. Sealed-tube reactions have the inherent disadvantage that, in successive runs, it is difficult to prepare material having the same electrical properties. As a result, open tube or flow systems have been used more recently in preparing gallium arsenide deposits. Newman and Goldsmith[4] passed the transport agent HCl over a gallium arsenide source, and the same reaction has been employed by Blakeslee[5] and by Weinstein et al.[6] Stopek[7] has used the combination hydrogen plus arsenic trichloride plus gallium as starting materials for depositing gallium arsenide layers.

To obtain independent control over the partial pressures of the arsenic species and the gallium species present in the vapor during growth, Goldsmith[8] used arsenic, gallium, and gallium trichloride as starting materials in a hydrogen atmosphere. The reaction sequence used in the work described here is chemically similar to that of Goldsmith and includes the following steps:

$$\text{(a)}\quad 4\,As_{solid} \xleftarrow{400\text{ to }450^\circ C} As_{4\ vapor}$$

$$\text{(b)}\quad HCl_{vapor} + Ga_{liquid} \xleftarrow{700\text{ to }800^\circ C} GaCl_{3\ vapor}\ (90\%) + GaCl_{vapor}\ (10\%)$$

$$\text{(c)}\quad 3\,GaCl_{vapor} \xleftarrow{600\text{ to }700^\circ C} 2\,Ga_{surface} + GaCl_{3\ vapor}$$

$$\text{(d)}\quad Ga_{surface} + 1/4\,As_4 \xleftarrow{600\text{ to }700^\circ C} GaAs_{solid}.$$

By placing the arsenic and the gallium in separate branches of a "T" apparatus, the partial pressure of the arsenic vapor and of the gallium monochloride vapor introduced into the reaction zone can be independently varied. The apparatus in which these reactions are carried out is described in detail below.

On the basis of experimental observations made by Richman,[9] it

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[4] R. L. Newman and N. Goldsmith, Recent News Item, J. Electrochemical Soc. Meeting, Pittsburgh, Pa., April 15-18, 1963.

[5] A. E. Blakeslee, Recent News Item II-3, Electrochemical Soc. Meeting, Pittsburgh, Pa., April 15-18, 1963.

[6] M. Weinstein, A. A. Menna, and A. I. Mlavsky, "Preparation and Properties of Epitaxial GaAs-GaP, GaAs-Ge, and GaP-Ge Heterojunctions," Abstract No. 59-A, Electrochem. Soc. Meeting, Pittsburgh, Pa., April 15-18, 1963.

[7] S. Stopek, Recent News Item II-2, Electrochemical Soc. Meeting, Pittsburgh, Pa., April 15-18, 1963.

[8] N. Goldsmith and W. Oshinsky, "Vapor-Phase Synthesis and Epitaxial Growth of Gallium Arsenide," *RCA Review*, Vol. 24, p. 546, Dec. 1963.

[9] D. Richman, "Gas Phase Equilibria in the System GaAs-I_2," *RCA Review*, Vol. 24, No. 4, p. 596, Dec. 1963.

is believed that the active halide is the monochloride rather than the dichloride. Depositions are normally carried out in a hydrogen atmosphere but will also take place in helium, hence disproportionation of the monochloride must be a primary reaction. The relative concentrations of the trichloride and the monochloride were estimated by Goldsmith[8] using available thermodynamic data.

Reaction (c) is shown as taking place on the substrate surface. That the reaction is surface catalyzed can be inferred from the observation that no gallium arsenide deposit forms on the quartz support rods in the immediate vicinity of the substrate wafers. Nucleation apparently will not take place on the quartz if a germanium wafer is nearby.

Substrate Materials

The germanium substrate wafers were obtained from the RCA Semiconductor Division as (111) oriented single-crystal slices having one surface mechanically polished to a mirror finish. Thicknesses of 10 to 25 mils were employed and resistivities ranged from 10^{-2} to 10 ohm-cm, both p and n-type. Dislocation densities were measured to be about $10^3/cm^2$. No correlation between the crystalline or microscopic character of the gallium arsenide deposits and the purity of the germanium substrates was noted.

Substrate Preparation

Perhaps the most critical step in the growth of gallium arsenide layers on foreign substrates is the substrate pre-cleaning step. The substrate surface is critical since it strongly influences the nucleation of the gallium arsenide deposit. Ideally, the substrate surface should be free of chemical contaminants such as oxide layers at the time nucleation takes place. It should also be free of work damage such as is usually left by mechanical polishing of the wafer. Furthermore, it is desirable that the surface of the substrate be free from macroscopic structure, such as the "orange-peel" left by solution etching in aqueous reagents.

These conditions can be met by etching a germanium substrate wafer in gaseous hydrogen chloride in the same apparatus in which growth will subsequently take place. At temperatures in the neighborhood of 800°C, HCl reacts with germanium oxide to form volatile germanium chlorides and water. Furthermore, the surface remaining on the substrate, after approximately 1/1000 inch has been removed by etching, is mirror smooth and free from structure, even on a microscopic level. Such a surface is free of any mechanical damage left by previous polishing and contains only chloride ions as potential impuri-

ties. Since these are present in the growth system in any case, the surface can be regarded as "clean" in both a crystallographic and a chemical sense.

A germanium substrate wafer etched in gaseous HCl is shown in Figure 1, along with a multiple-beam interference micrograph and a phase-contrast micrograph obtained at a magnification of 1000×. From these it is seen that the surface is essentially optically flat and structureless.

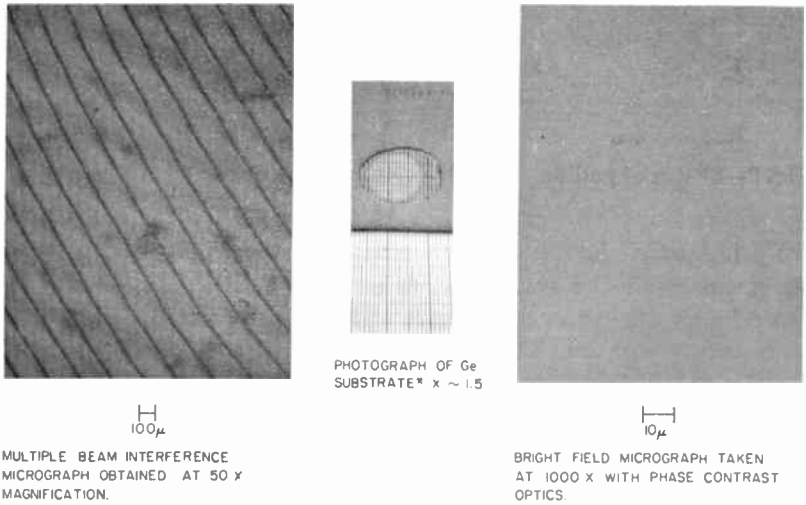

Fig. 1—Photograph and micrographs of HCl etched germanium substrate. Central bright elliptical area in photograph is a 1000 Å evaporated silver layer used to enhance reflectivity in multiple-beam interference.

Deposition Apparatus

The apparatus in which both the etching and the growth steps are carried out is shown schematically in Figure 2. This system is modified from that of Goldsmith[8] by the substitution of HCl as a carrier gas and by the addition of the etching zone. The etching zone is separated from the growth zone by a large bore Pyrex stopcock* which serves to isolate the growth zone from the atmosphere while the substrates are inserted or withdrawn from the apparatus. All standard taper joints are greased with Halocarbon† stopcock grease on the outer half of

* Wilmad Glass Co., Inc., Buena, N. J.

† Halocarbon Products Corp., Hackensack, N. J.

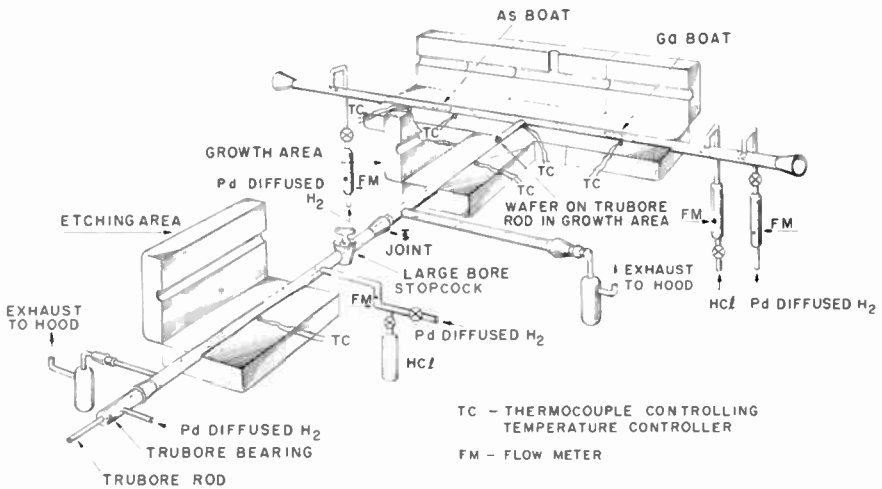

Fig. 2—Sketch of gallium arsenide deposition apparatus with furnaces open.

the joints only. In this manner, contact of the stopcock grease with the gases inside the system is minimized. Furthermore, all standard taper joints are far enough removed from the furnaces so that their temperature is that of the room ambient.

The substrate wafers are mounted vertically in a slotted quartz flat attached to a Trubore* quartz rod, as shown in Figure 3. This rod

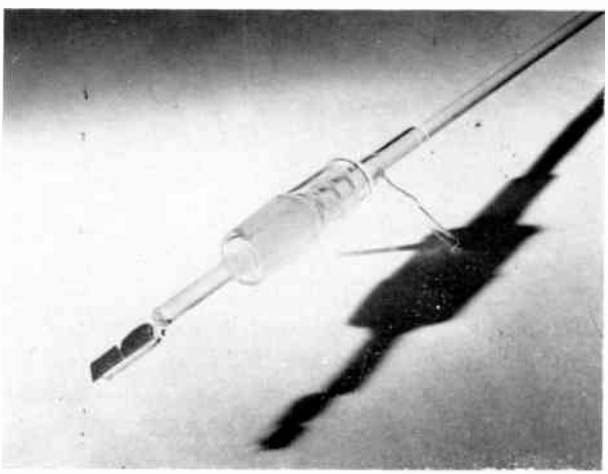

Fig. 3—Photograph of quartz Trubore rod and bearing with mounted germanium substrate wafers.

* Wilmad Glass Co., Inc., Buena, N. J.

fits tightly into a Trubore Pyrex bearing and provides the degree of freedom which permits moving the substrates from the etching zone into the growth zone. To minimize back diffusion of air into the apparatus through this bearing, hydrogen is forced into the center of the bearing through a side arm as shown in Figure 2. This "hydrogen seal" reduces the oxygen pressure in the system to a pressure estimated as less than 10^{-6} mm Hg.

All furnaces are independently temperature controlled and, following a suggestion of N. Goldsmith, the arsenic furnace is split transversely into two sections, each of which is independently temperature controlled. In this way, the arsenic boat can be kept at a uniform pre-set temperature which varies by no more than 5°C along the length of the boat. Temperatures are monitored with Chromel/Alumel thermocouples located between the furnace and the quartz reaction system.

Gaseous reactants are monitored into the system with flowmeters and needle-bore stopcocks.* Normally, flow rates of about 200 cc per minute of hydrogen are introduced into each arm of the "T". The HCl is introduced as a carrier gas at about 0.5 cc per minute. For etching, compositions of 2.5% to 30% HCl in hydrogen have been found satisfactory.

Usually, the substrates are first etched in the etching zone with the growth furnaces at room temperature. The wafers are then inserted into the growth zone and the growth furnaces are turned on simultaneously. When all furnaces have come up to temperature, the flow of carrier HCl is established and continued for the duration of the run.

Reagents

The reagents used in preparing the gallium arsenide layers were

Gallium, 99.9999% from Alcoa Chemicals

Arsenic, 99.999% from American Smelting and Refining Co., South Plainfield, N. J.

Hydrogen, Palladium diffused.†

Helium, Tank helium was used, unpurified, only to displace air from the system prior to a run.

Hydrogen Chloride gas, 94+%, Matheson‡ Lecture Cylinders.

The hydrogen chloride is by far the least pure material employed in the deposition. Currently, HCl gas is being synthesized at RCA Laboratories so that depositions can be carried out at higher purity.

* Fischer and Porter Co., Hatboro, Pa.

† Engelhard Industries, Newark, N. J.

‡ Matheson Co. Inc., East Rutherford, N. J.

Characteristics of Layers Grown on Germanium Substrates

The surfaces of gallium arsenide deposits on germanium substrates can be either "grainy" or smooth. Growth temperatures in the neighborhood of 700°C usually lead to a grainy surface whereas higher temperatures, in the neighborhood of 750°C, lead to smooth surfaces, as shown in Figure 4. In either case the gallium arsenide deposit is

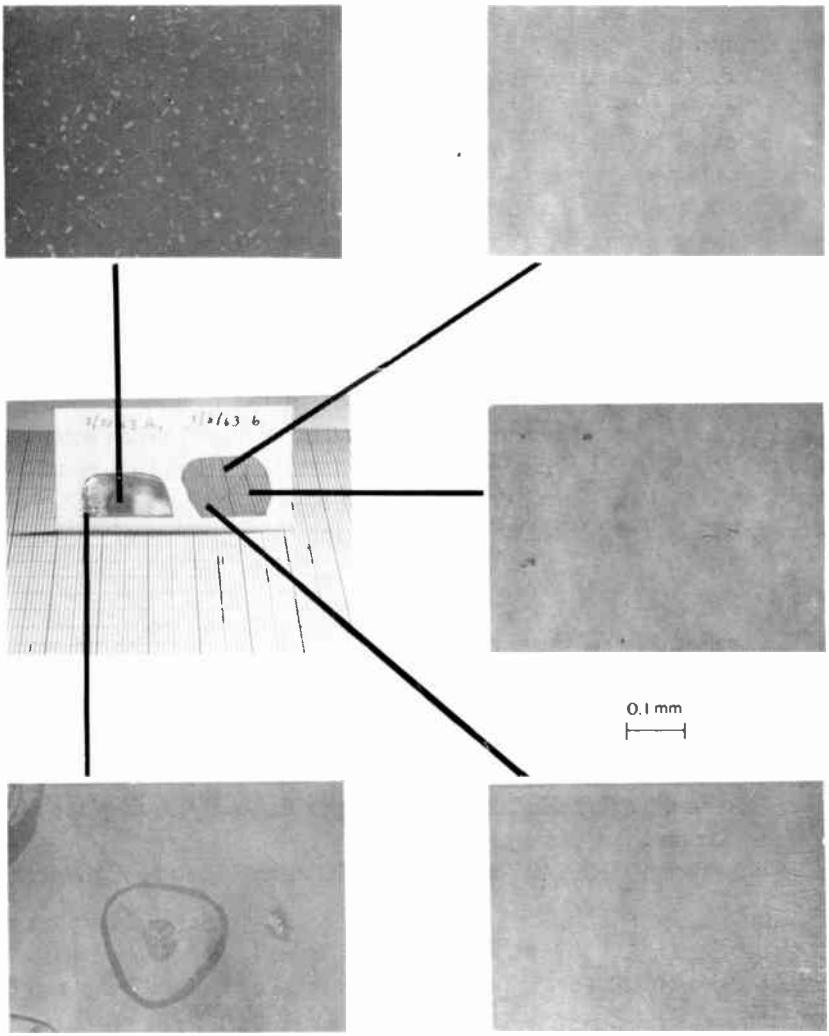

Fig. 4—Surfaces of wafers of GaAs on Ge grown at high and low temperatures: left wafer 2/20/63a grown at 720°C, right wafer 1/8/63b grown at 750°C.

essentially a single-crystal extension of the germanium substrate. Laue back reflection patterns obtained on the two deposits of Figure 4 are shown in Figure 5. A Laue pattern obtained on a single-crystal

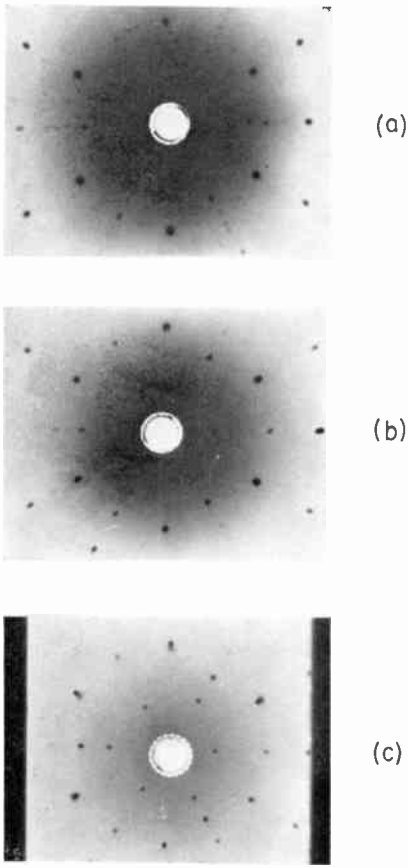

Fig. 5—Laue patterns of bright and grainy gallium arsenide layers deposited on germanium substrates: (a) matte surface, wafer 2/20/63a; (b) smooth surface, wafer 1/18/63b; (c) single crystal of GaAs for reference.

wafer of gallium arsenide is also shown for comparison. Extra Laue spots can be seen in the pattern obtained from the lower temperature deposit, showing that the crystallinity is less perfect in this layer. The pattern nevertheless retains the threefold symmetry of the 111 axis and clearly shows the orienting effect of the germanium substrate.

Characteristic surface defects are often observed on the "as grown" surfaces, especially where the growth is mostly mirror smooth. Such

defects are shown in Figures 6 and 7 and include the defects reported for silicon epitaxial layers by Flint, Lawrence, and Tucker,[10] namely pyramids, raised triangles, and holes extending to the germanium surface.

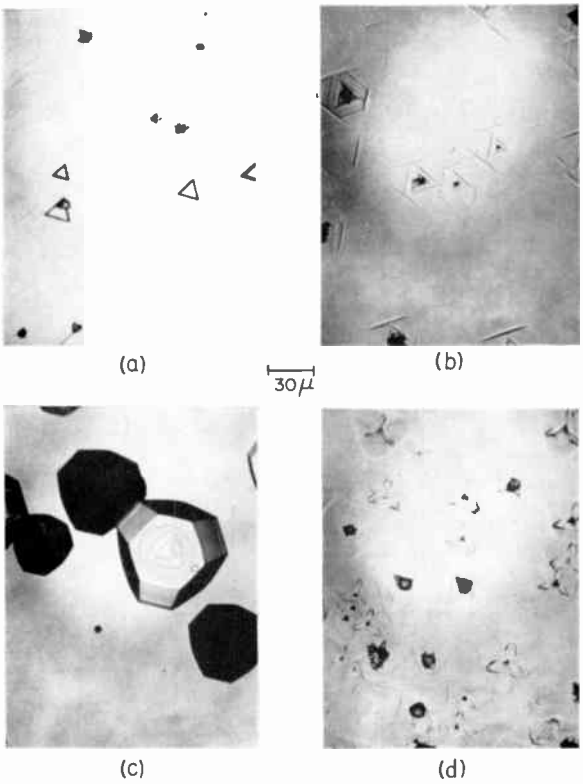

Fig. 6—Characteristic defects seen on epitaxial deposits of gallium arsenide on germanium. Growth temperature: (a) 750°C, (b) 730°C, (c) 710°C, (d) 700°C.

The interface between the gallium arsenide deposit and the germanium substrate is easily seen following angle-lapping since the two semiconductors are different in color (Figure 8). This interface is almost invariably a straight line when viewed at magnifications of 300 ×. This is reassuring both because it confirms the smoothness of the original substrate surface and because it shows that alloying of the deposit with the germanium substrate is not extensive. Note that

[10] P. S. Flint, J. E. Lawrence, and R. Tucker, "Silicon Epitaxial (111) Surface Defects," Abstract No. 73, Electrochem. Soc. Meeting, Pittsburgh, Pa., April 15-18, 1963.

layer 2/19/63 a_1 exhibits considerable porosity. Such porosity is characteristic of growth at temperatures in the range 700° to 720°C and is correlated with the appearance of extra spots in the Laue back reflection pattern.

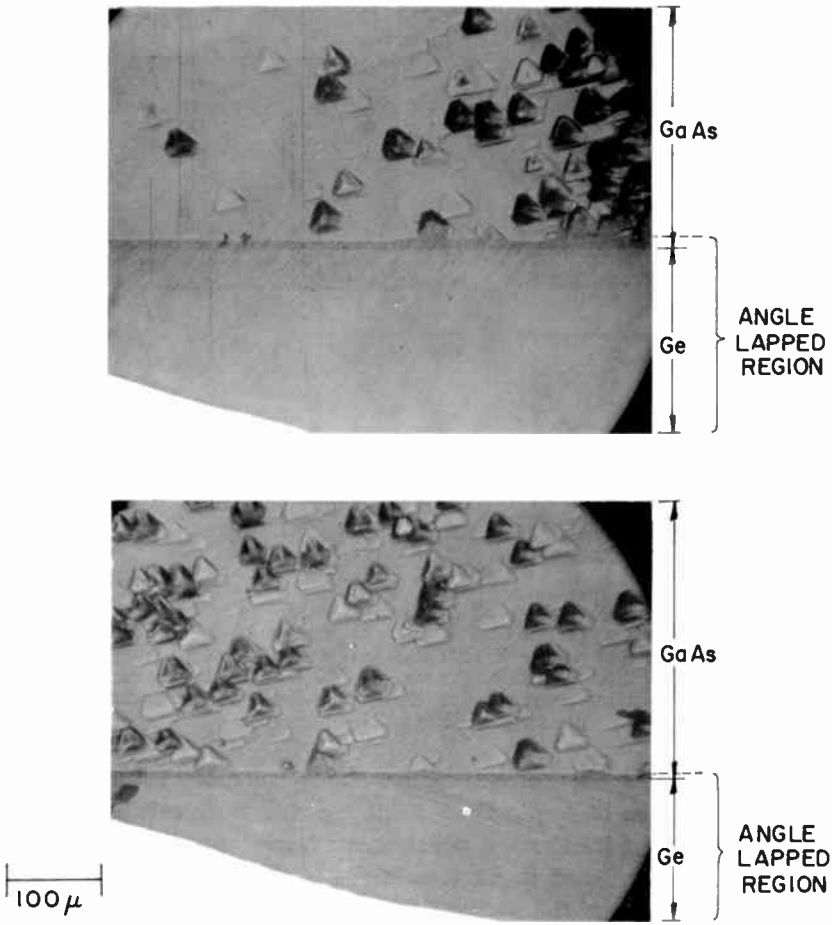

Fig. 7—Characteristic defects seen on epitaxial deposits of gallium arsenide on germanium. Deposit has been angle-lapped at 5° to show the projection of the defects above the surface. Note that both dark and light defects project upward. (Thickness of layer: about 0.8 micron.)

Polarity of the Gallium Arsenide Layer

The (111) face of a gallium arsenide crystal possesses different crystallographic and chemical properties from the $(\bar{1}\bar{1}\bar{1})$ face. The so-called "arsenic" face can be distinguished because, on exposure to

concentrated nitric acid, it reacts to form a dark colored stain. The "gallium" face remains unattacked and does not darken. This test has been applied by F. Hawrylo to the gallium arsenide deposits prepared as described above. In every case the outer surface of the gallium arsenide deposit was observed to stain, indicating that the arsenic surface was outermost.

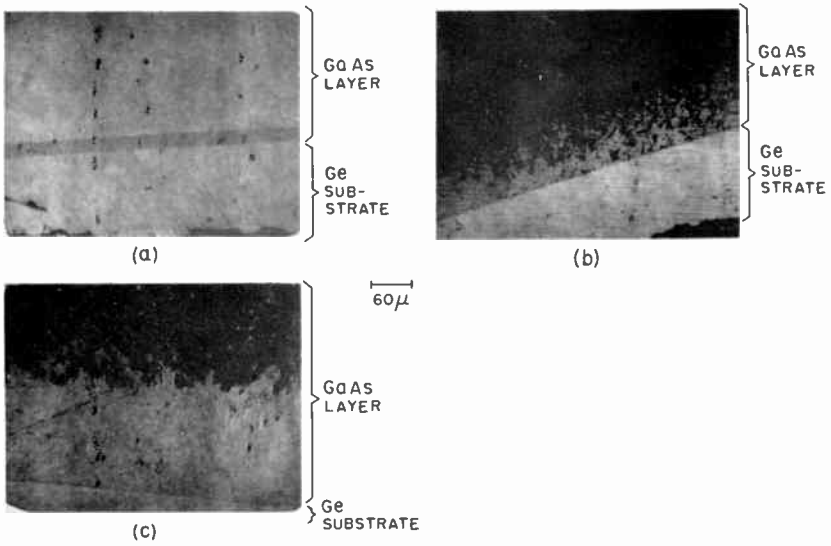

Fig. 8—Angle-lapped wafers of gallium arsenide on germanium showing the interface region (lapped at 5°): (a) wafer 12/3/62a_2, 2.1 μ thick, grown at 745°C; (b) wafer 2/19/63a_1, 7.95 μ thick, grown at 720°C; (c) wafer 2/20/63b_2, 26.5 μ thick, grown at 720°C (substrate inserted into growth furnace after operating temperature had been reached). Note porosity in layers (b) and (c).

To check this conclusion further, the germanium substrate was removed from the back of a thick gallium arsenide deposit by lapping. The gallium arsenide surface which was revealed by this process did not stain when exposed to nitric acid. It is therefore concluded that with this apparatus, the gallium face always forms adjacent to the germanium substrate surface and the arsenic face is outermost.

This conclusion can be rationalized by the known difference in the solubility of gallium and arsenic in germanium, as suggested by R. L. Rouse. Gallium is more soluble in germanium than arsenic[11] is

[11] F. A. Trumbore, "Solid Solubilities of Impurity Elements in Germanium and Silicon," *Bell Syst. Tech. Jour.*, Vol. 39, p. 205, Jan. 1960; see also F. A. Trumbore, W. G. Spitzer, R. A. Logan, and C. L. Luke, "Solid Solubilities of Antimony, Arsenic, and Bismuth in Germanium from a Saturation Diffusion Experiment," *Jour. Electrochem. Soc.*, Vol. 109, p. 734, Aug. 1962.

by at least a factor of 6. Furthermore, the vapor pressure of arsenic and its diffusion constant in germanium are both higher than the corresponding gallium values. Hence, it is anticipated that the first layer of depositing atoms should be mostly gallium, as is observed.

That this observation is not valid for all depositions of gallium arsenide on germanium is indicated by the results of other workers. Gottlieb and Corboy[12] have observed that in their apparatus, the arsenic face forms outermost, which is the same polarization as reported in this work. Newman and Goldsmith,[1] however, found that the gallium face was outermost following growth. Okada[13] has also reported that the outermost surface is predominantly gallium although small portions of the deposit in the early stages of growth show the arsenic face outermost. Apparently the polarity of a gallium arsenide layer grown on a germanium substrate is dependent on the chemical species present and their concentrations, or on the cleanliness of the substrate surface at the time of nucleation.

Correlation of Surface Defects with Irregularities at the Interface

One example of the correlation which can be made between defects appearing at the surface of the epitaxial layer and irregularities present at the interface between the layer and the substrate is shown in Figure 9. On the left, the "as grown" gallium arsenide surface is seen consisting of a generally smooth area with a few pyramidal mounds. In the center of one of these mounds a defect is observed which is shown enlarged in the micrograph above it. Such defects have been observed in a few percent of all such pyramidal growths. This particular defect is characterized by a triangular outline from one edge of which a line runs down the inclined face of the pyramid. Because the growth steps do not close as they cross this line, it is evidently associated with a spiral fault.

In the central micrograph, the same region is shown except that the gallium arsenide deposit has been partially removed by an etch in a hot mixture of hydrochloric and nitric acids, 1 to 1. Here it is apparent that the center of the pyramid etches more rapidly down to the interface than the smoother surrounding area, strongly suggesting that a screw type dislocation is present at the core of the pyramids.

After a second etch which served to remove most of the residual gallium arsenide layer, the micrograph on the right was obtained. In

[12] G. E. Gottlieb and J. F. Corboy, "Epitaxial Growth of GaAs Using Water Vapor," *RCA Review*, Vol. 24, p. 585, Dec. 1963.

[13] T. Okada, "Vapor Growth of GaAs in the Polar Direction," *Japanese Jour. Appl. Phys.*, Vol. 2, p. 206, 1963.

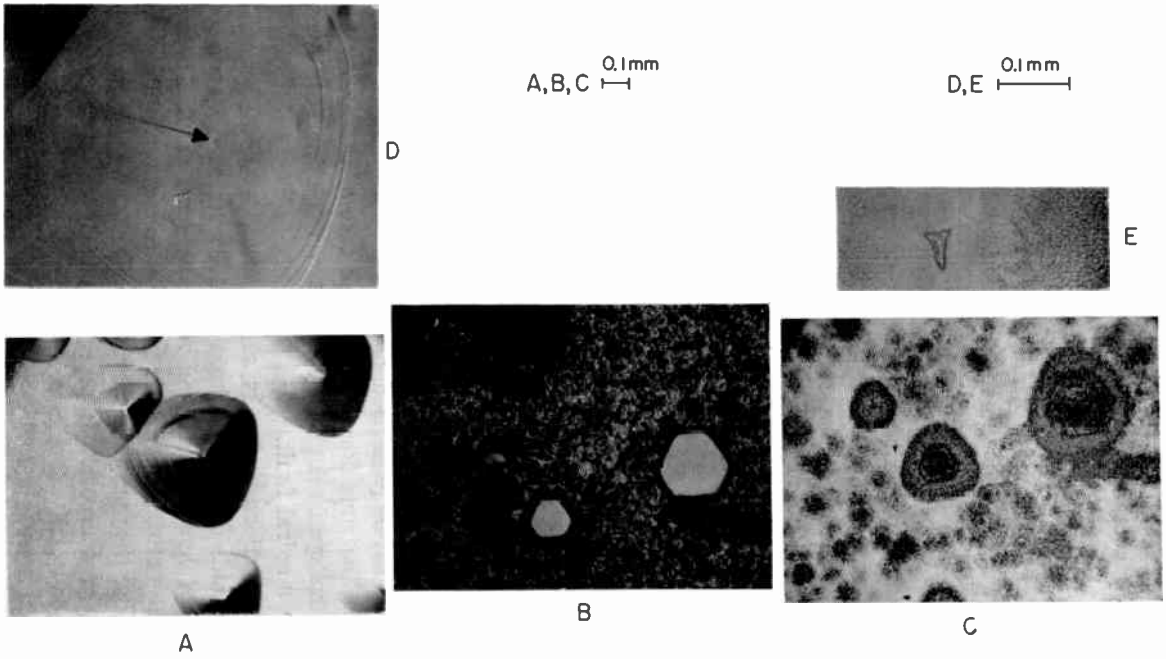

Fig. 9—Optical micrographs of the same area of a wafer of gallium arsenide on germanium (a) as grown, (b) after partial etch in warm 50/50 HCl–HNO_3, and (c) after second etch which almost entirely removes the GaAs layer. Original thickness of the GaAs layer about 1/2 mil.

this it is seen that a small residual triangle of gallium arsenide has not been completely removed although the entire surrounding area is free of gallium arsenide. This triangular section, shown enlarged in the micrograph above, would lie on a projection of the original fault line running down the face of the pyramid and is evidently associated with the appearance of this particular fault.

Accommodation of Strain Energy in the Composite Structure

How the strain energy resulting from lattice constant and thermal expansion coefficient mismatch is accommodated is one of the most important problems to be resolved for the growth of one material on another epitaxially. Attempts to define the location and density of dislocations in the composite layers have therefore been carried out. Linear arrays crossing at 60° angles can be seen* on the germanium substrate surface revealed by etching away the gallium arsenide layer (Figure 9c). Such arrays are strongly reminiscent of {111} <110> slip which can be revealed in mechanically deformed single crystals of germanium by etching, and which consists of linear arrays of edge dislocations.

If this surface of the germanium substrate is removed by a very short etch in CP4, a bright, shiny surface is obtained which contains etch pits in concentrations of about 1000 per cm^{-2}. This figure corresponds to the dislocation density observed for the starting substrate material before any gallium arsenide layer has been deposited. It is therefore concluded that, at least for distances of 5 microns or more from the interface, the dislocation density in the substrate is not affected perceptibly by the growth of a gallium arsenide layer on it. The dislocation density in the gallium arsenide layers has not yet been determined. This series of experiments therefore suggests that the strain energy is accommodated in a localized region at the interface between the gallium arsenide and the germanium, but is not accommodated entirely within the gallium arsenide layer, as might have been expected from the van der Merwe model.[1]

Chemical Purity and Electrical Properties of the Gallium Arsenide Deposit

Emission spectrographic analyses have been obtained of the gallium arsenide which deposits on the quartz support rod downstream from

* For porous layers such as 2/19/63a, (Figure 8), such structure is usually not observed in the substrate surface. Instead, following etching away of the gallium arsenide layer, the substrate has a mirror smooth appearance characteristic of that observed after an etch in gaseous HCl.

the substrate wafers. These reveal that germanium, the major contaminant, is present in concentrations of about 100 parts per million. Silicon is also usually detected in the 50 part per million range. Other impurities, including Fe, Al, Cu, Mg are present in concentrations of a few ppm. The germanium undoubtedly comes from the substrate, the silicon may arise by reaction of the hot gallium with the quartz boat. The other impurities are probably introduced by the HCl.

The gallium arsenide layers deposited on germanium substrates are always founds to be n-type with carrier concentrations of about 10^{17} per cm^3. This conductivity is interpreted as arising from the germanium and silicon impurities, both of which can serve as donors in gallium arsenide. Measurements of mobility and lifetime are in process of being carried out on these deposits and will be reported in a later publication.

Growth of Gallium Arsenide on Molybdenum and Tungsten Substrates

Molybdenum and tungsten are attractive substrate materials for use in epitaxial growth because of their low chemical reactivity. Both are reported to be stable in the presence of hydrogen and hydrogen chloride at temperatures near 700°C.[11] They are also available in the form of single crystals, and their electrical conductivity is only an order of magnitude less than that of silver.

Boules of tungsten and of molybdenum, grown by flame fusion, were oriented and sliced to yield substrates approximately 25 mils thick and having (111) surfaces. From Laue patterns it was observed that the slices were not single crystal. Rather, they contained several large grains similarly oriented.

To remove the work damage resulting from the slicing step, the substrates were first etched in a nitric–hydrofluoric acid etch, then in hydrofluoric acid alone. This process removes several mils from the wafers and leaves a bright, somewhat irregular surface in which the grain structure is clearly visible. Prior to deposition, substrates were heated in hydrogen to about 900°C in the etching zone for a few minutes. The oxides of tungsten and molybdenum are readily reduced under these conditions.[11] Hydrogen chloride was then admitted to the etching zone for three minutes. No reaction could be observed, however, and this step is probably unnecessary. Gallium arsenide depositions were then carried out as for the germanium substrates.

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[14] N. V. Sidgwick, *The Chemical Elements and their Compounds*, p. 1037 ff, London, Oxford University Press (1950).

The appearance of the gallium arsenide layer following growth on a molybdenum and on a tungsten substrate is shown in Figure 10, along with micrographs of the surfaces. Although the deposit on the molybdenum appears random, the grain structure of the tungsten substrate is manifest in the gallium arsenide layer and orientation of

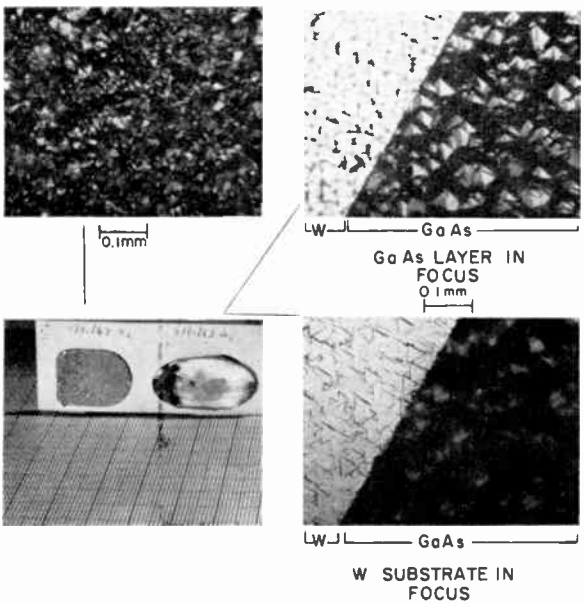

Fig. 10—Photographs and micrographs of GaAs layers on metal substrates: left, on molybdenum (111) substrate; right, on tungsten (111) substrate.

the layer is apparent. This observation is confirmed by the Laue patterns shown in Figures 11 and 12. For the deposit on molybdenum, the pattern shows only a few strong spots plus the Debye–Scherrer rings characteristic of polycrystalline gallium arsenide. The strong spots probably are due to the molybdenum substrate.

For the deposit on tungsten, however, the Laue pattern shows a high degree of orientation; in comparing the patterns shown in the center and at the bottom of Figure 12 it is seen that the Laue pattern for the deposit contains spots arranged on the same array as for a single-crystal gallium arsenide wafer. The spots are broken up, indicating that the layer consists of many single-crystal grains aligned in nearly the same manner, but the Debye–Scherrer rings characteristic of randomly oriented, polycrystalline material are absent. After obtaining the pattern shown in the center of Figure 12, it was observed that the gallium arsenide layer would chip off easily, revealing the tungsten

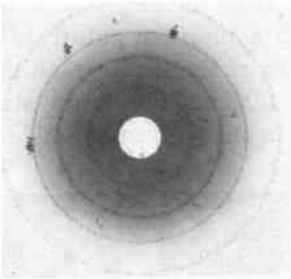

Fig. 11—Laue back reflection pattern of a gallium arsenide layer deposited on a molybdenum substrate.

substrate. A Laue pattern of the substrate was subsequently obtained and is shown at the top of Figure 12. Laue patterns of the gallium arsenide chip removed from the substrate were equivalent to that seen in the center of Figure 12. Note also the straight edges of the deposit from which the chip was removed (Figure 10).

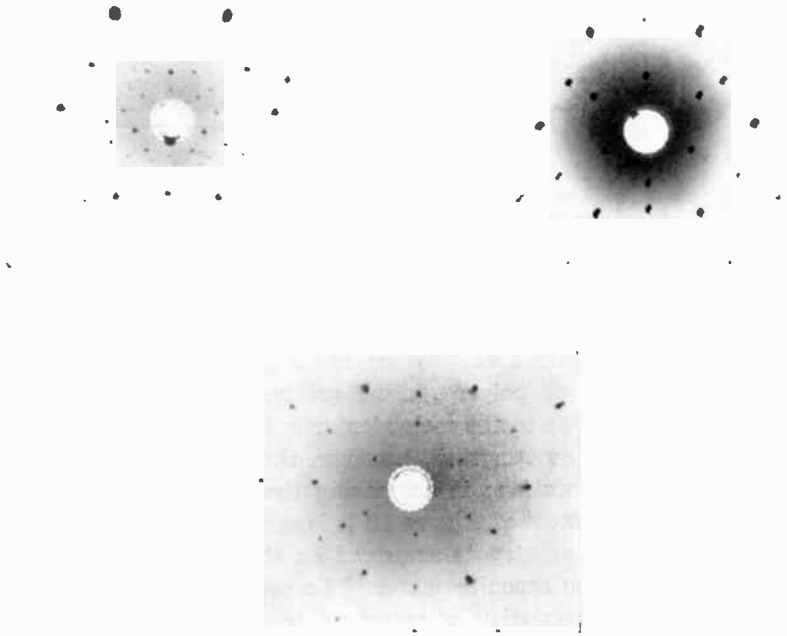

Fig. 12—Laue back reflection patterns of a gallium arsenide layer deposited on a tungsten substrate: (a) tungsten substrate after removal of the GaAs; (b) GaAs layer on the tungsten, prior to removal of the chip; (c) single-crystal wafer of GaAs for reference.

Unfortunately the gallium arsenide layer deposited on the tungsten substrate can easily be peeled off, e.g., by using a piece of Scotch tape. The deposit on molybdenum, however, is strongly adherent and is not easily removed mechanically. This behavior might have been anticipated by comparing the thermal expansion coefficients of molybdenum and tungsten with that for gallium arsenide. It may be that the difference in thermal coefficient of expansion for gallium arsenide and for tungsten is the cause of the breaking up of spots observed for the Laue pattern of this deposit; the gallium arsenide layer, as deposited at the growth temperature, may well have been single crystal. During the cooling of the layer, however, the gallium arsenide deposit may have broken up into nearly aligned crystallites to relieve the strain caused by the mismatch in expansion coefficients.

The orientation of the gallium arsenide layer on tungsten but not on molybdenum is very surprising. Tungsten and molybdenum have nearly the same lattice constant and are very similar in their chemical behavior. If one of these materials can serve as an orienting substrate for the growth of crystalline gallium arsenide layers, then the other should serve as well. This apparent discrepancy has yet to be resolved but may be due to the different chemical compositions formed at the tungsten or molybdenum surface upon exposure to arsenic prior to nucleation of the gallium arsenide deposit.

ACKNOWLEDGMENTS

For many helpful discussions and valuable suggestions the author is deeply indebted to N. Goldsmith of RCA Electronic Components and Devices, Somerville, N. J. Thanks are also due to G. W. Neighbor, W. C. Roth, and H. H. Whitaker for their help in obtaining x-ray and emission spectrographic analyses, and especially to J. G. White for permission to publish his results on the lattice constants and thermal expansion coefficients of germanium and gallium arsenide.

TRANSPORT OF GALLIUM ARSENIDE BY A CLOSE-SPACED TECHNIQUE

BY

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Summary—*Mirror-bright single-crystal layers of gallium arsenide have been grown on germanium substrates using close spacing between source and substrate. The results are consistent with the assumption that the transport agent is residual water vapor in the system which reacts with the source to form the volatile species Ga_2O. Typical growth rates of 1-3 mils/hr have been obtained. The parameters investigated were spacing between source and substrate, source temperature, substrate temperature, hydrogen flow rate, orientation of the source, and the efficiency of deposition. The log of the deposition rate has been found to be proportional to the temperature of the GaAs source, and an activation energy of 43 kcal/mole has been determined.*

INTRODUCTION

RECENTLY several systems for the vapor transport and epitaxial growth of III-V compounds have been described.[1-5] Both closed-end and opened-end apparatus is used. All of the systems have the following features in common: (1) a halide is used as the transporting agent, (2) a temperature gradient is maintained between the source and substrate, (3) the source and substrate are separated by an appreciable distance. This paper describes the growth of gallium

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[1] G. R. Antell and D. Effer, "Preparation of Crystals of InAs, InP, GaAs, and GaP by a Vapor Phase Reaction," *Jour. Electrochem. Soc.*, Vol. 106, No. 6, p. 509, June 1959.

[2] R. L. Newman and N. Goldsmith, "Vapor Growth of Gallium Arsenide," *Jour. Electrochem. Soc.*, Vol. 108, No. 12, p. 1127, Dec. 1961.

[3] V. J. Silvestri and V. J. Lyons, "Vapor Phase Equilibria for the Systems: GaAs-GaI_3-As_2 and Ga-GaI_3," *Jour. Electrochem. Soc.*, Vol. 109, No. 10, p. 963, Oct. 1962.

[4] N. Holonyak, Jr., D. C. Jillson, and S. F. Bevacqua, "Halogen Vapor Transport and Growth of Epitaxial Layers of Intermetallic Compounds and Compound Mixtures," *Proc. AIME* 1961 Conference on the Metallurgy of Semiconductor Materials, Los Angeles, Aug. 1961, Vol. 15, p. 49, John Wiley and Sons, Inc., New York, N. Y., 1962.

[5] R. R. Moest and B. R. Shupp, "Preparation of Epitaxial GaAs and GaP Films by Vapor Phase Reaction," *Jour. Electrochem. Soc.*, Vol. 109, No. 11, p. 1061, Nov. 1962.

arsenide on germanium substrates using a closed-spaced technique described by Nicoll,[6] without intentionally introducing a transport agent.

Experimental

Germanium was chosen as the substrate material because the coefficients of thermal expansion and the lattice constants for these two

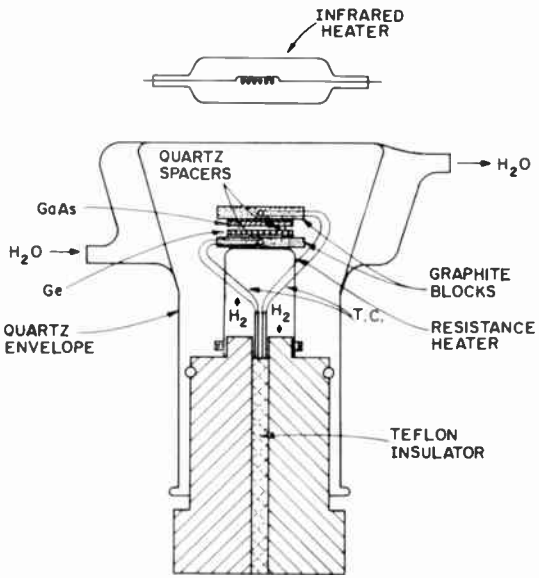

Fig. 1—Close-spaced apparatus.

semiconducting materials are within a few percent of each other. A modified alloying furnace, having a water-cooled quartz envelope as shown in Figure 1, was used. Heating from the bottom was accomplished by means of a platinum or molybdenum resistance heater. A graphite wafer containing a thermocouple was positioned on top of the resistance heater. The gallium arsenide source wafer was placed on top of this graphite. Quartz spacers were then used to separate the gallium arsenide source wafer from the germanium substrate. A second graphite wafer containing another thermocouple was placed on top of the germanium substrate. Independent infrared heating of the top graphite wafer was used to establish the desired temperature

[6] F. H. Nicoll, "The Use of Close Spacing in Chemical Transport Systems for Growing Epitaxial Layers of Semiconductors," *Jour. Electrochem. Soc.*, Vol. 110, No. 11, p. 1165, Nov. 1963.

gradient between source and substrate. The germanium substrates used were either |100| or |111| oriented n or p-type single-crystal slices. They were between 10 and 15 mils thick and were either mechanically polished, chemically polished or electropolished. The gallium arsenide source materials were single-crystal slices, n or p-type, and were also of either the |100| or |111| orientation. They were approximately 12 mils thick with chemically or mechanically polished surfaces. The hydrogen used was the purest available tank hydrogen further purified by use of a palladium diffuser. The graphite used was spectroscopic grade and vacuum-fired prior to use.

The various parameters investigated using the close-spaced technique for transporting gallium arsenide were: (1) spacing between source and substrate, (2) source temperature, (3) substrate temperature, (4) hydrogen flow rate, and (5) source orientation. The rate of transport of gallium arsenide was determined by measuring the thickness deposited on the germanium substrate per unit time. The thickness is determined by cleavage of the wafer and microscopic examination of its cross section. Observations on about 30 of these layers showed that they were very uniform in thickness, varying no more than about 1 μ almost out to the edge of the deposit.

Characteristics of the Epitaxial Layers

Mirror-bright, smooth epitaxial layers of gallium arsenide on |100| and on |111| germanium could be reproducibly obtained. Their Laue patterns were indistinguishable from those obtained on single-crystal wafers of GaAs. As grown, these layers were all doped n-type as determined by thermal probe measurements. The deposits were analyzed by emission spectrographic analysis and the major impurity was found to be germanium. Because tunneling characteristics were exhibited when alloy junctions were made in the epitaxial layers, it was concluded that the carrier concentration was in excess of 10^{17} cm^{-3}. The gallium arsenide deposits grew with the arsenic |111| surface outermost on |111| oriented germanium substrates as shown by darkening of the outer surface when stained with concentrated nitric acid. Photomicrographs of a typical layer are shown in Figures 2 and 3. When viewed in cross-section with a high-power microscope, the thickness could be measured since the gallium arsenide can easily be distinguished from the germanium due to the differences in color. Lineage lines oriented at 60° to one another show up on etching these deposits (Figure 4). These lines have been seen to extend about 4 μ into the germanium substrate. Typical thicknesses grown were one mil, although much thicker layers, about four mils, were used for the x-ray

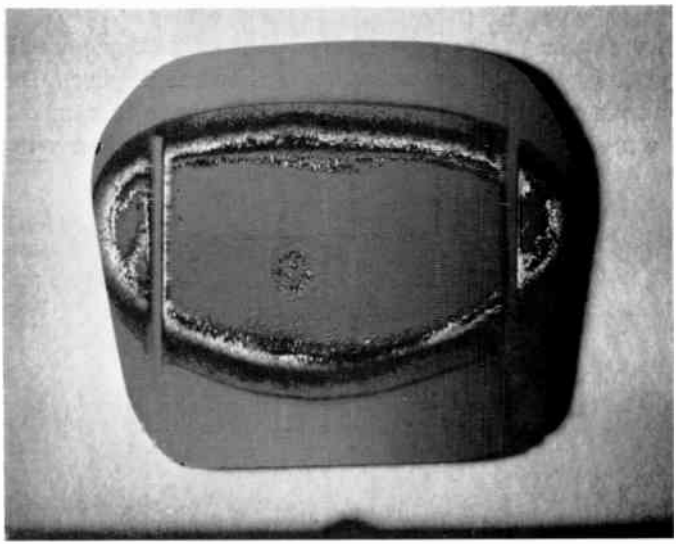

Fig. 2—Gallium arsenide layer deposited on germanium substrate.

studies. When the GaAs layers grown by the close-spaced technique were diffused, angle lapped, and stained, three regions showed up: (1) the gallium arsenide layer; (2) a very thin p-type region in the germanium, due to gallium diffusion; and (3) a thicker n-type region in the germanium, due to the faster arsenic diffusion.

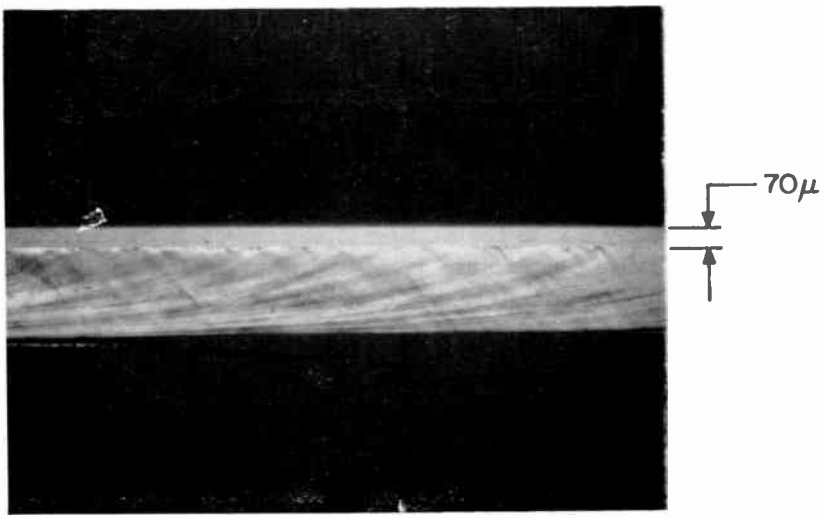

Fig. 3—Gallium arsenide layer on germanium viewed edgewise.

Growth Parameters

The variation of the rate of transport of gallium arsenide with spacing between source and substrate is shown in Figure 5 for source temperatures of 825° and 900°C. The substrate temperature for both curves was 725°C. The rate of transport rises with spacing up to

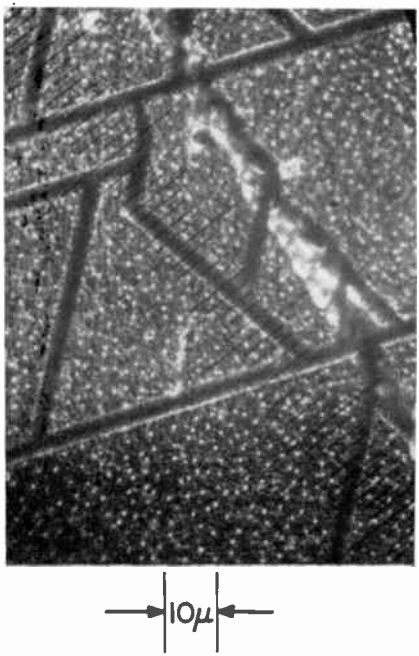

Fig. 4—Lineage lines on gallium arsenide deposit.

about six mils and thereafter remains essentially constant. This increase in the rate of transport with increasing spacing at very close spacing is possibly due to the heating of the substrate by the source wafer, the effective temperature gradient being therefore very much smaller than the temperature gradient measured between the two graphite discs. At a spacing of six mils the measured temperature gradient probably appears mostly across the gap and the rate of deposition thereafter remains constant with increased spacing.

Figure 6 shows the log of the deposition rate plotted against the temperature of the source material for a spacing of eight mils and a substrate temperature of 725°C. The resulting activation energy is 43 kcal/mole.

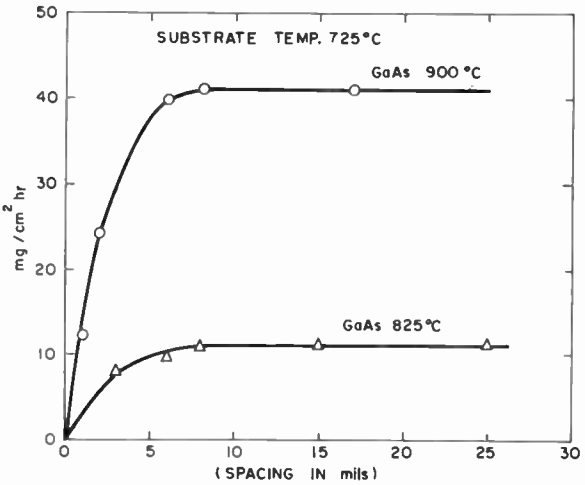

Fig. 5—Rate of transport versus spacing.

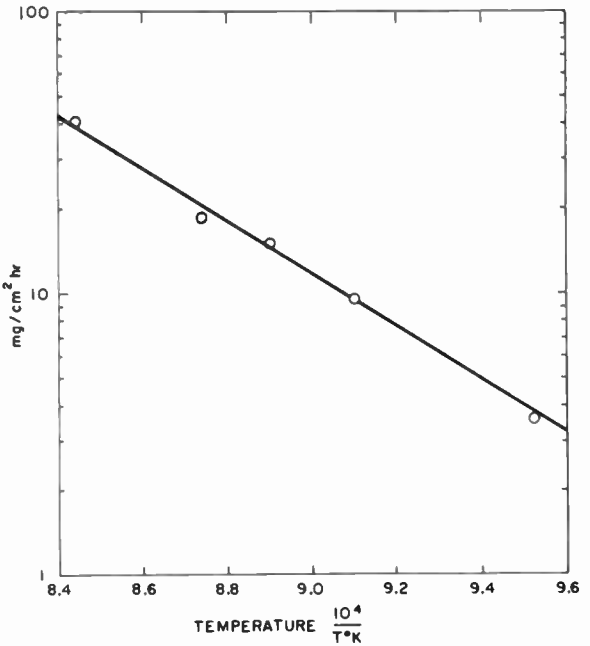

Fig. 6—Log rate of transport versus temperature.

The substrate temperature was of major importance only insofar as the appearance and single crystallinity of the layer was concerned. To obtain mirror-bright single-crystal layers, optimum temperatures were 725° to 775°C. Below these temperatures the layers were polycrystalline with a matte texture, while above this temperature the layers exhibited numerous hillocks and were usually quite rough when viewed under high power. The rate data presented were obtained at a substrate temperature of 725°C. It was also determined by a separate experiment that the amount of transport taking place at a source temperature of 725°C and a substrate temperature of 675°C was very small, less than 0.1 mg cm^{-2} hr^{-1}. This indicates that under the usual transport conditions almost no GaAs leaves the substrate after being deposited.

When the amount of hydrogen flowing in the system was greater than 4 cm^3 min^{-1}, the transport rate decreased rapidly with increasing hydrogen flow rates. Below 4 cm^3 min^{-1}, however, the transport rate was observed to be independent of the hydrogen flow rate. The rate data were therefore obtained at hydrogen rates smaller than 4 cm^3 min^{-1}.

The orientation of the source wafer influenced the transport rate. When the [111] As surface faced the Ge substrate, the transport was much more rapid than when the [111] Ga face faced the Ge wafer. The former gave rough-looking surfaces on the deposits for either [111] or [100] substrates, while the latter gave much smoother surfaces. The [100] oriented source surface, however, resulted in a uniformly smooth source surface as well as a smooth substrate surface, and the same source wafer could be used many times without further treatment. Both Ga and As [111] surfaces exhibited very deep pits and were very rough after use as a source.

The efficiency of the mass transport process, namely the ratio of the weight gained by the germanium to the weight lost by the gallium arsenide, ranged between 90% and 98%. Typical mass-transport efficiencies for open-tube flow systems are a few per cent.

Discussion

Mass spectrometric evidence for the existence of the volatile vapor species Ga_2O has been reported.[7] The measured high transport efficiencies indicate that the nonvolatile species Ga_2O_3 is not formed in

[7] W. A. Chupka, J. Berkowitz, C. F. Giese, and M. G. Inghram, "Thermodynamic Studies of Some Gaseous Metallic Carbides," *Jour. Phys. Chem.*, Vol. 62, No. 5, p. 611, May 1958.

the transport reaction with low concentrations of water vapor. This apparent failure of the stable Ga_2O_3 condensed phase to form has also been observed[8] for the growth of GaAs crystals under various partial pressures of oxygen.

Frosch and Thurmond[9] have reported that the mass transport of gallium arsenide in a wide-spaced growth apparatus increases with increasing water vapor content of the carrier gas. Gottlieb[10] has confirmed these results for the close-spaced system. Cochran and Foster[11] have calculated the equilibrium constants as a function of temperature for several reactions which produce Ga_2O. For the reaction

$$2\,Ga_{(l)} + H_2O_{(v)} \rightleftharpoons Ga_2O_{(v)} + H_{2(v)} \qquad (1)$$

they find a $\Delta H°_{298}$ of 38.1 kcal. The values of the equilibrium constants are not extremely large and they indicate that the forward reaction is favored at high temperature, while the reverse reaction is favored at the lower temperature. The fact that water vapor acts as the transporting agent in this apparatus is consistent with the fact that at fast hydrogen-flow rates the rate of transport decreases very rapidly. Since water vapor was not deliberately added to the hydrogen in these experiments, the source of the water vapor is probably (1) the reduction of the oxide layer on the germanium substrate with hydrogen, (2) adsorbed water on the quartz walls, and (3) absorbed water in the graphite wafers. The concentration of water vapor must be low so that at fast flow rates the water vapor in the apparatus would be rapidly removed from the system, resulting in a decreased transport rate.

A hydrogen ambient was not essential for the transport reaction since gallium arsenide was also transported in a vacuum of 10^{-6} mm Hg using this close-spaced technique. Under vacuum conditions, the transport rate dropped by more than a factor of 10, and the nature

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[8] J. F. Woods and N. G. Ainslie, "Role of Oxygen in Reducing Silicon Contamination of GaAs during Crystal Growth," *Jour. Appl. Phys.*, Vol. 34, No. 5, p. 1469, May 1963.

[9] C. J. Frosch and C. D. Thurmond, "Vapor Growth of Single Crystals of GaP and GaAs by a Ga_2O Vapor Transport Mechanism," Electrochem. Soc. Meeting, Boston, Sept. 1962.

[10] G. E. Gottlieb and J. F. Corboy, "Epitaxial Growth of GaAs Using Water Vapor," *RCA Review*, Vol. 24, No. 4, p. 585, Dec. 1963.

[11] C. N. Cochran and L. M. Foster, "Vapor Pressure of Gallium, Stability of Gallium Suboxide Vapor, and Equilibria of Some Reactions Producing Gallium Suboxide Vapor," *Jour. Electrochem. Soc.*, Vol. 109, No. 2, p. 144, Feb. 1962.

of the deposit was very different. The material did not alloy properly and resulted in poor wetting and high-resistance contacts. A large quantity of free gallium remained on the source surface after use.

Richman[12] has measured the vapor pressure of arsenic in equilibrium with solid gallium arsenide as a function of temperature. At the temperatures used in our experiments the vapor pressure of Ga_2O above solid Ga_2O is about 100 times greater than the equilibrium vapor pressure of As above GaAs. The low vapor pressure of liquid gallium, therefore, no longer limits its removal from the gallium arsenide surface, thus permitting the arsenic vapor pressure to increase toward its equilibrium vapor pressure. The arsenic is transported to the substrate surface where it reacts with gallium to form gallium arsenide.

The mechanism of recycling the water vapor from substrate to source must be a fast process such as convection. If diffusion is controlling the rate, the rate-versus-spacing curves would not saturate at the larger spacings, and a smaller activation energy would be required.

The most probable reaction for the results reported is

$$2\,GaAs_{(s)} + H_2O_{(v)} \rightleftharpoons Ga_2O_{(v)} + As_{2(v)} + H_{2(v)}. \qquad (2)$$

Weiser[13] has reported that the arsenic dimer is the predominant species in the vapor phase at the temperatures used for transport.

Conclusions

Epitaxial layers of gallium arsenide on germanium substrates were prepared using a close-spaced technique. The transporting agent was water vapor which reacts with the source to form the volatile species Ga_2O. A hydrogen ambient is not necessary for the transport reaction since transport of gallium arsenide was found to take place in vacuum. The equilibrium

$$Ga_{(s)} + H_2O_{(v)} \rightleftharpoons Ga_2O_{(v)} + H_{2(v)}$$

controlling the transport process is consistent with the results obtained. The major impurity found in these deposits was germanium. An activation energy of 43 kcal/mole has been determined.

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[12] D. Richman, "Dissociation Pressures of GaAs, GaP and InP and the Nature of III-V Melts," *Jour. Phys. Chem. Solids*, Vol. 24, No. 9, p. 1131, Sept. 1963.

[13] W. Weiser, "Thermodynamic Properties," from *Compound Semiconductors*, ed. by R. K. Willardson and H. L. Goering, Reinhold Publishing Corp., Vol. 1, p. 480, 1962.

ACKNOWLEDGMENTS

Thanks are due to F. H. Nicoll for his assistance and many helpful discussions regarding this work, and to Mrs. E. Moonan for fabrication and measurements of the alloyed junctions. Thanks are also due to G. W. Neighbor, W. C. Roth and H. H. Whitaker for x-ray and emission spectrographic analyses performed on the layers, to J. G. White for determination of lattice constant and thermal coefficients of expansion, and to D. Richman, J. Amick, and H. Johnson for critically reading the manuscript.

APPENDIX

A. Transport of Germanium

Lever and Jona[11] have recently reported the epitaxial growth of germanium using water vapor as the transporting agent and have obtained growth rates of .2μ/hr at 828°C. Results obtained using the close-space technique with no intentionally added water vapor are very similar to those reported by Lever and Jona. The source material used was (111) oriented single-crystal mechanically polished germanium wafers 20 mils thick at a temperature of 805°C. Substrates used were either (111) oriented single-crystal mechanically polished germanium wafers, also 20 mils thick, or (100) oriented GaAs single-crystal mechanically polished wafers at a temperature of 770°C. Growth rates of 4-6 μ/hr have been obtained and the resulting germanium deposit was mirror smooth and was determined to be single crystalline by Laue patterns on both types of substrates. The transporting species is GeO and the equilibrium $Ge_{(s)} + H_2O_{(g)} \rightleftharpoons GeO_{(g)} + H_{2(g)}$ controlling the transport from source to substrate is in agreement with the results of Lever and Jona.

B. Transport of InAs and InP

Indium is chemically very similar to gallium, and single-crystal layers of both InAs and InP on gallium arsenide substrates using the close-spaced technique with no added water vapor were also successfully grown. Polycrystalline InAs and InP were used as the source material and (100) and ($\bar{1}\bar{1}\bar{1}$) oriented mechanically polished gallium arsenide wafers were used as substrates. The optimum temperature for the polycrystalline InAs source was determined to be 825°C while for InP it was 725°C. Substrate temperatures 50° lower were used. Using these conditions growth rates of InAs were ~ 2 mils/hr while

[11] R. F. Lever and F. Jona, "Epitaxial Growth of Germanium Using Water Vapor," *Jour. Appl. Phys.*, Vol. 34, p. 3139, 1963.

for InP growth rates were ≈ 1 mil/hr. It was observed that at temperatures much higher than 825°C and 725°C, the dissociation pressures of As and P, respectively, become too high, resulting in a large excess of free indium on the source wafer, and very little transport to the substrate occurred. The transporting species is most likely In_2O and an equilibrium similar to those proposed for germanium and gallium arsenide is probably involved.

EPITAXIAL GROWTH OF GaAs USING WATER VAPOR

By

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Princeton, N. J.

Summary—*GaAs can be transported in a close-spaced system with water vapor as the transporting agent. The rate of growth can be controlled by varying the concentration of H_2O entering the system. The transport is assumed to proceed via the following equation: $2\,GaAs + H_2O \rightleftharpoons Ga_2O + H_2 + As_2$. From a plot of 1/T versus log rate, an activation energy of 49 kcal/mole was calculated for the above reaction. The rate of transport is found to be proportional to the square root of the water vapor pressure (concentration) over a wide range of vapor pressures. The conditions of transport therefore approach thermodynamic equilibrium. If internal sources of water vapor are eliminated, and no water vapor is admitted to the system, less than 1 milligram of GaAs/hr/cm² is transported. However, a growth rate of about 13 mg/hr/cm² (1 mil thickness) is obtained under normal operating conditions. The effects of temperature, spacing and flow rate on the rate of transport were also investigated.*

Introduction

F. H. NICOLL[1] and P. Robinson[2] have found that epitaxial films of GaAs can be deposited with high efficiency by vapor-phase transport in a flow of hydrogen. The most interesting feature of the apparatus used by Nicoll and Robinson is the close spacing (0.010 inch) between the GaAs source and the substrate. The mechanism of the transport reaction occurring in the close-spaced system is described in the present paper.

Procedure

The apparatus originally used by Nicoll and by Robinson was modified as shown in Figure 1 so that controlled amounts of water vapor, used as a source of oxygen, could be introduced into the system via the hydrogen stream. The relationship between the water vapor concentration and the amount of GaAs transported per unit time (weight loss of GaAs source) was then studied (Figure 2).

[1] F. H. Nicoll, "The Use of Close Spacing in Chemical Transport Systems for Growing Epitaxial Layers of Semiconductors," *Jour. Electrochem. Soc.*, Vol. 110, No. 11, p. 1165, Nov. 1963.

[2] P. Robinson, "Transport of Gallium Arsenide by a Close-Spaced Technique," *RCA Review*, Vol. 24, No. 4, p. 574, Dec. 1963.

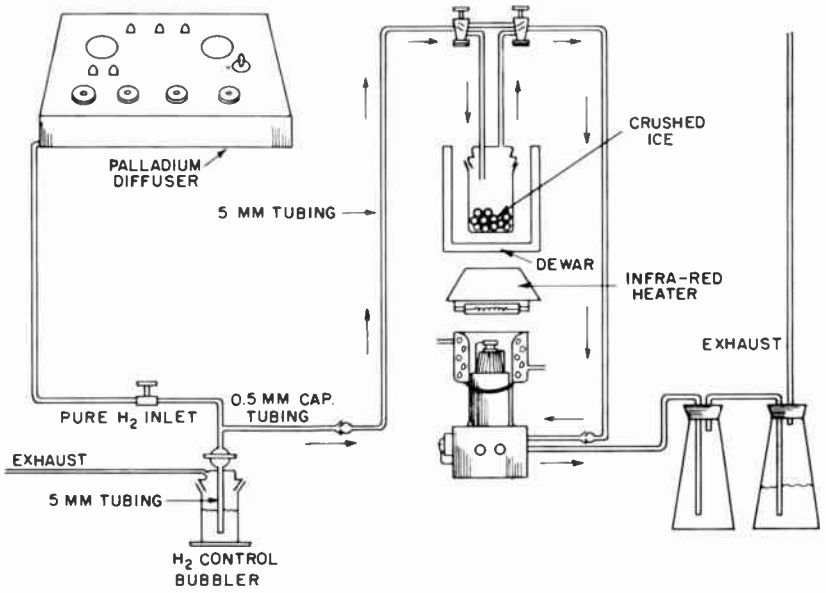

Fig. 1—Close-spaced system and associated water-vapor control apparatus.

Hydrogen was purified by use of a palladium diffuser. The amount of water vapor admitted was controlled by passing the pure hydrogen over ice, maintained by a salt–ice bath, at a sub-zero temperature. The dew point of the mixture emanating from the system was checked periodically. The dew point of the gas mixture was always found to

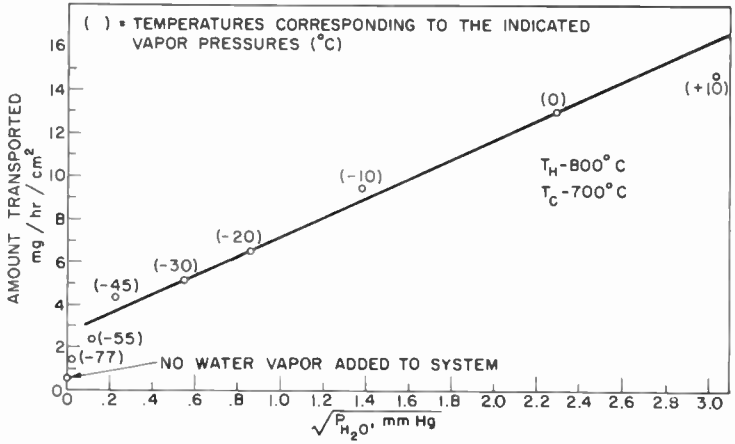

Fig. 2—Amount of GaAs transported as a function of water-vapor pressure.

be the temperature of the ice–salt mixture, and was independent of hydrogen flow rate. The gas flow rates used in this study are extremely small, and difficult to monitor with a flow meter; therefore flow rates were measured by counting the number of bubbles per minute passing through a glycerine trap. The flow rate was then determined by the displacement of water from a calibrated volume.

The temperatures of the source wafer (GaAs) and of the substrate wafer (Ge) were controlled by separate heaters. The source heater is a molybdenum strip below the wafer. The substrate heater is an infrared lamp mounted above the wafer, and external to the apparatus. To insure an equal temperature over the entire wafer, heavy molybdenum discs were placed between the wafers and their respective heaters. Quartz discs have also been used for this purpose. Any material of sufficient thermal conductivity is satisfactory if it is not porous and does not react with arsenic. Porous materials such as carbon absorb water vapor and reintroduce it into the system in an uncontrolled manner. Temperature control is facilitated by thermocouples placed in small holes in the molybdenum discs. To ascertain the reliability of thermocouple measurements, checks were made with "Tempil" pellets, certified to melt at 816°C ± 8°, placed on both the GaAs wafer and the molybdenum disc. Temperatures of the thermocouples agreed with the calibrated melting point of the pellets, indicating that the GaAs wafer and the molybdenum disc are in thermal equilibrium, and that the thermocouple reading is an accurate measure of the actual disc and wafer temperature.

Single-crystal GaAs wafers having (100) surfaces were used as source material. These wafers were optically polished on one side and etched in H_2O-H_2O_2-H_2SO_4 in the ratio 1:1:5 prior to use. The Ge substrate wafers had (111) faces; both mechanically polished and unpolished wafers were used. Some of the mechanically polished wafers were further polished with a vapor-phase HCl etch.[3]

RESULTS

The layers produced by the close-spaced system via water-vapor transport are single crystals, as determined by Laue patterns. Mirror-smooth layers, with occasional triangular growth patterns characteristic of (111) stacking faults, are normally obtained. A typical wafer is shown in Figure 3. The grown layers were tested with a concentrated nitric acid etch to determine whether the As or Ga face is

[3] J. Amick, E. A. Roth, and H. Gossenberger, "The Etching of Germanium Substrates in Gaseous Hydrogen Chloride," *RCA Review*, Vol. 24, No. 4, p. 473, Dec. 1963.

uppermost. A wide range of layers, varying from mirror finish to dull matte finish, were all found to give a black stain, and it is therefore deduced that they have the As surface outermost.

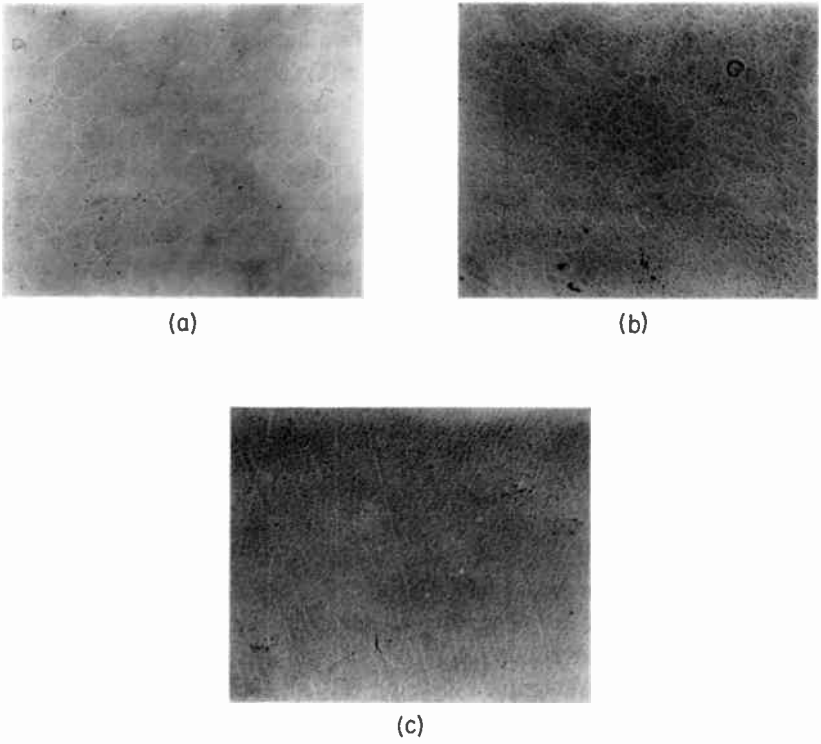

Fig. 3—Some typical GaAs surfaces obtained by water-vapor transport (all photos taken at 37×): (a) and (b) show mechanically polished (111) Ge substrates grown at 700°C; (c) shows mechanically polished and HCl vapor-etched (111) Ge substrate grown at 710°C.

The amount of GaAs transported as a function of temperature, with a constant water-vapor concentration and a constant temperature difference (50°C) between source and substrate, is shown in Figure 4; it approaches the expected logarithmic behavior. Using the flat part of the curve, an activation energy of 49 kcal/mole is obtained. The suitable temperature ranges were found to be 800°C ± 50° for the source and 700°C ± 50° for the substrate, with a temperature difference between source and substrate of 50°-100°C. Water-vapor bath temperatures from 0° to —10°C were found to be satisfactory. These conditions gave growth rates ranging from 0.5 to 2 mils per hour.

The effect of the water-vapor concentration on the amount transported is illustrated by the fact that when pure palladium-diffused hydrogen sans water vapor is used, less than one milligram/hour/cm^2 (0.05 mil/hour) is transported at 800°C (Figure 2). It was also found that when a constant amount of water vapor is continually added to the system, the flow rate of the hydrogen carrier can be varied by

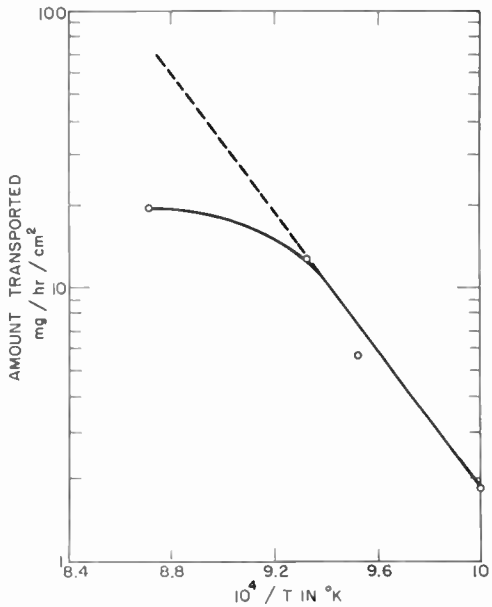

Fig. 4—Temperature dependence of the transport rate plotted as the amount of GaAs transported versus $10^4/T$.

an order of magnitude without substantially affecting the crystallinity of the grown layer or the amount of material transported. This is in direct contrast to the results of Robinson,[2] who finds that the hydrogen flow rate is extremely critical. This apparent discrepancy is due to the fact that the water vapor in Robinson's system comes from the carbon discs, instead of being introduced via the hydrogen stream. At high flow rates, the available water vapor is swept out of the system, and therefore the amount of GaAs transported decreases. In the apparatus used here, the ratio of H_2O to H_2 remains constant, and therefore the amount of GaAs transported remains relatively constant. This is shown in Figure 5. Even though the amount of GaAs transported does not vary significantly with the flow of hydrogen carrier gas, the deposition efficiency does vary considerably with flow. As

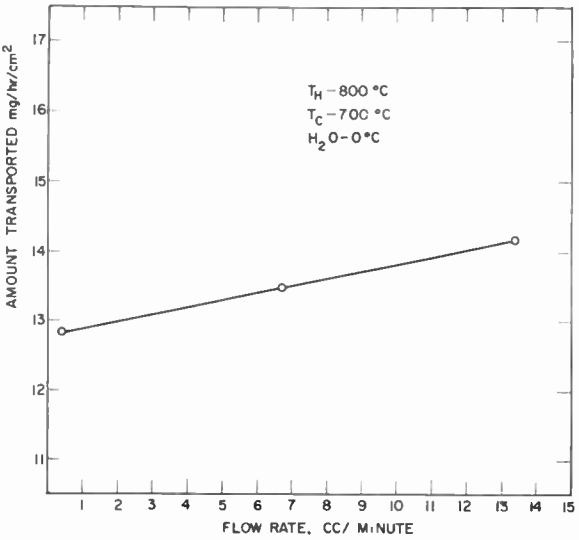

Fig. 5—Dependence of the amount of GaAs transported on flow rate.

shown in Figure 6, the deposition efficiency (gain in weight of substrate/loss in weight of source) increases with an increase in flow rate.

The effect of spacing between the GaAs and Ge wafers was also investigated. The amount of GaAs transported decreased as the spacing was increased, as shown in Figure 7.

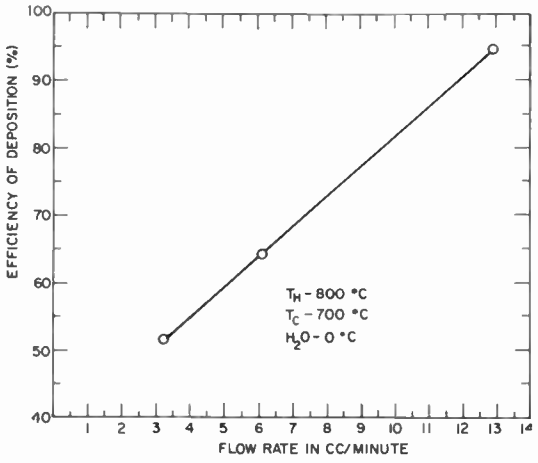

Fig. 6—Variation of deposition efficiency with flow rate.

The surface preparation of the substrate is of critical importance for the growth of satisfactory epitaxial layers. Layers have been grown on mechanically polished, chemically polished, unpolished, and vapor-phase etched Ge (111) wafers. The substrate defects usually manifested themselves in the grown layers. For this reason the smoothest, most optically perfect layers were obtained on the cleanest

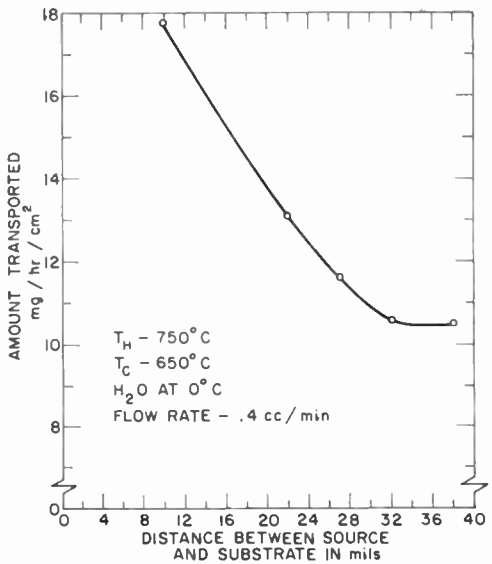

Fig. 7—Amount of GaAs transported as a function of spacing.

and smoothest substrate wafers, namely, the chemically polished and vapor-phase etched wafers. Mechanically polished wafers have surface scratches which produce irregularities in the grown layers. Smooth layers have been grown on this type of substrate, but with much poorer reproducibility. Most of the wafers were etched in HCl gas at about 850°C, using a technique similar to that described by Amick.[3]

Discussion

The actual transport is assumed to proceed via the following reaction:

$$2\,GaAs + H_2O \rightleftharpoons Ga_2O + H_2 + As_2. \qquad (1)$$

The Ga_2O is assumed to be the transporting species; this is in agreement with thermodynamic data and the observed vapor pressure of

Ga_2O relative to Ga_2O_3.[4] Vapor pressure measurements by Frosch and Thurmond[5] also indicate that Ga_2O is the volatile species. The use of Ga_2O as the transport agent for the synthesis of GaP has also been reported.[6]

Equation (1) states that an equilibrium exists between GaAs and Ga_2O. The direction of the equilibrium is determined by the temperature variation of K_p, the reaction proceeding from left to right at high temperatures (T_H) and right to left at low temperatures (T_L). With this equation, a yield of 100 per cent can be anticipated, since there is no undesired side product formed by the reaction.*

The amount of GaAs that should be transported by one milligram of H_2O, assuming just one Ga_2O molecule formed per water molecule, can be calculated from Equation (1). The amount of H_2O introduced into the close-spaced system during the course of an experiment can also be calculated, and from this can be obtained the amount of GaAs transported per water molecule introduced. The assumption made in this calculation is that all of the water vapor entering the system enters the reaction zone and combines with the GaAs. This calculation shows that several gallium arsenide molecules are transported for each water molecule introduced. This probably explains why considerable amounts of GaAs can be transported in "pure" hydrogen, since even

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[4] S. Antkiw and V. H. Dibeler, "Mass Spectrum of Gallium Vapor," *Jour. Chem. Phys.*, Vol. 21, No. 10, p. 1890, Oct. 1953.

[5] C. J. Frosch and C. D. Thurmond, "Vapor Pressure Measurements of Ga-Ga_2O_3 Mixtures," *Jour. Phys. Chem.*, Vol. 66, p. 877, May 1962.

[6] M. Gershenzon and R. M. Mikulyak, "Vapor Phase Preparation of Gallium Phosphide Crystals," *Jour. Electrochem. Soc.*, Vol. 108, No. 6, p. 548, June 1961.

* The alternative reaction scheme, based on the well-known disproportionation of Ga_2O to Ga_2O_3 and Ga,[7] can be ruled out.

$$2\,GaAs + H_2O \rightarrow Ga_2O - H_2 + As_2$$

$$3\,Ga_2O + 2\,As_2 \rightarrow 4\,GaAs + Ga_2O_3$$

Because 1/3 of the Ga present forms Ga_2O_3 instead of GaAs, the theoretical limit on the yield is 67 per cent. To obtain a yield of about 98 per cent by this series of reactions, it would be necessary to reduce the Ga_2O_3 with hydrogen back to Ga_2O or Ga. This reaction does not take place. The latter was attempted unsuccessfully by many workers. As with the findings of other workers,[8] no Ga_2O_3 has been observed in the course of this study.

[7] D. A. Brukl, "The Oxides of Gallium," *Z. Anor., and Allgem. Chem.*, Vol. 203, p. 23, 1932.

[8] C. N. Cochran and L. M. Foster, "Vapor Pressure of Gallium, Stability of Gallium Suboxide Vapor, and Equilibria of Some Reactions Producing Gallium Suboxide Vapor," *Jour. Electrochem. Soc.*, Vol. 109, No. 2, p. 144, Feb. 1962. See also J. F. Woods and N. G. Ainslie, "Role of Oxygen in Reducing Silicon Contamination of GaAs during Crystal Growth," *Jour. Appl. Phys.*, Vol. 34, No. 5, p. 1469, May 1963.

palladium-diffused hydrogen contains small amounts of water vapor as an impurity. Naturally, efficient use of transport agents is an inherent characteristic of sealed systems; however, it is unusual in flow-type systems and appears to be peculiar to the close-spaced system. The high efficiency of the transport in this apparatus clearly comes from the approximation to a sealed system which retains all reaction species. In large-flow systems, also, reactions of 100 per cent yield can be utilized. However, the efficient use of the transport agent cannot be duplicated, and the deposition efficiency is usually of the order of a few per cent. Therefore, the combination of a 100 per cent yield reaction, multiple use of the transporting agent, and a high deposition efficiency in a flow system are unique to the close-spaced system, and make it possible to transport relatively large amounts of material to the substrate with extremely small amounts of a transporting agent.

Figure 2 shows that the rate of transport is proportional to the square root of the water-vapor pressure. This is the relationship expected from Equation (1), and it is valid except for very low concentrations over the entire range studied. This observation implies that conditions in the reaction zone are always very near equilibrium during deposition.

Figure 7 shows a decrease in the amount of GaAs transported as the spacing between the source and the substrate is increased. This is in contrast to the results of Robinson,[2] who found an increase. It is interesting that the amount transported with a very large spacing approaches the same limit for both methods.

Most of the layers were grown on n-type Ge, and the deposits were predominantly n type. Doping of the grown layers by Ge originating from the substrate has been encountered frequently. Even when a heavily Zn-doped GaAs wafer was used as a source, n-type layers were produced. The same effect was observed when a Zn-doped source was used for growth on GaAs substrates. This result is probably explained by the low vapor pressure of ZnO which forms at the source and can not be transported to the substrate. The low vapor pressures of the common p-type dopant oxides makes the growth of p-type layers difficult. Te has been found to work effectively in this system as an n-type dopant.

Surfaces of deposits produced under the wide range of conditions investigated showed, when etched with concentrated nitric acid, the characteristics of the arsenic face, $\bar{1}\bar{1}\bar{1}$. This indicates that the nucleation process is a function of either the transport reaction utilized or

of GaAs-Ge growth, and is not influenced by differences in transport rate or temperature in the range studied.

There are indications that the procedure used to bring the system to the reaction temperatures can be important. The mode of heating arbitrarily can be one of the following:

(1) Hot and cold zone heated at same rate until the cold zone growth temperature (T_c) is reached.

(2) Hot zone is hotter than cold zone during the heating cycle.

(3) Cold zone is hotter than hot zone during the heating cycle, until T_c is reached.

If H_2O is present there are two reasons why the heating procedure can be of importance. First, Ge can be transported by oxygen as GeO, and second, GaAs is transported by O_2 at temperatures as low as 600°C. Therefore, condition (2) will tend to transport GaAs at temperatures considerably below the normal growth temperatures. The low substrate temperature would result in a low surface mobility, and therefore the GaAs grown under these conditions would tend to be polycrystalline. Since this is the initial epitaxial layer, any material grown on top of this would also tend to be polycrystalline. If condition (3) prevails, Ge could be transported from the substrate onto the GaAs source, so that when the source reaches the hot-zone growth temperature (T_H) Ge instead of GaAs is transported initially.

In view of the above, one might expect that the most desirable heating cycle is (1)—heating both zones at the same rate. However, this is exceedingly difficult to do. Also, condition (3) could actually be the most beneficial if the Ge removed from the substrate can be prevented from depositing on the GaAs source. Such conditions would aid in cleaning the Ge substrate without contaminating the GaAs source.

The system can also be brought to reaction temperatures under a flow of pure hydrogen. Since water vapor is not introduced until the growth temperatures are attained, the processes occurring during the heating cycle are mainly evaporation rather than transport. Under such circumstances the differences between conditions (1), (2), and (3) tend to become less pronounced. However, it was found that there was little if any difference visually or electrically between layers grown with pure hydrogen present during the heating cycle, and hydrogen–water during the heating cycle. It was also found that the presence or absence of H_2O during the heating cycle had no effect on the amounts of GaAs transported. This suggests that equilibrium is reached quickly in spite of the very slow flow rate.

Conclusion

It has been found that GaAs can be transported in a close-spaced system using water vapor. The rate of growth is found to be proportional to the square root of the water-vapor concentration. Smooth, mirror-like layers are normally obtained with this apparatus. A high deposition efficiency is obtained because of the close spacing. The deliberate addition of water vapor to the hydrogen stream makes the transport rate almost independent of the hydrogen flow rate.

Acknowledgment

The authors wish to acknowledge the advice and encouragement of P. G. Herkart, and useful discussions with F. H. Nicoll and P. Robinson. The authors are grateful to W. Roth and G. Neighbor for Laue back-reflection photographs, and to H. Bertram for providing the GaAs source wafers. Thanks are also due to D. Richman for a critical reading of the manuscript.

GAS PHASE EQUILIBRIA IN THE SYSTEM GaAs–I_2

By

D. Richman

Summary—The molecular species present in the gas phase for the system GaAs–I_2 have been determined by an absorption spectroscopic technique. The chemical reaction responsible for the transport of GaAs has been established to be

$$4GaAs_{(s)} + 2GaI_{3(g)} \rightleftharpoons 6GaI_{(g)} + As_{4(g)}.$$

Values of the equilibrium constant for this reaction as a function of temperature were calculated from the observed temperature dependence of the concentration of GaI in the gas phase.

Introduction

THE GROWTH of elemental and compound semiconductors by means of vapor phase transport is now a well established and widely applied technique. In order to fully utilize the advantages of this method of crystal growth, it is necessary to have as complete knowledge as possible of the chemical reactions and the mechanisms of growth. The chemical species present in the vapor phase and the equilibrium between them are of primary importance. In a previous publication[1] a method for identifying the species present and measuring their concentrations was described.

GaAs, because of its technological importance, has been the compound semiconductor most widely grown by the vapor transport technique. The chemical system commonly used consists of GaAs and a halogen, either chlorine or iodine. Lyons and Silvestri[2] have reported on the equilibria in the GaAs—I_2 systems as determined from total pressure measurements. In this paper, the results of a spectroscopic investigation of the gas phase in the GaAs—I_2 system are presented and compared with those of Lyons and Silvestri.

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[1] R. Nitsche and D. Richman, "Crystal Growth by Chemical Transport Reactions. II. Equilibrium Measurements in the System Cadmium Sulfide-Iodide," *Zeit. fur Elektrochemie*, Vol. 66, p. 709, 1962.

[2] V. J. Lyons and V. J. Silvestri, "Vapor-Phase Equilibriums for the Systems: GaAs-GaI_x-As_y and Ga-GaI_x," *Jour. Electrochem. Soc.*, Vol. 109, p. 963, Oct. 1962.

EXPERIMENTAL

The study of the GaAs—I_2 system is a straightforward extension of the work[1] previously carried out on the CdS—I_2 systems. There the concentration of molecules in the gas phase was determined by measuring the total pressure of CdS—I_2 mixtures enclosed in a known volume. The species present in the gas phase were identified by ultraviolet and visible absorption spectroscopy. In principle either measurement, together with the appropriate assumptions, should be sufficient to determine the equilibria in the system investigated. In the work reported here only the spectroscopic experiments were carried out.

A detailed exposition of the apparatus and experimental procedure has been given previously.[1] In addition to the study of the GaAs—I_2 system, the following related systems were studied in order to establish the absorption spectra of the various species which might have been present; Ga_{excess}—I_2; Ga—$I_{2\ excess}$; As; As—I_2; and pure GaAs.

All of the above systems were found to be transparent in the region near 12,000Å, so all were normalized to zero optical density at that wavelength. The investigation covered the spectral region from 12,000Å down to 2,500Å, at which wavelength the optical densities of the empty cells became appreciable.

The materials used were of reagent grade or of special high purity and were used without further purification. Typical initial concentrations of iodine were of the order of 5×10^{-7} gram atoms cm^{-3}. For each system studied at least two different absorption cells were filled and examined.

RESULTS

The results for the various systems investigated are presented individually below:

(1) Pure GaAs—No bands were observed in the spectral region investigated up to temperatures of 950°C.

(2) Pure As—An absorption band was observed in the neighborhood of 3200Å which decreased in intensity with increasing temperature probably due to the As_2, As_1 equilibria.

(3) As—I_2—This system showed an absorption band at low temperature beginning at 4600Å. The intensity of the band decreased with increasing temperature. Simultaneously, the free iodine absorption band appeared, indicating dissociation of the arsenic iodine compound initially present.

(4) Ga—$I_{2\ excess}$—Representative spectra for this system are shown in Figure 1. In the presence of excess iodine the stable iodide

of gallium is GaI_3. This compound melts at 210°C having a vapor pressure of 17 mm at its melting point.[3] The heat of sublimation is 23 kcal/mole, therefore GaI_3 would have a vapor pressure of 1 mm in the neighborhood of 160°C. The spectra of Figure 1 are consistent with this information. At temperatures below 100°C no bands are observed except the free iodine band at 5000Å. (In this representation the fine structure on the long wavelength side of the peak has been

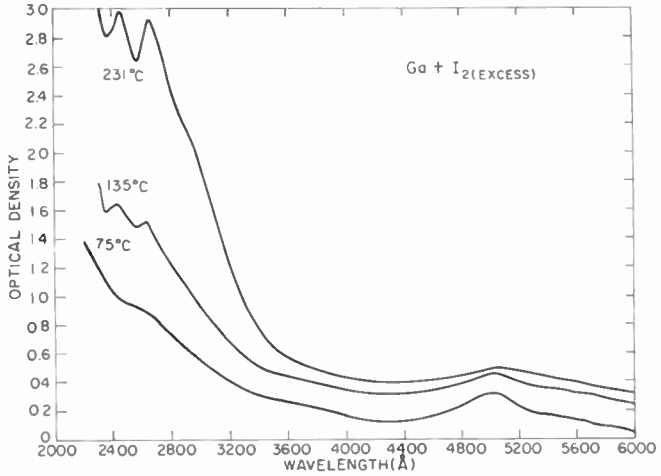

Fig. 1—Variation of optical density with wavelength of absorption in the vapor over the system Ga—$I_{2\ excess}$ for three different temperatures. Zero optical density is displaced for each temperature.

omitted.) At 135°C two additional bands appear—at 2450Å and 2650Å —and their intensity increases with increasing temperature. As long as the free iodine band is present no other bands are observed on increasing the temperature. When the free molecular iodine band disappears two more bands appear at 3050Å and 3900Å. These same two bands are observed in the spectra for the system Ga_{excess}—I_2.

(5) Ga_{excess}—I_2—The spectra for this system are shown in Figure 2. For the condition excess gallium plus iodine, two iodides are stable in the gas phase[4]—GaI_3 and GaI. Increasing temperature favors the

[3] F. J. Smith and R. F. Barrow, "Heats of Sublimation of Inorganic Substances. VI. Some Halides of Gallium and Indium," *Trans. Faraday Soc.*, Vol. 54, p. 826, 1958.

[4] L. Brewer, "The Fusion and Vaporization Data of the Halides," *Chemistry and Metallurgy of Miscellaneous Materials*, ed. by L. L. Quill, McGraw Hill Book Co., Inc., New York, 1950.

GaI. This is reflected in the spectra where it can be seen that as the temperature increases, the two bands at 3050Å and 3900Å increase. The absorption band at 3900Å shows considerable structure and has been shown previously[5] to be the result of two different electronic excitations of the GaI molecule. The greatest absorption peak in this band system is at 3910Å. This peak is extremely sharp and its intensity increases with GaI concentration but does not appreciably broaden. Therefore the height of this peak was taken as a measure of the GaI concentration in the gas phase.

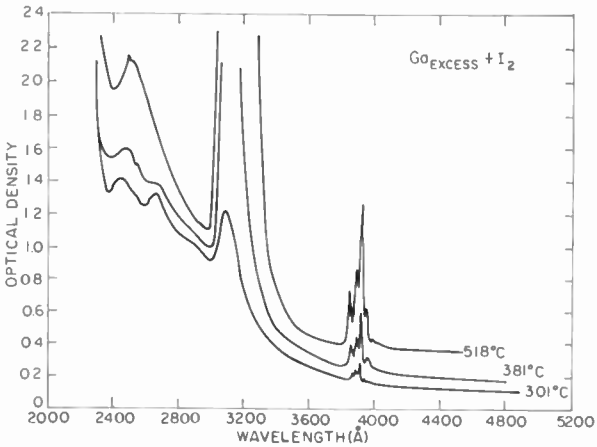

Fig. 2—Variation of optical density with wavelength of absorption in the vapor over the system Ga_{excess}—I_2 for three different temperatures. Zero optical density is displaced for each temperature.

In order to calibrate the peak height with GaI concentration in the gas phase, several cells were studied in which the initial concentration of iodine was low enough to ensure the presence of only GaI at high temperatures. Indeed, it was found for these cells that the 3910Å increased with temperature up to some maximum value, after which it remained constant with increasing temperature. The maximum height of the peak was then taken as being a measure of the GaI concentration.

(6) $GaAs_{excess}$—I_2—Figure 3 shows the spectra obtained for this system. The first notable feature of these spectra is no absorption

[5] E. Miescher and M. Wehrli, "Spectroscopic Study of Gallium Halides in the Vapor State. A Supplement Referring to the Spectrum of Gallium Oxide," *Helv. Phys. Acta*, Vol. 7, p. 331, 1934.

due to molecular iodine. Second, the four peaks corresponding to GaI_3 and GaI are evident. Third, with increasing temperature the peaks corresponding to GaI increase in intensity. Finally, there is also some absorption at the shorter wavelength due to free arsenic in the system.

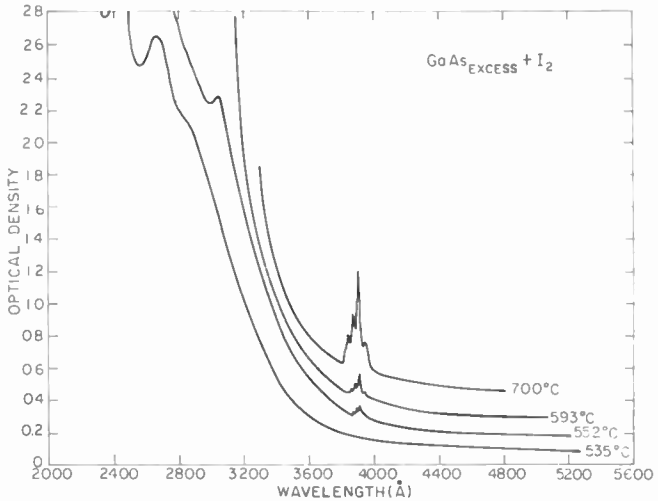

Fig. 3—Variation of optical density with wavelength of absorption in the vapor over the system $GaAs_{excess}$—I_2 for four different temperatures. Zero optical density is displaced for each temperature.

Discussion

It is concluded from the spectra that the only species present in the gas phase of the system $GaAs_{excess} + I_2$ are GaI_3, GaI, and arsenic. Therefore, the reaction responsible for the transport of GaAs is

$$4GaAs_{(s)} + 2GaI_{3(g)} \rightleftharpoons 6GaI_{(g)} + As_{4(g)}, \qquad (1)$$

where it should be noted that the arsenic equilibrium

$$2As_{2(g)} \rightleftharpoons As_4 \qquad (2)$$

must also be considered. From Equation (1) the equilibrium constant for the transport reaction is given by the expression

$$K = \frac{P_{GaI}{}^3 P_{As_4}{}^{1/2}}{P_{GaI_3}}.$$

Using the values for the concentration of GaI obtained from the spectra and making the assumptions that (a) the number of gram atoms of gallium present in the gas phase as GaI and GaI_3 is equal to the number of gram atoms of arsenic present as As_2 and As_4, (b) all the iodine initially present reacts to form an iodide of gallium and (c) the data of Sinke and Stull[6] for the $2As_2$, As_4 equilibria holds

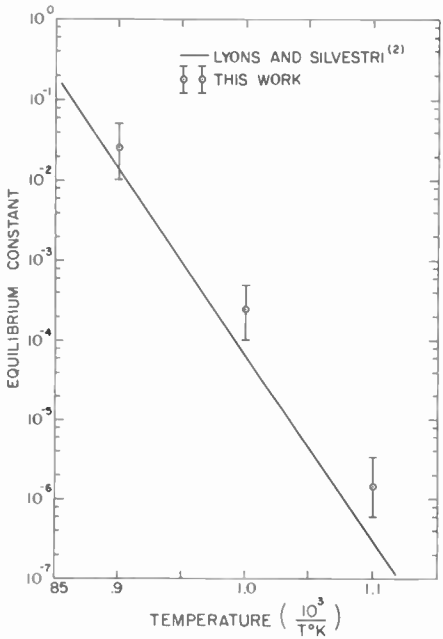

Fig. 4—Logarithm of the equilibrium constant for gallium arsenide transport reaction versus reciprocal of absolute temperature.

here, it is possible to calculate K over the temperature range investigated. The result of the calculation for two different initial concentrations of iodine are shown in Figure 4 together with the results of Lyons and Silvestri.[2] It is evident that the results reported here are in agreement with those of Lyons and Silvestri.

The slight difference between the equilibrium constant values found in this work and those found by Lyons and Silvestri arises from the lesser sensitivity of the optical technique and the necessity of doing

[6] D. R. Stull and G. C. Sinke, *Thermodynamic Properties of the Elements*, No. 18 of *Advances in Chemistry Series*, p. 8, Washington: American Chemical Soc., 1956.

the calibration experiments at low iodine concentrations. This latter restriction makes weighing-error effects much greater but was required in order to ensure the presence of only GaI at the higher temperatures. However, these results do demonstrate that the chemical reaction given by Equation (1) is the one responsible for the transport of GaAs.

Conclusions

The molecular species present in the gas phase of the GaAs—I_2 system have been determined by absorption spectroscopy. They are GaI, GaI_3 and free arsenic. The chemical equation which describes the vapor transport of GaAs using I_2 is

$$4GaAs_{(s)} + 2GaI_{3(g)} \rightleftharpoons 6GaI_{(g)} + As_{4(g)}.$$

The equilibrium constants found by the optical technique are in agreement with those of Lyons and Silvestri determined by pressure measurements.

EPITAXIAL GROWTH FROM THE LIQUID STATE AND ITS APPLICATION TO THE FABRICATION OF TUNNEL AND LASER DIODES

By

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Summary—*An apparatus and procedures have been developed for the epitaxial growth of GaAs and Ge from the liquid state. The resulting technology has been found to possess advantages over vapor-phase epitaxy in some applications demanding highly doped epitaxial films and high-quality p-n junctions at the substrate–film interface. In this connection, it is an important feature of the liquid-phase process that chemical impurities and mechanical damage of the substrate are removed when material is initially dissolved from the substrate surface prior to epitaxial growth. A clean interface p-n junction is thus obtained. Since liquid-phase epitaxy also favors the achievement of high doping and a steep concentration gradient at the p-n junctions, the process has proved itself eminently suitable for application in the manufacture of Ge tunnel diodes. In its application to the fabrication of the GaAs laser diode, it is an additional advantage of the liquid-phase process that the interface p-n junction is formed on a (100) crystal plane. As a consequence, this p-n junction is perfectly planar and also perpendicular to the (110) cleavage planes of the wafer. An optimum geometry (plane-parallel ends perpendicular to a perfectly flat p-n junction) is thus insured for diodes cleaved from (100) oriented GaAs wafers whose p-n junction has been formed by liquid-phase epitaxy.*

Introduction

IT IS WELL KNOWN that vapor-phase epitaxy has had a revolutionary impact on semiconductor device technology. It is less well known, however, that for some applications epitaxial growth from the liquid phase can also give excellent results. Investigations carried out in these Laboratories have shown, for instance, that liquid-phase epitaxy possesses advantages over vapor-phase epitaxy in applications demanding highly doped epitaxial films and high-quality p-n junctions at the substrate–film interface. Thus, liquid-phase epitaxy has found important applications in the manufacture of tunnel diodes[1] and in the fabrication of experimental GaAs laser diodes.

In this paper, the apparatus and the processing details involved in

[1] H. Nelson, "Epitaxial Crystal Growth from the Liquid Phase," *Solid State Device Conference*, Stanford University, June 26, 1961.

liquid-phase epitaxy are described. In addition, the physical properties of Ge and GaAs epitaxial material are discussed and device results presented.

Apparatus and Procedure

Liquid-Phase GaAs Epitaxy

Figure 1 illustrates the apparatus used for liquid-phase epitaxy. In the cross section at the top of the figure, the starting condition

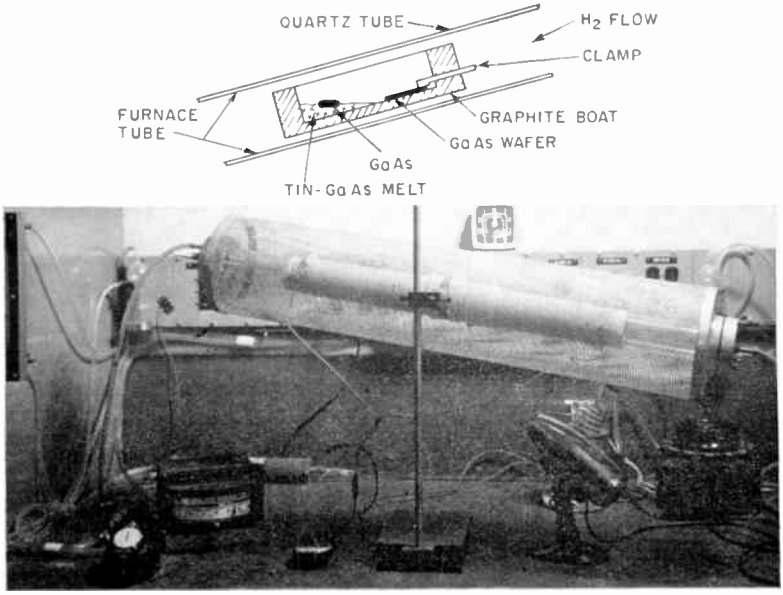

Fig. 1—Apparatus for epitaxial growth from the liquid state.

for the generation of an n-type GaAs film on a p-type GaAs substrate is illustrated. The substrate wafer to be processed is of the (100) orientation and it is held tightly against the flat bottom at the upper end of a graphite boat. A tin–GaAs mixture is placed at the lower end. The graphite boat is fixed in position at the center of a constant-temperature zone of the quartz furnace tube. With the furnace tube tipped as shown in the diagram and with a flow of hydrogen through the tube, the graphite boat is heated to about 640°C. As the temperature rises, GaAs particles dissolve in the tin at the lower end of the boat. When the temperature reaches about 640°C, the heating power is turned off and the furnace is tipped so that the molten tin covers the exposed surface of the GaAs wafer. At this time the tin

is nearly saturated with GaAs. As the furnace cools, GaAs initially dissolves from the substrate surface until a solution equilibrium is established. Then upon further cooling, precipitation of GaAs from the solution and epitaxial growth upon the substrate occurs. At about 400°C, the hydrogen flow through the furnace is replaced by nitrogen and the solution is decanted from the wafer surface by tipping the furnace back to its original position. Immediately afterwards the graphite boat is removed from the furnace tube and any remaining tin is wiped off the surface of the epitaxial layer. The same GaAs-Sn solution can be used successively for the processing of several wafers.

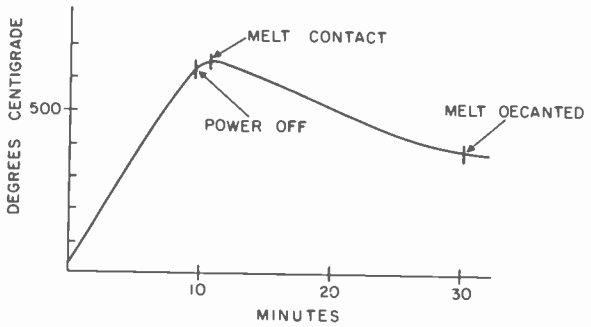

Fig. 2—Heating schedule for epitaxial deposit of GaAs from a tin solution.

More GaAs is occasionally added to the melt to replace that consumed in epitaxial growth. The details of the heating cycle employed are depicted in Figure 2. This heating cycle leads to the formation of an epitaxial layer about 1 mil thick.

It is an important feature of the liquid-phase process described above that during the substrate dissolution, which occurs before epitaxial growth begins, a solution front is formed which coincides with a (100) crystal plane of the wafer. As a consequence, the p-n junction formed is perfectly planar and also perpendicular to the (110) cleavage planes of the wafer. This condition is particularly advantageous when the liquid-phase process is used in the fabrication of laser diodes. An optimum geometry (plane-parallel ends perpendicular to a perfectly flat p-n junction) is insured for the parallelopiped diodes which are cleaved from the processed wafer. It is another desirable feature of the liquid-phase process that chemical impurities and work damage on the substrate surface are removed during dissolution of the surface

layer prior to epitaxial growth. Consequently, a clean, interface p-n junction with excellent diode characteristics is insured.

In the example of liquid-phase epitaxy described above, the tin used as a solvent is a donor in GaAs. As a consequence, it can be used for the generation of n-type regions with a net donor concentration of about 5×10^{17} cm^{-3} (determined by the as yet unknown function of the saturation solubility of tin in GaAs at these temperatures). Compensated n-type regions of higher resistivity, as well as p-type regions, can be obtained by adding zinc or cadmium to the tin used as solvent for the GaAs. However, to avoid the need for compensation, the tin

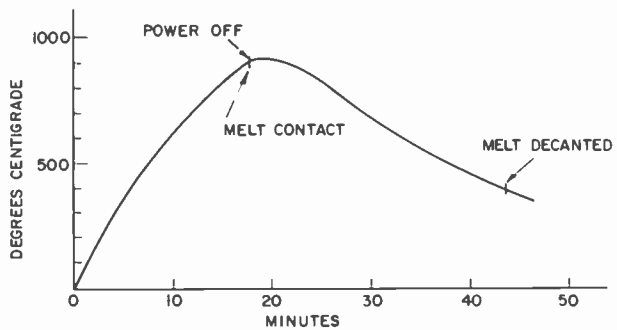

Fig. 3—Heating schedule for epitaxial growth of GaAs from a gallium melt.

can be replaced by gallium as a solvent for the GaAs. Type and degree of doping can then be controlled by adding the requisite amount of donor or acceptor impurity to the solvent melt. Thus, excellent epitaxial material for laser-diode use has been prepared using a solvent melt composed of 4.5 gram Ga and 0.7 gram GaAs. This basic melt has been doped with 0.010 gram of Te for the growth of n-type material or it has been doped with 0.10 gram of Zn for the growth of p-type films. The processing schedule is similar to the one used with tin except that higher temperatures are used. The heating cycle is shown in Figure 3. An epitaxial film about 5 mils thick is formed under these processing conditions.

Liquid-Phase Germanium Epitaxy

In the case of Ge, liquid-phase epitaxy has proved important chiefly in the manufacture of tunnel diodes. Epitaxial material for this application is processed in the same type of apparatus as is used with GaAs and the processing schedules are similar but (111) oriented wafers are employed as substrates. To deposit a degenerate p-type

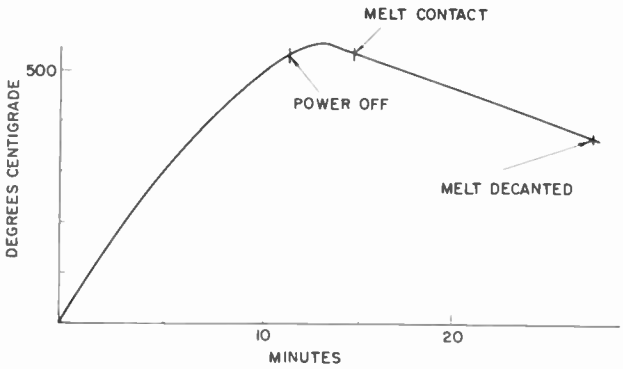

Fig. 4—Heating schedule for epitaxial deposit of Ge from an indium solution.

epitaxial film on an n-type substrate, Ga-doped indium is used as the solvent for the Ge. The n-type substrate material is doped with arsenic to a net donor concentration of, say, 2.5×10^{19} cm^{-3}. When the heating cycle shown in Figure 4 is employed, about 0.3 mil thickness of Ge is dissolved from the substrate after which an epitaxial film about one mil thick is deposited. The net acceptor concentration in the epitaxial layer is a function of the Ga content of the solvent melt. For a melt composed basically of 30 grams In and 3 grams Ge, the net acceptor concentrations varies with the weight of Ga added to the melt as shown in Figure 5.

The interface p-n junctions of epitaxial Ge material processed as above can be perfectly planar as observed by light microscopy. How-

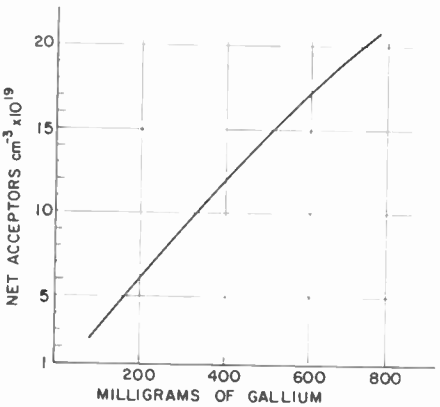

Fig. 5—Acceptor concentration in epitaxial layer versus weight of gallium added to a 30-gram indium solvent melt.

ever, in many instances slight departure from planarity occurs. Thus, for the growth of germanium on a germanium substrate, it is observed that the solution-front formed before regrowth is less likely to coincide with a wafer crystal plane than in the case of GaAs.

Epitaxial Ge material particularly suitable for the manufacture of high-quality tunnel diodes is prepared by the growth of degenerate n-type epitaxial layers on degenerate p-type substrates. A solvent melt composed of 40.0 grams of tin, 25.0 grams of lead, 5.0 grams of germanium, and 1.5 grams of arsenic is used. The heating cycle shown

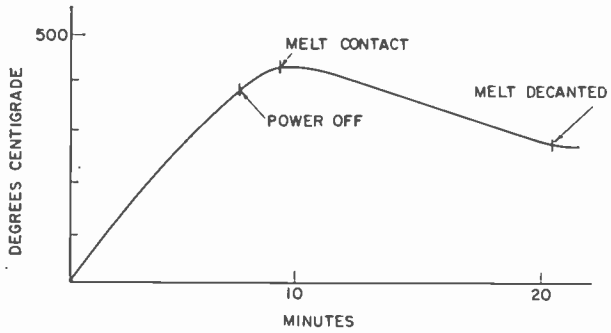

Fig. 6—Heating schedule for epitaxial deposit of Ge from a tin-lead solution.

in Figure 6 results in the growth of an epitaxial film about 0.3 mil thick following substrate dissolution to a depth of about 0.2 mil. The p-n interface region tends to be very jagged.

Additional work has been carried out in which high-purity lead was used as the main constituent of the solvent melt. This has allowed the deposition of high-quality epitaxial films in a range of thickness from 1 to 75 microns and in a range of resistivity from 0.001 to 0.8 cm. However, this work led to the conclusion that the liquid-phase epitaxy is not likely to be competitive with vapor-phase epitaxy in applications where a high degree of control and reproducibility with regard to resistivity and film-thickness is required.

Characteristics of Liquid-Phase Epitaxial Material

In the course of the investigations of liquid-phase epitaxy, device performance has been largely depended upon as a direct measure of the quality of the epitaxial material employed. Additional information has been obtained from x-ray diffraction data and from optical microscope observations on dislocation density and lineage. Except for

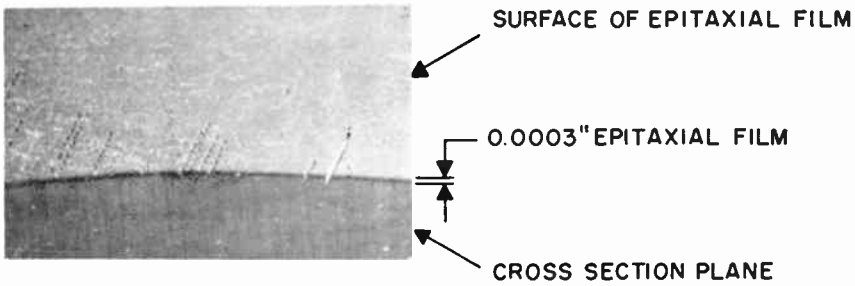

Fig. 7—Angle-lapped cross section of arsenic-saturated epitaxial film on degenerate p-type germanium.

arsenic-doped, highly degenerate germanium films, Laue patterns obtained on the epitaxial films are indistinguishable from those obtained for bulk, single-crystal material. In the case of n-type germanium films grown from a tin–arsenic solution, the crystalline quality deteriorates as the arsenic content is increased to the point where highly degenerate deposits are obtained. The surface texture becomes grainy and inclusions of GeAs are found at the surface of the films. As a result of the high saturation solubility of tin in germanium, the tin content of these films is as high as 0.5 at.%. Since tin is electrically inert in germanium, the semiconductor properties are little affected by its presence. However, it leads to a slight increase in the coefficient of thermal expansion of the germanium as evidenced by a "bimetallic strip effect" exhibited by processed wafers.

An angle-lapped cross section of an arsenic-doped, epitaxial film grown on degenerate p-type Ge is shown in Figure 7. The grainy texture of the epitaxial surface and the jagged p-n junction typical of this epitaxial material is apparent in the photograph. The cross section shown in Figure 8, however, is more typical of liquid-phase epitaxial

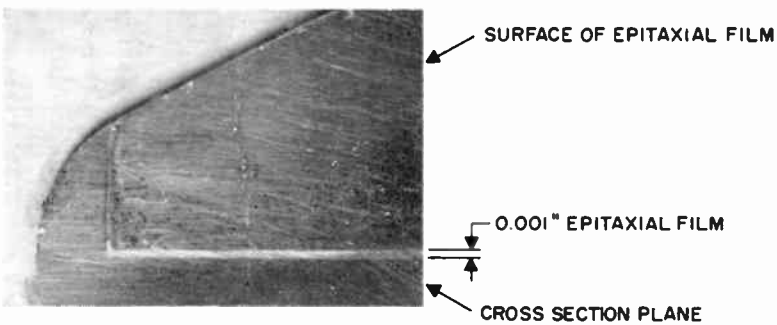

Fig. 8—Angle-lapped cross section of degenerate Ga-doped epitaxial film on degenerate n-type germanium.

material in general. It is an angle-lapped cross section of germanium epitaxial material prepared by growth of degenerate p-type germanium ($N_a \approx 8 \times 10^{19}$ cm^{-3}) on a degenerate n-type substrate ($N_d \approx 2.5 \times 10^{19}$ cm^{-3}). The surface of the epitaxial layer is relatively flat and the p-n junction is seen to be planar.

The microphotographs of Figure 9 show cross sections prepared by etching cleavage planes of typical epitaxial GaAs material prepared by liquid-phase epitaxy. As seen in these micrographs, the interface p-n junctions are planar and perpendicular to the (110) cleavage planes.

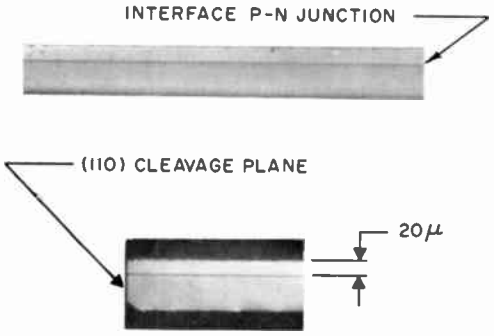

Fig. 9—Cross sections of GaAs epitaxial laser-diode material.

This is evidence of the fact that in GaAs, the pre-growth solution front tends to coincide with a (100) crystal plane.

Device Results

GaAs Laser Diodes

The application of liquid-phase epitaxy to the fabrication of experimental GaAs laser diodes was directed toward two main objectives. One of these was to provide laser diodes for the study of light emission and laser behavior as a function of doping impurities and distribution profiles of dopants, especially of those not readily obtained by diffusion. Another objective was to determine the merits of liquid-phase epitaxy relative to conventional diffusion for the fabrication of high-quality laser diodes.

Although these investigations have not been completed, significant results have been obtained. With regard to the first objective, the effects of different dopants and of unusual concentration gradients at the p-n junction in epitaxial laser diodes have been studied by J. Pan-

kove and by G. Dousmanis.[2] As an example of results obtained, the curves in Figure 10 show a markedly greater frequency shift of the incoherent emission peak with current density for diodes with steep concentration gradients than for diodes with more-shallow p-n junctions. The curves A and B represent data for a diffused and an epitaxial diode, respectively. The doping density on either side of the p-n junction is about the same for both diodes. As determined from

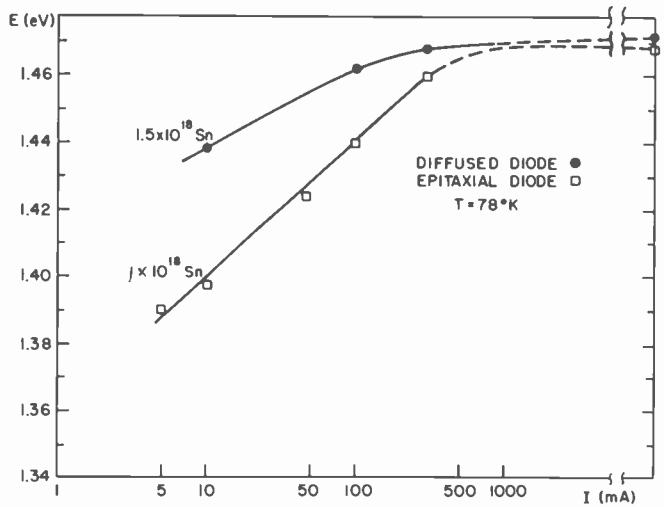

Fig. 10—Energy of emission peak versus current.

capacity measurements, however, the dopant concentration gradient at the p-n junction is 3.5×10^{22} cm^{-4} for the diffused and 1.4×10^{23} cm^{-4} for the epitaxial diode.

With regard to the second objective, tests carried out in the course of our investigations have shown lower laser thresholds for epitaxial than for diffused diodes. However, light emission efficiency and laser threshold for both types of diodes vary greatly from lot to lot of GaAs starting material, apparently as a result of variation in crystal quality. It is possible, therefore, that superiority in crystalline quality of starting material rather than superiority in processing technology is responsible for the improved results obtained with epitaxial laser diodes. It is worth emphasizing, however, that planar p-n junctions which are perpendicular to (110) cleavage planes can be more reliably achieved

[2] G. C. Dousmanis, C. W. Mueller, and H. Nelson, "Effect of Doping on Stimulated and Incoherent Emission in GaAs," to be published in *Jour. Appl. Phys. Letters.*

through liquid-phase epitaxy than through diffusion. Optimum laser-diode geometry should thus be more easily obtainable with epitaxially grown layers.

The laser performance data gathered in the course of this investigation have been obtained for laser diodes cleaved from epitaxy-processed wafers of the (100) orientation. Before cleavage these wafers are heat treated at 900°C for four hours and then lapped on the n-type side to a final thickness of three mils. Also, both of the major surfaces are metallized to provide high-conductivity ohmic contacts to the p- and n-type regions. The parallelopiped diodes cleaved from these wafers are dimensionally nonuniform, but for comparative tests, units are

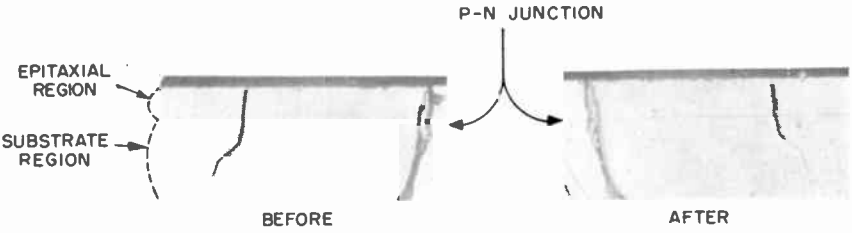

Fig. 11—Cross sections of epitaxial GaAs wafer before and after 4 hours of inter-diffusion at 900°C.

selected which are about 5 mils wide and 20 mils long. The 900°C heating step is essential for good laser performance. The resulting interdiffusion of acceptors and donors that occurs at the p-n junction leads to no perceptible displacement of this junction (see Figure 11). However, the interdiffusion results in an increased depletion-layer width at the p-n junction with a resultant improvement of the reverse and forward characteristics, as shown in Figure 12.

The curves in Figure 12 represent data obtained for a typical diode cleaved from material prepared by epitaxial growth of GaAs from a tellurium-doped gallium solution onto a zinc-doped substrate ($N_a \approx 1 \times 10^{19}$ cm^{-3}). Almost identical diode characteristics are obtained from diodes cleaved from material prepared by GaAs growth from a zinc-doped gallium solution on a tellurium-doped substrate ($N_a \approx 1.1 \times 10^{18}$ cm^{-3}). Table I shows threshold data for three representative diodes from each of the two types of material. For purpose of comparison, data for three diffused diodes are included in this table. These diodes were cleaved from material prepared by the diffusion of zinc into a tellurium-doped wafer ($N_d \approx 1.1 \times 10^{18}$ cm^{-3}). All diodes in-

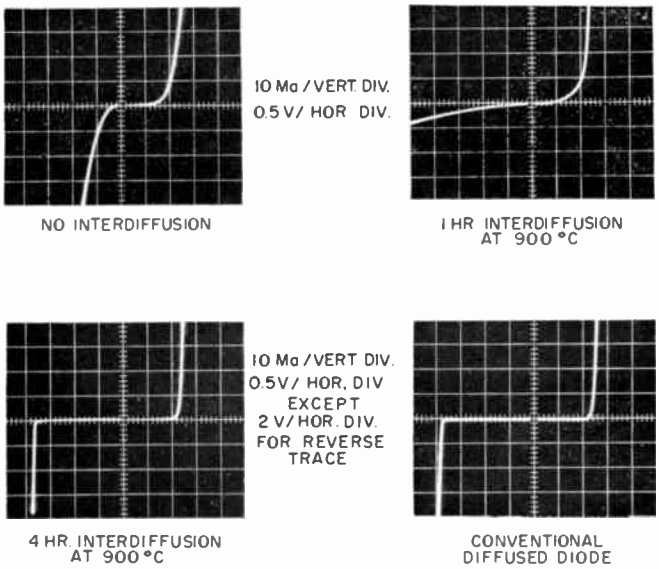

Fig. 12—Epitaxial GaAs diode characteristics.

volved are parallelopiped structures the sides of which have been sawed. They are all approximately 0.003 inch thick, 0.005 inch wide, and 0.020 inch long.

Germanium Tunnel Diodes

In the manufacture of tunnel diodes one of the principle advantages of liquid-phase epitaxy is that it permits the fabrication of numerous

Table I—Threshold Data for Epitaxial and Diffused GaAs Laser Diodes

Diode Type	Laser Threshold (amp cm^{-2}) Diode #1	Diode #2	Diode #3
Epitaxial n-type film on a p-type substrate	1.8×10^3	1.7×10^3	2.0×10^3
Epitaxial p-type film on an n-type substrate	1.5×10^3	1.6×10^3	1.4×10^3
P-type region diffused into an n-type wafer*	7.0×10^3	8.5×10^3	9.0×10^3

* This wafer and the above n-type substrate wafer were cut from the same GaAs crystal. GaAs laser diodes made from other crystals have yielded thresholds as low as 3×10^3 amp cm^{-2}.

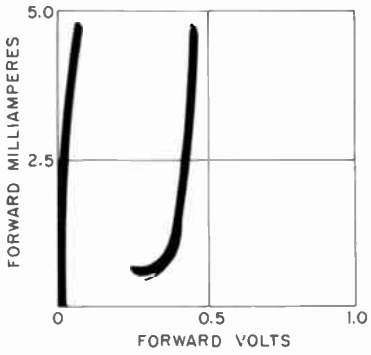

Fig. 13—Forward-bias characteristics of ten tunnel diodes from a 25-unit array.

identical devices from large-area wafers of processed material. The data represented in Figure 13 is testimony to the great uniformity from unit to unit which can be achieved by this technique. The curve shown is an "envelope" of the oscillograph traces for 10 equal-area tunnel diodes of a 25-unit array. This device uniformity is indicative also of the high degree of homogeneity which can be achieved in epitaxial films grown by liquid-phase epitaxy.

For a p-type epitaxial layer on an n-type substrate the forward-bias characteristics shown by the oscillographs traces A and B of Figure 14 are obtained. Traces A and B are typical for low and high doping densities, respectively. Trace A represents a diode with a net donor concentration in the n-region of about 2.2×10^{19} cm^{-3} and a net acceptor concentration in the p-region of about 8×10^{19} cm^{-3}. Trace B represents a diode for which the respective concentrations are 3.2×10^{19} cm^{-3} and 3.0×10^{20} cm^{-3}. The junction area is the same for both diodes. As evidenced by the data represented by Figure 12, it is characteristic of p- and n-type tunnel-diode material that high tunnel-

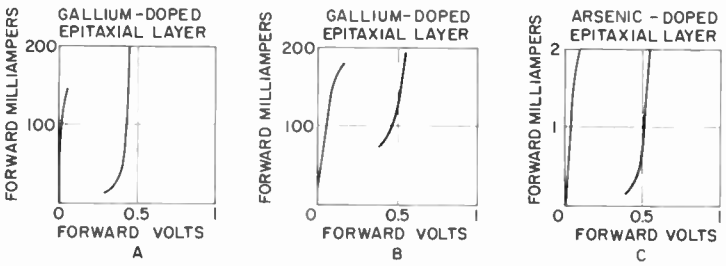

Fig. 14—Forward-bias characteristics of epitaxial Ge tunnel diodes.

current density cannot be achieved by increased doping without simultaneous loss of high peak-to-valley current ratio. In this respect superior results are obtained with n-on-p type material. Trace C of Figure 14 represents a diode of the same junction area as the one represented by traces A and B, but it is fabricated from epitaxial material prepared by growing arsenic and tin-saturated n-type germanium on a p-type substrate with a net acceptor (gallium) concentration of 8×10^{19} cm^{-3}. The high peak-to-valley current ratio evidenced by trace C is characteristic of this type of epitaxial material even at doping densities requisite for peak-currents densities up to 30,000 amp cm^{-2}.

Conclusions

The epitaxial growth of Ge and GaAs from the liquid state has proved a valuable addition to semiconductor technology. This process has found important practical applications in the manufacture of several types of Ge tunnel diodes and in the fabrication of high-quality, experimental GaAs laser diodes.

Compared to vapor-phase epitaxy, the liquid-phase process is characterized by simplicity and speed. Its equipment requirements are very modest and the same apparatus can be used for different semiconductor materials and for a great variety of growth conditions.

Acknowledgments

In the work reported upon, I have had the encouragement and the assistance of numerous coworkers. I am particularly indebted to H. S. Sommers for encouragement in early work on the preparation of epitaxial tunnel diodes and to S. Bragnum for invaluable direct assistance in this work. R. Glicksman, N. Ditrick, and R. M. Minton deserve special credit for major contributions in adapting the liquid-phase process for the successful manufacturing of Ge tunnel diodes.

Laser diode investigations by J. Pankove and G. Dousmanis have provided vital feedback information used in adapting the liquid-phase process for the fabrication of high-quality GaAs laser diodes. Also, the availability of ingenious test equipment developed by F. H. Nicoll has greatly facilitated this work. Finally, it is a pleasure to acknowledge that Frank Hawrylo's participation in the GaAs work has been characterized to an unusual degree by initiative and the contribution of valuable ideas.

HIGH-POWER EPITAXIAL SILICON VARACTOR DIODES

By

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Somerville, N. J.

Summary—This paper describes the fabrication, electrical characteristics, and circuit performance of high-power diffused epitaxial silicon variable-capacitance diodes mounted in a new low-thermal-impedance microwave package. These diodes are capable of efficient harmonic generation at C-band; a power output of 2.5 watts has been obtained with a single diode at 4000 megacycles. Measured frequency characteristics are shown to be in reasonable agreement with maximum theoretical values.

Introduction

VARIABLE-CAPACITANCE diodes have found extensive use as harmonic generators. Although gallium arsenide may be expected to be generally superior to both silicon and germanium as a material for the fabrication of diodes for operation well into the microwave region,[1] at lower frequencies silicon devices may be designed to give excellent circuit performance.

Significant improvements in silicon material and process technology have been made since the double-diffused diode described by Bakanowsky *et al.*[2] The present paper discusses the fabrication, electrical characteristics, and circuit performance of high-power diffused epitaxial p^+nn^+ diodes mounted in a new low-thermal-impedance microwave package. Agreement between the theoretically predicted frequency characteristics and the observed values is shown to be reasonably good.

Review of Design Considerations

The two parameters of importance in harmonic generation are power-conversion efficiency and power-handling capability. These parameters have been related to device characteristics in the analysis

[1] H. Kressel and N. Goldsmith, "High-voltage Epitaxial Gallium Arsenide Microwave Diodes," *RCA Review*, Vol. 24, p. 182, June 1963.
[2] A. E. Bakanowsky, N. G. Cranna and A. Uhlir, Jr., "Diffused Silicon Nonlinear Capacitors," *Trans. I.R.E. PGED*, p. 384, Oct. 1959.

by Penfield and Rafuse.[3] The maximum input power P_{in} for efficient conversion is

$$P_{in} = BC(V_B)V_B^2, \tag{1}$$

where $C(V_B)$ is the junction capacitance as measured at the breakdown voltage, V_B is the breakdown voltage, and B is a constant that depends on the order of the harmonic desired and the mode of operation.

The power-conversion efficiency is related to the diode cutoff frequency at breakdown $f_T(V_B)$, as given by

$$f_T(V_B) = \frac{1}{2\pi R_D C(V_B)}, \tag{2}$$

where R_D is the diode series resistance. In the analysis by Penfield

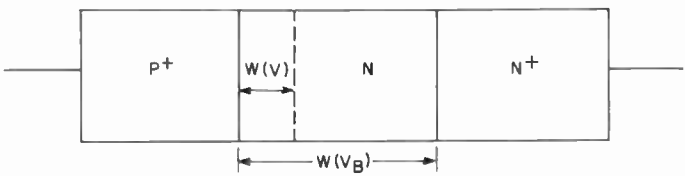

Fig. 1—Structure of p+nn+ diode.

and Rafuse, this resistance was assumed to be independent of reverse applied voltage.

The conversion efficiency η is a rather complicated function which, when $f_{in}/f_T(V_B) < 0.01$, is

$$\eta = 1 - D\frac{f_{in}}{f_T(V_B)}, \tag{3}$$

where f_{in} is the fundamental frequency and D is a constant that depends on the harmonic desired. The required diode power dissipation is, of course, determined by the input power level and the expected conversion efficiency.

If the capacitance is required to change up to the breakdown voltage, then the minimum base width for a p+nn+ device (Figure 1) is the width of the space-charge region at the breakdown voltage, $W(V_B)$ (it is assumed that the p+n junction is abrupt). The n-region

[3] P. Penfield and R. P. Rafuse, *Varactor Applications*, MIT Press, 1962.

doping is chosen so that the desired value of breakdown voltage is achieved. The intrinsic diode series resistance $R_S(V)$ at any applied voltage is assumed to be concentrated between the edge of the space-charge region $W(V)$ and the nn+ interface. If spreading effects in the base region are neglected, the diode resistance is given by

$$R_S(V) = \frac{\rho}{A}\,[W(V_B) - W(V)], \tag{4}$$

where ρ is the n-region resistivity and A is the junction area.

The additional contributions to the total series resistance (contacts, n+ and p+ regions, microwave losses) are lumped in a constant term R_p. Therefore, the equation becomes

$$R_D(V) = R_S(V) + R_p. \tag{5}$$

If the resistance R_p is neglected, the maximum diode cutoff frequency at any reverse applied voltage V is given by

$$f_c(V) = \frac{A}{2\pi\rho C(V)\,[W(V_B) - W(V)]}, \tag{6a}$$

or

$$f_c(V) = \frac{1}{2\pi\epsilon\rho\left[\dfrac{C(V)}{C(V_B)} - 1\right]}, \tag{6b}$$

where ϵ is the semiconductor dielectric constant.

Since $C(V)$ is proportional to $(\phi - V)^n$, where n lies between 1/3 and 1/2 and $\phi = 0.7$ volt for silicon, Equation (6) becomes

$$f_c(V) = \frac{1}{2\pi\epsilon\rho\left[\left(\dfrac{V_B}{\phi - V}\right)^n - 1\right]}, \tag{7}$$

where $V_B \gg \phi$.

For devices having relatively shallow, high-surface-concentration, diffused p+n junctions, the capacitance–voltage relationship is found to be nearly the same as that of an abrupt junction. The diodes described in this paper are fabricated with such junctions.

For silicon, the breakdown voltage is related to the base-region resistivity by an expression similar to the one empirically determined

for alloyed junctions.[4] For values between 40 and 300 volts, this expression is approximated[1] by

$$\rho = 5.5 \times 10^{-3} V_B^{1.2} \text{ ohm-cm.} \tag{8}$$

Thus, when Equation (8) is substituted into Equation (7), the maximum cutoff frequency becomes

$$f_c(V) \cong \frac{3 \times 10^{13}}{V_B^{1.2}\left[\left(\frac{V_B}{\phi - V}\right)^{1/2} - 1\right]} \text{ cycles/sec.} \tag{9}$$

A "parasitic" cutoff frequency can be defined as

$$f_p(V) = \frac{1}{2\pi R_p C(V)}. \tag{10}$$

Therefore, the observed cutoff frequency $f_T(V)$ is given by

$$f_T(V) = \frac{f_c(V)\, f_p(V)}{f_c(V) + f_p(V)}. \tag{11}$$

Diode Fabrication

The two main criteria for the basic material are (1) the degree of crystal perfection in the epitaxial film which insures reasonable values of breakdown voltage, and (2) the uniformity of the impurity profile in the film. The optimum combination of resistivity and base width can only be achieved by close control of the diffusion depth on epitaxial films having a known impurity profile.

Figures 2 and 3 show the resistivity profile and the capacitance–voltage relationship of the diode. The resistivity profile was determined by measurement of the microwave resistance as a function of reverse bias.[5] Diode A has a normal capacitance change as a function of voltage ($n = 0.44$) nearly up to the breakdown voltage, while diode B has a variable slope in the capacitance–voltage curve after 20 volts.

[4] K. G. McKay, "Avalanche Breakdown in Silicon," *Phys. Rev.*, Vol. 94, p. 877, May 1954.

[5] H. Kressel and M. Klein, "Determination of Epitaxial-layer Impurity Profile by Means of Microwave Diode Measurements," *Solid State Electronics*, Vol. 6, p. 309, May-June 1963.

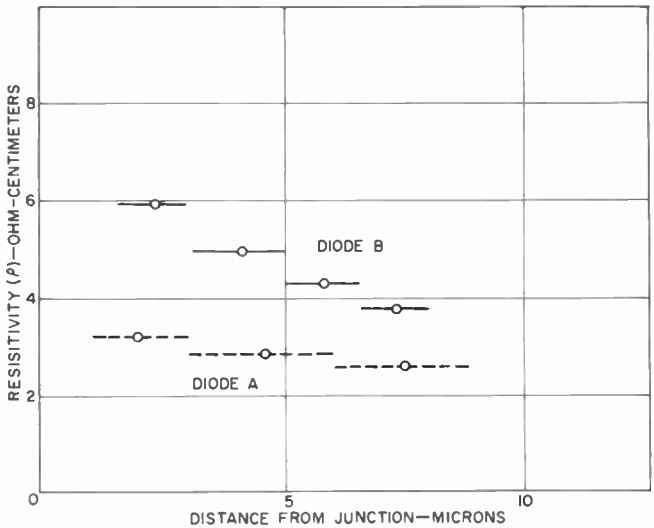

Fig. 2—Resistivity profile for two types of epitaxial films.

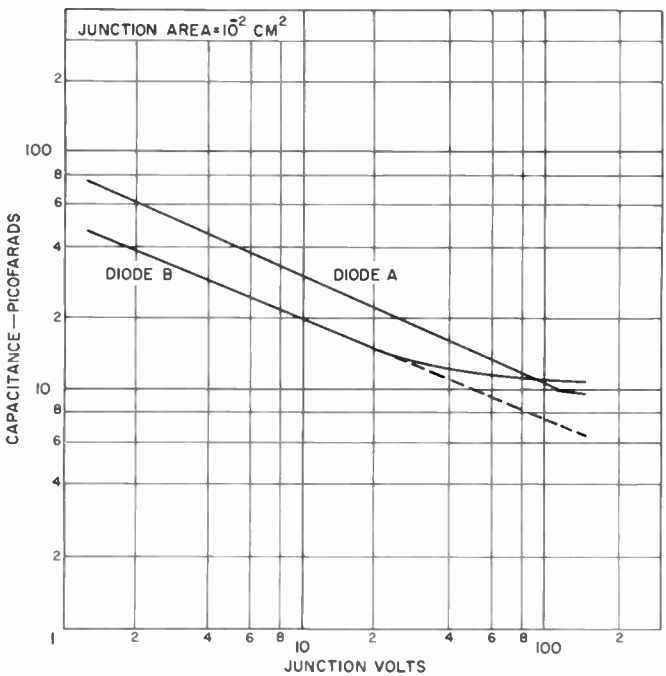

Fig. 3—Capacitance–voltage relationship for diodes fabricated on the epitaxial layers shown in Figure 2.

Epitaxial layers fabricated by the reduction of both $SiCl_4$ and SiH_4 have been used. Excellent results have been achieved in the fabrication of large-area (10^{-2} cm^2), high-voltage (over 200 volts) diodes having SiH_4 deposited layers.[6,7]

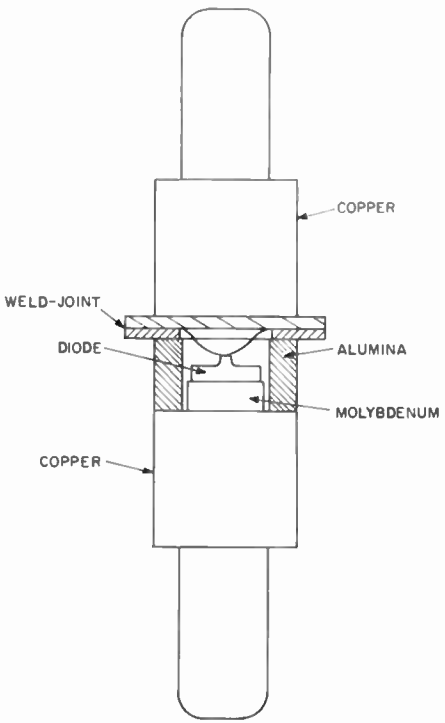

Fig. 4—Outline of silicon varactor diode using the new microwave case.

The p region is formed by boron diffusion. Surface concentrations are typically in excess of 5×10^{19} atoms per cubic centimeter and the junction penetration is adjusted to the desired base width. A metal contact is evaporated and alloyed onto the p layer. The junctions are defined by a wax mask, and individual pellets are soldered into the ceramic package. Contact to the mesa is made by bonding of a metal strip, as shown in Figure 4. The complete device is then rinsed, baked, and hermetically sealed in an inert atmosphere. Obviously, the package

[6] S. R. Bohla and A. Mayer, "Epitaxial Deposition of Silicon by Thermal Decomposition of Silane," *RCA Review*, Vol. 24, p. 511, Dec. 1963.

[7] M. A. Klein, H. Kressel, and A. Mayer, "Silane Epitaxial Silicon for Microwave Diodes," Electrochemical Society Meeting, Pittsburgh, April 1963.

is very important in the determination of circuit performance because its thermal resistance may limit power dissipation. The mechanical and thermal properties of the new package used for these devices are much superior to those of the conventional microwave cartridge. The pellet is mounted on a molybdenum base which is brazed to a large copper stud. This construction provides an excellent heat sink. In addition, this package eliminates the pressure contacts to the mesa top normally found in diodes mounted in conventional cartridges. As a result, the device is mechanically very rugged. The package has a typical capacitance of 0.6 picofarad and its outline is such that it fits into standard cartridge circuit holders.

Device Characteristics

The diode series resistance is determined at any desired reverse voltage from a measurement of the diode impedance at 2 gigacycles. The capacitance is measured at 1 megacycle by use of a capacitance bridge. The cutoff frequency can then be calculated.

Diodes having breakdown voltages between 50 and 300 volts have been fabricated. Measurements of the capacitance as a function of voltage show typical exponents which vary from about 0.45 between zero bias and one third of the breakdown voltage to 0.33 close to the breakdown voltage (because of the slight impurity gradient which is generally present in the layer).

Measurements of cutoff frequency at low values of applied voltage (the choice of —6 volts is arbitrary) will be discussed because the series resistance at that voltage is very nearly at its maximum value. The cutoff frequency values obtained from the better devices fabricated are shown in Figure 5 as a function of the breakdown voltage V_B between 50 and 130 volts. A plot of the maximum theoretical value for abrupt junctions (Equation (9)) is also shown. For some values of V_B, the observed cutoff frequency exceeds the theoretical because (1) as mentioned earlier, most diodes are not truly abrupt, and the average base resistivity is lower than the predicted one, and (2) the equation used to relate ρ and V_B is only an approximate one. These particular diodes are relatively small-area devices (capacitance at —6 volts is typically 1.0 picofarad), and the diode resistance is large relative to R_p. Evidently the cutoff frequency can be expected to increase for a given value of breakdown voltage when the base width is smaller than the one required for capacitance variation up to the breakdown voltage. Figure 6 compares the theoretical and observed values of the cutoff frequency for a group of 190-volt diodes as a

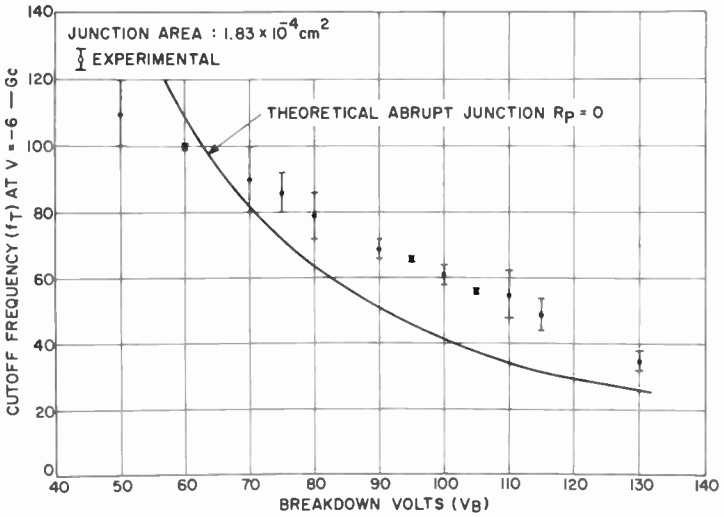

Fig. 5—Experimental and observed values of cutoff frequency at $V = -6$ volts as a function of breakdown voltage.

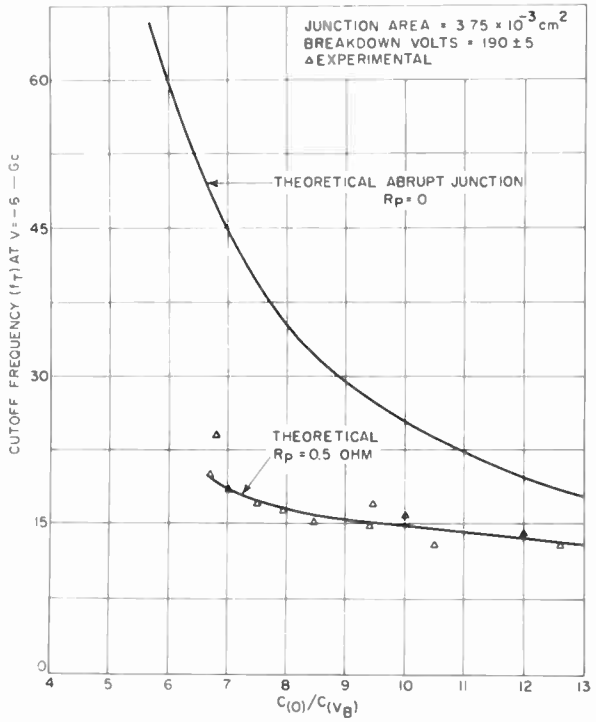

Fig. 6—Experimental and observed values of cutoff frequency at $V = -6$ volts as a function of $C(0)/C(V_B)$ for a group of 190-volt diodes.

retical values. Further refinements in fabrication techniques should further reduce the parasitic diode losses, which represent a significant part of the total resistance for the higher-capacitance devices, and thus make possible efficient operation at even higher power levels.

ACKNOWLEDGMENTS

The authors thank Dr. A. Blicher, under whose direction this work was performed, for many helpful suggestions; H. C. Lee and E. Markard for making available the data of Tables I and II, respectively; T. Gonda for providing the data for the 1100-2200 mc circuit; and W. Mueller for assisting in the fabrication of the devices.

AN ANALYSIS OF THE GAIN-BANDWIDTH LIMITATIONS OF SOLID-STATE TRIODES

By

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Summary*—*It is shown that the upper limit to the gain–bandwidth product of solid-state triodes is controlled mainly by the dielectric relaxation time of the space between emitter and grid. The high-frequency limit is then approximately* $f = 1/(2\pi\tau_{rel})$ *where* $\tau_{rel} = (K/(4\pi\sigma)) \times 10^{-12}$ *and* σ *is the conductivity of the space between emitter and grid. The conditions needed to achieve this limit are outlined for the bipolar transistor, unipolar transistor, space-charge-limited triode, field-emission triode, and "Barristor."

Introduction

THE ATTEMPTS to extend the performance of triodes to higher frequencies (e.g., above one gigacycle) have led various individuals to stress the virtues of one or more of the triode arrangements sketched in Figures 2-6. Johnson and Rose[1] have singled out the unique property of the bipolar transistor in that it achieves the closest physical coupling between the *controlling* and the *controlled* charge. Wright[2] has emphasized the short transit times attainable in the space-charge-limited triode.[3] The author had proposed a majority-carrier triode* (referred to at the time as the "Barristor") using a thin electron-permeable metal grid to avoid the limitations of the base resistance of the bipolar transistor. Mead[4] has proposed a "tunnel triode" in which the high emitter current densities are expected to lead to improved performance at high frequencies. Finally, the well-

[1] E. O. Johnson and A. Rose, "Simple General Analysis of Amplifier Devices with Emitter, Control and Collector Functions," *Proc. I.R.E.*, Vol. 47, No. 3, p. 407, March 1959.

[2] G. T. Wright, "A Proposed Space-Charge-Limited Dielectric Triode," *Jour. Brit. I.R.E.*, Vol. 20, p. 337, May 1960.

[3] W. Ruppel and R. W. Smith, "CdS Analog Diode and Triode," *RCA Review*, Vol. 20, p. 702, Dec. 1959.

* This structure was described in a Government Contract report (September 1960) on work supported in part by the U. S. Navy. It has since been described independently by M. M. Atalla at the IRE-AIEE Device Research Conference, Durham, N. H., 1962, and by D. V. Geppert, "A Metal-Base Transistor," *Proc. I.R.E.*, Vol. 50, p. 1527, June 1962.

[4] C. A. Mead, "The Tunnel-Emission Amplifier," *Proc. I.R.E.*, Vol. 48, No. 3, p. 359, March 1960.

known unipolar, or field-effect, transistor[5,6] has the advantage of being a simple, majority-carrier device.

It is the purpose of this analysis to show that none of the solid-state triodes has a unique advantage in its principle of operation at high frequencies, and that the upper limit to the high-frequency performance of all of the listed triodes is controlled in much the same way by the same physical parameters, of which the major parameter is the dielectric relaxation time of the space between emitter and grid. This conclusion does not preclude an emphasis on particular devices

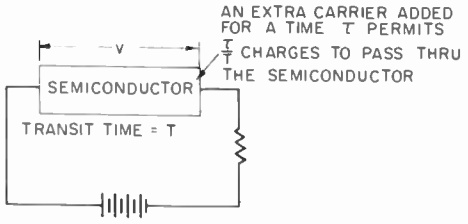

Fig. 1—Generalized argument for current gain.

for particular application for technological reasons, especially at frequencies below the upper limit.

Gain–Bandwidth Product

We review quickly the generalized formulation[1] of the gain–bandwidth product for charge-control devices.

Consider, as in Figure 1, two electrodes connected ohmically to a semiconductor. If we add an extra carrier to the semiconductor for a time τ, the extra carrier will allow τ/T extra electron charges to pass between the electrodes, where T is the transit time of a carrier between electrodes. The purpose of any control grid is to add (or subtract) extra carriers in the region between emitter and collector. If a charge $+Q$ is put on the grid, an equal and opposite charge $-Q$ is introduced into the emitter–collector space. The grid or control current is then Q/τ, and the collector or controlled current is Q/T. The current-gain is then:

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[5] W. Shockley, "A Unipolar 'Field Effect' Transistor," *Proc. I.R.E.*, Vol. 40, No. 11, p. 1365, Nov. 1952. O. Heil, British Patent 439, 457 (1935).

[6] P. K. Weimer, "The TFT—A New Thin Film Transistor," *Proc. I.R.E.*, Vol. 50, No. 6, p. 1462, June 1962.

$$\text{Current gain} \equiv G_I = \frac{\tau}{T}. \tag{1}$$

Now, to put the charge Q on the grid requires a voltage

$$V_i = \frac{Q}{C_i}$$

where C_i is the input or grid capacitance. The charge on the grid gives rise to the amplified charge $Q\tau/T$ at the collector. The voltage appearing at the collector will then be

$$V_0 = \frac{Q}{C_0}\frac{\tau}{T}$$

where C_0 is the output or collector capacitance; the voltage gain will be

$$G_V = \frac{C_i}{C_0}\frac{\tau}{T} = \frac{C_i}{C_0} G_I. \tag{2}$$

The power gain of the device can now be written as

$$G_P = G_I G_V = \frac{C_i}{C_0}\left(\frac{\tau}{T}\right)^2. \tag{3}$$

The bandwidth of the device is given by

$$\Delta f = \frac{1}{2\pi\tau}. \tag{4}$$

From Equations (3) and (4),

$$(G_P)^{1/2}\Delta f = \left(\frac{C_i}{C_0}\right)^{1/2}\frac{1}{2\pi T}. \tag{5}$$

Note that in this argument it is assumed that the total input capacitance is between the controlling charge on the grid and the controlled charge introduced into the emitter–collector space. Other sources of input capacitance detract from the performance of the device. Also,

it is assumed that the resistance of the control grid itself is negligible. This is not true in present high-frequency bipolar transistors. Their base resistance is a significant limitation to high-frequency performance. Finally, the collector is assumed to have negligible d-c leakage to other electrodes.

Discussion of Gain–Bandwidth Product

Inspection of Equation (5) shows that a large ratio of C_i/C_0 is advantageous. In most triodes C_i and C_0 are geometrical capacitances determined by electrode dimensions and separations. One would not expect any unusual differences to exist in these parameters for the several types of triodes, provided they have comparable dimensions. The bipolar transistor is the notable exception in that C_i is the sum of a geometrical capacitance (mainly base to emitter) and a diffusion capacitance that ordinarily is many times larger. In fact, the diffusion capacitance represents the high-capacitance limit when controlling and controlled charge are made to approach each other and to occupy finally the same physical space.

These considerations led Johnson and Rose[1] to single out the bipolar transistor as having a special advantage over other triodes. The argument, however, is not complete for the following reason. C_i is proportional to the base thickness, d. The transit time (through the base) is proportional to d^2. Consequently if one reduces the base thickness, more is gained from the shorter transit time than is lost by the smaller value of C_i. In fact it is profitable to reduce the base width at least until the transit time across the base is as small as the transit time between emitter and base or base and collector. We show below that, under these conditions, the diffusion capacitance becomes equal to the geometric capacitance between base and emitter, the geometric capacitance being that across a Debye length. The meaning of this result is that even though the controlling and the controlled charges (electrons and holes) occupy the same physical space in the base, the effective geometrical spacing to be associated with the diffusion capacitance is a Debye length of the minority carriers. Hence the diffusion capacitance can be matched in a unipolar device such as the field effect transistor by scaling the critical dimensions down to a Debye length. The net result is that the high input capacitance of the bipolar transistor does not lead to higher gain–bandwidth products than can be achieved by other triodes.

It remains then to examine the transit time, T, for the separate devices. It will be shown that this transit time can be traced in all

cases to an RC time constant, a transit time across a depletion layer, or a transit time across a space-charge-limited current element. Further, it will be shown that these three times are identical (assuming the drift velocity of carriers does not saturate) for materials having the same conductivity and dielectric constant—that is, for materials having the same dielectric relaxation time ($\tau_{rel} = (K/(4\pi\sigma)) \times 10^{-12}$ sec).

The conclusion then follows that *the upper limit of frequency response of all of the triode devices is the dielectric relaxation time of the material as used in the device.* It goes almost without saying that lower performance can result from improper design or operation. Further, the ease of realizing the maximum performance may differ among the several devices for significant technological reasons.

By way of calibration, the dielectric relaxation time of one-ohm-cm material is about 10^{-12} second.

Analysis

It is first shown that $T = RC$ for both a depletion layer and for a space-charge-limited current element.

The thickness of a depletion layer is given by

$$Q = CV \tag{6}$$

or

$$ned \doteq \frac{K}{4\pi d} V \times 10^{-12}, \tag{7}$$

where Q is the charge per cm^2 in the depletion layer, C its capacitance, and V the voltage step across the layer. V is the sum of the contact potential and the applied voltage, d is the thickness of depletion layer, K is the relative dielectric constant, and n is the volume density of of "available" charge. "Available" means free to move within the time of the experiment, and includes both free and trapped carriers. From Equation 7,

$$d^2 = \frac{K}{4\pi ne} V \times 10^{-12}, \tag{8}$$

and

$$T = \frac{d^2}{V\mu} = \frac{K}{4\pi ne\mu} \times 10^{-12} \text{ second.} \tag{9}$$

Also, for a leaky capacitor it is known that

$$RC = \frac{K}{4\pi\sigma} \times 10^{-12} = \frac{K}{4\pi ne\mu} \times 10^{-12} \text{ second.} \tag{10}$$

From Equations (9) and (10) it is concluded that $T = RC$. The error in regarding the depletion layer as a simple, rather than distributed, capacitor is less than a factor of 2, and enters in a self-cancelling manner in the computation of both T and RC.

Next it is shown that $T = RC$ for a space-charge-limited current element. The free charge introduced by the applied voltage in a space-charge-limited diode is

$$Q = CV. \tag{11}$$

The corresponding free carrier density is given by

$$Q = ned = \frac{K}{4\pi d} V \times 10^{-12}. \tag{12}$$

From Equation (12),

$$T = \frac{d^2}{V\mu} = \frac{K}{4\pi ne\mu} \times 10^{-12} = RC. \tag{13}$$

The transit times for the several triodes will now be examined individually beginning with the bipolar transistor.

Bipolar Transistor (Figure 2)

For simplicity we begin with a bipolar transistor in which the thickness of base has negligible effect on the transit time of carriers from emitter to collector. The implications of this assumption will be discussed later. Also, let the recombination lifetime for carriers in the base be large relative to the reciprocal of the frequency of operation.

If a positive charge is now added to the base (emitter is grounded), negative charge will be drawn in from the emitter to neutralize it. The time required for this neutralization is the RC time constant of the emitter–base electrodes considered as a simple capacitor. Since the negative charge drawn in from the emitter does not remain in the base, but is passed on to the collector, the ratio of total charge passed

to the charge on the base is

$$\frac{Q_{\text{coll}}}{Q_{\text{base}}} = \frac{\tau}{RC}, \tag{14}$$

where $\tau = 1/(2\pi f)$ and f is the operating frequency. Equation (14) also represents the current gain because both Q_{coll} and Q_{base} are referred to the same element of time, τ.

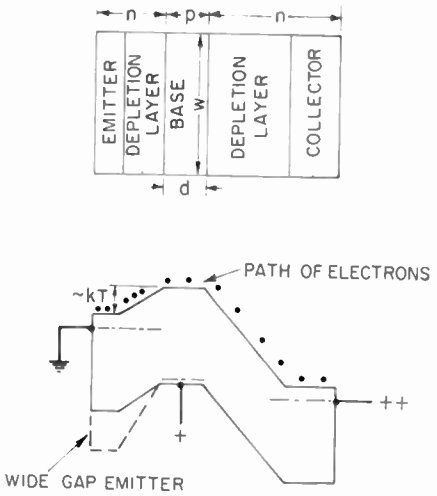

Fig. 2—Bipolar transistor. The relative dimensions have been chosen to fit the preferred arrangement discussed in the text. The wide-gap emitter needed to permit a highly conducting base is shown in dashed outline.

The resistance R between emitter and base is localized mainly in the last kT rise in potential in the depletion layer bordering the base. This resistance is reduced exponentially since the emitter is forward biased. Hence, it is of advantage to operate with the conduction band of the emitter within about kT of the conduction band of the base. Under these conditions the RC of the material lying between emitter and base is given closely by the dielectric relaxation time of the emitter material, namely,

$$RC = \frac{K}{4\pi\sigma_{\text{emitter}}}. \tag{15}$$

From Equations (14) and (15) it is seen that the characteristic

transit time that is to be inserted into Equation (5) (the general relation for gain–bandwidth product) is

$$T = RC = \frac{K}{4\pi\sigma_{\text{emitter}}}. \tag{16}$$

In arriving at Equation (16) it has been assumed that the transit time across the base is less than the time cited in Equation (16) for transit of charge from emitter to base. Since by Equation (9), the RC time of Equation (16) is also the transit time of carriers through the depletion layer when a potential of kT/e is applied, and since the effective potential across the base layer for the transit of carriers through the base is also kT/e, it follows that the base thickness should be less than the depletion layer thickness in order that the transit time through the base be less than the RC of the emitter–base depletion layer.

The same criterion, base thickness less than depletion layer thickness, is also the criterion for ensuring that the diffusion capacitance of the base is less than the geometric capacitance between emitter and base. This can be seen from the following two relations:

$$\text{diffusion capacitance} = \frac{(ned)_{\text{base}}}{kT/e} \tag{17}$$

geometric capacitance (from Equations (6) and (7))

$$= \frac{(ned)_{\text{depletion}}}{kT/e}. \tag{18}$$

The free-carrier densities n in Equations (17) and (18) are very nearly the same since the emitter and base conduction bands are within kT of each other.

In order that the high-frequency performance given by Equation (16) be realized it is, of course, important that there be no other time-limiting processes. If the collector is made of material at least as conducting as the emitter, then by Equation (9) the transit time from base to collector will be at least as short as that from emitter to base. This statement is based on a nonsaturated drift velocity. If the drift velocity is saturated, the transit time in the collector region can exceed that in the emitter region. The series resistance of emitter and collector leads will not impose limitations provided the thickness of emitter and collector layers in series with their respective depletion

layers is less than that of the depletion layers. (Alternatively, of course, these series layers could be designed to be thicker but proportionately more conducting, i.e., by diffusion or epitaxial growth.) The series resistance to the base layer, namely, the sheet resistance of the base, is a more serious problem. Here the conductivity of the base must exceed the conductivity of the emitter by the product of their aspect ratios, that is, the ratio of width to thickness. But this is highly unfavorable for emitter efficiency. The latter requires that the conductivity of the base be actually *less* than that of the emitter. One can still think in terms of a highly conducting base without adverse effect on emitter efficiency provided the forbidden gap of the emitter is appreciably larger than that of the base. Once one admits the high-band-gap emitter into the design possibilities of a bipolar transistor, one has only a short step to make to arrive at the Barristor—an essentially majority-carrier device.

In summary, one can achieve the high-frequency limit of a bipolar transistor given by the RC of its emitter provided a high-band-gap emitter is used and provided the thickness of emitter and base materials is not more than twice the thickness of their respective depletion layers.

Barristor (Figure 3)

It is now relatively easy to discuss the Barristor in terms of the arguments already detailed for the bipolar transistor. The characteristic time governing the high-frequency performance is again the RC time constant between emitter and grid.

No other limiting times enter in, since the same arguments used for the bipolar transistor hold here. The thickness of emitter and collector layers should be no greater than twice the thickness of their respective depletion layers. The conductivity of the collector should be at least as large as that of the emitter. The transit time of carriers through the metal grid will be negligible since the thickness of metal grid should be less than a few tens of angstroms to permit a high transparency for carriers going from emitter to collector. Since the metal grid is so much thinner than the emitter depletion layer, its conductivity must be correspondingly higher. In fact, to avoid limitation by the sheet resistance of the metal grid, the conductivity of the grid must be as large as

$$\sigma_{\text{grid}} = \sigma_{\text{emitter}} \frac{W^2}{d_{\text{grid}}\, d_{\text{depletion layer}}};$$

W is the sheet dimension of the grid and d_{grid} its thickness.

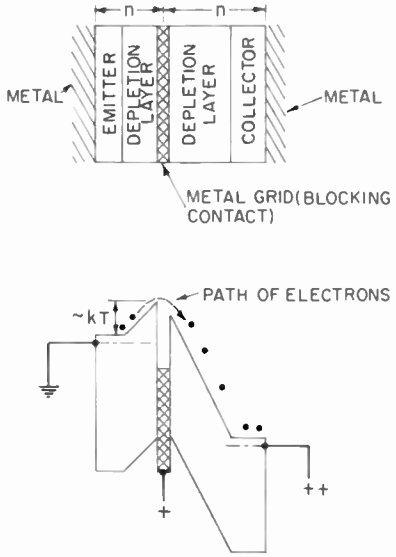

Fig. 3—Barristor. The difference in barrier heights on the two sides of the metal grid is obtained either by using different semiconductors for emitter and collector or by using different metals on the two faces of the grid.

Field-Emission or Tunnel Triode (Figure 4)

It is clear from Figures 3 and 4 that the major difference between the field-emission triode and the Barristor lies in the means of intro-

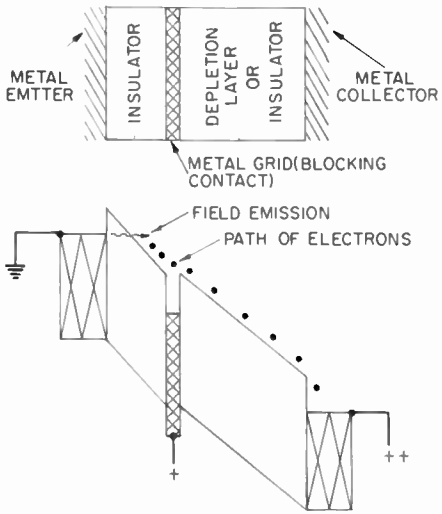

Fig. 4—Field-emission triode. While Mead's proposal used an insulator on the collector side of the grid, a depletion layer can be used as well.

ducing carriers into the emitter–grid space. The field-emission triode does so by causing carriers to tunnel from the emitter into the insulator separating emitter from grid. The barristor does so by the well-known forward bias characteristics of a metal–semiconductor rectifier. While Mead emphasizes the high current density available by field emission from a metal, this advantage is tempered by the difficulty of attaining uniform, nonerratic field emission, and by the questionable need for such high current densities. For example, the Barristor can already, in principle, achieve response times of 10^{-13} second by using

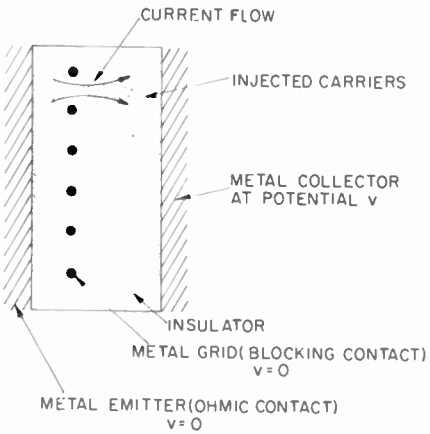

Fig. 5—Space-charge-limited triode. The leakage of the collector field through the grid wires provides the accelerating field at the cathode necessary to cause injection of carriers.

10^{-1} ohm-cm material for its emitter, which implies current densities of the order of 10^{4} amperes/cm^2. It remains to be seen whether such short times are even useable in a triode amplifier.

In brief, the field-emission triode is limited by the same RC time constant in the emitter–grid space as the Barristor and bipolar transistor. The side conditions on the emitter and collector leads as well as on the conductivity of the grid are the same as those for the Barristor.

Space-Charge-Limited Triode (Figure 5)

The space-charge-limited (SCL) triode begins with an insulating material to which electrodes are attached. The space between emitter and grid must be made conducting by the injection of carriers from the emitter. Under conditions of space-charge-limited flow, the transit time between emitter and grid becomes equal (see Equation (13)) to

the *RC* time constant (dielectric relaxation time) of the space between emitter and grid. As in the previous devices, the conductivity of this space becomes the governing parameter for high-frequency performance. It is worth noting from Equations (9) and (13) that the same magnitude of voltage is required to either inject or deplete a given space-charge density of carriers in a given space.

Unipolar Transistor (Figure 6)

The unipolar transistor shown in Figure 6 differs from the usual

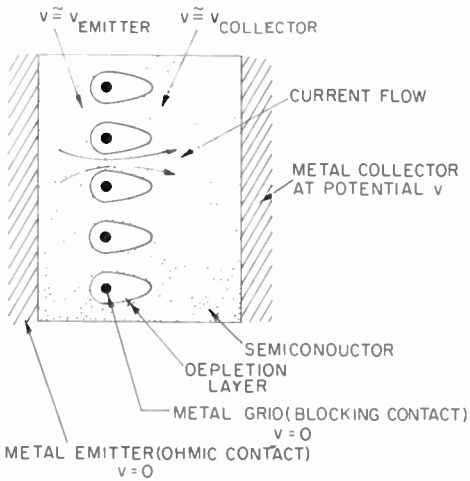

Fig. 6—Unipolar transistor. By virtue of the geometry of current flow, most of the applied voltage lies across the narrow channels.

geometry[5] in that the extent of grid along the direction of current flow is small compared with the separation of grid wires, and also in that there are many grid wires rather than the usual two. The latter extension serves to define a grid plane as in the other devices rather than just a grid line. The use of grid wires rather than long grid plates is not likely to alter the essential physics of the device.

While a quantitative solution for the current flow in the case of grid wires has not yet been carried out, certain significant features of the solution can be estimated with reasonable confidence. Consider the case of grid and emitter grounded and the collector potential high enough to "saturate" the current flowing through the grid plane. Under these conditions

1) The length of constricted channel through which the current

flows is approximately the long dimension of the depletion layer around the grid wires.

2) The potential drop along the channel is approximately the potential drop across the depletion layer. It is also approximately the potential applied to the collector.

From these statements and Equations (9) and (13), one can argue that the potential drop along the channel is almost sufficient to initiate space-charge-limited current flow. (It is not likely that in this geometry the density of carriers in the channel can at all be increased *above* their thermal equilibrium value by an applied voltage, since to do so would normally require a source of carriers close to the channel with an excess density of carriers.) We conclude then that the transit time of carriers from the emitter space to the collector space is given by the dielectric relaxation time of the semiconducting material as in the other four triodes discussed.

General Remarks

It is, of course, not unexpected that the dielectric relaxation time of the space between cathode and grid should be the controlling parameter for high-frequency performance. The same conclusion couched in terms of conductivity or current density is well known for vacuum triodes. Also, the current-gain–bandwidth product for trap-free photoconductors[7] has been shown to be equal to the (dielectric relaxation time)$^{-1}$ of the photoconductor. The dielectric relaxation time is, by definition, the time required for a perturbation in charge or electric field in a medium to decay. It should measure the upper limit to the speed at which the medium can respond to changes in charge or field.

The current-gain–bandwidth product of trap-dominated photoconductors was obtained in the form

$$G_f \frac{1}{\tau} = \frac{1}{\tau_{rel}} M,$$

where τ is the response time to varying light signals, and τ_{rel} is the dielectric relaxation time. M is a factor dependent upon the energy distribution of traps and recombination centers. Its value is usually unity but it may greatly exceed unity for special trap distributions. The last statement may appear to contradict the expectation that the

[7] A. Rose and M. A. Lampert, "Gain–Bandwidth Product for Photoconductors," *RCA Review*, Vol. 20, p. 57, March 1959.

dielectric relaxation time is the fastest response time of a medium. The apparent contradiction is resolved by recognizing that it is the conductivity of the emitter–grid space that is significant. By contrast, the grid–collector space may be made considerably less conducting than emitter–grid space by increasing the collector voltage. This can be seen by inspection of the bipolar transistor or Barristor figures. When the bipolar transistor or Barristor is used as a photoconductor by allowing the grid to float, the distinction between these two spaces is more clearly resolved, and M becomes unity for the emitter–grid space and greater than unity if the grid–collector space is included.[8] In the case of the photoconductor the two spaces are not clearly separated. The emitter–grid space may be regarded as the space between emitter and virtual cathode. The rest of the space — the bulk of the photoconductor — may be regarded as the grid–collector space. The somewhat confusing feature is that the grid controlling charge is generated by optical excitation throughout the bulk of the photoconductor, that is, in the grid–collector space.

At first glance there appear to be large differences between the several triodes sketched in Figures 2-6. One can de-emphasize these differences by starting with the Barristor, for example, and noting the small changes required to convert it into any of the other devices. If the metal grid is replaced by a degenerate p-type semiconductor, the Barristor becomes essentially the wide-gap-emitter bipolar transistor. If the metal is apertured instead of continuous, the barristor becomes a form of unipolar transistor. If, together with the apertured grid, the semiconductors are replaced by insulators, the Barristor becomes a space-charge-limited triode. The kinship of Barristor and field-emission triode has already been noted and is apparent by inspection.

ACKNOWLEDGMENT

The writer is indebted to H. S. Sommers, Jr. and P. K. Weimer for critical readings of this manuscript.

[8] A. Rose, "Maximum Performance of Photoconductors," *Helv. Phys. Acta*, Vol. 30, p. 242, 1957.

THE FIELD-EFFECT TRANSISTOR—A REVIEW

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Summary—The special features of the unipolar field-effect transistor are reviewed. Recently three factors have contributed to make it emerge from previous obscurity: a) advancements in semiconductor physics and technology making fabrication of field-effect structures practical, b) new technical features such as evaporated construction and insulated gate, c) need to complement bipolar transistors whose performance is insufficient in many applications such as high input impedance or lateral symmetry applications. Because of this situation the technical possibilities of unipolar field-effect transistors as active devices and as building blocks for integrated circuits are reassessed. A bibliography, arranged chronologically, is included at the end of the paper.

Introduction

In 1935 Oskar Heil of Berlin obtained a British patent (see bibliography, Ref. (1)) on "Improvements in or Relating to Electrical Amplifiers and Other Control Arrangements and Devices." Figure 1 of this patent is shown here. The light area marked 3 is described

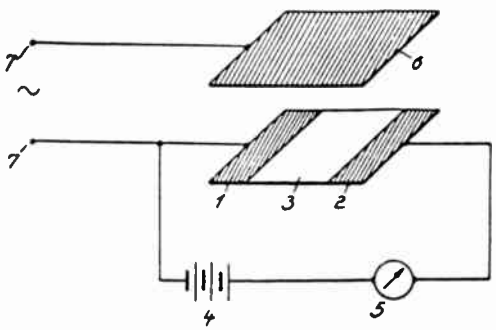

Fig. 1—Drawing from Brit. Patent 439,457, inventor—O. Heil.

as a thin layer of a semiconductor such as tellurium, iodine, cuprous oxide, or vanadium pentoxide; 1 and 2 designate ohmic contacts to the semiconductor. A thin metallic layer marked 6, immediately adjacent to but insulated from the semiconductor layer, serves as control electrode. Heil describes how a signal on the control electrode modu-

lates the resistance of the semiconductor layer so that an amplified signal may be observed by means of the current meter, 5. In modern terminology, one might describe this device as a unipolar field-effect transistor with insulated gate.

In 1952, W. Shockley (Ref. (3)) described a unipolar field-effect transistor with a control electrode consisting of a reverse-biased junction, shown in Figure 2. Such transistors were subsequently built and

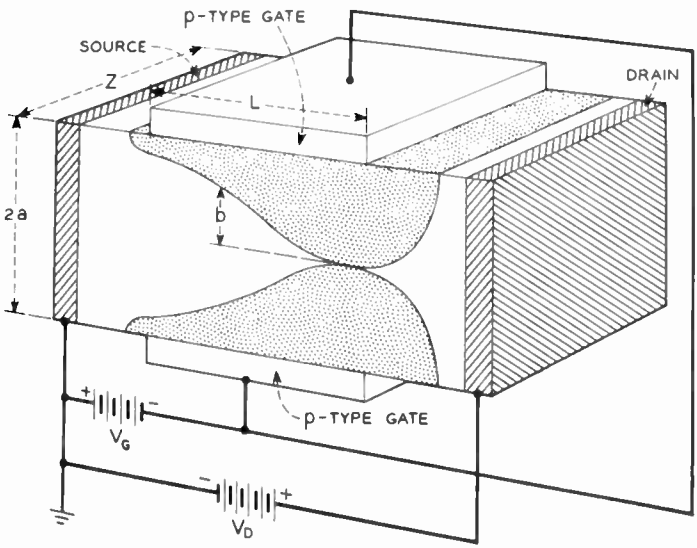

Fig. 2—Schematic diagram of unipolar field-effect transistor according to Shockley (Ref. (3)).

tested according to G. C. Dacey and I. M. Ross (Ref. (5)), who also added an analytical treatment of the performance limits of such devices in 1955. Until recently, however, the field-effect transistor remained in the laboratory.

Three factors have since contributed to the emergence of the unipolar field-effect transistor from previous obscurity. The first of these factors is the understanding of semiconductor physics and the related advance of semiconductor technology which now makes it possible to fabricate devices with predictable performance. The second is the addition of new technological features, such as fabrication by evaporation as described by P. K. Weimer (Ref. (24)), and particularly the insulated-gate construction described by S. R. Hofstein and F. P. Heiman (Ref. (54)), and others (Ref. (18) and (20)), which promise much improved performance over the reverse-biased-junction gate

construction. The insulated-gate construction is shown in cross section in Figure 3. The third factor is the very considerable extent to which transistorization of electronic equipment has now progressed. In this situation it becomes increasingly annoying to find a number of functions where the bipolar transistor falls far short of devices such as electron tubes, making complete transistorization impractical or uneconomical. Therefore a need has arisen for a transistor with the characteristics of the field-effect transistor to complement the bipolar transistor in particular applications.

The present paper summarizes the characteristics and the performance limits of field-effect transistors to the extent that they are different from those of bipolar transistors and are useful in applications.

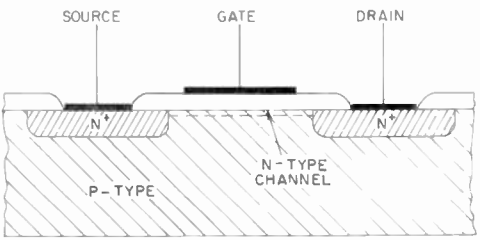

Fig. 3—Schematic diagram of insulated-gate field-effect transistor (Ref. (54)).

Active-Device Characteristics

Input Impedance

The most obvious feature of the field-effect transistor is its high input impedance. The saturation current drawn by the reverse-biased gate of a germanium field-effect transistor with typical resistivity and dimensions amounts to about 1 μa, corresponding to an input resistance of the order of 1 megohm at the operating point at room temperature. For a silicon transistor, the current is about 10^3 times smaller and the input resistance is consequently about 10^9 ohms at room temperature. The saturation current increases by about one order of magnitude for a rise in temperature of 30–50°C. Therefore, when appreciable power is dissipated or the cooling is insufficient, the input resistance may decrease. In contrast, the insulated-gate field-effect transistor has a gate input resistance of 10^9 to 10^{15} ohms. The latter value is so high that when a charge is deposited on the gate, it takes a period of at least several days for the leakage of charge to be detected by observing the change in current on the output side.

Also associated with the junction gate is an input capacitance which has a value of 20–100 picofarads at a transconductance of 1000–3000 μmhos for most field-effect transistors now commercially available. This capacitance can be made considerably smaller for the insulated gate than for a reverse-biased junction, and is typically 1–2 picofarads for the same transconductance. A breakdown of the factors that contribute to this capacitance is obtained from the equivalent circuit for such a transistor shown in Figure 4. The capacitances in

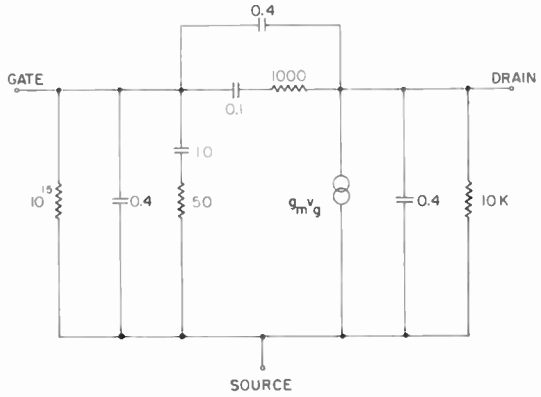

Fig. 4—Equivalent circuit of experimental insulated-gate field-effect transistor.

the stem between leads and the contact areas amount to about 0.4 picofarad. In the device itself, the capacitance between drain and gate (feed-back capacitance) is less than 0.1 picofarad while the gate-to-source capacitance is about 1 picofarad for a device with a transconductance of 1500 μmhos.

Current–Voltage Characteristics

Current–voltage characteristics obtained on a curve tracer for four different field-effect transistors are shown in Figure 5: (a) a silicon junction device, (b) a silicon insulated-gate depletion type, (c) an evaporated cadmium sulfide device, and (d) a silicon insulated-gate enhancement type. For comparison, all devices were operated with positive and negative drain voltage and with positive and negative gate voltage, although the junction input device is not designed for the dual mode of operation. When the gate has no bias ($V_g = 0$) transistors (a) and (b) draw a large drain current, while transistors (c) and (d) draw negligible current, typically less than 1 μa. When the gate is biased positively, transistor (a) quickly saturates as the

gate resistance becomes very low. In Figure 5 this results in an apparent voltage offset at $I_d = 0$, because of the construction of the curve tracer. When V_d is negative, the point at which the gate becomes forward biased shows up as a kink in the curves where they cross the dashed line. The decrements in drain current for increments in nega-

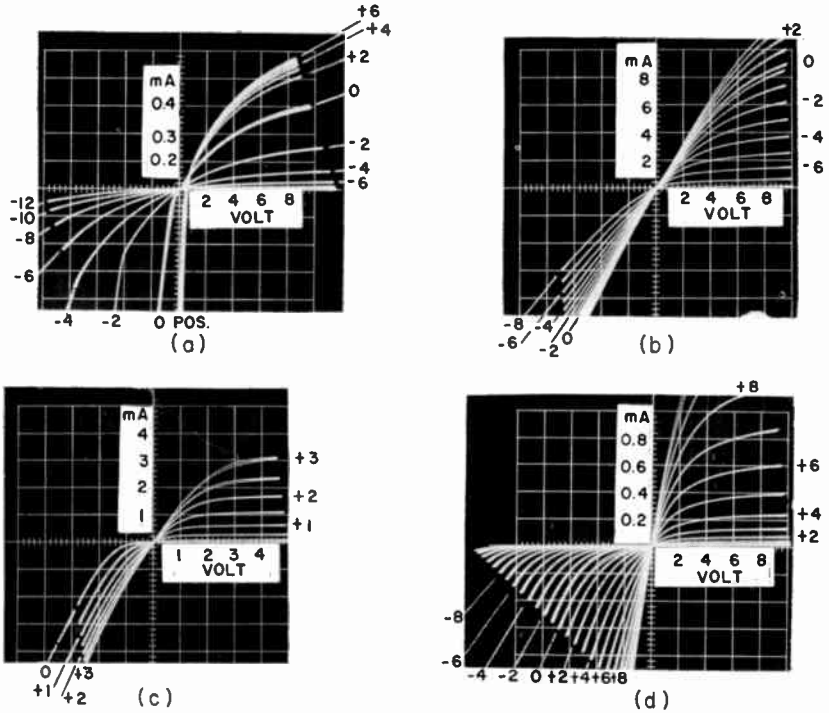

Fig. 5—Curve-tracer pictures of drain current versus drain voltage with gate voltage as parameter for several field-effect transistors: (a) silicon, junction gate, (b) silicon, insulated gate, depletion mode, (c) cadmium sulfide, insulated gate, enhancement mode, and (d) silicon, insulated gate, enhancement mode.

tive gate voltage decrease rapidly in case (a) which may also be expressed as a transconductance that varies strongly with gate bias. In cases (b), (c), and (d) the decrements in drain current for the same increments in gate voltage are uniform over a large range, or, in other words, the transconductance is nearly constant over a large range of current.

Frequency Response

The frequency response of field-effect transistors has been analyzed

by Dacey and Ross (see bibliography, Ref. (7)), who concluded that the response would be limited in germanium by the fact that the carrier mobility saturates beginning at a critical field of about 10^3 volt cm^{-1}. Higher fields would require such excessive power dissipation that it would be difficult to remove the generated heat. A comparison, based on this finding, between field-effect transistors and bipolar transistors was made by Early* and indicated a superiority in frequency response of the bipolar transistor over the field-effect transistor by a factor of ten. However, a later analysis by Rose† has indicated that the same physical phenomenon, the dielectric relaxation time of the material between the emitter and the control, limits the frequency response of all solid-state triodes—bipolar, field-effect transistors, field-emission triodes, and space-charge-limited triodes. If, instead of the critical velocity, the thermal velocity is accepted as an upper limit to the velocity of the carriers in field-effect transistors, the frequency response is indeed the same for bipolar transistors and field-effect transistors. The limiting frequency is then given by

$$f = \frac{6 \times 10^6}{L},$$

where L is the length of the gate, in centimeters, in the direction of current flow. In bipolar transistors L is the emitter stripe width (or the emitter-to-base spacing). In practical devices stray reactances that are difficult to avoid lower this figure considerably.

Figure 6 shows the gain–bandwidth figure, F, for a number of commercial field-effect transistors, where

$$F = \frac{g_m}{2\pi C_{\text{gate}}},$$

and C_{gate} is the total gate capacitance with drain and source grounded. Each horizontal line denotes a different manufacturer. The data has been obtained from commercial data sheets which usually give a maximum and a minimum transconductance with a typical value in between. This explains the ranges shown in Figure 6. The bottom line gives values for insulated-gate field-effect transistors; (A) denotes silicon

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* J. M. Early, "Structure-Determined Gain-Band Product of Junction Triode Transistors," *Proc. I.R.E.*, Vol. 46, p. 1924, Dec. 1958.

† A. Rose, "An Analysis of Gain-Bandwidth Limitations of Solid State Triodes," *RCA Review*, Vol. 24, p. 627, Dec. 1963.

units, which have a higher frequency response than commercial field-effect transistors, which all have junction input, and (B) denotes laboratory results for evaporated cadmium sulfide units. The difference in frequency response reflects the fact that carrier mobility in cadmium sulfide is lower than in silicon.

The insulated-gate field-effect transistor exhibits a higher gain–bandwidth product than junction-input types because it is easier to fabricate a short gate with the insulated-gate technology than with junction-gate technology.

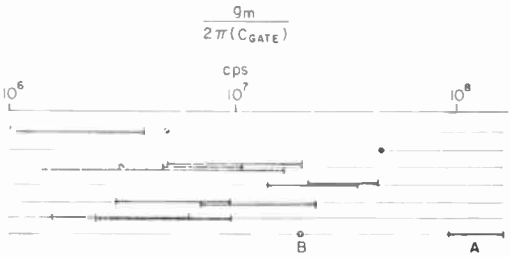

Fig. 6—Gain–bandwidth figure of merit for field-effect transistors. "A" indicates experimental silicon insulated-gate units, "B" experimental cadmium sulfide insulated-gate unit.

Because the field-effect transistor is a majority-carrier device, it does not exhibit carrier storage in switching applications. The switching speed is determined entirely by the RC time constant of the gate capacitance charging through the channel resistance. With a low-impedance driver, switching times as low as a fraction of a nanosecond have been observed, but for one field-effect unit driving another, switching times of 10-20 nanoseconds are more realistic at present.

Bilateral Symmetry, Offset Voltage

Many field-effect transistors are at the present time made symmetrical, with source and drain interchangeable. Although bipolar transistors can also be made symmetrical, this results in a sacrifice in performance. It is believed that, in the long run, the same will prove true for the field-effect transistor. For example, since the source series resistance gives a strong negative feedback and also contributes to the noise of the unit much more than the drain series resistance, it is advantageous to offset the gate towards the source electrode, gaining performance but sacrificing symmetry.

In contrast to bipolar transistors, the field-effect transistor has

no voltage offset. As may be seen in Figure 7, which shows the central portion of the current–voltage characteristics greatly magnified, the curves are monotonic through the origin. For voltages sufficiently small compared to the pinch-off voltage, the curves are approximately linear. The resistance values obtained range from a minimum of $1/g_m$, i.e., about a few hundred ohms, to the resistance of a reverse-biased junction (the drain junction) of about a few hundred megohms.

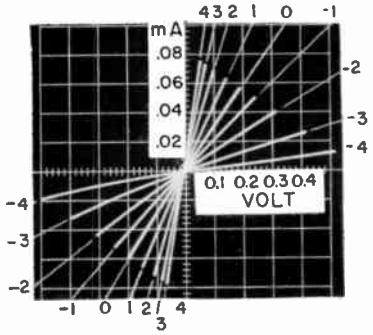

Fig. 7—Curve-tracer picture of drain current versus drain voltage with gate voltage as parameter for low drain voltages.

Radiation Tolerance

Because the field-effect transistors are majority-carrier devices, lifetime degradation is immaterial, and these transistors may therefore be expected to tolerate higher radiation doses than bipolar transistors. Dosages up to a value where either mobility or doping level change are tolerable, generally about ten times the dose for which lifetime begins to deteriorate. One would, therefore, expect field-effect transistors to tolerate about ten times higher radiation dose than bipolar transistors of comparable dimensions. At present very little data is available on radiation tolerance of field-effect transistors. Existing data has been summarized in Table I. It is well known that to make bipolar transistors radiation immune, one should use semiconductor material in which the lifetime is initially very low and make the base region very narrow. However, the same method may be adapted to field-effect transistors by using material which initially has very low mobility and high doping level. Therefore, it seems probable that the potential advantage of about ten times in radiation tolerance will remain.

Table I—Neutron Dose, n/cm², to Reduce Transconductance of Unipolar Field-Effect Transistor to 70% of Initial Value (it is assumed that damage is linear with dose; 1 MeV electron = 10^{-2} n/cm²).

Type	Semi-conductor	Number of Units Tested	Dose (n/cm²)
Junction Gate*	Si	3	1×10^{14}
Junction Gate*	GaAs	1	4×10^{15}
Junction Gate†	Si	–	3×10^{13}
Junction Gate‡	Si	3	1×10^{13} to 6×10^{13}
Insulated Gate depletion type‡	Si	3	1×10^{13} to 3×10^{14}
Insulated Gate enhancement type‡	Si	3	3×10^{14}

* Kulp, Jones, and Vetter, Ref. (21).
† Quarterly Progress Report #6, AF(616)-6278, Westinghouse Electric Corp.
‡ Measurements made at RCA.

Noise Behavior

While the main noise source in bipolar transistors is the shot noise connected with the flow of minority carriers, the main source of noise in field-effect transistors is the thermal noise in the output resistance. A summary of the different noise mechanisms which are important in field-effect transistors is shown in Figure 8. In addition to the thermal noise there are a number of other noise sources which may

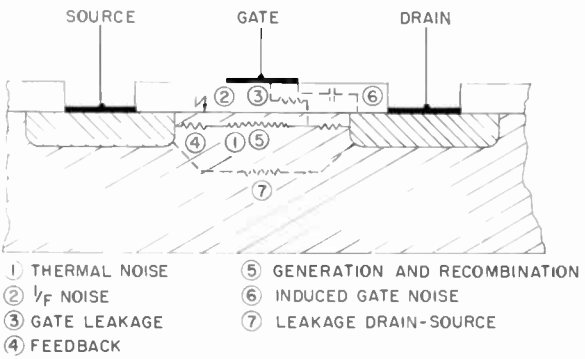

Fig. 8—Schematic picture of noise sources.

or may not be important depending upon the construction. At low frequencies 1/f noise appears. In field-effect transistors with junction input, the 1/f noise is greater than the thermal noise below about 100 cps. In insulated-gate transistors the 1/f noise is, as yet, quite large, and exceeds thermal noise at frequencies as high as several mc. Whether or not this may be improved in the future is not yet known. At high frequencies the drain-to-gate feedback capacitance causes thermal noise to be fed back to the gate and be amplified. However, since the signal is also fed back, the signal-to-noise ratio is, to a first approximation, unchanged. In the source end of the channel a source resistance constitutes an unbypassed resistance, the thermal noise of which appears in the input and becomes amplified. As a resistance in the drain lead does not have this disadvantage, it may be desirable to offset the gate towards the source. If the gate insulation is defective, the corresponding leakage current through the oxide gives rise to very strong noise. Also, leakage current from drain to source through, on the surface of, or outside the semiconductor gives noise.

The noise figure of a field-effect transistor is only a few tenths of a db at moderate frequencies and with sufficiently high input resistance, e.g., 3 megohms. Since the noise figure varies with the input resistance it is more convenient to use an equivalent noise resistance as is done for electron tubes. The equivalent noise resistance for a field-effect transistor is

$$R_{eq} \approx \frac{0.5}{g_m}.$$

One of the main degradation phenomena in bipolar transistors during use is lifetime deterioration. As this phenomenon is of no consequence in field-effect transistors, the prospect for life and reliability is correspondingly better.

Choice of Material

Another consequence of majority-carrier conduction is the large number of semiconductor materials which are potentially useful for field-effect transistors but not for bipolar transistors. This is borne out by Figure 9, which shows at left the semiconductors that have been used for bipolar transistors, and at right some of the common semiconductors that are potentially useful for field-effect transistors. The criteria for usefulness are either (a) that both p- and n-type materials can be made, so that a channel can be properly isolated from the bulk or from the gate, or (b) that the resistivity can be made

sufficiently high to prevent an induced channel on the surface from being shunted through the bulk by conduction. The Shockley-type field-effect transistor is an example which satisfies the first criterion, while the insulated gate field-effect transistor is an example which satisfies the second criterion. While very few semiconductor materials are at the present time useful for bipolar transistors, the opposite is true of field-effect transistors.

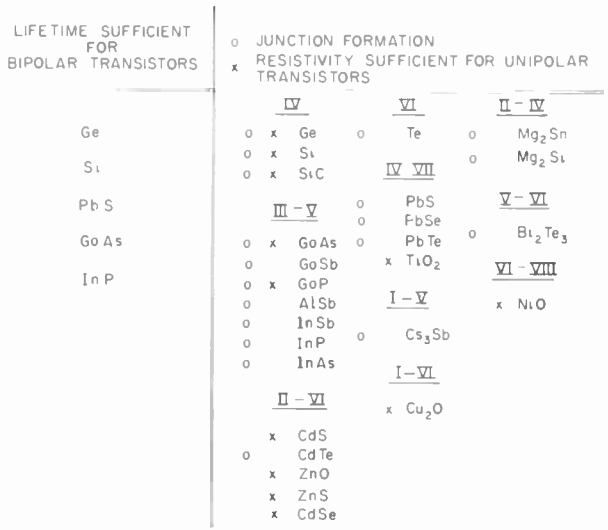

Fig. 9—Semiconductors which are potentially useful for bipolar and for unipolar transistors.

Therefore, when it comes to making transistors for special purposes requiring a particular semiconductor, it will frequently be necessary to resort to field-effect structures. Consider, for example, the necessity for using wide-band-gap materials such as silicon carbide, gallium arsenide, or cadmium sulfide in transistors for high-temperature operation. Another example is the fabrication of transistors by evaporation or plating in which case the short lifetime in the semiconductor does not permit bipolar principles to be used. A final example is that use of the thin-film structure permits fabrication of high-frequency performance transistors from semiconductors with extremely high mobility, such as InSb or InAs, without the need for a reduction of dimensions.

One factor that has not been discussed, although of central importance in insulated-gate field-effect transistors, is the surface. Whether all the listed semiconductors can be given a surface suffi-

ciently free of traps for satisfactory transistor performance is not yet known.

Thermal Stability

The temperature dependence of the characteristics of field-effect transistors is related to the majority-carrier mobility. In silicon in the resistivity range used for field-effect transistors, the mobility is proportional to the (absolute temperature) $^{-3/2}$ characteristic of lattice

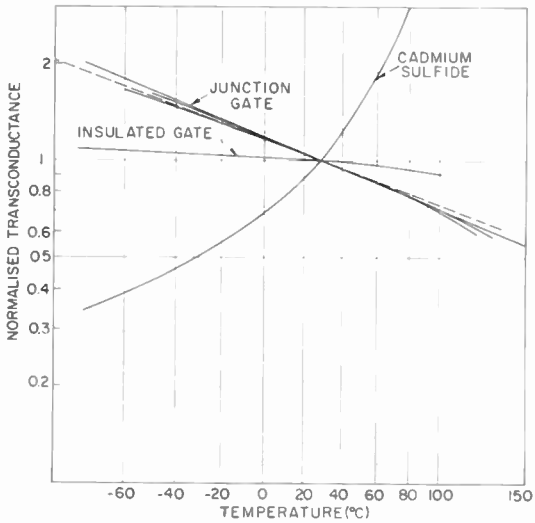

Fig. 10—Transconductance versus temperature for (a) silicon, junction gate, (b) silicon, insulated gate, and (c) cadmium sulfide, insulated gate.

scattering. This relation is shown in Figure 10 as a dashed line. The same figure shows curves of g_m versus temperature taken from data sheets for four different makes of silicon field-effect transistors which, within the accuracy of the data, all fall on this line. The same temperature dependence is obtained for the current at constant voltages. Figure 10 also shows data for a thin-film transistor of evaporated cadmium sulfide. In this case the temperature dependence is much larger, and the temperature coefficient is positive instead of negative. The evaporated cadmium sulfide layer is known to consist of many small crystallites with a large number of defects and grain boundaries. Therefore, in addition to lattice scattering, there is a considerable amount of surface and defect scattering which explains the different temperature dependence.

In the case of the insulated-gate field-effect transistor, which is

also shown in Figure 10, the temperature dependence is very small. In this transistor the current passes very close to the surface where the mobility is reduced by surface, and perhaps defect, scattering; it is therefore tempting to ascribe the small temperature dependence to a fortuitous balance of two effects with opposite temperature dependence, namely the lattice scattering with negative temperature coefficient and surface scattering with positive temperature coefficient. If this is so, it should be possible to accomplish an even closer balance for specific purposes, perhaps to the point where active devices may be obtained with the same small temperature coefficient that usually characterizes passive components, i.e., a few hundred parts per million per degree centigrade.

Another aspect of thermal stability is freedom from thermal runaway in field-effect transistors. In bipolar transistors the collector current increases with increasing temperature to the point where thermal runaway takes place and the transistor is destroyed. This is particularly troublesome in power transistors. In field-effect transistors (although at the present time not in thin-film transistors) the current decreases with increasing temperature, reducing the dissipated power and preventing thermal runaway.

Characteristics of Field-Effect Transistors in Integrated Circuits

Geometry

Bipolar transistors are difficult to incorporate into integrated circuits, partly because the current flow is perpendicular to the surface while the preferred circuit construction is in the plane of the surface, and partly because the carrier lifetime must be maintained. In contrast, the field-effect transistor is naturally a plane surface device with no requirement on carrier lifetime and which therefore can be easily used in integrated circuits. An integrated circuit using sixteen field-effect transistors is shown in Figure 11. The transistors are aligned in four rows of four each with one source (or drain) in common for each neighboring pair of units. The interconnections are deposited on the surface of the silicon wafer and are insulated from the active parts by an oxide layer. Another attractive feature of the field-effect transistor in this application is that a transistor is in effect a resistor and may with advantage be used as such in circuits. Such "resistors" are highly nonlinear, a characteristic that is usually advantageous in digital circuits.

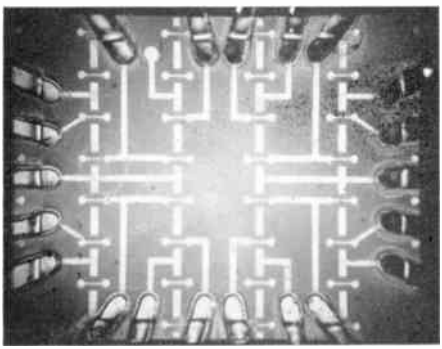

Fig. 11—Integrated circuit using four rows of interconnected field-effect transistors (Ref. (54)).

Digital Circuit Features

Another feature useful in digital circuits is the fact that an enhancement-type field-effect transistor is in itself an inverter. Figure 12a shows a transistor stage with a "low" input (no or negligible current flowing through the device) and, therefore, a "high" output. With a high input, as shown in Figure 12b, considerable drain current flows and the output is low. The voltages are identical and of the same polarity, so that direct coupling may be used.

A unique circuit, which uses pairs of field-effect transistors with complementary symmetry and makes logic possible without drawing any current except during switching, has recently been described (Figure 13). When the input potential is high, the top unit is cut off and the output potential is high. When the input is low, the bottom unit is cut off and the output is low. In neither position does the pair draw current since one unit in the series chain is always cut off. Only in the transition between states is current drawn.

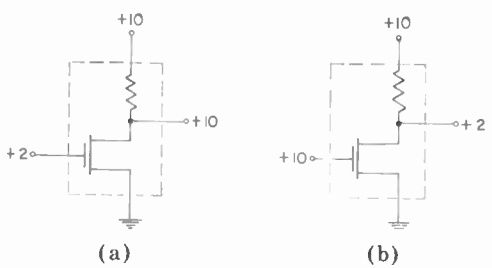

Fig. 12—Field-effect transistor inverter circuit (a) with OFF and (b) with ON signal on the input.

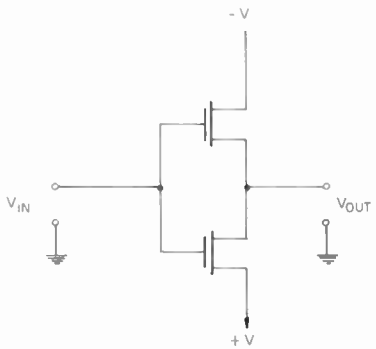

Fig. 13—Bistable circuit drawing no power except when switched.

Redundancy

In large integrated circuits the use of redundancy becomes more and more attractive the larger the circuit. One of the simplest ways to introduce redundancy is through the use of series–parallel four-groups, as shown in Figure 14a. Each element is replaced by a group of four identical elements, and the four-group performs the intended circuit function even if one, two, or even three of the elements in the group become faulty. With conventional bipolar transistors, such four-groups are not very efficient because a short circuit between input and output allows current flow between adjacent four-groups and interferes with the functioning of the redundancy. With field-effect transistors, however, redundancy in the form of four-groups is quite effective. Because of the high input resistance, there can be introduced in the gate lead a resistor large enough to protect against excessive current and, at the same time, small enough not to reduce the speed

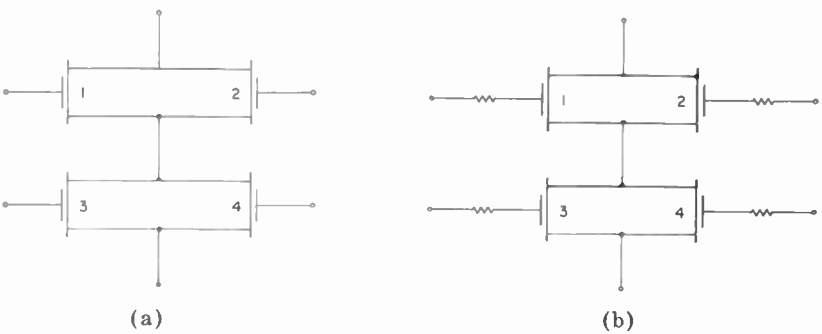

Fig. 14—(a) Redundant four-group and (b) redundant four-group with gate resistors (Ref. (42)).

of the circuit appreciably. A typical value may be 10^4 ohms. A redundant circuit of this type is shown in Figure 14b.

Multiple Units

Special advantages may be obtained by combining the functions of two or more units in a manner analogous to that in which special advantages may be obtained in electron tubes by introducing more than one grid. Figure 15 shows a simple combination of two series-connected units which reduces the feedback capacitance. Just as extra

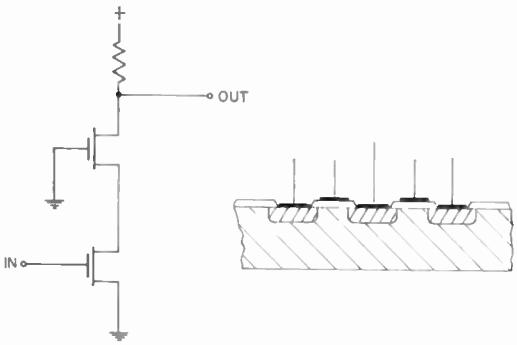

Fig. 15—Field-effect transistor cascode.

grids in electron tubes give better performance and lower cost than the use of multiple units, so the combination of two or more field-effect units in one structure may be cheaper and better than the use of several separate units.

Of special interest is the combination of a bipolar and a field-effect transistor which has been described recently. In this unit, shown in Figure 16, the extra field-effect electrode controls the surface potential of the base region and thereby the surface recombination velocity. When the field-electrode potential is positive, the surface potential is also positive and the surface recombination is consequently high. The base bias current is therefore used up for recombination of injected carriers under the field electrode and little is left for biasing the emitter. Therefore, the injected current is low. On the other hand, when the field-electrode potential is negative with respect to the base, the surface recombination is low and all the base bias current is available for injecting carriers from the emitter. Then the current transfer ratio is high.

The tetrode combines the advantages of a bipolar and a field-effect

transistor. However, the device requires that the bipolar characteristics and the field-effect characteristics be controlled at the same time on the same unit. This has led to difficulties in the fabrication, and such units are not yet commercially available.

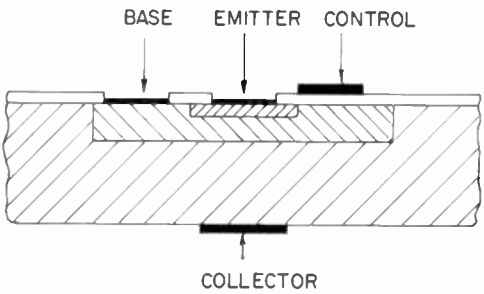

Fig. 16—Semiconductor tetrode using n-p-n transistor (Ref. (22)).

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COPLANAR-ELECTRODE INSULATED-GATE THIN-FILM TRANSISTORS*†

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Summary—*An improved electrode arrangement for the insulated-gate thin-film transistor (TFT) has yielded higher performance and greater ease of fabrication than the earlier "staggered-electrode" structure. "On-to-off" current ratios of 10^7, input resistance exceeding 10^{10} ohms, and gain–bandwidth products of more than 25 megacycles have been obtained with polycrystalline cadmium sulfide films. By depositing all electrodes on top of the semiconductor, greater precision in spacing of electrodes and more freedom in processing and choice of the semiconductor layer is obtained. Well-saturated current–voltage characteristics for both the coplanar and staggered TFT's are in excellent agreement with field-effect analyses. Physical processes affecting the control of the pinch-off voltage and anomalous saturation effects in the gate voltage characteristics are discussed. The effect of different pinch-off voltages upon the characteristics of the TFT operated as a diode is illustrated.*

Introduction

THIN-FILM CIRCUITS incorporating active as well as passive components permit a high versatility of design when the substrate is inert and all components can be deposited in any conceivable order. The cadmium sulfide thin-film transistor (TFT) which has been described in previous papers[1-3] was deposited upon an insulating substrate. These units required the source and drain electrodes to be located on the opposite sides of the thin semiconductor film for best results. It was desirable from the standpoint of ease of fabrication, as well as for maximum versatility in circuit design, to

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† Portions of this paper were presented at the IEEE Device Research Conference, Michigan State University, East Lansing, Michigan, June 1963.

[1] P. K. Weimer, "An Evaporated Thin Film Triode," presented at the Solid State Device Research Conference, Stanford University, California, June 1961.

[2] P. K. Weimer, "The TFT — A New Thin-Film Transistor," *Proc. I.R.E.*, Vol. 50, p. 1462, June 1962.

[3] R. Zuleeg, "CdS Thin-Film Electron Devices," *Solid State Electronics*, Vol. 6, p. 193, March-April 1963.

be able to build the TFT with all electrodes on the same side of the semiconductor.

The present paper describes a coplanar-electrode TFT whose performance is superior to that reported earlier with the "staggered-electrode" structure. While the basic field-effect control mechanism is the same for the coplanar TFT as for the staggered structure, differences in fabrication technology and details of operation have contributed to a more complete understanding of the device. The effect of electrode contacts and the semiconductor–insulator interface upon the characteristics of the TFT are discussed. The control of these

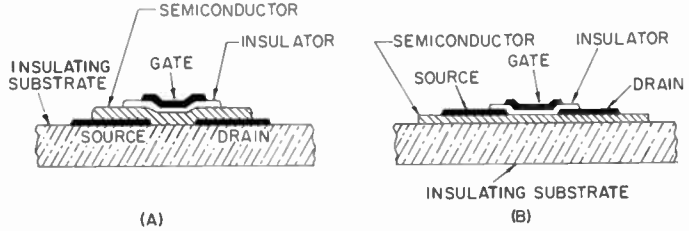


Fig. 1—Cross-sectional drawings of two structures used for thin-film insulated-gate transistors: (a) staggered electrodes and (b) coplanar electrodes.

factors has permitted the design of a novel thin-film field-effect diode which is readily compatible with the TFT in thin-film circuits. Although this discussion refers most frequently to polycrystalline cadmium sulfide as the semiconductor, application to other materials[4-6] will be apparent.

Coplanar Versus Staggered-Electrode TFT Structures

Figure 1 compares in cross-sectional view the coplanar-electrode TFT structure with the earlier staggered-electrode design. Although either structure can be made in inverted order, the two structures shown here have been used most frequently to date. Typical experimental TFT's of either type have source and drain electrodes 100 mils long separated by a gap distance L of about 0.4 mil, or 10 microns. All the evaporated layers have a thickness which is small compared

[4] F. V. Shallcross, "Cadmium Selenide Thin-Film Transistors," *Proc. I.E.E.E.*, Vol. 51, p. 851, May 1963.

[5] H. L. Wilson and W. A. Gutierrez, "Cadmium Selenide Thin Film Field Effect Transistors," presented at the Electrochemical Society Meeting, Pittsburgh, Pa., April 1963.

[6] F. V. Shallcross, "Evaluation of Cadmium Selenide Films for Use in Thin-Film Transistors," *RCA Review*, Vol. 24, p. 676, Dec. 1963.

to the gap distance. The semiconductor thickness usually ranges from one micron to a small fraction of a micron. Insulator thickness is usually less than 500 Å.

The source and drain electrodes are of a metal which makes a low-impedance ohmic contact to the semiconductor. Evaporated gold underlying the semiconductor in the staggered structure had been found to make a satisfactory contact to cadmium sulfide as well as to several other semiconductors. The usual fabrication procedure for the staggered CdS TFT was to deposit first the gold source and drain upon the glass, using a precision evaporation jig to position the movable masks which delineated the electrodes. Since the cadmium sulfide processing[7,8] required heating of the substrate during the deposition followed by an additional air-bake treatment, it was customary to remove the substrate from the precision jig after the source–drain evaporation. The CdS evaporation was carried out in a separate vacuum system, and after heat treatment, the substrate was replaced in the precision jig for deposition of the insulator and gate electrodes. This procedure was time-consuming and required a critical realignment of the substrate with the gate mask. Furthermore, a tendency of gold to peel from the substrate during the CdS evaporation or post-evaporation bake restricted the permissible processing temperature to rather low values.

The coplanar-electrode structure illustrated in Figure 1 permits the semiconductor to be deposited first upon the substrate by any suitable method with no limitations introduced by the presence of the electrodes. Following the high-temperature processing of the semiconductor, the substrate blank is inserted in the precision jig and the electrodes and insulator layer are deposited during one evacuation. The passive components and connections required for a complete thin-film circuit can be deposited simultaneously with the TFT electrodes permitting very complex circuits to be fabricated in a single operation. Although a mechanized jig with movable masks is required, this procedure is advantageous from the standpoint of speed and precision of alignment of the electrodes.

If the semiconductor is of a type which can be satisfactorily deposited upon a cold substrate through masks similar to those used for the electrodes, the entire evaporation sequence for either the coplanar

[7] J. Dresner and F. V. Shallcross, "Rectification and Space-Charge-Limited Currents in CdS Films," *Solid State Electronics*, Vol. 5, p. 205, July-Aug. 1962.

[8] J. Dresner and F. V. Shallcross, "Crystallinity and Electronic Properties of Evaporated CdS Films," *Jour. Appl. Phys.*, Vol. 34, p. 2390, Aug. 1963.

or staggered structure can be completed in one evacuation. In most cases, however, the semiconductor layer requires special processing which must be carried out independently of the electroding operations, a situation for which the coplanar structure is preferable. An alternate procedure which has also been used with some materials is to lay down coplanar electrodes, including the gate, directly upon the substrate prior to the deposition of the semiconductor.

Operating Characteristics of Coplanar Insulated-Gate TFT's

In common with conventional field-effect transistors, the TFT is a high-input-impedance device with well-saturated pentode-like char-

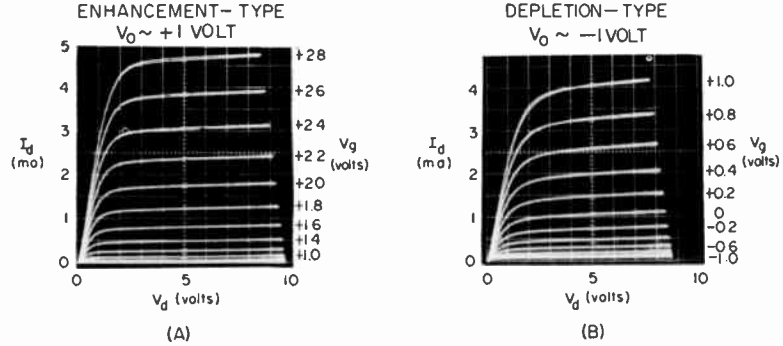


Fig. 2—Drain characteristics for two coplanar-electrode polycrystalline cadmium sulfide TFT's: (a) enhancement-type unit and (b) depletion-type unit.

acteristics. The gain is flat from d-c up to several megacycles where the response drops off at the 6 db per octave rate expected from the output impedance. The drain characteristics differ from those of the conventional p-n junction field-effect device in that the gate may be biased either positive or negative without drawing gate current. In most respects, the operating characteristics of representative units of the coplanar electrode construction are basically the same as for the staggered-electrode arrangement.[2,9] Although only n-type TFT's will be discussed and illustrated, the application of the following remarks to p-type TFT's will be apparent.

Typical plots of drain current versus drain voltage for coplanar thin-film transistors operating with the source grounded are shown in Figure 2. Since the drain current is substantially zero at zero gate

[9] H. Borkan and P. K. Weimer, "Characteristics of the Insulated-Gate Thin-Film Transistor," Northeast Electronics Research and Engineering Meeting, *I.R.E. NEREM Record*, Nov. 1962.

bias and increases by many orders of magnitude as the gate voltage is raised from zero to several volts positive, the TFT giving the characteristic shown in Figure 2(a) has been called an "enhancement-type" unit. This kind of operation is feasible only because the insulating layer prevents the flow of current from the semiconductor to the positively charged gate. The enhancement-type TFT shown here is to be contrasted with the depletion mode of operation used in the conventional field-effect transistor having a p-n junction at the gate. A "depletion-type" transistor is designed to have a useful drain cur-

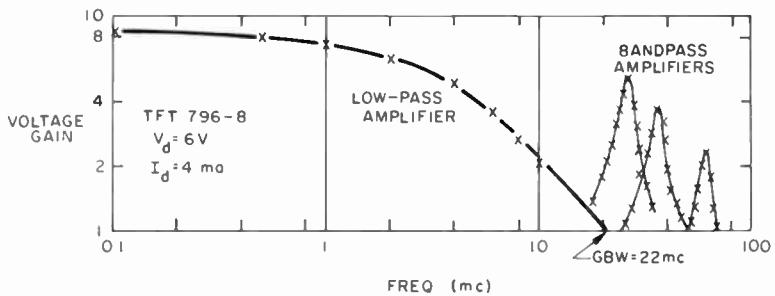


Fig. 3—Gain-versus-frequency characteristics of a CdS coplanar electrode TFT operated as low-pass and band-pass amplifiers.

rent at zero gate bias and negative gate voltage is used to pinch off the source-drain current. Figure 2(b) shows the operating characteristics of a depletion-type insulated-gate TFT. Such a unit is capable of operation in either the depletion or enhancement mode. For integrated-circuit applications the enhancement-type unit is to be preferred, although in some cases both types may be required.

The unit shown in Figure 2a has a transconductance of 4000 micromhos at a gate bias +2.6 volts. The dynamic output impedance derived from the slope of the saturated portion of the curve is 40,000 ohms. The voltage amplification factor, calculated from the product of these quantities, is 160. The input capacitance under operating conditions is about 30 picofarads. CdS TFT's have been built in the same geometry with transconductances up to 25,000 micromhos.

The gain-versus-frequency characteristics for a similar unit are shown in Figure 3. As a low-pass amplifier, it produced a voltage gain of 8.5 from d-c up to about 2.6 megacycles with a gain–bandwidth product of 22 mc. This test was made with a low-impedance signal source and with the inclusion of additional output capacitance to simulate a second TFT stage. Three different band-pass amplifier characteristics are shown for output circuits resonant at 25, 36, and

60 mc. The voltage gain at 60 mc was 2.5 with a gain–bandwidth product of 17 mc.

The d-c input resistance of the TFT is high, up to more than 10^9 ohms. The gate capacitance as a function of gate bias for a coplanar TFT is shown in Figure 4. It is noted that for both source and drain at ground potential the capacitance levels off with gate voltage, but

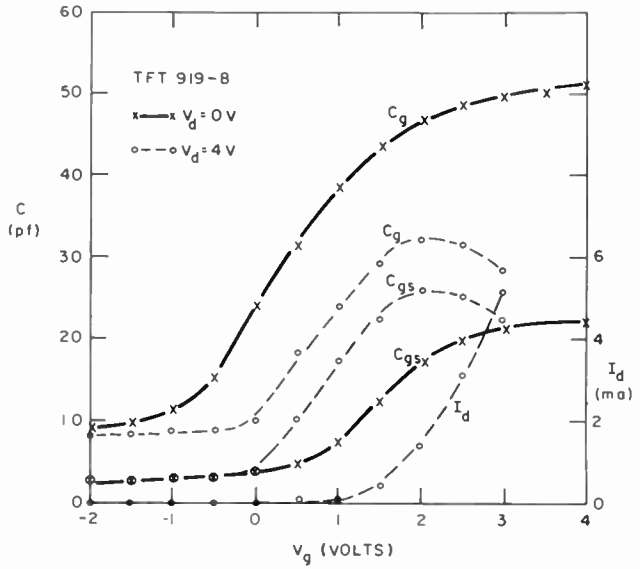


Fig. 4—Capacitance and transfer function of an enhancement-type coplanar-electrode cadmium sulfide TFT. C_g is the total gate capacitance and C_{gs} is the capacitance between gate and source electrodes.

when the drain is positive, as in normal operation, the capacitance reaches a maximum near the value of gate voltage required for the onset of drain current. Although the total gate capacitance divides about equally between the source and drain at zero drain voltage, the major portion of the capacitance at higher drain voltage occurs between gate and source. The variation in capacitance with gate voltage shown in Figure 4 is somewhat more pronounced than had been observed previously[9,10] for a staggered-electrode CdS TFT.

Figure 5 illustrates the switching waveforms which were observed with a cadmium sulfide TFT. Two 2-milliampere drain current transi-

[10] H. Borkan and P. K. Weimer, "An Analysis of the Characteristics of Insulated-Gate Thin-Film Transistors," *RCA Review*, Vol. 24, p. 153, June 1963.

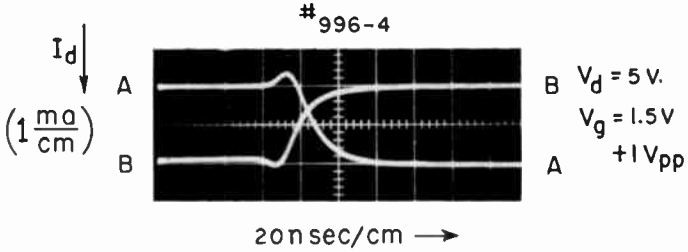


Fig. 5—Switching speed measurements for a cadmium sulfide coplanar TFT.

tions are shown; A is a transition from low to high drain current, while B is from high to low drain current. The opposite-polarity transient is direct feed-through of signal via the gate–drain capacitance. The pulse source impedance was 50 ohms. Note that the drain current transitions occur in about 30 nanoseconds.

Figure 6 shows the drain current at fixed voltages in a coplanar CdS TFT plotted as a function of the reciprocal of the absolute temperature. It is noted that at higher positive values of gate potential, V_g, the activation energy becomes progressively lower. This effect has been interpreted as due to a lowering of the barriers between CdS

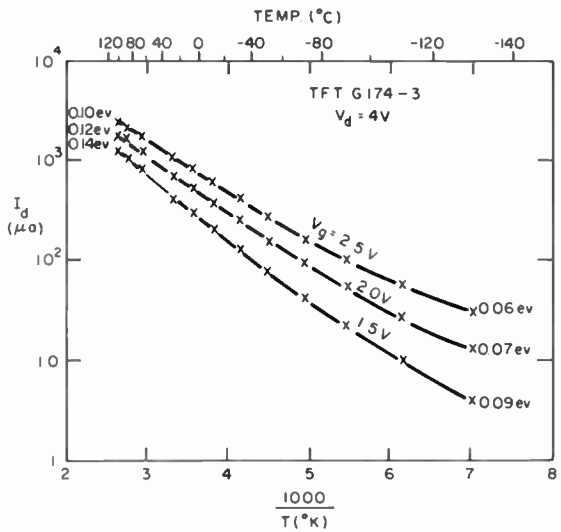


Fig. 6—Drain current plotted against the reciprocal temperature for a coplanar CdS TFT with constant electrode voltages applied. The measured activation energies are listed at the ends of the curves.

crystallites with increasing V_g, in agreement with the experimentally observed increase in Hall mobility with V_g.[11]

The saturated drain current–voltage characteristics of Figure 2 are typical of field-effect devices. Saturation occurs when the conduction channel is pinched off in the neighborhood of the drain. Such pentode-like characteristics are to be preferred over nonsaturating triode-like characteristics. In general, failure to saturate caused by unmodulated shunt paths between source and drain has been much less frequent with the coplanar structure than with the staggered structure.

Effect of Source–Drain Contacts upon Performance

Normal operation of an insulated-gate field-effect transistor requires a source contact having low impedance for injection of majority carriers. Each new semiconductor must be tested with various electrodes before the performance of the semiconductor can be effectively evaluated for TFT applications. As mentioned earlier, gold electrodes underlying the semiconductor were found to make ohmic contacts in the case of cadmium sulfide or cadmium selenide. Similar results were found by Dresner and Shallcross[7] who made thin-film diodes of cadmium sulfide with underlying gold electrodes as the injecting contact. These results may appear to be in contradiction to measurements which indicate that gold contacts evaporated on the surface of a single crystal of cadmium sulfide make a *blocking* contact[12] with a barrier height of 0.7 ev. The difference probably lies in the nonhomogeneous composition of the evaporated CdS layer with the first portion of the layer deposited on top of the gold having an excess of cadmium. The inhomogeneity may result from the normal tendency of CdS to dissociate on evaporation, with the additional factor that the condensation coefficient for cadmium on gold may be somewhat higher than on glass. The latter possibility has been suggested by R. Zuleeg who has found chemical evidence for an excess of cadmium in the neighborhood of the underlying gold electrode. When gold contacts are evaporated *on top* of a cadmium sulfide film, a blocking contact is usually obtained.

Although gold is unsuitable as an overlying source and drain in the coplanar CdS TFT, aluminum was found to make a satisfactory ohmic contact in this structure. A second advantage of aluminum as

[11] A. Waxman, V. E. Henrich, F. V. Shallcross, H. Borkan, and P. K. Weimer, "Electron Mobility Studies in Surface Space-Charge Layers in Evaporated CdS Films," presented at American Physical Society Meeting, Chicago, Illinois, Oct. 1963.

[12] A. M. Goodman, "Evaporated Metallic Contacts to Conducting Cadmium Sulfide Single Crystals," to be published in *Jour. Appl. Phys.*

compared to gold in the coplanar structure is that less difficulty is experienced during evaporation with the scattering[13] of material back of the mask into the source–drain gap region. Aluminum scatters less than gold, and the small fraction which does scatter tends to be deposited as an oxide rather than as a metal. A thin film of gold scat-

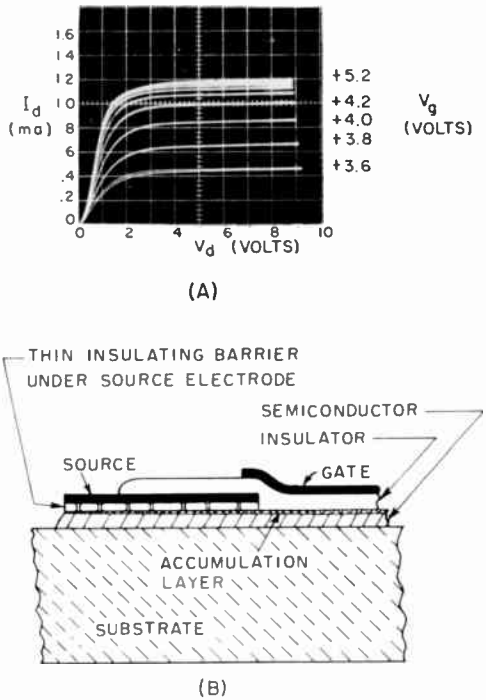


Fig. 7—(a) "Crowded" current–voltage characteristic observed in a coplanar CdS TFT having an inadvertent insulating barrier under the source electrode. (b) Current paths under the source electrode in a TFT having "crowded" characteristics.

tered into the gap interface region appears to form acceptor-like surface states on cadmium sulfide and reduces the transconductance significantly.

The failure to achieve a good ohmic contact at the source electrode will give a low transconductance and, in some cases, the peculiar "crowded" characteristics discussed below in reference to Figure 7. A blocking contact at the drain electrode is less serious since it is

[13] S. Gray and P. K. Weimer, "Production of Fine Patterns by Evaporation," *RCA Review*, Vol. 20, p. 413, Sept. 1959.

forward-biased in operation. Such a contact may be incorporated intentionally in the drain if a TFT having unidirectional characteristics is desired. A blocking contact at the drain, however, yields an S-shaped *I–V* characteristic in the neighborhood of the origin.

Figure 7(a) shows the type of source–drain characteristics which are obtained under certain conditions when an insulating barrier exists between the source electrode and the semiconductor in a coplanar-electrode TFT. Instead of continuing to increase with gate bias, the transconductance levels off and decreases toward zero as the family of curves crowd together at a maximum value of I_d. Although the "crowded" drain-current curves level off parallel to the normal saturated drain curves, the current-limiting action of the source contact occurs quite independently of the control gate itself. When the gate is omitted in such a unit, a source-limited, saturated current–voltage characteristic is observed.

Inasmuch as other physical explanations could also be offered for the type of current-limiting action observed, the evidence for its being caused primarily by a barrier at the source will be reviewed. Such characteristics have been found most frequently with the coplanar-electrode structure in which the source contact is aluminum evaporated on top of the semiconductor. Unless the aluminum is carefully evaporated, a thin film of oxide will be formed between the metal and the semiconductor. At low currents, leakage through the barrier or through pinholes at points somewhat removed from the gap is sufficient to supply the current required (see Figure 7(b)). At higher gate voltages when more carrier injection is demanded, the *IR* drop in the channel *under the source* causes this channel potential to begin to go positive with respect to the source. The field from the source pinches off the underlying conducting channel, thus limiting the current to a fixed value regardless of the gate or drain potentials. This saturation mechanism has been verified experimentally by the construction of experimental units having a thin film of insulator inserted under one electrode.

"Crowded" characteristics have rarely been seen in any TFT having the staggered-electrode geometry. The staggered-electrode structure puts less severe demands upon the source contact since the overlapping gate provides a larger effective area of contact.

Physical Factors Affecting the Pinch-Off Voltage

In the fabrication of thin-film circuits involving many TFT's on a single blank, it is necessary to be able to control the "pinch-off"

voltage, V_0, to within a specified range. An enhancement-type unit such as illustrated in Figure 2(a) could have a value of V_0 ranging from zero up to 4 or 5 volts positive for an n-type TFT. In a depletion-type unit (Figure 2(b)), V_0 could range from zero to several volts negative.

To discuss the physical factors influencing the value of V_0 it is convenient to use the analytical expression for drain current which has been derived previously by a simple field-effect analysis:[10]

$$I_d = \frac{\mu C_g}{L^2} \left\{ (V_g - V_0) V_d - \frac{V_d^2}{2} \right\}, \tag{1}$$

where I_d = drain current, in amperes,

μ = drift mobility, in cm^2/volt-sec,

C_g = capacitance across the insulating layer, and is approximately equal to the total gate capacitance, in farads,

L = length of gap between the source and drain electrodes, in cm,

V_0 = gate voltage required for onset (or pinch-off) of drain current,

V_g = applied gate voltage relative to source,

V_d = applied drain voltage relative to source.

This expression is valid for $0 \leqq V_d \leqq V_g - V_0$, up to the knee of the I_d versus V_d characteristic. Although the variation of input capacitance and change of drift mobility with gate voltage were neglected in deriving Equation (1), the expression is in good agreement with experimental observations. The V_0 term was introduced into the derivation to take into account the charges initially present in the semiconductor. V_0 is defined as

$$V_0 \equiv -\frac{N_0 q}{C_g}, \tag{2}$$

where q is the electronic charge and N_0 is the *total* number of charges initially present in the gap region.

N_0 is a function of the thickness of the semiconductor, the volume density of donors and acceptors, and the shape of energy bands near the interface. N_0 is positive for a depletion-type unit, where it repre-

sents the total number of free carriers initially present in the film. N_0 is negative for a strongly enhancement-type unit, and in this case represents the total number of acceptor states or traps which must be filled before the free-carrier density can be increased appreciably by field effect.

For a depletion-type unit N_0 must be large enough to yield the required value of I_{d0}, the saturated drain current at zero gate bias. The value of I_{d0} derived from Equations (1) and (2) is

$$I_{d0} = \frac{\mu N_0^2 q^2}{2L^2 C_g}, \tag{3}$$

or

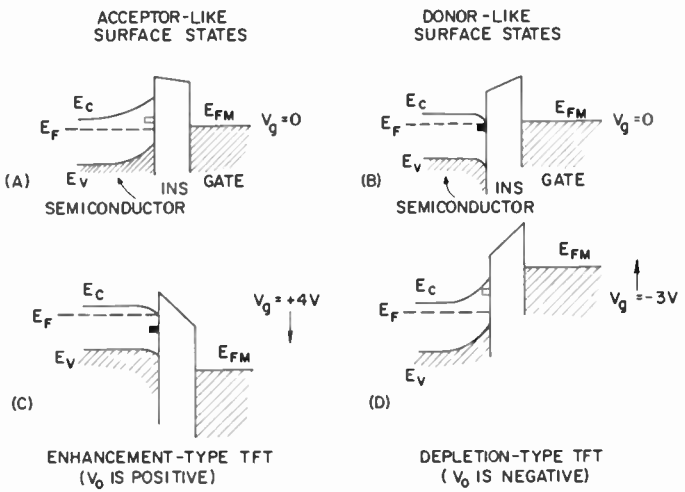
$$I_{d0} = -\frac{V_0}{2R_{SD}}, \tag{4}$$

where R_{SD} would be the source–drain resistance if the gate were absent. It is interesting to note that for all values of drain voltage much greater than $V_0/2$, the saturated drain current is considerably smaller than the value the drain current would have if the gate were absent. For a given semiconductor resistivity, the larger the gate capacitance the smaller I_{d0}.

In agreement with the above analysis, it has been found experimentally that by proper choice of the thicknesses of the insulator and semiconductor a low value of I_{d0} can be obtained even though the resistivity of the semiconductor is quite low. Since any depletion-type TFT can be operated in the enhancement mode, the characteristics of such units having a low I_{d0} are for practical purposes equivalent to a true enhancement-type unit whose value of I_{d0} is actually zero.

In a strongly enhancement-type TFT, a high positive gate bias must be applied to give an appreciable drain current (see Figure 2(a) above, or especially Figure 3 of Reference (2)). Such characteristics indicate that a large number (N_0) of acceptor states or traps must be filled by field effect before the conductivity of the semiconductor begins to increase. Although traps and donors throughout the thickness of the semiconductor layer may affect the performance of the TFT, those nearest the surface of the semiconductor at the semiconductor–insulator interface will have the major effect. Acceptor-like surface states will bend the bands up at the semiconductor surface as shown in Figure 8(a), while donor-like states bend the bands down at the surface as in 8(b). The effect of a positive gate bias (in an n-type unit) is to form an accumulation layer at the surface, as shown

in Figure 8(c), but this cannot occur until the unfilled acceptor-like surface states have been filled. If too large a density of surface states is present, the Fermi level is effectively clamped at the energy of the surface state permitting no modulation in conductivity. The same is true for the depletion type unit shown in Figures 8(b) and 8(d) where the donor-like surface states must be emptied before the negative gate



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can form a depletion layer at the surface. The fact that the surface-state density can be kept sufficiently small on evaporated polycrystalline surfaces to permit effective current modulation has been one of the most striking features of the TFT development.

The exact nature of the particular surface states that determine the pinch-off voltage V_0 in the CdS TFT is at present speculative. However, it has been possible in fabrication to control the value of V_0 moderately well by the processing of the semiconductor and by choice of insulator materials. A short 500°C air bake of the cadmium sulfide layer combined with the use of a calcium fluoride insulator will give an enhancement-type unit. A silicon monoxide insulator on the same semiconductor will give a depletion-type unit. This effect is probably due to the combination of the SiO with adsorbed oxygen on the surface of the CdS, which had been acting as acceptor states. A glow discharge over the surface of the CdS prior to deposition of the insulator will also remove oxygen or sulfur shifting the characteristics

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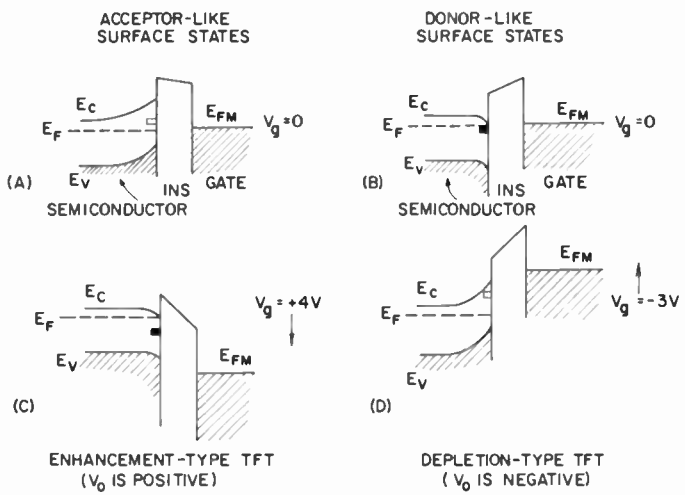

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toward depletion-type. The value of V_0 is also affected to some extent by the work function of the gate material. In general an aluminum gate tends to give a lower value of V_0 than a gold gate.

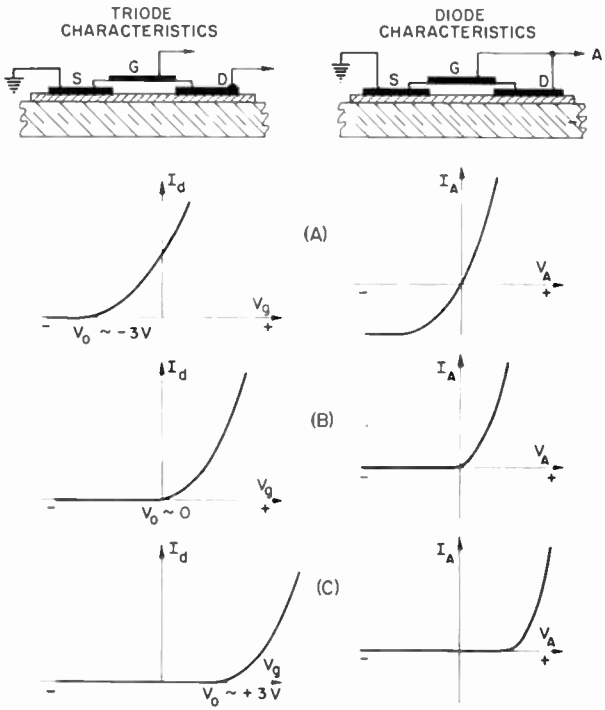

Fig. 9—Expected diode characteristics for an insulated-gate transistor having the gate tied to the drain: (a) $V_0 \approx -3$ volts, (b) $V_0 \approx 0$ volts, and (c) $V_0 \approx +3$ volts.

Characteristics of the TFT Operated as a Diode

In the fabrication of thin-film circuits it is desirable to be able to deposit thin-film diodes at the same time as the triodes by compatible procedures. The success in controlling V_0 in the TFT has made it feasible to use the triode itself or a modified version of the triode as a diode. Figure 9 shows the expected characteristics of three TFT's having different values of V_0 operated as a diode with the gate tied to the drain. Each TFT has bidirectional characteristics as normally operated, with ohmic contacts at both source and drain. A TFT having V_0 very close to zero would give the most satisfactory diode characteristic, although large positive or negative values of V_0 yield characteristics which may be of interest for special purposes. Figure

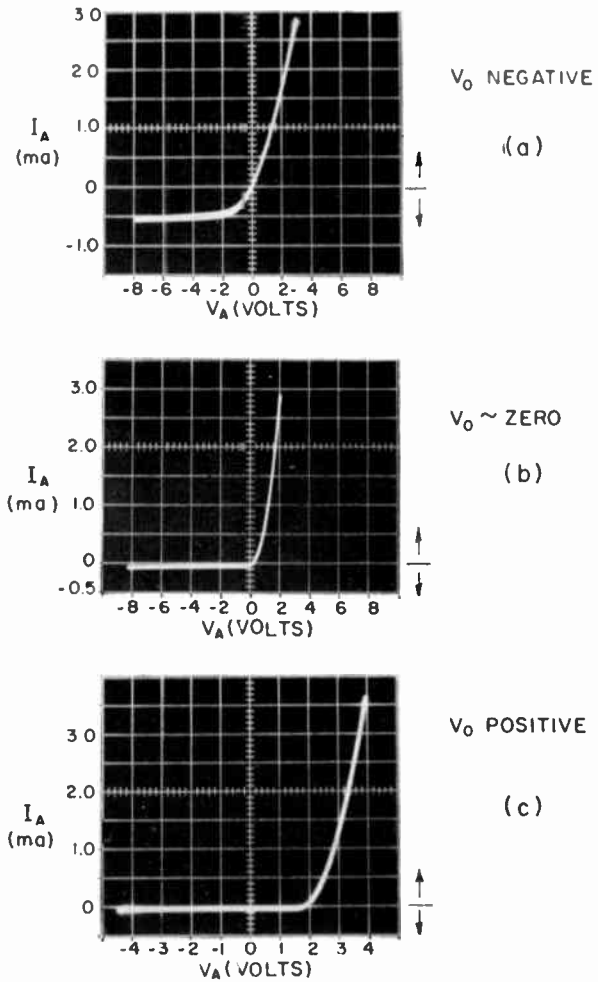

Fig. 10—Measured characteristics of three CdS TFT's having different values of V_0 and connected as field-effect diodes.

10 illustrates the actual diode characteristics observed in three TFT's having different values of V_0. A rectification ratio of 10^5 has been obtained in units having both source and drain electrodes making ohmic contact to the semiconductor.

Acknowledgment

helpful discussion and acknowledge the valuable contributions of W. S. Homa, V. L. Frantz and R. R. Goodrich in fabricating the experimental units.

The writers wish to express their appreciation to H. Johnson for

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temperatures from room temperature to 350°C; all such films appeared dark reddish in color. CdSe deposited on a room-temperature substrate appeared smooth at 450× magnification; CdSe deposited on a substrate at 350°C showed granularity on the order of 2 μ in size. The x-ray diffraction data indicated that average crystallite size was approximately 500 Å or larger for films 1 to 4 μ thick. The crystallite size increased with substrate temperature. Line-broadening effects in the Debye–Scherrer patterns of scraped films indicated that there was no extreme anisotropy of crystallite shape.

CdSe films about 4 μ thick deposited at substrate temperatures of 50° and 230°C were examined with the x-ray diffractometer; the films were then removed from the substrate, pulverized, and standard Debye–Scherrer powder patterns taken. Cu$K\alpha$ radiation was used. The data are summarized in Table I. Intensities were estimated by measuring peak heights directly on the diffractometer tracings, and peak heights in terms of optical density on microphotometer tracings of the powder patterns. They are given relative to the maximum intensity lines. There were no significant differences between the interplanar spacings, d, for the various experiments, and the results were averaged. The results are compared with data from National Bureau of Standards (NBS) tables on CdSe,[19] and also with NBS intensity data on cubic ZnS,[20] which is isomorphous with cubic CdSe and would be expected to yield a similar distribution of intensities for most of the observed reflections. In addition, the table gives the expected intensities calculated for cubic CdSe, assuming the zincblende structure and atomic scattering factors for Cd and Se given in International Tables for X-Ray Crystallography.[21] The calculated intensities include an empirically determined isotropic temperature factor of the form exp $(-0.9/d^2)$.

The observed diffraction patterns indicated that both films consisted largely of a mixture of cubic and hexagonal CdSe; there is approximately three times as much cubic as hexagonal phase in the high-temperature sample and approximately twice as much cubic as hexagonal phase in the low-temperature sample. The diffractometer tracings of the film show only reflections from planes parallel to the substrate. For these films the intensities for 002 (hex) and 111

[19] H. E. Swanson, N. T. Gilfrich, and M. I. Cook, "Standard X-Ray Diffraction Patterns," NBS Circular 539, Vol. 7, p. 12, 1957.

[20] H. E. Swanson and R. K. Fuyat, "Standard X-Ray Diffraction Patterns," NBS Circular 539, Vol. 2, p. 14, 1953.

[21] *International Tables for X-Ray Crystallography*, Vol. 3, pp. 201-212, Kynoch Press, Birmingham, England, 1962.

Table I—X-Ray Data on CdSe Films: Cubic and Hexagonal Phase Lines

Indices		NBS Tabulated Data			Calculated	Observed Results				
hkl (cub)	*hkl* (hex)	ZnS (cub) *I*	CdSe(hex) *I*	*d*(Å)	CdSe (cub) *I*	*d*(Å)	*I*(film) 50°C	*I*(film) 230°C	*I*(powder) 50°C	*I*(powder) 230°C
	100		100	3.72		3.70	5.3	0.3	25	12
111	002	100	70	3.51	100.0	3.49	100	100	100	100
	101		75	3.290		3.27	0.6	0.4	10	10
200		10			2.9	3.08	0.4	0.1	6	1
	102		36	2.554		2.57	<0.2	<0.1	4	3
220	110	51	85	2.151	65.2	2.14	0.9	0.1	58	47
	103		70	1.980		1.977	1.5	0 1	14	8
	200		12	1.863		1.875	<0.4	0.1	4	8
311	112	30	51	1.834	38.2	1.829	1.9	0.5	44	36
	201		11	1.800		1.802	0.4	0.1	4	10
222	004	2	—	—	0.6	1.750	0.6	0.6	3	3
	202		8	1.645		1.641	<0.2	<0.1	4	2
	104		—	—						
400		6			8.7	1.515	<0.2	<0.1	2	<2
	203		20	1.456		1.485	<0.4	0.1	6	2
	210		8	1.407		1.395	<0.4	<0.1	8	2
331		9			12.4					
	211		8	1.380		1.392	<0.4	<0.2		7
420	114	2	—	—	0.6	1.346	0.9	<0.2	4	1
	105		13	1.3120		1.310	0.6	0.1	4	2
	212		5	1.3059						
	204		—	—		1.283	<0.4	<0.1	<4	2
422	300	9	10	1.2411	14.7	1.238	<0.4	<0.2	13	8
	301		<1	1.2218		1.217	<0.4	0.1	4	6
	213		18	1.2055		1.206	<0.4	<0.2	10	3
333 511	006	5	—	—	7.8	1.169	0.6	0.8	12	7
	302		8	1.1700						
	205		7	1.1201		1.117	<0.2	<0.2	<4	1
	106		2	1.1144						
	214		—	—		1.094	<0.2	<0.2	<4	1
440	220	3	6	1.0748	4.2	1.072	<0.2	<0.2	8	3
	310		3	1.0327		—	<0.2	<0.1		
	222		6	1.0273						
	116		4	1.0267		1.026	0.4	<0.2	23	8
531		5			7.3					
	311		2	1.0219		—	<0.2	<0.2		
442 600					0.3	—	<0.2	<0.2	<6	<4
620					5.6	0.960	<0.2	<0.2	6	4
	313		6	0.9446		0.942	<0.2	<0.2	7	1
533					2.8	0.927	<0.2	<0.2	6	<4
622					0.2	—	<0.2	<0.2	<4	<4
	207		<1	0.8820		0.876	<0.2	0.3	6	<7
444	008		<1	0.8761	1.8					
	306		2	0.8508						
551 711					5.5	0.8513	<0.2	<0.3	10	5
640					0.2	—	<0.2	<0.3	<6	<4
642					12.6	0.8114	0.9	*	19	7
731 553					12.3	0.7907	*	*	10	5

* Reflection at angle not covered in diffractometer trace.

(cub) are unusually strong relative to other reflections when compared to the intensity distribution for a randomly oriented powder. Thus, in the films, both phases appear to show considerable preferred orientation, with the hexagonal c axis and the cubic [111] direction perpendicular to the substrate. Based on seven high-angle cubic reflections, the cubic cell dimension is 6.08 ± 0.01 Å. There is no significant

Table II—Extra Diffraction Lines from CdSe Films

d obs. (Å)	d calc. (Å)	hkl'	hkl''	I (powder) 50°C	I (powder) 230°C	I (film) 50°C	I (film) 230°C
11.2	10.5 11.7	003	002	29	16	*	*
8.84	8.76	004		19	4	*	*
6.90	7.01	005	003	15	11	*	*
5.95	5.84	006		11	5	*	*
4.41	4.38	008		4	<3	<0.4	<0.2
4.23	4.19		005	<4	<3	<0.4	0.3
3.80	3.90	009		<4	<3	<0.4	0.1
3.62				<4	<3	0.6	0.4
3.49	3.51	00,10	006	100	100	100	100
3.35				<4	<3	0.4	0.2
2.77	2.70	00,13		<4	1	0.4	0.2

* Reflection at angle not covered in diffractometer trace.

difference between the high- and low-temperature films in this; it is slightly higher than the value of 6.04 ± 0.03 Å given by Pashinkin and Sapozhnikov[22] for chemically precipitated powders, and may be a result of nonstoichiometry in the evaporated films. Additional x-ray diffractometer traces of a series of samples deposited on substrates between room temperature and 350°C showed the presence of highly oriented polycrystalline CdSe and were consistent with either hexagonal CdSe, cubic CdSe, or cubic–hexagonal phase mixtures.

In addition to the cubic and hexagonal phase lines in Table I, x-ray reflections for both samples were observed at low angle, corresponding to interplanar spacings between 5 and 11 Å. These and several other weak extra lines are given in Table II together with their intensities

[22] A. S. Pashinkin and R. A. Sapozhnikov, "Cubic Modification of Cadmium Selenide," *Kristallografia*, Vol. 7, p. 623, Aug. 1962.

relative to the lines with $d = 3.5$ Å. Reflections from wider-spaced planes would not have been observable. Most of the lines appear to be compatible with a hexagonal c-axis length of 35.1 Å. The usual hexagonal and cubic CdSe structures are layered forms differing only in the stacking arrangement; the hexagonal form is of the type ABABAB . . ., while the cubic form is of the type ABCABC . . . . The usual hexagonal distance A-B-A is about 7.01 Å. A stacking arrangement such as ABCABCABABABCABCABAB . . . would have the 35.1

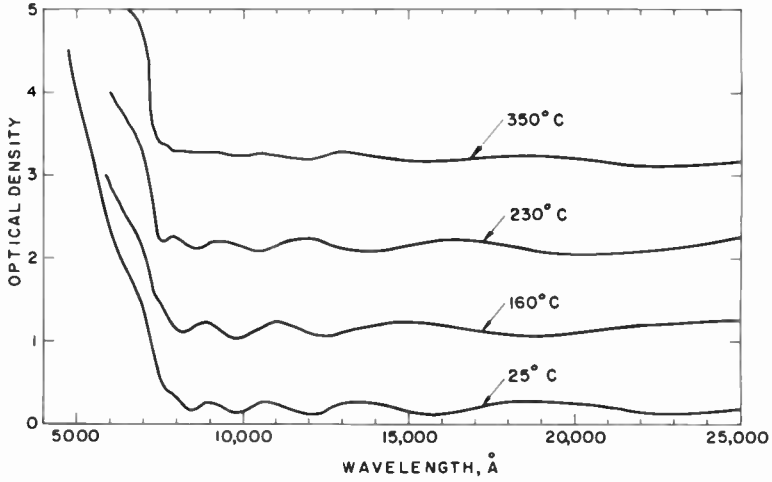

Fig. 1—Optical transmission of CdSe films deposited at various substrate temperatures. Successive curves are displaced by 1.0 in optical density for clarity.

Å repeat distance required, and indices are assigned on this basis. The simpler arrangement ABCABABCAB . . . would have a 17.5 Å repeat distance and would also account for many of the lines. The second set of indices given in Table II is based on a hexagonal cell with a c axis of 21.1 Å, corresponding to an arrangement such as ABABACABABAC . . . Essentially, these results indicate the presence of extensive stacking faults (of a repetitive type) in the evaporated CdSe films.

Figure 1 gives optical transmission data for several CdSe films approximately 0.9 μ thick deposited on glass. These were deposited on substrates ranging from room temperature to 350°C. Successive curves are displaced by 1.0 in optical density for clarity. The structure in the curves appears to be largely a result of interference fringes. No large differences are observed although the room-temperature film shows a slightly higher absorption in the red than the intermediate-temperature

films, and a somewhat more-gradual rise in absorption with decreasing wavelength. Fringes are less pronounced in the rougher films.

Spectrographic analysis of the CdSe films indicated no gross change in impurity content from that in the evaporant material. Measurements of film resistance for sequential fractions of evaporant indicated no large accumulation of electronically active impurities in a given fraction of the vapor which was used for film formation.

Table III—Hall Mobility and Resistivity for CdSe Films

Substrate Temperature (°C)	μ_H (cm²/volt-sec) dark	light	ρ (ohm-cm) dark	light
25	18	23	3×10^3	2×10^2
75	24	36	7×10^4	2×10^3
75*	50	130	4×10^6	1×10^4
160	5	10	2×10^2	3×10^1
230	4	8	4×10^2	4×10^1
310	6	14	2×10^4	3×10^2
350	7	14	2×10^3	8×10^1

* Baked in CdSe:Cu,Cl + air, 3 hours, 300°C.

Hall data were obtained on several samples made with various substrate temperatures, and otherwise similar deposition conditions. Results are given in Table III. These data include mobility and apparent resistivity in both the dark and in strong (white) illumination ($\sim 10^3$ foot-candles). Data are also given for one sample baked in CdSe:Cu,Cl powder plus air at 300°C. All samples were n-type. If the films were electrically inhomogeneous in the direction perpendicular to the substrate, the mobility and resistivity values would be mean values weighted according to carrier density. Such inhomogeneities might arise from adsorbed surface species, such as those described by Somorjai[11] and Russ.[23]

The values of mobility are considerably less than the highest reported for single crystals;[6,7] they are comparable to, although somewhat less than, values reported by Somorjai[11] for CdSe films deposited on unheated substrates in ultra-high vacuum. In that work, values of 50 cm²/volt-sec were obtained for films not exposed to oxygen above

[23] M. J. Russ, "Surface Conduction in Group II-VI Semi-Insulators," *Jour. Appl. Phys.*, Vol. 34, p. 1831, June 1963.

room temperature, and values of 10 cm^2/volt-sec were obtained for films heated in oxygen at 360°C. The difference was attributed to effects of impurity scattering. Those results suggest that oxygen incorporation during deposition at the higher pressures used in the present work may account for the results obtained here. For these CdSe films there is no simple dependence of resistivity or Hall mobility on substrate temperature or crystallite size; both mobility and resistivity appear to go through a minimum for substrate temperatures near 200°C. The effect of baking the CdSe films in contact with doped powder is consistent with previous results for CdS,[16] both dark and light mobility increasing substantially. Pronounced photo-Hall effects were observed for many of the CdSe films, especially those baked in CdSe powder and those deposited at high substrate temperature.

The dependence of CdSe film resistance on evaporation parameters is not completely clear, although it appears to be quite sensitive to the details of the film preparation process and can vary over many orders of magnitude. In the case of CdS, the effect of substrate temperature on film resistance is large; increasing the substrate temperature apparently decreases the amount of excess cadmium and thus increases the CdS resistivity. For CdSe the effect of substrate temperature was masked by other large variations. Resistivity can be quite high even for films deposited on unheated substrates. For a set of 16 films deposited over a period of time on room-temperature substrates, but with other deposition parameters allowed to vary, resistivities ranged from 10^8 to 10^{-2} ohm-cm. Although some evidence exists for differences in resistivity between cubic and hexagonal CdSe,[24] it is unlikely that differences in the ratio of phases present alone account for the results observed here. Samples deposited simultaneously with those described in Table I had resistivities of 1 and 10^4 ohm-cm for the 50° and 230°C substrates, respectively, with relatively little difference in the phases present.

Data on variation of resistivity of successive fractions of the CdSe were obtained by condensing the film on a substrate moving past a slit evaporation mask. The results indicate some increase in resistivity during deposition (about one order of magnitude) but no very large effect attributable to evaporant fractionation. In general, post-evaporation baking of the samples in contact with cadmium vapor or vacuum decreased the film resistivity, while baking them in contact with selenium vapor or air increased the resistivity, the magnitude of the effects depending on details of the heating cycles. A decrease in CdSe

[24] M. Aoki and S. Tanaka. "Crystal Structure and Physical Properties of CdSe," *Ôyô Butsuri*, Vol. 24, p. 113, 1955.

film resistance on applying an over-layer of dielectric such as silicon monoxide has been described by Wilson and Gutierrez;[10] similar results have been obtained in this work and in the case of CdS layers.[4,5] The change may be attributable to the formation of an accumulation layer at the CdSe–SiO interface in a process involving migration of adsorbed oxygen into the SiO.

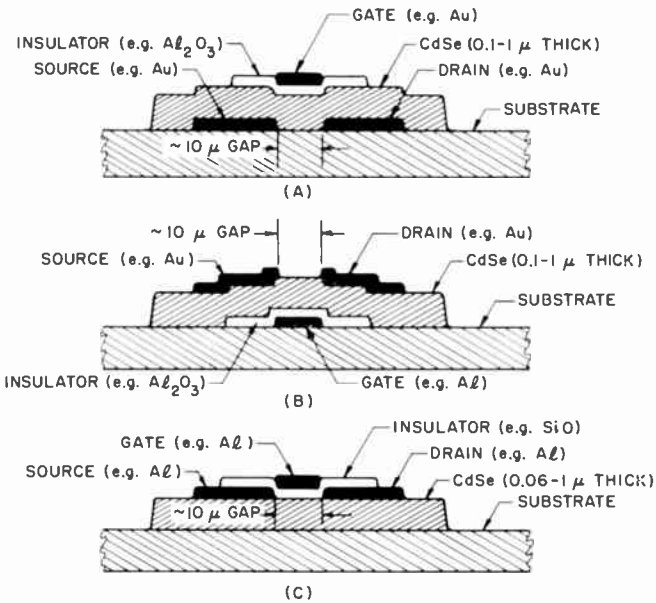

Fig. 2—Cross-sectional drawing of CdSe TFT's: (A) standard staggered unit, (B) inverted staggered unit, (C) coplanar unit.

CdSe Thin-Film Transistors

Evaporated transistors were constructed using CdSe films and incorporating various geometries described by Weimer.[1-5] Figure 2 illustrates three types of successful structures. Coplanar- and staggered-electrode geometries both yielded units with good performance. Satisfactory units were made with the gate on either the top or bottom of the unit. In the latter case, the performance appears to be a more critical function of semiconductor and insulator condition than in the former.

Electrode spacings of 8 to 25 microns and lengths of 2 to 5 mm were used. The source–drain spacing and electrode lengths were not crucial within the limits examined.

CdSe thickness was varied between 600 Å and 1 μ. Insulator and electrode thickness was several hundred angstroms.

Gold, aluminum, gold–indium oxide, and aluminum–indium electrodes were used for source and drain, and aluminum, gold, or combinations for the gate. In the coplanar structures, aluminum electrodes were superior to gold electrodes; as in the case of CdS,[4,5] CdSe coplanar units with gold source and drain showed low transconductance and poor saturation. The effect may be due to a gold–CdSe blocking contact or to acceptor states at the CdSe insulator interface produced by the presence of scattered gold. However, inverted staggered units having gold electrodes on top of the CdSe and the gate beneath showed excellent performance. This difference may be due to an effective overlap of gate and source electrodes, the use of CdSe deposited under different conditions, or the absence of scattered gold at the CdSe–insulator interface. In standard staggered structures, use of In_2O_3 under the gold permitted its use in the 200-250°C range by increasing adherence to the substrate. Various insulator layers were employed, including CaF_2, SiO, Al_2O_3, SiO_2, and multiple layers of CaF_2 and Al_2O_3. As in the case of CdS,[4,5] the nature of the insulator is important in determining both the details of band bending at the semiconductor–insulator interface and also the breakdown voltage of the unit.

The best CdSe units were ones in which the CdSe was deposited at substrate temperatures of 150°C or higher. In addition, annealing the films in air at temperatures in excess of 300°C improved the performance. Films deposited or annealed at high temperatures were less subject to "crowding," hysteresis loops, and "rubbery" characteristics.[4,5] Crowding is apparently due to formation of an insulating layer between the source electrode and the semiconductor and appears as a limitation in the maximum current which can be drawn through the device. Rubbery characteristics appear as an instability of operating characteristics with variations in bias.

Both enhancement and depletion operation was obtained. The V_0, or gate bias required for onset or pinch-off of drain current,[3] is a function of sample geometry and processing. Values of V_0 between about —2.0 and +2.4 volts have been obtained. Figure 3 gives drain characteristics for two CdSe TFT's. Transconductances as high as 25,000 micromhos have been obtained for units with 5-mm-long gates, and 12,000 micromhos together with a voltage gain of 150, for a 2-mm-long unit. Gate capacitance for the units shown in Figure 3 is on the order of 30 to 50 picofarads.

Conclusions

In summary, polycrystalline CdSe films have physical properties similar to CdS films. X-ray measurements indicate the presence of

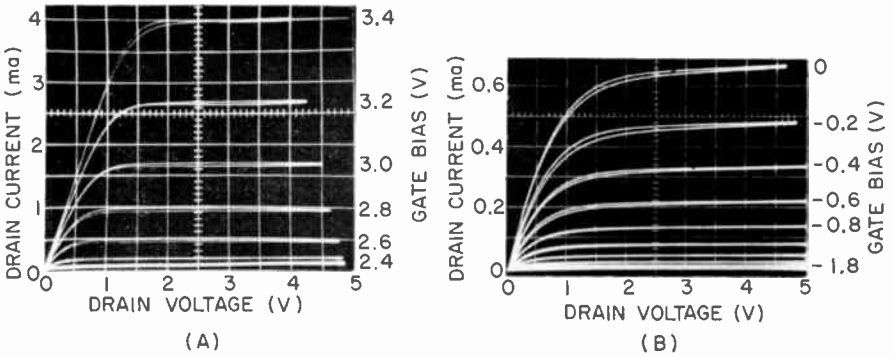

Fig. 3—Drain characteristics for two CdSe TFT's: (A) unit showing enhancement operation and (B) unit showing depletion operation.

both cubic and hexagonal phases. The CdSe films apparently can be deposited at higher substrate temperatures than CdS films. The dependence of film resistivity on deposition parameters appears to differ somewhat from that for CdS. In particular, films deposited at low substrate temperatures can be made with relatively high resistivity, and deviations from stoichiometry are apparently not as pronounced as in the case of CdS; this result is consistent with the results of Wilson and Gutierrez.[10] Effects of powder-baking CdSe films are similar to those encountered with CdS.

Thin-film transistors using cadmium selenide as the semiconductor have performance comparable with that of units made in a similar way with cadmium sulfide. Effects of electrode materials, geometry, and processing are qualitatively similar to those observed with CdS.

Acknowledgments

The author is indebted to P. K. Weimer and H. Johnson for helpful discussions, to J. Dresner for Hall measurements, to R. J. Paff for aid in x-ray measurements, and to V. L. Frantz, H. P. Lambert, W. S. Homa, and R. B. Schilling for assistance in the fabrication and testing of TFT's.

TRANSFER CHARACTERISTICS OF FIELD-EFFECT TRANSISTORS

By

W. A. Bösenberg*

Summary—The transfer characteristic of field-effect transistors can be designed to fit a particular application. For example, sharp-cutoff devices are desirable for use in amplifiers and frequency modulators, while remote-cutoff devices are suitable for use in amplifiers having automatic gain control. The desired cutoff characteristics can be achieved by establishing proper impurity profiles of the channel region. Conventional channel-diffusion profiles result in sharp-cutoff devices, while epitaxial techniques may be used for remote-cutoff devices.

Introduction

AMPLIFYING DEVICES are usually characterized by a transconductance, g_m, given by

$$g_m = \left(\frac{\partial I_{\text{output}}}{\partial V_{\text{input}}} \right) V_{\text{output}} = \text{constant}, \tag{1}$$

and by a voltage amplification factor μ given by

$$\mu = \left(\frac{\partial V_{\text{output}}}{\partial V_{\text{input}}} \right) I_{\text{output}} = \text{constant}, \tag{2}$$

where I_{output} is the plate or drain current, V_{input} is the grid or gate voltage, and V_{output} is the plate or drain voltage for electron tubes or field-effect transistors, respectively.

For a practical device, both high transconductance and high-voltage amplification are desirable.

Sharp-Cutoff and Remote-Cutoff Devices

The transconductance, g_m, is usually a function of the input voltage. For a sharp-cutoff device, the transconductance may be defined as

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$$g_m = g_{m0}\left(1 - \frac{V_{\text{input}}}{V_p}\right) \tag{3}$$

where g_{m0} is the zero-bias transconductance and V_p is the pinch-off voltage.

For a remote-cutoff device, the transconductance should be a slow function of the input voltage, defined as

$$\log g_m = C_1 - C_2 V_{\text{input}}, \tag{4}$$

where C_1 and C_2 are constants.

Frequency Modulator

As stated above, the sharp-cutoff device is highly desirable for use in a frequency modulator or mixer. The output current of such a device is

$$I_{\text{output}} = g_m V_g, \tag{5}$$

where V_g is the grid or gate voltage. If $V_g = V_1 + V_2$, where V_1 and V_2 are the signals to be mixed, the output current is given by

$$\begin{aligned} I_{\text{output}} &= g_{m0}\left(1 - \frac{V_1 + V_2}{V_p}\right)(V_1 + V_2) \\ &= g_{m0}\left(V_1 + V_2 - \frac{V_1^2}{V_p} - \frac{2V_1V_2}{V_p} - \frac{V_2^2}{V_p}\right); \end{aligned} \tag{6}$$

here, $g_{m0}V_1$ is the amplified signal of V_1,

$g_{m0}V_2$ is the amplified signal of V_2,

$g_{m0}\dfrac{V_1^2}{V_p}$ is the amplified second harmonic of V_1,

$g_{m0}\dfrac{V_2^2}{V_p}$ is the amplified second harmonic of V_2,

$g_{m0}\dfrac{V_1V_2}{V_p}$ is the desired nonlinear mixing term.

Equation (6) shows that only the frequencies ω_1, ω_2, $2\omega_1$, $2\omega_2$, $\omega_1 + \omega_2$, and $\omega_1 - \omega_2$ are obtained, and that the terms $m\omega_1 \pm n\omega_2$, which must be suppressed in conventional mixers, are not present.

Automatic-Gain-Control Amplifiers

Automatic gain control is often obtained by use of a d-c bias proportional to the output voltage to control the gain of a remote-cutoff amplifier. If the relationship given in Equation (4) is used, the output current can be expressed as an exponential function of the input voltage;

$$I_{output} = g_m V_{input} = V_{input} \exp (C_1 - C_2 V_{input}). \tag{7}$$

The gain-control feature can be extended over several stages to provide an essentially constant output signal for changes of several orders of magnitude in the input voltage.

Field-Effect Transistors

In the preceding paragraphs, the basic criteria for sharp-cutoff and remote-cutoff devices were given. Now, calculations will be made to derive the specific relationships that must be established for the field-effect transistor to meet these criteria. For the geometry that is assumed, the calculations show that the transfer characteristics of the field-effect transistor can be made to fit a particular application and that the desired cutoff characteristic can be achieved by establishing the proper impurity profiles in the channel region.

Geometry of the Field-Effect Transistor

For the calculations of the field-effect transistors, the geometry shown in Figures 1 and 2 has been assumed. These figures show that the mathematical problem does not depend on the coordinate y, which will contribute only a factor proportional to W, the width of the field-effect transistor.

Poisson's Equation and Sheet Conductance

In a p-n junction, a high electrical (Boltzmann) field is generated by the donors and acceptors to prevent mobile charge carriers from diffusing across the junction. This electrical-field zone expands with an increase in the reverse bias. The field distribution depends on the net donor and acceptor concentration C and is defined by Poisson's equation as

$$\Delta V = -q \frac{C(z)}{\epsilon\epsilon_0} \tag{8}$$

where q is the electronic charge and $\epsilon\epsilon_0$ is the absolute dielectric constant of the semiconductor material used.

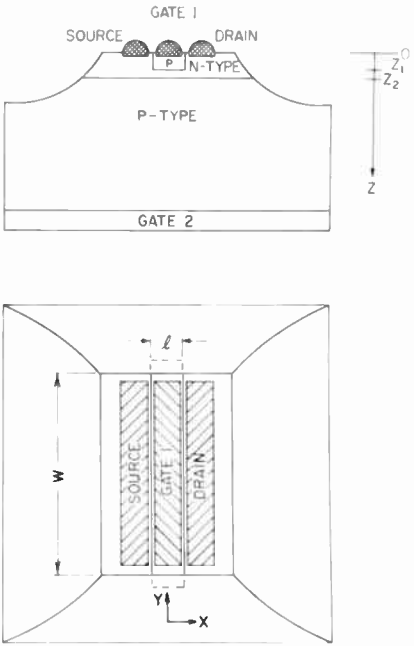

Fig. 1—Geometry of the field-effect transistor.

When no (or very little) current is flowing from source to drain, Equation (8) can be simplified to a one-dimensional equation for the voltage V. The resultant equation becomes

$$\frac{d^2V}{dz^2} = -q\frac{C(z)}{\epsilon\epsilon_0}. \tag{9}$$

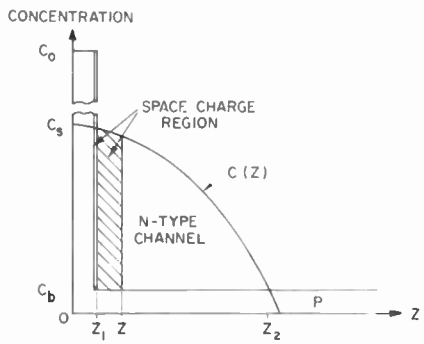

Fig. 2—Concentration profile for field-effect transistors having an n-type channel.

If $C(z)$ is known, $V(z)$ can be obtained by double integration of Equation (9). As a first boundary condition, the field is assumed to be zero at the end of the high-field region (point z in Figure 2). This assumption is valid for the reverse-biased p-n junction. The second boundary condition is reached when the space-charge layer penetrates the whole channel ($z = z_2$ in Figure 2); the gate voltage V is then equal to the pinch-off voltage, V_p. The variation of the space-charge layer on the p-type side can be neglected if the doping level is sufficiently high, a condition that is easily fulfilled for an alloyed or a heavily diffused top gate.

The transconductance g_m is proportional to the sheet conductance G; that is,

$$g_m \sim G = \int_z^{z_2} q\mu(C)C(z)dz. \tag{10}$$

In semiconductors, the mobilities, μ, are generally dependent on the concentration, and Equation (10) must be integrated numerically. This integration has been performed for germanium by Veloric and Greig[1] and for silicon by Irvin.[2]

For practical applications, the surface concentration, C_s, is equal to 10^{17} cm^{-3}, and the background concentration, C_b, is equal to 10^{15} cm^{-3}. The electron mobility changes only slightly in this range, and an average mobility $\bar{\mu}$ may be assumed. The conductance is then given by

$$G = q\bar{\mu} \int_z^{z_2} C(z)dz. \tag{11}$$

The sheet conductance is largest, and is equal to G_0 when z is zero. Both the normalized gate voltage, V/V_p, and the normalized sheet conductance, G/G_0, which are used to establish universal design curves, depend only on z as a parameter.

The simplest case is a field-effect transistor with constant channel doping, in which the net concentration C is equal to the surface concentration, C_s, and the background concentration, C_b, is zero (case A,

[1] H. S. Veloric and W. J. Greig, "Evaluation and Control of Diffused Impurity Layers in Germanium," *RCA Review*, Vol. 21, p. 437, Sept. 1960.

[2] J. C. Irvin, "Resistivity of Bulk Silicon and Diffused Layers in Silicon," *Bell Syst. Tech. Jour.*, Vol. 41, p. 387, March 1962.

Figures 3 and 4). These conditions are dependent upon the following relationship:[3]

$$\frac{g_m}{g_{mo}} = \frac{G}{G_0} = 1 - \sqrt{\frac{V}{V_p}}. \tag{12}$$

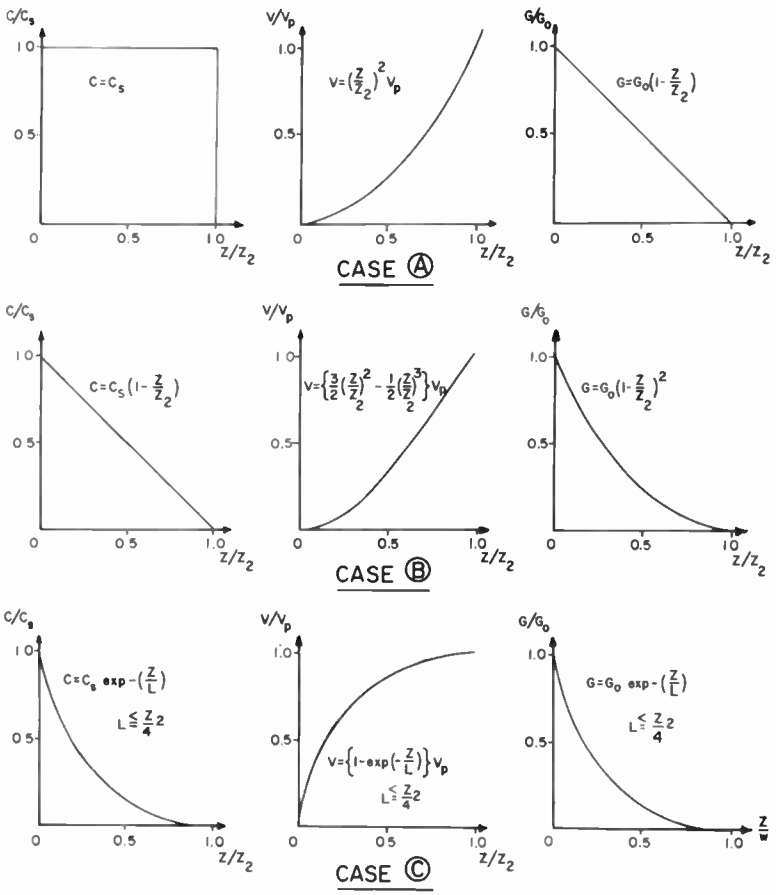

Fig. 3—Impurity, voltage, and sheet conductance as a function of distance for various distributions.

If epitaxial techniques are used, a concentration profile that decreases linearly with distance may be achieved by a linear change in the doping rate (case B, Figures 3, 4, and 5). For this condition, the

[3] W. Shockley, "A Unipolar Field Effect Transistor," *Proc. I.R.E.*, Vol. 40, p. 1365, Nov. 1952.

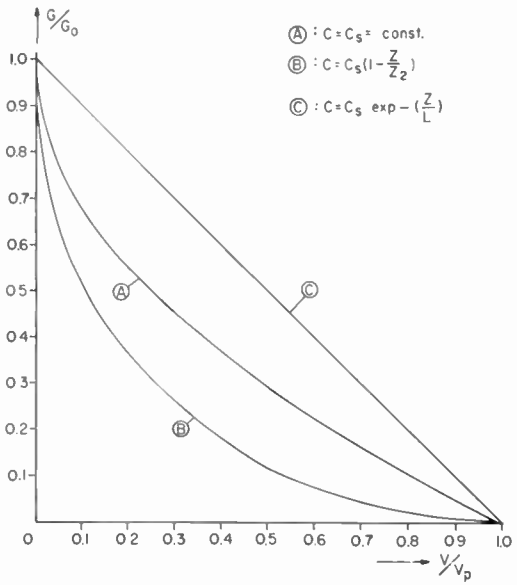

Fig. 4—Normalized sheet conductance as a function of the normalized gate voltage for the different cases shown in Figure 3.

concentration is given by the following equation:

$$C = C_s\left(1 - \frac{z}{z_2}\right) \tag{13}$$

A remote-cutoff device is obtained with this impurity distribution. Appendix A shows the general case in which the concentration can

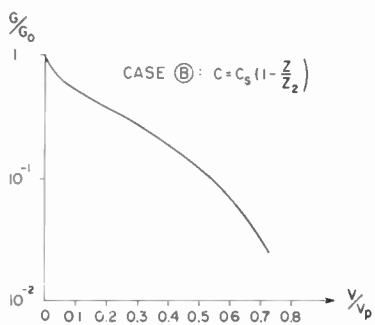

Fig. 5—Normalized sheet conductance as a function of the normalized gate voltage for case B (logarithmic scale).

be developed into a Taylor Series of the form

$$C = c_0 + c_1\left(\frac{z}{z_2}\right) + c_2\left(\frac{z}{z_2}\right)^2 + c_3\left(\frac{z}{z_2}\right)^3 + \cdots$$

The linear dependence of Equation (3) is obtained for an impurity distribution given by

$$C = C_s \exp\{-(z/L)\}, \tag{14}$$

where the diffusion length, L, is $2\sqrt{Dt}$ (see Appendix B). This distribution (case C in Figures 3 and 4) is difficult to achieve in practice. For a limited-source diffusion, the following impurity distribution is obtained:

$$C = \frac{2N_0}{\sqrt{\pi}L} \exp\{-(z/L)^2\} \approx \overline{C_s} \exp\{-(z/L)^2\}. \tag{15}$$

For an unlimited-source diffusion, the impurity distribution is given by

$$C = C_s\left[1 - \frac{2}{\sqrt{\pi}}\int_{z/L}^{z_2/L} \exp\{-z^2 dz\}\right] = C_s \operatorname{erfc}(z/L) \Big|_{z/L}^{z_2/L}. \tag{16}$$

Equations (15) and (16), both of which are exponential functions, have been used for the integration in Appendix B and the results are plotted in Figure 6. The figure shows that the error-function approximation given by Equation (16) more closely represents a linear relationship between g_m and the gate voltage.

The insert of Figure 7 shows a more typical case for experimental silicon field-effect transistors. Curve (a) shows calculated data for a mobility averaged over the concentration range from 1×10^{15} to 2×10^{16} cm^{-3}. Curve (b) shows data for a germanium field-effect transistor reported by Veloric and Greig, in which the dependence of the mobility on the concentration has been taken into consideration. Curve (c) shows similar data for silicon field-effect transistors.[2*]

Because the mobility decreases with concentration, it is plausible that a curve of case (c) may result. The difference between the more

[*] The author thanks J. C. Irvin for providing more accurate numerical data for this calculation.

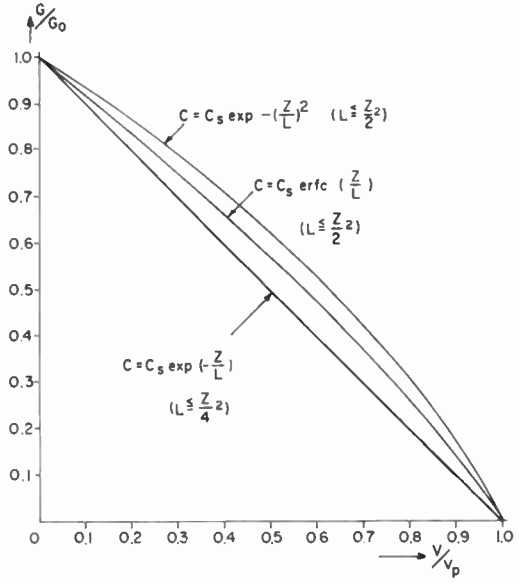

Fig. 6—Normalized sheet conductance as a function of the normalized gate voltage for three different related exponential functions.

exact cases for germanium and silicon in which the dependence of the mobility on the concentration was considered is not understood.

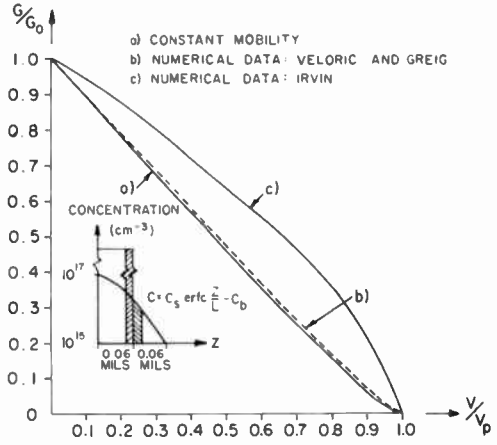

Fig. 7—Normalized sheet conductance as a function of the normalized gate voltage for a practical device: (a) calculated with an averaged mobility $\bar{\mu}$; (b) calculated using Veloric and Greig's data for germanium; (c) calculated using Irvin's data for silicon.

The experimental data seem to confirm more the distributions of the cases (a) and (b) than case (c) as shown in Figures 8 and 9.[4] The substrate bias may serve as an independent g_m control.

Other Approaches

Other methods of changing the transfer characteristics to obtain the remote-cutoff characteristic have certain disadvantages.

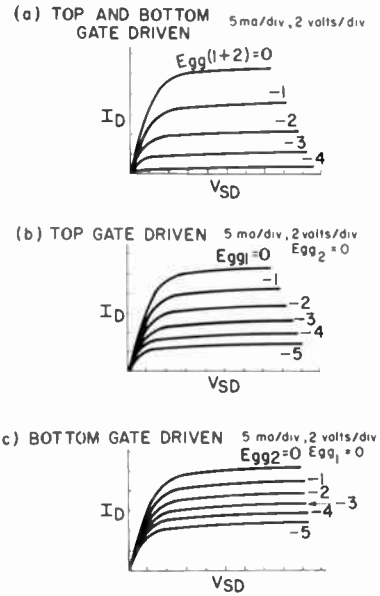

Fig. 8—Pentode-tube-like characteristics of experimental silicon field-effect devices.

If the diffusion penetration is tapered to make z_2 a function of y, certain regions will pinch off earlier than others. Furthermore, tapering is not easily controllable with diffusion techniques, which are essential for high-frequency transistors. With insulated-gate field-effect transistors, the thickness of the insulating layer may be tapered in either the x or the y direction to provide variable pinch-off characteristics.

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[4] W. A. Bösenberg, J. A. Olmstead, and K. Wybrands, "Design and Application of Silicon Unipolar Transistors made by Diffusion Techniques," I.R.E. Meeting on Electron Devices, Washington, D. C., Oct. 26-28, 1961.

Conclusions

The transfer characteristic of field-effect transistors can be tailored to a particular application. The desired cutoff characteristic can be most easily achieved by establishing proper impurity profiles in the channel region. Diffusion techniques provide complementary-error-function distributions and result in sharp-cutoff devices. Epitaxial techniques provide more freedom in designing the impurity profile and may be used to obtain remote-cutoff devices.

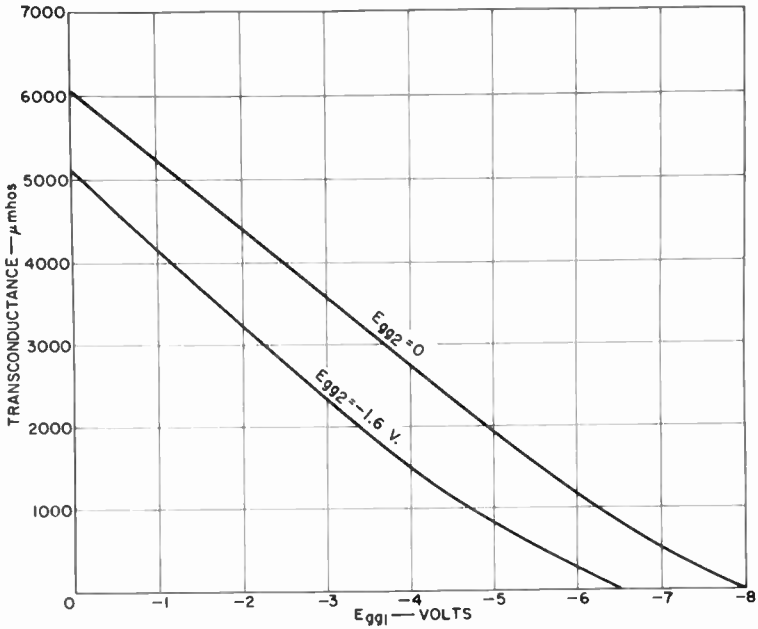

Fig. 9—Transfer characteristics of experimental silicon field-effect transistors having different bias values at gate 2.

Acknowledgments

Many helpful suggestions have been made by J. A. Olmstead. The experimental field-effect transistors were fabricated and measured by J. A. Olmstead, L. Krassner, J. H. Scott, and C. E. Sickles.

Appendix A—Taylor Series Development of Impurity Distribution

The following assumptions have been made for the calculations:

1. The gate doping is large compared with the channel doping. The space-charge layer spreads mostly into the channel.

2. The geometry of the electric field is one-dimensional.† Figure 2 shows the model which has been used in the calculations.

Derivation of Normalized Gate Voltage, V/V_p

The concentration C can be developed with a Taylor series such that

$$C = c_0 + c_1\left(\frac{z}{z_2}\right) + c_2\left(\frac{z}{z_2}\right)^2 + c_3\left(\frac{z}{z_2}\right)^3 + \cdots \qquad (17)$$

The space-charge layer moves into the channel a total length z_2 when the gate voltage is increased. At $z = z_2$, the channel is pinched off (the corresponding voltage is V_p); at lower voltages the space-charge layer ends at z (see Figure 2).

In order to obtain the relationship between V and z, Poisson's equation,

$$\frac{d^2V}{dz^2} = \frac{qC}{\epsilon\epsilon_0} \qquad (18)$$

must be integrated twice. (In Equation (18), q is the electronic charge and $\epsilon\epsilon_0$ is the absolute dielectric constant of the semiconductor material used.) An n-type channel is assumed in Equation (18). The following equation is obtained from the double integration:

$$V = K_2 + K_1 z + \frac{qz_2^2}{\epsilon\epsilon_0}\left[\frac{c_0}{2}\left(\frac{z}{z_2}\right)^2 + \frac{c_1}{6}\left(\frac{z}{z_2}\right)^3 + \frac{c_2}{12}\left(\frac{z}{z_2}\right)^4 + \frac{c_3}{4\times 5}\left(\frac{z}{z_2}\right)^5 + \ldots\right] \qquad (19)$$

The constants K_1 and K_2 are determined from the boundary conditions. At $z = 0$, $V = V_{\text{applied}} + V_0 = 0$; therefore $K_2 = 0$. A more rigorous calculation which takes the gate side into account reveals that K_1 must also be zero.

---

† Some cases with cylindrical geometry have been treated by Teszner[5] and by Marcus. There is one case with a cylindrical gate and a hollow cylindrical channel which will also give the desired properties of transconductance decreasing linearly with gate voltage.

[5] S. Teszner, "Le Tecnetron"—Nouveau Dispositif Semiconducteur, Amplificateur et Oscillateur,—International Congress of Solid State Physics and Its Applications to Electronics and Telecommunications, Brussels, June 2-7, 1958.

As stated previously, at the upper limit ($z = z_2$), $V = V_p$. Thus,

$$V_p = \frac{qz_2^2}{\epsilon\epsilon_0}\left[\frac{c_0}{2} + \frac{c_1}{6} + \frac{c_2}{12} + \frac{c_3}{4\times 5} + \cdots\right] \tag{20}$$

The equation for the normalized gate voltage, V/V_p, can then be obtained from Equations (19) and (20).

Derivation of the Normalized Sheet Conductance, G/G_0

The transconductance, g_m, is proportional to the sheet conductance, G. This latter term is defined by

$$G = q\int_z^{z_2} \mu(C)C(z)\,dz. \tag{21}$$

The mobility μ is concentration dependent. Some numerical expressions have been given by Veloric and Greig[1] for germanium and by Irvin[2] for silicon. In the case being considered here, the concentration dependence may be neglected, and the mobility is considered to have an average velocity $\bar{\mu}$. Then the equation for the conductance becomes

$$G = \bar{\mu}q\int_z^{z_2} C(z)\,dz. \tag{22}$$

On integrating,

$$G = \bar{\mu}q\,z_2\left[K_3 + c_0\left(\frac{z}{z_2}\right) + \frac{c_1}{2}\left(\frac{z}{z_2}\right)^2 + \frac{c_2}{3}\left(\frac{z}{z_2}\right)^3 + \frac{c_3}{4}\left(\frac{z}{z_2}\right)^4 + \cdots\cdots\right] \tag{23}$$

The integration constant, K_3, is determined from the boundary condition that, at $z = z_2$, $G = 0$. Equation (23) then becomes

$$G = \bar{\mu}qz_2\left\{c_0\left[1-\left(\frac{z}{z_2}\right)\right] + \frac{c_1}{2}\left[1-\left(\frac{z}{z_2}\right)^2\right] + \frac{c_2}{3}\left[1-\left(\frac{z}{z_2}\right)^3\right] + \frac{c_3}{4}\left[1-\left(\frac{z}{z_2}\right)^4\right] + \cdots\cdots\right\}. \tag{24}$$

At $z = 0$, the highest sheet conductance, G_0, is obtained;

$$G_0 = \bar{\mu} q z_2 \left(c_0 + \frac{c_1}{2} + \frac{c_2}{3} + \frac{c_3}{4} + \cdots\cdots\cdots \right). \tag{25}$$

The equation for the normalized sheet conductance, G/G_0, follows from Equations (24) and (25).

Appendix B—Exponential and Related Impurity Distributions

Exponential Function

An impurity concentration of the form

$$C = C_s \exp\left\{ -\frac{z}{L} \right\} \tag{26}$$

has been assumed (see Figure 2). To obtain the relationship between V and z, Poisson's Equation,

$$\frac{d^2V}{dz^2} = \frac{C_s q}{\epsilon\epsilon_0} \exp\left\{ -\frac{z}{L} \right\}$$

must be integrated twice. The resultant equation is

$$V = K_3 + K_4 z + \frac{C_s q L^2}{\epsilon\epsilon_0} \exp\left\{ -\frac{z}{L} \right\} \tag{27}$$

For $z = 0$, $V = 0$; therefore,

$$K_4 = \frac{C_s q L^2}{\epsilon\epsilon_0}. \tag{28}$$

For $z_2 \gg L$, $dV/dz = 0$; therefore,

$$K_5 = 0.$$

Equation (27) then becomes

$$V = \frac{+C_s q L^2}{\epsilon\epsilon_0} \left[1 - \exp\left\{ -\frac{z}{L} \right\} \right]. \tag{29}$$

For $z = z_2 \gg L$, the gate voltage, V, is equal to the pinch-off voltage, V_p. Thus,

$$V_p = \frac{C_s q L^2}{\epsilon\epsilon_0}. \tag{30}$$

Then,

$$\frac{V}{V_p} = 1 - \exp\left\{-\frac{z}{L}\right\}. \tag{31}$$

The sheet conductivity can be computed by integrating the following equation:

$$Q = q\int_{z}^{z_2} \mu(C)C(z)\,dz = q\bar{\mu}C_s \int_{z}^{z_2} \exp\left\{-\frac{z}{L}\right\}\, dz. \tag{32}$$

The result is

$$G = q\bar{\mu}LC_s \exp\left\{-\frac{z}{L}\right\} + K_6; \tag{33}$$

for $z = z_2 \gg L$, $G = 0$; therefore, $K_6 = 0$.

For $z = 0$,

$$G_0 = q\bar{\mu}LC_s, \tag{34}$$

$$G/G_0 = \exp\left\{-\frac{z}{L}\right\} \tag{35}$$

If the relationship expressed by Equation (31) is substituted in Equation (35), the following equation is obtained:

$$\frac{G}{G_0} = 1 - \frac{V}{V_p}. \tag{36}$$

This is the desired relationship for sharp-cutoff devices.

Error-Function Distribution

By means of impurity diffusion, two distributions may be achieved easily. For a limited source, the distribution is given by

$$C = \frac{N_s}{\sqrt{\pi Dt}} \exp\left\{-\left(\frac{z}{L}\right)^2\right\} \tag{37}$$

where N_s is the initial concentration per unit area. For constant surface concentration C_s, the distribution is given by

$$C = C_s \operatorname{erfc}\left(\frac{z}{L}\right) = C_s\left[1 - \frac{2}{\sqrt{\pi}} \int_{u=z/L}^{\infty} \exp\{-u^2\}\, du\right]. \tag{38}$$

In the first case, the quantity $N_s/\sqrt{\pi Dt}$ usually varies only slowly with time, and its influence on concentration is not nearly so great as that of the exponential function. Thus, for a limited source, an approximation of the distribution is

$$C = C_s \exp\left\{-\left(\frac{z}{L}\right)^2\right\} \tag{37a}$$

Of more importance is the impurity distribution given by Equation (38). For practical cases, the background concentration, C_b, is not negligible. Therefore, the distribution expressed as

$$C = C_s \operatorname{erfc}\left(\frac{z}{L}\right) - C_b = C_s\left[\operatorname{erfc}\left(\frac{z}{L}\right) - K\right] \tag{38a}$$

is more accurate. ($K = C_b/C_s$, see Figure 2.)

Again, Poisson's equation,

$$\frac{d^2V}{dz^2} = \frac{C_s q}{\epsilon\epsilon_0}\left[\operatorname{erfc}\left(\frac{z}{L}\right) - K\right], \tag{39}$$

must be integrated twice. The double integration of Equation (39) yields the following equation:

$$V = \text{Const} + \frac{qC_sL^2}{\epsilon\epsilon_0}\left[\int_{v=z_2/L}^{v=z/L}\int_{u=z_2/L}^{u=z/L} \operatorname{erfc} u\, du\, dv - \frac{K}{2L^2}(z - z_2)^2\right]. \tag{40}$$

At $z = z_2$, $V = V_p$; thus, V_p is equal to the constant of integration. At $z = z_1$, $V = 0$. Then,

$$V_p = \frac{qC_s L^2}{\epsilon\epsilon_0}\left[\int_{v=z_2/L}^{v=z_1/L}\int_{u=z_2/L}^{u=z_1/L} \operatorname{erfc} u\,du\,dv - \frac{K}{2L^2}(z_1 - z_2)^2\right], \tag{41}$$

The equation for V/V_p is obtained from Equations (40) and (41). The transconductance is again proportional to the sheet conductance, G, which is given by

$$G = q\int_{u=z_2}^{u=z} \mu(C)C\,dz = C_s q\bar{\mu}L\left[\int_{u=z_2/L}^{u=z/L} \operatorname{erfc} u\,du - K\left(\frac{z - z_2}{L}\right)\right]. \tag{42}$$

For $z = z_1$, the sheet conductance has its maximum value, G_0;

$$G_0 = -C_s q\bar{\mu}L\left[\int_{u=z_2/L}^{u=z_1/L} \operatorname{erfc} u\,du - K\left(\frac{z_1 - z_2}{L}\right)\right], \tag{43}$$

and the equation for G/G_0 derives from Equations (42) and (43). Because both V/V_p and G/G_0 are dependent only on z/L as a parameter, it is possible to plot G/G_0 as a function of V/V_p.

In order to perform the evaluations, tables of the following functions were made up:

$$\exp\{-u^2\}$$

$$\operatorname{erfc} u$$

$$\int_u^\infty \operatorname{erfc} v\,dv$$

$$\int_u^\infty\int_v^\infty \operatorname{erfc} t\,dt\,dv.$$

These functions were tabulated in increments of 0.01 up to $u = 4.00$.*

* A limited number of copies of these tables are available on request; requests should be addressed to *RCA Review*, RCA Laboratories, Princeton, N. J.

LAMINATED FERRITE MEMORY*

By

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Summary—*The batch fabrication technology and 100-nanosecond-cycle operating characteristics of monolithic ferrite sheets with integrated windings are described. The fabrication technology is based on embedding printed conductors on doctor-bladed ferrite sheets and laminating and sintering the sheets to form an array.*

Introduction

THIS PAPER describes a random-access magnetic memory consisting of a monolithic sheet of ferrite with embedded conductors made by a simple batch-fabrication technique—lamination of ferrites. Its tightly packed elements with closed flux paths of only two to three mils in equivalent diameters are the smallest yet realized by any technique. This smallness is being exploited for high speed. Cycle times as short as 100 nanoseconds have been demonstrated. The smallness of the elements leading to modest drive requirements of only a few tens of milliamperes combined with the inherently low cost "integrated" batch-fabrication technique opens the possibility of low-cost memories of very large capacities—tens or hundreds of millions of bits. A significant cost reduction for the whole memory system is possible because this type of magnetic structure lends itself particularly well to fabrication with integrated semiconductor driving and sensing circuits.

A few general remarks may help to set the subject in perspective within the rapidly advancing art of computer memories. The usefulness of a digital computer depends to a large extent on the speed and storage capacity of its random-access memory. In general, the maximum attainable capacity decreases with increasing speed.[1] Capacities in the range of a few million bits at a cycle time of a few microseconds have been obtained with ferrite cores.

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* This paper was presented at the Fall Joint Computer Conference, Las Vegas, Nev., Nov. 12-14, 1963.

[1] J. A. Rajchman, "Computer Memories—Possible Future Developments," *RCA Review*, Vol. 23, No. 2, p. 137, June 1962.

Recently, the feasibility of a 100 nanosecond cycle-time (i.e., 10 mc repetition rate) ferrite system was established[2] and microferrite memories with a cycle time of 375 nanoseconds are commercially available.[3] These results have extended the usefulness of the well-established ferrite technology to the high speeds which were the original goals motivating much of the efforts with thin magnetic metallic films. Ferrite systems with these capabilities are obtained by miniaturization of the element and increasing the density of appropriate "printed" microscopic windings. Impulse or partial switching is used in addition to miniaturization to further reduce the magnetic size of the storage element below its physical size. In a sense, the laminated technology presented here is a culmination of our recent efforts[2,3] to reduce the element size by providing a means of making small elements and all necessary windings in a single step.

Elements with closed magnetic paths can provide a relatively higher ratio of sense voltage to drive current than open-flux-path elements. Furthermore, there are no limitations to geometrical shapes due to demagnetizing effects, and there are no fringing fields limiting packing density. To obtain some of these benefits with thin-film technology, paired patches are resorted to in many of the more recent approaches.[4]

The successful development of integrated magnetic structures with elements having closed magnetic flux paths includes the aperture ferrite plate,[5] the FLEA permalloy sheet,[6] and the waffle-iron memory.[7] It is believed that the laminated ferrite memory is a further step in this integration, providing smaller elements at much lower cost.

The paper describes the fabrication methods, the results obtained with the magnetic structures, and some speculations on the possibility of integrated semiconductor drives.

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[2] R. Shahbender, T. Nelson, R. Lochinger, and J. Walentine, "Micro-aperture High-Speed Ferrite Memory," *RCA Review*, Vol. 23, No. 4, p. 539, Dec. 1962.

[3] H. Amemiya, H. P. Lemaire, R. L. Pryor, and T. R. Mayhew, "High Speed Ferrite Memories," *Proc. Fall Joint Computer Conference*, p. 184, 1962.

[4] A. V. Pohm, R. J. Zingg, G. A. Watson, T. A. Smag, and R. M. Stewart, Jr., "Large High Speed, DRO Film Memories," *Proc. INTERMAG Conference*, p. 9-5-1, April 1963.

[5] J. A. Rajchman, "Ferrite Apertured Plate for Random Access Memory," *Proc. I.R.E.*, Vol. 45, p. 325, March 1957.

[6] G. R. Briggs and J. W. Tuska, "Design and Operating Characteristics of a High-Bit Density Permalloy Sheet Transfluxor Memory Stack," *Proc. INTERMAG Conference*, p. 3-4-2, April 1963.

[7] T. R. Finch and A. H. Bobeck, "The Waffle Iron Store," *International Solid-State Circuits Conference Digest of Technical Papers*, p. 12, 1963.

Orthogonal Array Structure

The laminate technology permits a great flexibility in the geometries of the windings. The simple orthogonal winding structure shown in Figure 1 is particularly suited for high speed, and is described in detail. In this structure two orthogonal sets of conductors, an

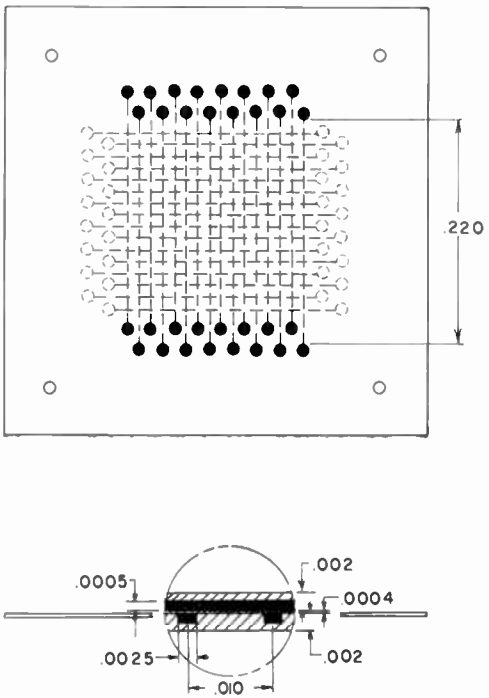


Fig. 1—Laminated-array structure.

X-directed set and a Y-directed set, are embedded in a sheet of square-loop ferrite. The conductors are electrically insulated from one another by ferrite. Each cross-over point between an X and a Y conductor is a storage location. For high speed the array is operated using impulse switching in a word-organized, two crossovers per bit mode, analogous to the word-organized two cores per bit[5] mode of conventional arrays. The word current (read–write) is applied to an X-winding, and the Y-windings are used for both digit and sense.

The experimental arrays fabricated to date have a capacity of 256 crossovers (128 bits is equivalent to 16 words of 8 bits each). The over-all thickness of the ferrite laminate is approximately 5 mils, and

the conductor spacing for both the X and Y conductors is 10 mils. The conductor cross-sectional dimensions are approximately 2.5 × 0.7 mils.

Memory Fabrication Technology

The basic operations involved in the fabrication of a laminated memory array are doctor blading, laminating and sintering, and conductor screening.

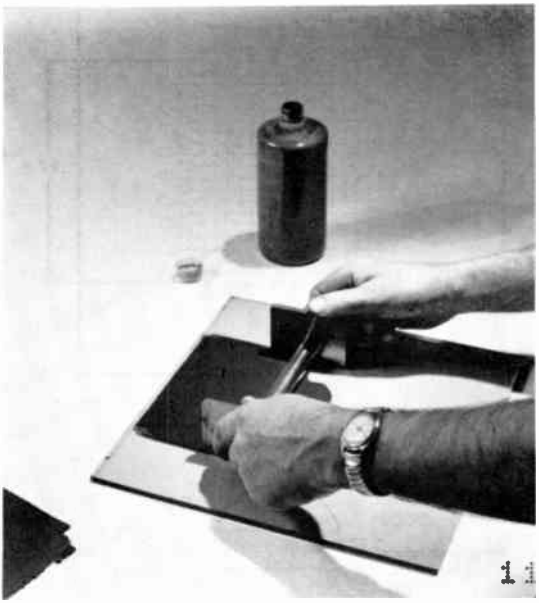


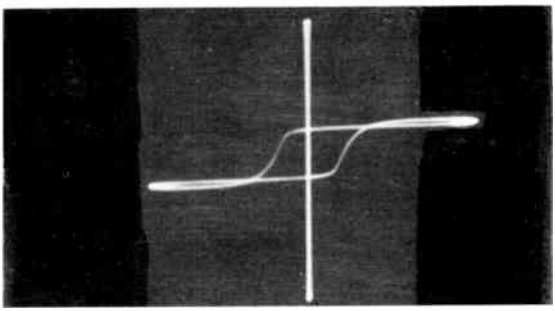
Fig. 2—Doctor blading ferrite.

Doctor Bladed Ferrites

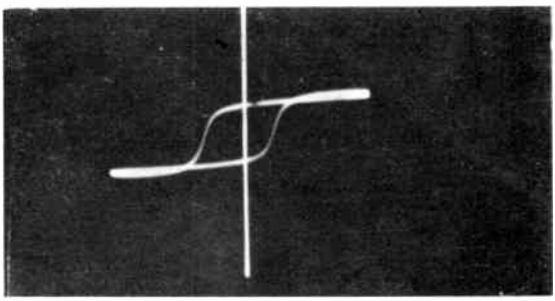
The doctor blading (DB) technique for fabricating sheets of ferrites consists of preparing a slurry of the desired ferrite powder and appropriate organic binders. The slurry is spread in an even layer on a glass substrate by the sweeping action of a blade, called a doctor blade, held at a fixed distance above the glass surface as shown in Figure 2. The sheet is air dried and peeled from the glass surface.

The 60-cycle hysteresis loops for toroids of the same composition fabricated conventionally (dry pressing) and by DB, and fired simultaneously are shown in Figure 3. The saturation flux for both types of cores is essentially the same. The coercive force for the DB cores is somewhat higher than that for the dry-pressed cores when both are

fired under the same conditions. However, by modifying the firing schedule for the DB cores, the resulting characteristics are the same as those of dry-pressed cores. The pulse behavior of DB cores is again essentially the same as that of dry-pressed cores (equal switching coefficients).



(a)



(b)

Fig. 3—Hysteresis loop of (a) pressed ferrite core and (b) doctor-bladed ferrite core.

Laminated Ferrites

Monolithic structures with embedded conductors are fabricated by laminating together the required number of sheets. This is accomplished by pressing "green" sheets together at moderate pressures and temperatures which are not too critical. A simple hydraulic press with heated platens is adequate for this purpose. The ferrite sheets are sandwiched between two aluminum blocks, as shown schematically in Figure 4, and placed between the heated platens of the press. Pressure is applied for a few minutes after the block temperature, as

monitored by a thermocouple, has stabilized. The laminated sheets are next sintered in a controlled-temperature furnace.

Multiple lamination was tested with many layers. For example, a sample consisting of a total of 60 sheets, each of 2.5 mils thickness, was successfully laminated and fired. Figure 5 shows a micrograph of a section through the sample which contains an 8×8 matrix of embedded conductors whose ends can clearly be seen. Inspection of

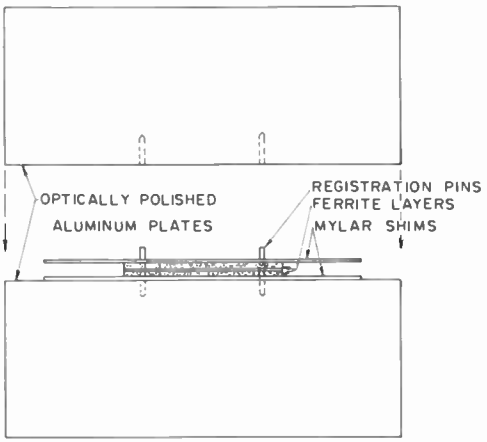


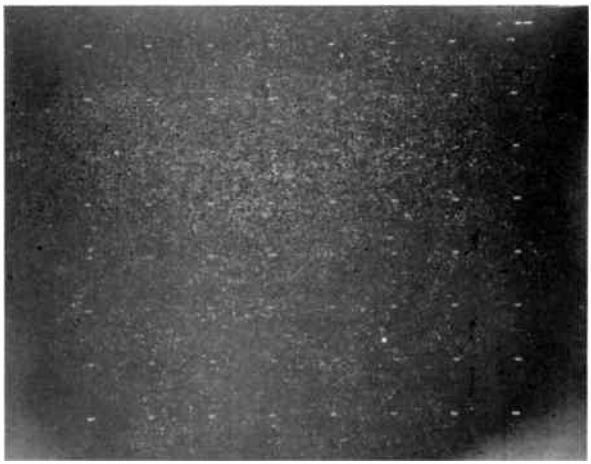
Fig. 4—Laminating jig.

the micrograph shows a uniform ceramic body with no delamination marks. Magnetic testing of this and similar samples in which the flux is switched across the laminating plane leads to the same results as when the flux is switched in the plane of the original doctor-bladed ferrite sheets. In other words, a truly uniform isotropic material is obtained.

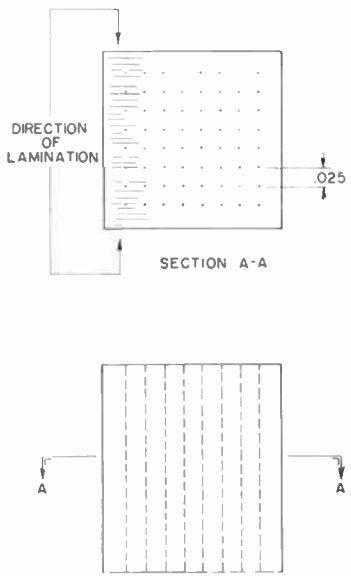
Experiments with dimensional stability were made using sheets of 5×10 inches and thicknesses varying from 0.1 to 10 mils. It was found that properly sintered samples cut from these sheets could be relied on to have all their dimensions within $\pm$ 5 per cent. Better tolerances were obtained under special conditions. For example, the sample of Figure 5 had spacing between conductors as shown in Figure 6. It is seen that variations in spacings are only $\pm$ 0.5 mil for a nominal spacing of 0.025 inch.

Conductor Screening

The technique developed for forming conductors as an integral



(a)



(b)

Fig. 5—Thick laminate: (a) micrograph of section and (b) side and top view.

part of a green ferrite sheet is similar to the familiar silk-screening process. A photoformed metal mask is laid on a glass substrate and a paste consisting of the required metal powder and a binder is squeegeed through the mask onto the glass substrate. The mask is then removed leaving the required conductor pattern on the glass surface. Ferrite is doctor bladed on the glass substrate over the conductor pattern. When peeled off the glass, the ferrite sheet contains the conductors intimately embedded in it and flush with its surface.

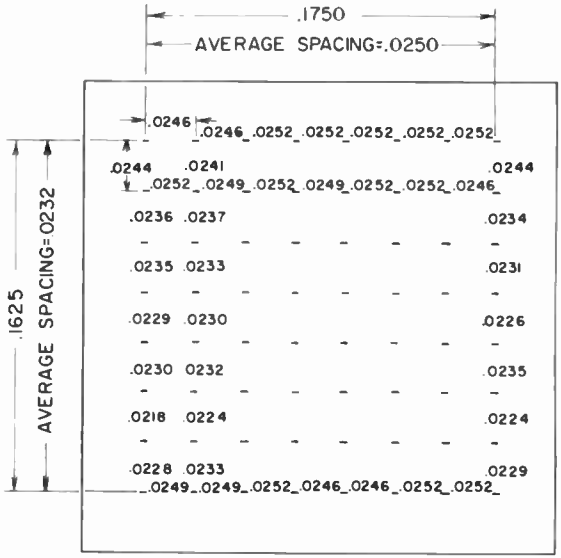


Fig. 6—Dimensions of thick laminate.

Similar ferrite sheets with conductors, or spacer sheets without conductors, are then laminated, as described above. On firing, the conductors sinter along with the ferrite.

Conductors as small as 1.3 × 0.5 mils in cross section and with a resistance of 2 ohms per inch have been obtained as shown in Figure 7. For most of the arrays tested, the conductor cross section is 2.5 × 0.7 mils, as shown in Figure 8, and their resistance is 3 ohms per inch.

Orthogonal Array Fabrication

A number of 16 × 16 experimental arrays were made. The orthogonal array structure, as shown in Figure 1, is fabricated by laminating three sheets of doctor-bladed ferrite in the order shown in Figure 9.

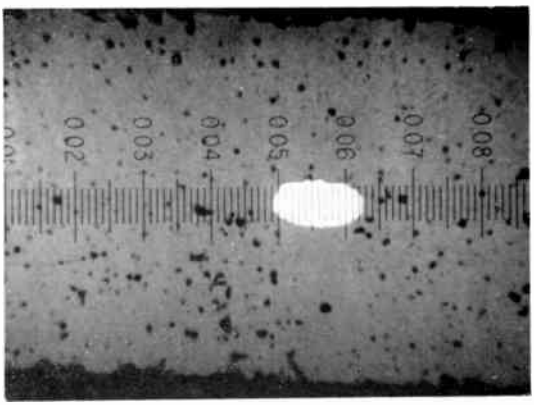


Fig. 7—1.3 × 0.7 mil conductor section.

The top and bottom sheets, with a "green" thickness of approximately 2.5 mils, contain conductors spaced 13 mils apart.

The center sheet is 0.5 mil thick and contains no conductors. Sixteen-mil-diameter holes are gang punched in each sheet in the patterns shown in Figure 9. The rows of holes are used as access to the embedded conductors. The corner holes are used for registry during assembly and match the pin locations in the laminating jig of Figure 4. After sintering, the ferrite laminate shrinks to the dimensions shown in Figure 1 (over-all thickness approximately 5 mils, conductor spacing 10 mils).

Interconnections to the embedded conductors are provided via the plastic film with etched conductors shown in Figure 10. The conduc-

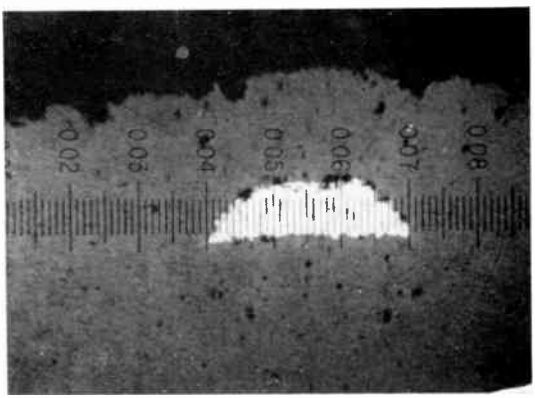


Fig. 8—3.0 × 0.8 mil conductor section.

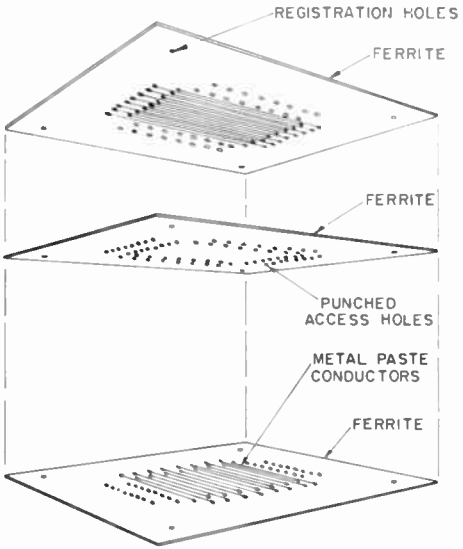


Fig. 9—Laminate details.

tors, spaced on 10 mil centers, overhang the plastic film and are positioned over the access holes. They are then manually soldered in place. Figure 11 shows a 16 × 16 array mounted on a printed circuit board ready for testing. Figure 12 is a magnified x-ray photograph of an

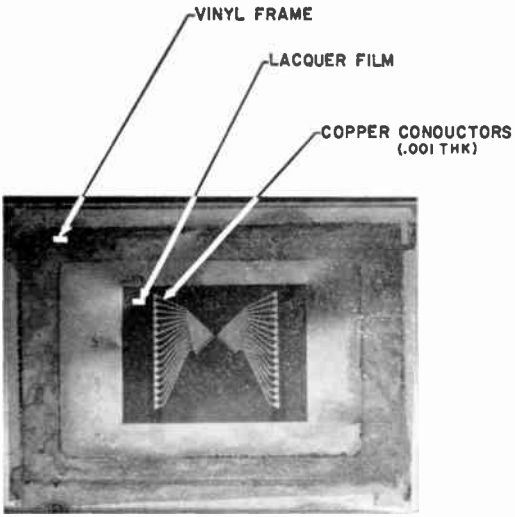


Fig. 10—Interconnecting conductors.

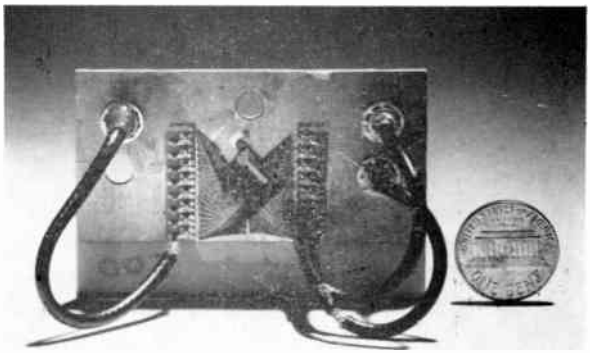


Fig. 11—16 × 16 array mounted for test.

array. Figure 13 is a partial cross section of some of the embedded conductors and shows the monolithic nature of the ferrite without any trace of the lamination.

Operating Mode

The memory is word organized, and two crossovers per bit are used. In this mode all bits of a selected word are subjected to the same

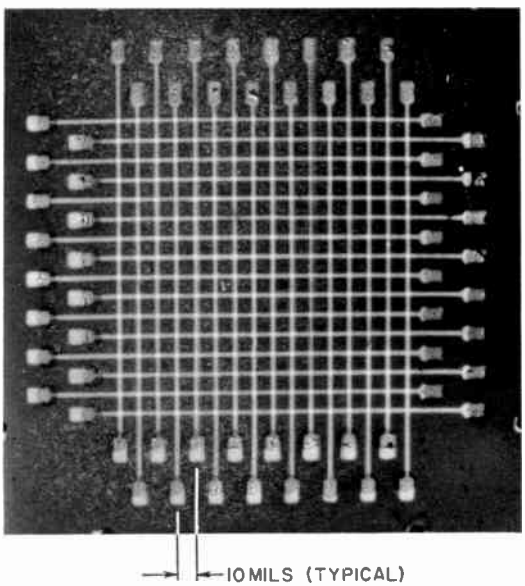


Fig. 12—Magnified x-ray photo of array.

read–write current pulses. The best digit drive techniques[2] found consist of applying a unipolar digit pulse to either one of the two crossovers of a bit in time coincidence with the write pulse. In other words, if the two crossovers of a bit are labeled A and B, crossover A is digited with, say, a positive pulse to write a binary "1" and crossover B is digited with a positive pulse, also, to write a binary "0".

Sensing is differential in that the output sense voltage obtained during the read is the difference between the two voltages induced along the digit sense windings linking the two crossovers of a bit. Different polarities of voltage correspond to the two binary states.

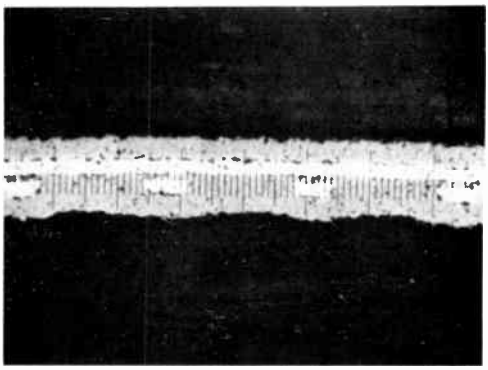


Fig. 13—Micrograph of partial cross section of array.

Because of the orthogonal disposition of word and digit conductors, word read–write currents switch flux along a selected word conductor that does not link the digit conductor. A digit pulse applied to a digit conductor in time coincidence with a write pulse switches a component of flux mutual to both the word and digit conductors at the corresponding crossover point. The application of a read pulse switches this mutual flux and induces a sense voltage in the digit winding. The polarity of the induced sense voltage is determined by the polarity of the applied digit current.

Operation of a bit may be visualized with the aid of the vector diagrams shown in Figure 14. The flux switched by the word-write current in the vicinity of a crossover point may be represented by the vector ϕ_w. The magnitude of this vector is proportional to the flux contributing to the bit operation. The direction of this vector is normal to the plane of the flux itself and, using the right-hand rule convention, is in the direction of the current establishing the flux. The application

of a digit current in time coincidence with the write pulse causes the vector ϕ_w to tilt to ϕ_t in the direction of the digit current, i.e., to have a component in the digit direction, as shown in Figure 14.

Application of the word-read current reverses the flux vector ϕ_t to the position ϕ_r resulting in a sense output. Increasing the amplitude of the digit current relative to the write current increases the tilt

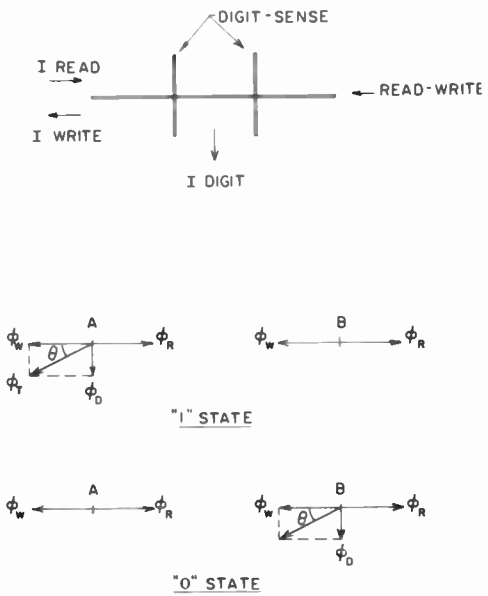


Fig. 14—Flux vector diagram.

angle and, correspondingly, the sense output. The amplitude of the digit current is limited by its disturbing effect on the stored information.

System Analysis

The high-speed performance of the orthogonal array structure may be predicted from the known ferrite characteristics and some simplifying assumptions. Starting with the switching equation[8]

$$T_s (H - H_c) = S_w$$

[8] N. Menyuk and J. B. Goodenough, "Magnetic Materials for Digital Computer Components," *Jour. Appl. Physics*, Vol. 26, No. 1, p. 8, 1955.

where T_s = switching time,

H = applied magnetic reversing field,

H_c = coercive field of ferrite used,

S_w = switching coefficient of ferrite used,

an estimate of the required word-writing current may be made. For optimum operation the write-current magnitude is adjusted to completely switch along the perimeter of the word conductor and to partially switch beyond. From the switching equation, the optimum write current is

$$I_w = 2\pi R_0 \left[\frac{S_w}{T_s} + H_c \right]$$

where $2\pi R_0$ = cross-sectional perimeter of the word conductor.

The amount of inelastic flux partially switched by the word-write current per crossover (flux vector ϕ_w in Figure 14) may be estimated by assuming an inverse relationship between flux switched and switching time. In other words if B_r is the remanent saturation flux of the ferrite, then the flux B partially switched by I_w at a radius r is

$$B = K \frac{B_r}{r}.$$

The proportionality constant K is determined from the condition that at

$$r = R_0, \quad B = B_r.$$

The total inelastic flux switched by I_w per crossover is

$$\phi_w = Kl \int_{R_0}^{R} \frac{B_r}{r}\, dr = KlB_r \ln \frac{R}{R_0},$$

where R = outside radius to which flux is switched,

l = spacing between conductors.

The back voltage V_w induced on the word drive line per crossover due to the write current switching the inelastic flux from $-\phi_w$ to $+\phi_w$, and assuming a peaking factor of 2, is

$$V_w = \frac{2(2\phi_w)}{T_s}.$$

For the sample assumptions, the back voltage V_{wc} due to the elastic flux switched by the word write current is

$$V_{wc} = \frac{4\phi_w}{T_s}\frac{1-S}{S},$$

where S is the squareness ratio of the ferrite defined as the ratio of the remanance flux to the saturation flux.

The digit current causes the flux vector ϕ_w (Figure 14) to tip through an angle θ which, for small θ, is

$$\theta \simeq \frac{I_d}{I_w}.$$

The flux contributing to the sense output is

$$\phi_s = \phi_w \tan\theta \simeq \phi_w \frac{I_d}{I_w}.$$

The expected sense output voltage V_s due to tne switching of the flux ϕ_s by a read current I_r from $+\phi_s$ to a neutral state (assuming the same peaking factor of 2) is

$$V_s = \frac{2\phi_s}{T_s}\frac{I_r}{I_w} = \frac{2\phi_w}{T_s}\frac{I_d I_r}{I_w^2}.$$

The value of digit current I_{dm} at which disturb effects are initiated is determined by the coercive force of the material. For this digit current to disturb stored information, it must switch flux linking the word conductor. The minimum path length, P, along which this occurs is defined by the conductor dimensions and their separation;

$$P = 2w + 4t + 2d,$$

where

w = conductor width,

t = conductor thickness,

d = separation between conductors.

The disturbing digit current is given by

$$I_{dm} \propto H_c P.$$

Digit current values greater than I_{dm} may be used if a slight disturb in sense outputs can be tolerated. This is especially true in a system where the sense outputs are bipolar.

The back voltage induced on the word line, per crossover, due to the read current I_r switching both inelastic and elastic flux is

$$V_r = (V_w + V_{wc}) \frac{I_r}{I_w}$$

$$= \frac{4\phi_w}{T_s} \frac{I_r}{I_w} \frac{1}{S}.$$

The resistive drop in the conductor must be added to the above to compute the required driving voltage.

For the ferrite selected for the laminated memory,[2] and for 100 nanoseconds cycle time, the following values may be used in the preceding equations:

$$H_c = 1 \text{ oersted},$$

$$S_w = 0.3 \times 10^{-6} \text{ oersted-second},$$

$$B_r = 10^3 \text{ gauss},$$

$$T_s = 30 \times 10^{-9} \text{ second},$$

$$S = 0.7,$$

$$w = 2.5 \text{ mils},$$

$$t = 0.5 \text{ mil},$$

$$R_0 = \frac{6}{2\pi} \text{ mils},$$

$$R = 1.75 \text{ mils},$$

$$d = 0.4 \text{ mil},$$

$$l = 10 \text{ mils}.$$

Substituting these values in the above equations leads to

$$I_w = 132 \text{ ma},$$

$$\phi_w = 3.6 \times 10^{-2} \text{ maxwell},$$

$$V_w = 4.8 \times 10^{-2} \text{ volt},$$

$$I_{dm} = 16 \text{ ma}.$$

Assuming a read current of 300 ma, and a digit current of 20 ma, the sense output and back voltage per crossover are

$$V_s = 8.3 \times 10^{-3} \text{ volt},$$

$$V_r = 1.56 \times 10^{-1} \text{ volt}.$$

The characteristics of the digit-sense winding may be estimated by computing L, the distributed inductance per crossover, and C, the total capacitance per crossover. These quantities are

$$L \propto \mu l \ln \frac{R}{R_0},$$

$$C \propto \frac{\epsilon A}{d} + \frac{\epsilon w l}{R},$$

where μ = small-signal relative permeability of ferrite,

ϵ = relative dielectric constant of ferrite,

$A = w^2$ = crossover area between a word and a digit conductor.

The characteristic impedance Z_0, and delay per bit τ_d for the sense digit line are approximately given by

$$Z_0 \approx \sqrt{\frac{L}{C}} \text{ ohms},$$

$$\tau_d \approx \sqrt{LC} \text{ seconds}.$$

For the ferrites used in the laminated memory and at frequencies compatible with 10-mc operation, the following values may be used:

$$\mu = 100,$$

$$\epsilon = 10,$$

leading to

$$L = 3 \times 10^{-9} \text{ henry},$$

$$C = 6.6 \times 10^{-14} \text{ farad},$$

$$Z_0 = 214 \text{ ohms},$$

$$\tau_d = 1.4 \times 10^{-11} \text{ second/bit}.$$

Experimental Data

Ferrite Composition

The composition selected for the high-speed laminated array is the same as that in use for the previously developed high-speed ferrite memories.[2,3] The switching coefficient for this material is 0.3 oersted-microsecond, the coercive force is 1.0 oersted, the Curie temperature is 100°C, and the squareness ratio is 0.7. The magnetic characteristics achieved with this material using doctor blading and laminating techniques are identical to those of conventionally processed toroids.

With different materials other operational characteristics could be obtained. For example, power requirements can be very low using a switchable ferrite with low coercivity, e.g., one half oersted. Also, recently developed wide temperature range material could be used.[9]

Array Operation

Three basic pulse programs are used to evaluate the performance of an array. These are

(1) alternate one-zero read–write,

(2) alternate one-zero read–write with disturbs,

(3) mixed one's and zero's read–write with disturbs.

These programs are provided by a set of transistor drivers (described in detail in Reference (2)) triggered by commercially available 10-mc logic building blocks. The read–write and digit pulses are of adjustable amplitude, 30 nanoseconds wide at the base with a maximum repetition rate of 10 mc.

Figure 15 shows the circuit layout used to test the array operation. Individual words are connected to the read–write drivers, and digiting is accomplished via the resistors connected to the sense-digit lines. A sense output transformer with a 1:1 turns ratio (10 turns on each side) wound on a ferrite bead is used to obtain the difference signals. The reactance of the transformer is considerably higher than the impedance to ground presented by the sense-digit lines for 16×16 arrays. Thus the shunting effect produced by the transformer in series with the undigited side on an applied digit pulse is negligible.

Alternate One-Zero Read–Write

In this program an alternating pattern of one and zero is cyclicly written into and read out of the memory bit at a cycle time of 100

[9] E. G. Fortin and H. Lessoff, "Temperature-Stable Ferrites for Memory Applications," *Proc. INTERMAG Conference*, p. 1, April 1963.

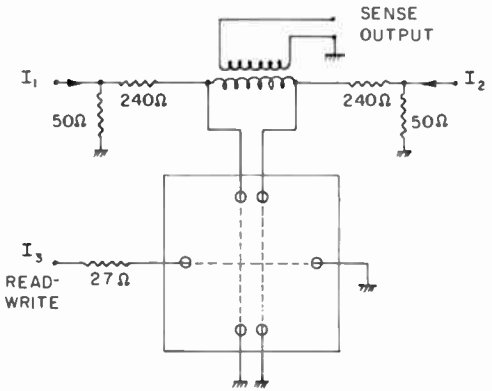


Fig. 15—Memory-array test schematic.

nanoseconds and a repetition rate up to 10 mc. Figure 16 shows the pulse program used and Figure 17 shows oscillograms of the voltage developed at the sense output terminals under constant drive conditions and at three different repetition rates: 0.05, 2.0, and 7.2 mc. The one and zero outputs are shown superimposed at the lower repetition rates. Inspection of Figure 17 shows that the sense voltage is independent of repetition rate. The operating current levels and sense outputs are

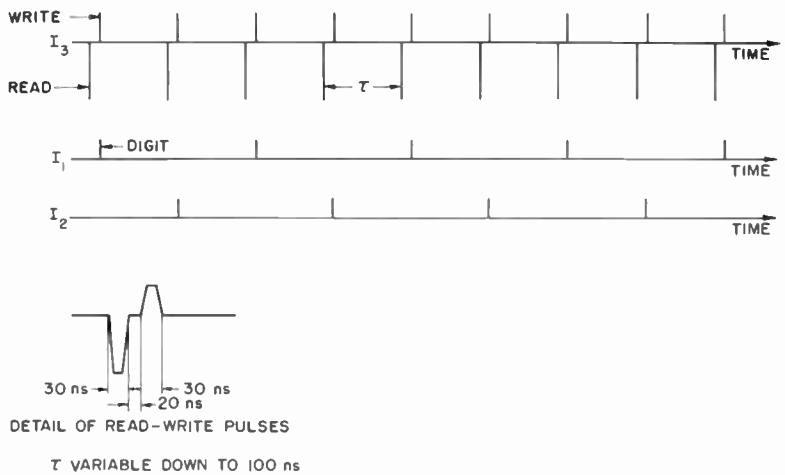


Fig. 16—Alternate one and zero pulse program.

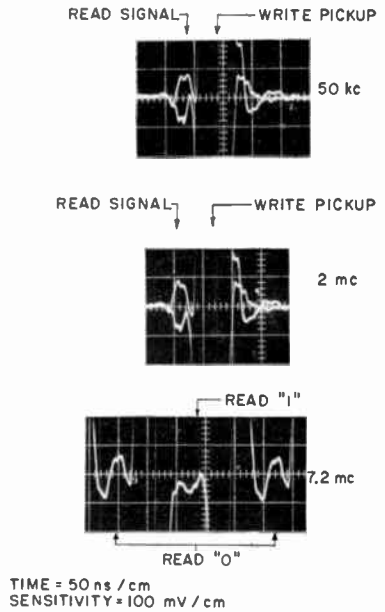


Fig. 17—Sense output voltages at 50 kc and 2 and 7.2 mc (pulse program of Figure 16).

read current = 370 ma,

write current = 220 ma,

digit current = 21 ma,

undisturbed sense output = ±9 mv,

back voltage per crossover (including IR drop) = 340 mv.

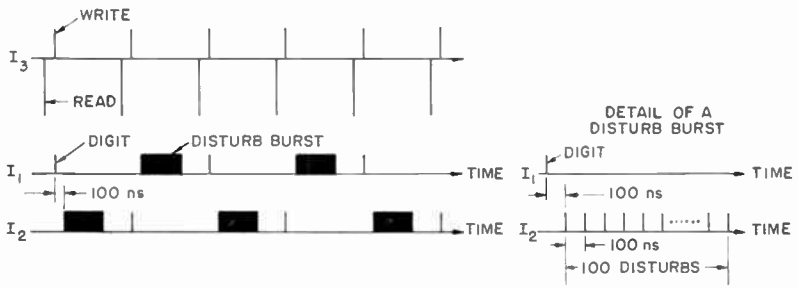


Fig. 18—Alternate one and zero with disturbs pulse program.

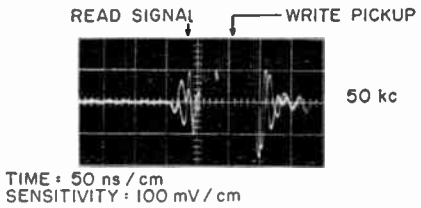


Fig. 19—Sense output voltages with 10 mc disturbs (pulse program of Figure 18).

Alternate One-Zero Read–Write with Disturbs

In this program an alternating pattern of one and zero is cyclicly written into the memory bit. Each write operation prior to reading is followed by the application of disturb pulses aimed at destroying the stored information. Figure 18 shows the pulse program and Figure 19 shows oscillograms of the voltage developed at the sense output terminals for the same current drive levels as above.

The disturbed sense voltages are ±6 mv, a decrease of 3 mv due to the digit disturbs. It was determined experimentally that 3×10^5 disturb pulses produced no additional disturb effects as compared to only 100 pulses.

Mixed One-Zero Read–Write with Disturbs

The pulse program described in the preceding paragraph is not the most pessimistic. A further deterioration of the sense signal occurs if the following pulse program is applied: a large number of one's each followed by disturbs in the one direction, is written and read from the bit; this is followed by a single zero, which is then disturbed in the one direction. This zero is then read out and the output voltage recorded. The mirror image of this program is then applied, and a one read out and recorded. The program is shown in Figure 20, and

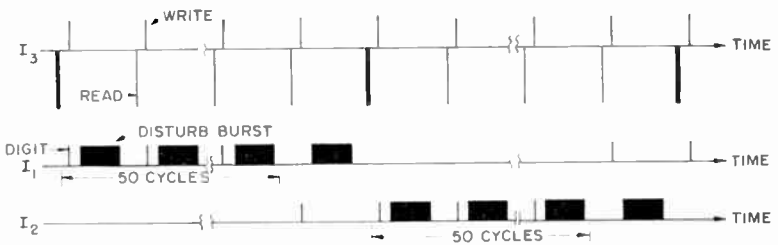


Fig. 20—Mixed one and zero with disturbs pulse program.

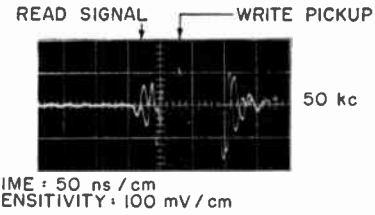


Fig. 21—Sense output voltages with 10 mc disturbs (pulse program of Figure 20).

Figure 21 shows oscillograms of the voltage developed at the sense output terminals for the same current levels as above. The sense voltages are ±5 mv. Comparing Figures 17, 19, and 21, a progressive decrease in output voltage is noted. It is felt that the pulse program of Figure 21 represents a sufficiently stringent test so that a memory array that yields the acceptable output of Figure 21 under the conditions of the test will perform satisfactorily in a computer under random conditions.

Uniformity of Fabricated Arrays

The uniformity of the electrical and magnetic characteristics of laminated arrays is obviously of importance in determining the feasibility of the fabrication process. The measured electrical resistances of $2 \times 16 = 32$ embedded conductors in a recently fabricated sample have a total variation of 0.2 ohm (15 conductors have a resistance of 0.7 ohm, 11 conductors have a resistance of 0.8 ohm, and the remaining 6 conductors have a resistance of 0.9 ohm). Figure 22 shows the superimposed sense output signals obtained from the same bit position in eight successive words. Approximately 80 per cent of the 128 bits in the array have acceptable outputs above a certain arbitrary minimum;

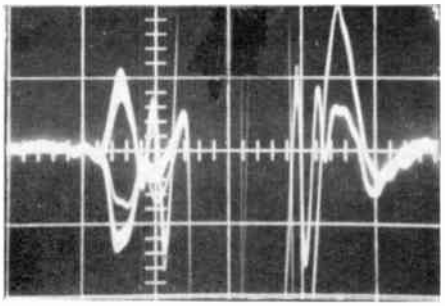


Fig. 22—Superimposed sense outputs from corresponding bit of eight words.

the remaining bits could possibly be used, but would present undue system difficulties. The nonuniformity in output is attributable entirely to a nonuniform conductor cross section, and reasonable care in the fabrication of the conductors should provide the required uniformity.

Propagation Characteristics of Sense-Digit Line

The experimentally determined characteristics of the sense-digit lines in a laminated array are

$$Z_0 = 200 \text{ ohms},$$
$$\alpha_{ac} = 5.7 \times 10^{-3} \text{ db/bit},$$
$$\alpha_{dc} = 1.2 \times 10^{-3} \text{ db/bit},$$
$$\tau_d = 3.3 \times 10^{-11} \text{ sec/bit}.$$

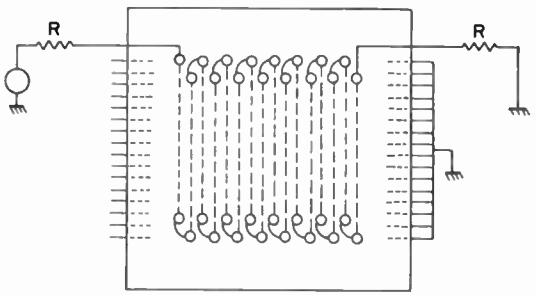


Fig. 23—Long bit sense digit line.

This data is obtained by propagating a pulse along a line consisting of the series connection of 16 sense-digit conductors in an array. The total embedded conductor length is 3.32 inches. This is equivalent to 332 bits spaced 10 mils apart. The 16 word conductors in the array are grounded as shown schematically in Figure 23. The characteristic impedance of the line is experimentally determined from the condition of minimum reflection. The delay per bit is computed from the total delay between the peak of the output pulse and that of the input pulse, shown in Figure 24, divided by 332, the number of equivalent bits on the line. The pulse attenuation is due to two factors—the attenuation α_{dc} due to the series d-c resistance of the line (measured value of 10 ohms), and α_{ac}, that due to the losses in the ferrite reflected as an equivalent a-c line resistance. It may be noted that the a-c losses exceed the d-c losses.

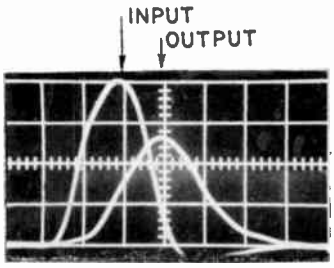


Fig. 24—Pulse propagation characteristics.

Future Developments

The fabrication techniques described are obviously applicable to the fabrication of a large class of ferrite devices and systems with integrated windings. The memory arrays fabricated and tested have not been especially optimized. For example, higher bit packing densities can be achieved quite readily. Figure 25 is an x-ray photograph of an array with 5-mil conductor spacing. The advantages to be gained from this tighter packing is a reduction in back voltages, in propagation delays, and in signal attenuation. A further decrease in bit spacing, down to a few mils is possible with the small cross-sectional conductor dimensions shown in Figure 7. The reduction in conductor cross section will result in a reduction in drive-current requirements without a deterioration in sense output. For memories of short word lengths, say 20 to 30 bits, a thicker ferrite laminate may be used to advantage to give higher sense outputs with correspondingly higher back voltages. Conversely, long words are readily realized by reducing the laminate thickness. This reduces both the sense output and signal attenuation.

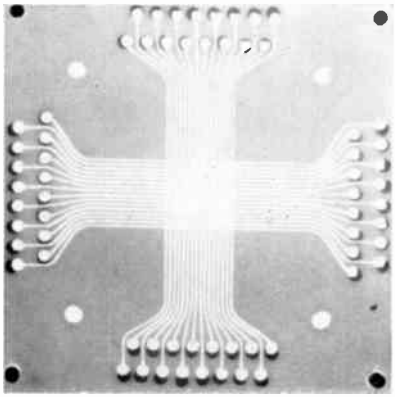


Fig. 25—X-ray of array with 5-mil conductor spacing.

For relatively low speed operation, say a one microsecond cycle time, the required drive currents are under 50 ma as has been experimentally verified. The sense output is approximately one millivolt. The low drive currents and the relatively high sense outputs are well matched to the capabilities of integrated electronic circuitry. Word drivers, triggered by address decoding trees, can be fabricated and assembled as integrated arrays. Similarly, integrated sense amplifiers may be built to detect the binary signals. The physical structure, and physical dimensions of laminated arrays are also well suited for interconnection to arrays of integrated semiconducting elements. Combining laminated arrays with integrated electronic circuitry promises to result in a substantial cost per bit reduction over the present state of the art. This in itself will make economical random-access ferrite memories with capacities in excess of 10^7 bits. The expected cycle time of these memories will be predominantly determined by the characteristics of the integrated semiconducting circuits and may conceivably be less than 0.5 microsecond.

Conclusions

The results presented in this paper show conclusively that the techniques described are well suited for the low-cost fabrication of memory arrays of micro size at exceptionally high packing densities. The physical and electrical characteristics of these arrays may be tailored to meet all important aspects of digital random-access memories, including high speed (100-nanosecond cycle), large capacities (in excess of 10^7 bits), nondestructive read-out, and wide temperature range operation. The drive requirements and sense outputs for these arrays as well as their ease of fabrication place them in a favorable position with respect to other integrated magnetic arrays, such as FLEA memories, twistor memories, thin magnetic film memories, and the waffle iron memory.

Acknowledgments

The authors wish to express their appreciation to their many colleagues at RCA Laboratories and the product divisions of RCA who were involved in this program. Bernard Schwartz, RCA Laboratories, suggested the basic ceramic techniques used for the fabrication of these memory arrays. The authors wish to express their appreciation to him for his help during the early phases of the work. Thanks are also due to R. Noack and A. Monsen, RCA Laboratories, who fabricated and wired many of the sample arrays.

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ALFRED MAYER obtained the B.S. degree with honors from the University of London, England, in 1946. He worked in the field of analytical chemistry and extraction metallurgy on a wide range of materials including iron, magnesium, zirconium, niobium, and tantalum. He joined the RCA Semiconductor and Materials Division in Somerville, N. J. in 1959 and has made contributions to the materials technology of gallium arsenide and silicon. For the past two years he has headed the Device Chemistry group at Somerville, working on surface studies and silicon and gallium arsenide epitaxy. Mr. Mayer is a member of the Electrochemical Society, a Fellow of the Royal Institute of Chemistry, and a member of the Institution for Metallurgists.

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